TEXAS INSTRUMENTS

TPA3116D2-Q1, TPA3118D2-Q1

SLOS862B – JULY 2015 – REVISED OCTOBER 2016

TPA311xD2-Q1 100-W and 50-W Class-D Stereo Automotive Amplifiers

1 Features

- Supports Multiple Output Configurations
  - 2 × 50 W Into a 4-Ω BTL Load at 21 V (TPA3116D2-Q1)
  - 2 × 30 W Into an 8-Ω BTL Load at 24 V (TPA3118D2-Q1)
- Wide Voltage Range: 4.5 V to 26 V
- Efficient Class-D Operation
  - >90% Power Efficiency Combined With Low Idle Loss Greatly Reduces Heat Sink Size
  - Advanced Modulation Schemes
- Multiple Switching Frequencies
  - AM Avoidance
  - Master and Slave Synchronization
  - Up to 1.2-MHz Switching Frequency
- Feedback Power-Stage Architecture With High PSRR Reduces PSU Requirements
- Programmable Power Limit
- Differential and Single-Ended Inputs
- Stereo BTL and Mono PBTL Modes
- Single Power Supply Reduces Component Count
- Integrated Self-Protection Circuits Including Overvoltage, Undervoltage, Overtemperature, DC-Detect, and Short Circuit With Error Reporting
- Designed for Automotive EMC Requirements
- Thermally Enhanced Packages
  - DAD (32-pin HTSSOP Pad Up)
  - DAP (32-pin HTSSOP Pad Down)
  - –40°C to 125°C Ambient Temperature Range
- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B

2 Applications

- Automotive Audio
- Emergency Call
- Driver Notifications

3 Description

The TPA311xD2-Q1 devices are automotive stereo, efficient, digital-amplifier power stages for driving speakers up to 100 W into 2 Ω in mono. The TPA3118D2-Q1 can even drive 2 × 30 W into 8 Ω without a heat sink on a dual-layer PCB. If even higher power is needed, the TPA3116D2-Q1 drives 2 × 50 W into 4 Ω with a small heat sink attached to its top-side thermal pad.

The TPA311xD2-Q1 advanced oscillator and PLL circuit employ a multiple-switching-frequency option to avoid AM interference; this is achieved together with an option of either master or slave selection, making it possible to synchronize multiple devices.

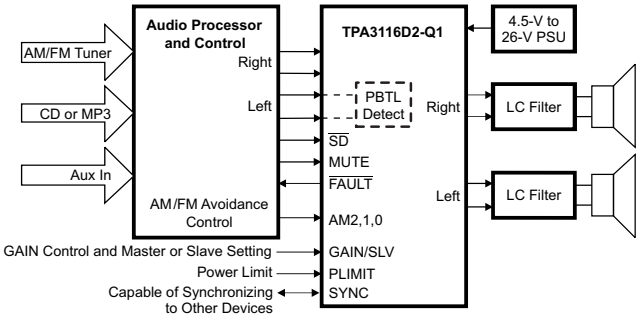
The TPA311xD2-Q1 devices are fully protected against faults with short-circuit protection and thermal protection as well as overvoltage, undervoltage and dc protection. Faults are reported back to the processor to prevent devices from being damaged during overload conditions.

Device Information(1)

DEVICE	PACKAGE	BODY SIZE (NOM)
TPA3116D2-Q1	HTSSOP (32)	11.00 mm × 6.20 mm
TPA3118D2-Q1		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision A (August 2015) to Revision B **Page**

- Changed Table 3, column R to GND From: Short To: Open and column R to GVDD From: Open To: Short ... 13
- Changed Figure 19 ... 19

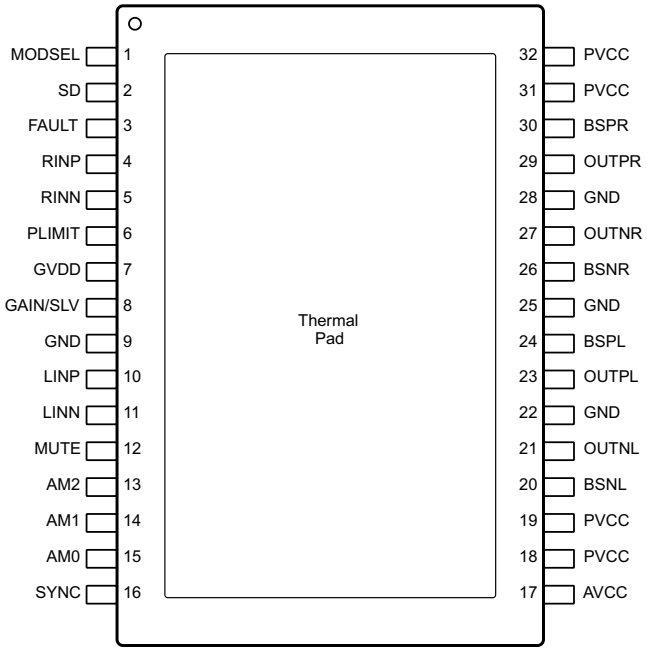
Changes from Original (July 2015) to Revision A **Page**

- Added all information following the pin description diagrams ... 4

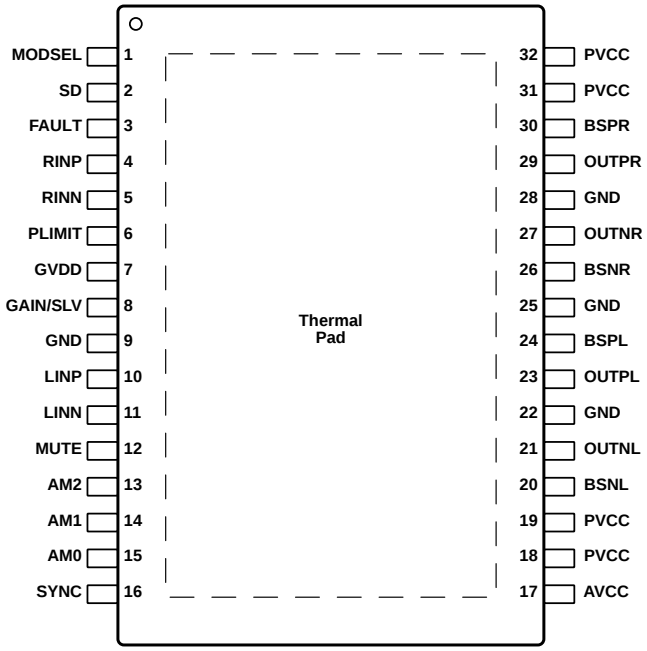
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5 Pin Configuration and Functions

DAD PowerPAD™ Package
32-Pin HTSSOP With Exposed Thermal Pad Up
TPA3116D2-Q1 Top View



DAP PowerPAD™ Package
32-Pin HTSSOP With Exposed Thermal Pad Down
TPA3118D2-Q1 Top View



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Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AM[2:0]	13–15	I	AM avoidance frequency selection
AVCC	17	P	Analog supply
BSNL	20	BST	Bootstrap for negative left channel output, connect to 220-nF X5R, or better ceramic cap to OUTPL
BSNR	26	BST	Bootstrap for negative right channel output, connect to 220-nF X5R, or better ceramic cap to OUTNR
BSPL	24	BST	Bootstrap for positive left channel output, connect to 220-nF X5R, or better ceramic cap to OUTNL
BSPR	30	BST	Bootstrap for positive right channel output, connect to 220-nF X5R or better ceramic cap to OUTPR
$\overline{\text{FAULT}}$	3	DO	General fault reporting including overtemperature, dc detect, open drain. $\overline{\text{FAULT}}$ = High, normal operation $\overline{\text{FAULT}}$ = Low, fault condition
GAIN/SLV	8	I	Selects gain and selects between master and slave modes depending on pin voltage divider.
GND	9, 22, 25, 28	G	Ground
GVDD	7	PO	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1-µF X7R ceramic decoupling capacitor and the PLIMIT and GAIN/SLV resistor dividers.
LINN	11	I	Negative audio input for left channel. Biased at 3 V. Connect to GND for PBTL mode.
LINP	10	I	Positive audio input for left channel. Biased at 3 V. Connect to GND for PBTL mode.
MODSEL	1	I	Mode selection logic input (LOW = BD mode, HIGH = 1 SPW mode). TTL logic levels with compliance to AVCC.
MUTE	12	I	Mute signal for fast disable or enable of outputs (HIGH = outputs Hi-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
OUTNL	21	PO	Negative left-channel output
OUTNR	27	PO	Negative right-channel output
OUTPL	23	PO	Positive left-channel output
OUTPR	29	PO	Positive right-channel output
PLIMIT	6	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
PVCC	18, 19, 31, 32	P	Power supply
RINN	5	I	Negative audio input for right channel. Biased at 3 V.
RINP	4	I	Positive audio input for right channel. Biased at 3 V.
$\overline{\text{SD}}$	2	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
SYNC	16	DIO	Clock input/output for synchronizing multiple class-D devices. Direction determined by GAIN/SLV pin.
Thermal pad	—	G	Connect to GND for best system performance. If not connected to GND, leave floating.

(1) **TYPE**: DO = Digital output, I = Analog input, G = General ground, PO = Power output, BST = Bootstrap.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}	PVCC, AVCC	–0.3	30	V
Input voltage, V_I	INPL, INNL, INPR, INNR	–0.3	6.3	V
	PLIMIT, GAIN/SLV, SYNC	–0.3	GVDD + 0.3	V
	AM0, AM1, AM2, MUTE, $\overline{SD}$, MODSEL	–0.3	PV_{CC} + 0.3	V
Slew rate, maximum(2)	AM0, AM1, AM2, MUTE, $\overline{SD}$, MODSEL		10	V/ms
Operating ambient temperature, T_A		–40	125	°C
Operating junction temperature range, T_J		–40	150	°C
Storage temperature range, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) 100-kΩ series resistor is needed if maximum slew rate is exceeded.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±450	
			Corner pins (1, 16, 17, and 32)	±450	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	4.5		26	V
V_{IH}	High-level input voltage	AM0, AM1, AM2, MUTE, $\overline{SD}$, SYNC, MODSEL	2			V
V_{IL}	Low-level input voltage	AM0, AM1, AM2, MUTE, $\overline{SD}$, SYNC, MODSEL			0.8	V
V_{OL}	Low-level output voltage	$\overline{FAULT}$, R_{PULLUP} = 100 kΩ, $V_{(PVCC)}$ = 26 V			0.8	V
I_{IH}	High-level input current	AM0, AM1, AM2, MUTE, $\overline{SD}$, MODSEL (V_I = 2 V, V_{CC} = 18 V)			50	µA
R_L	Minimum load impedance	Output filter: L = 10 µH, C = 680 nF, BTL	3.2	4		Ω
		Output filter: L = 10 µH, C = 1 µF, PBTL	1.6			
L_o	Output-filter inductance	Minimum output filter inductance under short-circuit condition	1			µH

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6.4 Thermal Information

THERMAL METRIC[1]		TPA3116D2-Q1 DAD 32 PINS	TPA3118D2-Q1 DAP 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.7[2]	32.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.2	17.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.5	17.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21	17.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Modeled with a 15-mm × 15-mm × 2-mm copper heat slug heat sink. A better heat sink or airflow would yield a much better $R_{\theta JA}$. Perfect heat sink results could be as low as $R_{\theta JC(top)}$ = 1.2 ºC/W.

6.5 DC Electrical Characteristics

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V, gain = 36 dB		1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load or filter, $V_{(PVCC)}$ = 12 V		20	35	mA
		$\overline{SD}$ = 2 V, no load or filter, $V_{(PVCC)}$ = 24 V		32	50	
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load or filter, $V_{(PVCC)}$ = 12 V		<50		µA
		$\overline{SD}$ = 0.8 V, no load or filter, $V_{(PVCC)}$ = 24 V		50	400	
$r_{DS(on)}$	Drain-source on-state resistance, measured pin-to-pin	$V_{(PVCC)}$ = 21 V, I_O = 500 mA, T_J = 25°C		120		mΩ
G	Gain (BTL)	R1 = open, R2 = 20 kΩ	19	20	21	dB
		R1 = 100 kΩ, R2 = 20 kΩ	25	26	27	
		R1 = 100 kΩ, R2 = 39 kΩ	31	32	33	dB
		R1 = 75 kΩ, R2 = 47 kΩ	35	36	37	
G	Gain (SLV)	R1 = 51 kΩ, R2 = 51 kΩ	19	20	21	dB
		R1 = 47 kΩ, R2 = 75 kΩ	25	26	27	
		R1 = 39 kΩ, R2 = 100 kΩ	31	32	33	dB
		R1 = 16 kΩ, R2 = 100 kΩ	35	36	37	
t_{on}	Turn-on time	$V_{(\overline{SD})}$ = 2 V		10		ms
t_{off}	Turn-off time	$V_{(\overline{SD})}$ = 0.8 V		2		µs
GVDD	Gate drive supply	$I_{(GVDD)}$ < 200 µA	6.4	6.9	7.4	V
V_O	Output voltage maximum under PLIMIT control	$V_{(PLIMIT)}$ = 2 V; V_I = 1 V_{rms}	6.75	7.9	8.75	V

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6.6 AC Electrical Characteristics

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
KSVR	Power supply ripple rejection	200 mV_{PP} ripple at 1 kHz, gain = 20 dB, inputs ac-coupled to GND		–70		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz, $V_{(PVCC)}$ = 14.4 V		25		W
		THD+N = 10%, f = 1 kHz, $V_{(PVCC)}$ = 21 V		50		
THD+N	Total harmonic distortion + noise	V_{CC} = 21 V, f = 1 kHz, P_O = 25 W (half-power)		0.1%		
Vn	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	V_O = 1 V_{rms}, gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency	AM[2:0] = 000	376	400	424	kHz
		AM[2:0] = 001	470	500	530	
		AM[2:0] = 010	564	600	636	
		AM[2:0] = 011	940	1000	1060	
		AM[2:0] = 100	1128	1200	1278	
		AM[2:0] = 101	Reserved			
		AM[2:0] = 110				
		AM[2:0] = 111				
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C
	Overcurrent trip point			7.5		A

6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
t_d	Delay from MUTE rising to $\overline{SD}$ falling	1.4			s

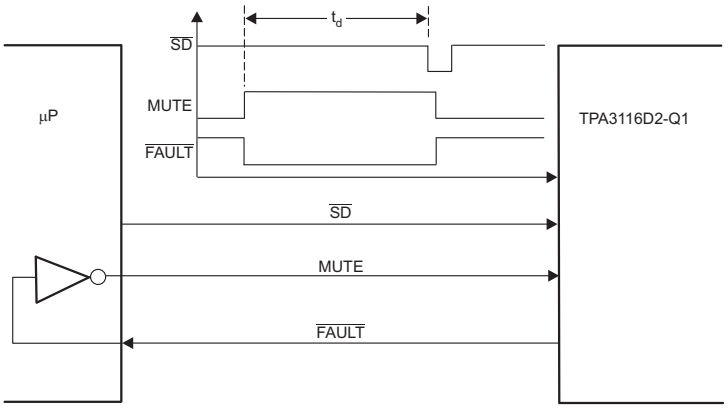
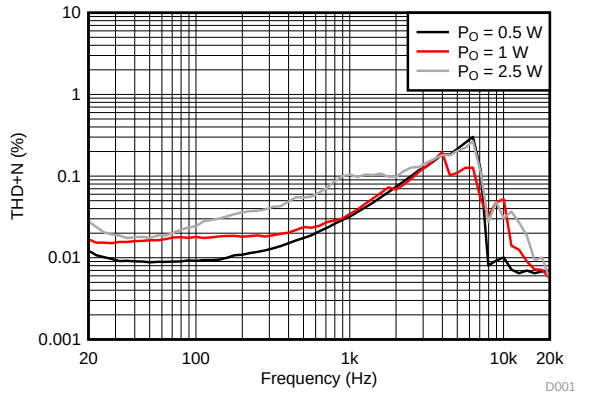


Figure 1. Timing Requirement for $\overline{SD}$

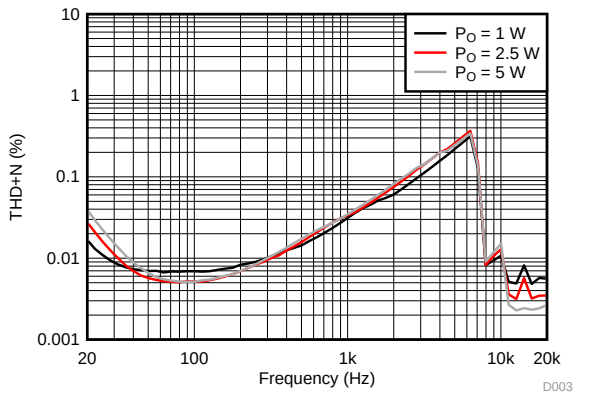
6.8 Typical Characteristics

f_s = 400 kHz, BD mode (unless otherwise noted)



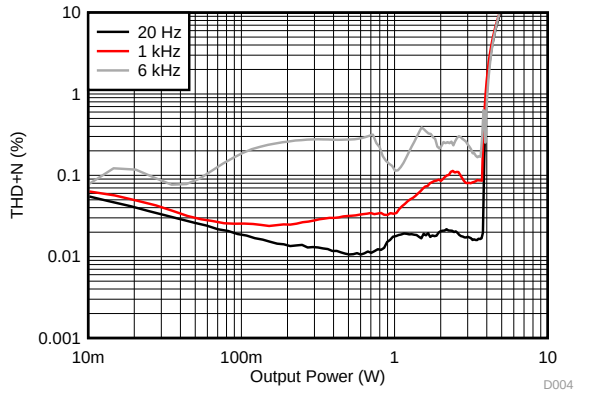
Gain = 26 dB PVCC = 6 V T_A = 25°C
R_L = 4 Ω 10-µH + 0.68-µF filter

Figure 2. Total Harmonic Distortion + Noise (BTL) vs Frequency



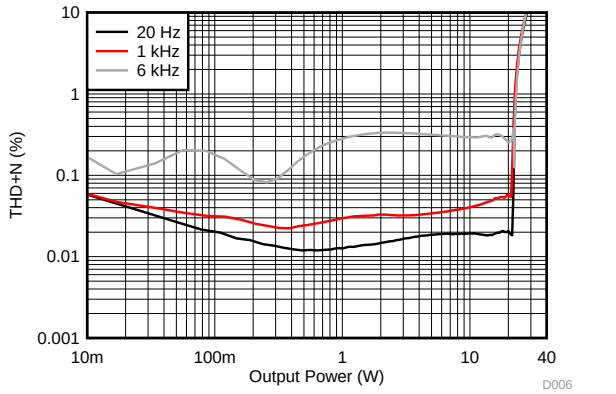
Gain = 26 dB PVCC = 14.4 V T_A = 25°C
R_L = 4 Ω 10-µH + 0.68-µF filter

Figure 3. Total Harmonic Distortion + Noise (BTL) vs Frequency



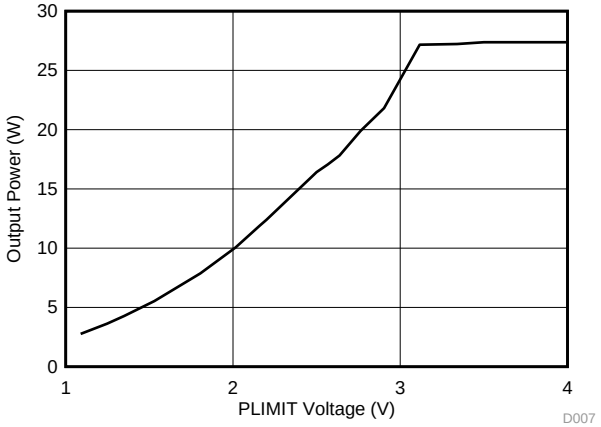
Gain = 26 dB PVCC = 6 V T_A = 25°C
R_L = 4 Ω 10-µH + 0.68-µF filter

Figure 4. Total Harmonic Distortion + Noise (BTL) vs Output Power



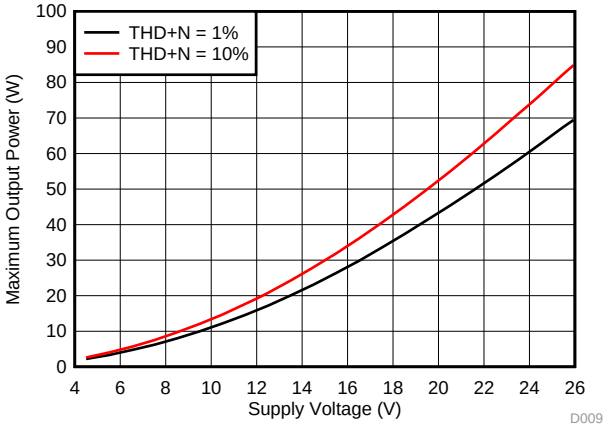
Gain = 26 dB PVCC = 14.4 V T_A = 25°C
R_L = 4 Ω 10-µH + 0.68-µF filter

Figure 5. Total Harmonic Distortion + Noise (BTL) vs Output Power



Gain = 26 dB PVCC = 14.4 V T_A = 25°C
R_L = 4 Ω 10-µH + 0.68-µF filter

Figure 6. Output Power (BTL) vs PLIMIT Voltage



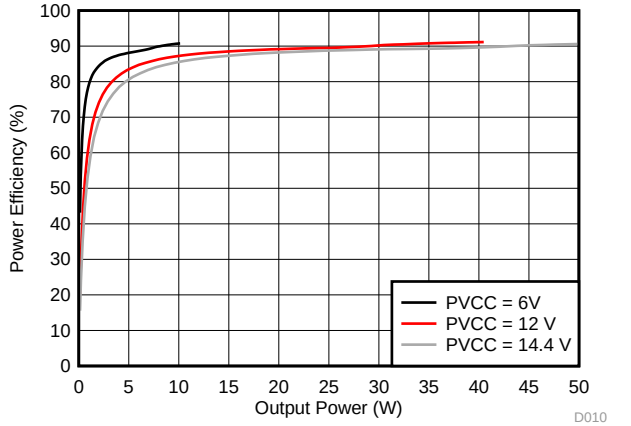
Gain = 26 dB T_A = 25°C R_L = 4 Ω
10-µH + 0.68-µF filter

Figure 7. Maximum Output Power (BTL) vs Supply Voltage

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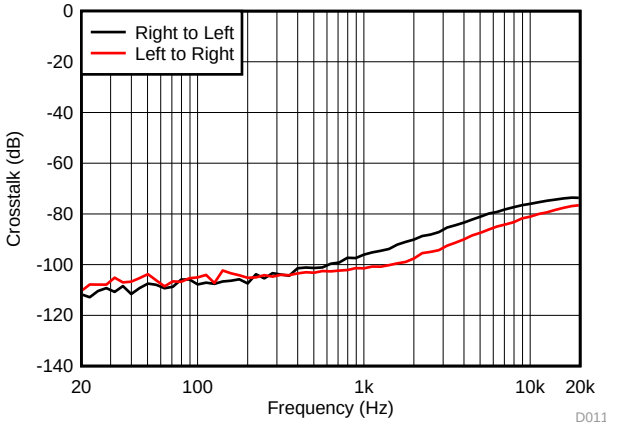
Typical Characteristics (continued)

f_s = 400 kHz, BD mode (unless otherwise noted)



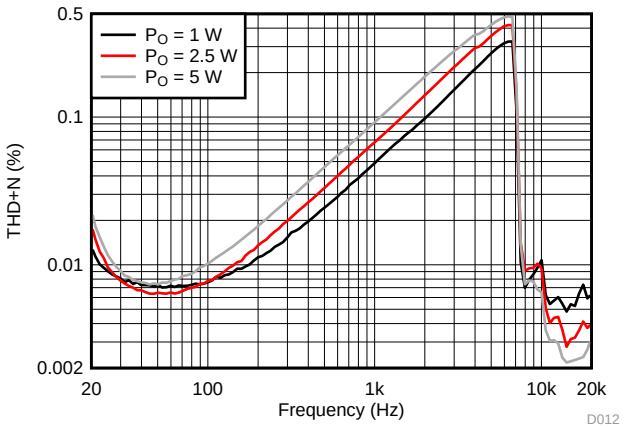
Gain = 26 dB T_A = 25°C R_L = 4 Ω
10-µH + 0.68-µF filter

Figure 8. Power Efficiency (BTL) vs Output Power



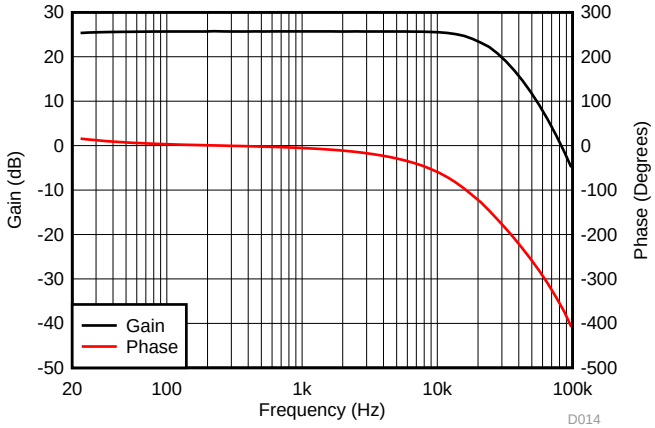
Gain = 26 dB PVCC = 12 V T_A = 25°C
R_L = 4 Ω 10-µH + 0.68-µF filter

Figure 9. Crosstalk vs Frequency



Gain = 26 dB PVCC = 14.4 V T_A = 25°C
R_L = 4 Ω 22-µH + 1-µF filter

Figure 10. Total Harmonic Distortion + Noise (BTL) vs Frequency



PVCC = 14.4 V T_A = 25°C R_L = 4 Ω
22-µH + 3.3-µF filter

Figure 11. Gain and Phase (BTL) vs Frequency

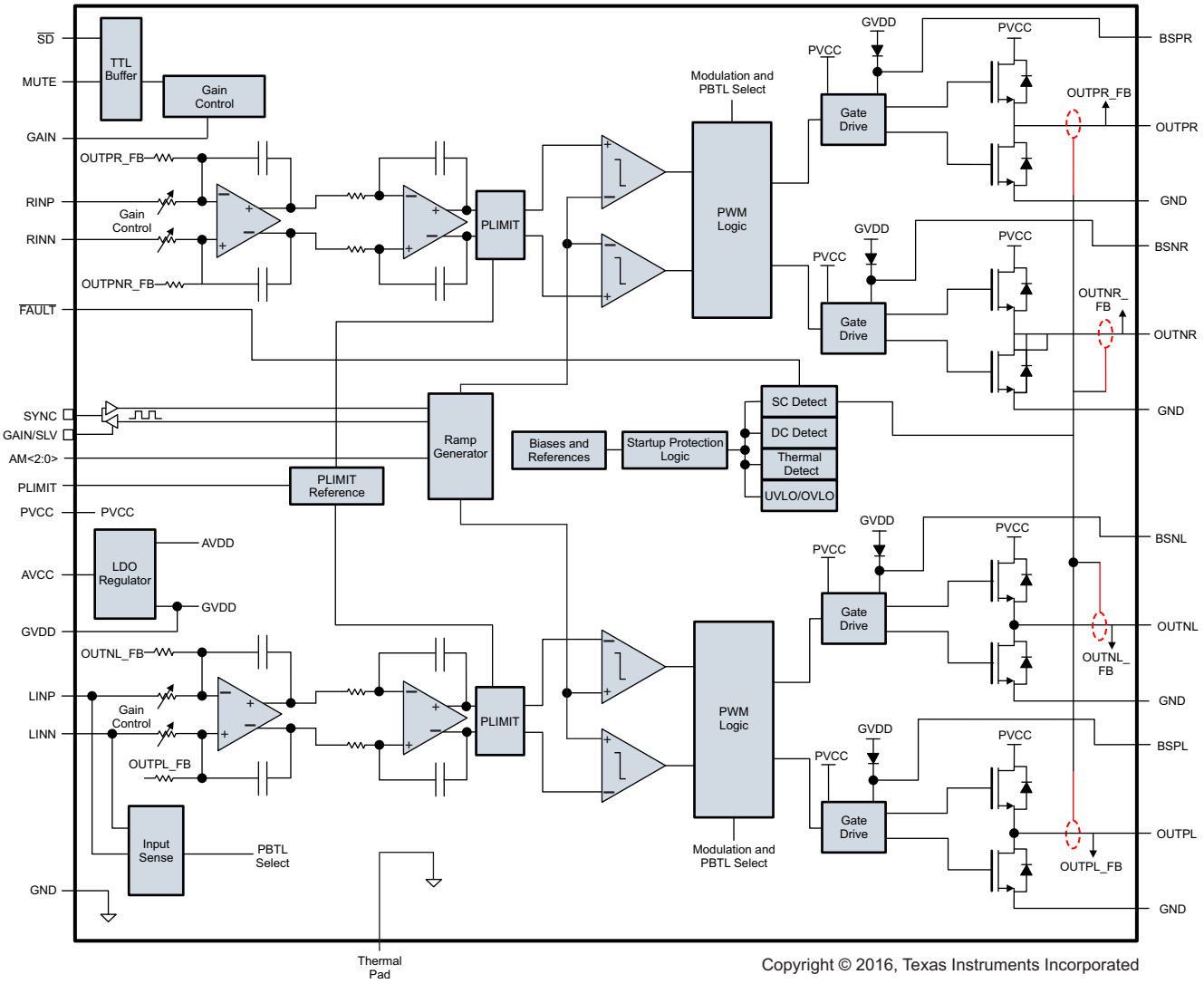
7 Detailed Description

7.1 Overview

The TPA311xD2-Q1 devices are highly efficient class-D audio amplifiers with integrated 120-mΩ MOSFETs that allow output currents up to 7.5 A. The high efficiency allows the amplifier to provide an excellent audio performance without the need for a bulky heat sink.

The device can be configured for either master or slave operation by using the SYNC pin. Doing so helps to prevent audible beat noise.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Gain Setting and Master and Slave

The gain of the TPA311xD2-Q1 family is set by the voltage divider connected to the GAIN/SLV control pin. Master or slave mode is also controlled by the same pin. An internal ADC is used to detect the eight input states. The first four stages set the GAIN in master mode to gains of 20, 26, 32, and 36 dB, respectively, whereas the next four stages set the GAIN in slave mode to gains of 20, 26, 32, and 36 dB, respectively. The gain setting is latched during power up and cannot be changed while device is powered. Table 1 lists the recommended resistor values and the state and gain.

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Table 1. Gain and Master or Slave

MASTER / SLAVE MODE	GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	26 dB	20 kΩ	100 kΩ	30 kΩ
Master	32 dB	39 kΩ	100 kΩ	15 kΩ
Master	36 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	26 dB	75 kΩ	47 kΩ	30 kΩ
Slave	32 dB	100 kΩ	39 kΩ	15 kΩ
Slave	36 dB	100 kΩ	16 kΩ	9 kΩ

(1) Resistor tolerance should be 5% or better.

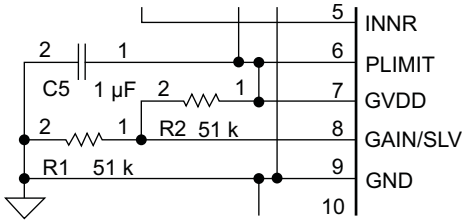


Figure 12. Gain, Master or Slave

In master mode, the SYNC terminal is an output, in slave mode, SYNC terminal is an input for a clock input.

7.3.2 Input Impedance

The input stage of the TPA311xD2-Q1 family is a fully differential input stage, and the input impedance changes with the gain setting from 9 kΩ at 36-dB gain to 60 kΩ at 20-dB gain. Table 1 lists the values from mininimum to maximum gain. The tolerance of the input resistor value is ±20%, so the minimum value is higher than 7.2 kΩ. The inputs must be ac-coupled to minimize the output dc offset and ensure correct ramping of the output voltages during power ON and power OFF. The input ac-coupling capacitor together with the input impedance forms a high-pass filter with the following cutoff frequency:

$$f = \frac{1}{2\pi Z_i C_i} \quad (1)$$

If a flat bass response is required down to 20 Hz, the recommended cutoff frequency is a tenth of that, 2 Hz. Table 2 lists the recommended ac-coupling capacitors for each gain step. If –3 dB is accepted at 20 Hz, 10 times lower capacitors can used – for example, a 1 µF can be used.

Table 2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 µF	1.8 Hz
26 dB	30 kΩ	3.3 µF	1.6 Hz
32 dB	15 kΩ	5.6 µF	2.3 Hz
36 dB	9 kΩ	10 µF	1.8 Hz

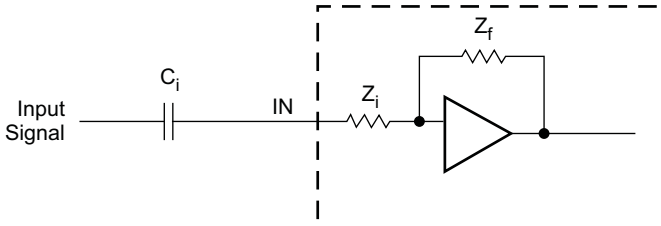


Figure 13. Input Impedance

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The input capacitors used should be a type with low leakage, like quality electrolytic, tantalum, or ceramic. If a polarized type is used, the positive connection should face the input pins, which are biased to 3 Vdc.

7.3.3 Start-Up and Shutdown Operation

The TPA311xD2-Q1 family employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level for power conservation during periods of nonuse. The $\overline{SD}$ input pin should be held high (see *Recommended Operating Conditions* for $\overline{SD}$ V_{IH} and V_{IL} levels) during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low sets the outputs to mute, and the amplifier enters a low-current state. It is not recommended to leave $\overline{SD}$ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply. The gain setting is selected at the end of the start-up cycle. At the end of the start-up cycle, the gain is selected and cannot be changed until the next power up.

7.3.4 PLIMIT Operation

The TPA311xD2-Q1 family has a built-in voltage limiter that can be used to limit the output voltage level below the supply rail, the amplifier simply operates as if it was powered by a lower supply voltage, and thereby limits the output power. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Add a 1-µF capacitor from the PLIMIT pin to ground to ensure stability. It is recommended to connect PLIMIT to GVDD when using 1SPW-modulation mode.

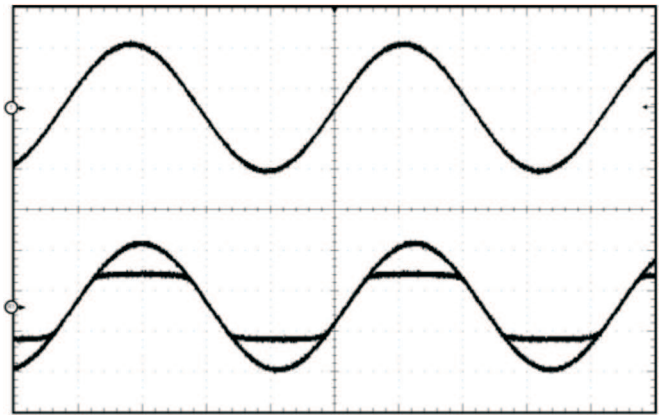


Figure 14. Power Limit Example

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to a fixed maximum value. This limit can be thought of as a *virtual* voltage rail which is lower than the supply connected to PVCC. This virtual rail is approximately 4 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power} \tag{2}$$

where

- P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)
- R_L is the load resistance.
- R_S is the total series resistance including $R_{DS(on)}$ and output filter resistance.
- V_P is the peak amplitude
- V_P = 4 × PLIMIT voltage if PLIMIT < 4 × V_P

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Table 3. Power Limit Example

PV_{CC} (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT VOLTAGE (V_{rms})
24 V	GVDD	Open	Short	17.9
24 V	3.3	45 kΩ	51 kΩ	12.67
24 V	2.25	24 kΩ	51 kΩ	9
12 V	GVDD	Open	Short	10.33
12 V	2.25	24 kΩ	51 kΩ	9
12 V	1.5	18 kΩ	68 kΩ	6.3

(1) PLIMIT measurements taken with EVM gain set to 26 dB and input voltage set to 1 V_{rms}.

7.3.5 GVDD Supply

The GVDD supply is used to power the gates of the output full-bridge transistors. The GVDD supply can also be used to supply the PLIMIT and GAIN/SLV voltage dividers. Decouple GVDD with an X5R ceramic 1-µF capacitor to GND. The GVDD supply is not intended to be used for external supply. It is recommended to limit the current consumption by using resistor voltage dividers of 100 kΩ or more for GAIN/SLV and PLIMIT.

7.3.6 BSPx and BSNx Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, to turn on correctly they require bootstrap capacitors for the high side of each output. A 220-nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to its corresponding bootstrap input. (See the application circuit diagram in Figure 19.) The bootstrap capacitors connected between the BSxx pins and their corresponding outputs function as a floating power supply for the high-side N-channel power MOSFET gate-drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

7.3.7 Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA311xD2-Q1 family with a differential source, connect the positive lead of the audio source to the RINP or LINP input and the negative lead from the audio source to the RINN or LINN input. To use the TPA311xD2-Q1 family with a single-ended source, ac-ground the negative input through a capacitor equal in value to the input capacitor on the positive input and apply the audio source to either input. In a single-ended input application, the unused input should be ac-grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc-blocking capacitors to become completely charged during the 10-ms power-up time. If the input capacitors are not allowed to completely charge, there is some additional sensitivity to component matching which can result in a pop if the input components are not well matched.

7.3.8 Device Protection System

The TPA311xD2-Q1 family contains a complete set of protection circuits to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, overtemperature, and undervoltage. The $\overline{\text{FAULT}}$ pin signals if an error is detected according to Table 4:

Table 4. Fault Reporting

FAULT	TRIGGERING CONDITION (typical value)	$\overline{\text{FAULT}}$	ACTION	LATCHED OR SELF-CLEARING
Overcurrent	Output short or short to PVCC or GND	Low	Output high impedance	Latched
Overtemperature	T_j > 150°C	Low	Output high impedance	Latched
Too-high dc offset	DC output voltage	Low	Output high impedance	Latched
Undervoltage on PVCC	$V_{(PVCC)}$ < 4.5 V	–	Output high impedance	Self-clearing
Overvoltage on PVCC	$V_{(PVCC)}$ > 27 V	–	Output high impedance	Self-clearing

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7.3.9 DC-Detect Protection

The TPA311xD2-Q1 family has circuitry which protects the speakers from dc current, which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A dc-detect fault is reported on the $\overline{\text{FAULT}}$ pin as a low state. The dc-detect fault also causes the amplifier to shut down by changing the state of the outputs to Hi-Z.

If automatic recovery from the short-circuit protection latch is desired, connect the $\overline{\text{FAULT}}$ pin directly to the $\overline{\text{SD}}$ pin. This allows the $\overline{\text{FAULT}}$ pin function to automatically drive the $\overline{\text{SD}}$ pin low which clears the dc-detect protection latch.

A dc-detect fault is issued when the output differential duty-cycle of either channel exceeds 60% for more than 420 ms at the same polarity. For several values of the supply voltage, Table 5 shows some examples of the typical output offset voltages that trigger dc-detect protection. This feature protects the speaker from large dc currents or ac currents less than 2 Hz. To avoid nuisance faults due to the dc-detect circuit, hold the $\overline{\text{SD}}$ pin low at power up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance dc-detect faults.

Table 5 lists the minimum output offset voltages required to trigger the dc detect. The outputs must remain at or above the voltage listed in the table for more than 420 ms to trigger the dc detect.

Table 5. DC Detect Threshold

$V_{(PVCC)}$ (V)	V_{OS} - OUTPUT OFFSET VOLTAGE (V)
4.5	0.96
6	1.3
12	2.6
18	3.9

7.3.10 Short-Circuit Protection and Automatic Recovery Feature

The TPA311xD2-Q1 family has protection from overcurrent conditions caused by a short circuit on the output stage. The short-circuit protection fault is reported on the $\overline{\text{FAULT}}$ pin as a low state. The amplifier outputs are switched to a high-impedance state when the short-circuit protection latch is engaged. The latch can be cleared by cycling the $\overline{\text{SD}}$ pin through the low state.

If automatic recovery from the short-circuit protection latch is desired, connect the $\overline{\text{FAULT}}$ pin directly to the $\overline{\text{SD}}$ pin. This allows the $\overline{\text{FAULT}}$ pin function to automatically drive the $\overline{\text{SD}}$ pin low, which clears the short-circuit protection latch.

In systems where a possibility of a permanent short from the output to PVDD or to a high-voltage battery like a car battery can occur, pull the MUTE pin low with the $\overline{\text{FAULT}}$ signal and an inverting transistor to ensure a high-Z restart, as shown in Figure 15.

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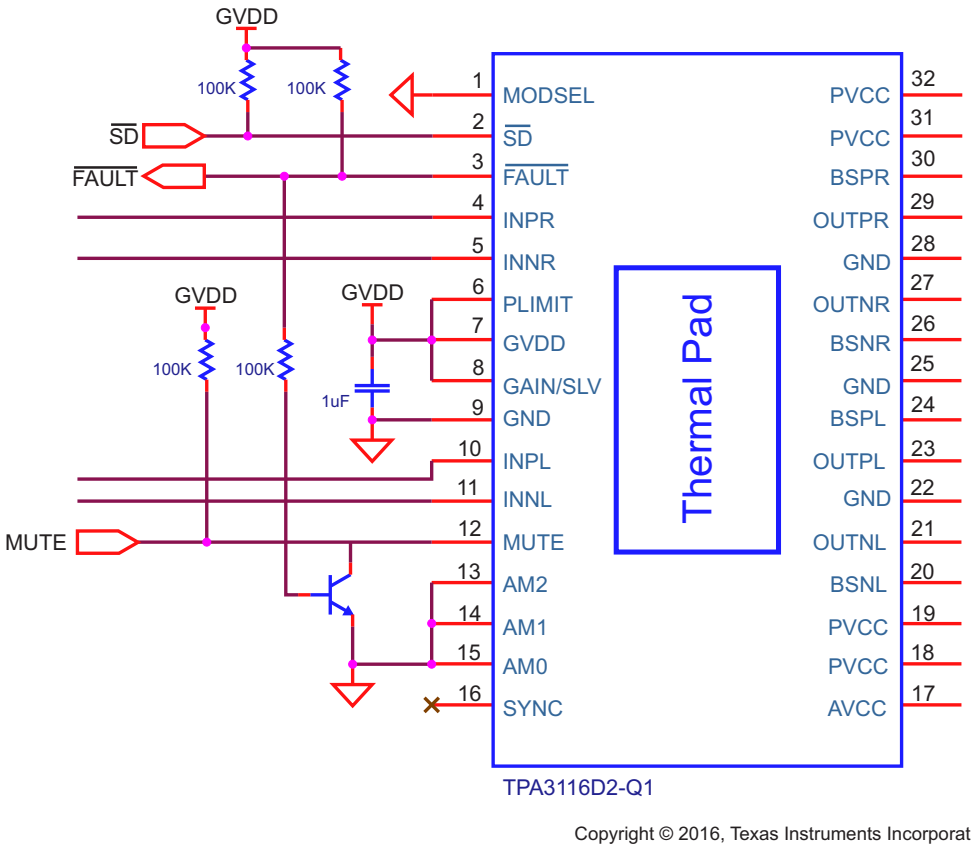


Figure 15. MUTE Driven by Inverted $\overline{\text{FAULT}}$

7.3.11 Thermal Protection

Thermal protection on the TPA311xD2-Q1 family prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal trip point, the device enters the shutdown state and the outputs are disabled. This is a latched fault.

Thermal protection faults are reported on the $\overline{\text{FAULT}}$ pin as a low state.

If automatic recovery from the thermal protection latch is desired, connect the $\overline{\text{FAULT}}$ pin directly to the $\overline{\text{SD}}$ pin. This allows the $\overline{\text{FAULT}}$ pin function to automatically drive the $\overline{\text{SD}}$ pin low, which clears the thermal protection latch.

7.3.12 TPA311xD2-Q1 Modulation Scheme

The TPA311xD2-Q1 family has the option of running in either BD modulation or 1SPW modulation; this is set by the MODSEL pin.

7.3.12.1 MODSEL = GND: BD Modulation

Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

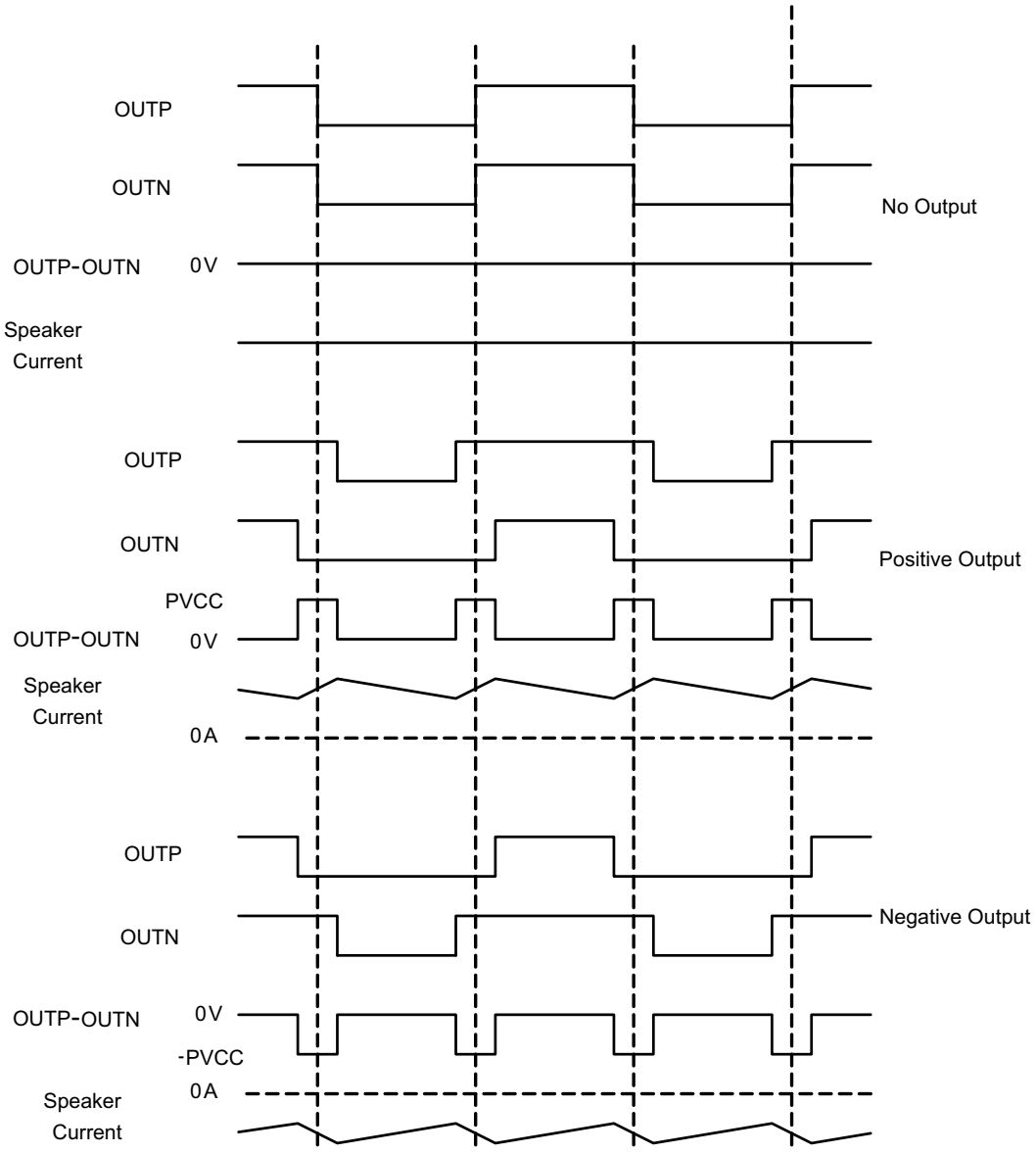


Figure 16. BD Mode Modulation

7.3.12.2 MODSEL = HIGH: 1SPW Modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation, and more attention required in the output filter selection. In 1SPW mode, the outputs operate at approximately 15% modulation during idle conditions. When an audio signal is applied, one output decreases and one increases. The decreasing output signal quickly rails to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses. The THD penalty in 1SPW mode is minimized by the high-performance feedback loop. The resulting audio signal at each half-output has a discontinuity each time the output rails to GND. This can cause ringing in the audio reconstruction filter unless care is taken in the selection of the filter components and type of filter used.

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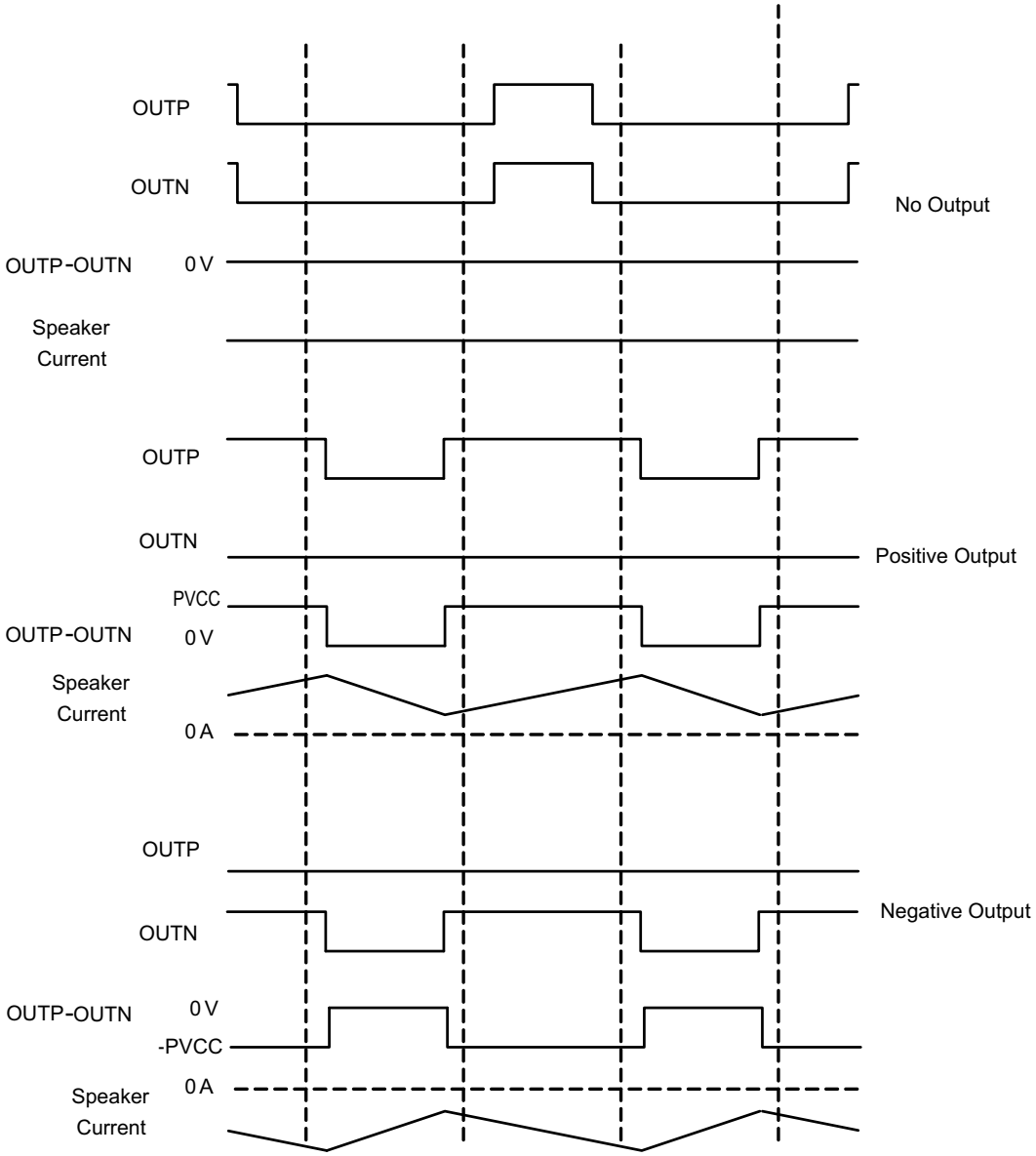


Figure 17. 1SPW Mode Modulation

7.3.13 AM Avoidance EMI Reduction

To reduce interference in the AM radio band, the TPA3116D2-Q1 has the ability to change the switching frequency via the AM[2:0] pins. The recommended frequencies are listed in Table 6. The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to the switching frequency being demodulated by the AM radio.

Table 6. AM Frequencies

US	EUROPEAN				
AM FREQUENCY (kHz)	AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)	AM2	AM1	AM0
	522–540				
540–917	540–914	500	0	0	1
917–1125	914–1122	600 (or 400)	0 0	1 0	0 0
1125–1375	1122–1373	500	0	0	1
1375–1547	1373–1548	600 (or 400)	0 0	1 0	0 0
1547–1700	1548–1701	600 (or 500)	0 0	1 0	0 1

7.4 Device Functional Mode

7.4.1 Mono Mode (PBTL)

The TPA311xD2-Q1 family can be connected in MONO mode enabling up to 100-W output power. This is done by:

- Connecting INPL and INNL directly to ground (without capacitors) to set the device in mono mode during power up
- Connecting OUTPR and OUTNR together for the positive speaker terminal and OUTNL and OUTPL together for the negative terminal
- Applying the analog input signal to INPR and INNR

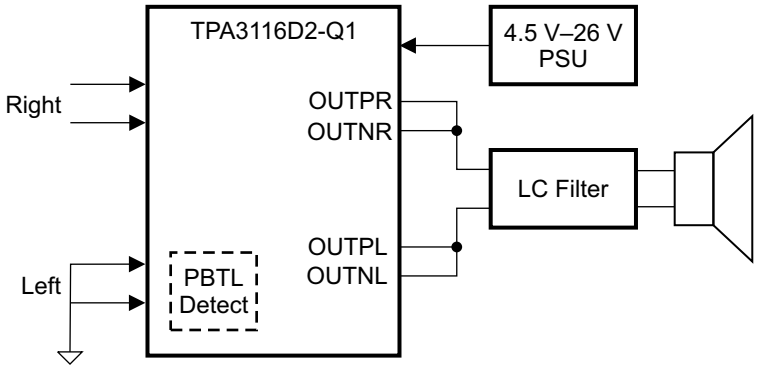


Figure 18. Mono Mode (PBTL)

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

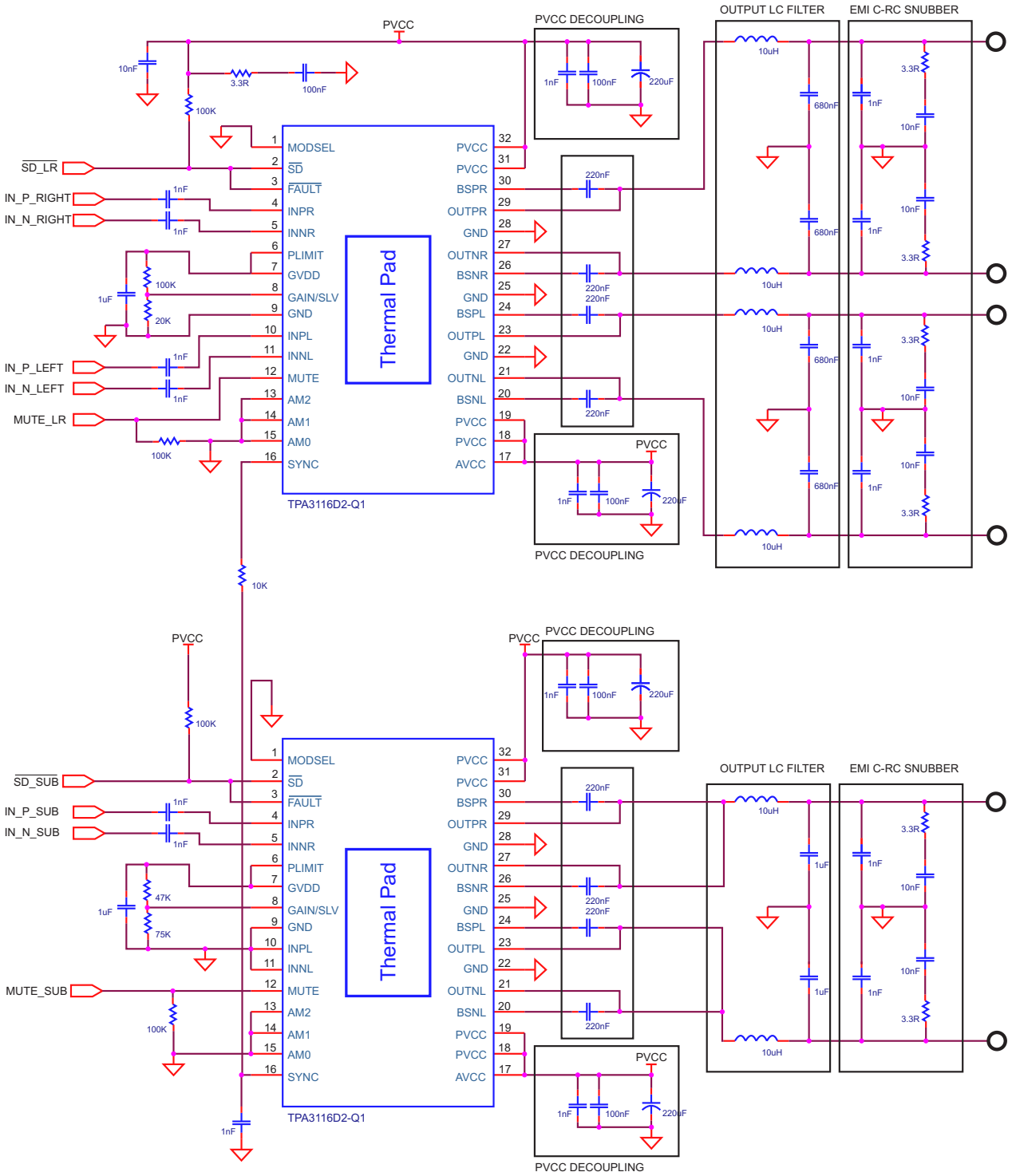
This section describes a 2.1 master-and-slave application. The master is configured as stereo outputs and the slave is configured as a mono PBTL output.

8.2 Typical Application

A 2.1 solution, U1 TPA3116D2-Q1 in master mode 400 kHz, BTL, gain if 20 dB, power limit not implemented. U2 in Slave, PBTL mode gain of 20 dB. Inputs are connected for differential inputs.

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Typical Application (continued)



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Figure 19. Typical Application Schematic

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Typical Application (continued)

8.2.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range, $V_{(PVCC)}$	4.5 V to 26 V
PWM output frequencies	400 kHz, 500 kHz, 600 kHz, 1 MHz or 1.2 MHz
Maximum output power	50 W

8.2.2 Detailed Design Procedure

The TPA311xD2-Q1 family is a very flexible and easy-to-use class-D amplifier; therefore, the design process is straightforward. Before beginning the design, gather the following information regarding the audio system.

- PVCC rail planned for the design
- Speaker or load impedance
- Maximum output-power requirement
- Desired PWM frequency

8.2.2.1 Select the PWM Frequency

Set the PWM frequency by using AM0, AM1 and AM2 pins.

8.2.2.2 Select the Amplifier Gain and Master or Slave Mode

In order to select the amplifier gain setting, the designer must determine the maximum power target and the speaker impedance. Once these parameters have been determined, calculate the required output-voltage swing which delivers the maximum output power.

Choose the lowest analog gain setting that produces an output-voltage swing greater than the required output swing for maximum power. The analog gain and master or slave mode can be set by selecting the voltage divider resistors (R1 and R2) on the GAIN/SLV pin.

8.2.2.3 Select Input Capacitance

Select the bulk capacitors at the PVCC inputs for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well-designed power supply, two 100-μF, 50-V capacitors should be sufficient. One capacitor should be placed near the PVCC inputs at each side of the device. PVCC capacitors should be a low-ESR type because they are being used in a high-speed switching application.

8.2.2.4 Select Decoupling Capacitors

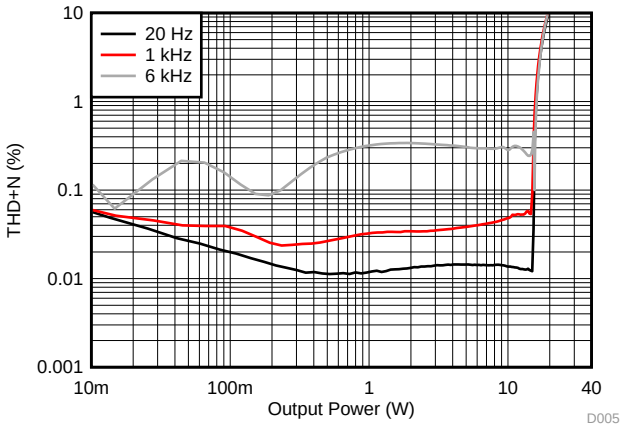
Good-quality decoupling capacitors must be added at each of the PVCC inputs to provide good reliability, good audio performance, and to meet regulatory requirements. X5R or better ratings should be used in this application. Consider temperature, ripple current, and voltage overshoots when selecting decoupling capacitors. Also, these decoupling capacitors should be located near the PVCC and GND connections to the device in order to minimize series inductances.

8.2.2.5 Select Bootstrap Capacitors

Each of the outputs requires bootstrap capacitors to provide gate drive for the high-side output FETs. For this design, use 0.22-μF, 25-V capacitors of X5R quality or better.

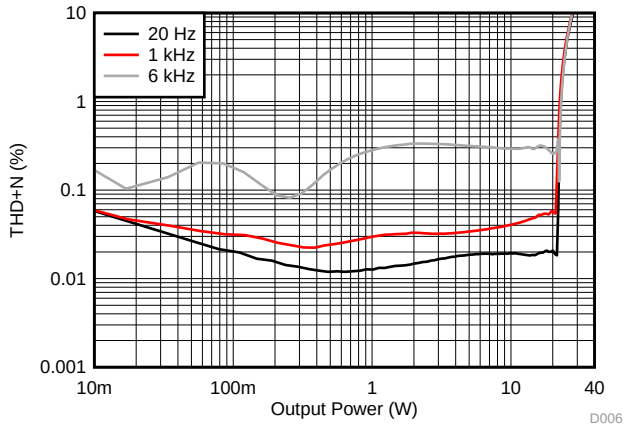
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8.2.3 Application Curves



Gain = 26 dB PVCC = 12 V T_A = 25°C
R_L = 4 Ω 10-µH + 0.68-µF filter

Figure 20. Total Harmonic Distortion + Noise (BTL) vs Output Power



Gain = 26 dB PVCC = 14.4 V T_A = 25°C
R_L = 4 Ω 10-µH + 0.68-µF filte

Figure 21. Total Harmonic Distortion + Noise (BTL) vs Output Power

9 Power Supply Recommendations

The power supply requirements for the TPA3116D2-Q1 consist of one higher-voltage supply to power the output stage of the speaker amplifier. Several on-chip regulators are included on the TPA3116D2-Q1 to generate the voltages necessary for the internal circuitry of the audio path. It is important to note that the voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. The high-voltage supply, between 4.5 V and 26 V, supplies the analog circuitry (AVCC) and the power stage (PVCC). The AVCC supply feeds the internal LDOs, including GVDD. The LDO outputs are connected to external pins for filtering purposes, but should not be connected to external circuits. The GVDD LDO output has been sized to provide current necessary for internal functions but not for external loading.

10 Layout

10.1 Layout Guidelines

Because the class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions help to meet EMC requirements.

- Decoupling capacitors — The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (100 µF or greater) bulk power supply decoupling capacitors should be placed near the TPA3116D2-Q1 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These capacitors can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good-quality, low-ESR ceramic capacitor between 220 pF and 1 nF and a larger mid-frequency capacitor of value between 100 nF and 1 µF, also of good quality, to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the filter and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding — The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the TPA3116D2-Q1.
- Output filter — The LC filter should be placed close to the outputs. The capacitor used in the LC filter should be grounded.

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Layout Guidelines (continued)

For an example layout, see the TPA3116D2 Evaluation Module (TPA3116D2EVM) User Guide (SLOU336). Both the EVM user manual and the thermal pad application reports, SLMA002 and SLMA004, are available on the TI Web site at http://www.ti.com.

10.2 Layout Example

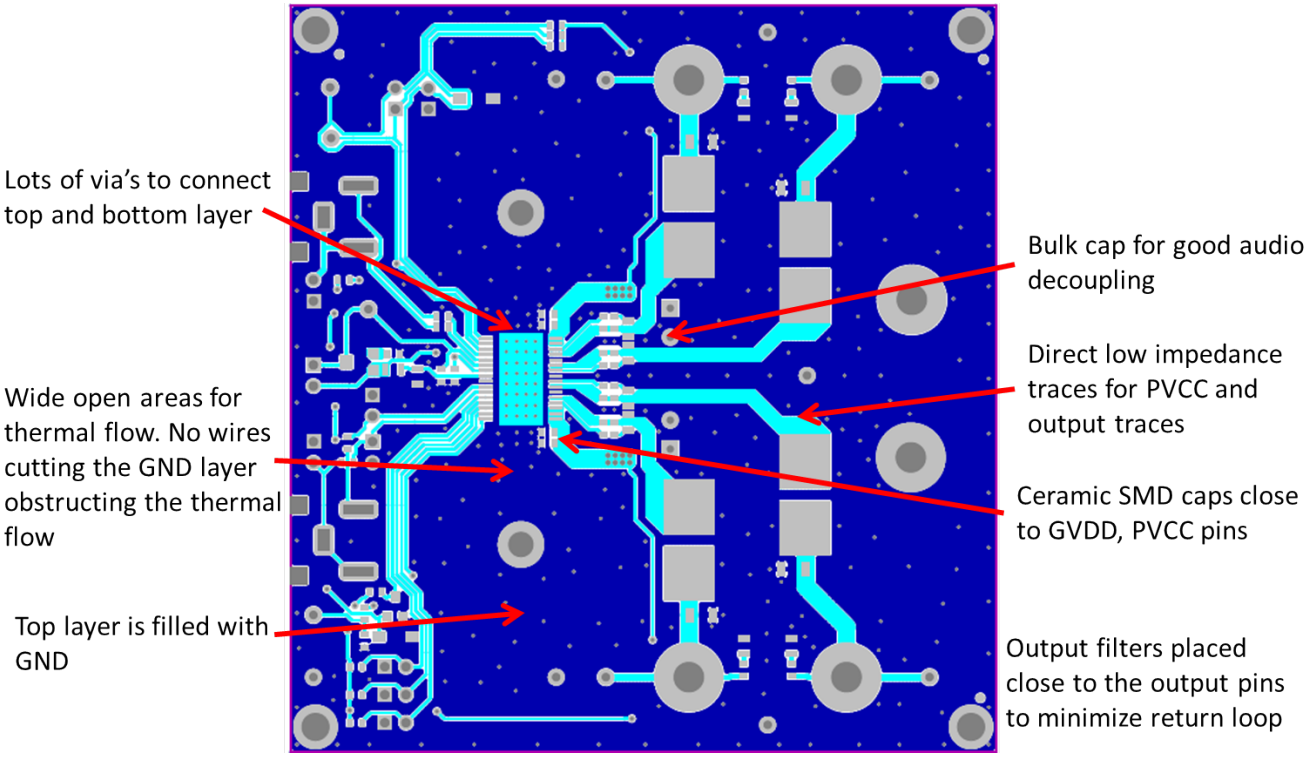


Figure 22. Layout Example Top

Layout Example (continued)

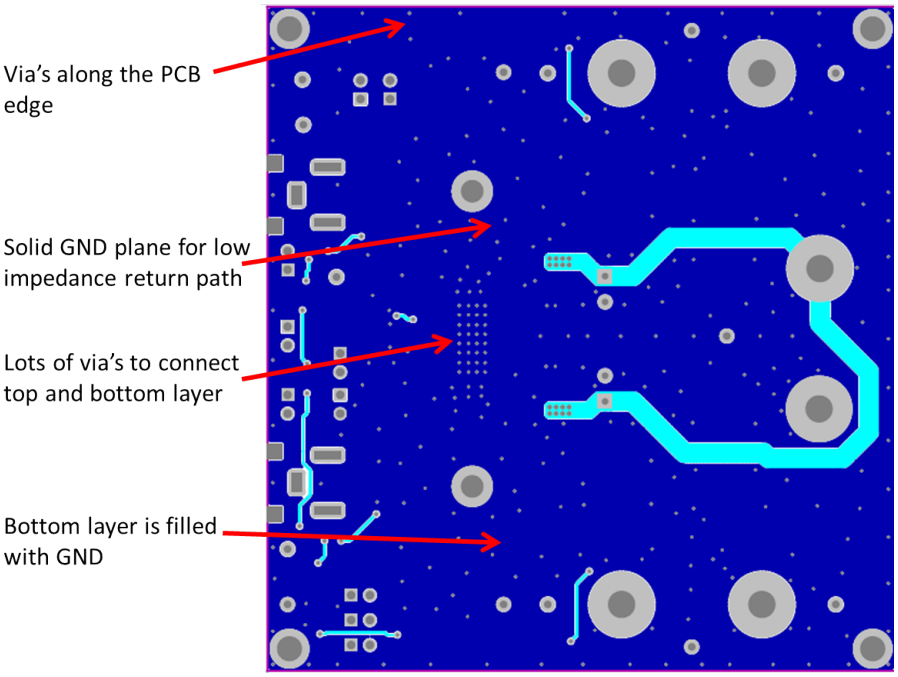


Figure 23. Layout Example Bottom

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10.3 Heat Sink Used on the EVM

The heat sink (part number ATS-TI 10 OP-521-C1-R1 or equivalent) used on the EVM is a 14-mm × 25-mm × 50-mm extruded aluminum heat sink with three fins (see Figure 24). For additional information on the heat sink, go to www.qats.com.

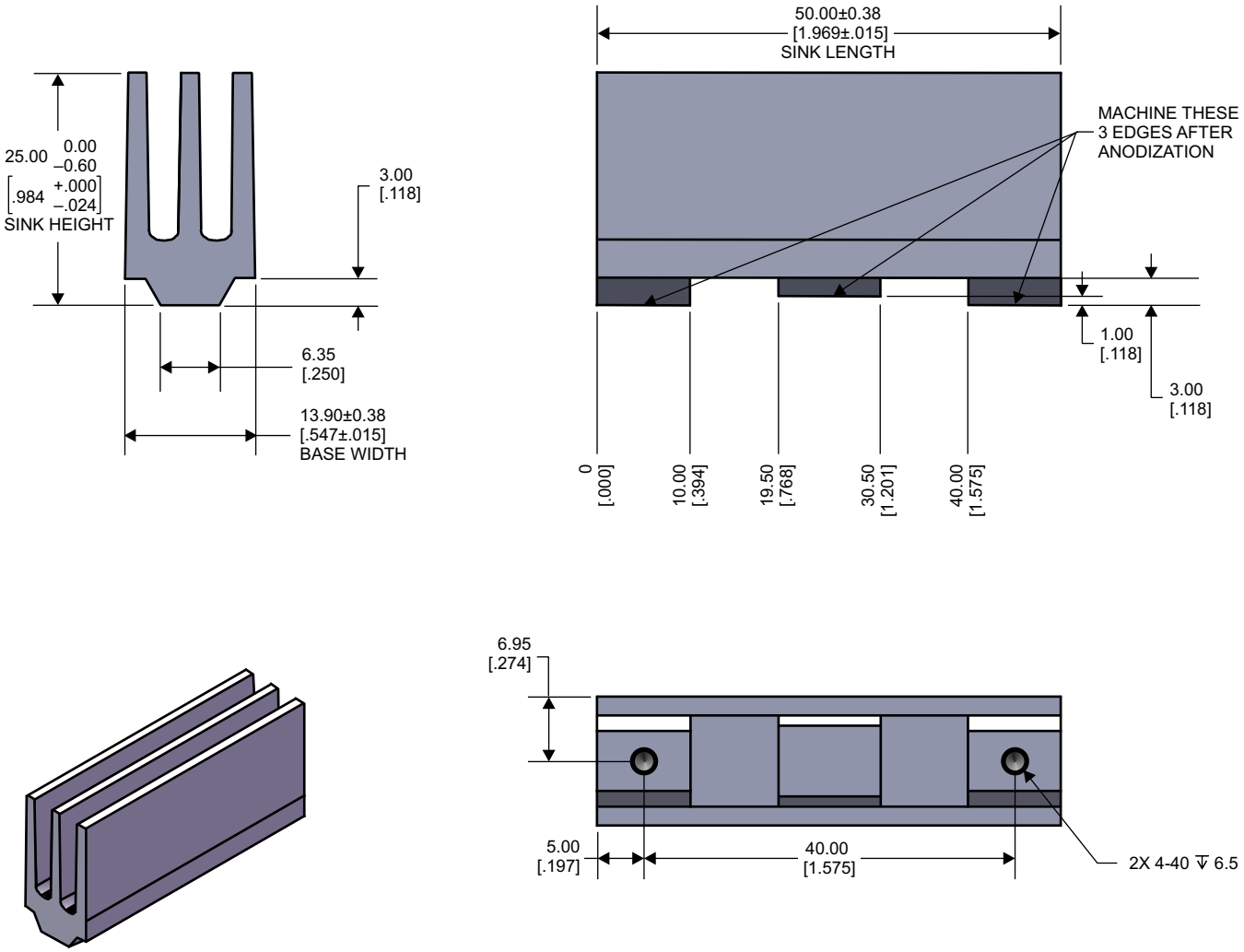


Figure 24. EVM Heatsink

This size heat sink has shown to be sufficient for continuous output power. The crest factor of music and having airflow lowers the requirement for heat sinking, and smaller types of heat sinks can be used.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPA3116D2-Q1	Click here	Click here	Click here	Click here	Click here
TPA3118D2-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA3116D2QDADRQ1	ACTIVE	HTSSOP	DAD	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPA 3116Q D2	Samples
TPA3118D2QDAPRQ1	ACTIVE	HTSSOP	DAP	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPA3118Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPA3116D2-Q1, TPA3118D2-Q1 :

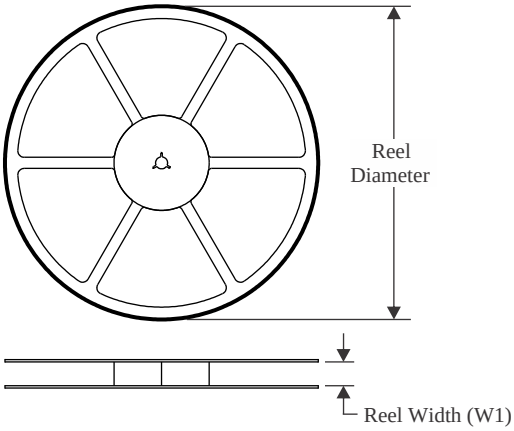
- Catalog: TPA3116D2, TPA3118D2

NOTE: Qualified Version Definitions:

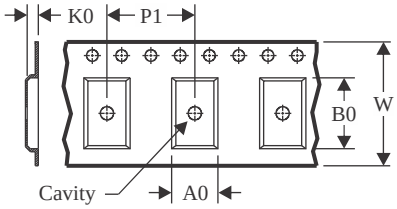
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

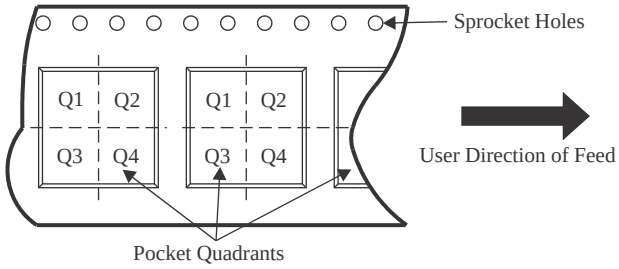


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

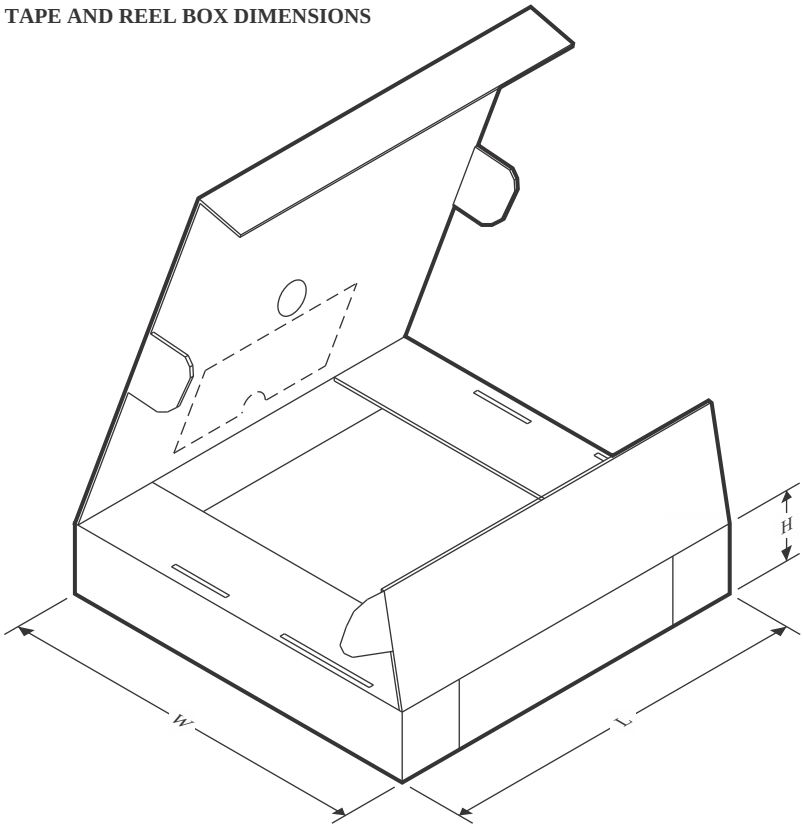
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3116D2QDADRQ1	HTSSOP	DAD	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TPA3118D2QDAPRQ1	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

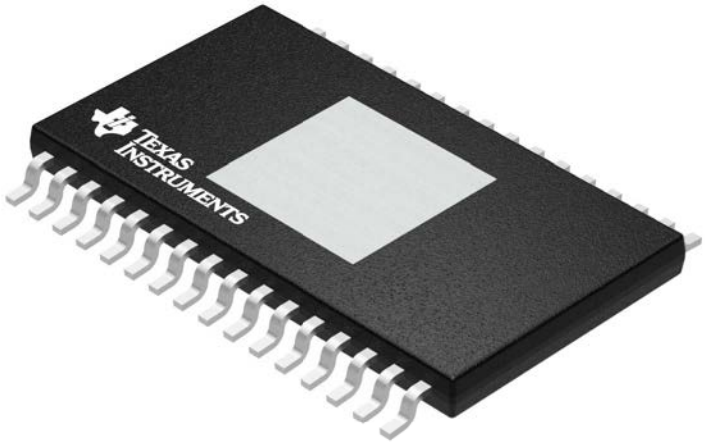


*All dimensions are nominal

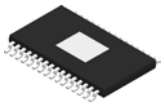
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3116D2QDADRQ1	HTSSOP	DAD	32	2000	350.0	350.0	43.0
TPA3118D2QDAPRQ1	HTSSOP	DAP	32	2000	350.0	350.0	43.0

DAD 32 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

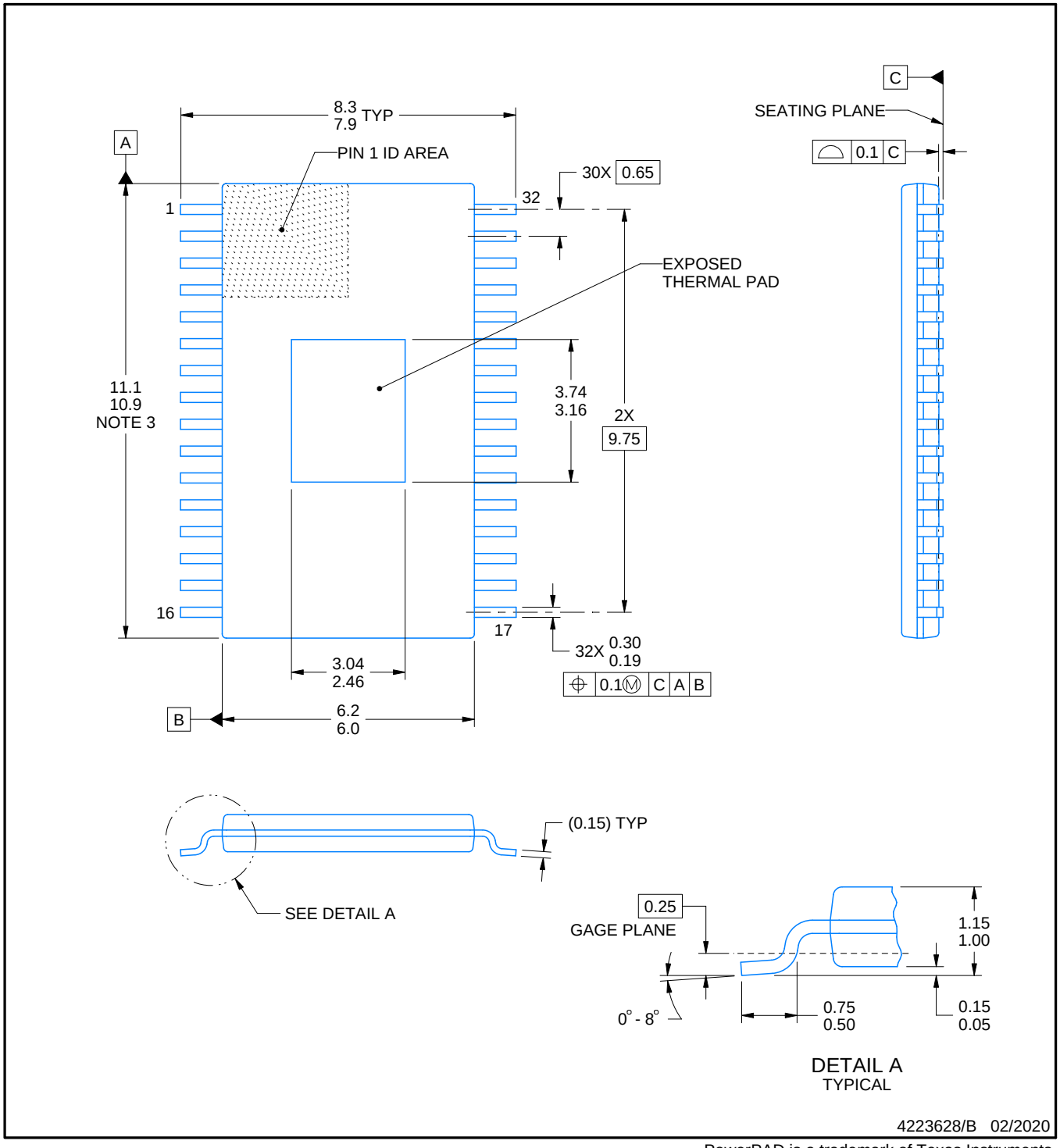


PACKAGE OUTLINE

DAD0032C

PowerPAD ™TSSOP - 1.15 mm max height

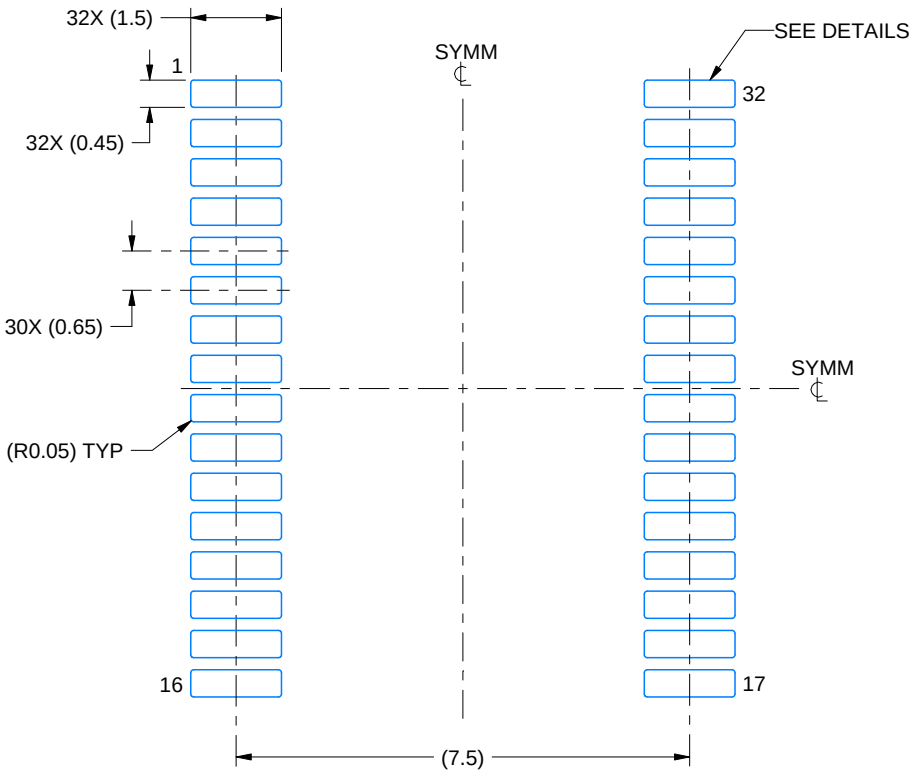
PLASTIC SMALL OUTLINE



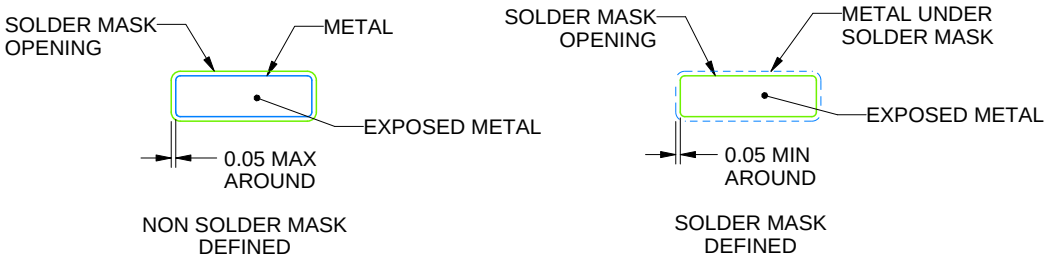
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

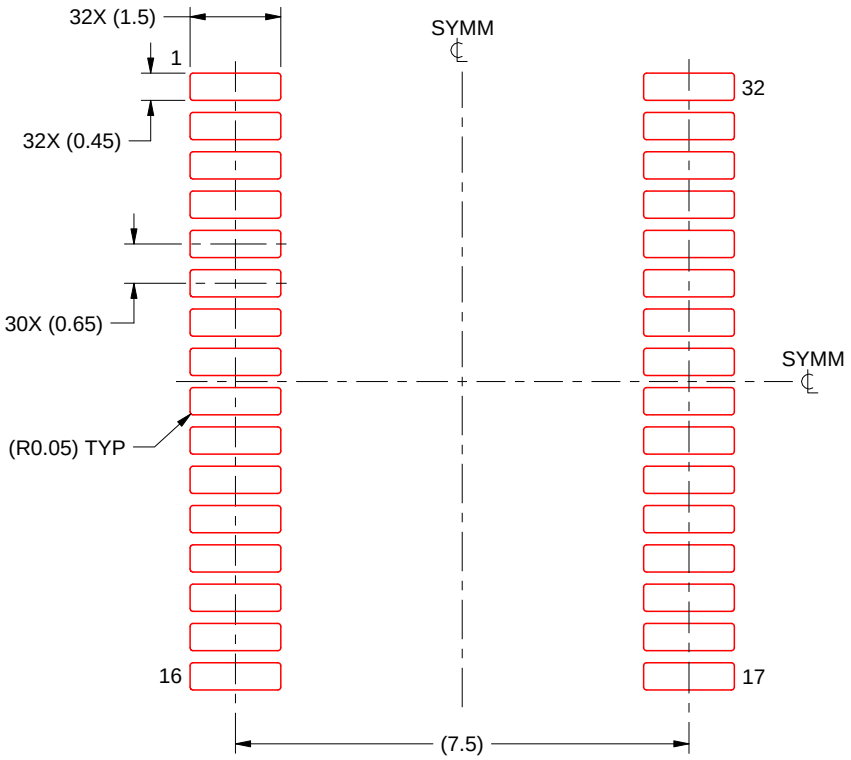


SOLDER MASK DETAILS
NOT TO SCALE

4223628/B 02/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4223628/B 02/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

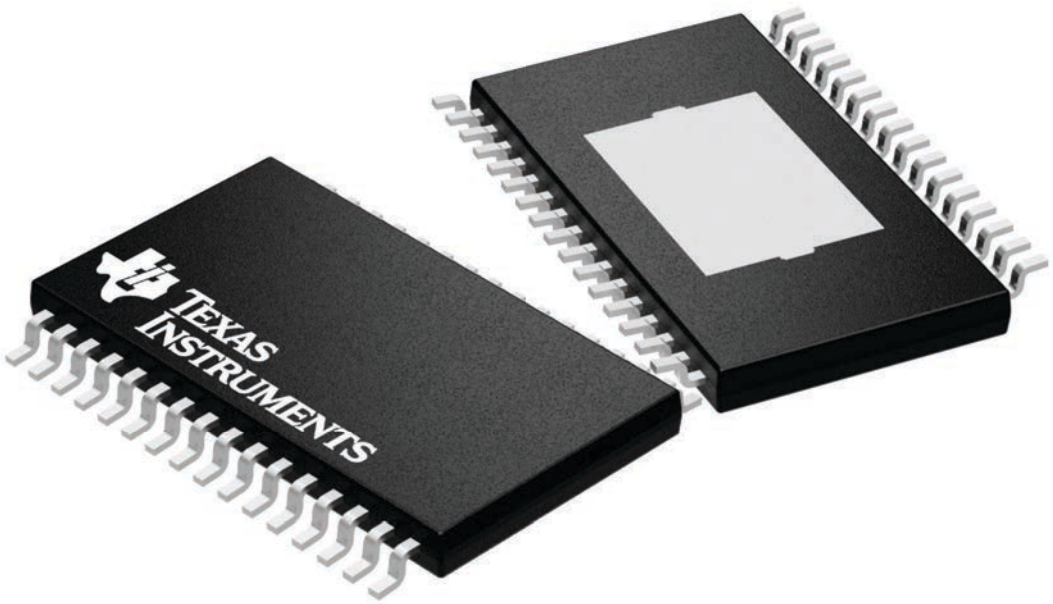
DAP 32

PowerPAD™ TSSOP - 1.2 mm max height

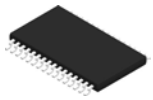
8.1 x 11, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225303/A

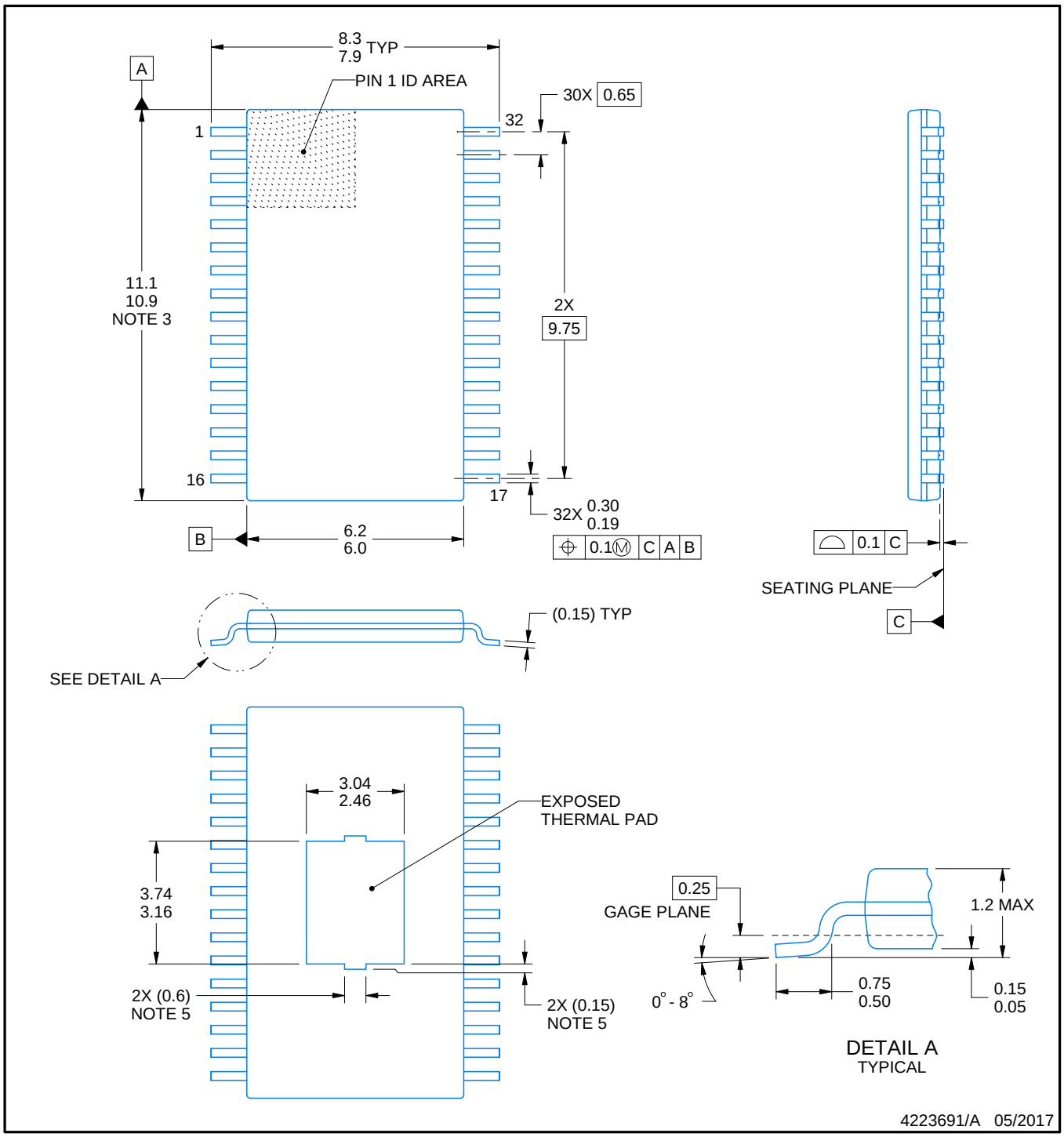


PACKAGE OUTLINE

DAP0032C

PowerPAD™ TSSOP - 1.2 mm max height

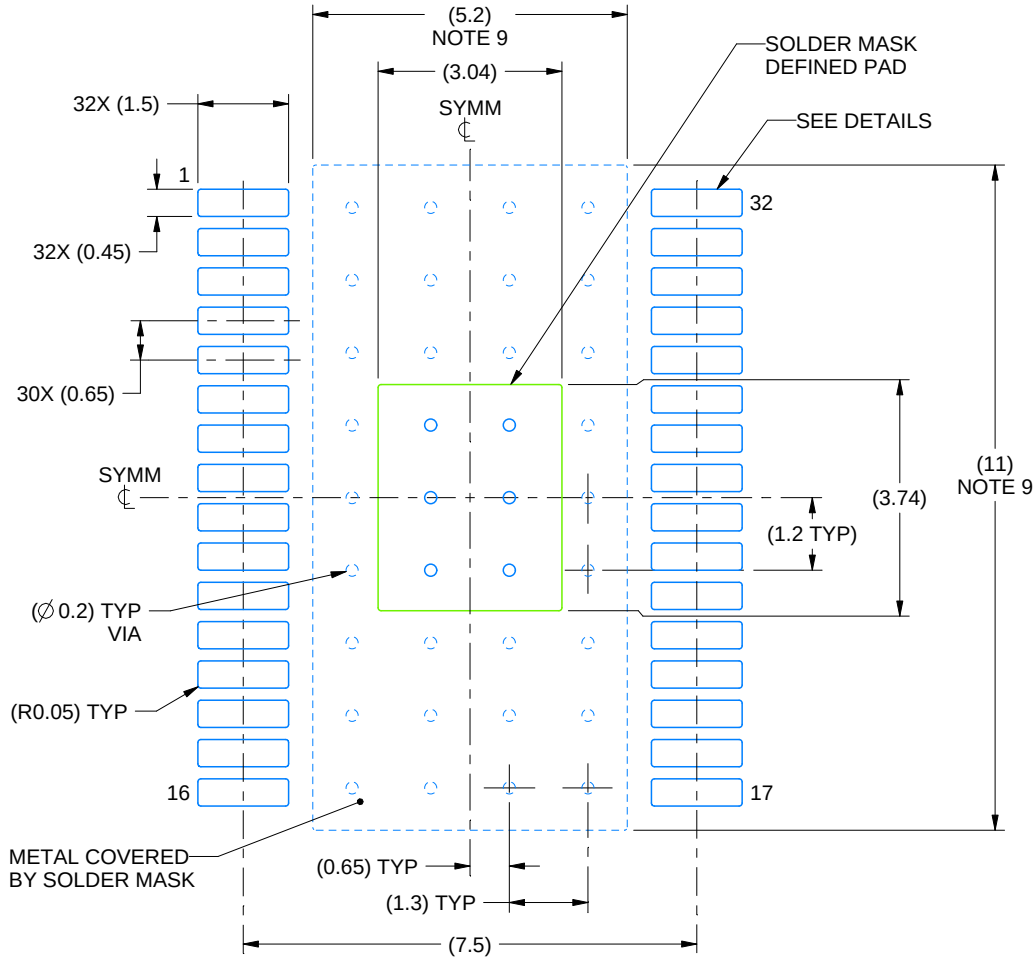
PLASTIC SMALL OUTLINE



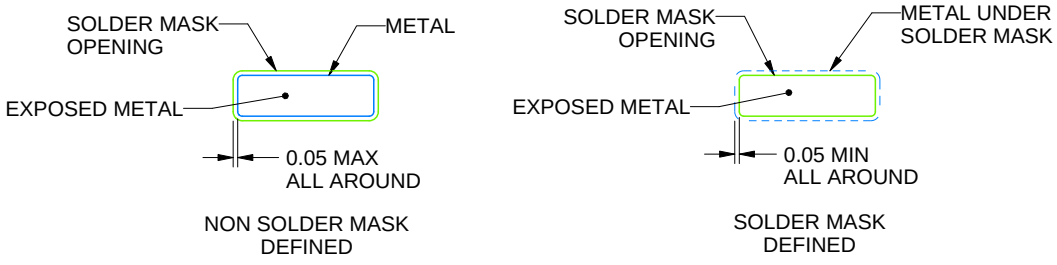
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

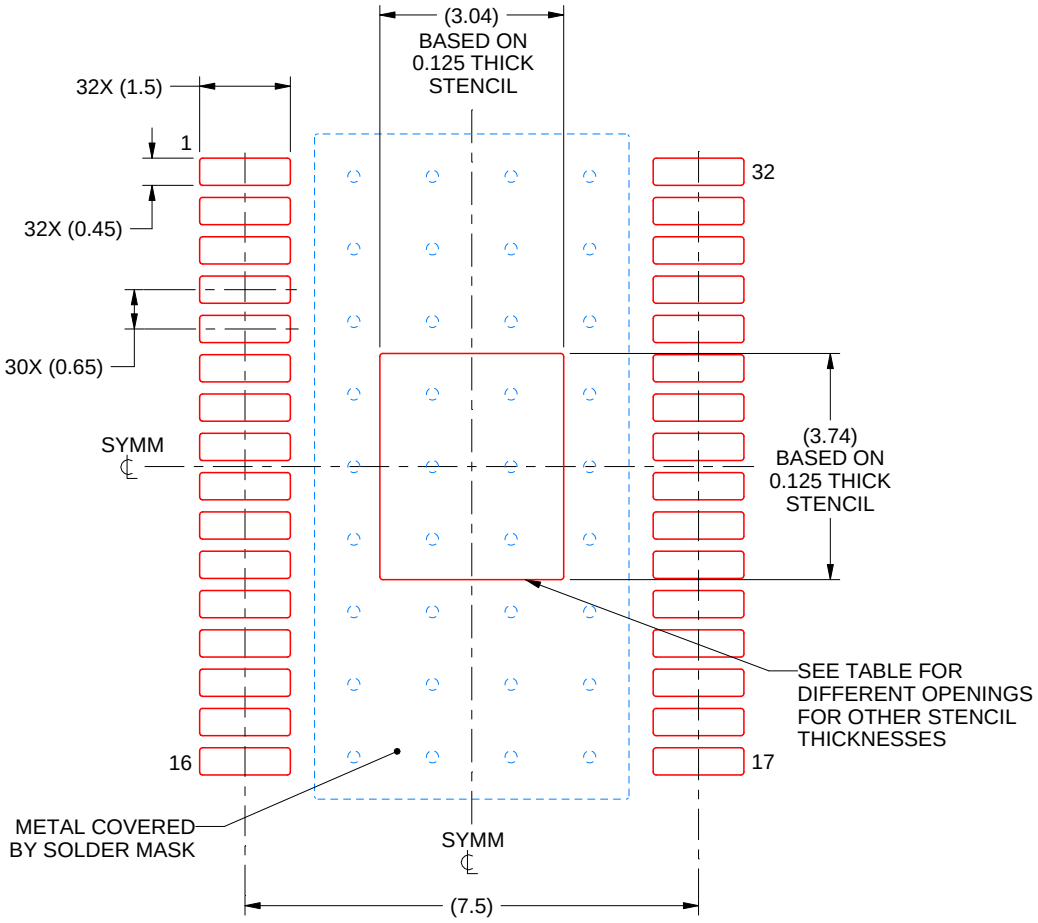


SOLDER MASK DETAILS
NOT TO SCALE

4223691/A 05/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.40 X 4.18
0.125	3.04 X 3.74 (SHOWN)
0.15	2.78 X 3.41
0.175	2.57 X 3.16

4223691/A 05/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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