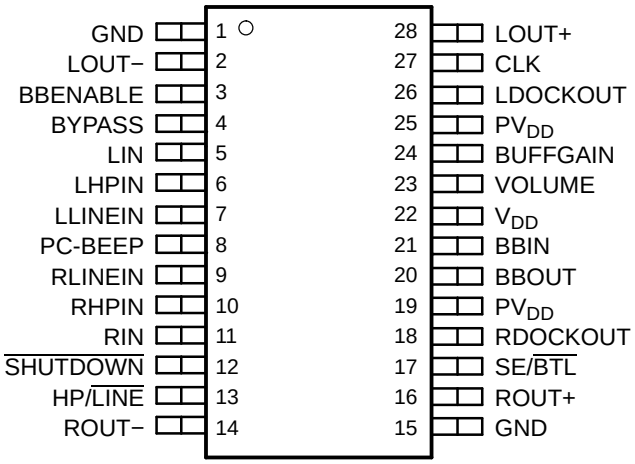
STEREO 2.7-W AUDIO POWER AMPLIFIER WITH BASS BOOST AND DC VOLUME CONTROL

FEATURES

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **DC Volume and Gain Control Adjustable From 34 dB to -86 dB**
- **Bass Boost**
- **Buffered Docking Station Outputs**
- **2.7-W/Ch Output Power Into 3-Ω Load**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 28-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



DESCRIPTION

The TPA6010A4 is a stereo audio power amplifier in a 28-pin TSSOP thermally enhanced package capable of delivering 2.7 W of continuous RMS output power into 3-Ω loads. When driving 1 W into 8-Ω speakers, the TPA6010A4 has less than 0.22% THD+N across its specified frequency range.

The TPA6010A4 has several features optimized for notebook PCs including bass boost, docking station outputs, dc volume control, and dc gain control.

The TPA6010A4 has a buffer and volume control gain stage that are set by dc voltages. The buffer has a differential input and a differential output. The gain of the buffer, which is controlled by the dc voltage on the BUFFGAIN terminal, is adjustable from -46 dB to 14 dB. The docking station output is 6 dB lower than the buffer gain because the buffer has a differential output and the docking station output is taken from just one of the buffer outputs. The volume control amplifier is adjustable from -34 dB to 20 dB in BTL mode and is 6 dB lower in SE mode. The volume control stage is adjustable by dc voltage on the VOLUME terminal. The amplifier gain from input-to-speaker is the sum of the volume control and the buffer gain. The input-to-speaker gain is adjustable from -86 dB to 34 dB in BTL mode and -92 dB to 28 dB in the SE mode.

The bass boost of the amplifier sums the right and left inputs, adds gain, filters out the high frequencies, and then adds the bass boost signal back into the output power amplifier. The frequency of the bass boost is adjusted by adding an RC filter from BBOUT to BBIN. The gain of the bass boost is set to 12 dB if the same bass is present in both the right and left channels. If the bass is present in just one of the channels, the gain of the bass is set to 9.5 dB. The gain can be reduced by adding a voltage divider from BBIN to BBOUT. If not using the bass boost, pull the BBENABLE pin low.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

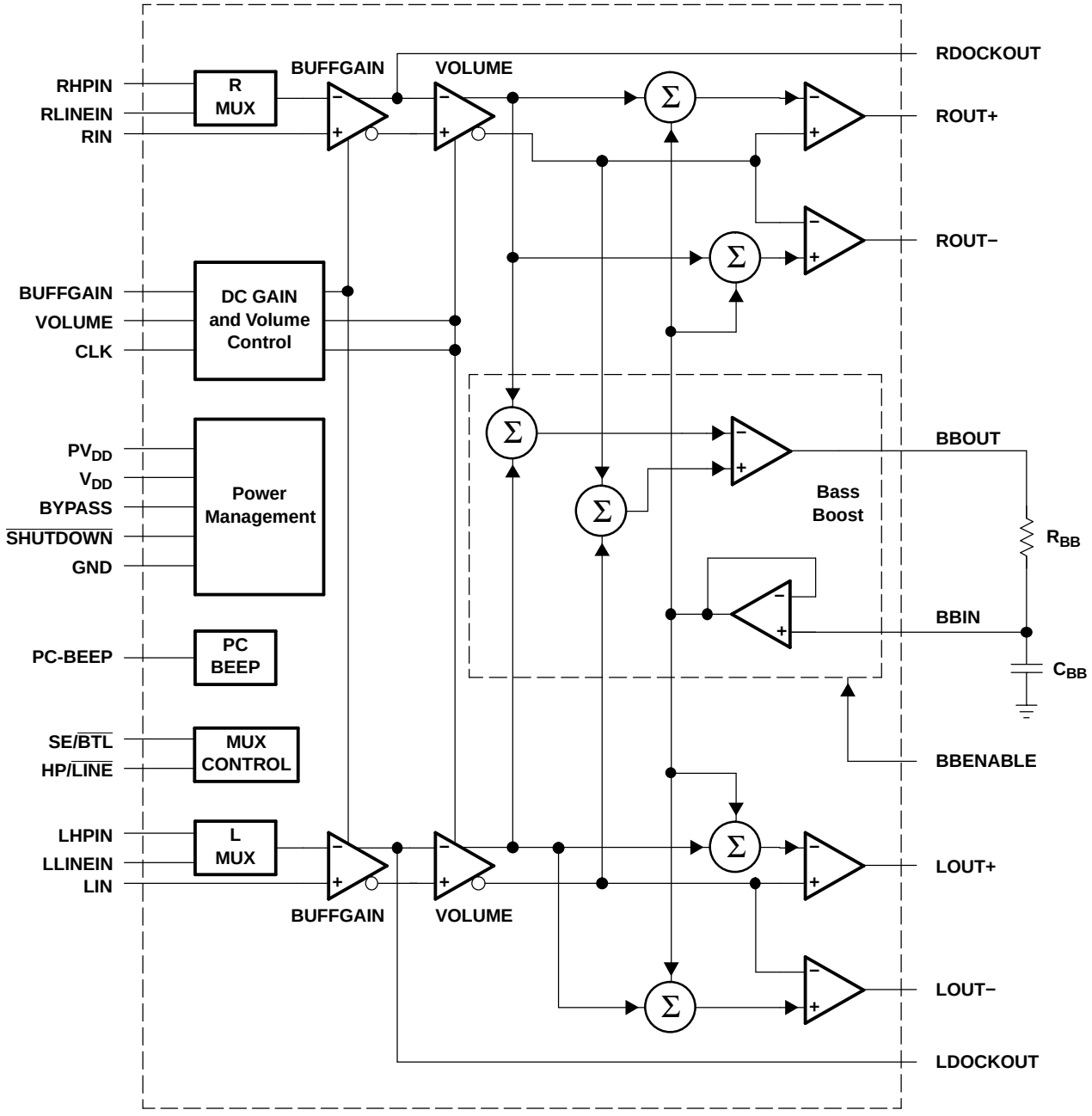
PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2000–2004, Texas Instruments Incorporated

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are truly realized in multilayer PCB applications. This allows the TPA6010A4 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

FUNCTIONAL BLOCK DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP(1) (PWP)
-40°C to 85°C	TPA6010A4PWP

(1) The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA6010A4PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BBENABLE	3	I	BBENABLE is the bass boost control input. When this terminal is held high, the extra bass from the bass boost circuitry is added to the output signal. When this terminal is held low, no extra bass is added.
BBIN	21	I	BBIN is the buffered input to the power amplifier from the bass boost circuitry.
BBOUT	20	O	BBOUT is the bass boost output. A low pass filter must be placed from BBOUT to BBIN to select the low frequencies to be boosted.
BYPASS	4		Tap to voltage divider for internal midsupply bias generator
CLK	27	I	If a 47-nF capacitor is attached, the TPA6010A4 generates an internal clock. An external clock can override the internal clock input to this terminal.
BUFFGAIN	24	I	The gain of the dockout buffer is adjustable from -52 dB to 8 dB to LDOCKOUT and RDOCKOUT, and is set by a dc voltage from 0 V to 3.54 V. When the dc level is over 3.54 V, the device is muted.
GND	1, 15		Ground connection for circuitry. Connected to thermal pad.
HP/$\overline{\text{LINE}}$	13	I	MUX control input, hold high to select LHPIN or RHPIN, hold low to select LLINEIN or RLINEIN.
LHPIN	6	I	Left channel headphone input, selected when HP/$\overline{\text{LINE}}$ is held high
LIN	5	I	Common left input for fully differential input. AC ground for single-ended inputs
LLINEIN	7	I	Left channel line negative input, selected when HP/$\overline{\text{LINE}}$ is held low
LDOCKOUT	26	O	LDOCKOUT is the buffered output of LLINEIN or LHPIN. Use BUFFGAIN for volume adjustment of this pin.
LOUT+	28	O	Left channel positive output in BTL mode and positive output in SE mode
LOUT-	2	O	Left channel negative output in BTL mode and high-impedance in SE mode
PC-BEEP	8	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1.5-V (peak-to-peak) square wave is input to PC-BEEP. AC ground if use is not desired.
PV_{DD}	19, 25	I	Power supply for output stage
RHPIN	10	I	Right channel headphone input, selected when HP/$\overline{\text{LINE}}$ is held high
RIN	11	I	Common right input for fully differential input. AC ground for single-ended inputs
RLINEIN	9	I	Right channel line input, selected when HP/$\overline{\text{LINE}}$ is held low
RDOCKOUT	18	O	RDOCKOUT is the buffered output of RLINEIN or RHPIN. Use BUFFGAIN for volume adjustment of this pin.
ROUT+	16	O	Right channel positive output in BTL mode and positive output in SE mode
ROUT-	14	O	Right channel negative output in BTL mode and high-impedance in SE mode
SE/$\overline{\text{BTL}}$	17	I	Output MUX control. When this terminal is high, SE outputs are selected. When this terminal is low, the BTL outputs are selected.
$\overline{\text{SHUTDOWN}}$	12	I	When held low, this terminal places the entire device, except PC-BEEP detect circuitry, in shutdown mode.
V_{DD}	22	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.
VOLUME	23	I	VOLUME detects the dc level at the terminal and sets the gain for 31 discrete steps covering a range of 20 dB to -40 dB for dc levels of 0.15 V to 3.54. When the dc level is over 3.54 V, the device is muted.
Thermal Pad			Connect to GND. The pad must be soldered down in all applications in order to properly secure the device to the PCB.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
V_{DD}	Supply voltage	6 V
V_I	Input voltage	-0.3 V to V_{DD} +0.3 V
	Continuous total power dissipation	Internally Limited (see Dissipation Rating Table)
T_A	Operating free-air temperature range	-40°C to 85°C
T_J	Operating junction temperature range	-40°C to 150°C
T_{stg}	Storage temperature range	-65°C to 85°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W(1)	21.8 mW/°C	1.7 W	1.4 W

(1) See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (SLMA002), for more information on the PowerPAD™ package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$	$0.8 \times V_{DD}$		V
		$\overline{\text{SHUTDOWN}}$, BBENABLE	2		
V_{IL}	Low-level input voltage	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$		$0.6 \times V_{DD}$	V
		$\overline{\text{SHUTDOWN}}$, BBENABLE		0.8	
T_A	Operating free-air temperature		-40	85	°C

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Output offset voltage (measured differentially)		A_V = 6 dB			35	mV
PSRR	Power supply rejection ratio		V_{DD} = 4.9 V to 5.1 V		67		dB
$\lvert I_{IH} \rvert$	High-level input current	$\overline{\text{SHUTDOWN}}$, SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$, VOLUME, BUFFGAIN, BBENABLE	V_{DD} = 5.5 V, $V_I = V_{DD}$			1	µA
$\lvert I_{IL} \rvert$	Low-level input current	$\overline{\text{SHUTDOWN}}$, SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$, VOLUME, BUFFGAIN, BBENABLE	V_{DD} = 5.5 V, V_I = 0 V			1	µA
I_{DD}	Supply current		BTL mode, $\overline{\text{SHUTDOWN}}$ = 2 V, SE/$\overline{\text{BTL}}$ = $0.6 \times V_{DD}$		12	18	mA
			SE mode, $\overline{\text{SHUTDOWN}}$ = 2 V, SE/$\overline{\text{BTL}}$ = $0.8 \times V_{DD}$		6.5	10	
$I_{DD(SD)}$	Supply current, shutdown mode		PC-BEEP = 2.5 V, $\overline{\text{SHUTDOWN}}$ = 0 V		95	250	µA
			PC-BEEP = 0 V, $\overline{\text{SHUTDOWN}}$ = 0 V		62	200	

OPERATING CHARACTERISTICS

V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω, Gain = 6 dB, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	R_L = 3 Ω, f = 1 kHz	THD = 10%		2.7		W
			THD = 1%		2.2		
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.45%		
B_{OM}	Bandwidth, maximum output power	THD = 1%			>15		kHz
k_{SVR}	Supply ripple rejection ratio	f = 20 Hz to 20 kHz, C_{Bypass} = 1 µF, V_{ripple} = 200 mV_{pp}	BTL mode		56		dB
V_n	Output noise voltage	C_{Bypass} = 1 µF, f = 20 Hz to 20 kHz	BTL mode		50		μV_{RMS}
			SE mode		32		
xtalk	Crosstalk	f = 20 Hz to 20 kHz	BTL mode		-80		dB

OPERATING CHARACTERISTICS

V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω, Gain = 6 dB, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.06%,	f = 1 kHz		1		W
THD + N	Total harmonic distortion plus noise	P_O = 0.5 W,	f = 20 Hz to 15 kHz		0.5%		
B_{OM}	Bandwidth, maximum output power	THD = 1%			>15		kHz
k_{SVR}	Supply ripple rejection ratio	f = 20 Hz to 20 kHz, C_{Bypass} = 1 µF, V_{ripple} = 200 mV_{pp}	BTL mode		56		dB
V_n	Output noise voltage	C_B = 1 µF, f = 20 Hz to 20 kHz	BTL mode		50		μV_{RMS}
			SE mode		32		
xtalk	Crosstalk	f = 20 Hz to 20 kHz	BTL mode		-80		dB

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD + N	Total harmonic distortion + noise	vs Output power	1,2
		vs Dockout voltage	3
		vs Frequency	4, 5, 6

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

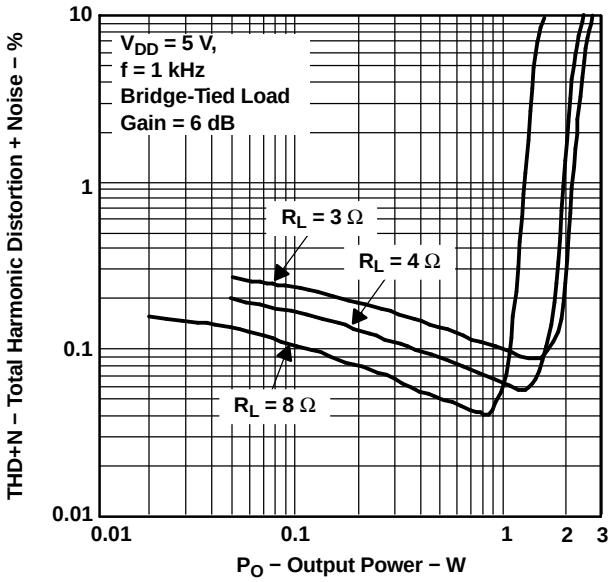


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

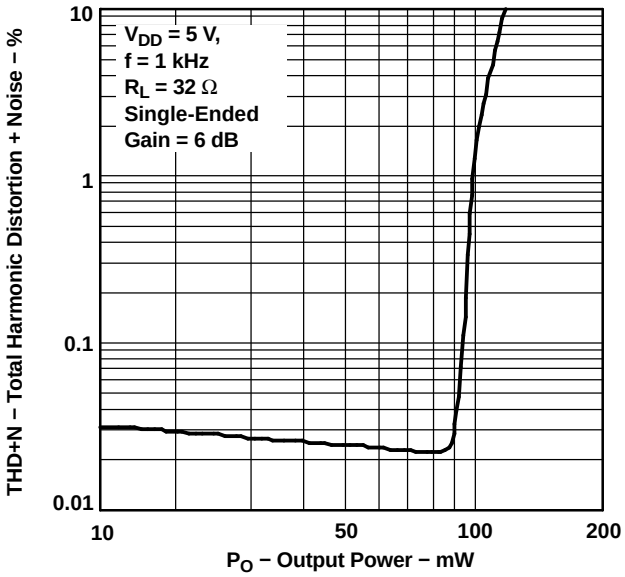


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE
vs
DOCKOUT VOLTAGE

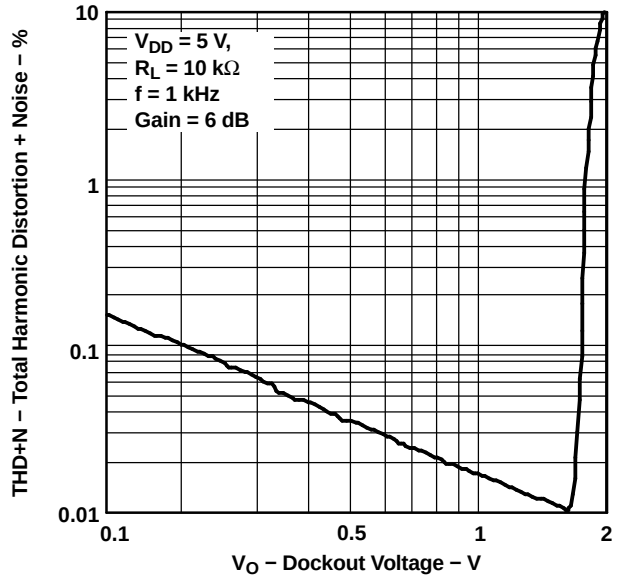


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

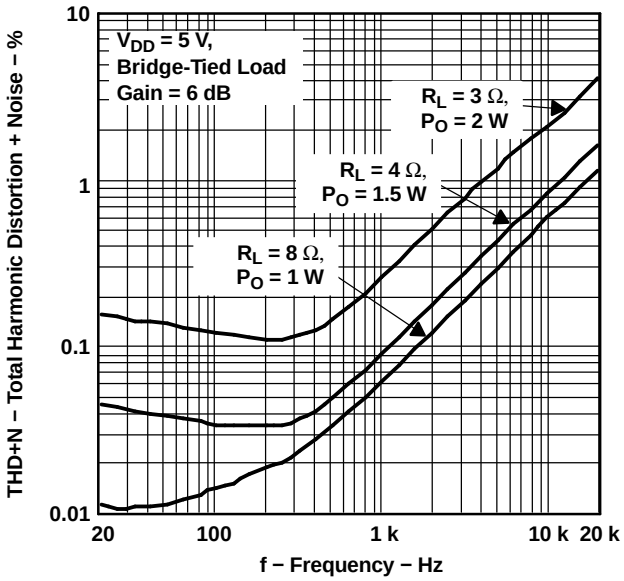


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

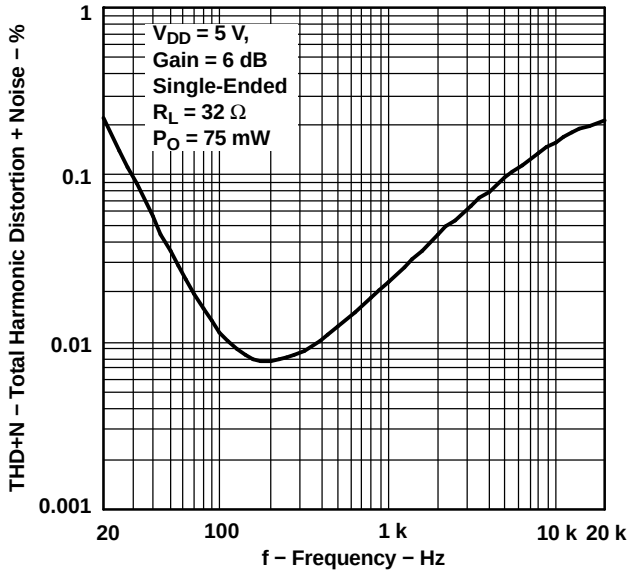


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

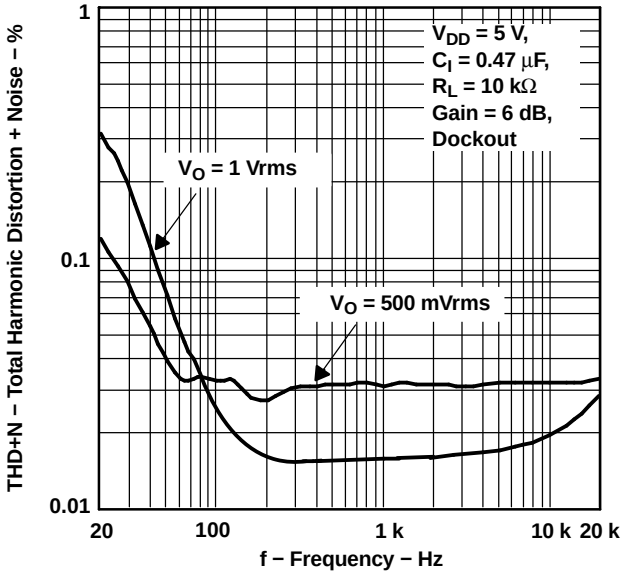


Figure 6.

APPLICATION INFORMATION

INTERNAL BUFFER GAIN AND VOLUME GAIN

The typical voltage and gain levels are shown in Table 1 and Table 2.

Table 1. BUFFGAIN Voltage and Gain Values

BUFFGAIN (Terminal 24)		TYPICAL GAIN OF AMPLIFIER (VOLUME Stage)(1)	
Inceasing Voltage (V)(2)(3)	Decreasing Voltage (V)(2)(3)	Internal Gain (dB)	DOCKOUT Gain (dB)
0.00 – 0.20	0.16 – 0.00	14	8
0.21 – 0.31	0.27 – 0.17	12	6
0.32 – 0.42	0.38 – 0.28	10	4
0.43 – 0.54	0.50 – 0.39	8	2
0.55 – 0.65	0.61 – 0.51	6	0
0.66 – 0.76	0.72 – 0.62	4	-2
0.77 – 0.88	0.84 – 0.73	2	-4
0.89 – 0.99	0.96 – 0.85	0	-6
1.00 – 1.11	1.07 – 0.97	-2	-8
1.12 – 1.22	1.19 – 1.08	-4	-10
1.23 – 1.34	1.30 – 1.20	-6	-12
1.35 – 1.45	1.42 – 1.31	-8	-14
1.46 – 1.56	1.53 – 1.43	-10	-16
1.57 – 1.68	1.64 – 1.54	-12	-18
1.69 – 1.79	1.76 – 1.65	-14	-20
1.80 – 1.91	1.88 – 1.77	-16	-22
1.92 – 2.02	1.99 – 1.89	-18	-24
2.03 – 2.14	2.11 – 2.00	-20	-26
2.15 – 2.25	2.23 – 2.12	-22	-28
2.26 – 2.37	2.34 – 2.24	-24	-30
2.38 – 2.48	2.47 – 2.35	-26	-32
2.49 – 2.60	2.57 – 2.46	-28	-34
2.61 – 2.71	2.69 – 2.58	-30	-36
2.72 – 2.83	2.81 – 2.70	-32	-38
2.84 – 2.95	2.92 – 2.82	-34	-40
2.96 – 3.06	3.04 – 2.93	-36	-42
3.07 – 3.18	3.15 – 3.05	-38	-44
3.19 – 3.29	3.27 – 3.16	-40	-46
3.30 – 3.41	3.39 – 3.28	-42	-48
3.42 – 3.52	3.50 – 3.40	-44	-50
3.53 – 3.63	3.62 – 3.51	-46	-52
3.64 – 5.00	5.00 – 3.63	-75	-81

(1) Typical gain values can vary by ±2 dB.
(2) To set the Internal and DOCKOUT gain to a fixed value upon power up, use the appropriate voltage range in the Decreasing Voltage column.
(3) For best results, set the voltage to the middle of the appropriate voltage range.

Table 2. VOLUME Voltage and Gain Values

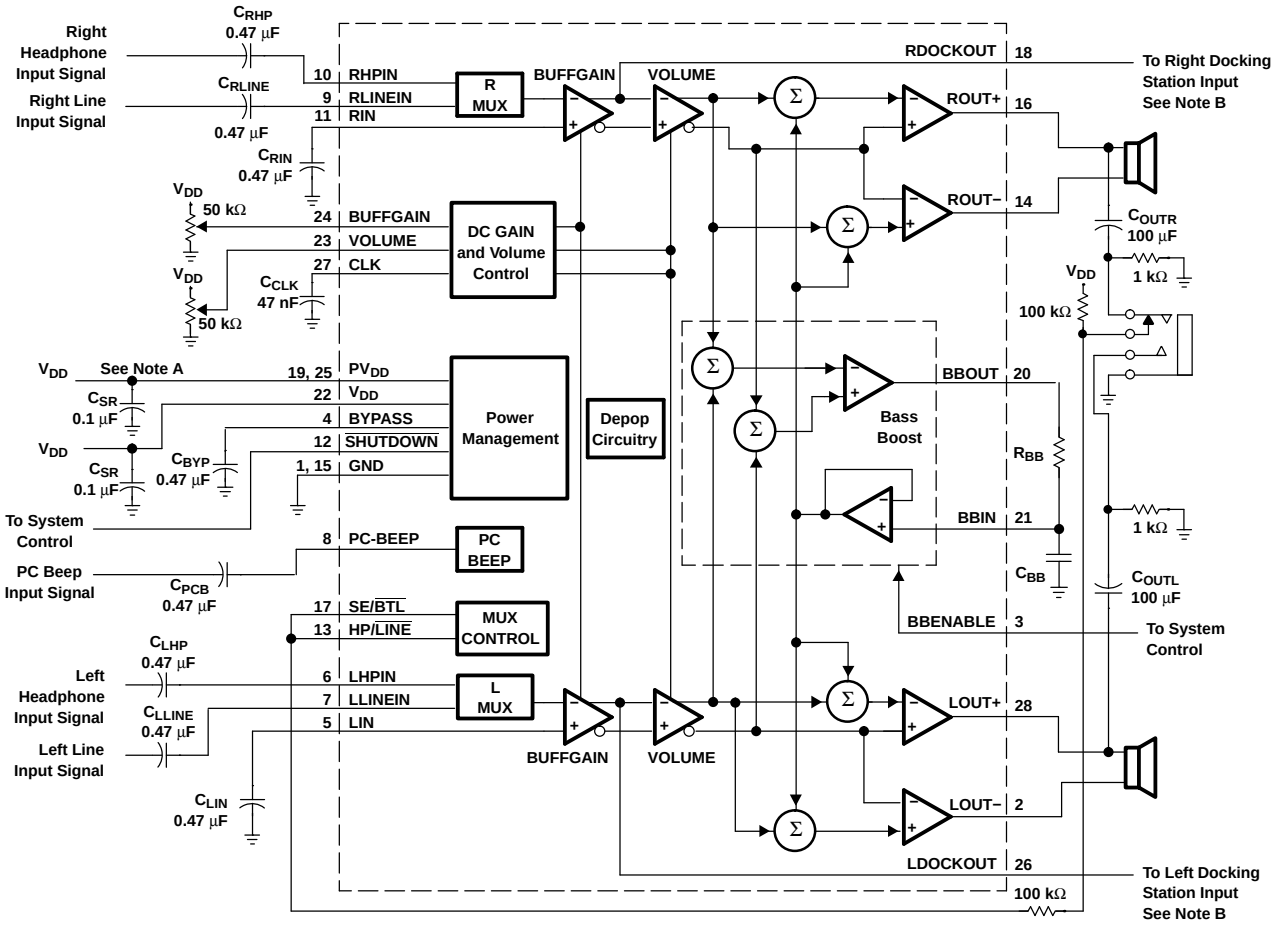
VOLUME (Terminal 23)		TYPICAL GAIN OF AMPLIFIER (VOLUME Stage)(1)	
Inceasing Voltage (V)(2)(3)	Decreasing Voltage (V)(2)(3)	BTL Gain (dB)	SE Gain (dB)
0.00 – 0.20	0.16 – 0.00	20	14
0.21 – 0.31	0.27 – 0.17	18	12
0.32 – 0.42	0.38 – 0.28	16	10
0.43 – 0.54	0.50 – 0.39	14	8
0.55 – 0.65	0.61 – 0.51	12	6
0.66 – 0.76	0.72 – 0.62	10	4
0.77 – 0.88	0.84 – 0.73	8	2
0.89 – 0.99	0.96 – 0.85	6	0
1.00 – 1.11	1.07 – 0.97	4	-2
1.12 – 1.22	1.19 – 1.08	2	-4
1.23 – 1.34	1.30 – 1.20	0	-6
1.35 – 1.45	1.42 – 1.31	-2	-8
1.46 – 1.56	1.53 – 1.43	-4	-10
1.57 – 1.68	1.64 – 1.54	-6	-12
1.69 – 1.79	1.76 – 1.65	-8	-14
1.80 – 1.91	1.88 – 1.77	-10	-16
1.92 – 2.02	1.99 – 1.89	-12	-18
2.03 – 2.14	2.11 – 2.00	-14	-20
2.15 – 2.25	2.23 – 2.12	-16	-22
2.26 – 2.37	2.34 – 2.24	-18	-24
2.38 – 2.48	2.47 – 2.35	-20	-26
2.49 – 2.60	2.57 – 2.46	-22	-28
2.61 – 2.71	2.69 – 2.58	-24	-30
2.72 – 2.83	2.81 – 2.70	-26	-32
2.84 – 2.95	2.92 – 2.82	-28	-34
2.96 – 3.06	3.04 – 2.93	-30	-36
3.07 – 3.18	3.15 – 3.05	-32	-38
3.19 – 3.29	3.27 – 3.16	-34	-40
3.30 – 3.41	3.39 – 3.28	-36	-42
3.42 – 3.52	3.50 – 3.40	-38	-44
3.53 – 3.63	3.62 – 3.51	-40	-46
3.64 – 5.00	5.00 – 3.63	-95	-95

(1) Typical gain values can vary by ±2 dB.
(2) To set the Internal and DOCKOUT gain to a fixed value upon power up, use the appropriate voltage range in the Decreasing Voltage column.
(3) For best results, set the voltage to the middle of the appropriate voltage range.

The total gain of the amplifier can be determined using the following equations:

Total gain = Internal gain (dB) + BTL gain (dB), if outputs are bridge-tied.

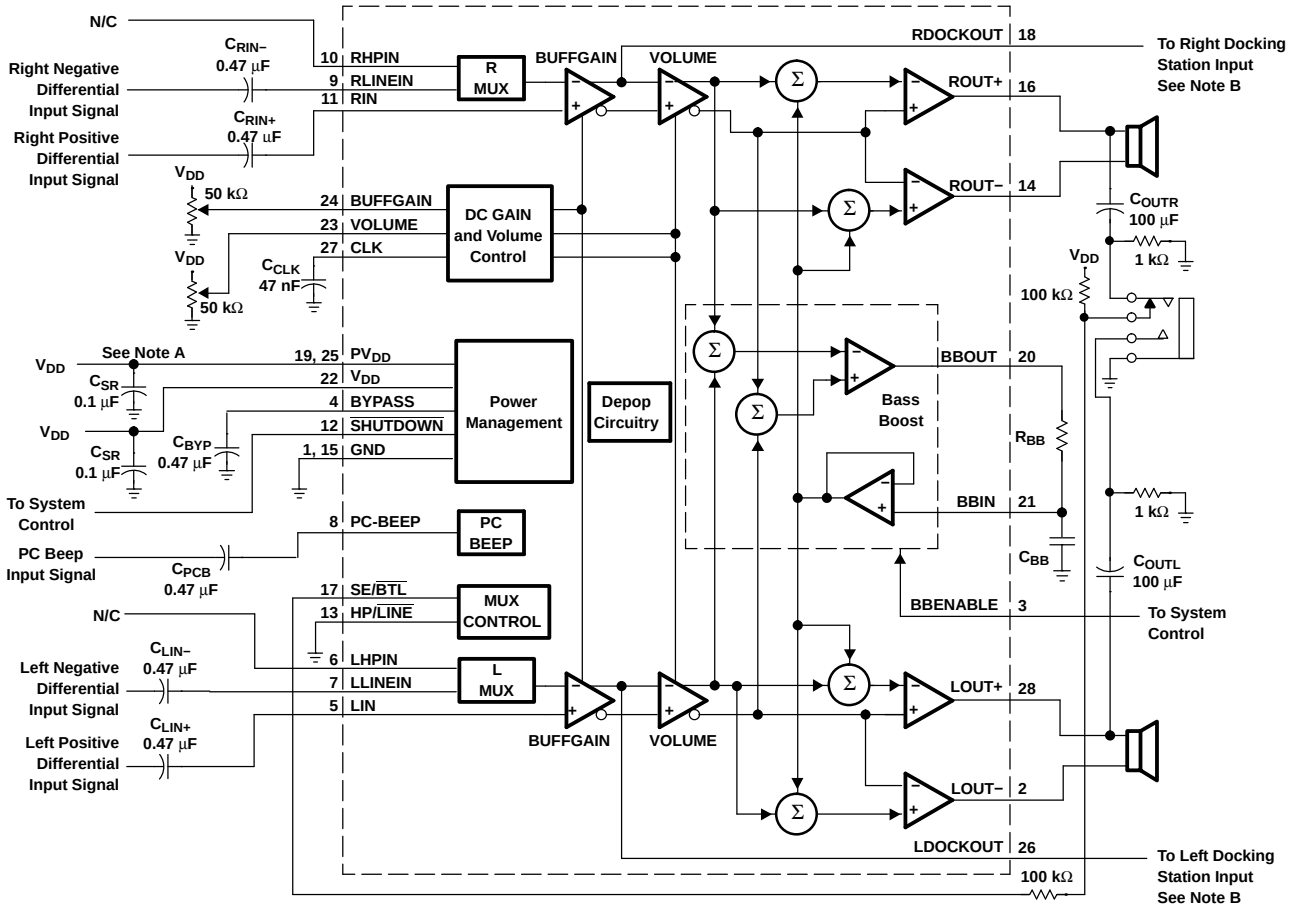
Total gain = Internal gain (dB) + SE gain (dB), if outputs are single-ended.



A. A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

B. A DC-blocking capacitor should be placed at each input to the amplifier in the docking station, as the RDOCKOUT and LDOCKOUT pins are biased to $V_{DD}/2$.

Figure 7. Typical TPA6010A4 Application Circuit Using Single-Ended Inputs and Input MUX



A. A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

B. A DC-blocking capacitor should be placed at each input to the amplifier in the docking station, as the RDOCKOUT and LDOCKOUT pins are biased to $V_{DD}/2$.

Figure 8. Typical TPA6010A4 Application Circuit Using Differential Inputs

INPUT RESISTANCE

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the -3 dB or cut-off frequency also changes by over 6 times.

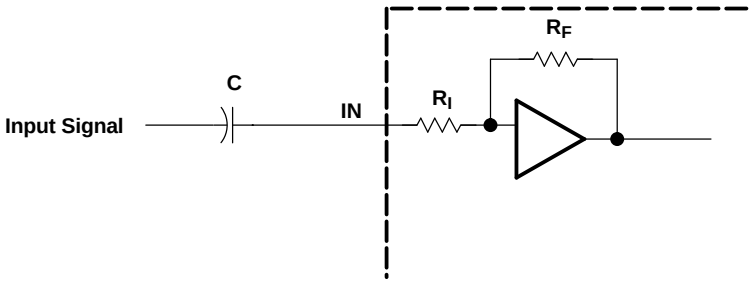
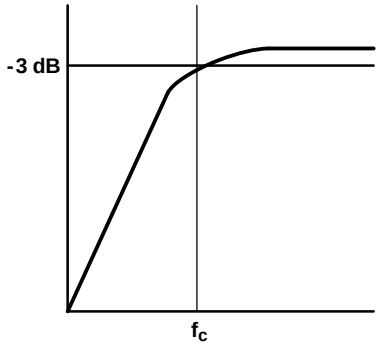


Figure 9. Resistor-On Input for Cut-Off Frequency

INPUT CAPACITOR, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input resistance of the amplifier, R_I, form a high-pass filter with the corner frequency determined in Equation 1.

$$f_c = \frac{1}{2\pi R_I C_I} \quad (1)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 70 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 1 is reconfigured as Equation 2.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (2)$$

In this example, C_I is 5.6 nF so one would likely choose a value in the range of 5.6 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

POWER SUPPLY DECOUPLING, C_S

The TPA6010A4 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

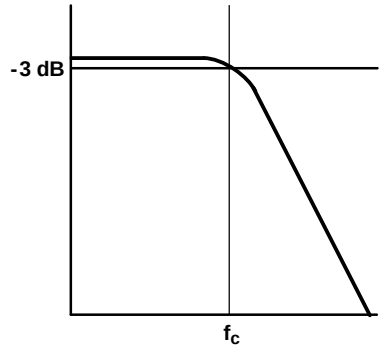
MIDRAIL BYPASS CAPACITOR, C_{BYP}

The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

For the bypass capacitor, C_{BYP}, 0.47 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

BASS BOOST OPERATION

The bass boost feature of the TPA6010A4 sums the left and right inputs, adds gain, filters out the high frequencies, and adds the bass-boosted signal back into the current-gain stage of the amplifier. The cutoff frequency is set by R_{BB} and C_{BB} as shown in Equation 3.



$$f_C = \frac{1}{2\pi R_{BB} C_{BB}} \quad (3)$$

The gain of the bass boost is set internally at 12 dB if bass is present in both the right and left channels. If bass is only present in one of the channels, the boost is reduced to 9.5 dB.

The total bass boost gain may be determined by using Equation 4.

$$\text{Bass Boost Gain} = 12\text{ dB} + 20\text{Log}\left(\frac{R2}{R1 + R2}\right) \quad \text{(bass present on both channels)}$$

$$\text{Bass Boost Gain} = 9.5\text{ dB} + 20\text{Log}\left(\frac{R2}{R1 + R2}\right) \quad \text{(bass present on only one channel)} \quad (4)$$

Consider the following example application. The desired cutoff frequency for the bass boost is 300 Hz and the desired bass boost gain is 6 dB. The filter components could be R_{BB} = 1.1 kΩ and C_{BB} = 0.47 µF.

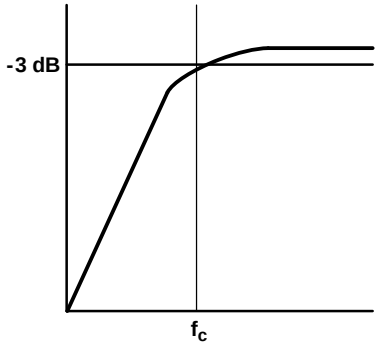
If the bass boost feature is not to be used or if the user wishes to disable the boost, the BBENABLE pin should be pulled low.

Finally, as illustrated in the functional block diagram, the bass boost is only applied to the speaker outputs, not to the docking station outputs.

OUTPUT COUPLING CAPACITOR, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 5.

$$f_c = \frac{1}{2\pi R_L C_C}$$



(5)

The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32Ω , 10 kΩ, and 47 kΩ. Table 3 summarizes the frequency response characteristics of each configuration.

Table 3. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 3 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

BRIDGED-TIED LOAD VERSUS SINGLE-ENDED MODE

Figure 10 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA6010A4 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance as in Equation 6.

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \quad (6)$$

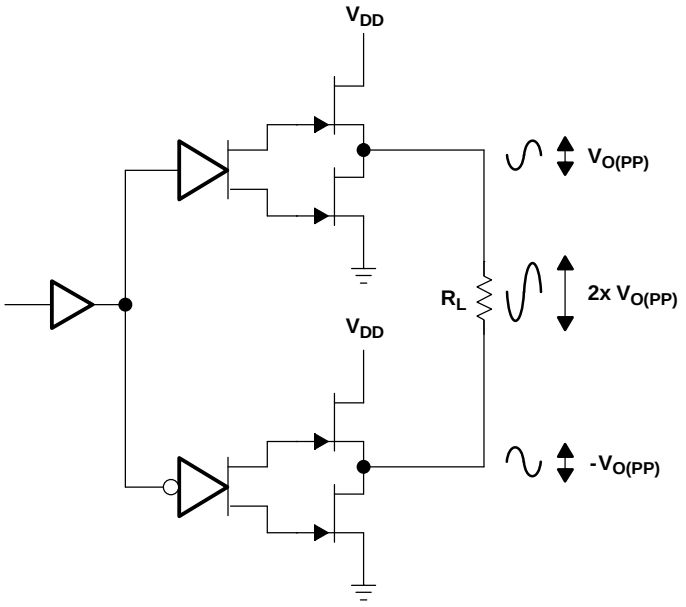


Figure 10. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 11. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated with Equation 7.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (7)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

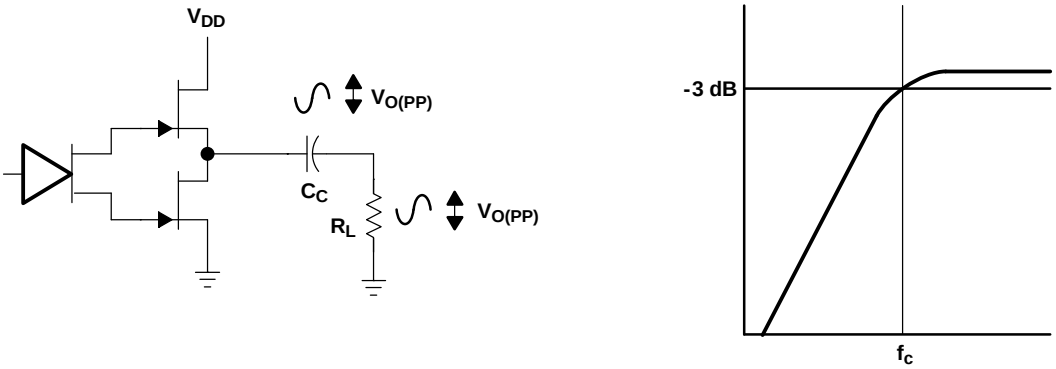


Figure 11. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *CREST FACTOR and THERMAL CONSIDERATIONS* section.

SINGLE-ENDED OPERATION

In SE mode (see Figure 10 and Figure 11), the load is driven from the primary amplifier output for each channel (OUT+, terminals 28 and 16).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 1 V/V.

BTL AMPLIFIER EFFICIENCY

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 12).

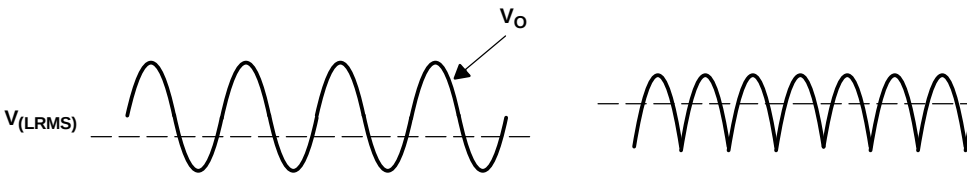


Figure 12. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. Equation 8 and Equation 9 are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{8}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

and $$P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = -\frac{1}{\pi} \times \frac{V_P}{R_L} \left[\cos(t)\right]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\pi\, R_L}$$

Substituting P_L and P_{SUP} into equation 8,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2\, R_L}}{\frac{2\, V_{DD}\, V_P}{\pi\, R_L}} = \frac{\pi\, V_P}{4\, V_{DD}}$$

Where:

$$V_P = \sqrt{2\, P_L\, R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2\, P_L\, R_L}}{4\, V_{DD}} \tag{9}$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

Table 4 employs equation 9 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased, resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 4. Efficiency vs Output Power in 5-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47(1)	0.53

(1) High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to the utmost advantage when possible. Note that in Equation 9, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

CREST FACTOR AND THERMAL CONSIDERATIONS

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the TPA6010A4 data sheet, one can see that when the TPA6010A4 is operating from a 5-V supply into a 3-Ω speaker that 4-W peaks are available. Converting watts to dB as in Equation 10:

$$P_{dB} = 10\,\text{Log}\frac{P_W}{P_{ref}} = 10\,\text{Log}\frac{4\ \text{W}}{1\ \text{W}} = 6\ \text{dB} \tag{10}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB − 15 dB = − 9 dB (15 dB crest factor)

6 dB − 12 dB = − 6 dB (12 dB crest factor)

6 dB − 9 dB = − 3 dB (9 dB crest factor)

6 dB − 6 dB = 0 dB (6 dB crest factor)

6 dB − 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts as in Equation 11:

$$P_W = 10^{PdB/10} \times P_{ref}$$

= 63 mW (18 dB crest factor)

= 125 mW (15 dB crest factor)

= 250 mW (9 dB crest factor)

= 500 mW (6 dB crest factor)

= 1000 mW (3 dB crest factor)

= 2000 mW (15 dB crest factor) (11)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA6010A4 and maximum ambient temperatures are shown in Table 5.

Table 5. TPA6010A4 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2000 mW (3 dB)	1.7	-3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	85°C(1)

(1) Package limited to 85°C ambient.

Table 6. TPA6010A4 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5	1250 mW (3 dB crest factor)	0.55	85°C(1)
2.5	1000 mW (4 dB crest factor)	0.62	85°C(1)
2.5	500 mW (7 dB crest factor)	0.59	85°C(1)
2.5	250 mW (10 dB crest factor)	0.53	85°C(1)

(1) Package limited to 85°C ambient.

The maximum dissipated power, $P_{D(max)}$, is reached at a much lower output power level for an 8-Ω load than for a 3-Ω load. As a result, for calculating $P_{D(max)}$ for an 8-Ω application, use Equation 12:

$$P_{D(max)} = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{12}$$

However, in the case of a 3-Ω load, $P_{D(max)}$ occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the $P_{D(max)}$ formula for a 3-Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the Dissipation Rating Table. To convert this to θ_{JA} use Equation 13:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°\text{C/W} \tag{13}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with Equation 14. The maximum recommended junction temperature for the TPA6010A4 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$\begin{aligned} T_A\,\text{Max} &= T_J\,\text{Max} - \Theta_{JA} P_D \\ &= 150 - 45(0.6 \times 2) = 96°\text{C (15 dB crest factor)} \end{aligned} \tag{14}$$

A. Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB crest factor per channel. Due to package limitations the actual T_A Max is 85°C.

Table 5 and Table 6 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA6010A4 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 5 and Table 6 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

SE/$\overline{\text{BTL}}$ OPERATION

The ability of the TPA6010A4 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA6010A4, two separate amplifiers drive OUT+ and OUT-. The SE/$\overline{\text{BTL}}$ input (terminal 17) controls the operation of the follower amplifier that drives LOUT- and ROUT- (terminals 2 and 14). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA6010A4 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT- amplifiers are in a high output impedance state, which configures the TPA6010A4 as an SE driver from LOUT+ and ROUT+ (terminals 28 and 16). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 13.

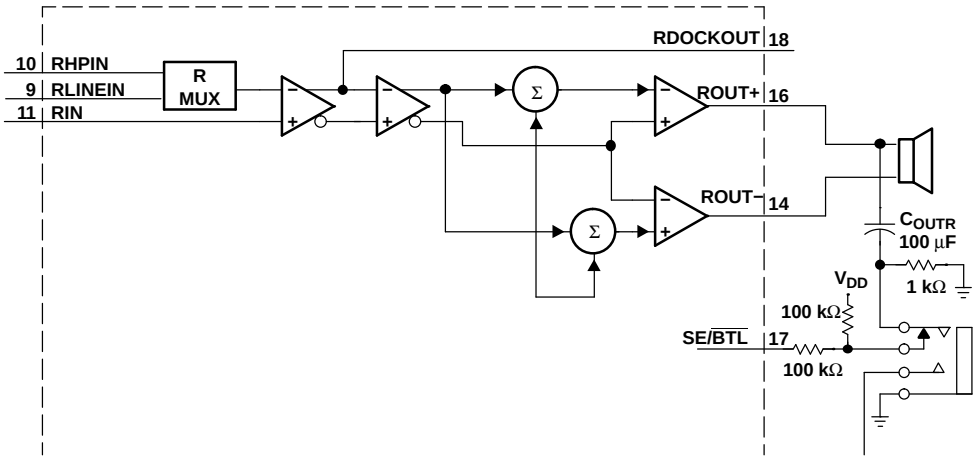


Figure 13. TPA6010A4 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT- amplifier is shut down causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

PC BEEP OPERATION

The PC BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is activated automatically. When the PC BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC BEEP. The gain from the PC BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC BEEP input is deselected, the amplifier returns to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC BEEP takes the device out of shutdown and outputs the PC BEEP signal, and then returns the amplifier to shutdown mode.

The amplifier automatically switches to PC BEEP mode after detecting a valid signal at the PC BEEP input. The preferred input signal is a square wave or pulse train with an amplitude of 1.5 V_{pp} or greater. To be accurately detected, the signal must have a minimum of 1.5-V_{pp} amplitude, rise and fall times of less than 0.1 µs, and a minimum of 8 rising edges. When the signal is no longer detected, the amplifier returns to its previous operating mode and volume setting.

If it is desired to ac-couple the PC BEEP input, the value of the coupling capacitor should be chosen to satisfy Equation 15:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB} (100\ k\Omega)} \quad (15)$$

The PC BEEP input can also be dc-coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

INPUT MUX OPERATION

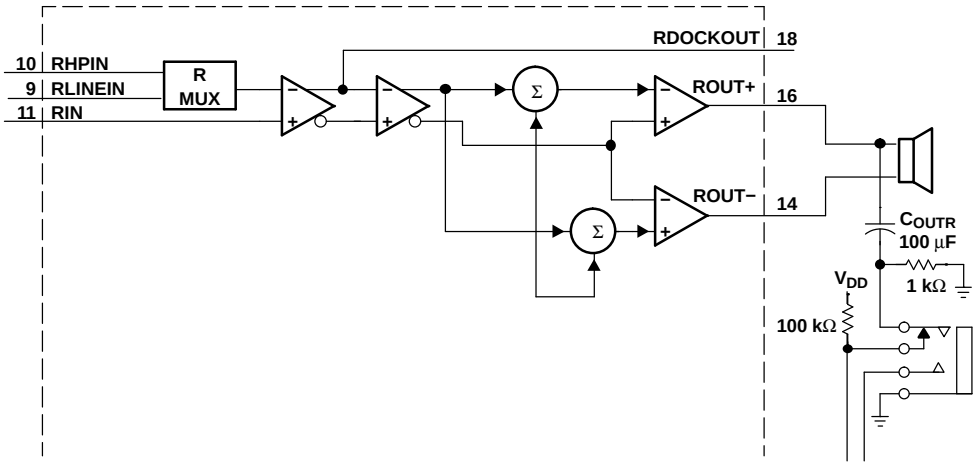


Figure 14. TPA6010A4 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to -1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/$\overline{\text{BTL}}$ OPERATION section for a description of the headphone jack control circuit.

SHUTDOWN MODES

The TPA6010A4 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

Table 7. Shutdown and Mute Mode Functions

INPUTS(1)		AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
Low	High	Line	BTL
X	Low	X(2)	Mute
High	High	HP	SE

(1) Inputs should never be left unconnected.
(2) X = do not care

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA6010A4PWP	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA6010
TPA6010A4PWP.A	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA6010
TPA6010A4PWPR	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA6010
TPA6010A4PWPR.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA6010

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

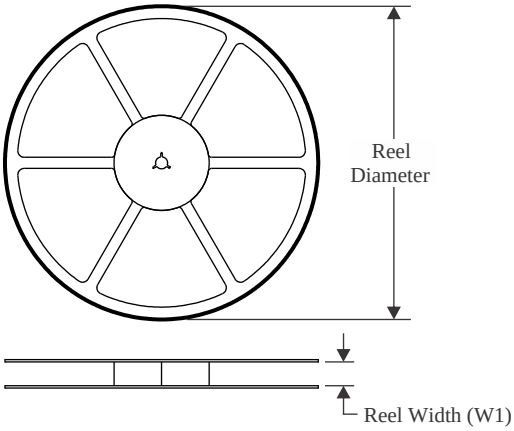
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

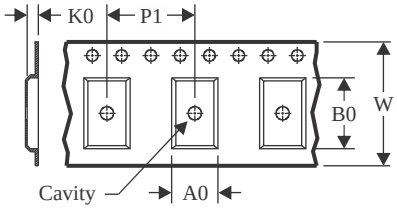
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

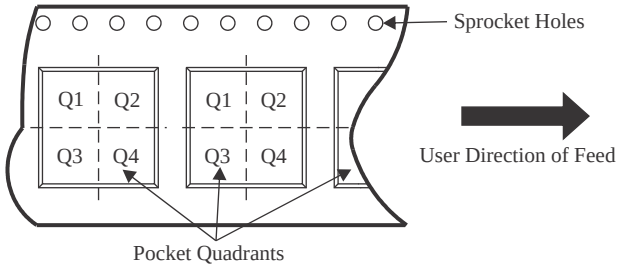


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

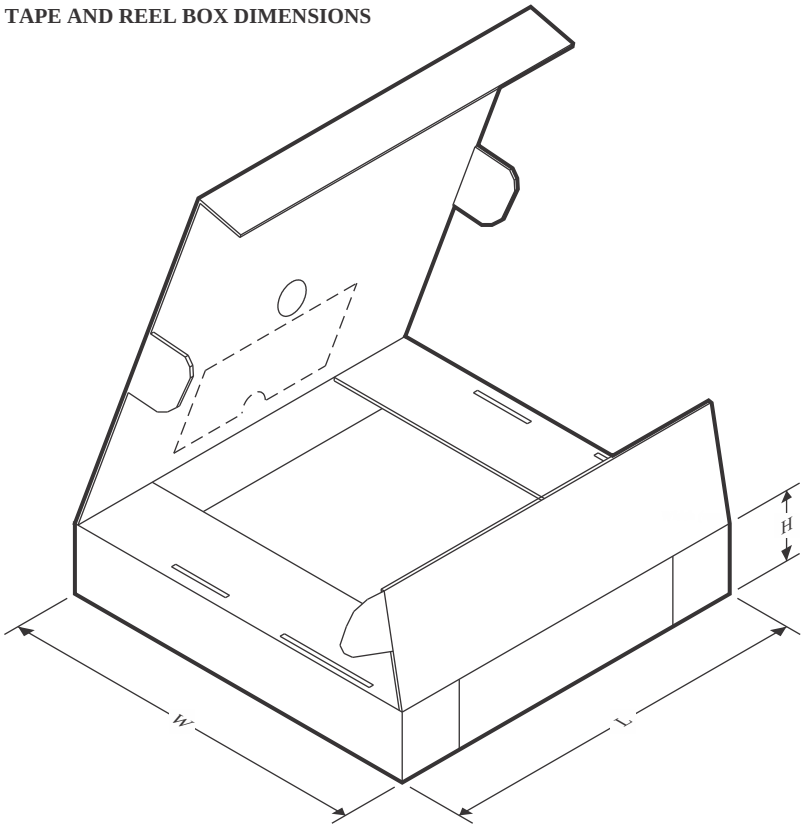
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6010A4PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

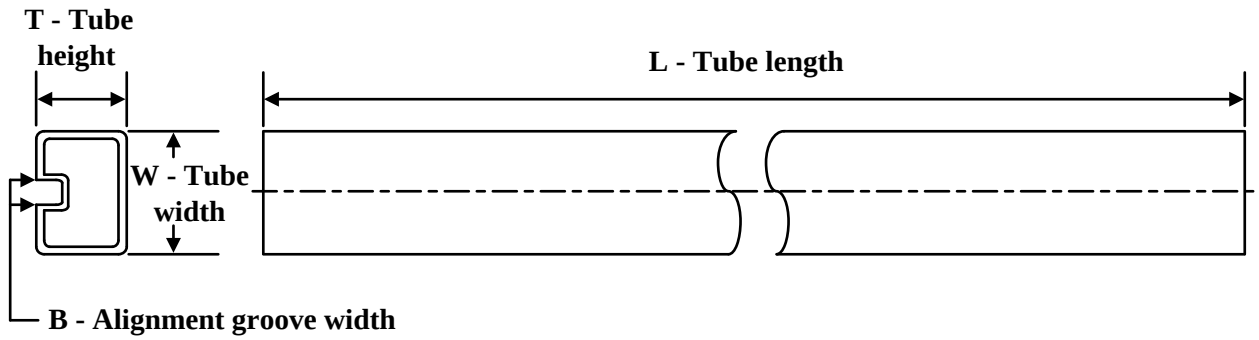
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6010A4PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA6010A4PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPA6010A4PWP.A	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

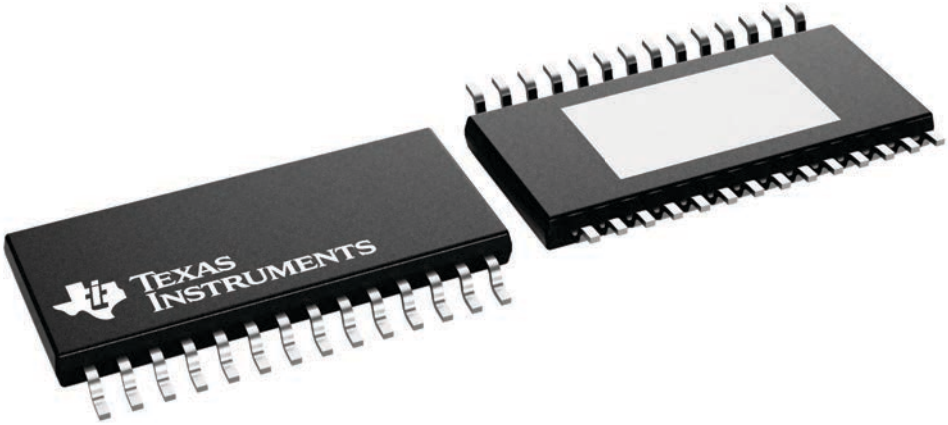
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

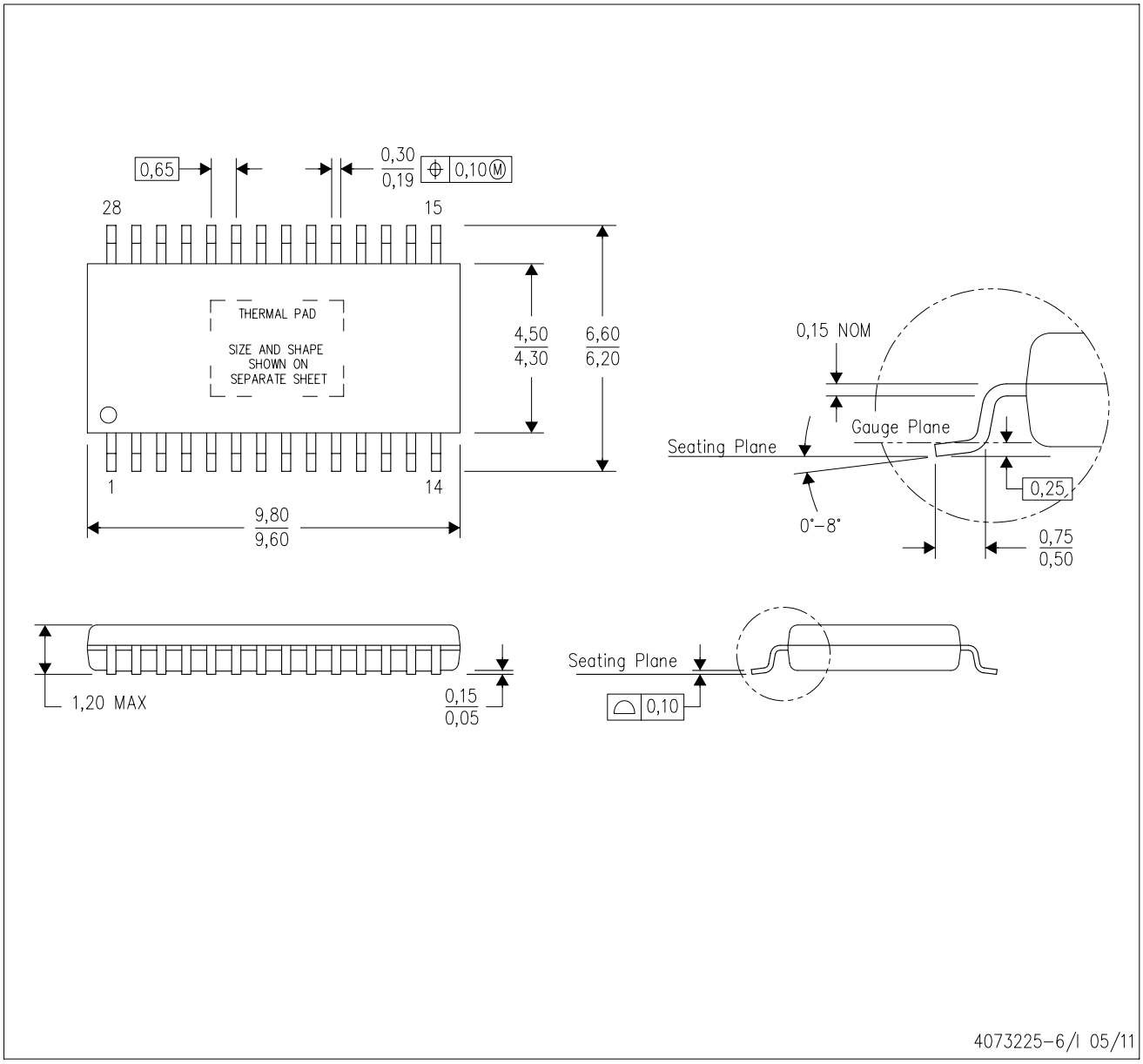
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

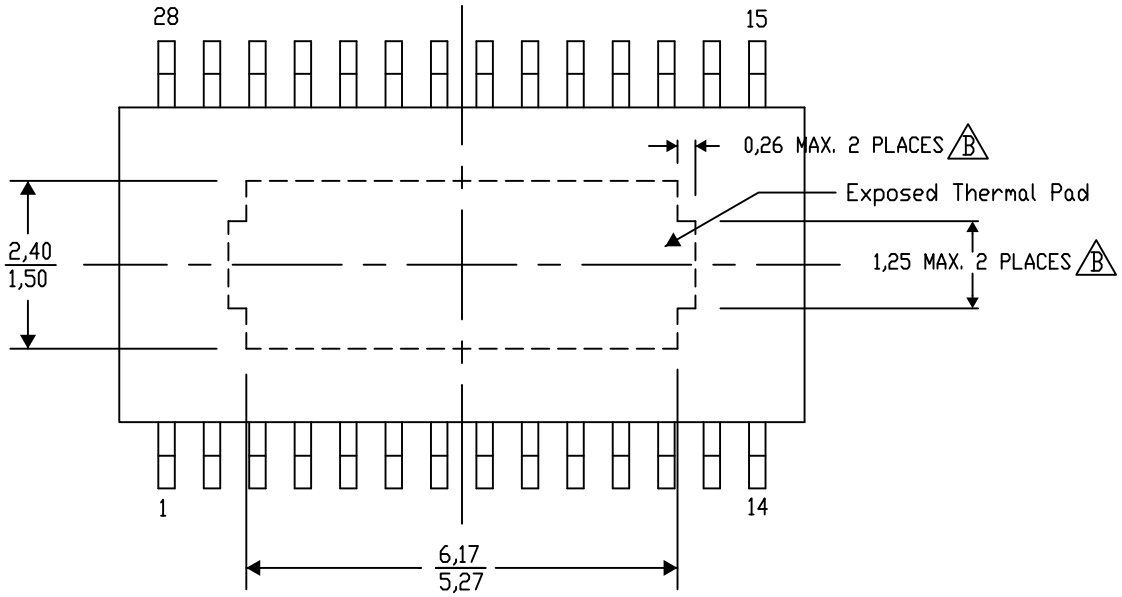
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

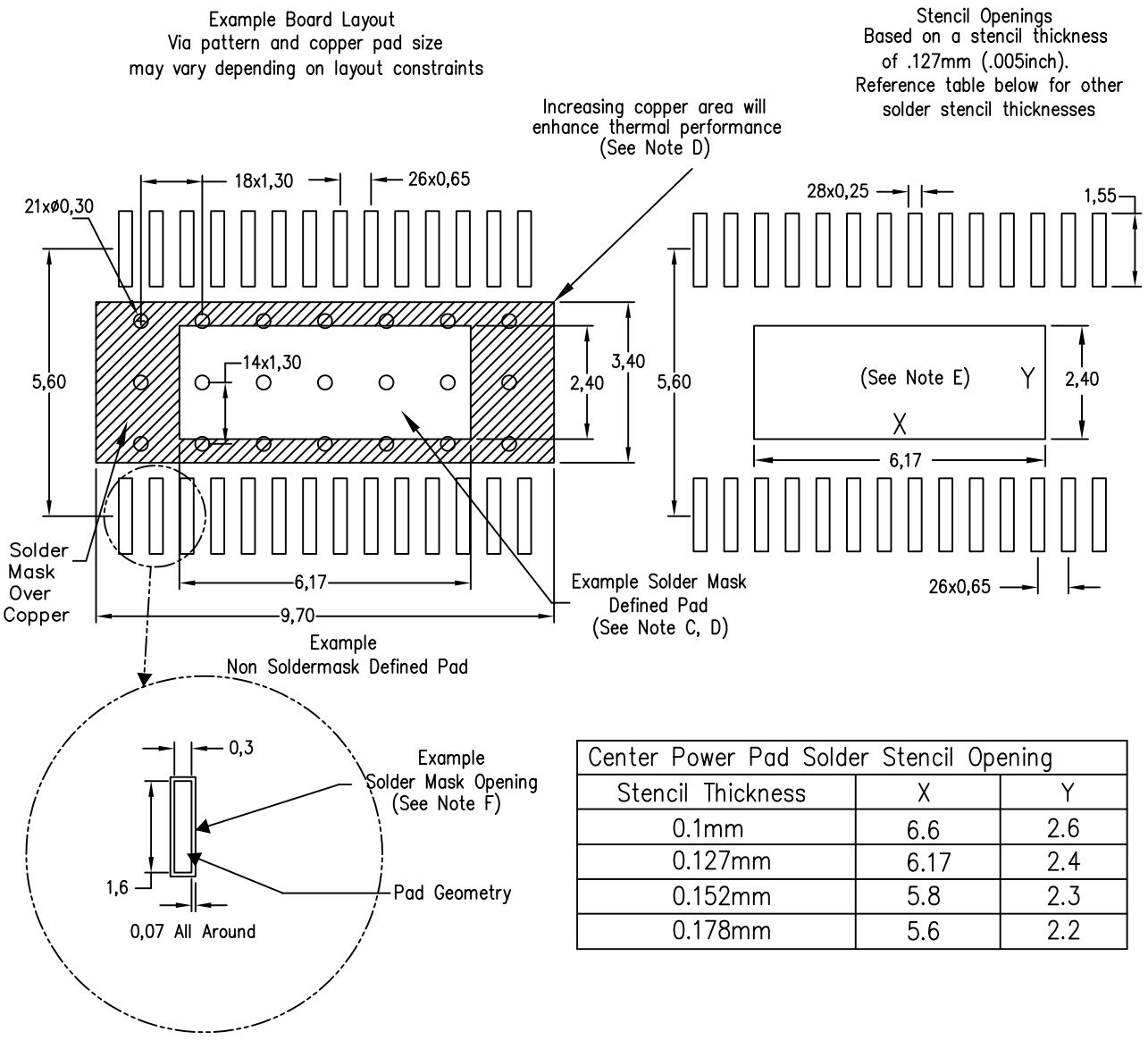
4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

4207609–19/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025