TPD1E04U04 1-Channel ESD Protection Diode with Low R_{DYN} for HDMI 2.0 and USB 3.0

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±16-kV Contact Discharge
  - ±16-kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 2.5 A (8/20 µs)
- IO Capacitance: 0.5-pF (Typ), 0.65-pF (Max)
- Ultra-low ESD Clamping Voltage
  - 8.9 V at 16-A TLP
  - –4.6 V at –16-A TLP
- Low R_{DYN}
  - 0.25 Ω IO to GND
  - 0.18 Ω GND to IO
- DC Breakdown Voltage: 5 V (Minimum)
- Ultra-low Leakage Current: 10 nA (Maximum)
- Supports High Speed Interfaces up to 6 Gbps
- Industrial Temperature Range: –40°C to +125°C
- Industry Standard 0402 and 0201 Packages

2 Applications

- End Equipment
  - Set-Top Boxes
  - Laptops and Desktops
  - TV and Monitors
  - Mobile and Tablets
  - DVR and NVR
- Interfaces
  - HDMI 2.0
  - HDMI 1.4b
  - USB 3.0
  - DisplayPort 1.2
  - PCI Express 3.0

3 Description

The TPD1E04U04 is a unidirectional TVS ESD protection diode for HDMI 2.0 and USB 3.0 circuit protection. The TPD1E04U04 is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

This device features a 0.5-pF IO capacitance making it ideal for protecting high-speed interfaces up to 6 Gbps such as HDMI 2.0 and USB 3.0. The low dynamic resistance and ultra-low clamping voltage ensure system level protection against transient events for sensitive SoCs.

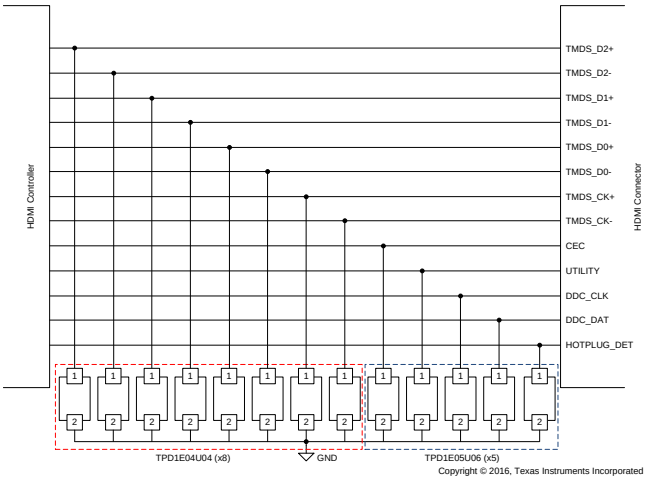
The TPD1E04U04 is offered in the industry standard 0402 (DPY) and 0201 (DPL) packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD1E04U04	X1SON (2)	0.60 mm × 1.00 mm
TPD1E04U04	X2SON (2)	0.60 mm × 0.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical HDMI 2.0 Application



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4 Revision History

Changes from Revision A (April 2016) to Revision B **Page**

- Added new DPL package ... 1
- Added DPL Package information in the *Absolute Maximum Ratings* table ... 4
- Added Thermal information for DPL package in the *Thermal Information* table ... 4
- Changed Vbr min spec from 5 V to 4.5 V in the *Electrical Characteristics* table ... 5

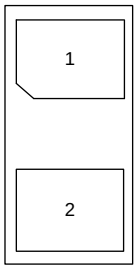
Changes from Original (March 2016) to Revision A **Page**

- Changed device status from *Product Preview* to *Production Data* ... 1

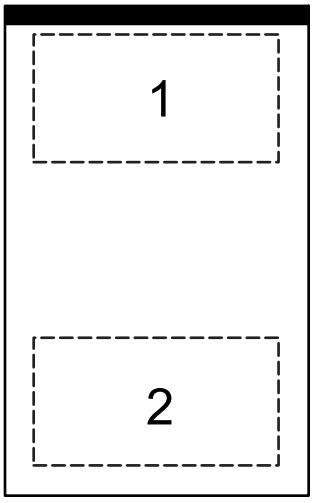
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5 Pin Configuration and Functions

DPL Package
2-Pin X2SON
Top View



DPY Package
2-Pin X1SON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel
2	GND	Ground	Ground. Connect to ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-4 (5/50 ns)		80	A
Peak pulse	IEC 61000-4-5 power (t_p - 8/20 µs) - DPY Package		19	W
	IEC 61000-4-5 power (t_p - 8/20 µs) - DPL Package		16	W
	IEC 61000-4-5 current (t_p - 8/20 µs)		2.5	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±16000	V
		IEC 61000-4-2 air-gap discharge	±16000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	0	3.6	V
T_A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		TPD1E04U04 DPY (X1SON) 2 PINS	TPD1E04U04 DPL (X2SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	683.6	574	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	494.2	332.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	568.7	237.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	217.4	150.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	568.7	238.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA			3.6	V
V_{BR}	Breakdown voltage, IO pin to GND	T_A = 25°C (1)	4.5	6.2	7.5	V
V_F	Forward diode voltage, GND to IO pin	I_{IO} = 1 mA, T_A = 25°C		0.8		V
V_{HOLD}	Holding voltage	I_{IO} = 1 mA		5.3		V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from IO to GND		5.3		V
		I_{PP} = 16 A, TLP, from IO to GND		8.9		
		I_{PP} = 1 A, TLP, from GND to IO		1.3		
		I_{PP} = 16 A, TLP, from GND to IO		4.6		
I_{LEAK}	Leakage current, any IO to GND	V_{IO} = 2.5 V		0.1	10	nA
R_{DYN}	Dynamic resistance	IO to GND		0.25		Ω
		GND to IO		0.18		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, IO to GND, T_A = 25°C		0.5	0.65	pF

(1) Measured as the maximum voltage before device snaps back into V_{HOLD} voltage.

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6.7 Typical Characteristics

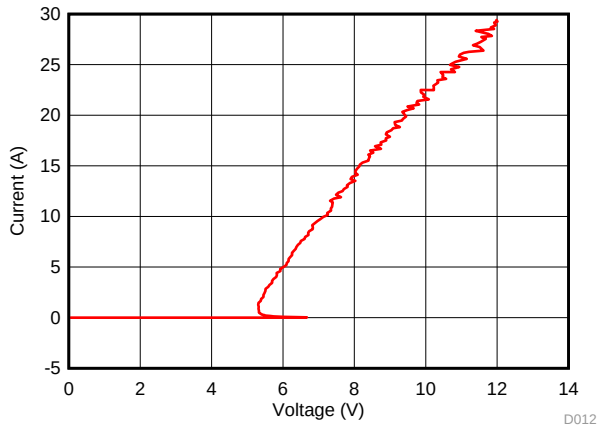


Figure 1. Positive TLP Curve

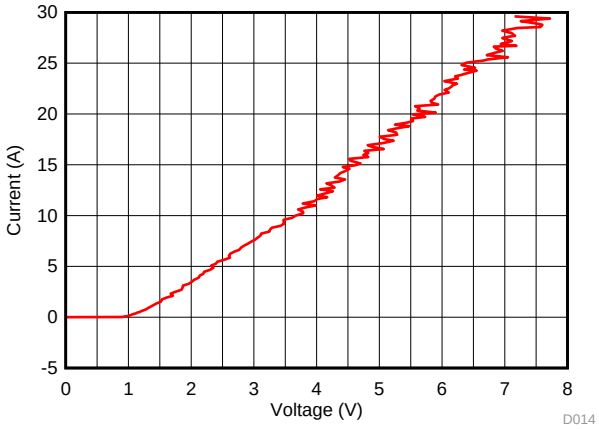


Figure 2. Negative TLP Curve

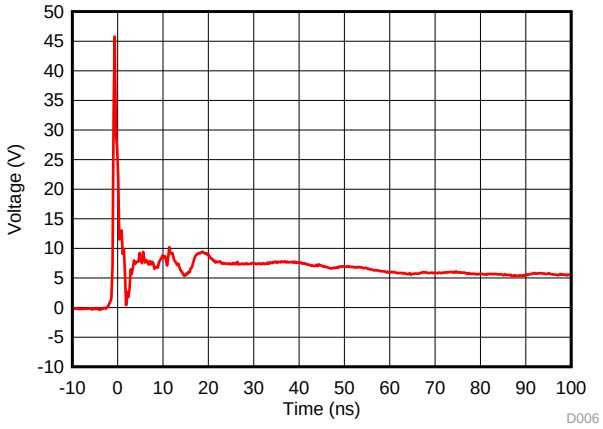


Figure 3. 8-kV IEC Waveform

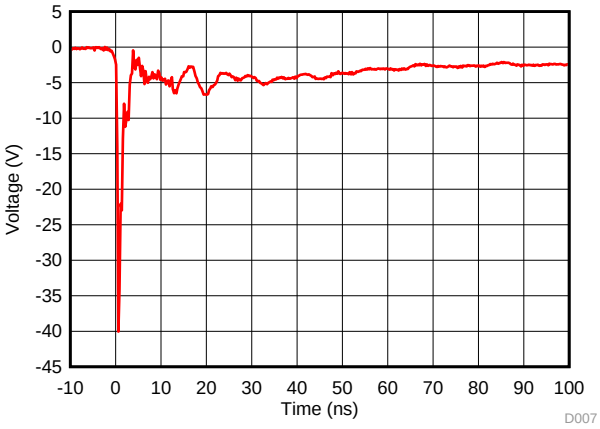


Figure 4. –8-kV IEC Waveform

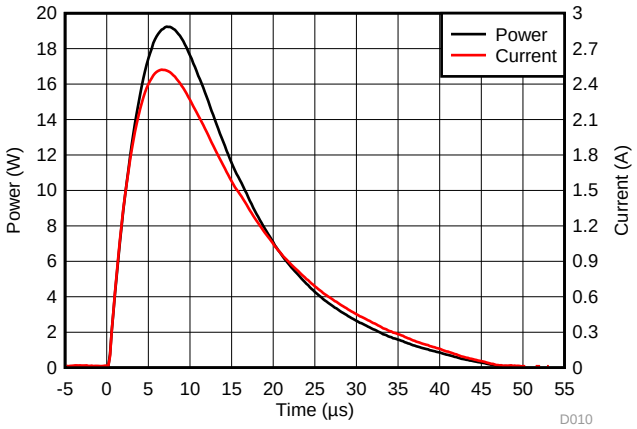


Figure 5. Surge Curve (t_p = 8/20µs), IO Pin to GND

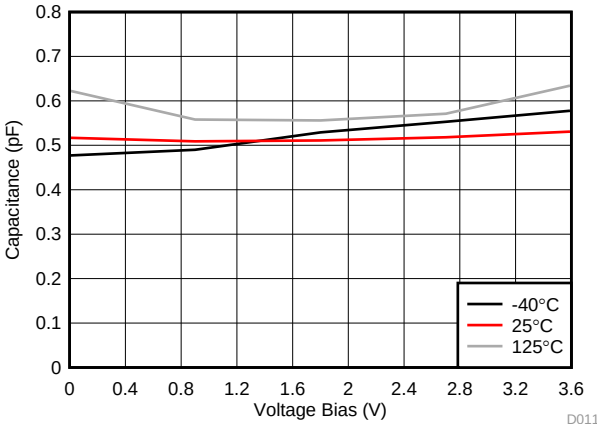


Figure 6. Capacitance vs Bias Voltage

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Typical Characteristics (continued)

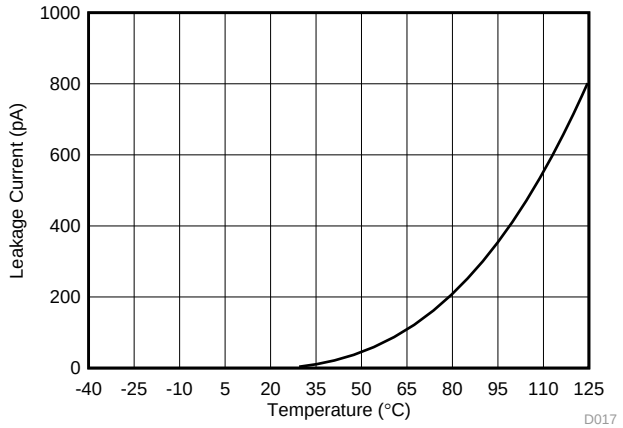


Figure 7. Leakage Current vs Temperature

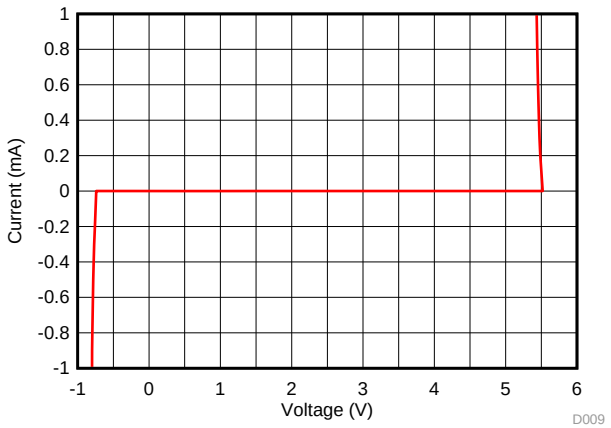


Figure 8. DC Voltage Sweep I-V Curve

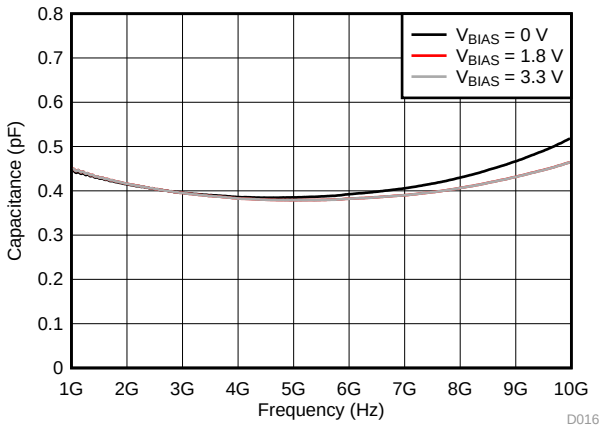


Figure 9. Capacitance vs Frequency

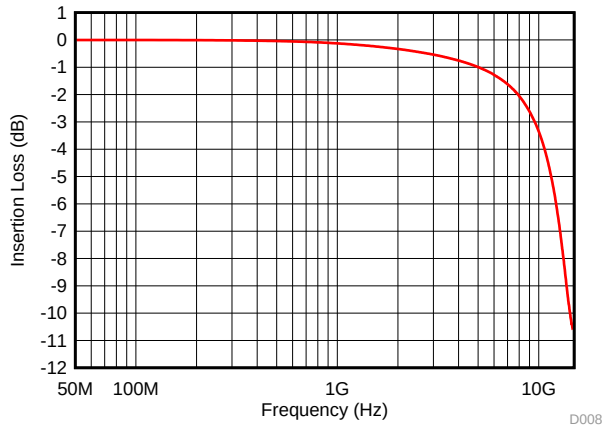


Figure 10. Insertion Loss

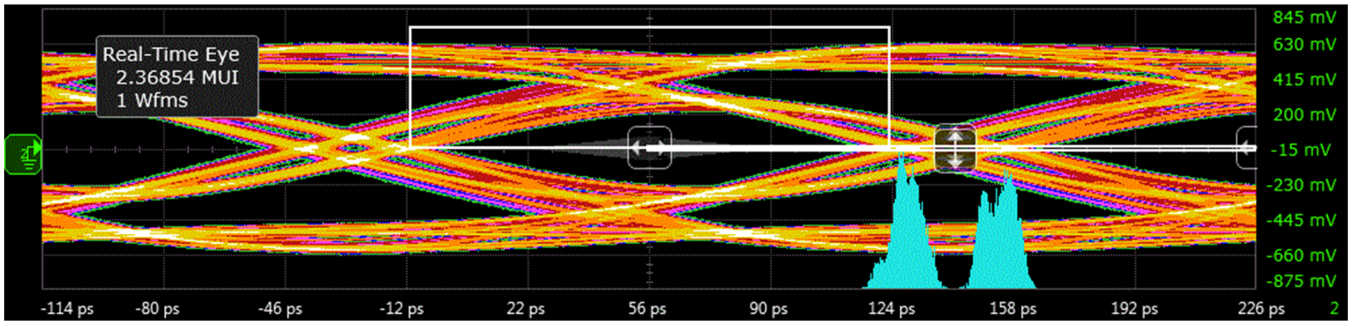


Figure 11. HDMI2.0 6-Gbps TP2 Eye Diagram (Bare Board)

Typical Characteristics (continued)

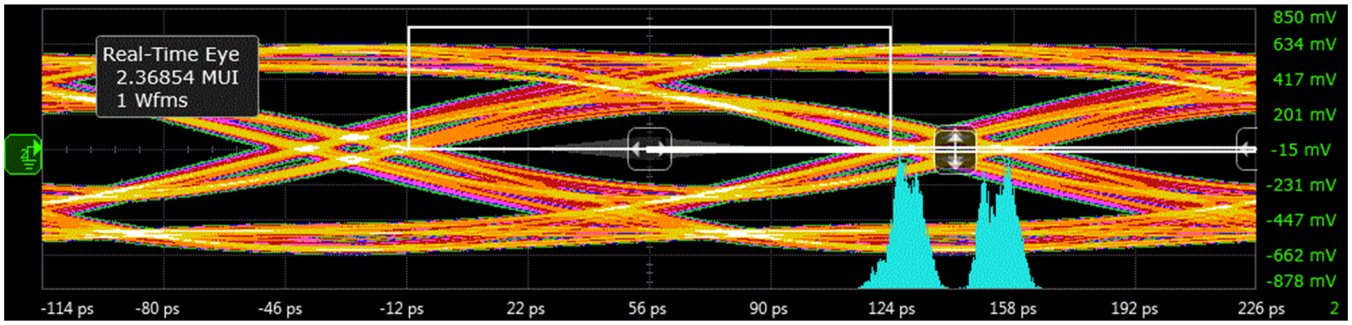


Figure 12. HDMI2.0 6-Gbps TP2 Eye Diagram (With TPD1E04U04)

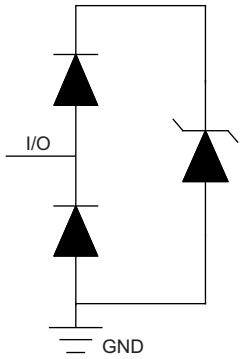
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7 Detailed Description

7.1 Overview

The TPD1E04U04 is a unidirectional ESD Protection Diode with ultra-low capacitance designed for HDMI 2.0 and USB 3.0. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The extremely low clamping voltage and low R_{DYN} make this device ideal for supporting the next-generation small feature size SoCs. The low capacitance also makes this device ideal for protecting any high-speed signal pins on these sensitive interface pins.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The IO pins can withstand ESD events up to ±16-kV contact and ±16-kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The IO pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 2.5 A and 19 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each IO pin to ground is 0.5-pF (typical) and 0.65-pF (maximum). This device supports data rates up to 6 Gbps.

7.3.5 Ultra-Low ESD Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to 8.9 V (I_{TLP} = 16 A) and –4.6 V (I_{TLP} = –16 A).

7.3.6 Low R_{DYN}

The IO pins feature an ESD clamp that has an extremely low R_{DYN} of 0.25 Ω (IO to GND) and 0.18 Ω (GND to IO) which prevents system damage during ESD events.

7.3.7 DC Breakdown Voltage

The DC breakdown voltage of each IO pin is a minimum of 5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 3.6 V.

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Feature Description (continued)

7.3.8 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of 2.5 V.

7.3.9 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 6 Gbps, because of the very low IO capacitance.

7.3.10 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.3.11 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPD1E04U04 is a passive integrated circuit that triggers when voltages are above V_{BR} or below V_F. During ESD events, voltages as high as ±16-kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD1E04U04 (usually within 10s of nano-seconds) the device reverts to passive.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD1E04U04 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

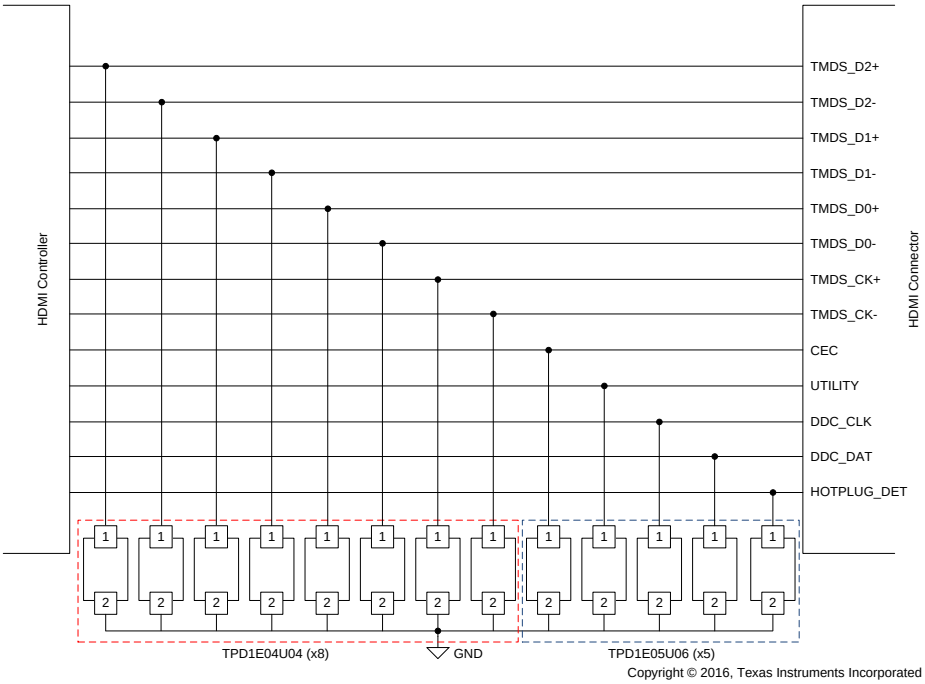


Figure 13. HDMI 2.0 ESD Schematic

8.2.1 Design Requirements

For this design example eight TPD1E04U04 devices and five TPD1E05U06 devices are being used in a HDMI 2.0 application. This provides a complete ESD protection scheme.

Given the HDMI 2.0 application, the parameters listed in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on TMDS lines	0 V to 3.6 V
Operating frequency on TMDS lines	up to 3 GHz
Signal range on control lines	0 V to 5.5 V

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD1E04U04 supports signal ranges between 0 V and 3.6 V, which supports the TMDS pairs on the HDMI 2.0 application. The TPD1E05U06 supports signal ranges between 0 V and 5.5 V, which supports the control lines.

8.2.2.2 Operating Frequency

The TPD1E04U04 has a 0.5-pF (typical) capacitance, which supports the HDMI 2.0 data rates of 6-Gbps. The TPD1E05U06 has a 0.5-pF (typical) capacitance as well, which easily supports the control line data rates.

8.2.3 Application Curves

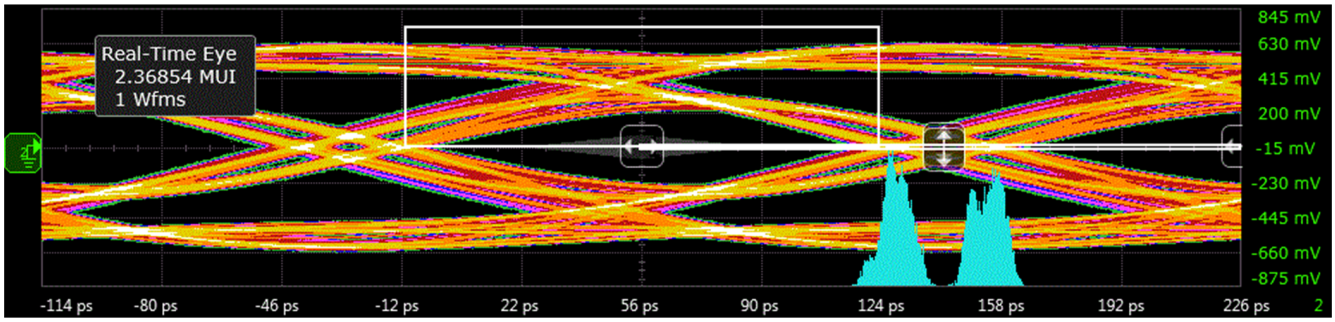


Figure 14. HDMI2.0 6-Gbps TP2 Eye Diagram (Bare Board)

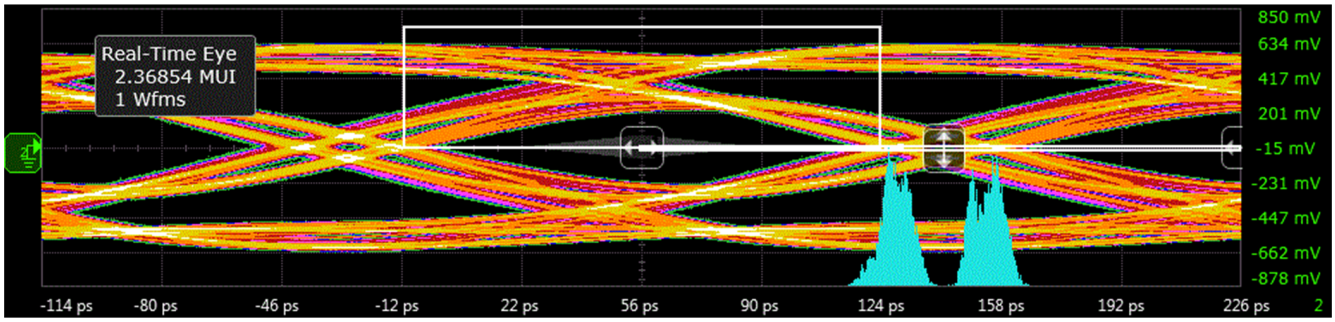


Figure 15. HDMI2.0 6-Gbps TP2 Eye Diagram (With TPD1E04U04)

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9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended IO specification (0 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

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10.2 Layout Example

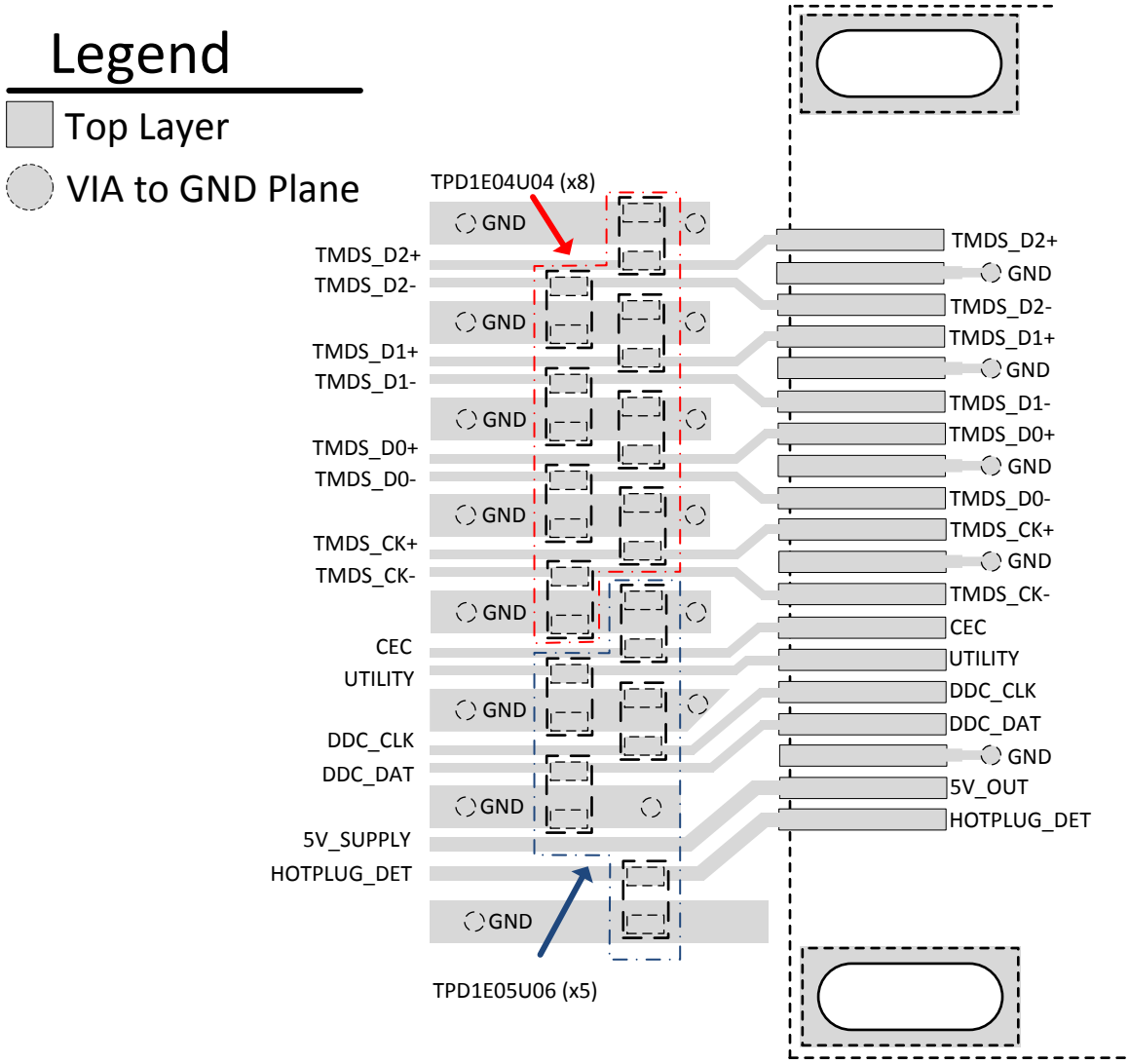


Figure 16. HDMI2.0 Type-A Transmitter Port ESD Layout

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *TPD1E04U04 Evaluation Module User's Guide*
- *Picking ESD Diodes for Ultra High-Speed Data Lines*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD1E04U04DPLR	Active	Production	X2SON (DPL) | 2	15000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K
TPD1E04U04DPLR.B	Active	Production	X2SON (DPL) | 2	15000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K
TPD1E04U04DPLT	Active	Production	X2SON (DPL) | 2	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K
TPD1E04U04DPLT.B	Active	Production	X2SON (DPL) | 2	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K
TPD1E04U04DPLTG4	Active	Production	X2SON (DPL) | 2	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K
TPD1E04U04DPLTG4.B	Active	Production	X2SON (DPL) | 2	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K
TPD1E04U04DPYR	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3K
TPD1E04U04DPYR.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3K
TPD1E04U04DPYRG4	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3K
TPD1E04U04DPYRG4.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3K
TPD1E04U04DPYT	Active	Production	X1SON (DPY) | 2	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3K
TPD1E04U04DPYT.B	Active	Production	X1SON (DPY) | 2	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3K

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

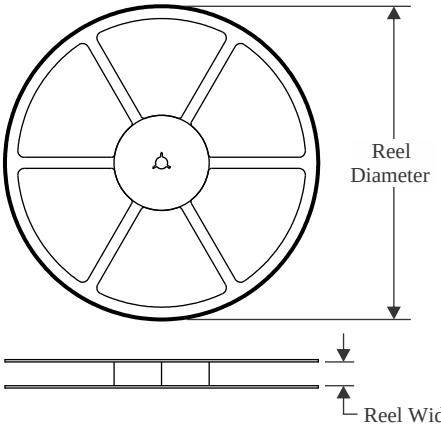
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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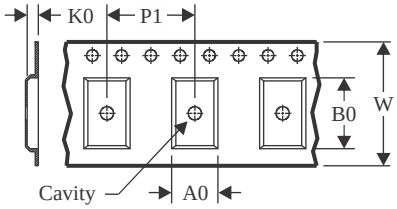
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

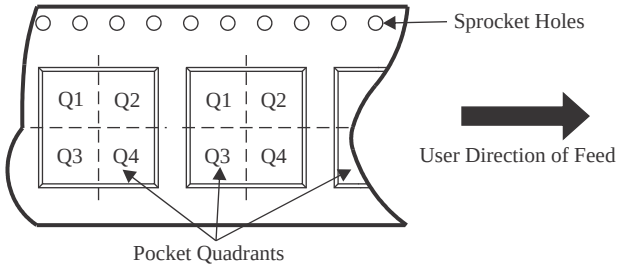


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

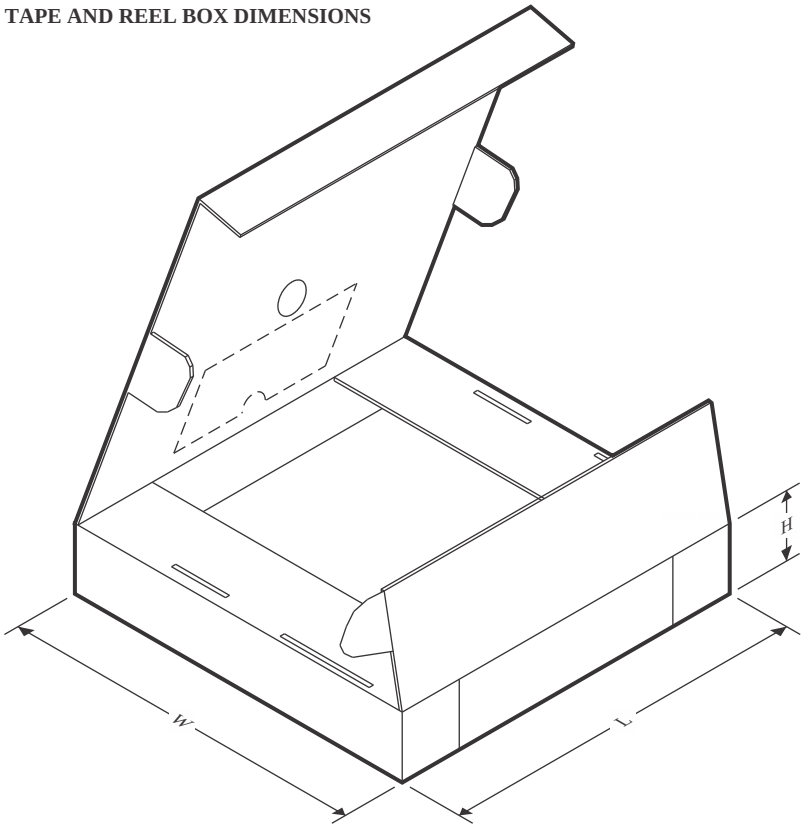
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E04U04DPLR	X2SON	DPL	2	15000	178.0	8.4	0.36	0.66	0.33	2.0	8.0	Q1
TPD1E04U04DPLT	X2SON	DPL	2	250	178.0	8.4	0.36	0.66	0.33	2.0	8.0	Q1
TPD1E04U04DPLTG4	X2SON	DPL	2	250	178.0	8.4	0.36	0.66	0.33	2.0	8.0	Q1
TPD1E04U04DPYR	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2
TPD1E04U04DPYRG4	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2
TPD1E04U04DPYT	X1SON	DPY	2	250	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E04U04DPLR	X2SON	DPL	2	15000	205.0	200.0	33.0
TPD1E04U04DPLT	X2SON	DPL	2	250	205.0	200.0	33.0
TPD1E04U04DPLTG4	X2SON	DPL	2	250	205.0	200.0	33.0
TPD1E04U04DPYR	X1SON	DPY	2	10000	210.0	185.0	35.0
TPD1E04U04DPYRG4	X1SON	DPY	2	10000	210.0	185.0	35.0
TPD1E04U04DPYT	X1SON	DPY	2	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



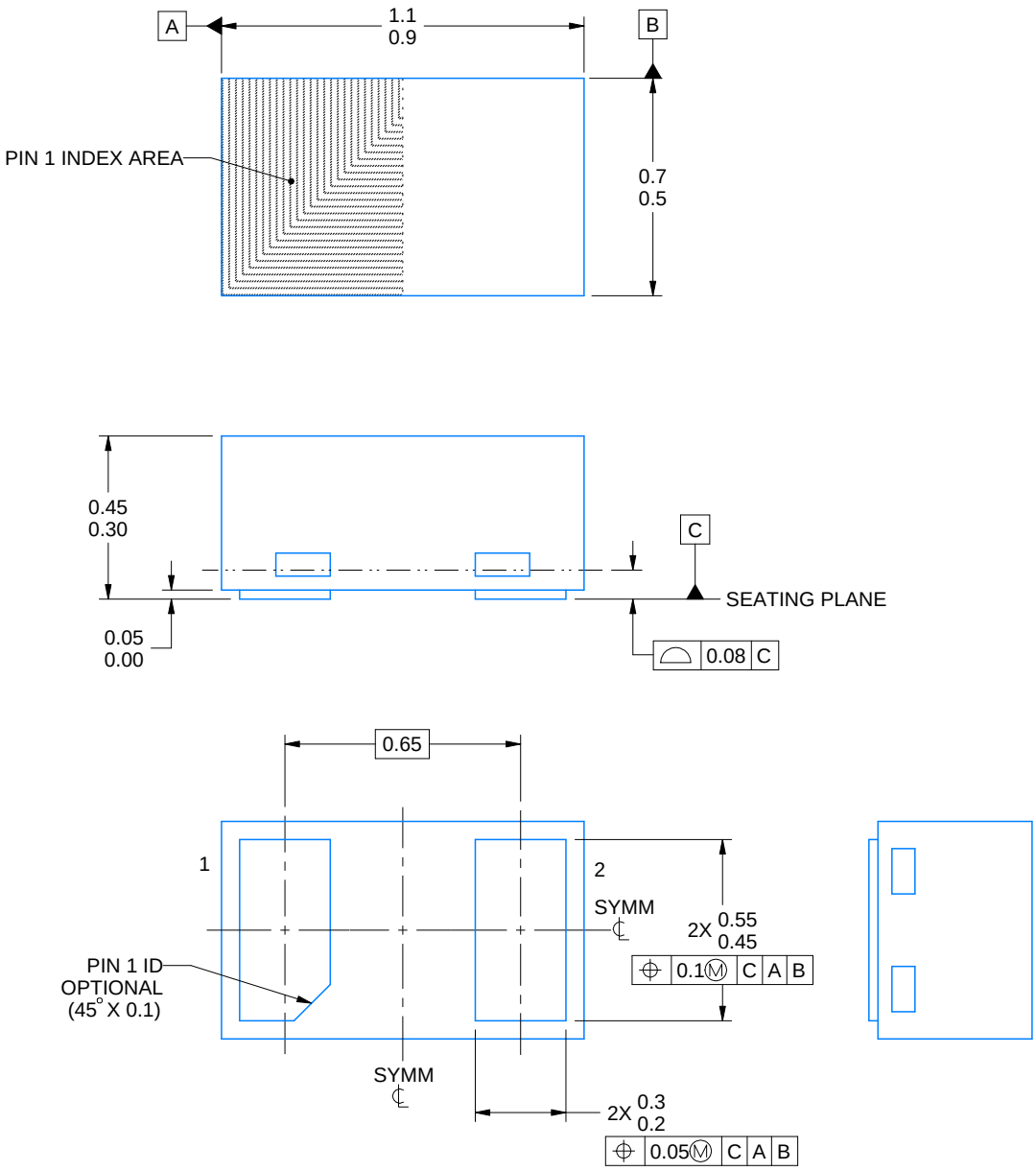
4231484/A

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

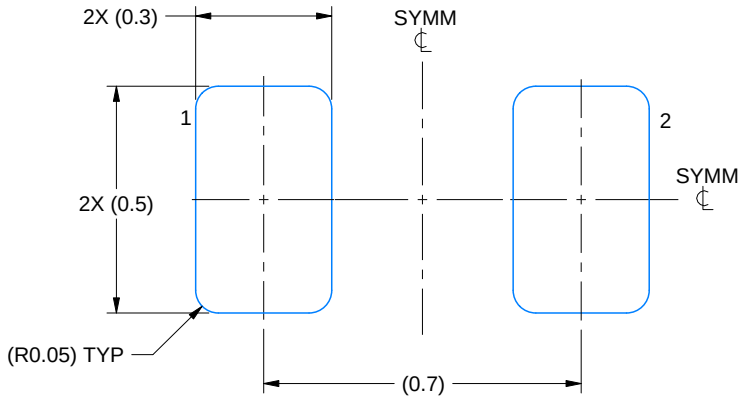
PLASTIC SMALL OUTLINE - NO LEAD



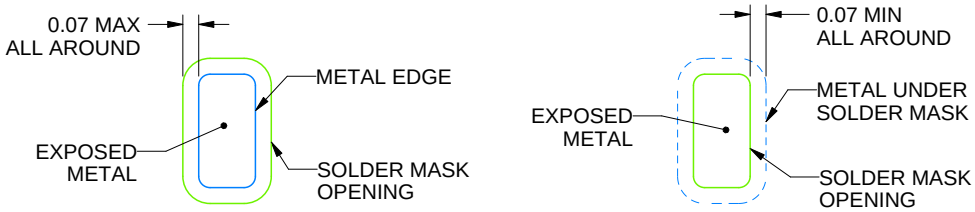
4224561/C 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

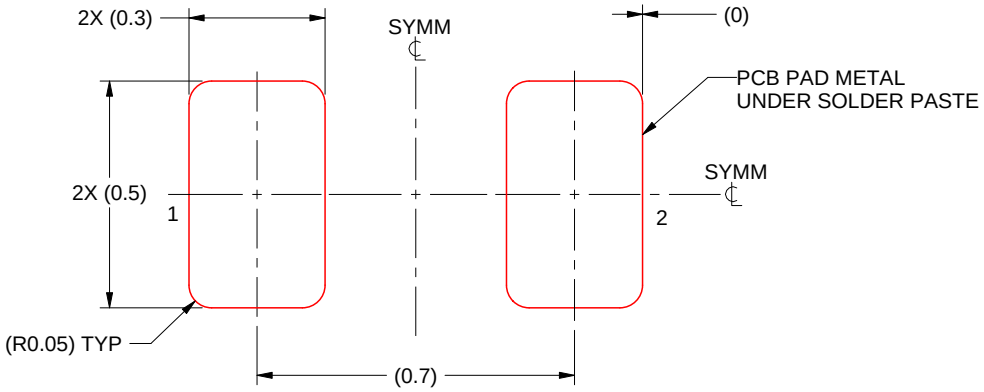


SOLDER MASK DETAILS

4224561/C 07/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



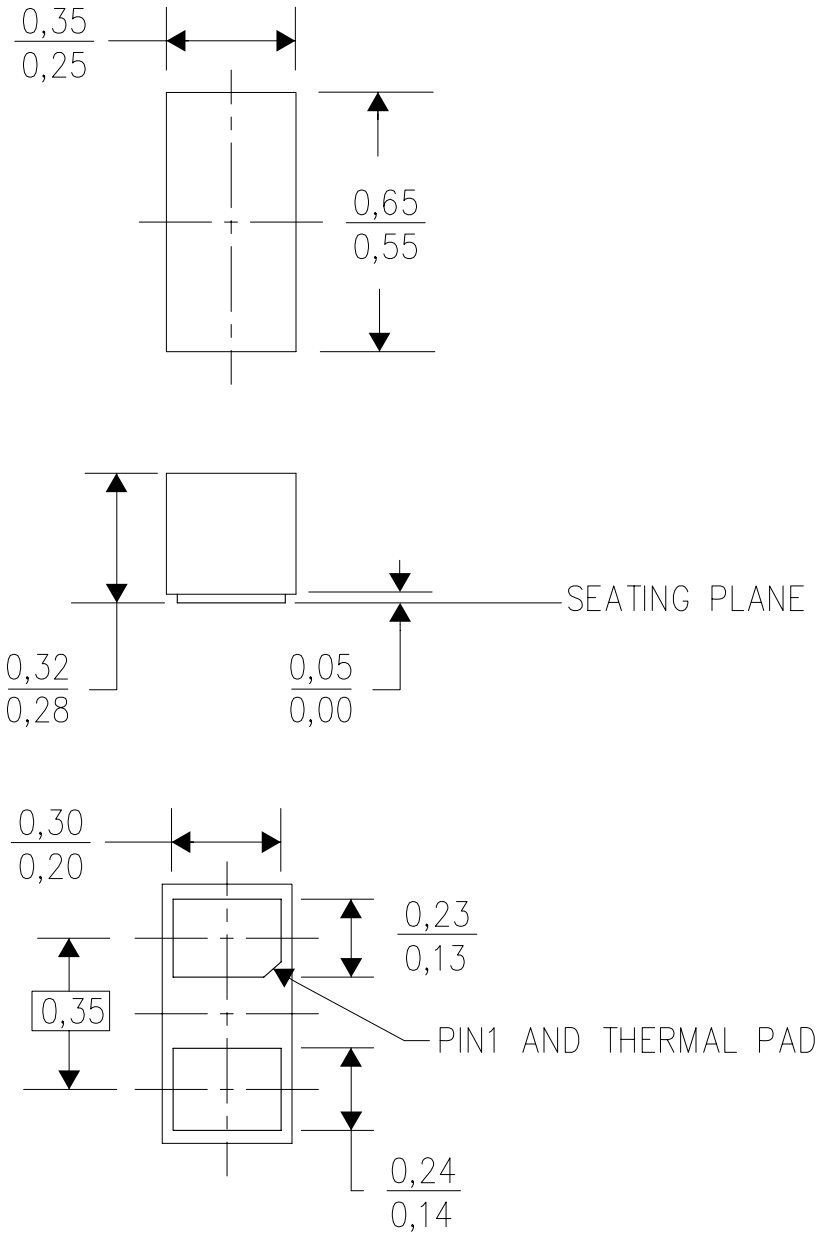
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/C 07/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DPL (R–PX2SON–N2) PLASTIC SMALL OUTLINE NO–LEAD

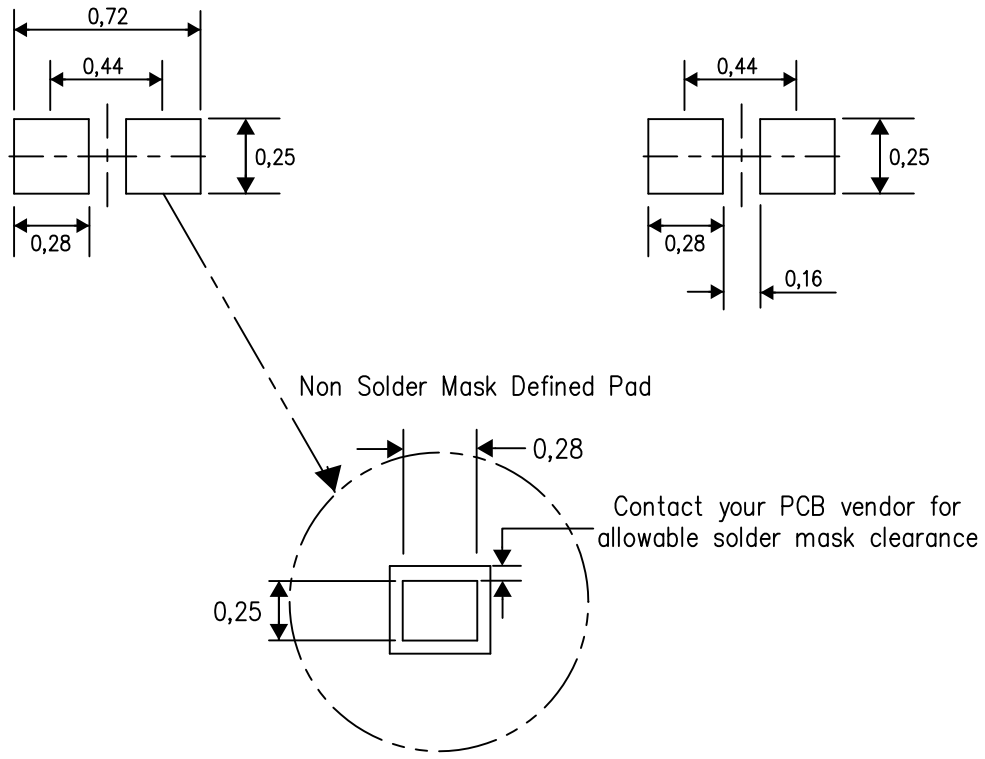


4212149/B 10/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

DPL (R–PX2SON–N2) SMALL PACKAGE OUTLINE NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)

4217903/A 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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Last updated 10/2025