

# TPIC6259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

SLIS009A – APRIL 1992 – REVISED SEPTEMBER 1995

- Low  $r_{DS(on)}$  . . . 1.3  $\Omega$  Typical
- Avalanche Energy . . . 75 mJ
- Eight Power DMOS Transistor Outputs of 250-mA Continuous Current
- 1.5-A Pulsed Current Per Output
- Output Clamp Voltage at 45 V
- Four Distinct Function Modes
- Low Power Consumption

## description

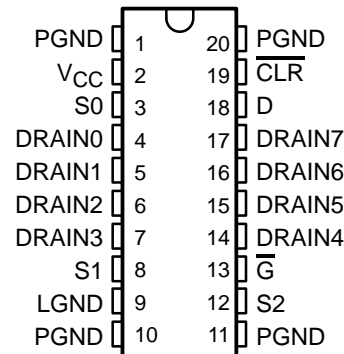
This power logic 8-bit addressable latch controls open-drain DMOS transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multi-functional device capable of storing single-line data in eight addressable latches with 3-to-8 decoding or demultiplexing mode active-low DMOS outputs.

Four distinct modes of operation are selectable by controlling the clear ( $\overline{CLR}$ ) and enable ( $\overline{G}$ ) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable  $\overline{G}$  should be held high (inactive) while the address lines are changing. In the 3-to-8 decoding or demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are high. In the clear mode, all outputs are high and unaffected by the address and data inputs.

Separate power and logic level ground pins are provided to facilitate maximum system flexibility. Pins 1, 10, 11, and 20 are internally connected, and each pin must be externally connected to the power system ground in order to minimize parasitic inductance. A single-point connection between pin 9, logic ground (LGND), and pins 1, 10, 11, and 20, power ground (PGND) must be externally made in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6259 is characterized for operation over the operating case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

DW OR N PACKAGE  
(TOP VIEW)



FUNCTION TABLE

INPUTS			OUTPUT OF ADDRESSED DRAIN	EACH OTHER DRAIN	FUNCTION
$\overline{CLR}$	$\overline{G}$	D			
H	L	H	L	$Q_{i0}$	Addressable Latch
H	L	L	H	$Q_{i0}$	
H	H	X	$Q_{i0}$	$Q_{i0}$	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	
L	H	X	H	H	Clear

LATCH SELECTION TABLE

SELECT INPUTS			DRAIN ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7



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**TEXAS  
INSTRUMENTS**

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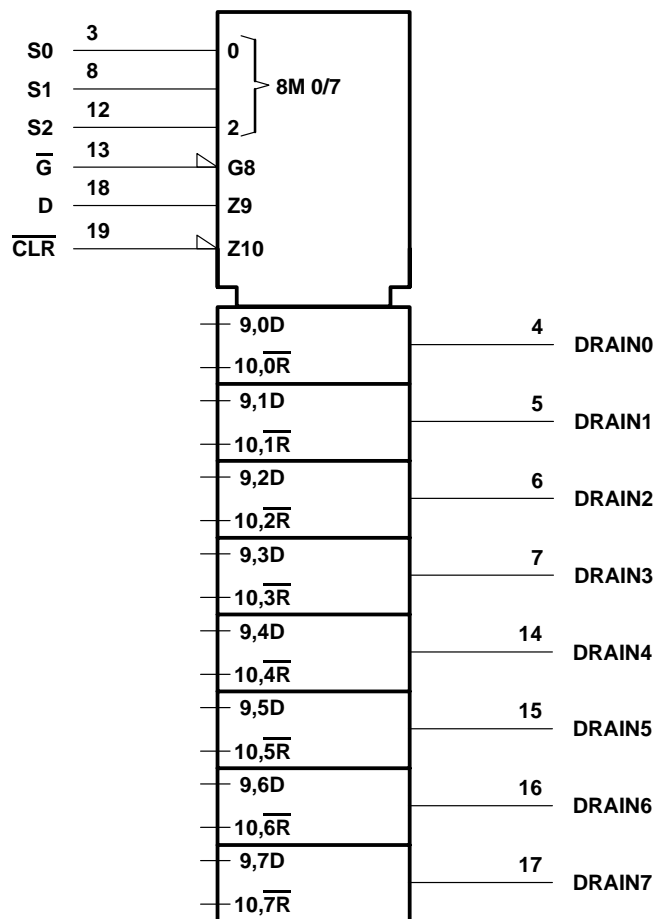
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# TPIC6259

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logic symbol†

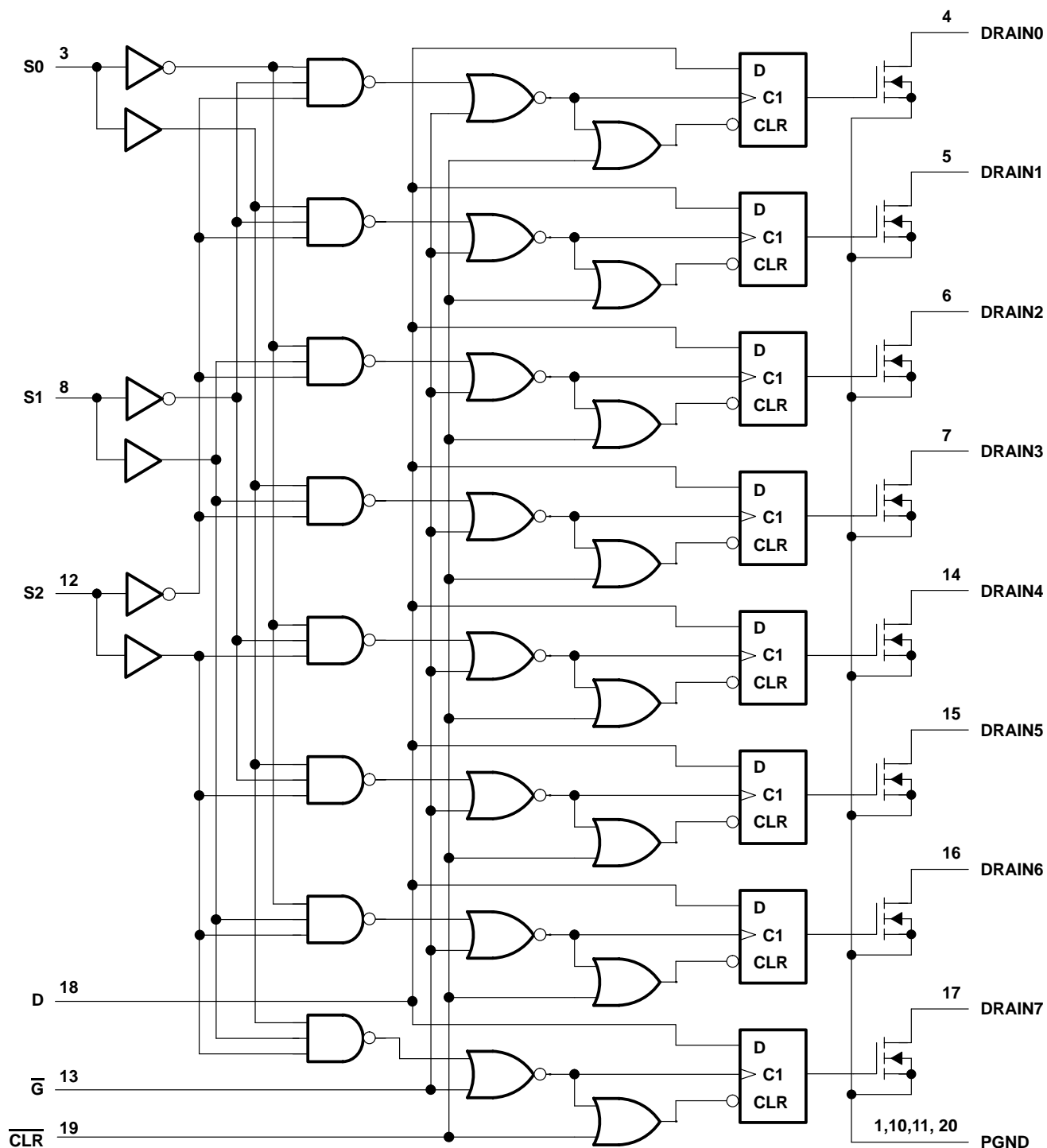


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



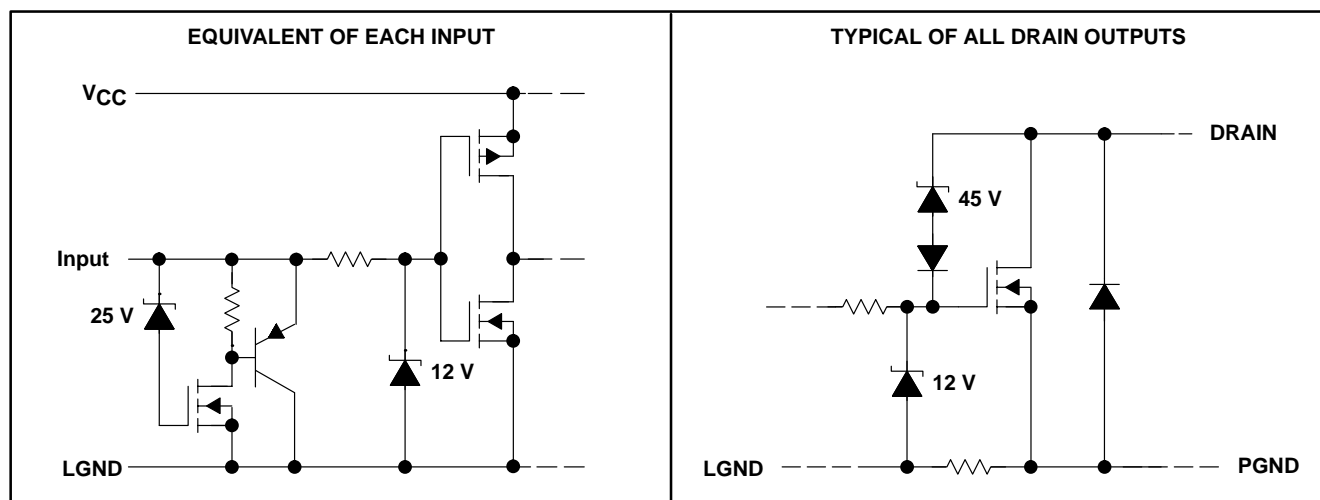
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# TPIC6259

## POWER LOGIC 8-BIT ADDRESSABLE LATCH

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### schematic of inputs and outputs



### absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)<sup>†</sup>

Logic supply voltage, $V_{CC}$ (see Note 1)	7 V
Logic input voltage range, $V_I$	–0.3 V to 7 V
Power DMOS drain-to-source voltage, $V_{DS}$ (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, $I_{Dn}$ , $T_A = 25^\circ\text{C}$ (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, $I_{Dn}$ , $T_A = 25^\circ\text{C}$	250 mA
Peak drain current single output, $I_{DM}$ , $T_A = 25^\circ\text{C}$ (see Note 3)	2 A
Single-pulse avalanche energy, $E_{AS}$ (see Note 4)	75 mJ
Avalanche current, $I_{AS}$ (see Note 4)	1 A
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$	–40°C to 150°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to LGND and PGND.
  2. Each power DMOS source is internally connected to PGND.
  3. Pulse duration  $\leq 100 \mu\text{s}$ , duty cycle  $\leq 2\%$
  4. DRAIN supply voltage = 15 V, starting junction temperature,  $(T_{JS}) = 25^\circ\text{C}$ ,  $L = 100 \text{ mH}$ ,  $I_{AS} = 1 \text{ A}$  (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 125^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

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**recommended operating conditions over recommended operating temperature range (unless otherwise noted)**

	MIN	MAX	UNIT
Logic supply voltage, $V_{CC}$	4.5	5.5	V
High-level input voltage, $V_{IH}$	0.85 $V_{CC}$		V
Low-level input voltage, $V_{IL}$		0.15 $V_{CC}$	V
Pulsed drain output current, $T_C = 25^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ (see Notes 3 and 5)	-1.8	1.5	A
Setup time, D high before $\overline{G}\uparrow$ , $t_{SU}$ (see Figure 2)	10		ns
Hold time, D high after $\overline{G}\uparrow$ , $t_H$ (see Figure 2)	5		ns
Pulse duration, $t_W$ (see Figure 2)	15		ns
Operating case temperature, $T_C$	-40	125	$^\circ\text{C}$

**electrical characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>(BR)DSX</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA		45			V
V <sub>SD</sub>	Source-drain diode forward voltage	I <sub>F</sub> = 250 mA,	See Note 3		0.85	1	V
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub>			1	μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0			−1	μA
I <sub>CC</sub>	Logic supply current	I <sub>O</sub> = 0,	All inputs low		15	100	μA
I <sub>N</sub>	Nominal current	V <sub>DS(on)</sub> = 0.5 V, I <sub>N</sub> = I <sub>D</sub> , T <sub>C</sub> = 85°C, See Notes 5, 6, and 7			250		mA
I <sub>DSX</sub>	Off-state drain current	V <sub>DS</sub> = 40 V			0.05	1	μA
		V <sub>DS</sub> = 40 V, T <sub>C</sub> = 125°C			0.15	5	
r <sub>DS(on)</sub>	Static drain-source on-state resistance	I <sub>D</sub> = 250 mA, V <sub>CC</sub> = 4.5 V	See Notes 5 and 6 and Figures 8 and 9		1.3	2	Ω
		I <sub>D</sub> = 250 mA, V <sub>CC</sub> = 4.5 V T <sub>C</sub> = 125°C,			2	3.2	
		I <sub>D</sub> = 500 mA, V <sub>CC</sub> = 4.5 V			1.3	2	

**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output from D	$C_L = 30\text{ pF}$ , $I_D = 250\text{ mA}$ , See Figures 1, 2, and 10		625		ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from D			140		ns
$t_r$ Rise time, drain output			650		ns
$t_f$ Fall time, drain output			400		ns
$t_a$ Reverse-recovery-current rise time	$I_F = 250\text{ mA}$ , $di/dt = 20\text{ A}/\mu\text{s}$ , See Notes 5 and 6 and Figure 3		100		ns
$t_{rr}$ Reverse-recovery time			300		

- NOTES: 3. Pulse duration  $\leq 100\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
5. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.  
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of  $0.5\text{ V}$  at  $T_C = 85^\circ\text{C}$ .

**thermal resistance**

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$ Thermal resistance junction-to-ambient	DW package		111	$^\circ\text{C}/\text{W}$
	N package		108	



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## PARAMETER MEASUREMENT INFORMATION

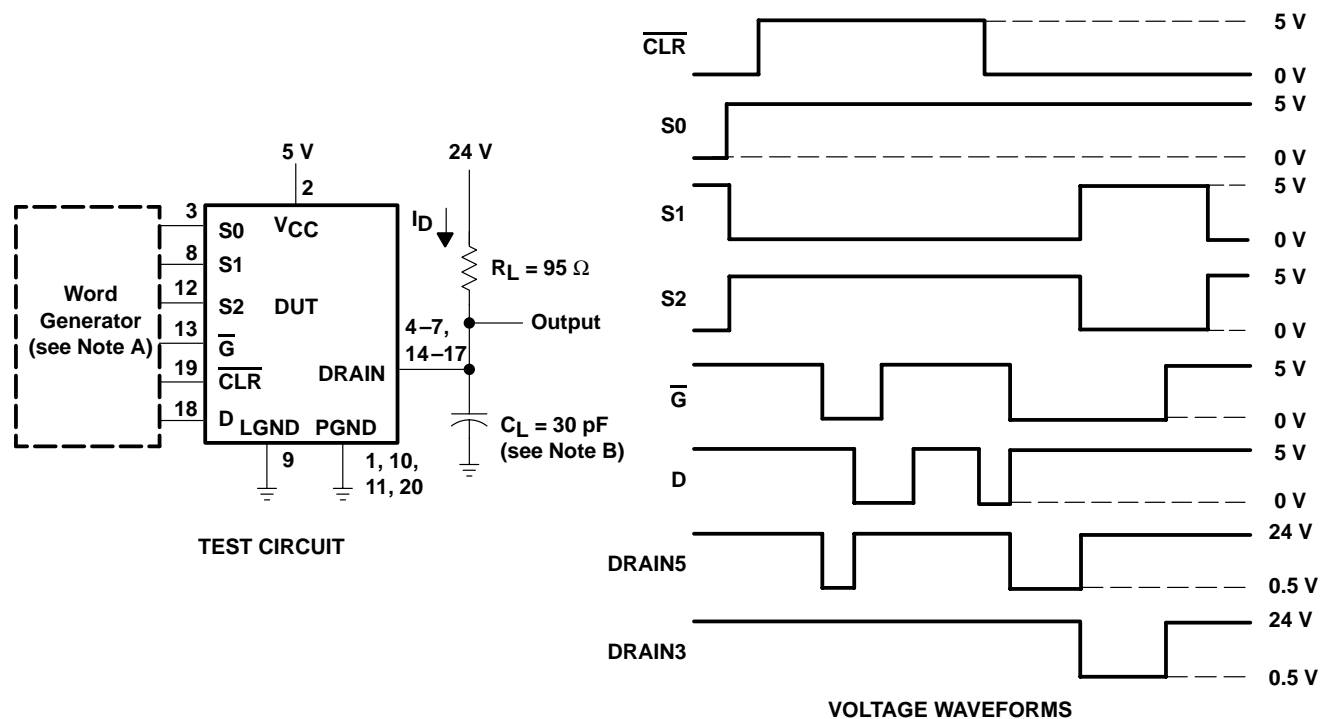


Figure 1. Typical Operation Mode

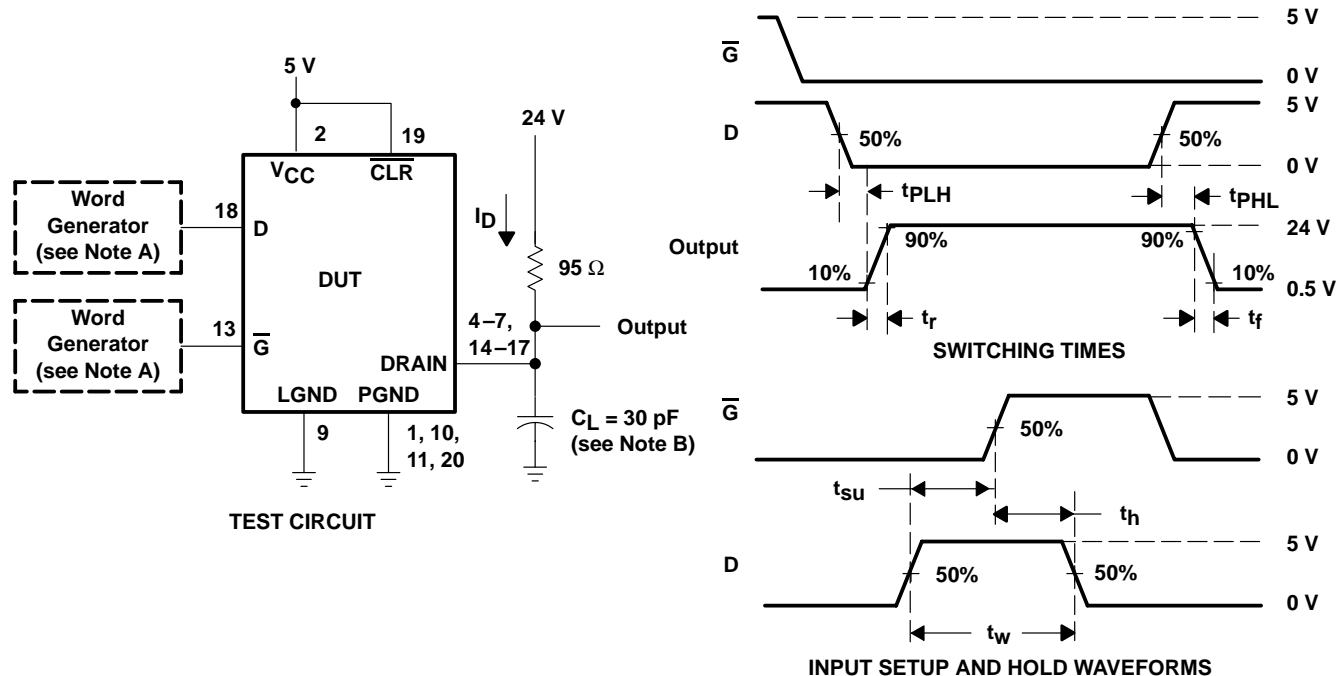


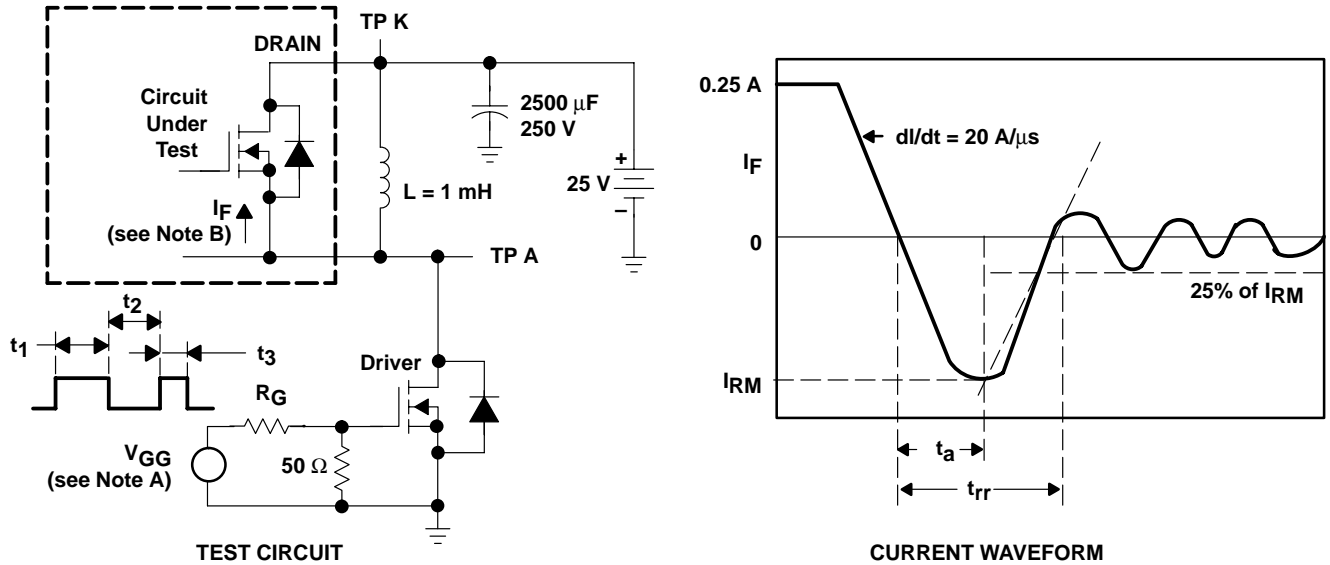
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $t_w = 300$  ns, pulsed repetition rate (PRR) = 5 kHz,  $Z_O = 50$   $\Omega$ .  
B.  $C_L$  includes probe and jig capacitance.



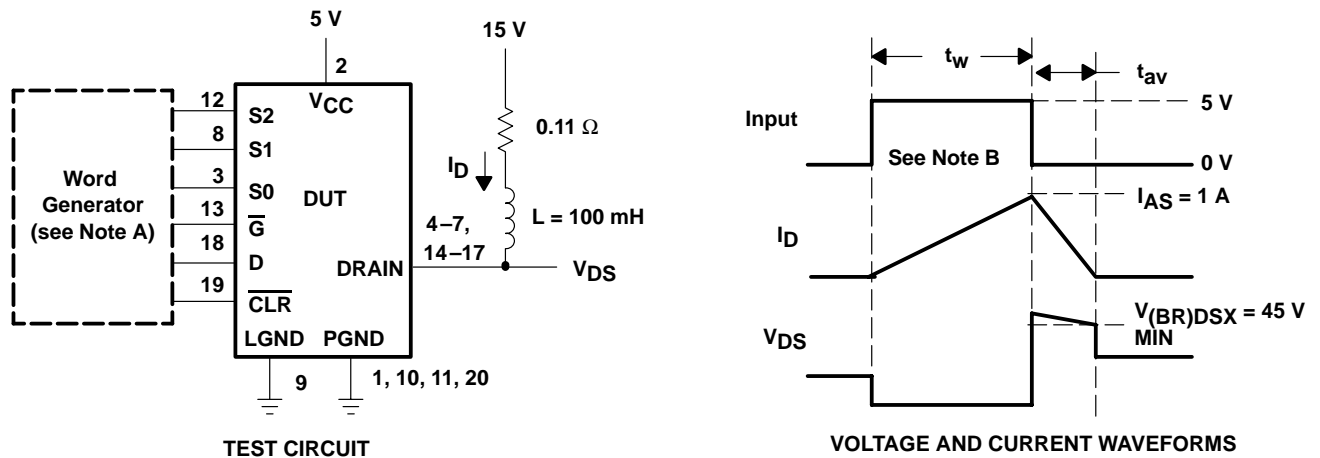
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### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The  $V_{GG}$  amplitude and  $R_G$  are adjusted for  $di/dt = 20 \text{ A}/\mu\text{s}$ . A  $V_{GG}$  double-pulse train is used to set  $I_F = 0.25 \text{ A}$ , where  $t_1 = 10 \mu\text{s}$ ,  $t_2 = 7 \mu\text{s}$ , and  $t_3 = 3 \mu\text{s}$ .
- B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

**Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode**



- NOTES: A. The pulse generator has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $Z_0 = 50 \Omega$ .
- B. Input pulse duration,  $t_w$ , is increased until peak current  $I_{AS} = 1 \text{ A}$ .  
 Energy test level is defined as  $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 75 \text{ mJ}$ .

**Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms**

# TPIC6259

## POWER LOGIC 8-BIT ADDRESSABLE LATCH

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### TYPICAL CHARACTERISTICS

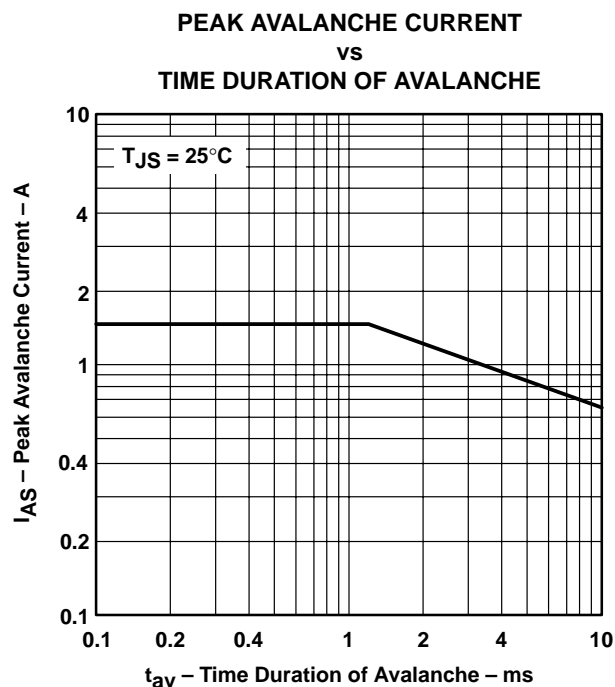


Figure 5

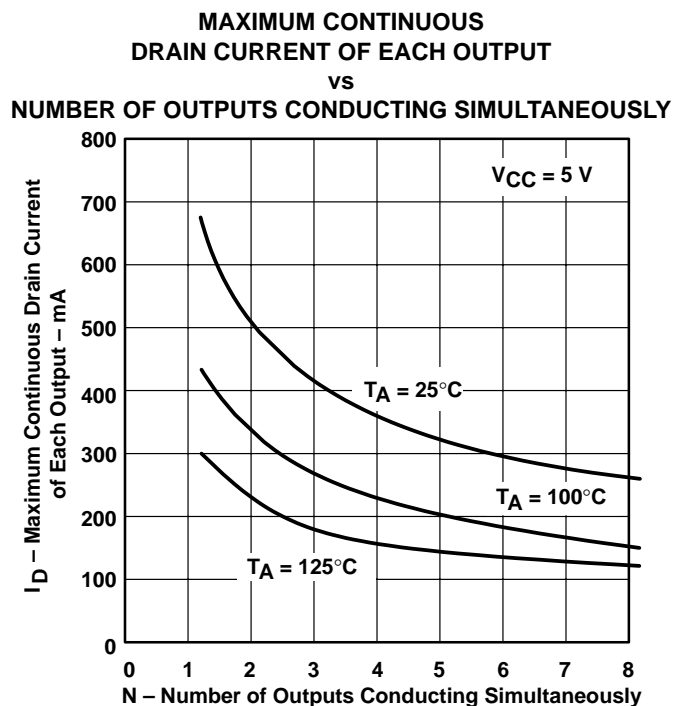


Figure 6

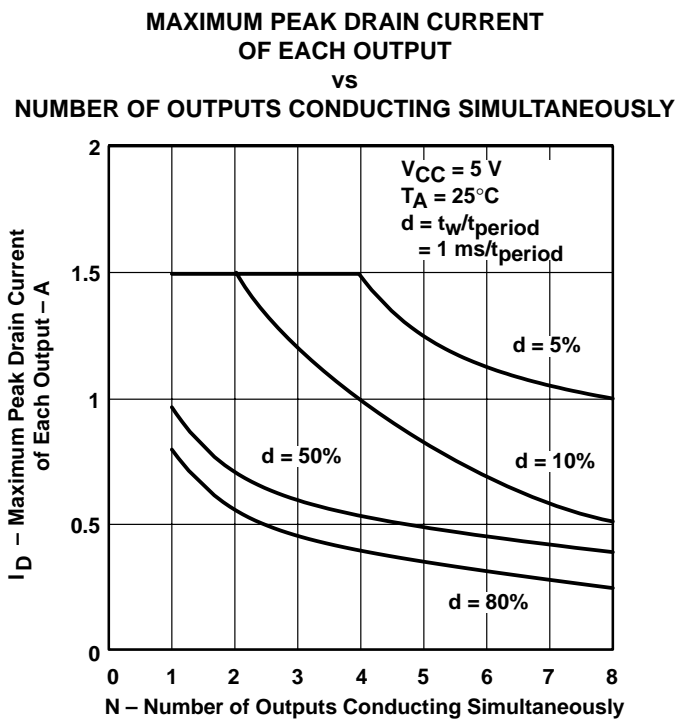
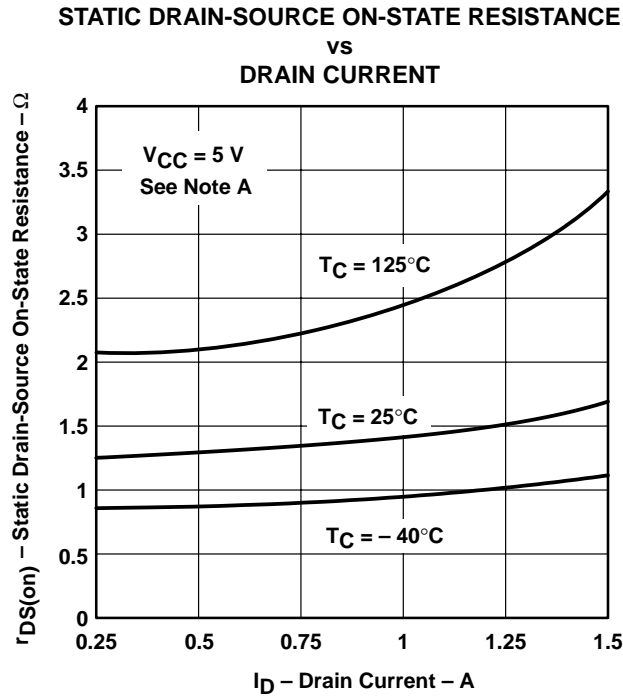


Figure 7

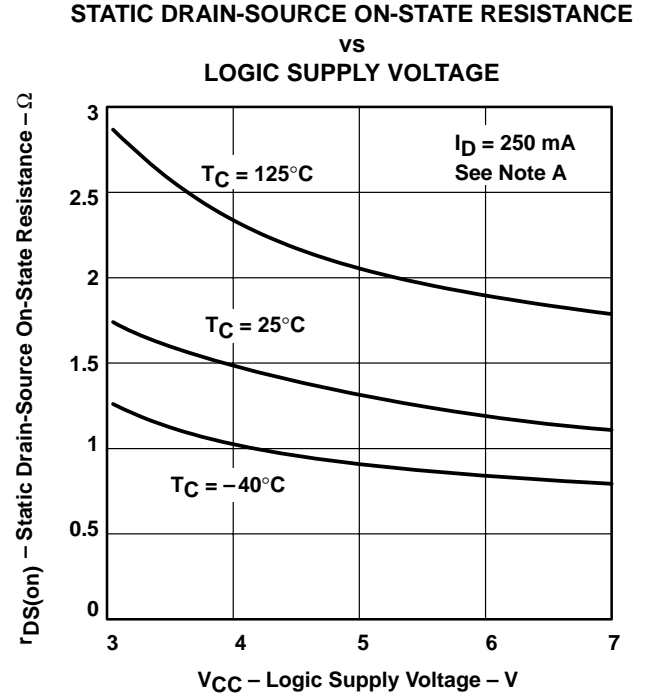




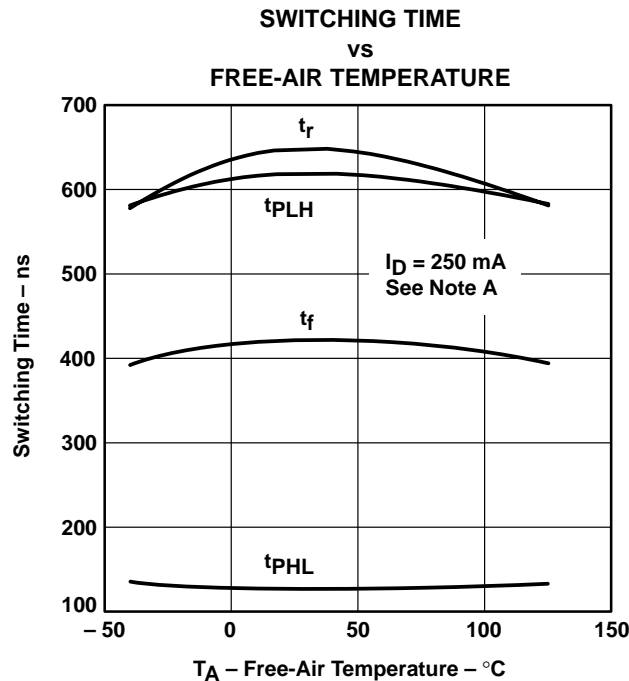
## TYPICAL CHARACTERISTICS



**Figure 8**



**Figure 9**



**Figure 10**

NOTE A: Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPIC6259DW</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6259
TPIC6259DW.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6259
<a href="#">TPIC6259DWG4</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	TPIC6259
TPIC6259DWG4.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6259
<a href="#">TPIC6259DWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6259
TPIC6259DWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6259
<a href="#">TPIC6259DWRG4</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TPIC6259
TPIC6259DWRG4.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6259
<a href="#">TPIC6259N</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPIC6259N
TPIC6259N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPIC6259N

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6259DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TPIC6259DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6259DWR	SOIC	DW	20	2000	350.0	350.0	43.0
TPIC6259DWRG4	SOIC	DW	20	2000	350.0	350.0	43.0

## TUBE



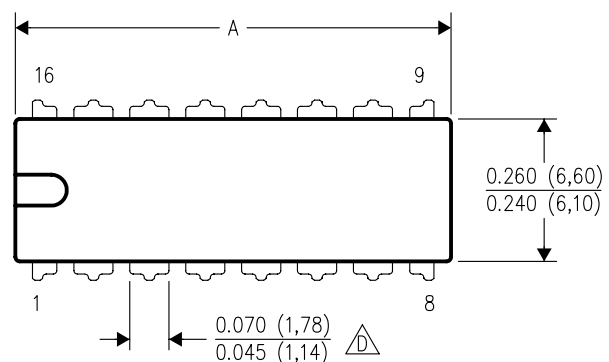
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPIC6259DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TPIC6259DW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6
TPIC6259DWG4	DW	SOIC	20	25	506.98	12.7	4826	6.6
TPIC6259DWG4.A	DW	SOIC	20	25	506.98	12.7	4826	6.6
TPIC6259N	N	PDIP	20	20	506	13.97	11230	4.32
TPIC6259N.A	N	PDIP	20	20	506	13.97	11230	4.32

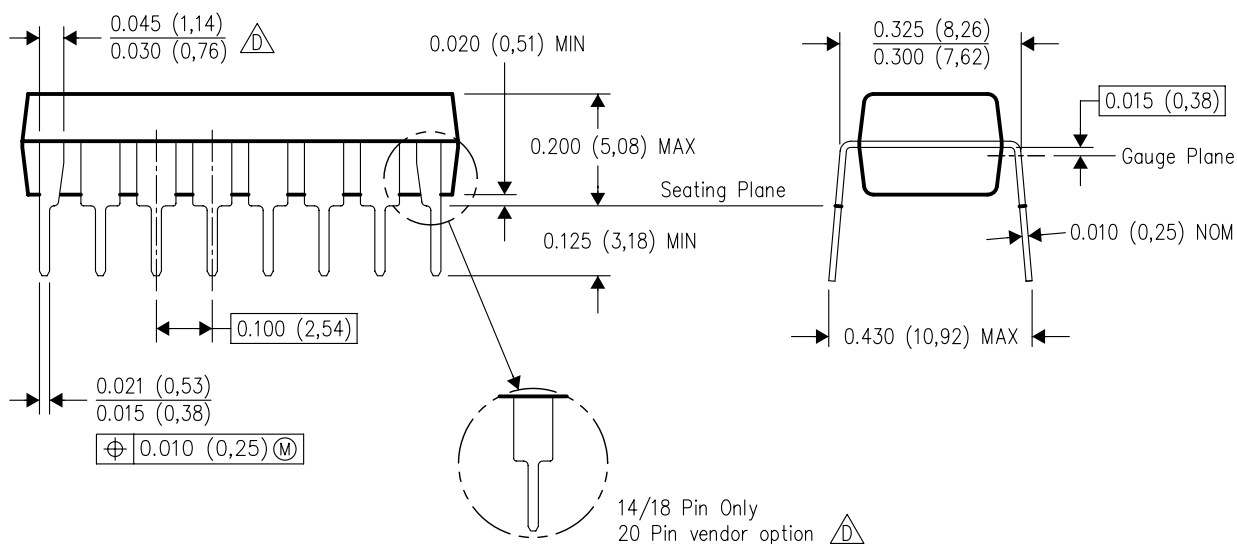
N (R-PDIP-T\*\*)

16 PINS SHOWN



## PLASTIC DUAL-IN-LINE PACKAGE

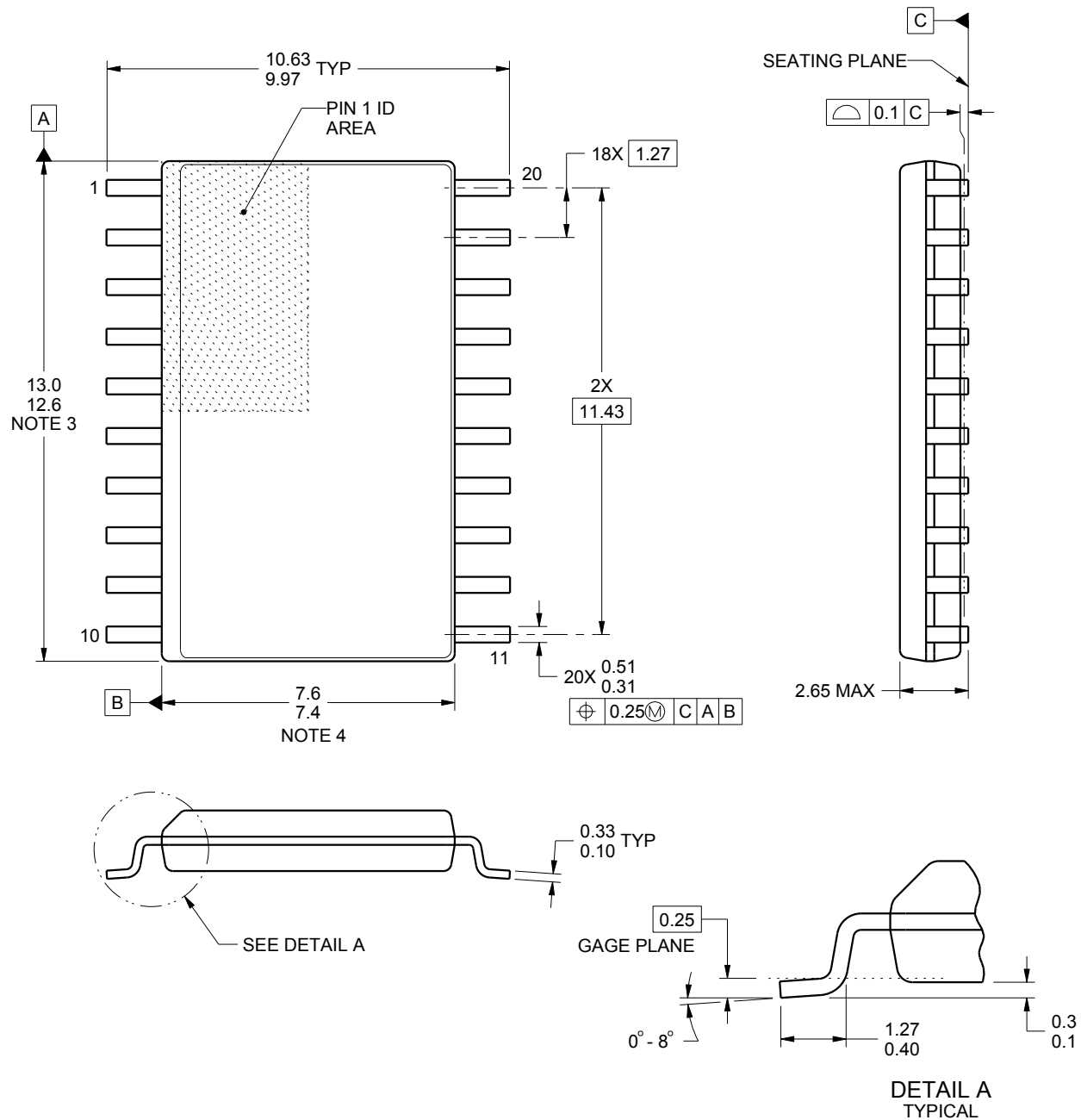
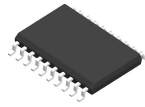


PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

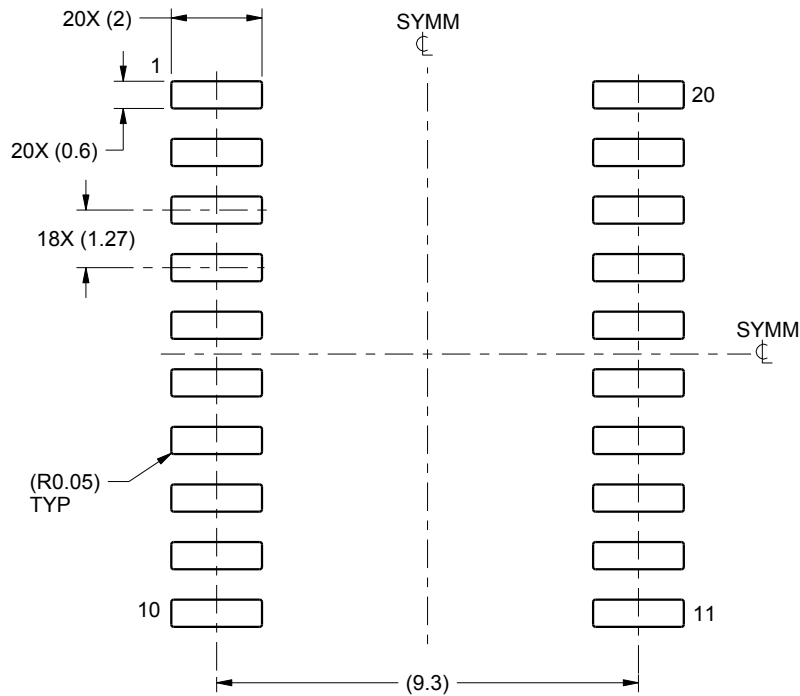


# EXAMPLE BOARD LAYOUT

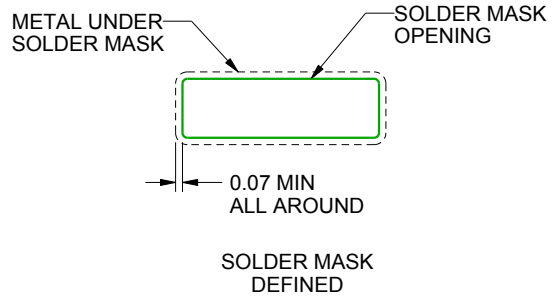
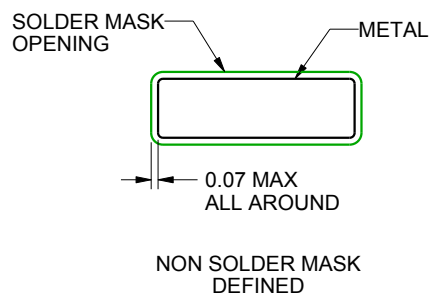
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

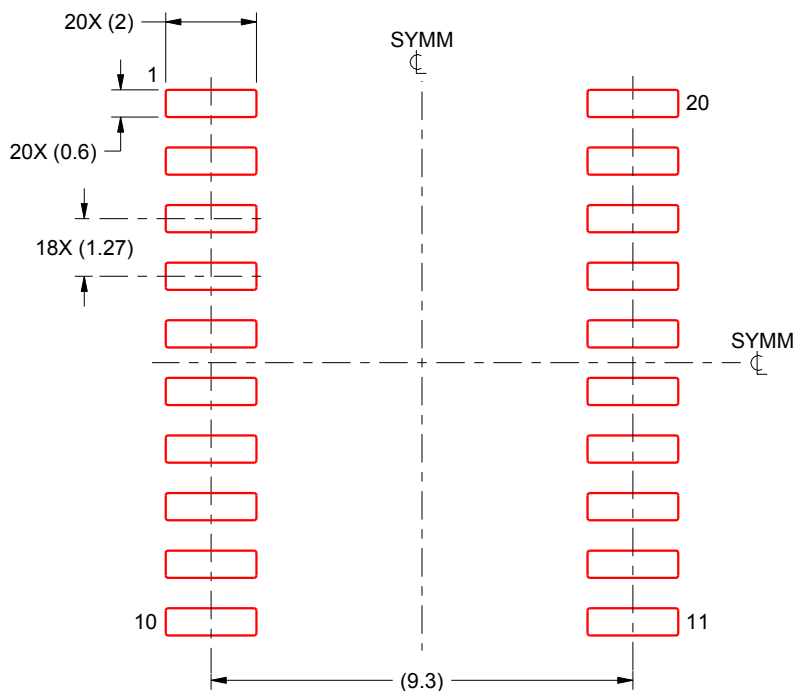
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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