

- Low  $r_{DS(on)}$  . . . 5  $\Omega$  Typical
- Avalanche Energy . . . 30 mJ
- Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current
- 500-mA Typical Current-Limiting Capability
- Output Clamp Voltage . . . 50 V
- Four Distinct Function Modes
- Low Power Consumption

**description**

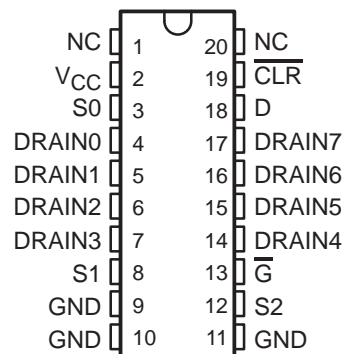
This power logic 8-bit addressable latch controls open-drain DMOS-transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multi-functional device capable of storing single-line data in eight addressable latches and 3-to-8 decoder or demultiplexer with active-low DMOS outputs.

Four distinct modes of operation are selectable by controlling the clear ( $\overline{CLR}$ ) and enable ( $\overline{G}$ ) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable  $\overline{G}$  should be held high (inactive) while the address lines are changing. In the 3-to-8 decoding or demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are off. In the clear mode, all outputs are off and unaffected by the address and data inputs. When data is low for a given output, the DMOS-transistor output is off. When data is high, the DMOS-transistor output has sink-current capability.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at  $T_C = 25^\circ\text{C}$ . The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B259 is characterized for operation over the operating case temperature range of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

DW OR N PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS			OUTPUT OF ADDRESSED DRAIN	EACH OTHER DRAIN	FUNCTION
$\overline{CLR}$	$\overline{G}$	D			
H	L	H	L	$Q_{i0}$	Addressable Latch
H	L	L	H	$Q_{i0}$	
H	H	X	$Q_{i0}$	$Q_{i0}$	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	
L	H	X	H	H	Clear

LATCH SELECTION TABLE

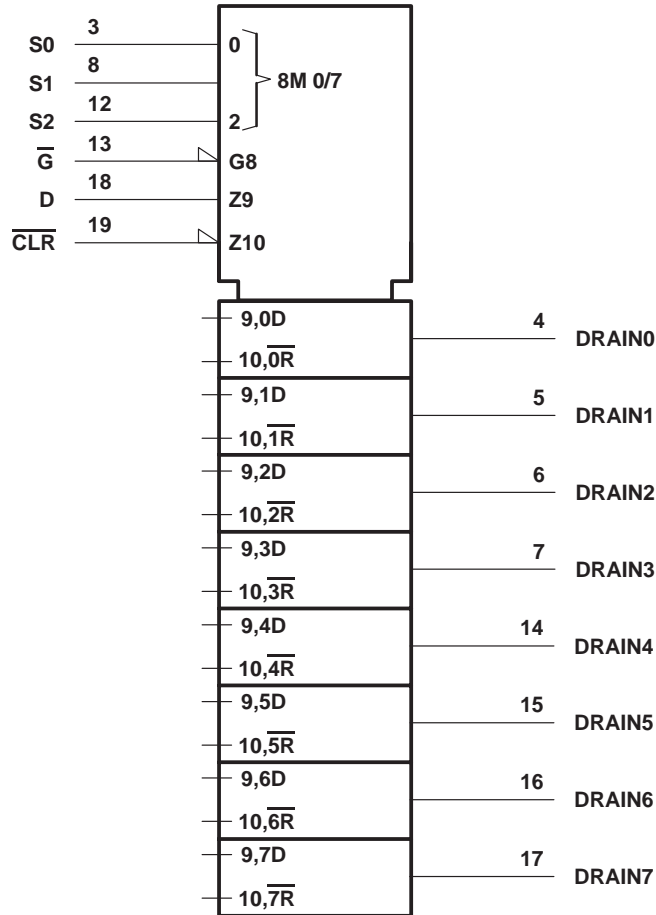
SELECT INPUTS			DRAIN ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = high level, L = low level

# TPIC6B259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

SLIS030 – APRIL 1994 – REVISED JULY 1995

## logic symbol†

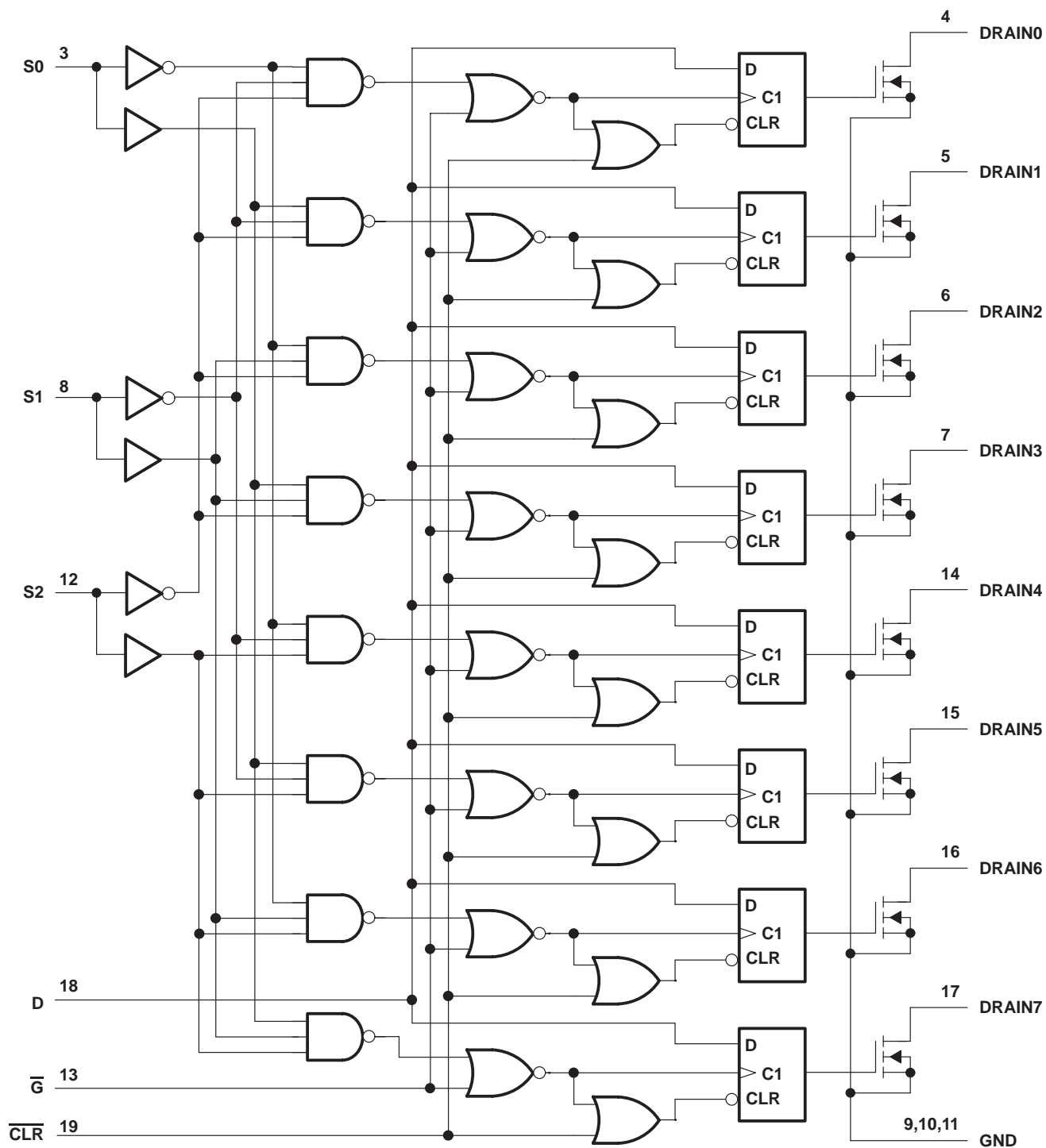


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# TPIC6B259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

SLIS030 – APRIL 1994 – REVISED JULY 1995

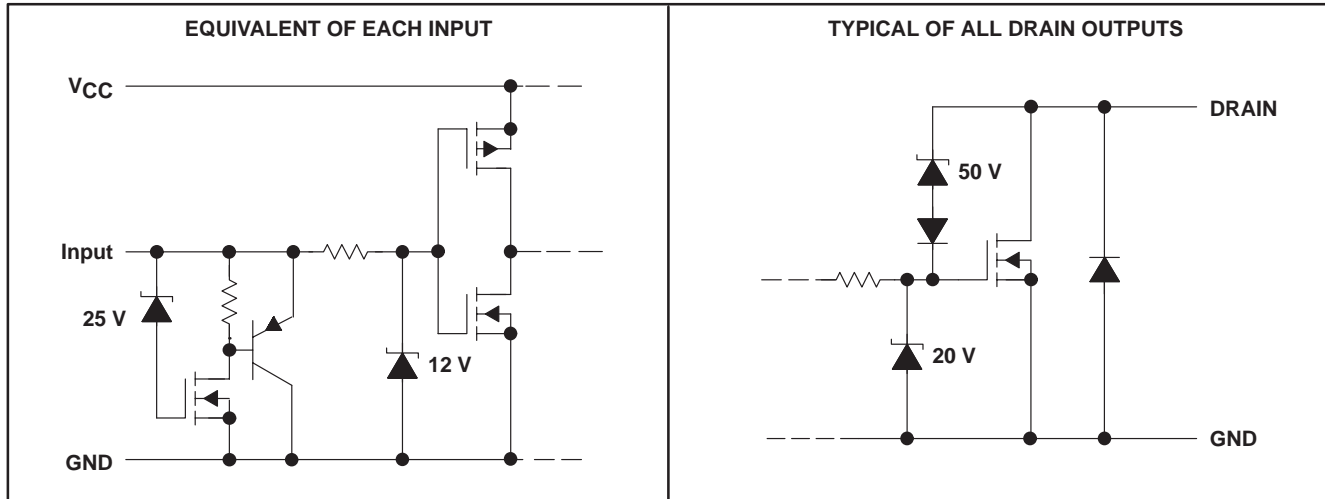
logic diagram (positive logic)



# TPIC6B259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

SLIS030 – APRIL 1994 – REVISED JULY 1995

## schematic of inputs and outputs



## absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)<sup>†</sup>

Logic supply voltage, $V_{CC}$ (see Note 1)	7 V
Logic input voltage range, $V_I$	-0.3 V to 7 V
Power DMOS drain-to-source voltage, $V_{DS}$ (see Note 2)	50 V
Continuous source-to-drain diode anode current	500 mA
Pulsed source-to-drain diode anode current (see Note 3)	1 A
Pulsed drain current, each output, all outputs on, $I_D$ , $T_C = 25^\circ\text{C}$ (see Note 3)	500 mA
Continuous drain current, each output, all outputs on, $I_D$ , $T_C = 25^\circ\text{C}$	150 mA
Peak drain current single output, $I_{DM}$ , $T_C = 25^\circ\text{C}$ (see Note 3)	500 mA
Single-pulse avalanche energy, $E_{AS}$ (see Figure 4)	30 mJ
Avalanche current, $I_{AS}$ (see Note 4)	500 mA
Continuous total dissipation	See Dissipating Rating Table
Operating virtual junction temperature range, $T_J$	-40°C to 150°C
Operating case temperature range, $T_C$	-40°C to 125°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.  
 2. Each power DMOS source is internally connected to GND.  
 3. Pulse duration  $\leq 100 \mu\text{s}$  and duty cycle  $\leq 2\%$ .  
 4. DRAIN supply voltage = 15 V, starting junction temperature ( $T_{JS}$ ) = 25°C,  $L = 200 \text{ mH}$ ,  $I_{AS} = 0.5 \text{ A}$  (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 125^\circ\text{C}$ POWER RATING
DW	1389 mW	11.1 mW/°C	278 mW
N	1050 mW	10.5 mW/°C	263 mW

**recommended operating conditions**

	MIN	MAX	UNIT
Logic supply voltage, $V_{CC}$	4.5	5.5	V
High-level input voltage, $V_{IH}$	0.85 $V_{CC}$		V
Low-level input voltage, $V_{IL}$	0.15 $V_{CC}$		V
Pulsed drain output current, $T_C = 25^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ (see Notes 3 and 5)	-500	500	mA
Setup time, D high before $\overline{G}\uparrow$ , $t_{SU}$ (see Figure 2)	20		ns
Hold time, D high after $\overline{G}\uparrow$ , $t_H$ (see Figure 2)	20		ns
Pulse duration, $t_W$ (see Figure 2)	40		ns
Operating case temperature, $T_C$	-40	125	$^\circ\text{C}$

**electrical characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$ Drain-to-source breakdown voltage	$I_D = 1\text{ mA}$	50			V
$V_{SD}$ Source-to-drain diode forward voltage	$I_F = 100\text{ mA}$		0.85	1	V
$I_{IH}$ High-level input current	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}$			1	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = 5.5\text{ V}$ , $V_I = 0$			-1	$\mu\text{A}$
$I_{CC}$ Logic supply current	$V_{CC} = 5.5\text{ V}$	All outputs off	20	100	$\mu\text{A}$
		All outputs on	150	300	
$I_N$ Nominal current	$V_{DS(on)} = 0.5\text{ V}$ , $I_N = I_D$ , $T_C = 85^\circ\text{C}$ , See Notes 5, 6, and 7		90		mA
$I_{DSX}$ Off-state drain current	$V_{DS} = 40\text{ V}$ , $V_{CC} = 5.5\text{ V}$		0.1	5	$\mu\text{A}$
	$V_{DS} = 40\text{ V}$ , $V_{CC} = 5.5\text{ V}$ , $T_C = 125^\circ\text{C}$		0.15	8	
$r_{DS(on)}$ Static drain-to-source on-state resistance	$I_D = 100\text{ mA}$ , $V_{CC} = 4.5\text{ V}$	See Notes 5 and 6 and Figures 6 and 7	4.2	5.7	$\Omega$
	$I_D = 100\text{ mA}$ , $V_{CC} = 4.5\text{ V}$ , $T_C = 125^\circ\text{C}$		6.8	9.5	
	$I_D = 350\text{ mA}$ , $V_{CC} = 4.5\text{ V}$		5.5	8	

**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output from D	$C_L = 30\text{ pF}$ , $I_D = 100\text{ mA}$ , See Figures 1, 2, and 8		150		ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from D			90		ns
$t_r$ Rise time, drain output			200		ns
$t_f$ Fall time, drain output			200		ns
$t_a$ Reverse-recovery-current rise time	$I_F = 100\text{ mA}$ , $di/dt = 20\text{ A}/\mu\text{s}$ , See Notes 5 and 6 and Figure 3		100		ns
$t_{rr}$ Reverse-recovery time			300		

- NOTES: 3. Pulse duration  $\leq 100\ \mu\text{s}$  and duty cycle  $\leq 2\%$ .  
 5. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.  
 7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at  $T_C = 85^\circ\text{C}$ .

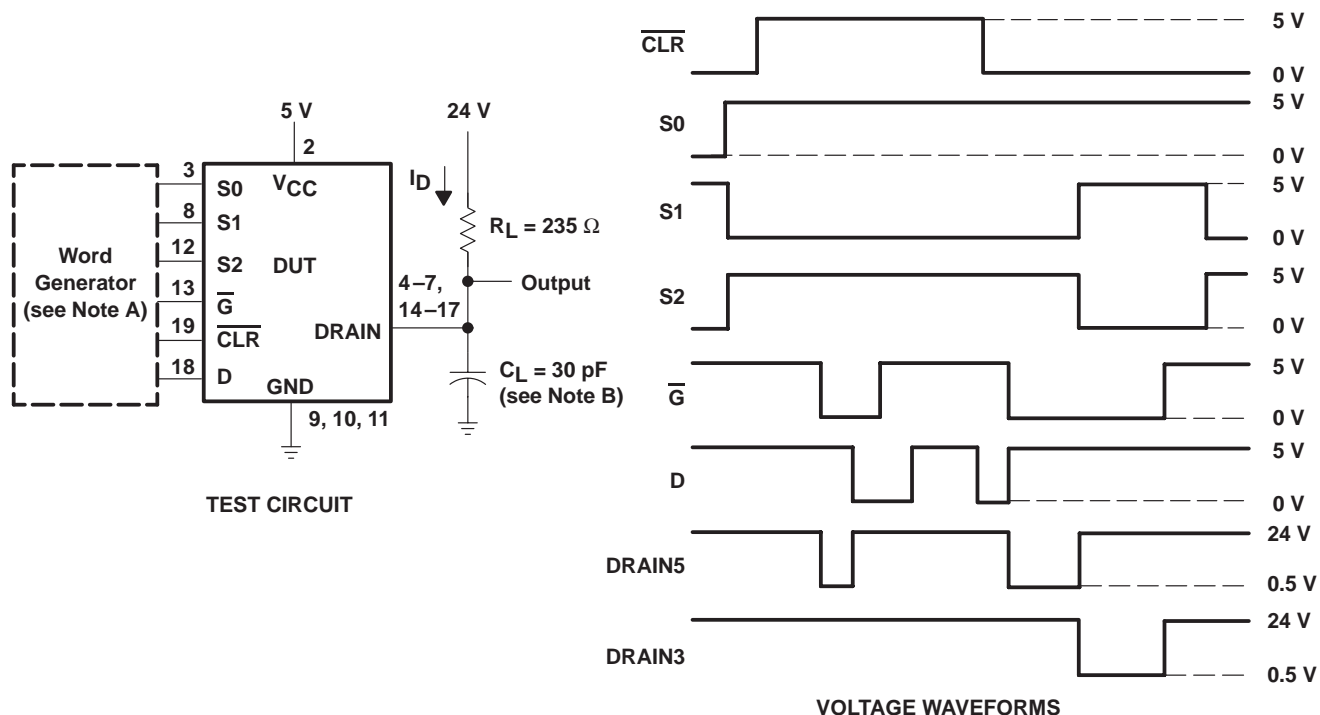
# TPIC6B259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

SLIS030 – APRIL 1994 – REVISED JULY 1995

## thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
R <sub>θJA</sub>	Thermal resistance junction-to-ambient	All 8 outputs with equal power		90	°C/W
				95	

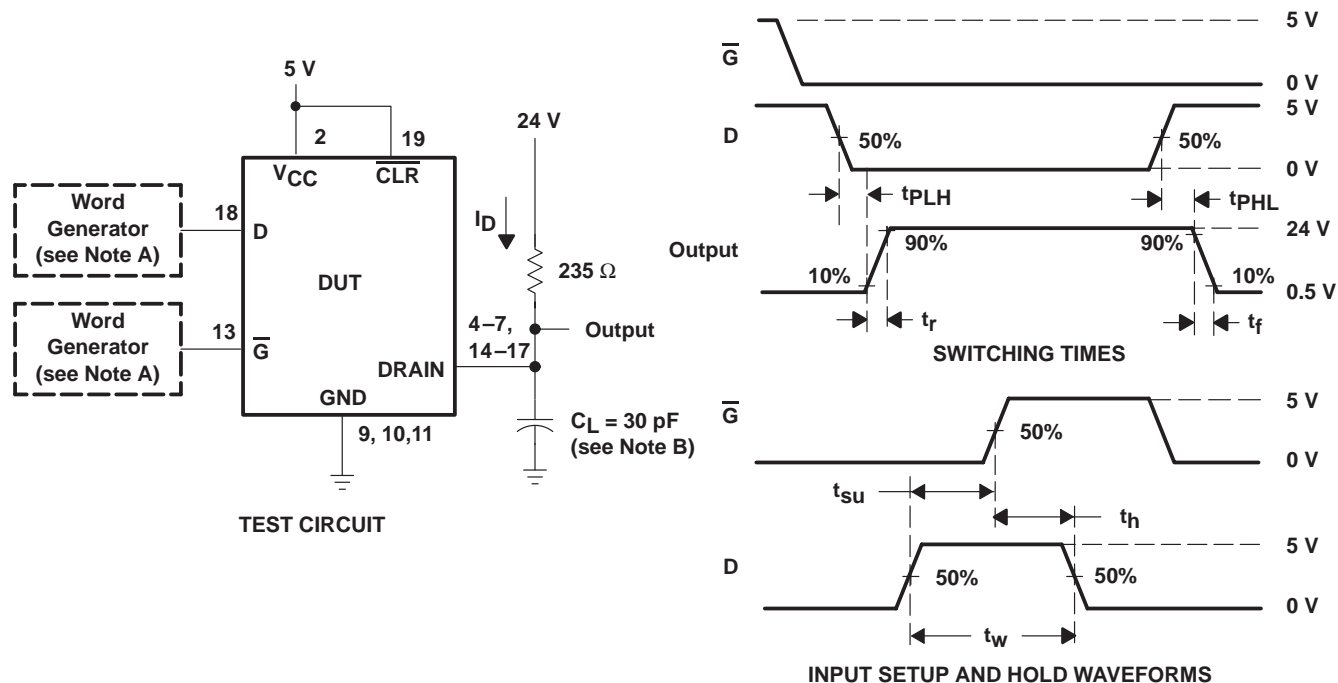
## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $t_w = 300$  ns, pulsed repetition rate (PRR) = 5 kHz,  $Z_O = 50$  Ω.  
B.  $C_L$  includes probe and jig capacitance.

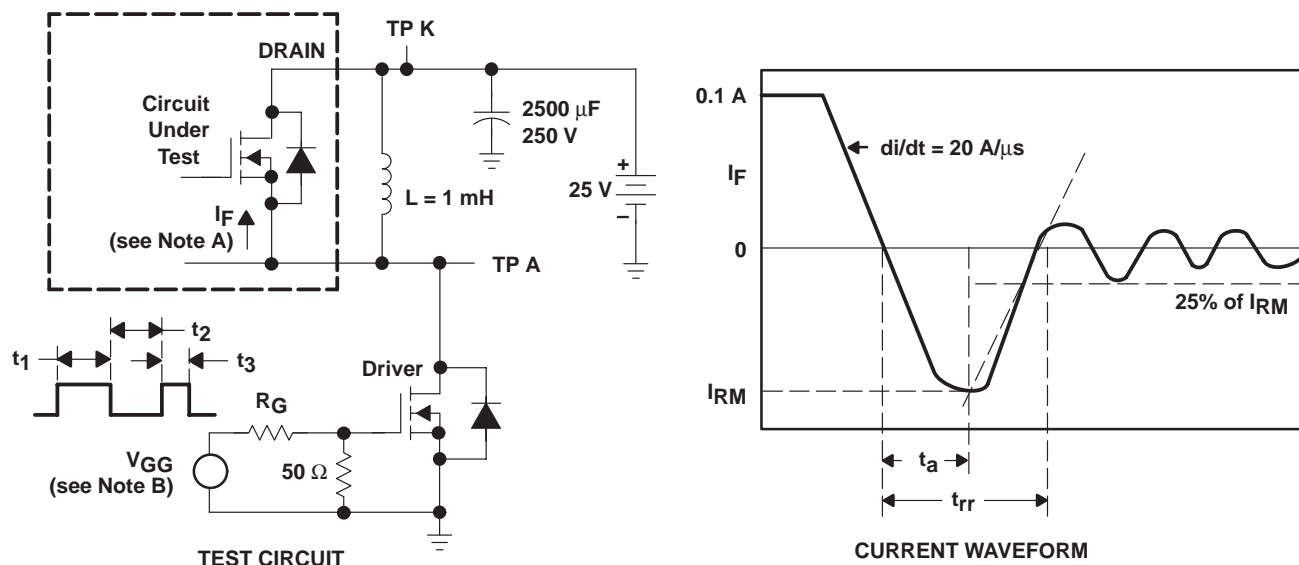
Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $t_w = 300$  ns, pulsed repetition rate (PRR) = 5 kHz,  $Z_0 = 50$   $\Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms



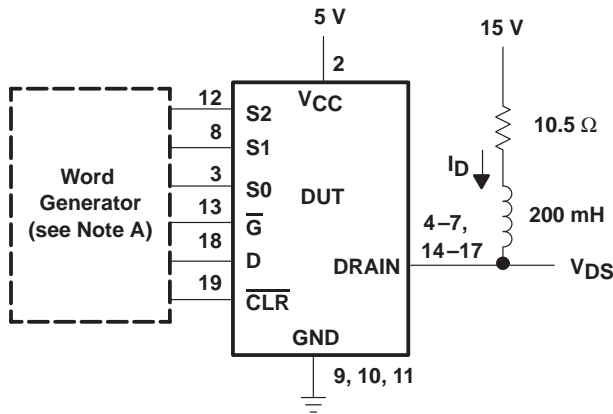
- NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.  
B. The  $V_{GG}$  amplitude and  $R_G$  are adjusted for  $di/dt = 20$  A/ $\mu$ s. A  $V_{GG}$  double-pulse train is used to set  $I_F = 0.1$  A, where  $t_1 = 10$   $\mu$ s,  $t_2 = 7$   $\mu$ s, and  $t_3 = 3$   $\mu$ s.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode

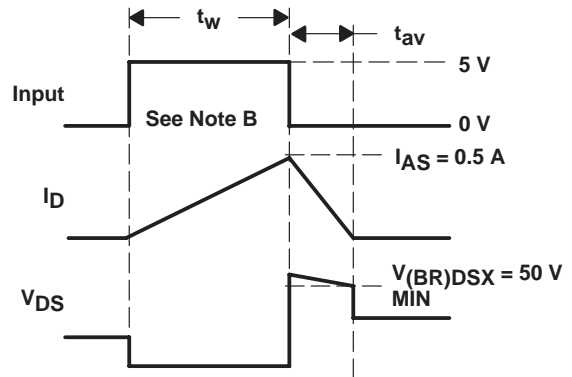
# TPIC6B259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

SLIS030 – APRIL 1994 – REVISED JULY 1995

## PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .  
 B. Input pulse duration,  $t_w$ , is increased until peak current  $I_{AS} = 0.5$  A.  
 Energy test level is defined as  $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30$  mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

## TYPICAL CHARACTERISTICS

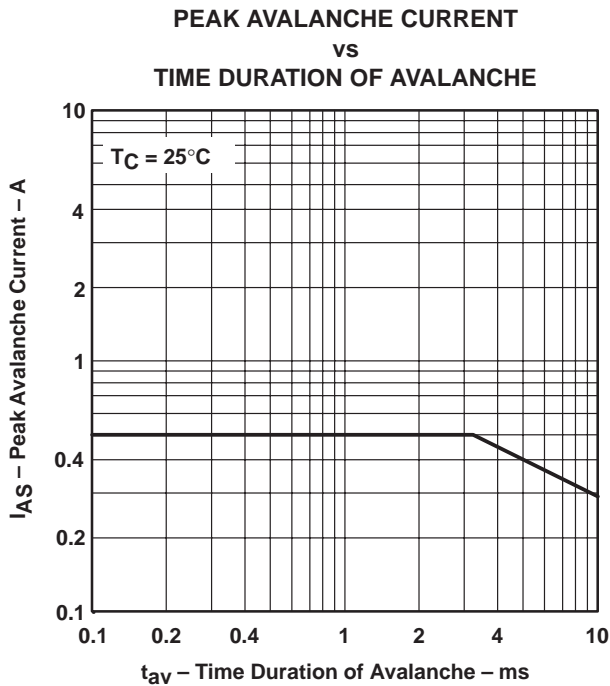
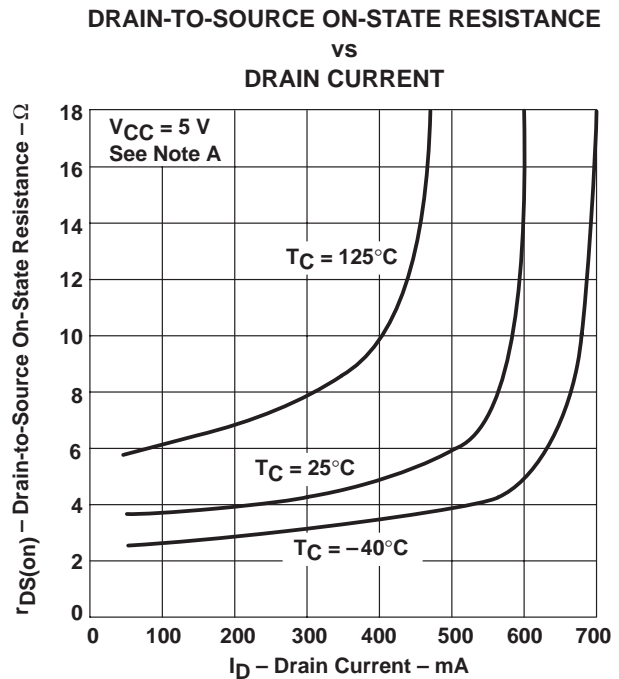


Figure 5



NOTE C: Technique should limit  $T_J - T_C$  to 10°C maximum.

Figure 6



TYPICAL CHARACTERISTICS

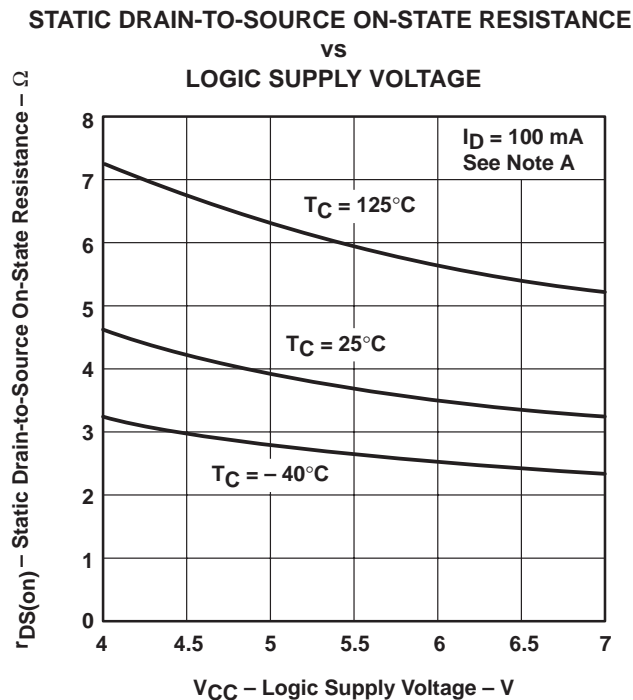


Figure 7

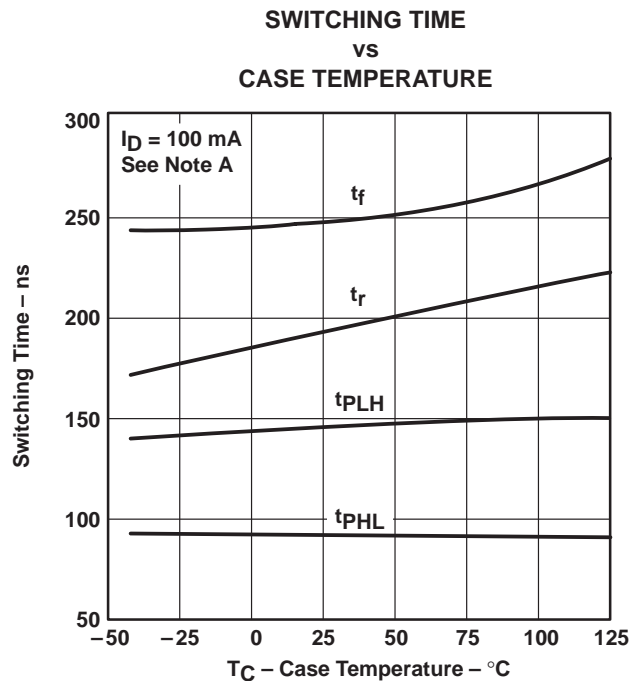


Figure 8

NOTE D: Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

# TPIC6B259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

SLIS030 – APRIL 1994 – REVISED JULY 1995

## THERMAL INFORMATION

MAXIMUM CONTINUOUS  
DRAIN CURRENT OF EACH OUTPUT  
vs  
NUMBER OF OUTPUTS CONDUCTING  
SIMULTANEOUSLY

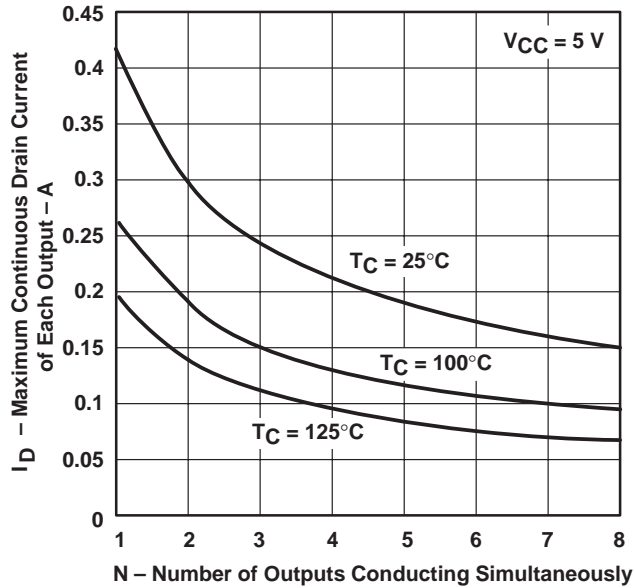


Figure 9

MAXIMUM PEAK DRAIN CURRENT  
OF EACH OUTPUT  
vs  
NUMBER OF OUTPUTS CONDUCTING  
SIMULTANEOUSLY

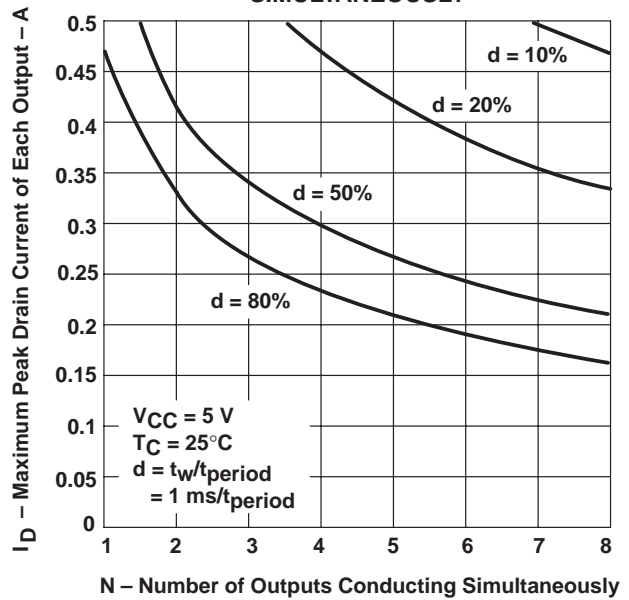


Figure 10

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC6B259DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6B259	<a href="#">Samples</a>
TPIC6B259DWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TPIC6B259	<a href="#">Samples</a>
TPIC6B259DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6B259	<a href="#">Samples</a>
TPIC6B259DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TPIC6B259	<a href="#">Samples</a>
TPIC6B259N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 125	TPIC6B259N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6B259DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TPIC6B259DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6B259DWR	SOIC	DW	20	2000	350.0	350.0	43.0
TPIC6B259DWRG4	SOIC	DW	20	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPIC6B259DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TPIC6B259DWG4	DW	SOIC	20	25	506.98	12.7	4826	6.6
TPIC6B259N	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated