

TPLD1202 Programmable Logic Device With I²C/SPI and 10-GPIO

1 Features

- Operating characteristics
 - Extended temperature range: -40°C to 125°C
 - Wide supply voltage range: 1.71V to 5.5V
- Configurable macro-cells
 - 2-, 3-, and 4-bit lookup tables
 - D-type flip-flops and latches with and without reset/set option
 - 8-bit shift register
 - 16-bit pattern generator
 - Counters and delay generators
 - PWM generators
 - Programmable deglitch filter or edge detector
 - Multi-channel sampling analog comparator
 - Voltage reference and Analog temperature sensor
 - Oscillators
- Flexible digital I/O features
 - All digital signals can be routed to any GPIO
 - Digital input modes: digital in with and without Schmitt-trigger, low-voltage digital in
 - Digital output modes: push-pull, open-drain NMOS, tri-state
- Development tools
 - TPLD1202 evaluation module
 - TPLD programmer
 - InterConnect Studio
- In-line programming capable

2 Applications

- [Factory automation and control](#)
- [Communications equipment](#)
- [Retail automation and payment](#)
- [Test and measurement](#)
- [Pro audio, video, and signage](#)
- [Personal electronics](#)

3 Description

The TPLD1202 is part of the TI programmable logic device (TPLD) family of devices that feature versatile programmable logic ICs with combinational logic, sequential logic, and analog blocks. TPLD provides a fully integrated, low power solution to implement common system functions, such as timing delays, voltage monitors, system resets, power sequencers, I/O expanders, and more. This device features configurable I/O structures that extends compatibility within mixed-signal environments, reducing the number of discrete components required.

System designers can create circuits and configure the macro-cells, I/O pins, and interconnections by temporarily emulating the non-volatile memory or by permanently programming the one-time programmable (OTP) through InterConnect Studio. The TPLD1202 is supported by a hardware and software ecosystem with application notes, reference designs, and design examples. Visit [ti.com](https://www.ti.com) for more information and access to design tools.

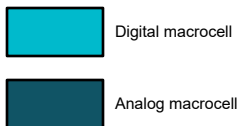
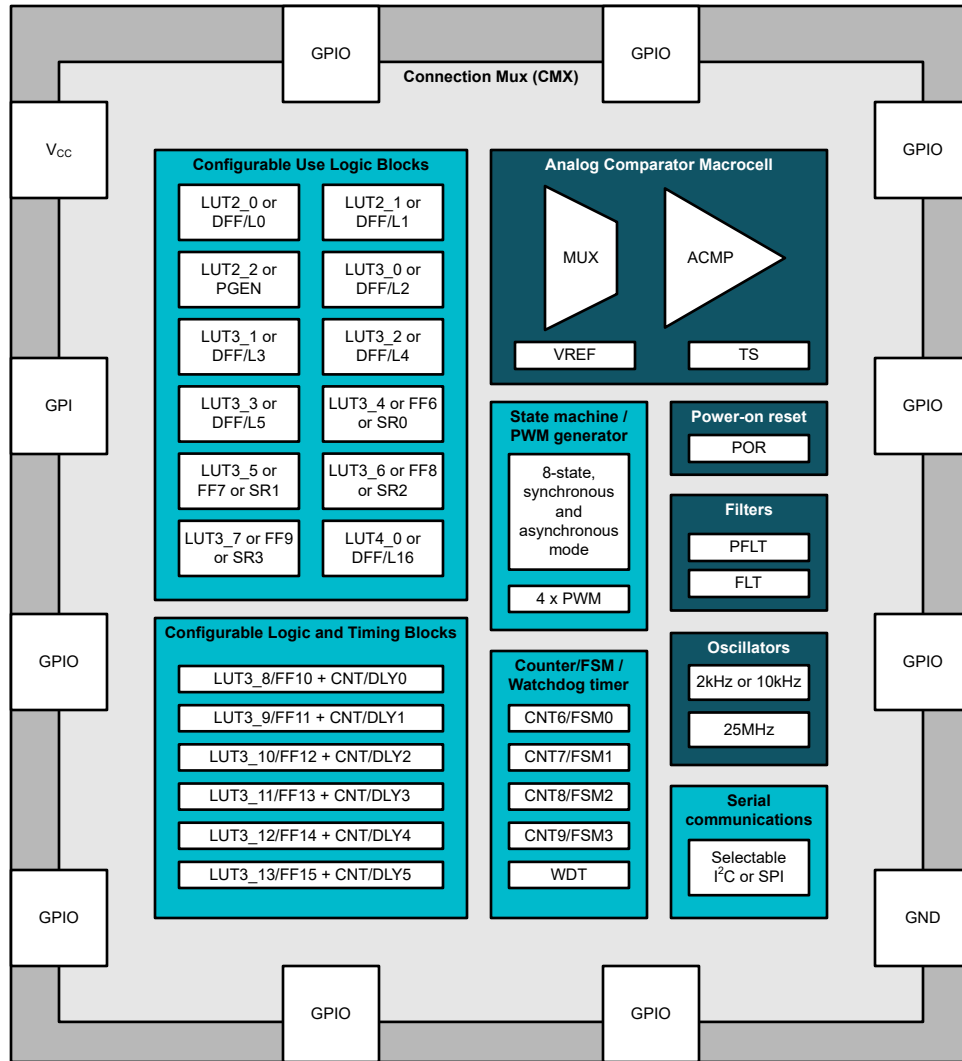
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TPLD1202	DYY (SOT-23-THN, 14)	2.00mm × 4.20mm
	RWS (X2QFN, 12)	1.60mm × 1.60mm
	RWB (X2QFN, 12)	1.60mm × 1.60mm

- (1) For all available packages, see [Section 6](#).
 (2) The package size (length × width) is a nominal value and includes pins, where applicable.



ADVANCE INFORMATION



TPLD1202 Block Diagram

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4 Device and Documentation Support

4.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

4.3 Trademarks

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4.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2024) to Revision A (April 2026)	Page
• Added RWS Package option.	1

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

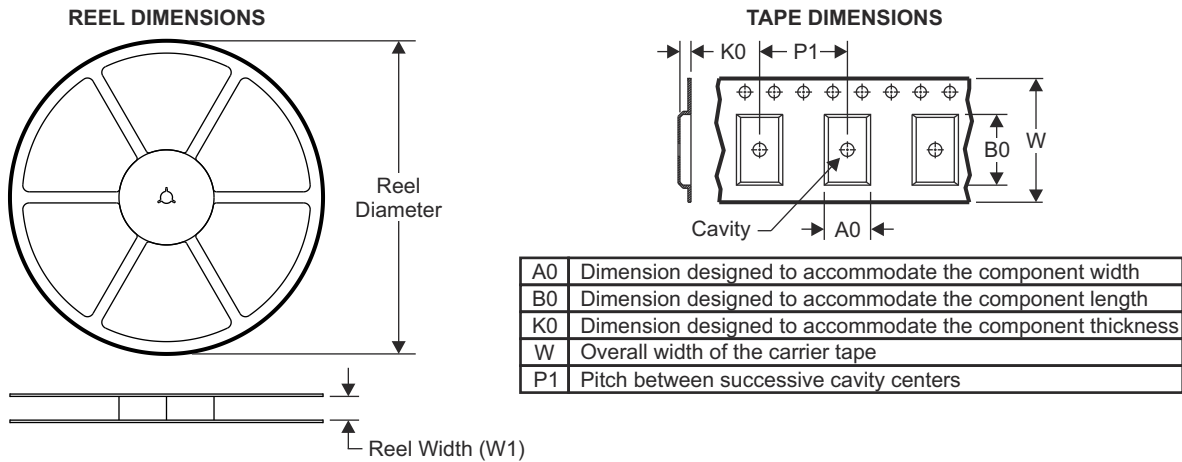
6.1 Packaging Option Addendum

Packaging Information

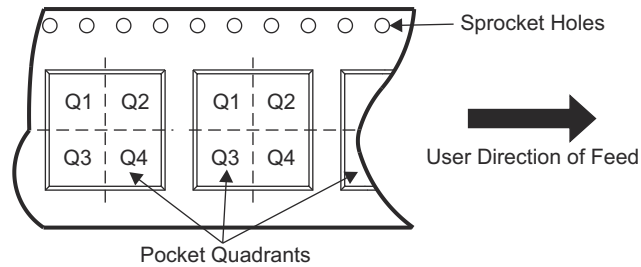
Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁴⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^{(5) (6)}
TPLD1202RWBR	PREVIEW	X2QFN	RWB	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TO
TPLD1202RWSR	PREVIEW	X2QFN	RWS	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TP
TPLD1202DYYR	PREVIEW	SOT-23-THN	DYY	14	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	TPLD1202

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
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6.2 Tape and Reel Information



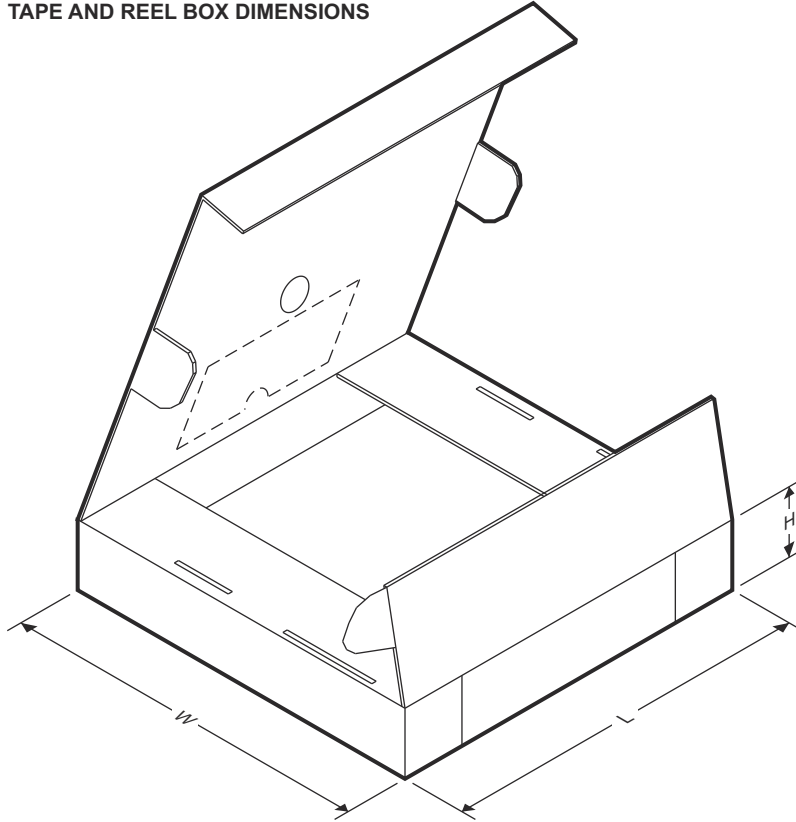
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPLD1202RWBR	X2QFN	RWB	12	3000	180	8.4	1.8	1.8	0.48	4	8	2
TPLD1202RWSR	X2QFN	RWS	12	3000	180	8.4	1.8	1.8	0.48	4	8	1
TPLD1202DYR	SOT-23-THN	DYY	12	3000	180	8.4	4.5	3.56	1.35	8	12	3

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



ADVANCE INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPLD1202RWBR	X2QFN	RWB	12	3000	210	185	35
PTPLD1202RWSR	X2QFN	RWS	12	3000	210	185	35
PTPLD1202DYYR	SOT-23-THN	DYY	12	3000	210	185	35

6.3 Mechanical Data

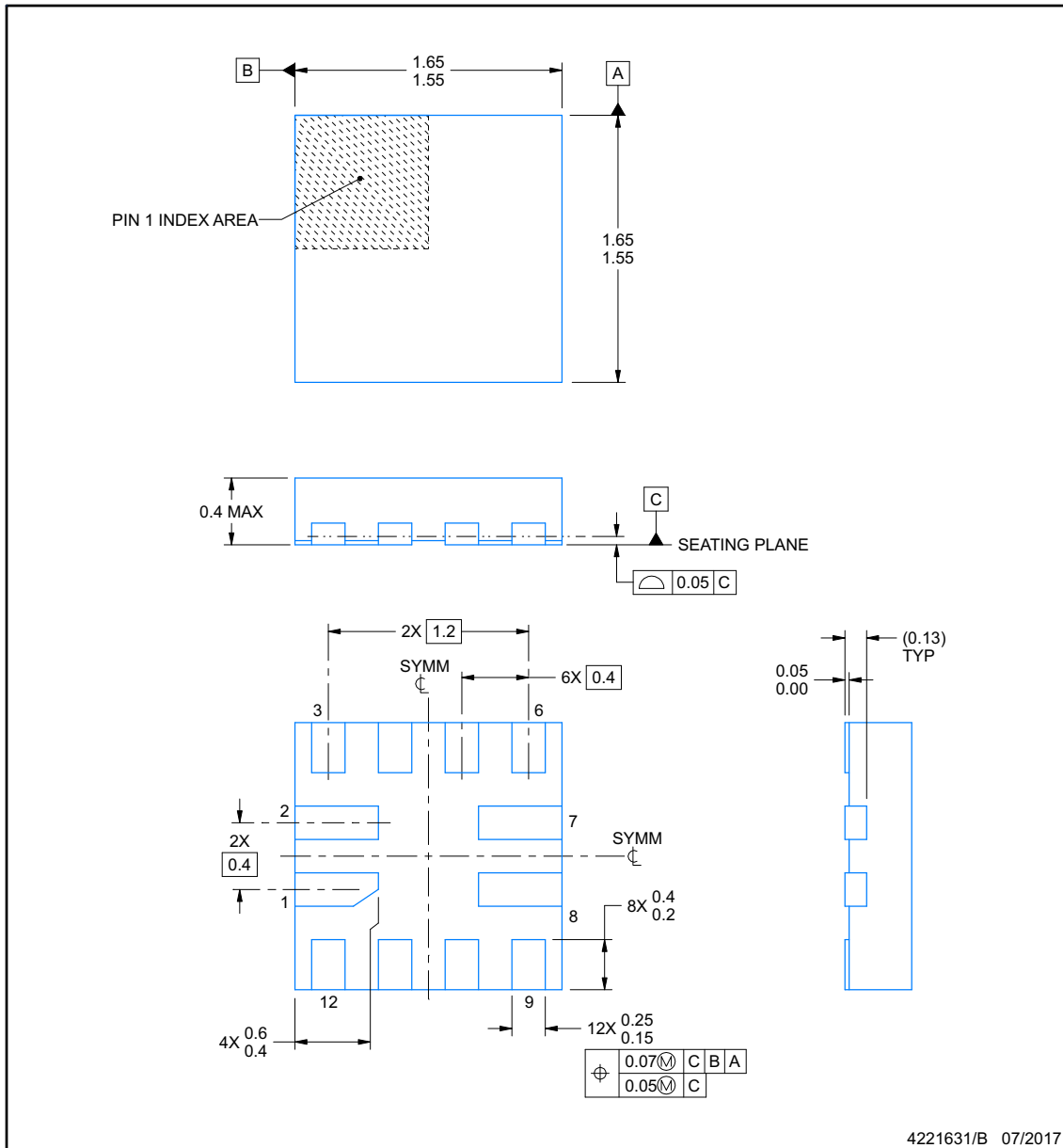


PACKAGE OUTLINE

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

ADVANCE INFORMATION

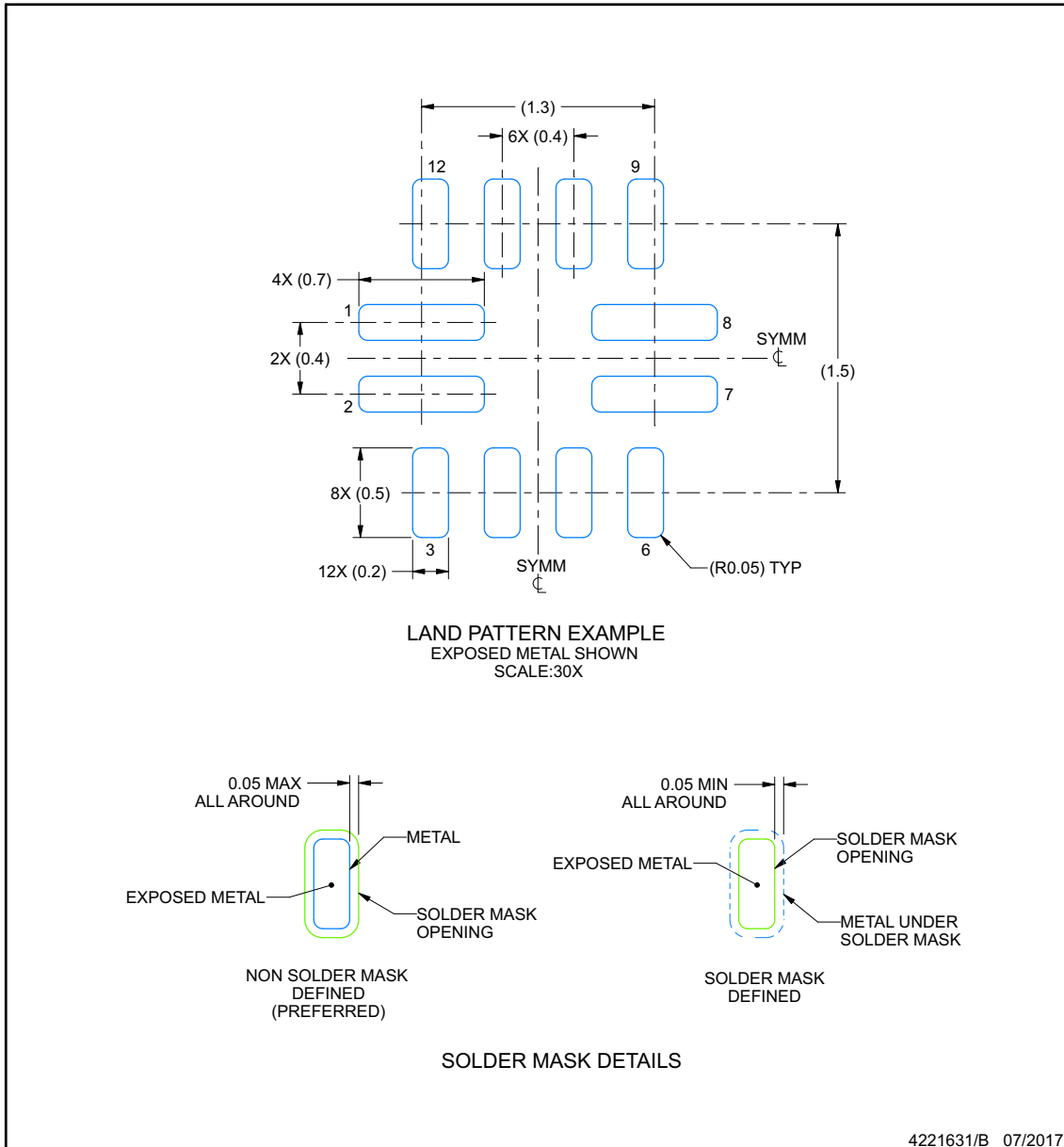
EXAMPLE BOARD LAYOUT

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

ADVANCE INFORMATION



NOTES: (continued)

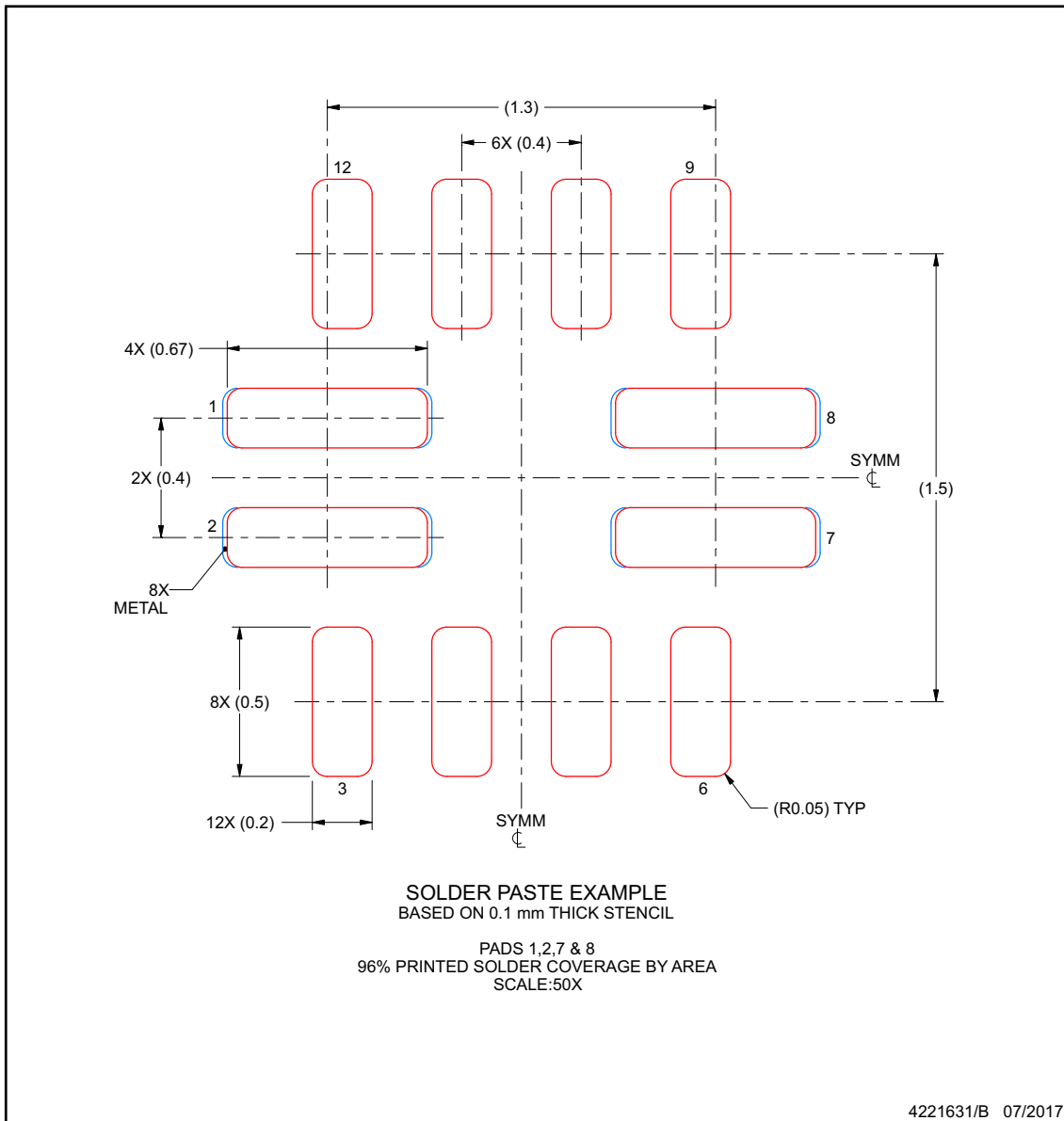
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RWB0012A

X2QFN - 0.4 mm max height

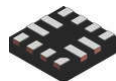
PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

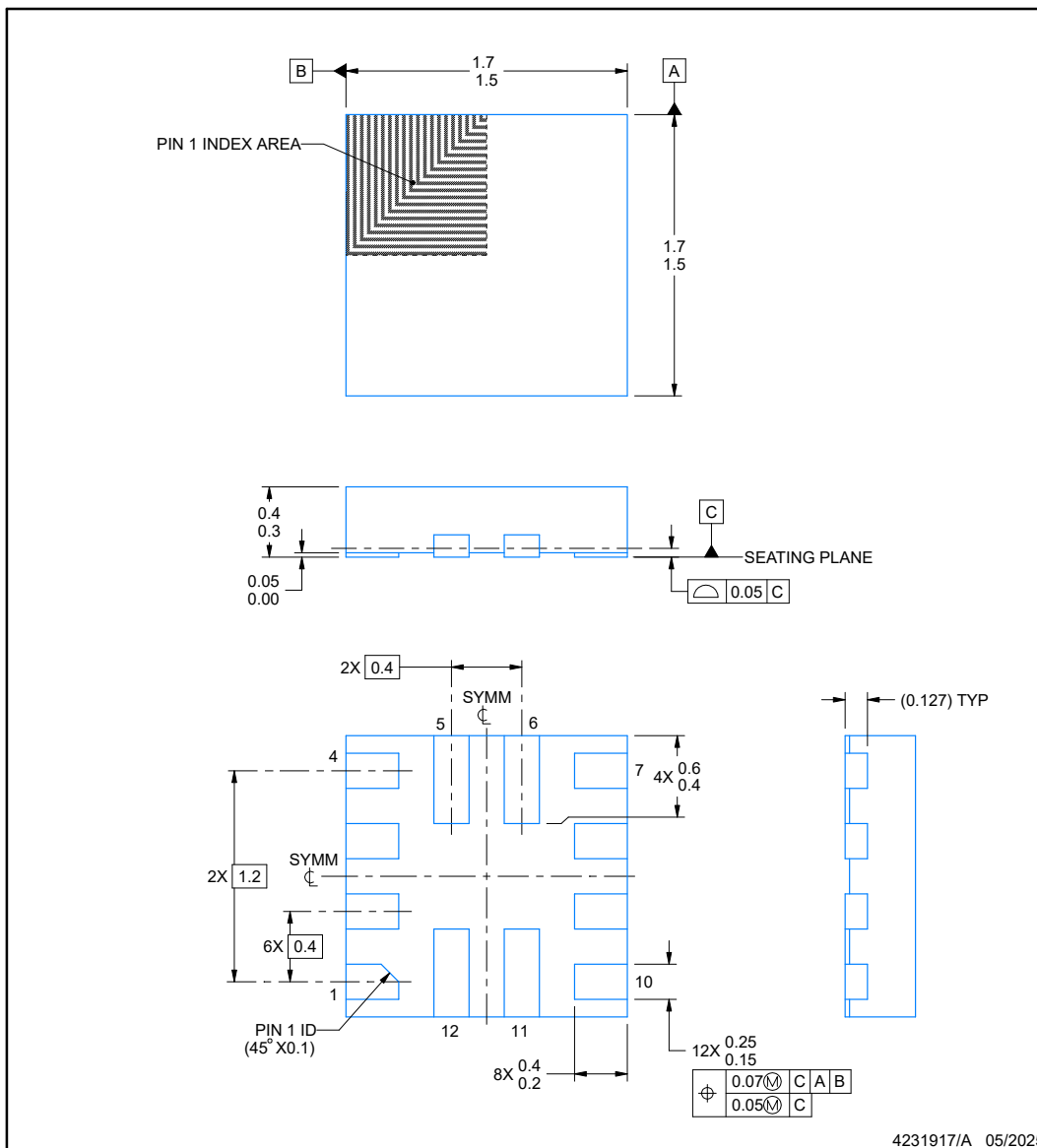


RWS0012A

PACKAGE OUTLINE

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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NOTES:

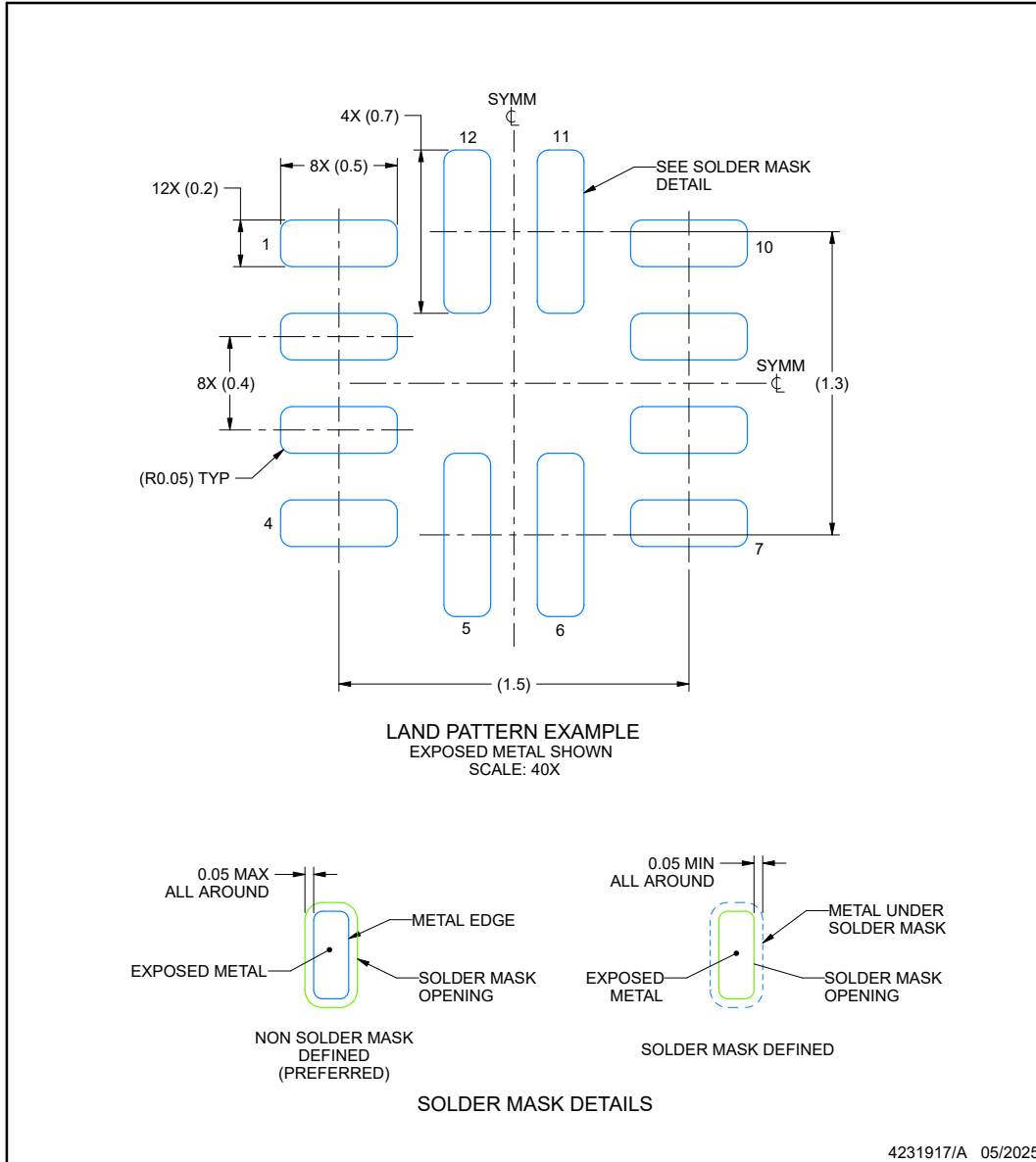
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

RWS0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

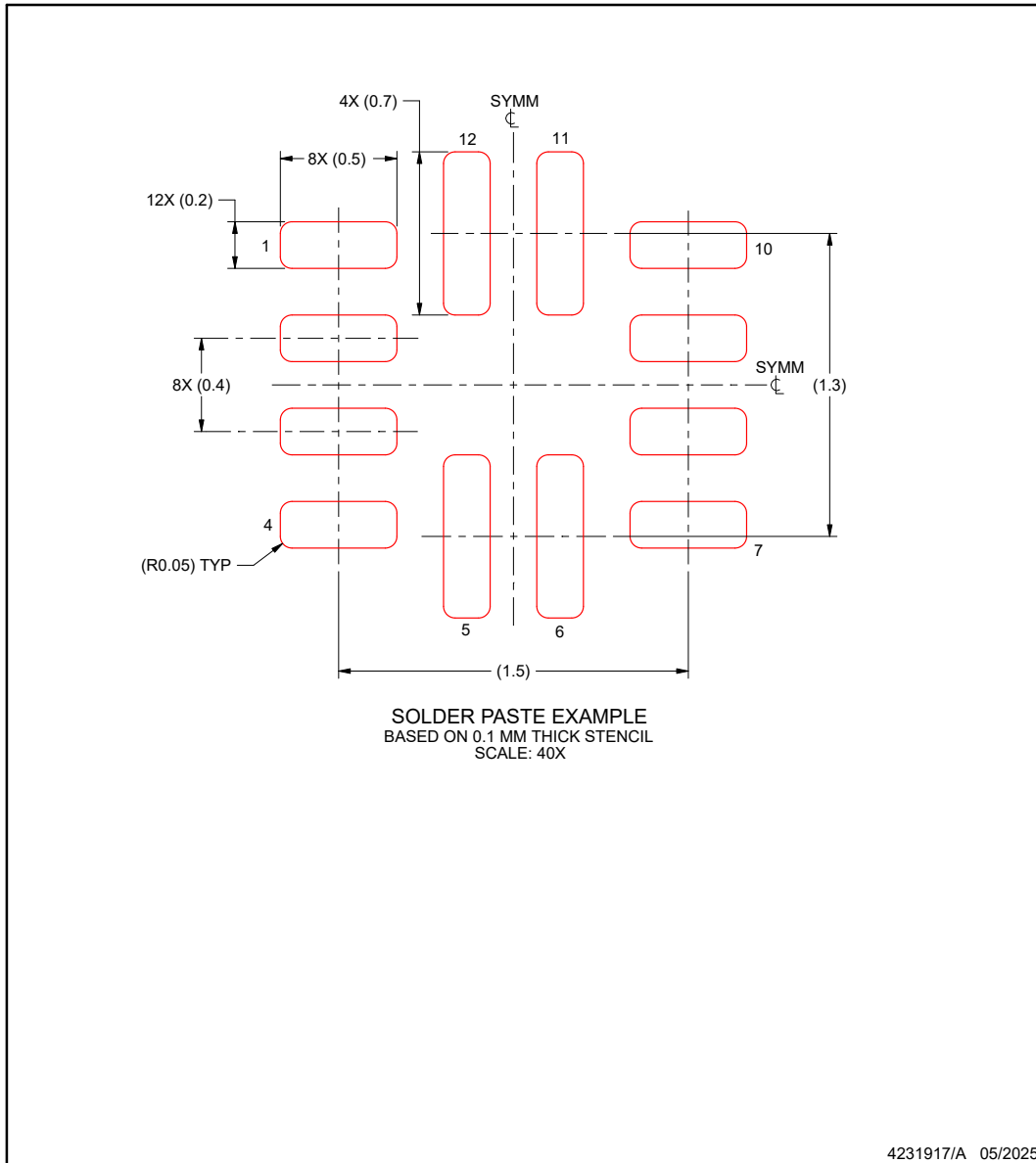
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RWS0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



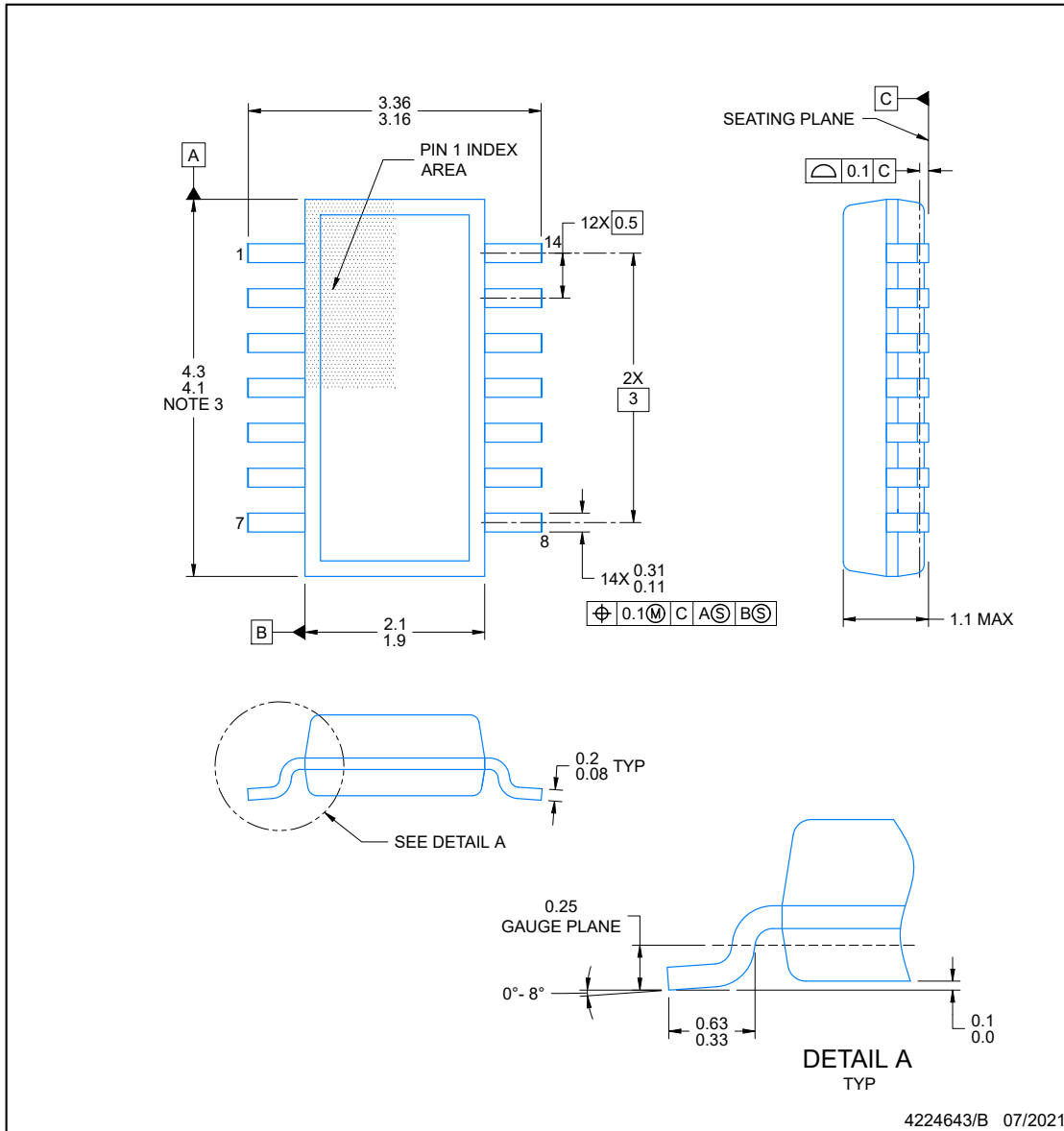
NOTES: (continued)

- 4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DYY0014A

PACKAGE OUTLINE
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

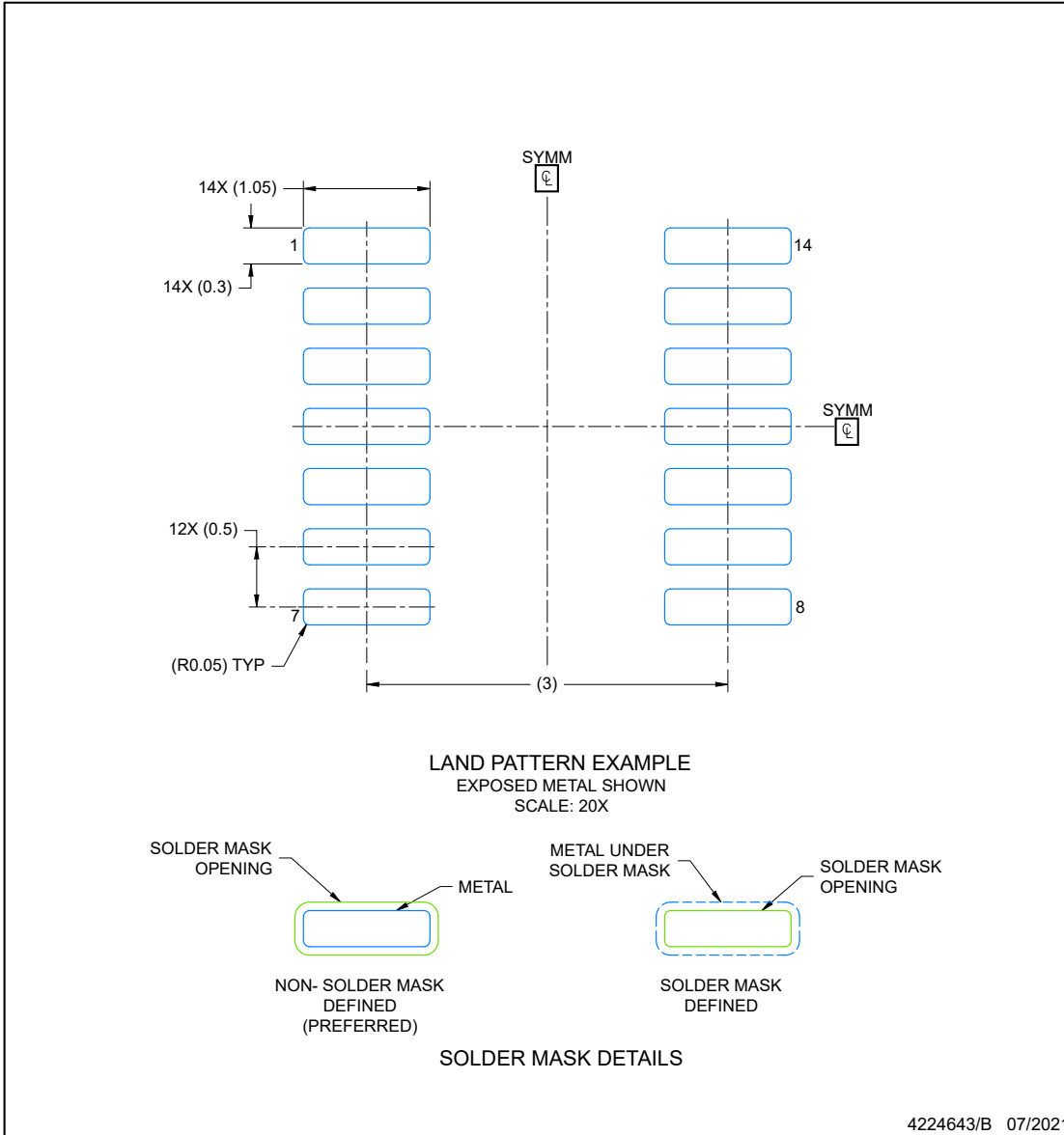
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB

EXAMPLE BOARD LAYOUT
SOT-23-THIN - 1.1 mm max height

DYY0014A

PLASTIC SMALL OUTLINE

ADVANCE INFORMATION



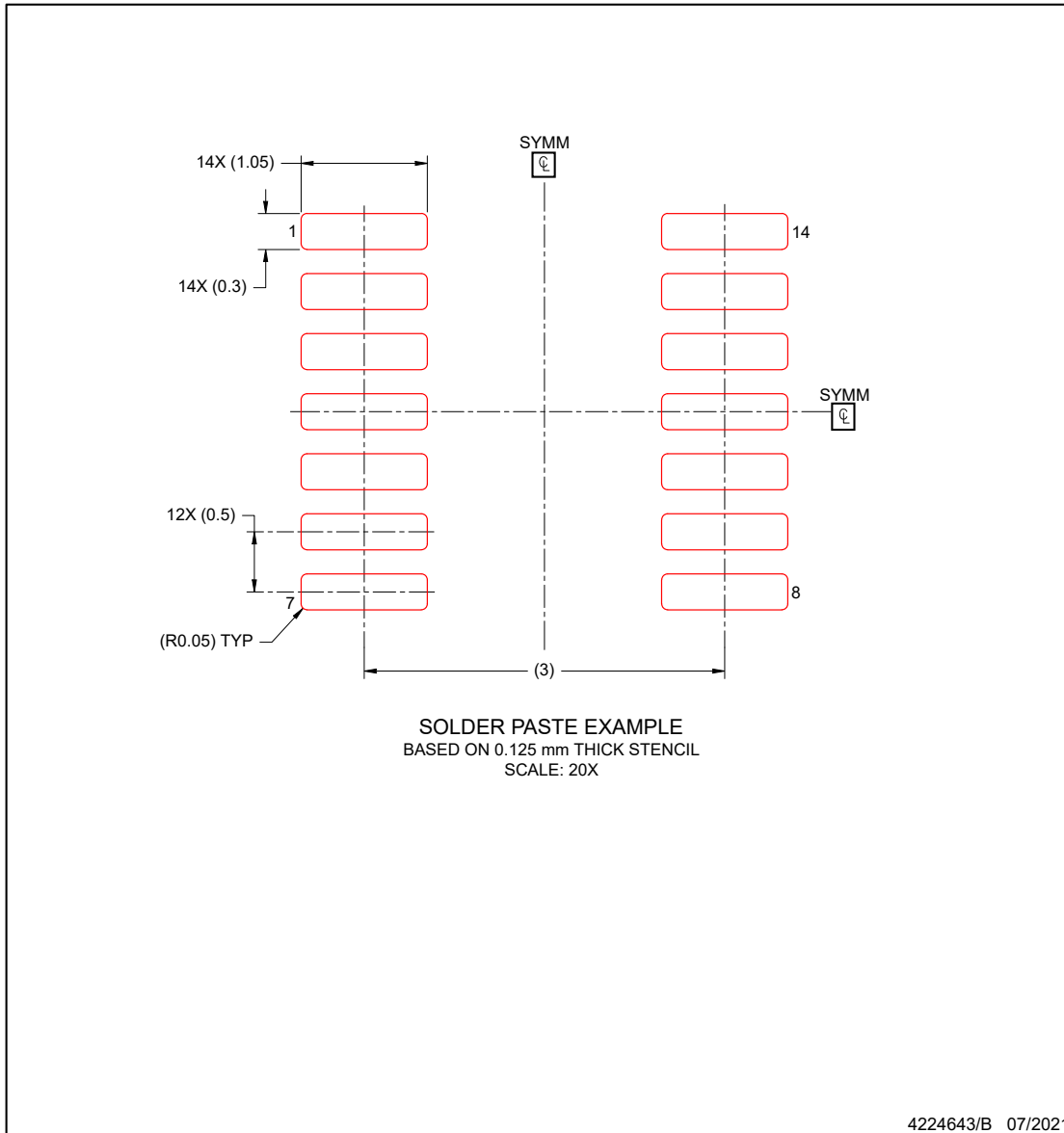
NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN
SOT-23-THIN - 1.1 mm max height

DYY0014A

PLASTIC SMALL OUTLINE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

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