

TPS1101, TPS1101Y SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS079C – DECEMBER 1993 – REVISED AUGUST 1995

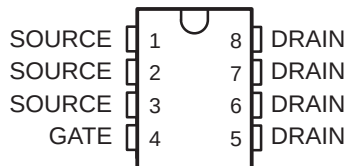
- Low $r_{DS(on)}$. . . 0.09 Ω Typ at $V_{GS} = -10$ V
- 3 V Compatible
- Requires No External V_{CC}
- TTL and CMOS Compatible Inputs
- $V_{GS(th)} = -1.5$ V Max
- Available in Ultrathin TSSOP Package (PW)
- ESD Protection Up to 2 kV per MIL-STD-883C, Method 3015

description

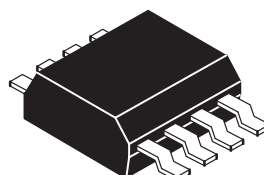
The TPS1101 is a single, low- $r_{DS(on)}$, P-channel, enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of the Texas Instruments LinBiCMOS™ process. With a maximum $V_{GS(th)}$ of -1.5 V and an I_{DSS} of only 0.5 μ A, the TPS1101 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low $r_{DS(on)}$ and excellent ac characteristics (rise time 5.5 ns typical) of the TPS1101 make it the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin thin shrink small-outline package or TSSOP (PW) version fits in height-restricted places where other P-channel MOSFETs cannot. The size advantage is especially important where board height restrictions do not allow for an small-outline integrated circuit (SOIC) package. Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other P-channel MOSFETs in SOIC packages.

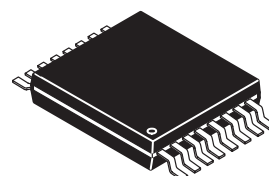
D PACKAGE
(TOP VIEW)



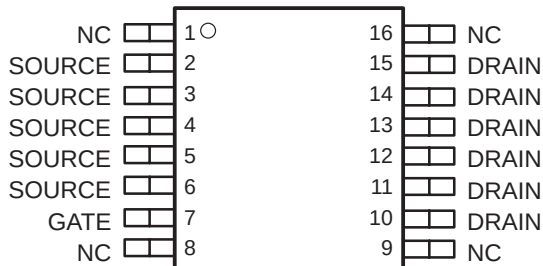
D PACKAGE



PW PACKAGE



PW PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES†		CHIP FORM (Y)
	SMALL OUTLINE (D)	TSSOP (PW)	
-40°C to 150°C	TPS1101D	TPS1101PWLE	TPS1101Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1101DR). The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1101PWLE). The chip form is tested at 25°C .



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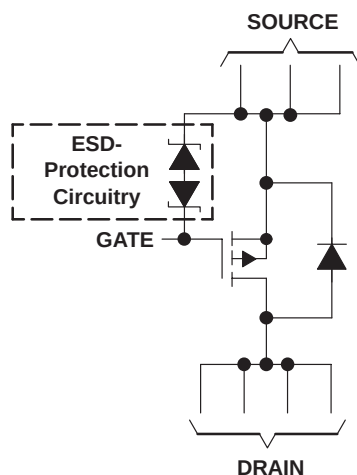
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SLVS079C – DECEMBER 1993 – REVISED AUGUST 1995

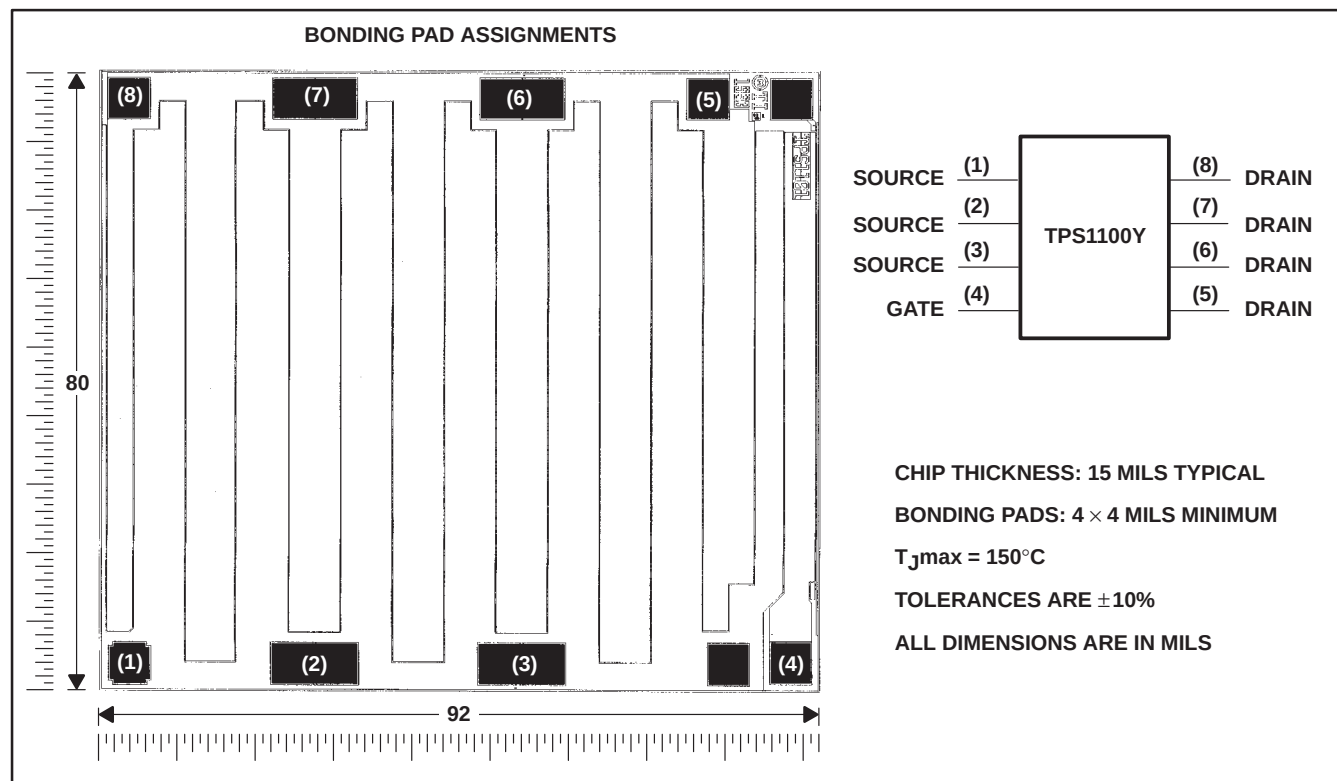
schematic



NOTE A: For all applications, all source terminals should be connected and all drain terminals should be connected.

TPS1101Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1101. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



TPS1101, TPS1101Y

SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS079C – DECEMBER 1993 – REVISED AUGUST 1995

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

					UNIT
Drain-to-source voltage, V_{DS}				– 15	V
Gate-to-source voltage, V_{GS}				2 or – 15	V
Continuous drain current ($T_J = 150^{\circ}\text{C}$), $I_D^{\ddagger}$	$V_{GS} = -2.7\text{ V}$	D package	$T_A = 25^{\circ}\text{C}$	± 0.62	A
			$T_A = 125^{\circ}\text{C}$	± 0.39	
		PW package	$T_A = 25^{\circ}\text{C}$	± 0.61	
			$T_A = 125^{\circ}\text{C}$	± 0.38	
	$V_{GS} = -3\text{ V}$	D package	$T_A = 25^{\circ}\text{C}$	± 0.88	
			$T_A = 125^{\circ}\text{C}$	± 0.47	
		PW package	$T_A = 25^{\circ}\text{C}$	± 0.86	
			$T_A = 125^{\circ}\text{C}$	± 0.45	
	$V_{GS} = -4.5\text{ V}$	D package	$T_A = 25^{\circ}\text{C}$	± 1.52	
			$T_A = 125^{\circ}\text{C}$	± 0.71	
		PW package	$T_A = 25^{\circ}\text{C}$	± 1.44	
			$T_A = 125^{\circ}\text{C}$	± 0.67	
	$V_{GS} = -10\text{ V}$	D package	$T_A = 25^{\circ}\text{C}$	± 2.30	
			$T_A = 125^{\circ}\text{C}$	± 1.04	
		PW package	$T_A = 25^{\circ}\text{C}$	± 2.18	
			$T_A = 125^{\circ}\text{C}$	± 0.98	
Pulsed drain current, $I_D^{\ddagger}$			$T_A = 25^{\circ}\text{C}$	± 10	A
Continuous source current (diode conduction), I_S			$T_A = 25^{\circ}\text{C}$	– 1.1	A
Storage temperature range, T_{stg}				– 55 to 150	$^{\circ}\text{C}$
Operating junction temperature range, T_J				– 40 to 150	$^{\circ}\text{C}$
Operating free-air temperature range, T_A				– 40 to 125	$^{\circ}\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				260	$^{\circ}\text{C}$

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Maximum values are calculated using a derating factor based on $R_{\theta JA} = 158^\circ\text{C/W}$ for the D package and $R_{\theta JA} = 176^\circ\text{C/W}$ for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR [‡] ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	791 mW	6.33 mW/ $^\circ\text{C}$	506 mW	411 mW	158 mW
PW	710 mW	5.68 mW/ $^\circ\text{C}$	454 mW	369 mW	142 mW

[‡] Maximum values are calculated using a derating factor based on $R_{\theta JA} = 158^\circ\text{C/W}$ for the D package and $R_{\theta JA} = 176^\circ\text{C/W}$ for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

TPS1101, TPS1101Y

SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS079C – DECEMBER 1993 – REVISED AUGUST 1995

electrical characteristics at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS		TPS1101			TPS1101Y			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = −250 μA		−1	−1.25	−1.5	−1.25			V
V _{SD}	Source-to-drain voltage (diode-forward voltage) [†]	I _S = −1 A, V _{GS} = 0 V		−1.04			−1.04			V
I _{GSS}	Reverse gate current, drain short circuited to source	V _{DS} = 0 V, V _{GS} = −12 V		±100						nA
I _{DSS}	Zero-gate-voltage drain current	V _{DS} = −12 V, V _{GS} = 0 V	T _J = 25°C	−0.5						μA
			T _J = 125°C	−10						
r _{DS(on)}	Static drain-to-source on-state resistance [†]	V _{GS} = −10 V	I _D = −2.5 A	90			90			mΩ
		V _{GS} = −4.5 V	I _D = −1.5 A	134 190			134			
		V _{GS} = −3 V	I _D = −0.5 A	198 310			198			
		V _{GS} = −2.7 V		232 400			232			
g _{fs}	Forward transconductance [†]	V _{DS} = −10 V, I _D = −2 A		4.3			4.3			S

[†] Pulse test: pulse duration $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

dynamic

PARAMETER	TEST CONDITIONS	TPS1101, TPS1101Y			UNIT
		MIN	TYP	MAX	
Q_g Total gate charge	$V_{DS} = -10\ \text{V}$, $V_{GS} = -10\ \text{V}$, $I_D = -1\ \text{A}$		11.25		nC
Q_{gs} Gate-to-source charge			1.5		
Q_{gd} Gate-to-drain charge			2.6		
$t_{d(on)}$ Turn-on delay time	$V_{DD} = -10\ \text{V}$, $R_L = 10\ \Omega$, $I_D = -1\ \text{A}$, $R_G = 6\ \Omega$, See Figures 1 and 2		6.5		ns
$t_{d(off)}$ Turn-off delay time			19		ns
t_r Rise time			5.5		ns
t_f Fall time			13		
$t_{rr(SD)}$ Source-to-drain reverse recovery time	$I_F = 5.3\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		16		

PARAMETER MEASUREMENT INFORMATION

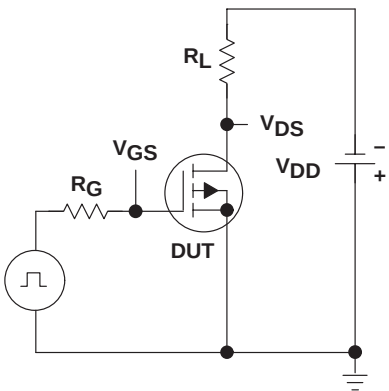


Figure 1. Switching-Time Test Circuit

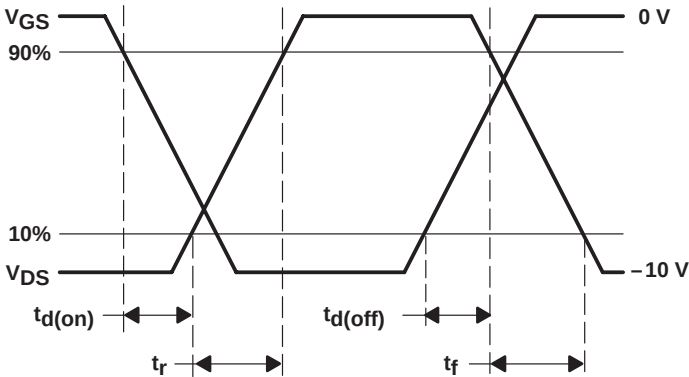


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS

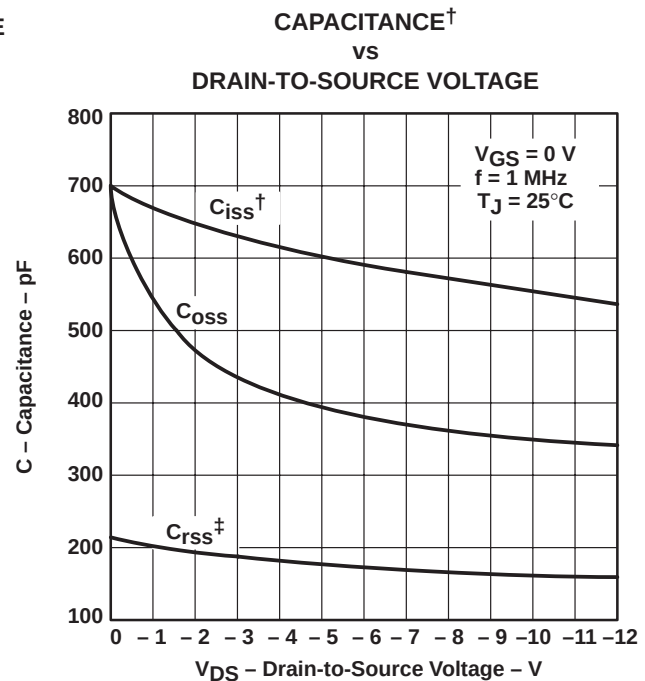
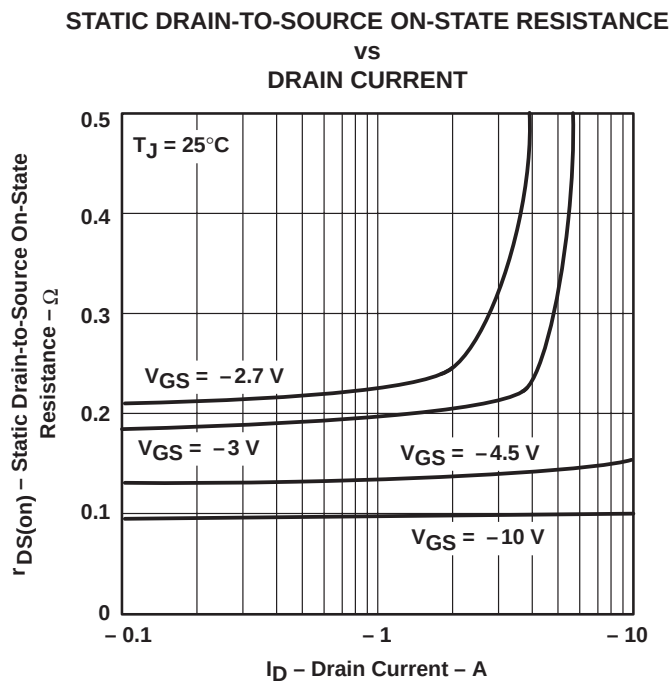
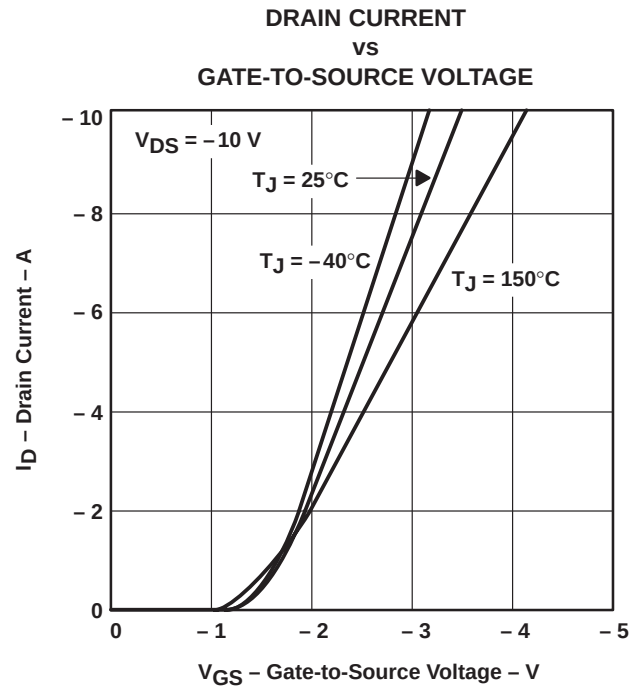
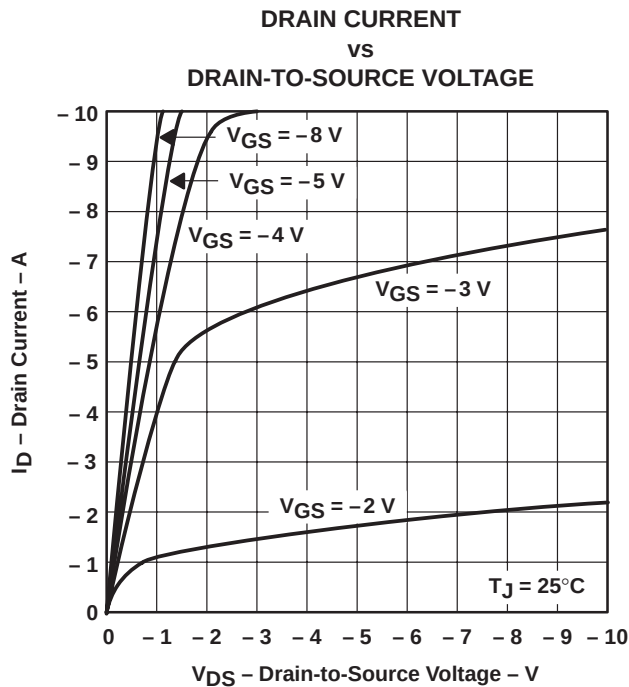
Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

TPS1101, TPS1101Y SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS079C – DECEMBER 1993 – REVISED AUGUST 1995

TYPICAL CHARACTERISTICS



$$† C_{iss} = C_{gs} + C_{gd}, C_{ds(short)}$$

$$‡ C_{rss} = C_{gd}, C_{oss} = C_{ds} + \frac{C_{gs} C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$$

TYPICAL CHARACTERISTICS

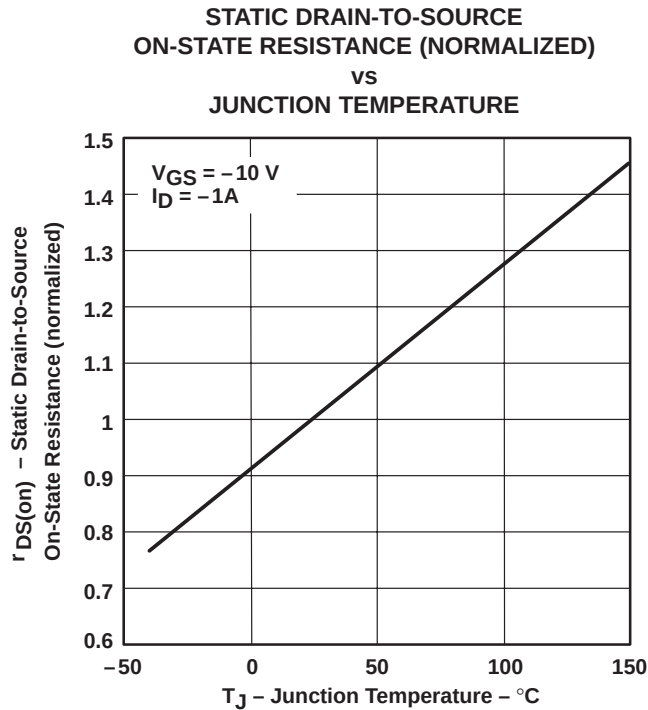


Figure 7

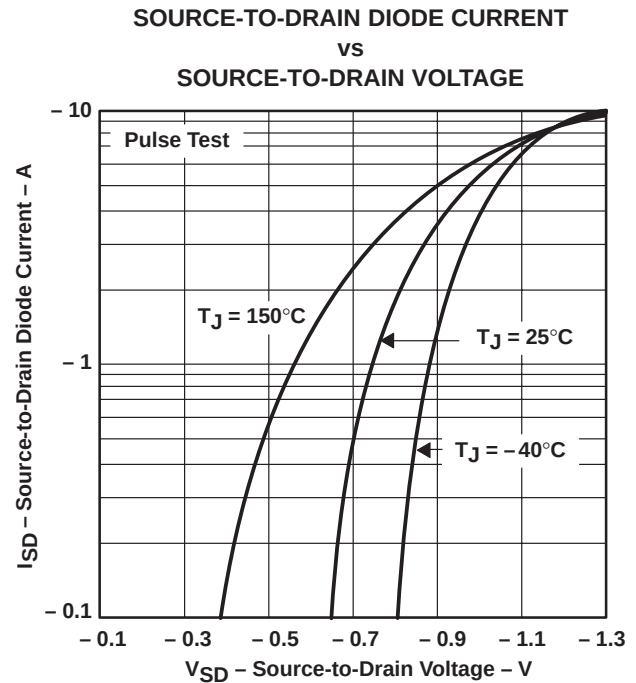


Figure 8

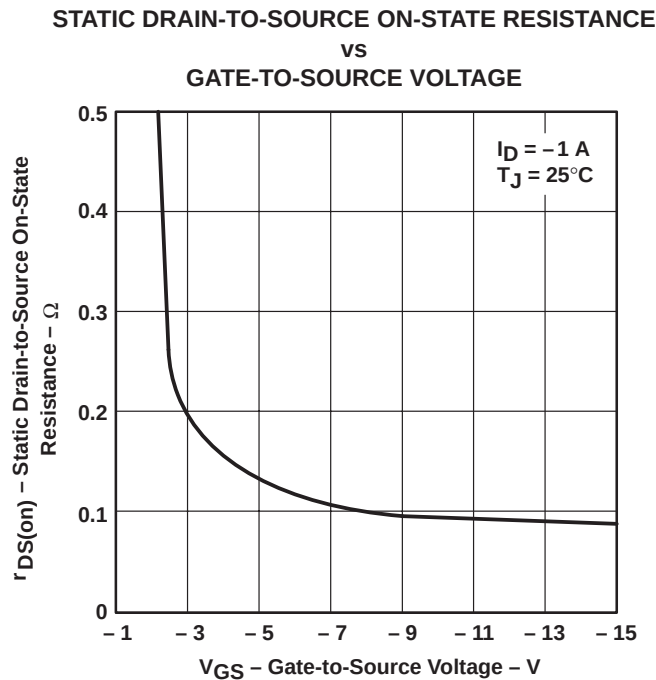


Figure 9

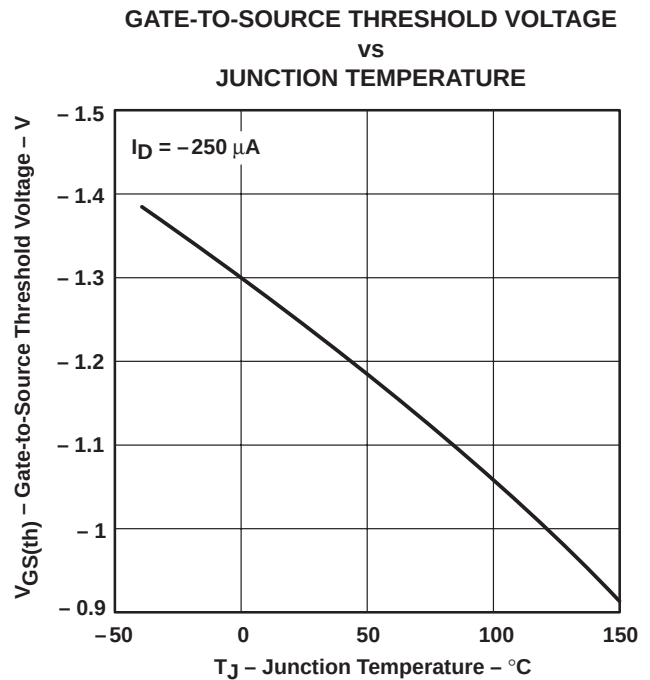


Figure 10

TPS1101, TPS1101Y
SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS079C – DECEMBER 1993 – REVISED AUGUST 1995

TYPICAL CHARACTERISTICS

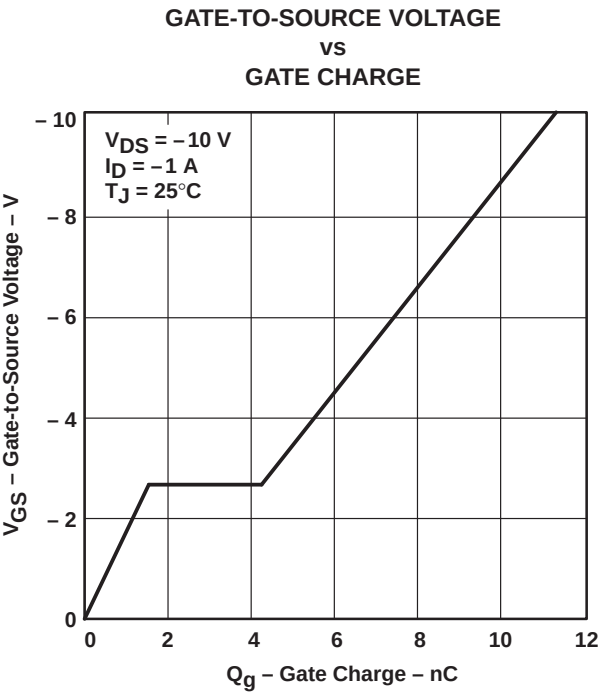
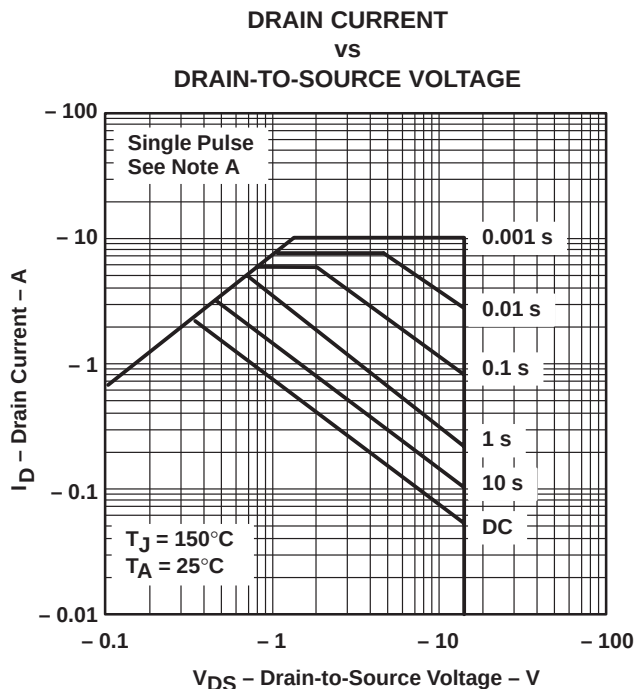


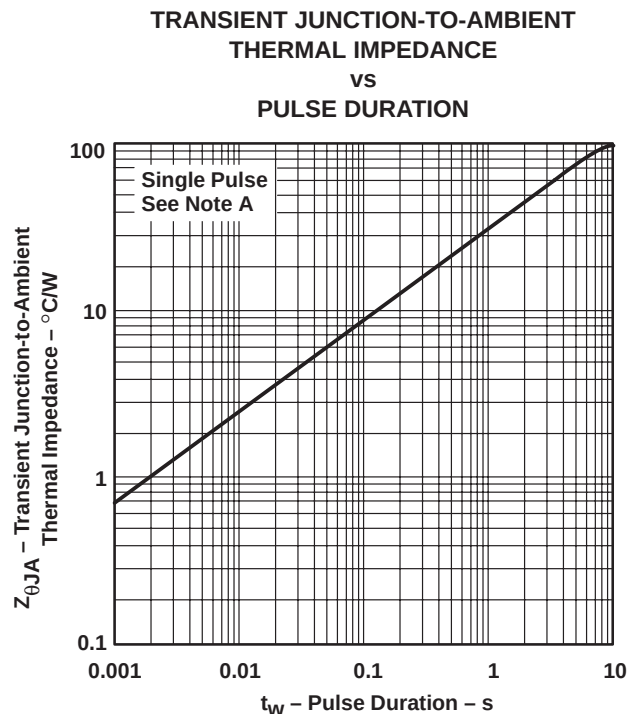
Figure 11

THERMAL INFORMATION



NOTE A: Values are for the D package and are FR4-board-mounted only.

Figure 12



NOTE A: Values are for the D package and are FR4-board-mounted only.

Figure 13

APPLICATION INFORMATION

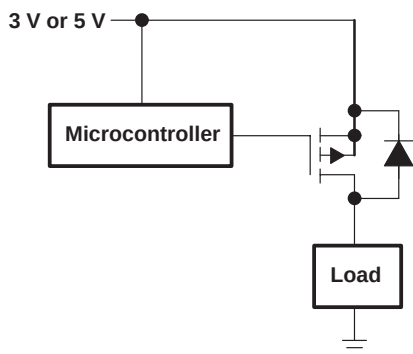


Figure 14. Notebook Load Management

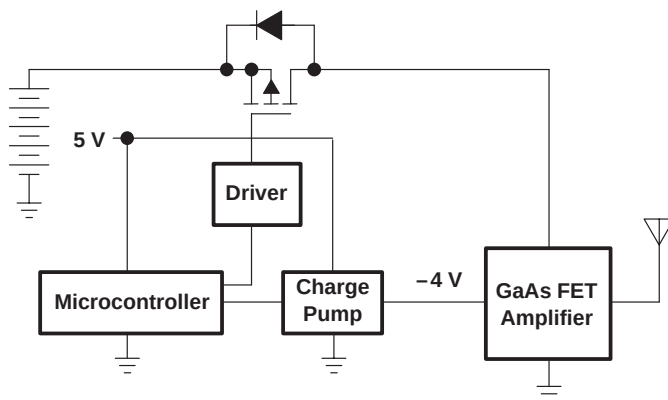


Figure 15. Cellular Phone Output Drive

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS1101D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	1101
TPS1101D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	See TPS1101D	1101
TPS1101DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	1101
TPS1101DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See TPS1101DR	1101
TPS1101PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	PS1101
TPS1101PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See TPS1101PWR	PS1101
TPS1101PWR.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See TPS1101PWR	PS1101

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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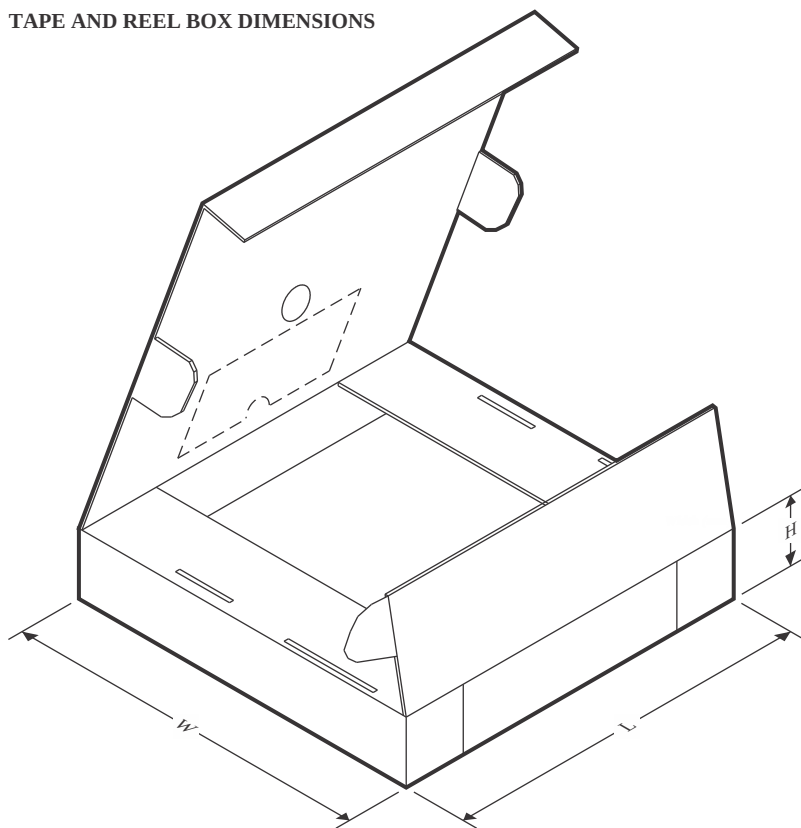
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS1101DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS1101PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

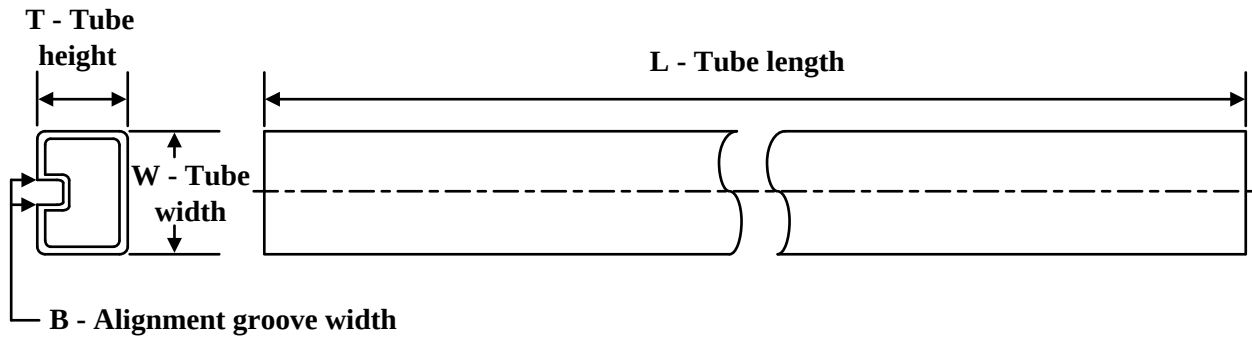
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1101DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS1101PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS1101D	D	SOIC	8	75	507	8	3940	4.32
TPS1101D.A	D	SOIC	8	75	507	8	3940	4.32

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