TPS1663x 60V, 6A eFuse with Adjustable Output Power Limiting

1 Features

- Operating voltage: 4.5V to 60V
  - Absolute maximum: 67V
- Integrated 60V, 31mΩ R_{ON} hot-swap FET
- Adjustable current limit: 0.6A to 6A (±7%)
- Low quiescent current: 21µA in shutdown
- Adjustable output power limiting (TPS16632 and TPS16637) (±6%)
- Adjustable UVLO and OVP cutoff with ±2% accuracy
  - Fixed 39V maximum overvoltage clamp (TPS16632 only)
- Adjustable output slew rate control for inrush current limiting
  - Charges large and unknown capacitive loads through thermal regulation during device power-up
- Power Good output (PGOOD)
- Selectable overcurrent fault response options between auto-retry and latch off (MODE)
- Analog current monitor (IMON) output (±6%)
- UL 2367 recognized
  - File No. E169910
  - RILIM ≥ 3kΩ
- IEC 62368-1 certified
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Available in easy-to-use 24-pin VQFN package

2 Applications

- Factory automation and control – PLC, DCS, HMI, I/O modules, sensor hubs
- Motor drives – CNC, encoder supply
- Electronic circuit breakers
- Telecom radios
- Industrial printers

3 Description

The TPS1663x is an easy-to-use, positive 60V, 6A eFuse with a 31mΩ integrated FET. Protection for the load, source, and eFuse itself are provided along with adjustable features such as accurate overcurrent protection, fast short circuit protection, output slew rate control, overvoltage protection and undervoltage lockout. The TPS16332 device integrates adjustable output power limiting (PLIM) functionality that simplifies and enables compliance to standards such as IEC61010-1 and UL1310. The device also includes adjustable overcurrent functionality. PGOOD can be used for enable and disable control of the downstream DC/DC converters.

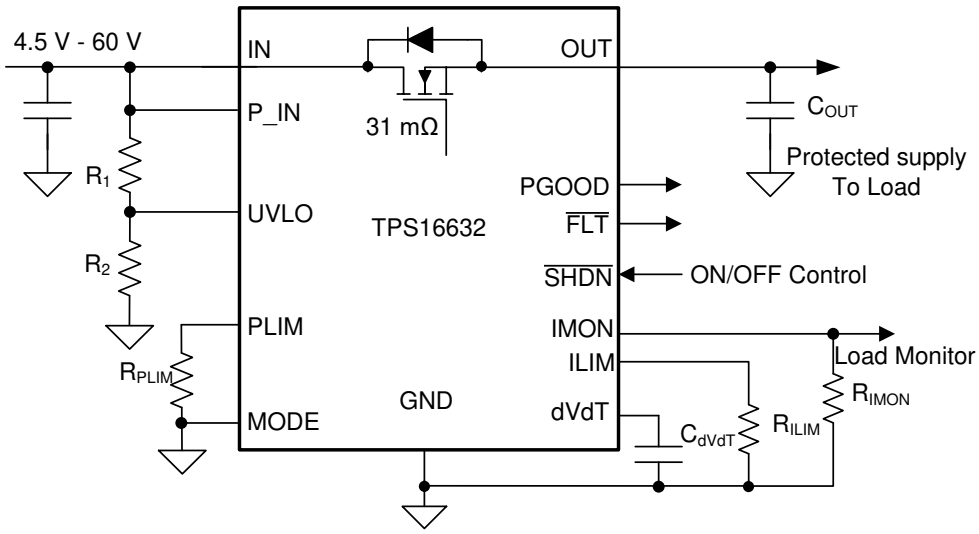
A shutdown pin provides external control for enabling and disabling the internal FET, as well as placing the device in a low current shutdown mode. For system status monitoring and downstream load control, the device provides fault and a precise current monitor output. The MODE pin allows flexibility to configure the device between the two current-limiting fault responses (latch off and auto-retry).

The devices are available in a 4mm × 4mm 24-pin VQFN package and are specified over a –40°C to +125°C temperature range.

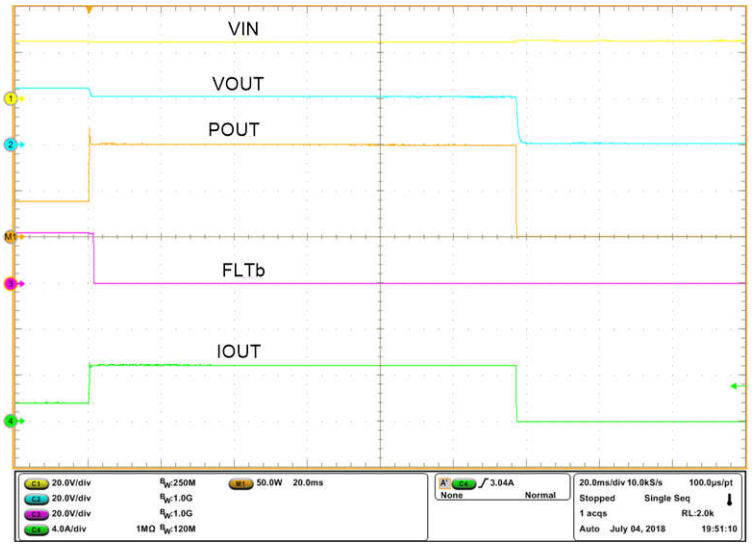
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS16630	VQFN (24)	4.00mm × 4.00mm
TPS16632		
TPS16637		
TPS16630	HTSSOP (20)	6.50mm × 4.40 mm
TPS16637		

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic



Output Power Limiting Performance of TPS16632

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4 Device Comparison Table

PART NUMBER	OVERVOLTAGE PROTECTION	ADJUSTABLE OUTPUT POWER LIMITING
TPS16630	Overvoltage cutoff, adjustable	No
TPS16632	Overvoltage clamp, fixed (39V maximum)	Yes
TPS16637	NA	Yes

5 Pin Configuration and Functions

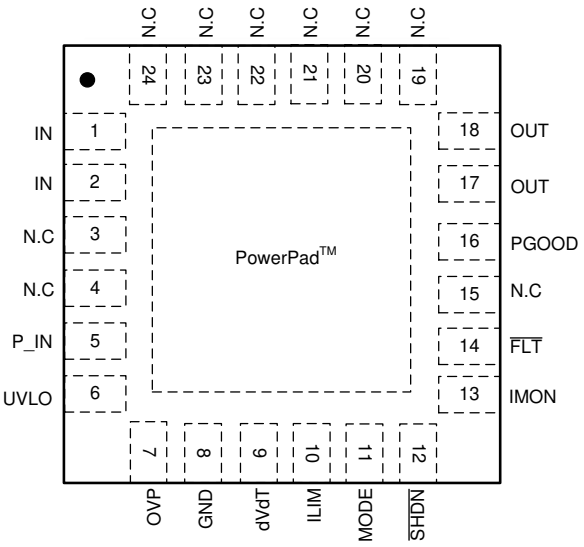


Figure 5-1. TPS16630 RGE Package, 24-Pin VQFN (Top View)

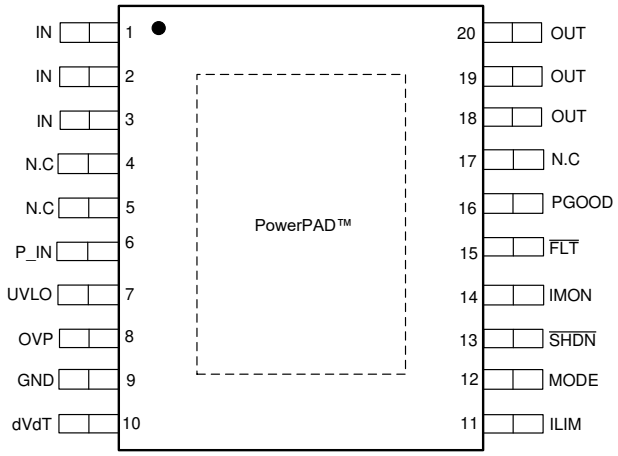


Figure 5-2. TPS16630 PWP Package, 20-Pin HTSSOP (Top View)

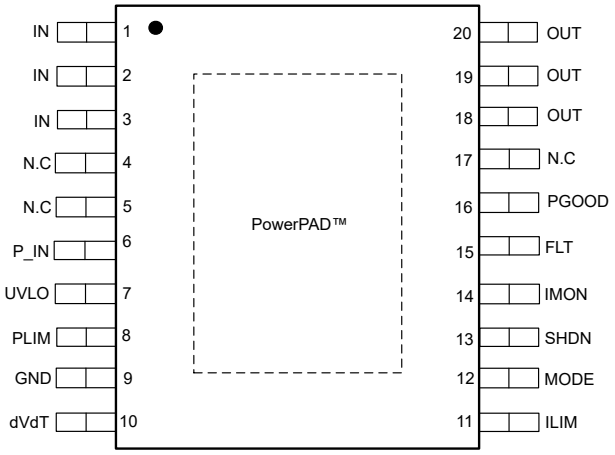


Figure 5-3. TPS16637 PWP Package, 20-Pin HTSSOP (Top View)

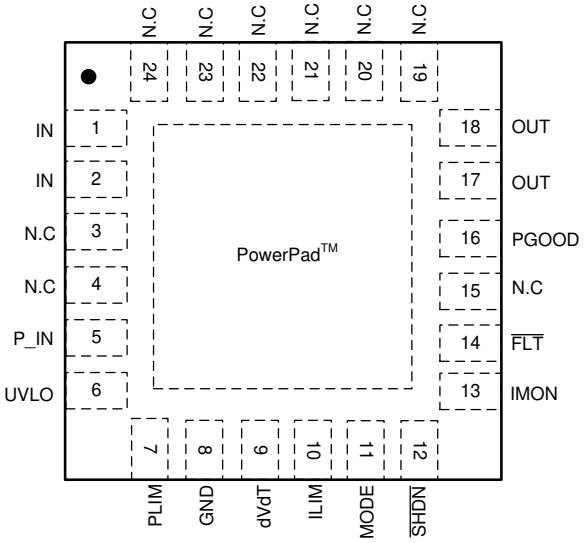


Figure 5-4. TPS16632 and TPS16637 RGE Package, 24-Pin VQFN (Top View)

Table 5-1. Pin Functions

PIN					TYPE (1)	DESCRIPTION
NAME	TPS16630		TPS16632 and TPS16637			
	VQFN	HTSSOP	VQFN	HTSSOP		
IN	1	1	1	1	P	Power input. Connects to the DRAIN of the internal FET.
	2	2	2	2		
	—	3	—	3		
P_IN	5	6	5	6	P	Supply voltage of the device. Always connect P_IN to IN directly.

Table 5-1. Pin Functions (continued)

PIN					TYPE (1)	DESCRIPTION
NAME	TPS16630		TPS16632 and TPS16637			
	VQFN	HTSSOP	VQFN	HTSSOP		
UVLO	6	7	6	7	I	Input for setting the programmable undervoltage lockout threshold. An undervoltage event turns off the internal FET and asserts $\overline{FLT}$ to indicate the power-failure.
OVP	7	8	—	—	I	Input for setting the adjustable overvoltage protection threshold (for TPS16630 only). An overvoltage event turns off the internal FET and asserts $\overline{FLT}$ to indicate the overvoltage fault.
PLIM	—	—	7	8	I	Input for setting the adjustable output power limiting threshold (TPS16632 and TPS16637). Connect a resistor across PLIM to GND to set the output power limit. Connect PLIM to GND if PLIM feature is not used. See *Output Power Limiting, PLIM (TPS16632 Only)* section.
GND	8	9	8	9	—	Connect GND to system ground.
dVdT	9	10	9	10	I/O	A capacitor from this pin to GND sets output voltage slew rate. Leaving this pin floating enables device power up in thermal regulation resulting in fast output charge. See the *Hot Pug-In and In-Rush Current Control* section.
ILIM	10	11	10	11	I/O	A resistor from this pin to GND sets the overload limit. See *Overload and Short Circuit Protection* section.
MODE	11	12	11	12	I	Mode selection pin for Overload fault response. See the *Device Functional Modes* section.
$\overline{SHDN}$	12	13	12	13	I	Shutdown pin. Pulling $\overline{SHDN}$ low makes the device to enter into low power shutdown mode. Cycling $\overline{SHDN}$ pin voltage resets the device that has latched off due to a fault condition.
IMON	13	14	13	14	O	Analog current monitor output. This pin sources a scaled down ratio of current through the internal FET. A resistor from this pin to GND converts current to proportional voltage. If unused, leave it floating.
$\overline{FLT}$	14	15	14	15	O	Fault event indicator. This pin is an open drain output. If unused, leave floating or connect to GND.
PGOOD	16	16	16	16	O	Active High. A high indicates that the internal FET is enhanced. PGOOD goes low when the internal FET is turned OFF during a fault or when $\overline{SHDN}$ is pulled low. If PGOOD is unused, then connect to GND or leave it floating.
OUT	17	18	17	18	P	Power output of the device.
	18	19	18	19		
	—	20	—	20		
N.C	3	4	3	4	—	No connect.
	4	5	4	5		
	15	17	15	17		
	19	—	19	—		
	20	—	20	—		
	21	—	21	—		
	22	—	22	—		
	23	—	23	—		
	24	—	24	—		
PowerPAD™					—	Connect PowerPAD to GND plane for heat sinking. Do not use PowerPAD as the only electrical connection to GND.

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IN, P_IN, OUT, UVLO, $\overline{FLT}$, PGOOD	Input Voltage	–0.3	67	V
IN, P_IN (10ms transient), T_A = 25°C		–0.3	75	
OVP, dVdT, IMON, MODE, $\overline{SHDN}$, ILIM		–0.3	5.5	
$I_{\overline{FLT}}$, I_{dVdT}, I_{PGOOD}	Sink current		10	mA
I_{dVdT}, I_{ILIM}, I_{PLIM}, I_{MODE}, $I_{\overline{SHDN}}$	Source current	Internally limited		
T_J	Operating Junction temperature	–40	150	°C
	Transient junction temperature	–65	$T_{(TSD)}$	
T_{stg}	Storage temperature	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN, P_IN	Input Voltage	4.5		60	V
OUT, UVLO, PGOOD, $\overline{FLT}$		0		60	
OVP, dVdT, IMON, MODE		0		4	
$\overline{SHDN}$		0		5	
ILIM	Resistance	3		30	kΩ
PLIM		60.4		150	
IMON		1			
IN, P_IN, OUT	External Capacitance	0.1			µF
dVdT		10			nF
T_J	Operating Junction temperature	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS1663		UNIT
		RGE (VSON)	PWP (HTSSOP)	
		24 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.4	32.2	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		TPS1663		UNIT
		RGE (VSON)	PWP (HTSSOP)	
		24 PINS	20 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.2	23.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.2	10	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.2	9.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, 4.5V < $V_{(IN)}$ = $V_{(P\_IN)}$ < 60V, $V_{(\overline{SHDN})}$ = 2V, $R_{(ILIM)}$ = 30kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(IN)}$, $V_{(P\_IN)}$	Operating input voltage		4.5		60	V
$IQ_{(ON)}$	Supply current	Enabled: $V_{(\overline{SHDN})}$ = 2V		1.38	1.7	mA
$IQ_{(OFF)}$		$V_{(\overline{SHDN})}$ = 0V		21	60	µA
$V_{(OVC)}$	Over voltage clamp	TPS16632 Only, $V_{(IN)}$ > 40V, $I_{(OUT)}$ = 1mA	35.7	36.6	39	V
UNDERVOLTAGE LOCKOUT (UVLO) INPUT						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.176	1.2	1.224	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		1.09	1.122	1.15	V
$I_{(UVLO)}$	UVLO Input leakage current	0V ≤ $V_{(UVLO)}$ ≤ 60V	–150	8	150	nA
OVERVOLTAGE PROTECTION (OVP) INPUT						
$V_{(OVPR)}$	over-voltage threshold voltage, rising		1.176	1.2	1.224	V
$V_{(OVPF)}$	over-voltage threshold voltage, falling		1.09	1.122	1.15	V
$I_{(OVP)}$	OVP Input leakage current	0V ≤ $V_{(OVP)}$ ≤ 4V	–150	0	150	nA
CURRENT LIMIT PROGRAMMING (ILIM)						
$I_{(OL)}$	Over Load current limit	$R_{(ILIM)}$ = 30kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1V	0.54	0.6	0.66	A
		$R_{(ILIM)}$ = 9kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1V	1.84	2	2.16	A
		$R_{(ILIM)}$ = 4.02kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1V	4.185	4.5	4.815	A
		$R_{(ILIM)}$ = 3kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1V	5.58	6	6.42	A
$I_{(FASTRIP)}$	Fast-trip comparator threshold			2x$I_{(OL)}$		A
$I_{(SCP)}$	Short Circuit Protect current			45		A
OUTPUT POWER LIMITING CONTROL (PLIM) INPUT – TPS16632 and TPS16637 ONLY						
$V_{(SEL\_PLIM)}$	Power Limit Feature select threshold		180	210	240	mV
$I_{(PLIM)}$	PLIM sourcing current	$V_{(PLIM)}$ = 0V	4.4	5.02	5.6	µA
$P_{(PLIM)}$	Max Output power	$R_{(PLIM)}$ = 100kΩ	94	100	106	W
		$R_{(PLIM)}$ = 150kΩ (1)	141.9	151	160.1	W
$P_{(PLIM)}$	Max Output power	$R_{(PLIM)}$ = 100kΩ, V_{IN} = 54V, TPS16637		100		W
PASS FET OUTPUT (OUT)						
R_{ON}	IN to OUT total ON resistance	0.6A ≤ $I_{(OUT)}$ ≤ 6A, T_J = 25°C	26	30.44	34.5	mΩ
R_{ON}	IN to OUT total ON resistance	0.6A ≤ $I_{(OUT)}$ ≤ 6A, T_J = 85°C	33		45	mΩ

6.5 Electrical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, 4.5V < $V_{(IN)}$ = $V_{(P\_IN)}$ < 60V, $V_{(\overline{SHDN})}$ = 2V, $R_{(ILIM)}$ = 30kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ON}	IN to OUT total ON resistance	0.6A ≤ $I_{(OUT)}$ ≤ 6A, –40°C ≤ T_J ≤ +125°C	19	30.44	53	mΩ
OUTPUT RAMP CONTROL (dVdT)						
$I_{(dVdT)}$	dVdT charging current	$V_{(dVdT)}$ = 0V	1.775	2	2.225	µA
$GAIN_{(dVdT)}$	dVdT to OUT gain	$V_{(OUT)}$ /$V_{(dVdT)}$	23.5	25	26	V/V
$V_{(dVdTmax)}$	dVdT maximum capacitor voltage		3.8	4.17	4.75	V
$R_{(dVdT)}$	dVdT discharging resistance		10	16.6	26.6	Ω
CURRENT MONITOR OUTPUT (IMON)						
$GAIN_{(IMON)}$	Gain factor $I_{(IMON)}$:$I_{(OUT)}$	0.6A ≤ $I_{(OUT)}$ < 2A	25.66	27.9	30.14	µA/A
		2A ≤ $I_{(OUT)}$ ≤ 6A	26.22	27.9	29.58	µA/A
LOW IQ SHUTDOWN ($\overline{SHDN}$) INPUT						
$V_{(\overline{SHDN})}$	Open circuit voltage	$I_{(\overline{SHDN})}$ = 0.1 µA	2.48	2.7	3.3	V
$V_{(SHUTF)}$	$\overline{SHDN}$ threshold voltage for low IQ shutdown, falling		0.8			V
$V_{(SHUTR)}$	$\overline{SHDN}$ threshold rising				2	V
$I_{(\overline{SHDN})}$	Leakage current	$V_{(\overline{SHDN})}$ = 0V	–10			µA
FAULT FLAG ($\overline{FLT}$): ACTIVE LOW						
$R_{(\overline{FLT})}$	$\overline{FLT}$ Pull-down resistance		36	70	130	Ω
$I_{(\overline{FLT})}$	$\overline{FLT}$ Input leakage current	0V ≤ $V_{(\overline{FLT})}$ ≤ 60V	–150	6	150	nA
POWER GOOD (PGOOD)						
$R_{(PGOOD)}$	PGOOD Pull-down resistance		36	70	130	Ω
$I_{(PGOOD)}$	PGOOD Input leakage current	0V ≤ $V_{(PGOOD)}$ ≤ 60V	–150	6	150	nA
THERMAL PROTECTION						
$T_{(J\_REG)}$	Thermal regulation set point		136	145	154	ºC
$T_{(TSD)}$	Thermal shutdown (TSD) threshold, rising			165		ºC
$T_{(TSDhyst)}$	TSD hysteresis			11		ºC
MODE						
MODE_SEL	Mode selection	MODE = Open		Latch		
		MODE = Short to GND		Auto – Retry		

(1) Parameter guaranteed by design and characterization, not tested in production

6.6 Timing Requirements

–40°C ≤ T_A = T_J ≤ +125°C, 4.5V < $V_{(IN)}$ = $V_{(P\_IN)}$ < 60V, $V_{(\overline{SHDN})}$ = 2V, $R_{(ILIM)}$ = 30kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
UVLO INPUT (UVLO)						
UVLO_$t_{on(dly)}$	UVLO switch turnon delay	UVLO↑ (100mV above $V_{(UVLOR)}$) to $V_{(OUT)}$ = 100mV , $C_{(dVdT)}$ ≥ 10nF, [$C_{(dVdT)}$ in nF]		742 + 49.5x $C_{(dVdT)}$		µs
UVLO_$t_{off(dly)}$	UVLO switch turnoff delay	UVLO↓(20mV below $V_{(UVLOF)}$) to $\overline{FLT}$↓	9	11	16	µs
$t_{UVLO\_FLT(dly)}$	UVLO to Fault de-assertion delay	UVLO↑ to $\overline{FLT}$ ↑ delay	500	617	700	µs
OVER VOLTAGE PROTECTION INPUT (OVP)						
OVP_$t_{off(dly)}$	OVP switch turnOFF delay	OVP↑ (20mV above $V_{(OVPR)}$) to $\overline{FLT}$↓	8.5	11	14	µs

6.6 Timing Requirements (continued)

–40°C ≤ T_A = T_J ≤ +125°C, 4.5V < $V_{(IN)}$ = $V_{(P\_IN)}$ < 60V, $V_{(\overline{SHDN})}$ = 2V, $R_{(ILIM)}$ = 30kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
OVP_$t_{on(dly)}$	OVP switch disable delay	OVP↓ (100mV below $V_{(OVPF)}$) to FET ON , $C_{(dVdT)}$ ≥ 10nF, [$C_{(dVdT)}$ in nF]		150 + 49.5x $C_{(dVdT)}$		µs
$t_{OVC(dly)}$	Maximum duration in over voltage clamp operation	TPS16632 Only		162		ms
OVC_$t_{FLT(dly)}$	$\overline{FLT}$ assertion delay in over voltage clamp operation	TPS16632 Only		617		µs
SHUTDOWN CONTROL INPUT ($\overline{SHDN}$)						
$t_{SD(dly)}$	SHUTDOWN entry delay	$\overline{SHDN}$↓ (below $V_{(SHUTF)}$) to FET OFF	0.8	1	1.5	µs
CURRENT LIMIT						
$t_{FASTTRIP(dly)}$	Hot-short response time	$I_{(OUT)}$ > $I_{(SCP)}$		1		µs
	Soft short response	$I_{(FASTTRIP)}$ < $I_{(OUT)}$ < $I_{(SCP)}$	2.2	3.2	4.5	µs
$t_{CL\_PLIM(dly)}$	Maximum duration in current & (power limiting: TPS16632 and TPS16637)		129	162	202	ms
$t_{CL\_PLIM\_FLT(dly)}$	$\overline{FLT}$ delay in current & (power limiting: TPS16632 and TPS16637)		1.09	1.3	1.6	ms
OUTPUT RAMP CONTROL (dVdT)						
$t_{(FASTCHARGE)}$	Output ramp time in fast charging	$C_{(dVdT)}$ = Open, 10% to 90% $V_{(OUT)}$, $C_{(OUT)}$ = 1 µF; $V_{(IN)}$ = 24V	350	495	700	µs
$t_{(dVdT)}$	Output ramp time	$C_{(dVdT)}$ = 22nF, 10% to 90% $V_{(OUT)}$, $V_{(IN)}$ = 24V		8.35		ms
POWER GOOD (PGOOD)						
t_{PGOODR}	PGOOD delay (deglitch) time	Rising edge	8	11.5	13	ms
t_{PGOODF}	PGOOD delay (deglitch) time	Falling edge	8	10	13	ms
THERMAL PROTECTION						
$t_{(TSD\_retry)}$	Retry delay in TSD	MODE = GND	500	648	800	ms
$t_{(Treg\_timeout)}$	Thermal Regulation Timeout		1.1	1.25	1.5	s

6.7 Typical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = $V_{(P\_IN)}$ = 24V, $V_{(\overline{SHDN})}$ = 2V, $R_{(ILIM)}$ = 30kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1µF, $C_{(dVdT)}$ = OPEN (unless stated otherwise)

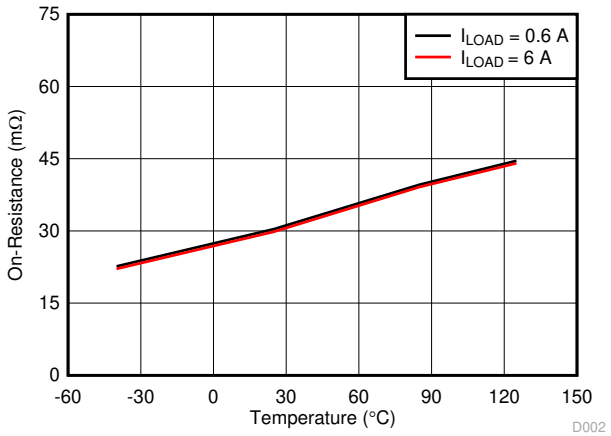
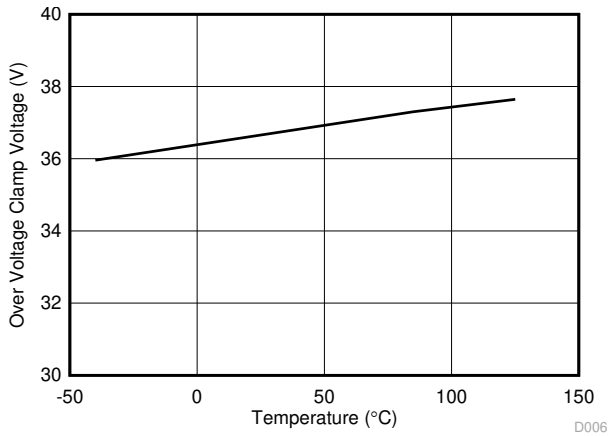


Figure 6-1. On-Resistance vs Temperature Across Load Current



TPS16632

Figure 6-2. Overvoltage Clamp Threshold vs Temperature

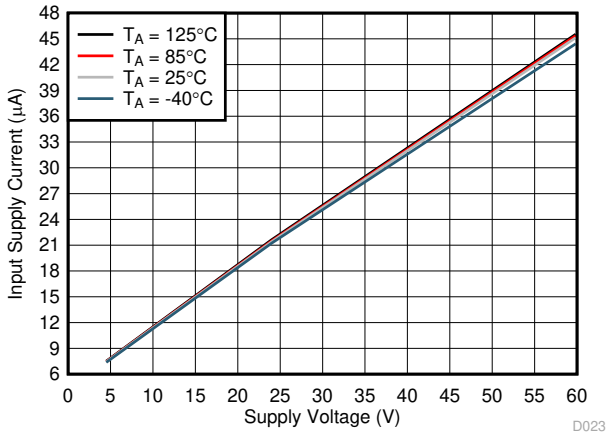


Figure 6-3. Input Supply Current vs Supply Voltage in Shutdown

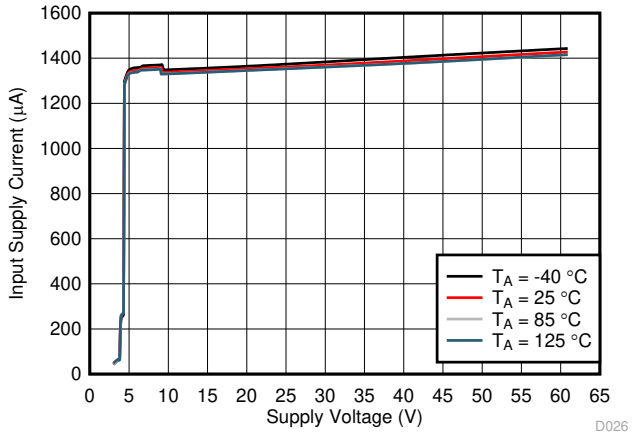


Figure 6-4. Input Supply Current vs Supply Voltage During Normal Operation

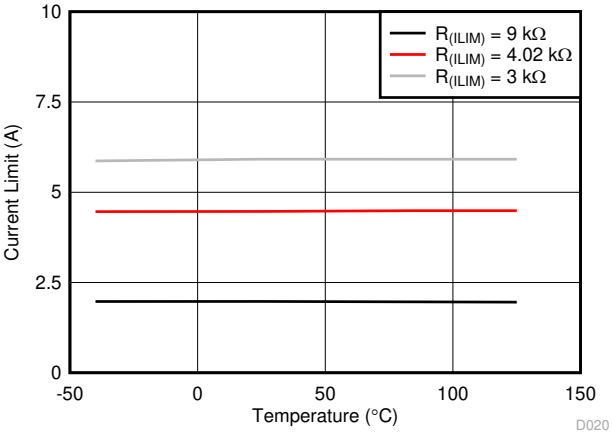


Figure 6-5. Overload Current Limit vs Temperature

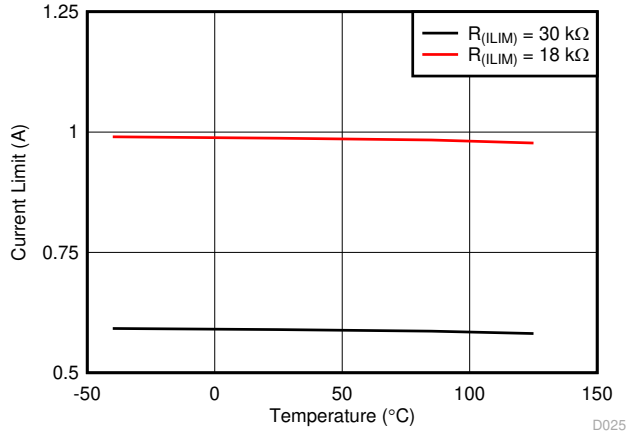


Figure 6-6. Overload Current Limit vs Temperature

6.7 Typical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = $V_{(P\_IN)}$ = 24V, $V_{(\overline{SHDN})}$ = 2V, $R_{(ILIM)}$ = 30kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1µF, $C_{(dVdT)}$ = OPEN (unless stated otherwise)

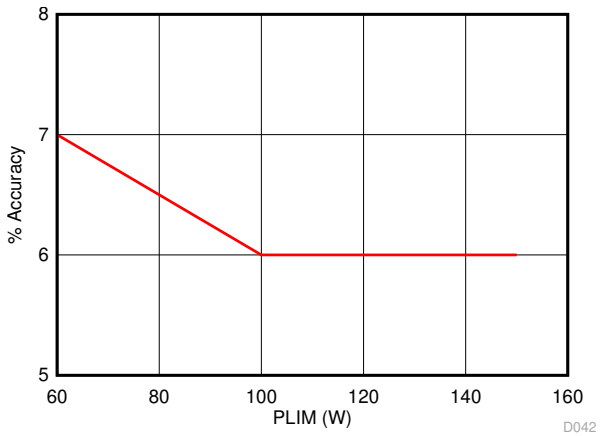


Figure 6-7. Output Power Limiting Accuracy vs PLIM

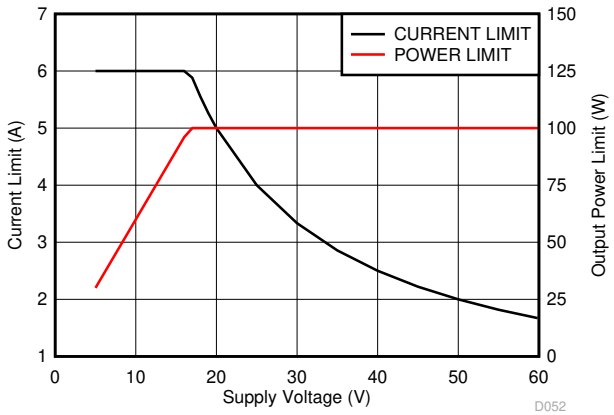


Figure 6-8. Power Limit, Current Limit vs Supply Voltage

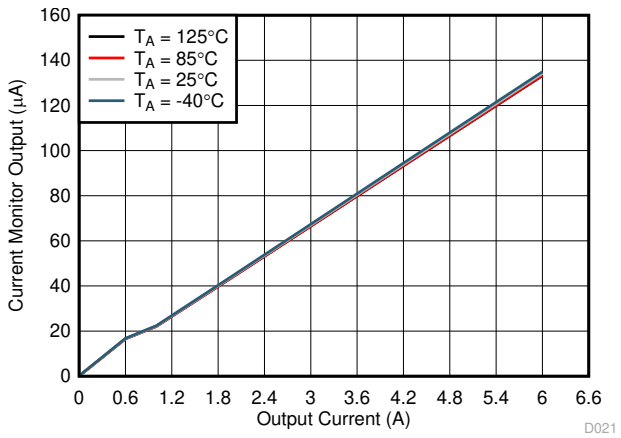


Figure 6-9. Current Monitor Output vs Output Current

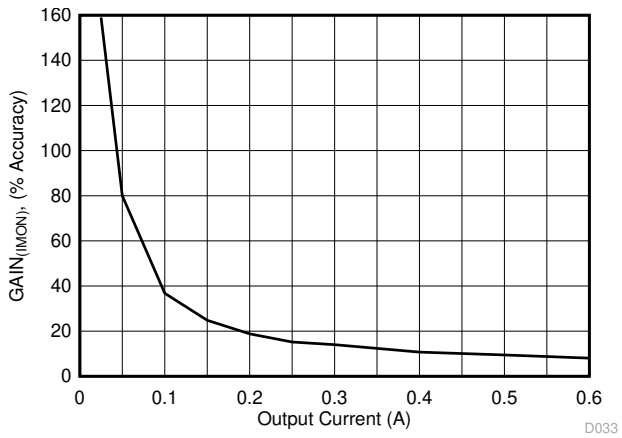


Figure 6-10. IMON Gain Accuracy at Low Output Current Levels

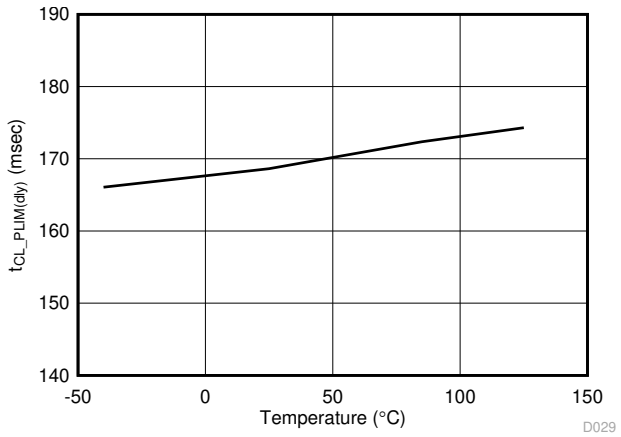


Figure 6-11. Maximum Duration in Current and Power Limiting vs Temperature

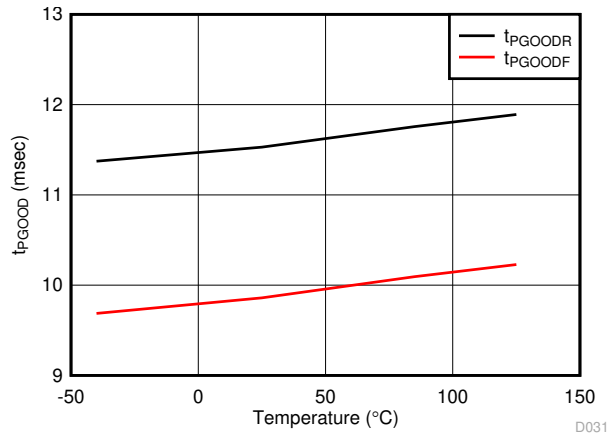
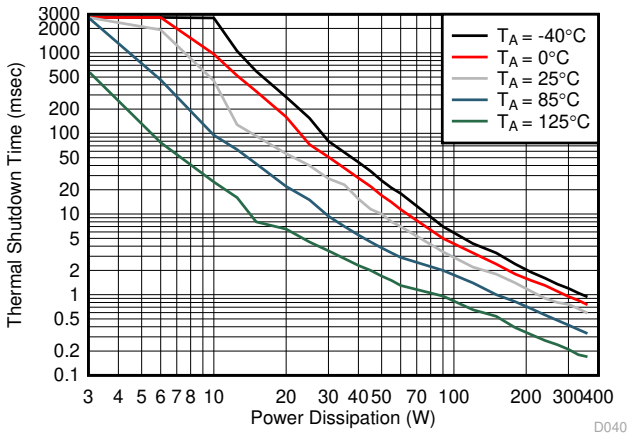


Figure 6-12. PGOOD Rising and Falling Delay vs Temperature

6.7 Typical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = $V_{(P\_IN)}$ = 24V, $V_{(\overline{SHDN})}$ = 2V, $R_{(ILIM)}$ = 30kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1µF, $C_{(dVdT)}$ = OPEN (unless stated otherwise)



Taken on VQFN device on EVM Board

Figure 6-13. Thermal Shutdown Time vs Power Dissipation

7 Parameter Measurement Information

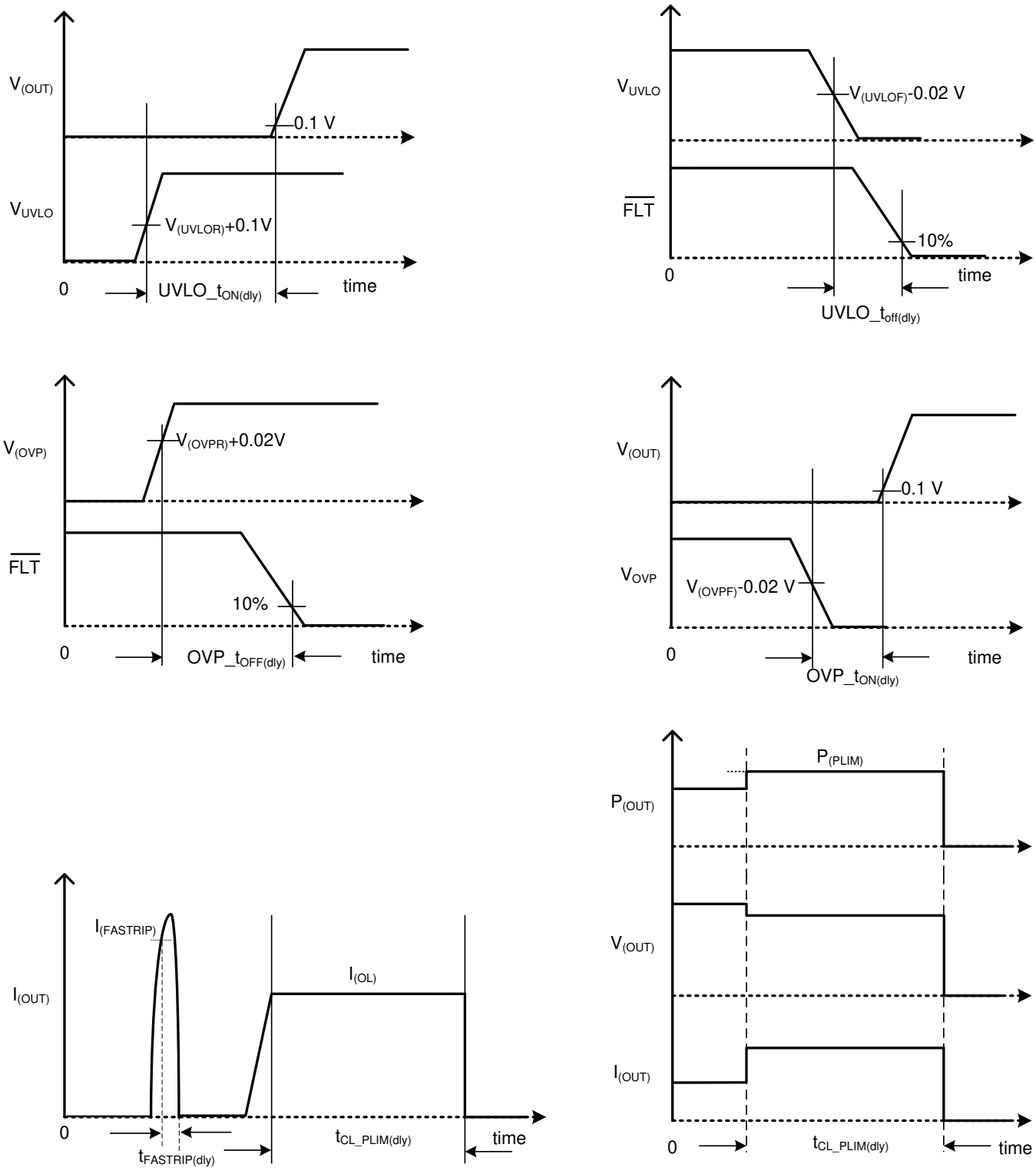


Figure 7-1. Timing Waveforms

8 Detailed Description

8.1 Overview

The TPS1663x is a family of 60V industrial eFuses. The device provides robust protection for all systems and applications powered from 4.5V to 60V. For hot-pluggable boards, the device provides hot-swap power management with in-rush current control and programmable output voltage slew rate features using the dVdT pin. Load, source, and device protections are provided with many programmable features including overcurrent, overvoltage and undervoltage. The 60V maximum DC operating and 62V absolute maximum voltage rating enables system protection from 60V DC input supply faults from industrial SELV power supplies. The precision overcurrent limit (±7% at 6A) helps to minimize over design of the input power supply, while the fast response short circuit protection 1µs (typical) immediately isolates the faulty load from the input supply when a short circuit is detected.

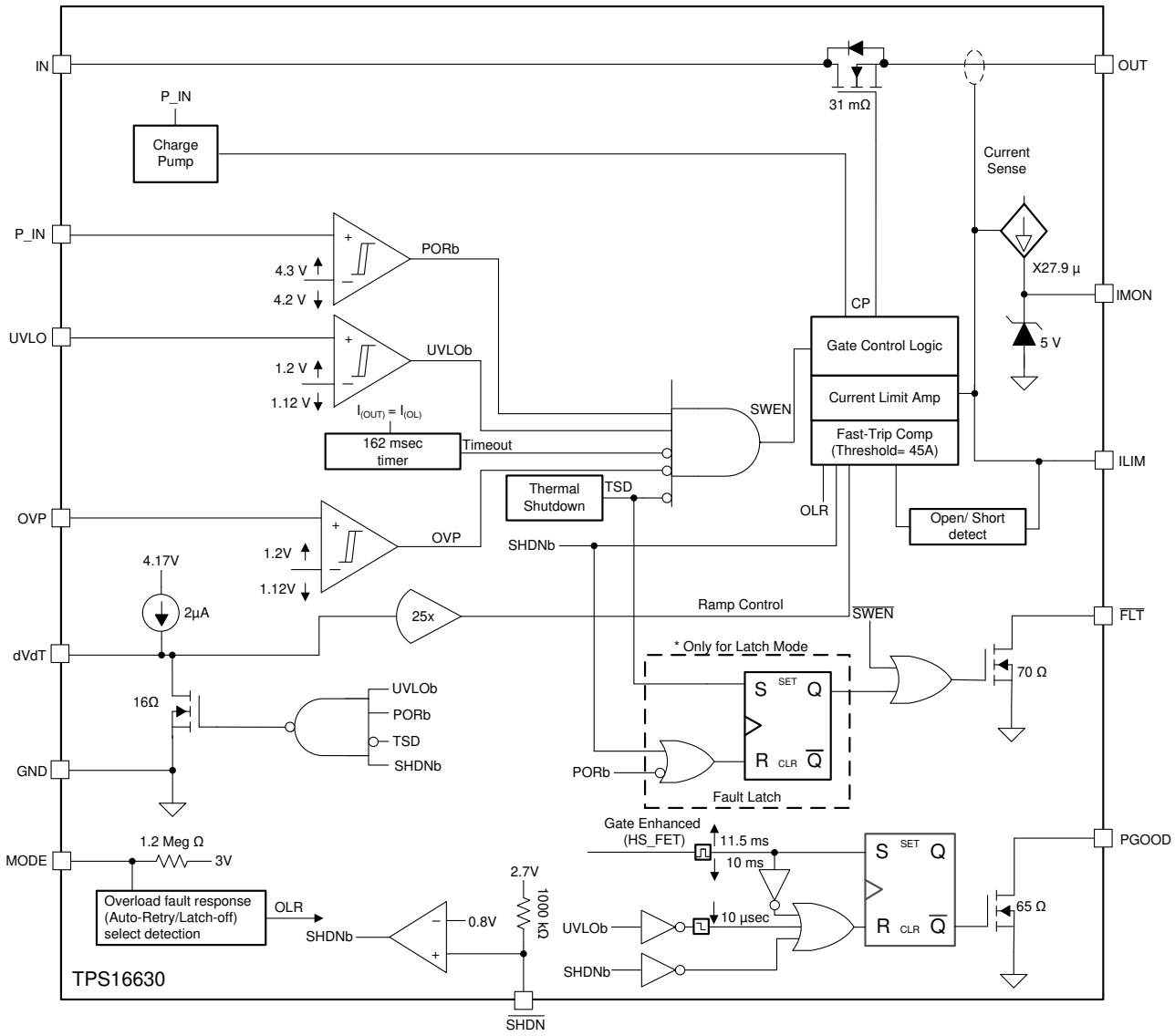
The TPS16632 device integrate adjustable output power limiting (PLIM) functionality that simplifies the system design requiring compliance in accordance to standards like IEC61010-1 and UL1310.

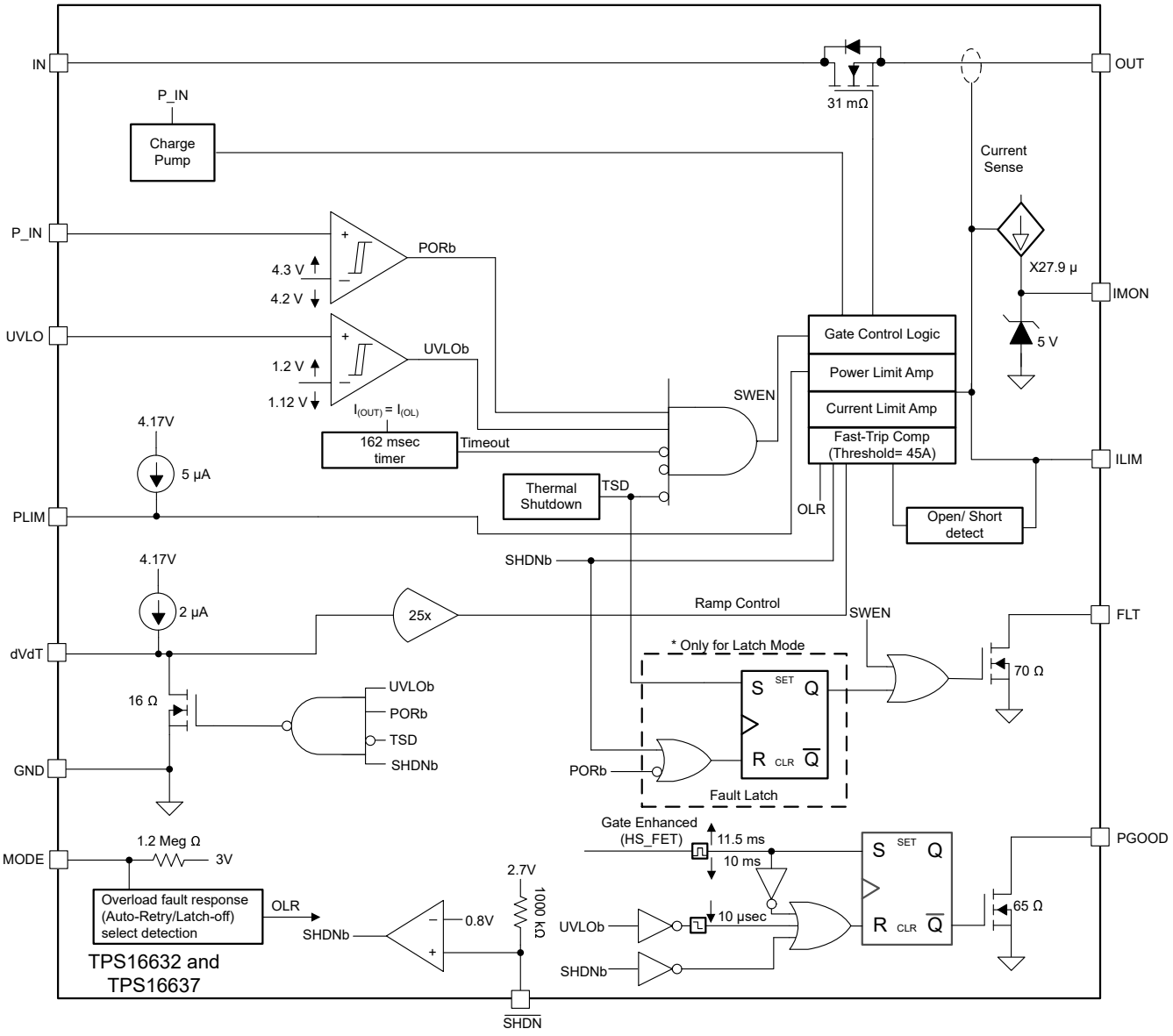
The device provides precise monitoring of voltage bus for brown-out and overvoltage conditions and asserts fault signal for the downstream system. The device's overall threshold accuracy of 2% ensures tight supervision of bus, eliminating the need for a separate supply voltage supervisor chip.

Additional features of the TPS1663x include:

- ±6% current monitor output (IMON) for health monitoring of the system
- A choice of latch off or automatic restart mode response during current limit, power limit, and thermal fault using MODE pin
- PGOOD indicator output
- Overtemperature protection to safely shutdown in the event of an overcurrent event
- De-glitched fault reporting for supply brown-out and overvoltage faults
- Enable and Disable control from an MCU using $\overline{\text{SHDN}}$ pin

8.2 Functional Block Diagram





8.3 Feature Description

8.3.1 Hot Plug-In and In-Rush Current Control

The devices are designed to control the in-rush current upon insertion of a card into a live backplane or other *hot* power source. This design limits the voltage sag on the backplane supply voltage and prevents unintended resets of the system power. The controlled start-up also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to GND defines the slew rate of the output voltage at power-on. The fastest output slew rate of 24V/500µs can be achieved by leaving dVdT pin floating. The inrush current can be calculated using Equation 1.

$$I = C \times \frac{dV}{dT} \geq I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{t_{dVdT}} \quad (1)$$

where

$$t_{dVdT} = 20.8 \times 10^{3} \times V_{(IN)} \times C_{(dVdT)} \quad (2)$$

Figure 8-1 illustrates in-rush current control performance of the device during Hot Plug-In.

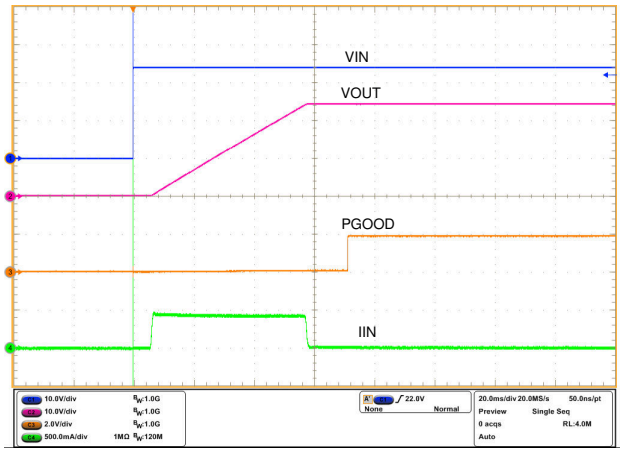


Figure 8-1. Hot Plug In and In-Rush Current Control at 24V Input

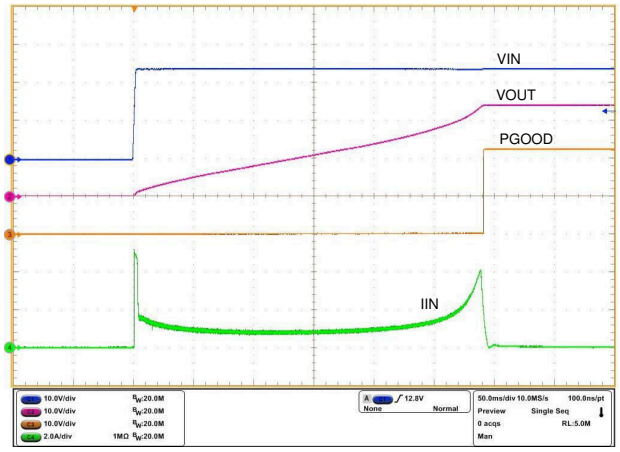
8.3.1.1 Thermal Regulation Loop

The average power dissipation within the eFuse during power up with a capacitive load can be calculated using Equation 3.

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (3)$$

System designs requiring to charge large output capacitors rapidly can result in an operating point that exceeds the power dissipation versus time boundary limits of the device defined by Figure 6-13 characteristic curve. This event can result in increase in junction temperature beyond the device's maximum allowed junction temperature. To keep the junction temperature within the operating range, the thermal regulation control loop regulates the junction temperature at $T_{(J\_REG)}$, 145°C (typical) by controlling the inrush current profile and thereby limiting the power dissipation within the device automatically. An internal 1.25 sec (typical), $t_{(Treg\_timeout)}$ timer starts from the instance the thermal regulation operation kicks in. If the output does not power up within this time then the internal FET is turned OFF. Subsequent operation of the device depends on the MODE configuration (auto-retry or latch OFF) setting as per the Table 8-1. The maximum time-out of 1.25 sec (typical) in thermal regulation loop operation ensures that the device and the system board does not heat up during steady fault conditions such as wake up with output short-circuit. This scheme ensures reliable power-up operation.

Thermal regulation control loop is internally enabled during power up by $V_{(IN)}$, UVLO cycling and turn ON using $\overline{SHDN}$ control. Figure 8-2 illustrates performance of the device operating in thermal regulation loop during power up by $V_{(IN)}$ with a large output capacitor. The thermal regulation loop gets disabled internally after the power up sequence when the internal FET's gate gets fully enhanced or when the $t_{(Treg\_timeout)}$ of 1.25 sec (typical) time is elapsed.



C_{dVdT} = Open C_{OUT} = 15mF R_{ILIM} = 4.02kΩ

Figure 8-2. Thermal Regulation Loop Response During Power Up With Large Capacitive Load

8.3.2 Undervoltage Lockout (UVLO)

The TPS1663x devices feature an accurate ± 2% adjustable undervoltage lockout functionality. When the voltage at UVLO pin falls below $V_{(UVLOF)}$ during input undervoltage fault, the internal FET quickly turns off and $\overline{FLT}$ is asserted. The UVLO comparator has a hysteresis of 78mV (typical). To set the input UVLO threshold, connect a resistor divider network from IN supply to UVLO terminal to GND as shown in Figure 8-3. If the Undervoltage Lockout function is not needed, the UVLO terminal must be connected to the IN terminal. UVLO terminal must not be left floating.

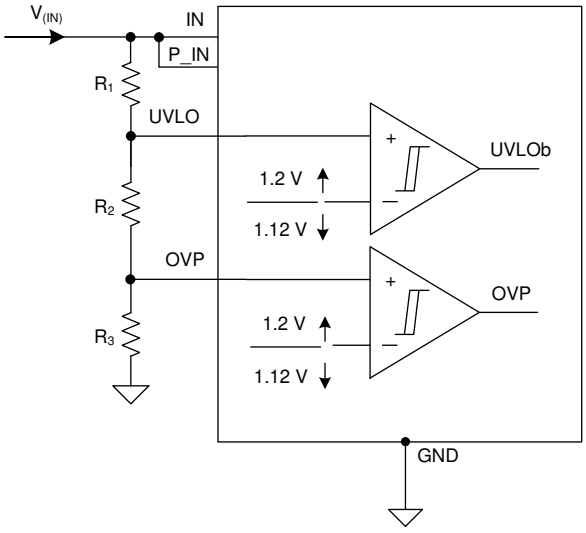


Figure 8-3. UVLO and OVP Thresholds Set by R_1, R_2, and R_3

8.3.3 Overvoltage Protection (OVP)

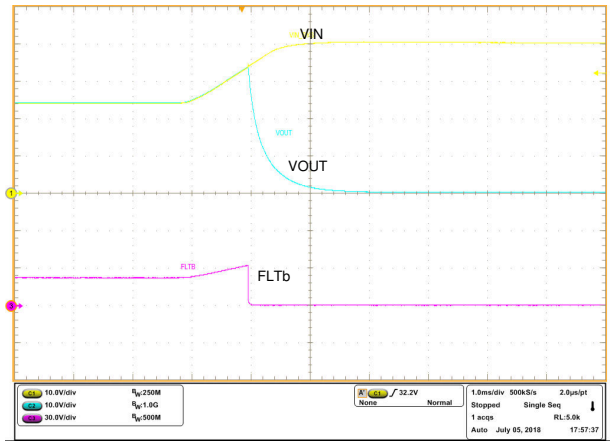
The TPS1663x incorporate circuitry to protect the system during overvoltage conditions. The TPS16630 features an accurate ± 2% adjustable overvoltage cut off functionality. A voltage more than $V_{(OVPR)}$ on OVP pin turns off the internal FET and protects the downstream load. To program the OVP threshold externally, connect a resistor divider from IN supply to OVP terminal to GND as shown in Figure 8-3. The TPS16632 features an internally fixed 39V maximum overvoltage clamp $V_{(OVC)}$ functionality. The TPS16632 clamps the output voltage to $V_{(OVC)}$,

when the input voltage exceeds 40V. During the output voltage clamp operation, the power dissipation in the internal MOSFET is

$$PD = \left[V_{(IN)} - V_{(OVC)}\right] \times I_{(OUT)} \quad (4)$$

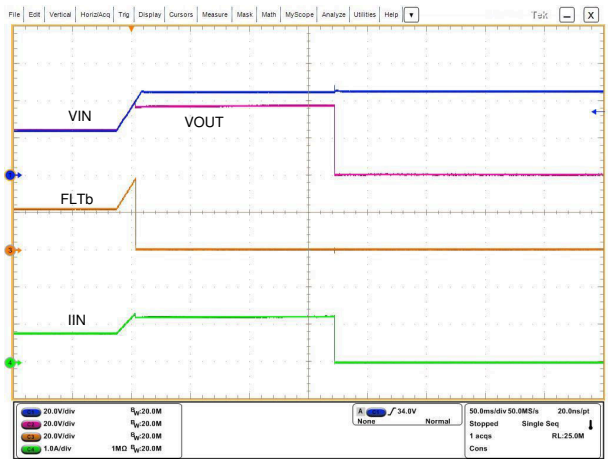
Excess power dissipation for a prolonged period can increase the device temperature. To avoid this, the internal FET is operated in overvoltage clamp for a maximum duration of $t_{OVC(dly)}$, 162msec (typical). After this duration, the internal FET is turned OFF and the subsequent operation of the device depends on the MODE configuration (auto-retry or latch off) setting as per the Table 8-1.

Figure 8-4 illustrates the overvoltage cut-off functionality and Figure 8-5 illustrates the overvoltage clamp functionality. $\overline{FLT}$ is asserted after a delay of 617µs (typical) after entering in overvoltage clamp mode and remains asserted until the overvoltage fault is removed.



TPS16630 OVP Setting at 33V

Figure 8-4. Overvoltage Cut-Off Response at 33V Level



TPS16632 C_{OUT} = 10 µF, $\overline{FLT}$ connected to V_{OUT} R_{LOAD} = 30 Ω

Figure 8-5. Overvoltage Clamp Response

8.3.4 Overload and Short Circuit Protection

The device monitors the load current by sensing the voltage across the internal sense resistor. The FET current is monitored during start-up and normal operation.

8.3.4.1 Overload Protection

The TPS1663x devices feature accurate overload current limiting and fast short circuit protection feature. If the load current exceeds the programmed current limit I_{OL}, the device regulates the current through it at I_{OL} eventually reducing the output voltage. The power dissipation across the device during this operation is:

$$(V_{IN} - V_{OUT}) \times I_{OL} \quad (5)$$

This can heat up the device and eventually enter into thermal shutdown. The maximum duration for the overcurrent through the FET is $t_{CL\_PLIM(dly)}$, 162msec (typical). If the thermal shutdown occurs before this time the internal FET turns OFF and the device operates either in auto-retry or latch off mode based on MODE pin configuration in Table 8-1. Set the current limit using Equation 6.

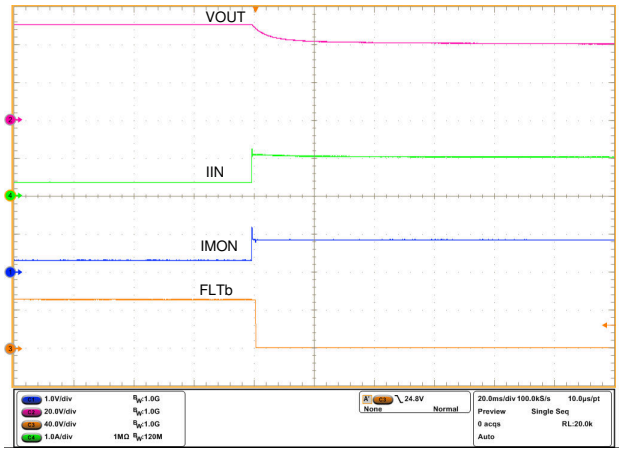
$$I_{OL} = \frac{18}{R_{(ILIM)}} \quad (6)$$

where

- $I_{(OL)}$ is the overload current limit in Ampere

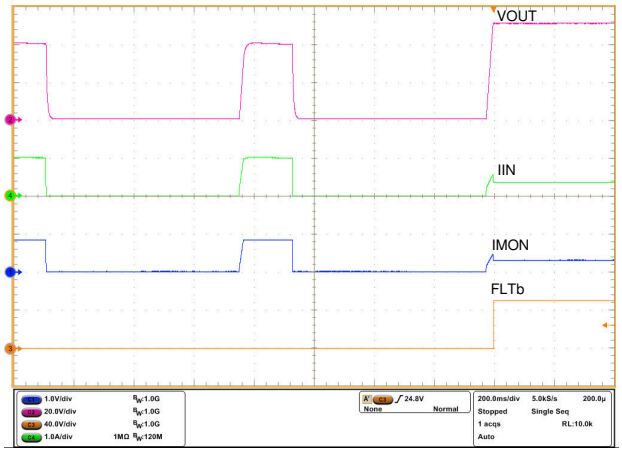
- $R_{(ILIM)}$ is the current limit resistor in kΩ

During the overload current limiting if the overload condition exists for more than $t_{CL\_PLIM\_FLT(dly)}$, 1.3msec (typical), the $\overline{FLT}$ asserts to warn of impending turnoff of the internal FETs due to the subsequent thermal shutdown event or due to $t_{CL\_PLIM(dly)}$ timer expiry. The $\overline{FLT}$ signal remains asserted until the fault condition is removed and the device resumes normal operation. Figure 8-6 and Figure 8-7 illustrate overload current limiting performance.



V_{IN} = 50V MODE = GND R_{ILIM} = 18kΩ

Figure 8-6. Overload Performance During Load Step from 140Ω to 40Ω



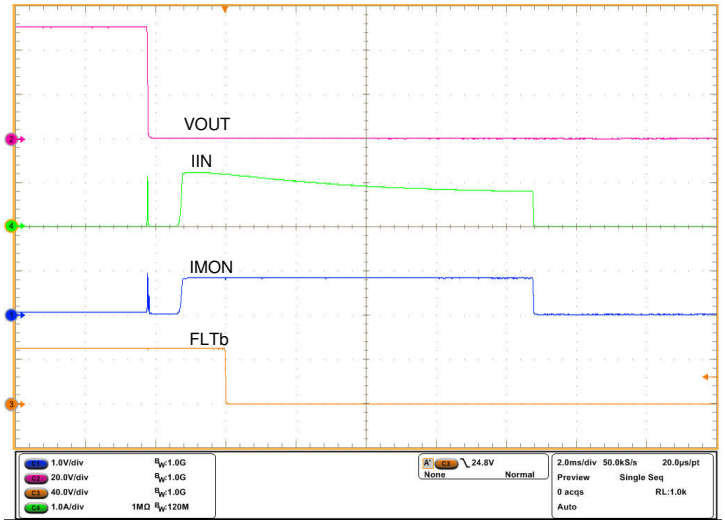
V_{IN} = 50V MODE = GND R_{ILIM} = 18kΩ

Figure 8-7. Coming Out of Overload With Load Step from 40 Ω to 140Ω

The TPS1663x devices features ILIM pin short and open fault detection and protection. The internal FET is turned OFF when ILIM pin is detected short or open to GND and it remains OFF until the ILIM pin fault is removed.

8.3.4.2 Short Circuit Protection

During a transient output short circuit event, the current through the device increases rapidly. As the current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator. The fast-trip comparator architecture is designed for fast turn OFF $t_{FASTTRIP(dly)}$ = 1µs (typical) with $I_{(SCP)}$ = 45A of the internal FET during an output short circuit event. The fast-trip threshold is internally set to $I_{(FASTTRIP)}$. The fast-trip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to $I_{(OL)}$. Then the device functions similar to the overload condition. Figure 8-8 illustrates output hot-short performance of the device.



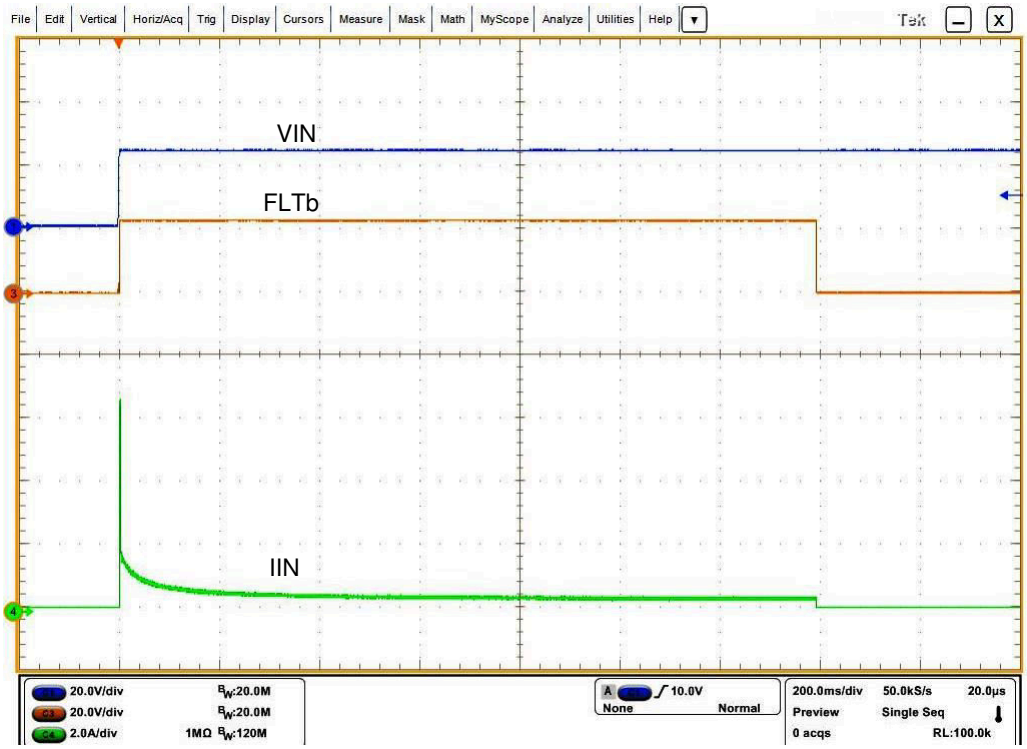
V_{IN} = 50V R_{ILIM} = 18kΩ

Figure 8-8. Output Hot-Short Response

The fast-trip comparator architecture has a supply line noise immunity resulting in a robust performance in noisy environments. This supply line noise immunity is achieved by controlling the turn OFF time of the internal FET based on the overcurrent level, $I_{(FASTTRIP)}$, through the device. The higher the overcurrent, the faster the turn OFF time, $t_{FASTTRIP(dly)}$. At Overload current level in the range of $I_{FASTTRIP} < I_{OUT} < I_{SCP}$, the fast-trip comparator response is 3.2µs (typical).

8.3.4.2.1 Start-Up With Short-Circuit On Output

When the device is started with short-circuit on the output, the current begins to limit at $I_{(OL)}$. Due to high power dissipation of VIN × $I_{(OL)}$ within the device the junction temperature increases. Subsequently, the thermal regulation control loop limits the load current to regulate the junction temperature at $T_{(J\_REG)}$, 145°C (typical) for a duration of $t_{(Treg\_timeout)}$, 1.25 sec (typical). Subsequent operation of the device depends on the MODE configuration (auto-retry or latch off) setting as per the Table 8-1. $\overline{FLT}$ gets asserted after $t_{(Treg\_timeout)}$ and remains asserted until the output short-circuit is removed. Figure 8-9 illustrates the behavior of the device in this condition.



V_{IN} = 24V R_{ILIM} = 3kΩ

Figure 8-9. Start-Up With Short on Output

8.3.5 Output Power Limiting, PLIM (TPS16632 and TPS16637)

In TPS16630, with a fixed overcurrent limit threshold the maximum output power limit increases linearly with supply input. Electrical Industrial process control equipment such as PLC CPU must comply with standards like IEC61010-1 and UL1310 for fire safety which require limited energy and power circuits. Limiting the output power becomes a challenge in such high power applications where the operating supply voltage range is wide. TPS16632 and TPS16637 integrate adjustable output power limiting functionality that simplifies the system design requiring compliance in accordance to this standard.

Connect a resistor from PLIM to GND as shown in Figure 8-10 to set the output power limiting value. If output power limiting is not required, then connect PLIM to GND directly. This connection disables the PLIM functionality.

During an over-power load event, the TPS16632 and TPS16637 limit the output power at the programmed value set by PLIM resistor. This limit indirectly results in the device operation in current limiting mode with steady state output voltage and current set by the load characteristics and:

$$P_{LIM} = V_{OUT} \times I_{OUT} \quad (7)$$

Figure 6-8 shows the output power limit and current limit characteristics of TPS16632 with 100W power limit setting. The maximum duration for the device in power limiting mode is 162msec (typical), $t_{CL\_PLIM(dly)}$. After this time, the device operates either in auto-retry or latch off mode based on MODE pin configuration in Table 8-1.

$$P_{(PLIM)} = 1 \times R_{(PLIM)} \quad (8)$$

Here, $P_{(PLIM)}$ is output power limit in watts, and $R_{(PLIM)}$ is the power limit setting resistor in kΩ.

During the output power limiting operation, $\overline{FLT}$ asserts after a delay of $t_{CL\_PLIM\_FLT(dly)}$. The $\overline{FLT}$ signal remains asserted until the over power load condition is removed and the device resumes normal operation.

Figure 8-11 illustrates output power limiting performance of TPS16632 with 100W setting for class-2 power supply designs.

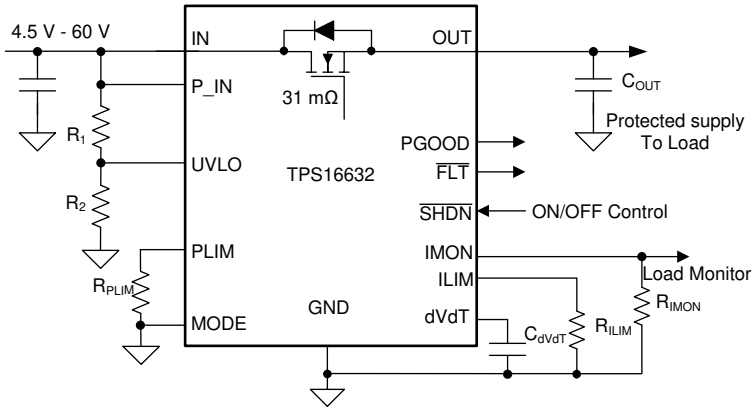
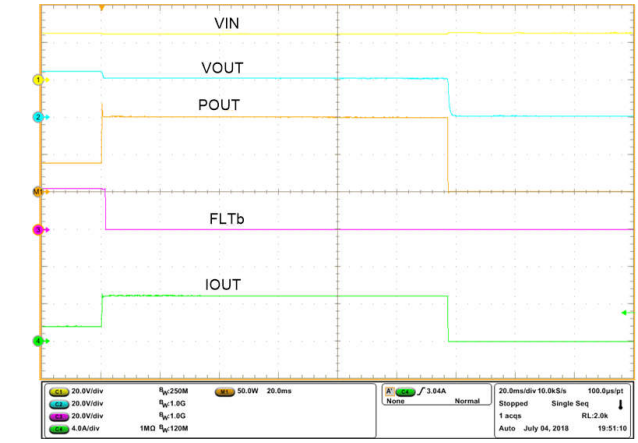


Figure 8-10. TPS16632 Typical Application Schematic



R_{PLIM} = 100kΩ R_{ILIM} = 3kΩ

Figure 8-11. 100W class 2, Output Power Limiting Response of TPS16632

8.3.6 Current Monitoring Output (IMON)

The TPS1663x devices feature an accurate analog current monitoring output. A current source at IMON terminal is internally configured to be proportional to the current flowing from IN to OUT. This current can be converted into a voltage using a resistor $R_{(IMON)}$ from IMON terminal to GND terminal. The IMON voltage can be used as a means of monitoring current flow through the system. The maximum voltage ($V_{(IMONmax)}$) for monitoring the current is limited to 4V. This limitation puts a limitation on maximum value of $R_{(IMON)}$ resistor and is determined by Equation 9.

$$V_{(IMON)} = \left[I_{(OUT)} \times GAIN_{(IMON)}\right] \times R_{(IMON)} \quad (9)$$

Where,

- $GAIN_{(IMON)}$ is the gain factor $I_{(IMON)}$:$I_{(OUT)}$ = 27.9µA/A (typical)
- $I_{(OUT)}$ is the load current

Refer to Figure 6-9 for IMON output versus load current plot. Figure 8-12 illustrates IMON performance.

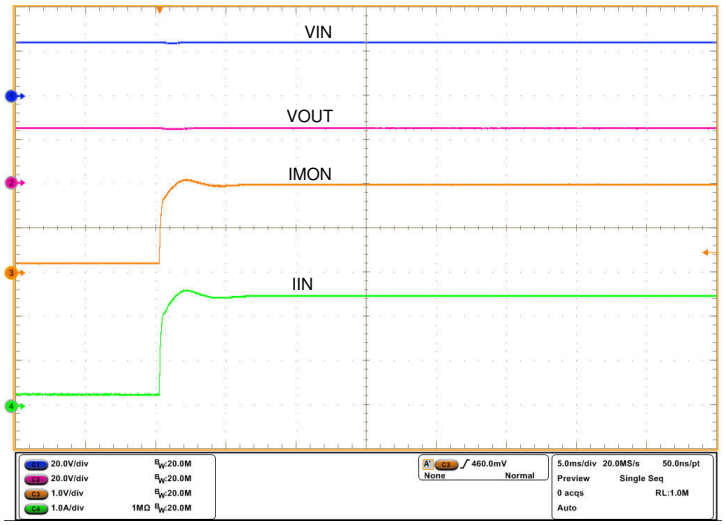


Figure 8-12. IMON Response During a Load Step

The IMON pin must not have a bypass capacitor to avoid delay in the current monitoring information.

8.3.7 FAULT Response ($\overline{FLT}$)

The $\overline{FLT}$ open-drain output asserts (active low) under the faults events such as undervoltage, overvoltage, overload, power limiting, ILIM pin short, and thermal shutdown conditions. The device is designed to eliminate false reporting by using an internal *de-glitch* circuit for fault conditions without the need for an external circuitry. $\overline{FLT}$ can be left open or connected to GND when not used.

8.3.8 Power Good Output (PGOOD)

The devices feature an open drain Power Good (PGOOD) indicator output. PGOOD can be used for enable-disable control of the downstream loads like DC/DC converters. PGOOD goes high when the internal FET's gate is enhanced. PGOOD goes low when the internal FET turns OFF during a fault event or when $\overline{SHDN}$ is pulled low. There is a deglitch of 11.5msec (typical), t_{PGOODR}, at the rising edge and 10msec (typical), t_{PGOODF}, on falling edge. PGOOD is a rated for 60V and can be pulled to IN or OUT through a resistor.

8.3.9 IN, P_IN, OUT and GND Pins

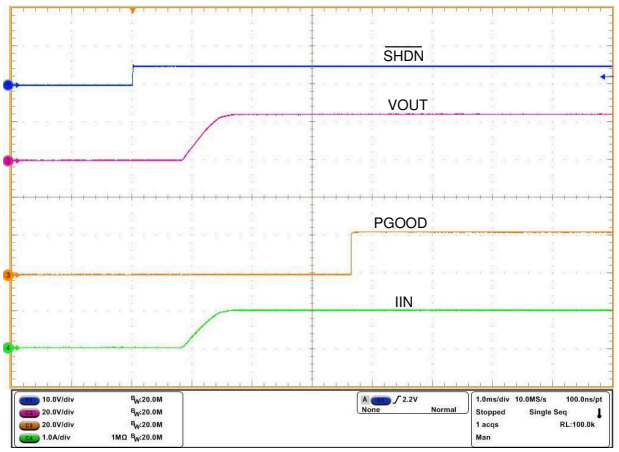
Connect a minimum of a 0.1-µF capacitor across IN and GND. Connect P_IN and IN together. Do not leave any of the IN and OUT pins un-connected.

8.3.10 Thermal Shutdown

The device has a built-in overtemperature shutdown circuitry designed to protect the internal FET if the junction temperature exceeds $T_{(TSD)}$, 165°C (typical). After the thermal shutdown event, depending upon the mode of fault response configured as shown in Table 8-1, the device either latches off or commences an auto-retry cycle of 648msec (typical), $t_{(TSD\_retry)}$ after $T_J < (_{(TSD)} - 11°C)$. During the thermal shutdown, the fault pin $\overline{FLT}$ pulls low to indicate a fault condition.

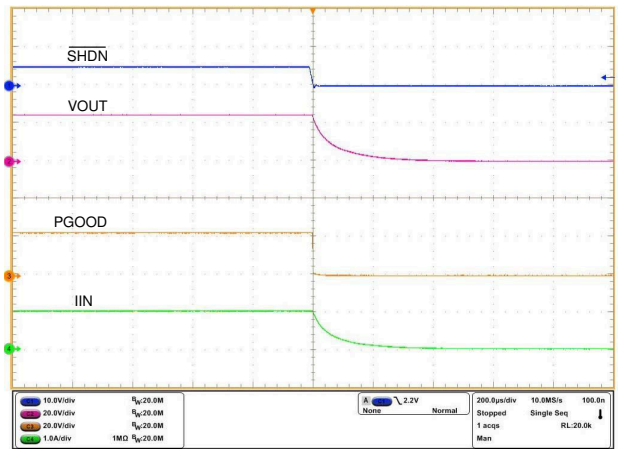
8.3.11 Low Current Shutdown Control ($\overline{SHDN}$)

The internal and the external FET and hence the load current can be switched off by pulling the $\overline{SHDN}$ pin below 0.8V threshold with a micro-controller GPIO pin or can be controlled remotely with an opto-isolator device. The device quiescent current reduces to 21µA (typical) in shutdown state. To assert $\overline{SHDN}$ low, the pull down must have sinking capability of at least 10 µA. To enable the device, $\overline{SHDN}$ must be pulled up to at least 2V. Once the device is enabled, the internal FET turns on with dVdT mode.Figure 8-13 and Figure 8-14 illustrate the performance of $\overline{SHDN}$ control.



V_{IN} = 24 V $C_{(dVdT)}$ = 22 nF R_{LOAD} = 24 Ω

Figure 8-13. Turnon Control With $\overline{SHDN}$



V_{IN} = 24 V $C_{(dVdT)}$ = 22 nF R_{LOAD} = 24 Ω

Figure 8-14. Turnoff Control With $\overline{SHDN}$

8.4 Device Functional Modes

The TPS1663x devices respond differently to overload with MODE pin configurations. Table 8-1 lists the operational differences.

Table 8-1. Device Operational Differences Under Different MODE Configurations

MODE Pin Configuration	Power Limiting, Over Current fault and Thermal Shutdown Operation
Open	Active Current limiting for a maximum duration of $t_{CL\_PLIM(dly)}$. There after Latches OFF. Latch reset by toggling $\overline{SHDN}$ or UVLO low to high or power cycling IN.
Shorted to GND	Active current limiting for a maximum duration of $t_{CL\_PLIM(dly)}$. There after auto-retries after a delay of $t_{(TSD\_retry)}$.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS1663x is a 60V eFuse, typically used for hot-swap and power rail protection applications. The device operates from 4.5V to 60V with programmable current limit, overvoltage, and undervoltage protections. The device aids in controlling in-rush current and provides output power limiting for systems such as PLCs, Telecom radios, and industrial printers. The device also provides robust protection for multiple faults on the system rail.

The *Detailed Design Procedure* section can be used to select component values for the device. Additionally, a spreadsheet design tool, *TPS1663 Design Calculator*, is available in the web product folder.

9.2 Typical Application

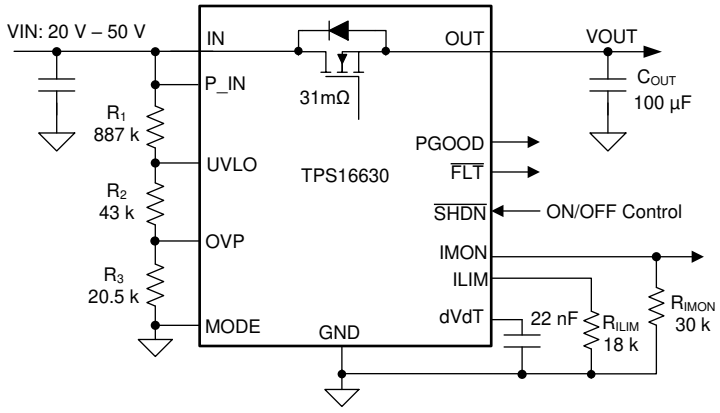


Figure 9-1. 20V –50V, 1A eFuse Protection Circuit for Telecom Radios

9.2.1 Design Requirements

Table 9-1 shows the design requirements for TPS16630.

Table 9-1. Design Requirements

DESIGN PARAMETER		EXAMPLE VALUE
$V_{(IN)}$	Input voltage range	20V–50V
$V_{(UV)}$	Undervoltage lockout set point	18V
$V_{(OV)}$	Overvoltage cutoff set point	55V
$I_{(LIM)}$	Overload current limit	1A
C_{OUT}	Output capacitor	100 µF
$I_{(INRUSH)}$	Inrush current limit	300mA

9.2.2 Detailed Design Procedure

9.2.2.1 Programming the Current-Limit Threshold $R_{(ILIM)}$ Selection

The $R_{(ILIM)}$ resistor at the ILIM pin sets the overload current limit. The overload current limit can be set using Equation 10.

$$R_{(ILIM)} = \frac{18}{I_{OL}} = 18k\Omega \quad (10)$$

where

- I_{LIM} = 1A

Select the closest standard 1% resistor value: $R_{(ILIM)}$ = 18kΩ

9.2.2.2 Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using an external voltage divider network of R_1, R_2 and R_3 connected between IN, UVLO, OVP and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving Equation 11 and Equation 12.

$$V_{(OVPR)} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{(OV)} \quad (11)$$

$$V_{(UVLOR)} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{(UV)} \quad (12)$$

For minimizing the input current drawn from the power supply:

$$\left[I_{(R123)} = \frac{V_{(IN)}}{R_1 + R_2 + R_3}\right] \quad (13)$$

TI recommends to use higher value resistance for R_1, R_2 and R_3.

However, the leakage current due to external active components connected at resistor string can add error to these calculations. So, the resistor string current, $I(R_{123})$, must be chosen to be 20 times greater than the leakage current of UVLO and OVP pins.

From the device electrical specifications, $V_{(OVPR)}$ = 1.2V and $V_{(UVLOR)}$ = 1.2V. From the design requirements, $V_{(OV)}$ is 55V and $V_{(UV)}$ is 18V. To solve the equation, first select the value of R_3 = 20.5kΩ and use Equation 11 to solve for (R_1 + R_2) = 930kΩ. Use Equation 12 and value of (R_1 + R_2) to solve for R_2 = 43kΩ and finally R_1 = 887kΩ.

select the closest standard 1% resistor values: R_1 = 887kΩ, R_2 = 43kΩ, and R_3 = 20.5kΩ.

9.2.2.3 Setting Output Voltage Ramp Time (t_{dVdT})

Use Equation 1 and Equation 2 to calculate required $C_{(dVdT)}$ for achieving an inrush current of 300 mA. $C_{(dVdT)}$ = 22nF. Figure 9-2 and Figure 9-3 illustrate the inrush current limiting performance during 50V hot-plug in condition.

9.2.2.3.1 Support Component Selections R_{PGOOD} and $C_{(IN)}$

The R_{PGOOD} serves as pull-up for the open-drain output. The current sink by this pin must not exceed 10mA (see the Absolute Maximum Ratings table). TI recommends typical resistance value in the range from 10kΩ to 100kΩ for R_{PGOOD}. Figure 9-5 and Figure 9-7 illustrate the power up and power down performance of the system respectively. The C_{IN} is a local bypass capacitor to suppress noise at the input. TI recommends a minimum of 0.1µF for $C_{(IN)}$.

9.2.3 Application Curves

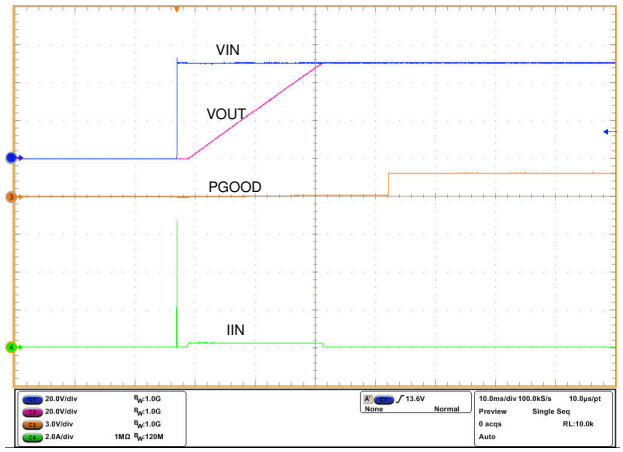


Figure 9-2. Hot-Plug In at 50V Supply With No Load

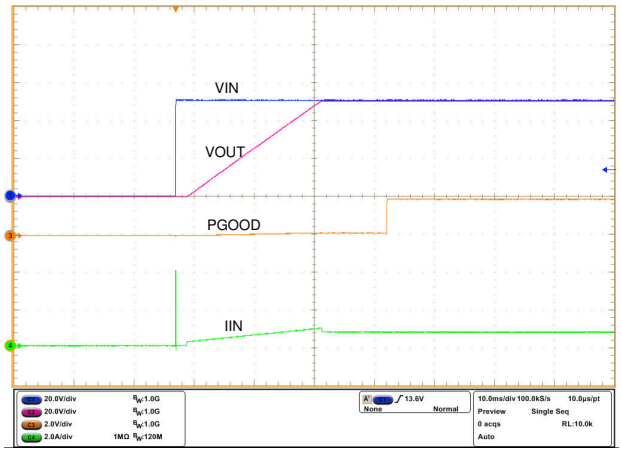


Figure 9-3. Hot-Plug In at 50V Supply With 60Ω Load

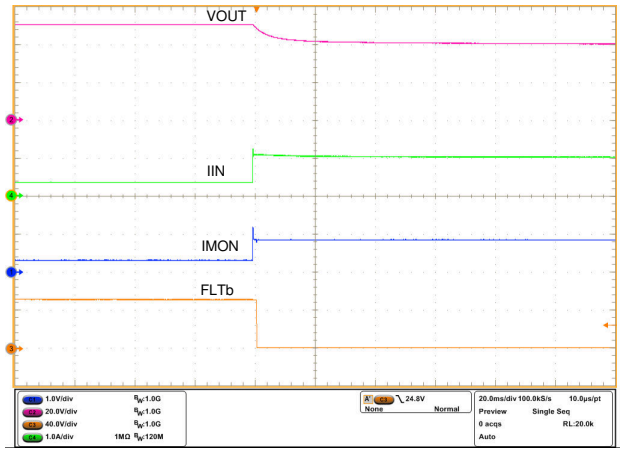


Figure 9-4. Overload Performance During Load Step From 140Ω to 40Ω

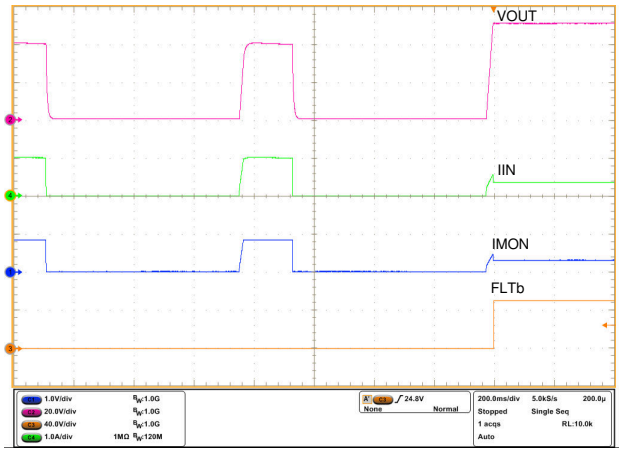


Figure 9-5. Coming Out of Overload With Load Step From 40Ω to 140Ω

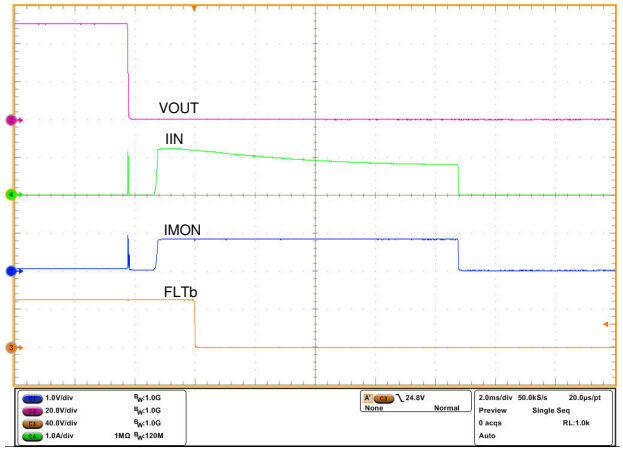


Figure 9-6. Output Hot-short Performance With 50V Input Supply

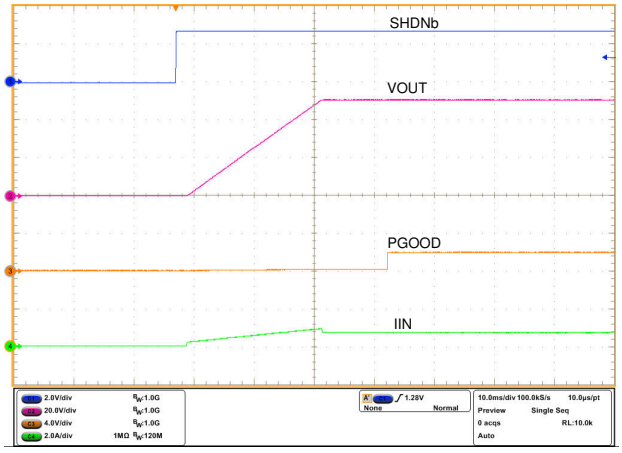


Figure 9-7. Turn ON Using $\overline{\text{SHDN}}$ Control

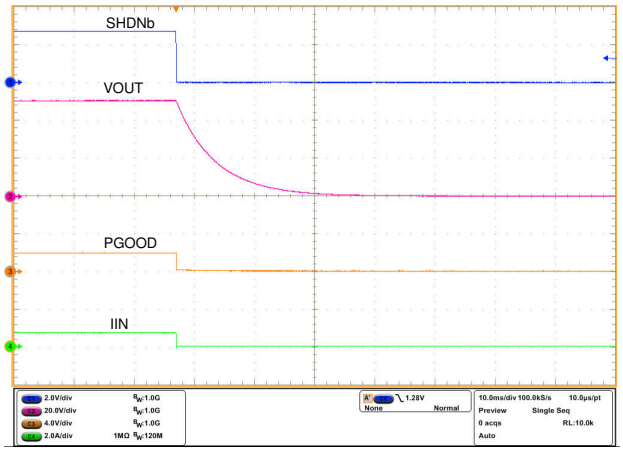


Figure 9-8. Turn OFF Using $\overline{\text{SHDN}}$ Control

9.3 System Examples

9.3.1 Simple 24V Power Supply Path Protection

With the TPS1663x, a simple 24V power supply path protection can be realized using a minimum of three external components, as shown in the schematic diagram in Figure 9-9. The external components required are a $R_{(ILIM)}$ resistor to program the current limit and $C_{(IN)}$ and $C_{(OUT)}$ capacitors.

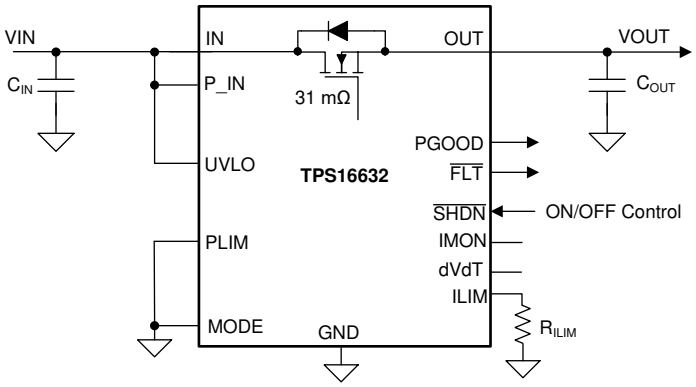


Figure 9-9. TPS16630 Configured for a Simple Power Supply Path Protection

Protection features with this configuration include:

- 39V (maximum) overvoltage clamp output
- Inrush current control with 24V/500µs output voltage slew rate
- Accurate current limiting with auto-retry

9.4 Power Supply Recommendations

The TPS1663x eFuse is designed for the supply voltage range of 4.5V ≤ V_{IN} ≤ 60V. If the input supply is located more than a few inches from the device, TI recommends an input ceramic bypass capacitor higher than 0.1µF. Power supply must be rated higher than the current limit set to avoid voltage droops during overcurrent and short circuit conditions.

9.4.1 Transient Protection

In case of short circuit and overload current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the

input or output of the device. These transients can exceed Absolute Maximum Ratings of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Using a Schottky diode across the output and GND to absorb negative spikes
- Using low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1µF) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with Equation 14.

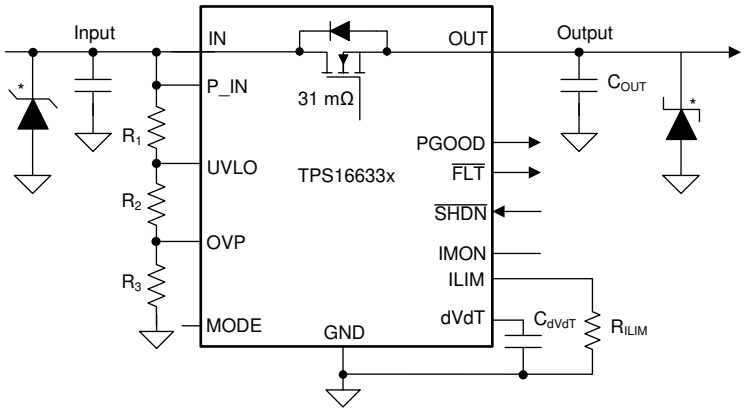
$$V_{spike(Absolute)} = V_{IN} + I_{(LOAD)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (14)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications can require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding Absolute Maximum Ratings of the device. These transients can occur during positive and negative surge tests on the supply lines. In such applications, TI recommends to place at least 1µF of input capacitor.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and Schottky diode) is shown in Figure 9-10.



* Optional components needed for suppression of transients

Figure 9-10. Circuit Implementation With Optional Protection Components for TPS1663x

9.5 Layout

9.5.1 Layout Guidelines

- For all the applications, TI recommends a 0.1 µF or higher value ceramic decoupling capacitor between IN terminal and GND.
- High current carrying power path connections must be as short as possible and must be sized to carry at least twice the full-load current. See Figure 9-11 and Figure 9-12 for a typical PCB layout example.
- Locate all the TPS1663x family support components $R_{(ILIM)}$, $R_{(PLIM)}$, $C_{(dVdT)}$, $R_{(IMON)}$, UVLO, OVP resistors close to their connection pin. Connect the other end of the component to the GND with shortest trace length.

- The trace routing for the $R_{(ILIM)}$, $R_{(PLIM)}$ component to the device must be as short as possible to reduce parasitic effects on the current limit and power limit accuracy. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads, and it must be physically close to the OUT and GND pins.
- Thermal Considerations: when properly mounted, the PowerPAD package provides significantly greater cooling ability. To operate at rated power, the PowerPAD must be soldered directly to the board GND plane directly under the device. Other planes, such as the bottom side of the circuit board, can be used to increase heat sinking in higher current applications.

9.5.2 Layout Example

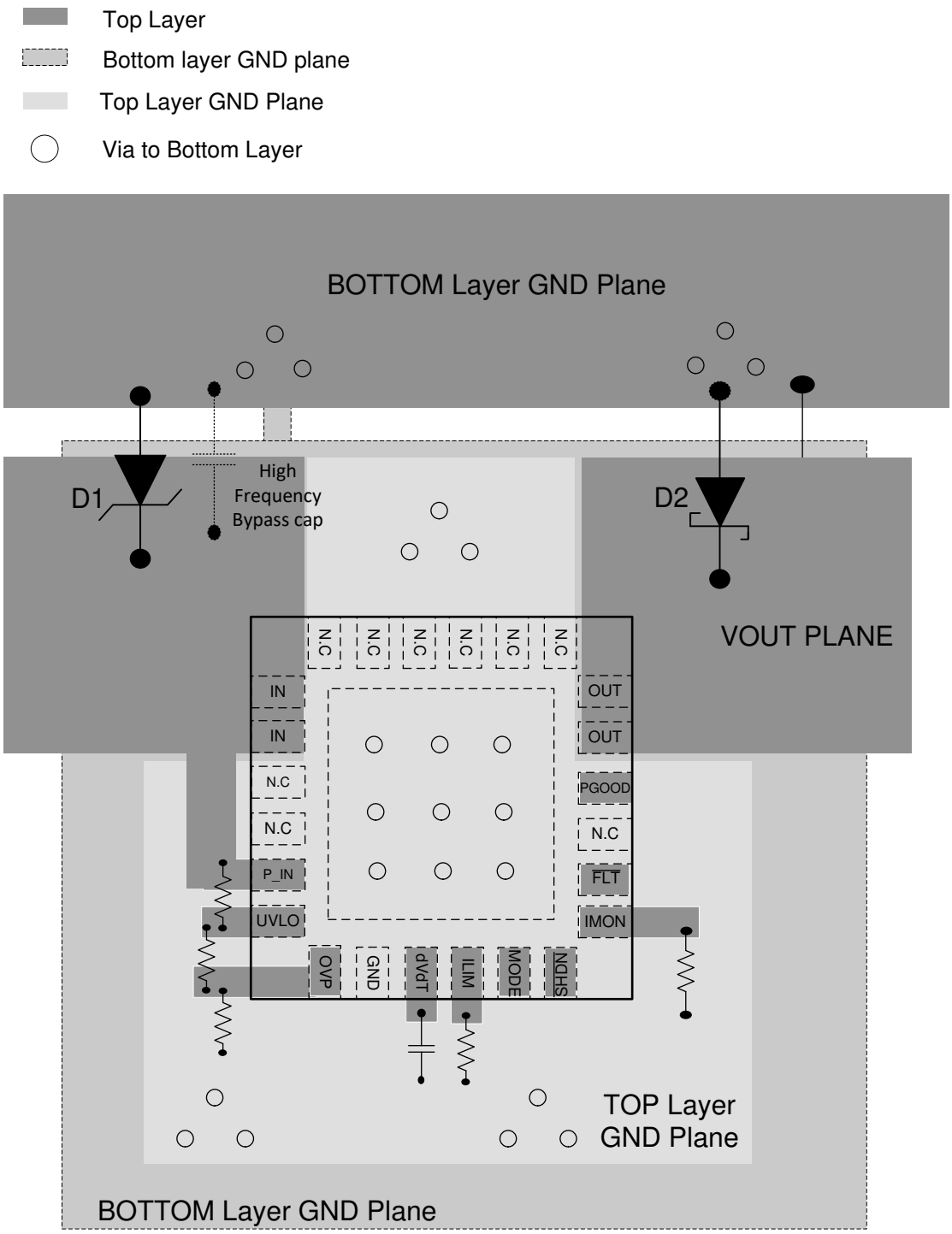


Figure 9-11. PCB Layout Example With QFN Package With a 2-Layer PCB

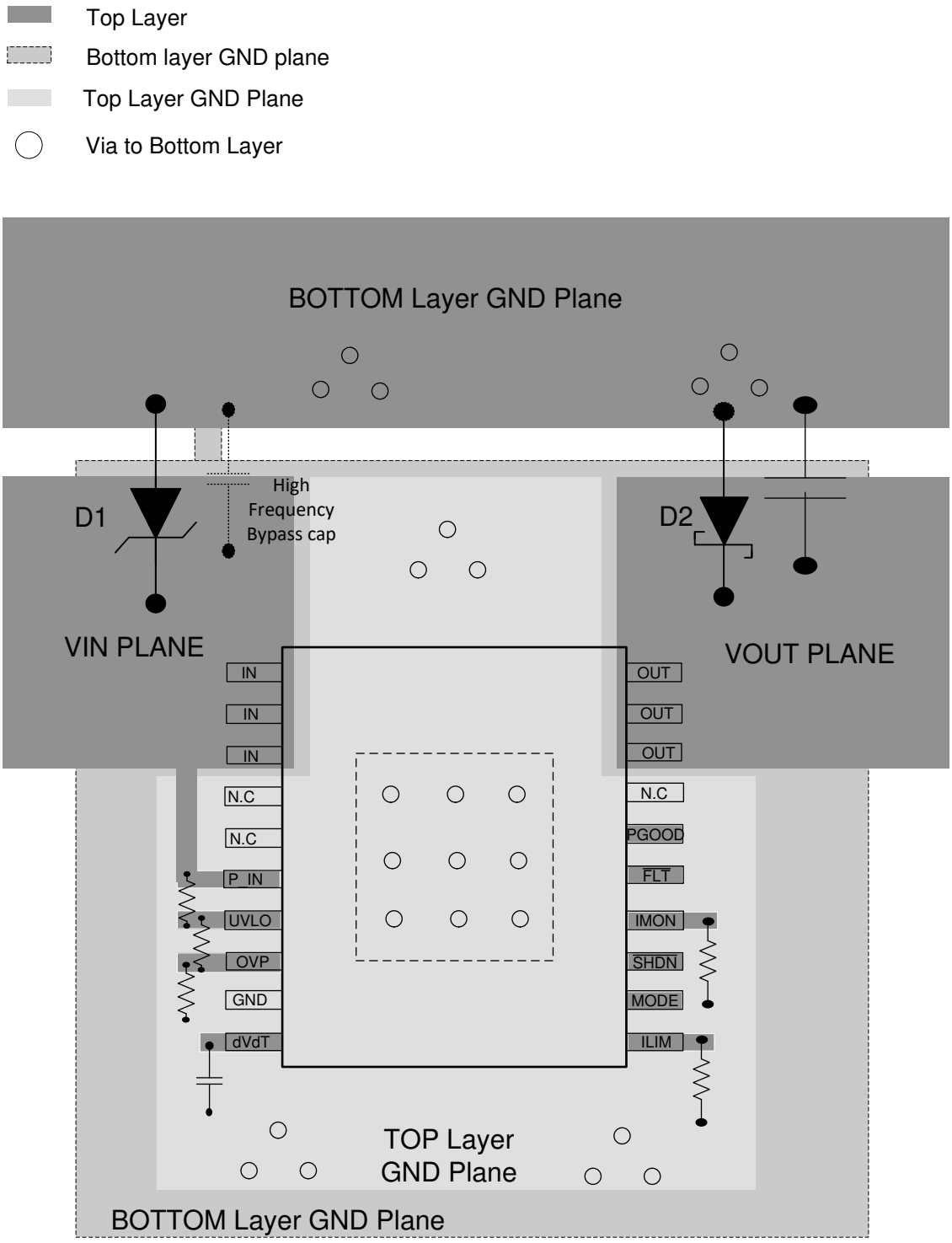


Figure 9-12. Typical PCB Layout Example With HTSSOP Package With a 2-Layer PCB

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- *TPS1663 Design Calculator*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (February 2023) to Revision G (April 2026)	Page
• Added TPS16637 device variant	1
• Added TPS16637 device variant	4
• Added TPS16637 device variant	5

Changes from Revision E (March 2020) to Revision F (February 2023)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	1
• Added Functional Safety-Capable bullet to the *Features* section	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS16630PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS16630
TPS16630PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS16630
TPS16630PWPT	Active	Production	HTSSOP (PWP) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS16630
TPS16630PWPT.A	Active	Production	HTSSOP (PWP) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS16630
TPS16630RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 16630
TPS16630RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 16630
TPS16630RGERG4	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 16630
TPS16630RGERG4.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 16630
TPS16630RGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 16630
TPS16630RGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 16630
TPS16632RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 16632
TPS16632RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 16632
TPS16632RGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 16632
TPS16632RGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 16632
TPS16637PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS16637
TPS16637PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS16637
TPS16637RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 16637
TPS16637RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS 16637

(1) **Status:** For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

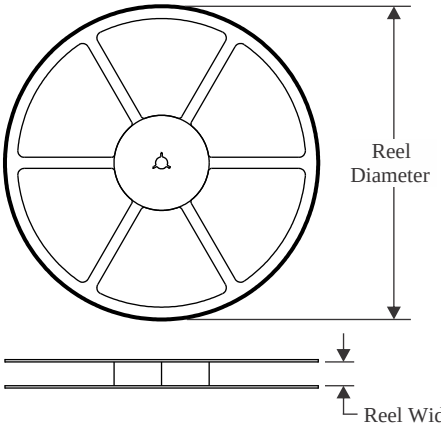
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

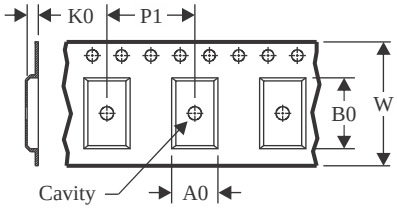
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

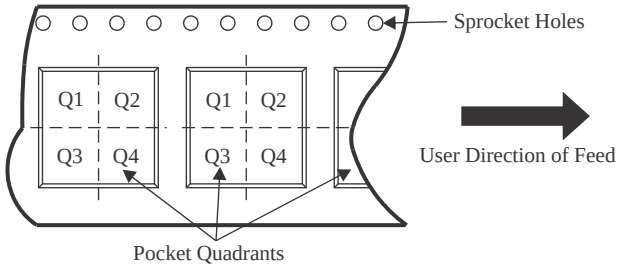


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

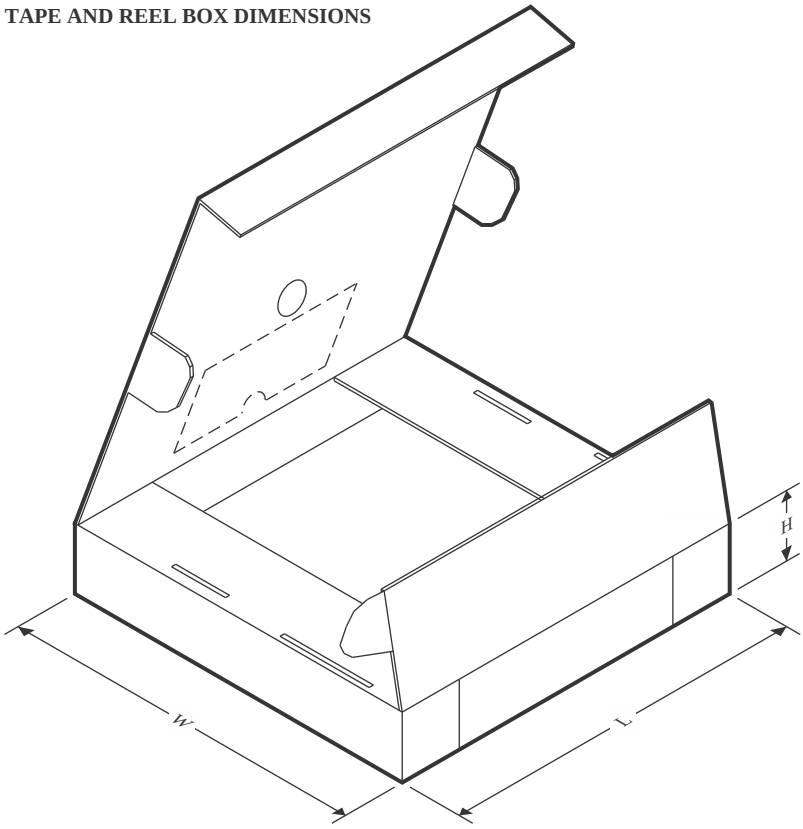
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS16630PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TPS16630PWPT	HTSSOP	PWP	20	250	180.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TPS16630RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS16630RGERG4	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS16630RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS16632RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS16632RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS16637PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TPS16637RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS16630PWPR	HTSSOP	PWP	20	2000	353.0	353.0	32.0
TPS16630PWPT	HTSSOP	PWP	20	250	213.0	191.0	35.0
TPS16630RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS16630RGERG4	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS16630RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS16632RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS16632RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS16637PWPR	HTSSOP	PWP	20	2000	353.0	353.0	32.0
TPS16637RGER	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

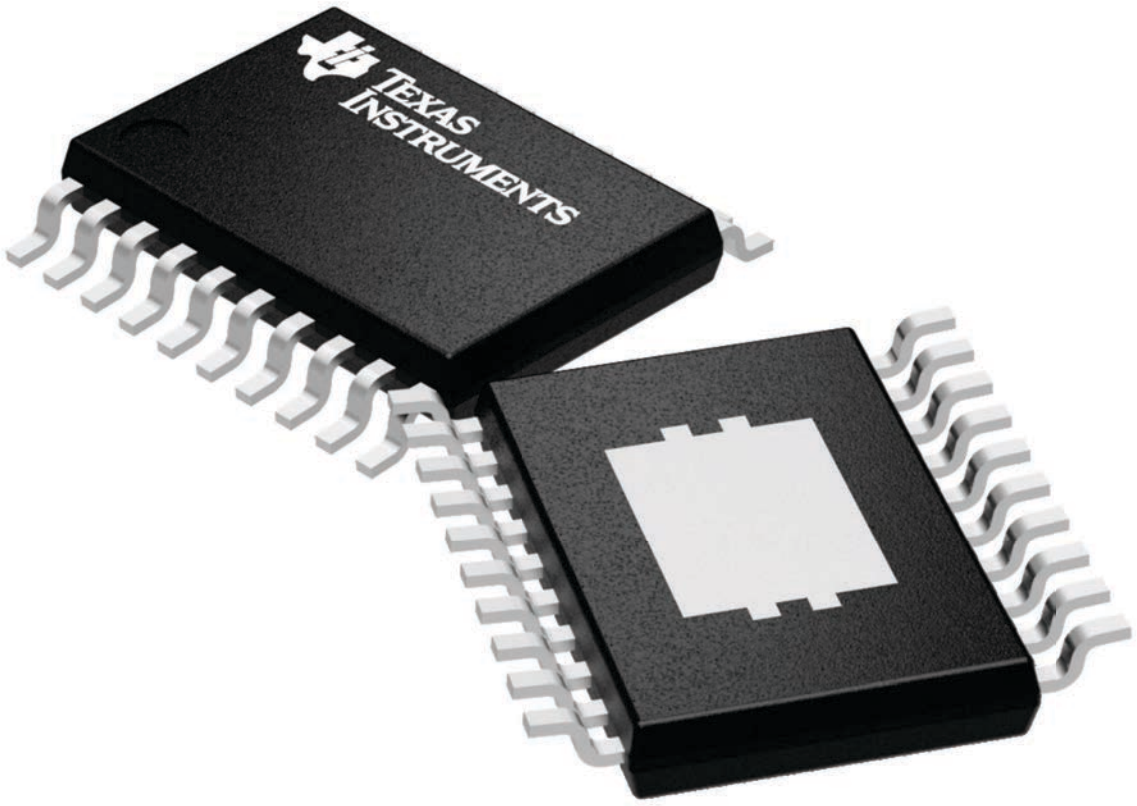
PWP 20

HTSSOP - 1.2 mm max height

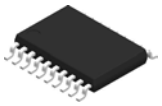
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

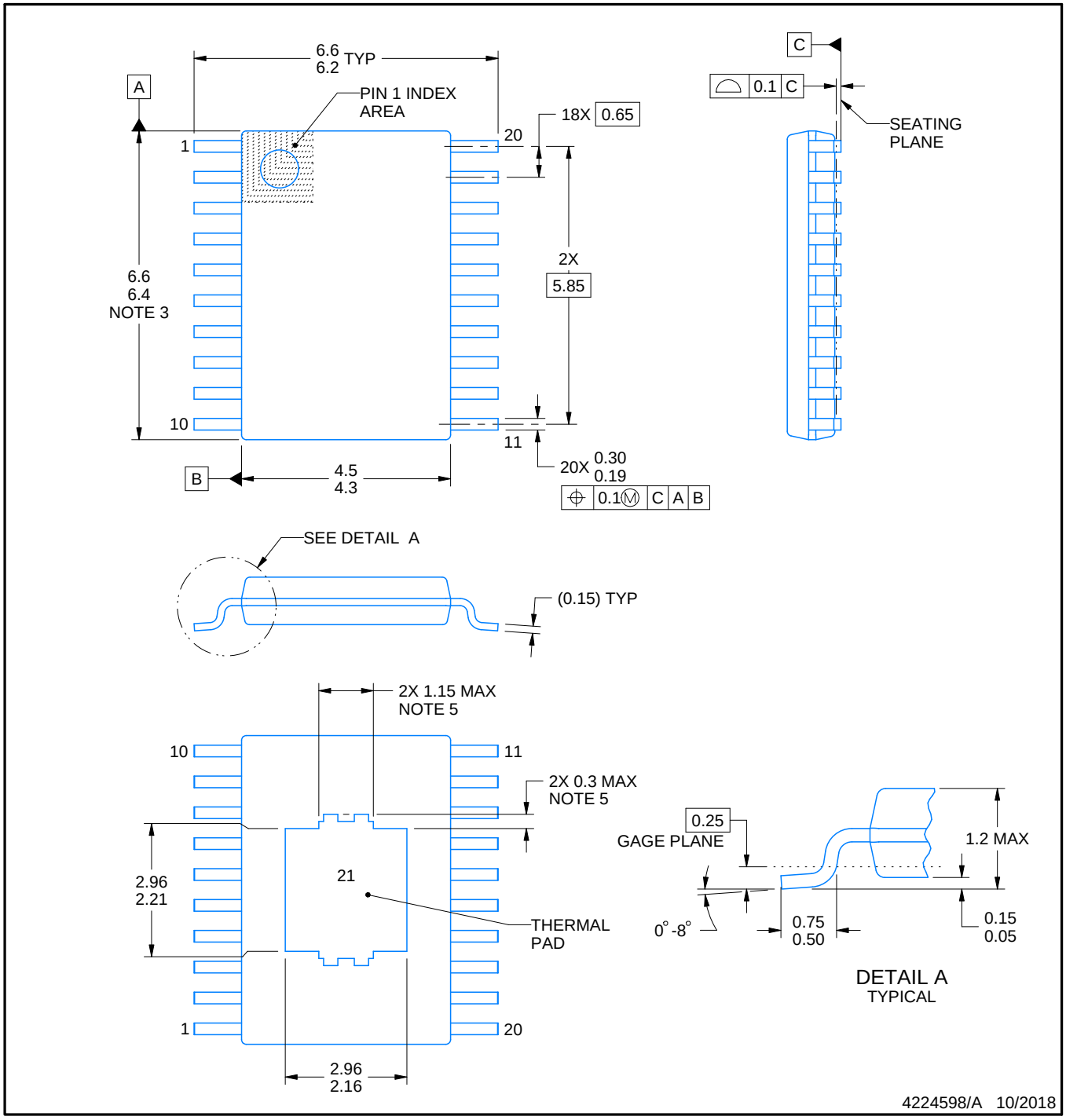


PACKAGE OUTLINE

PWP0020T

PowerPAD™ TSSOP - 1.2 mm max height

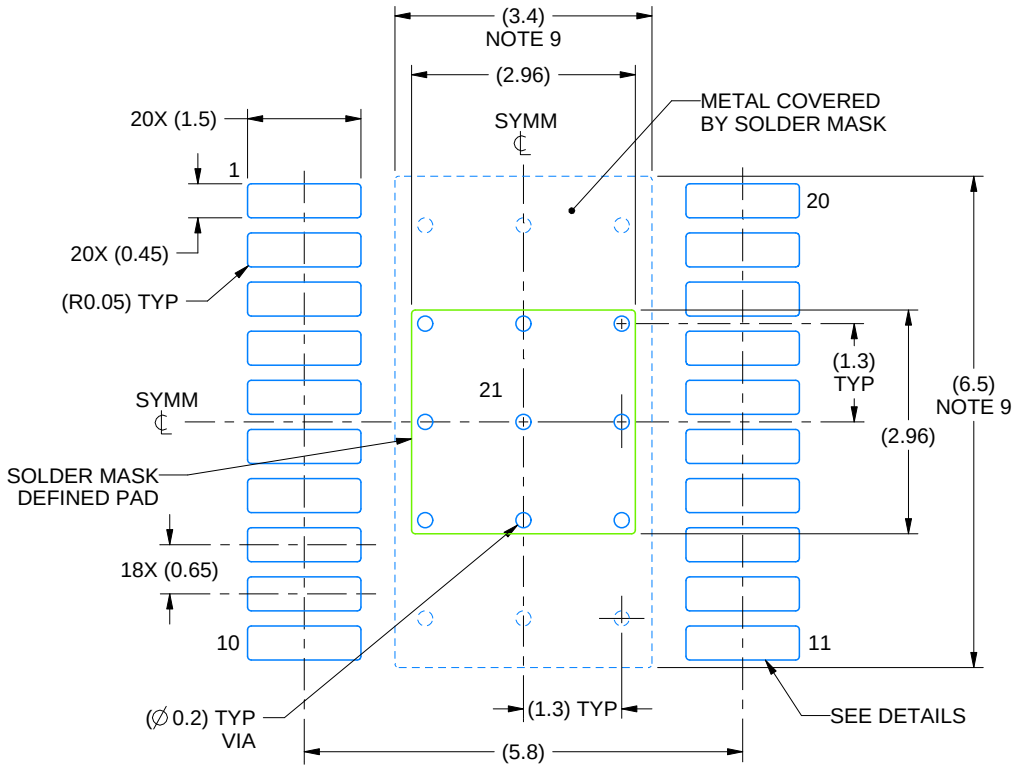
SMALL OUTLINE PACKAGE



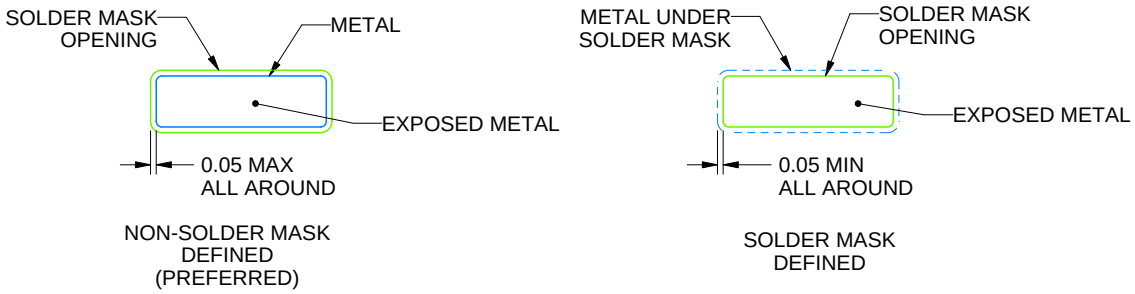
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

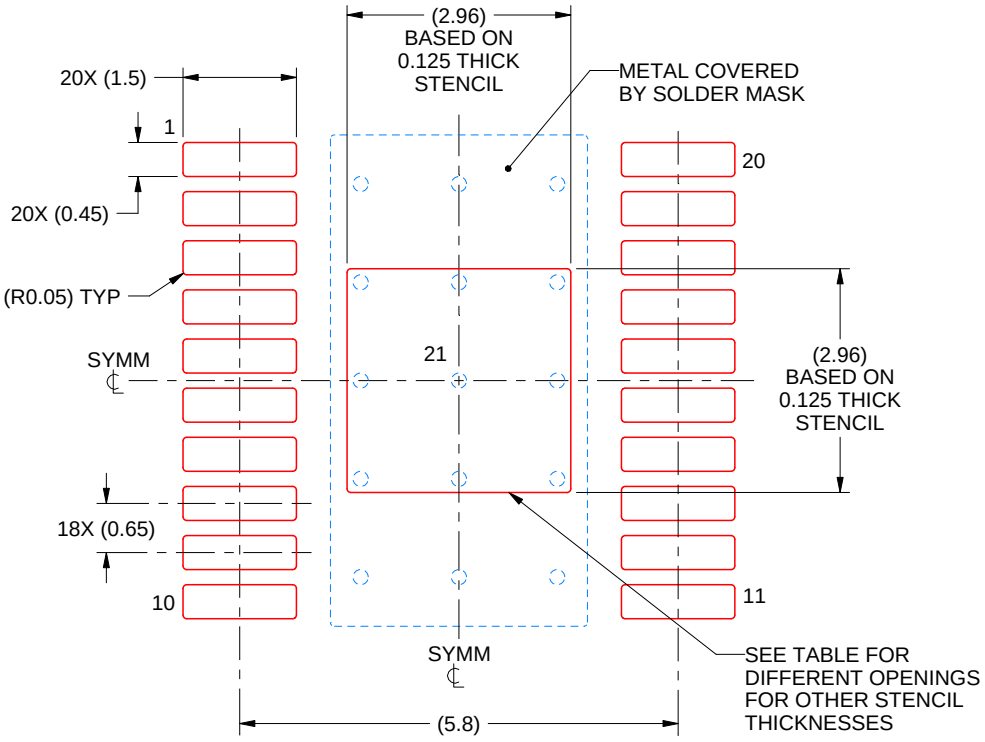


SOLDER MASK DETAILS

4224598/A 10/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.31 X 3.31
0.125	2.96 X 2.96 (SHOWN)
0.15	2.70 X 2.70
0.175	2.50 X 2.50

4224598/A 10/2018

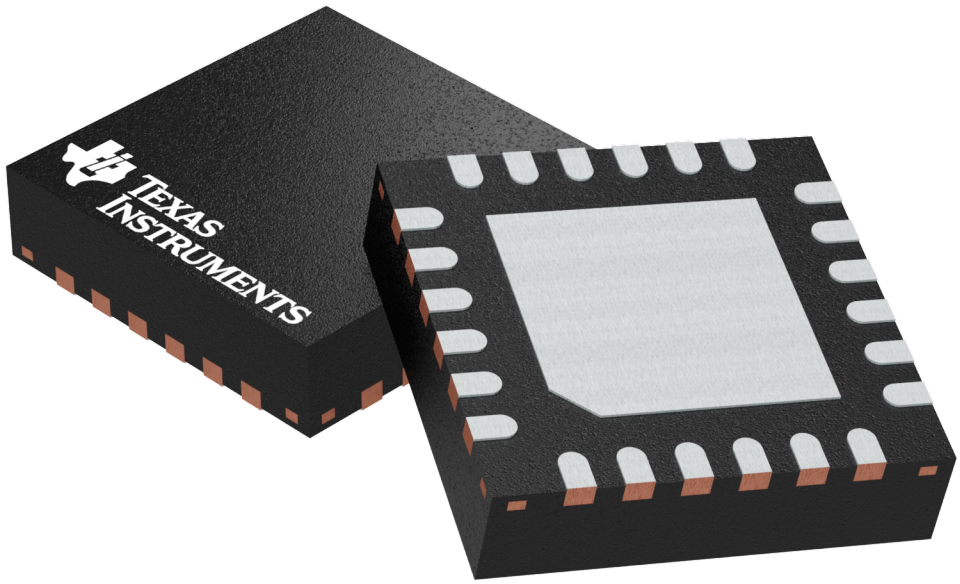
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

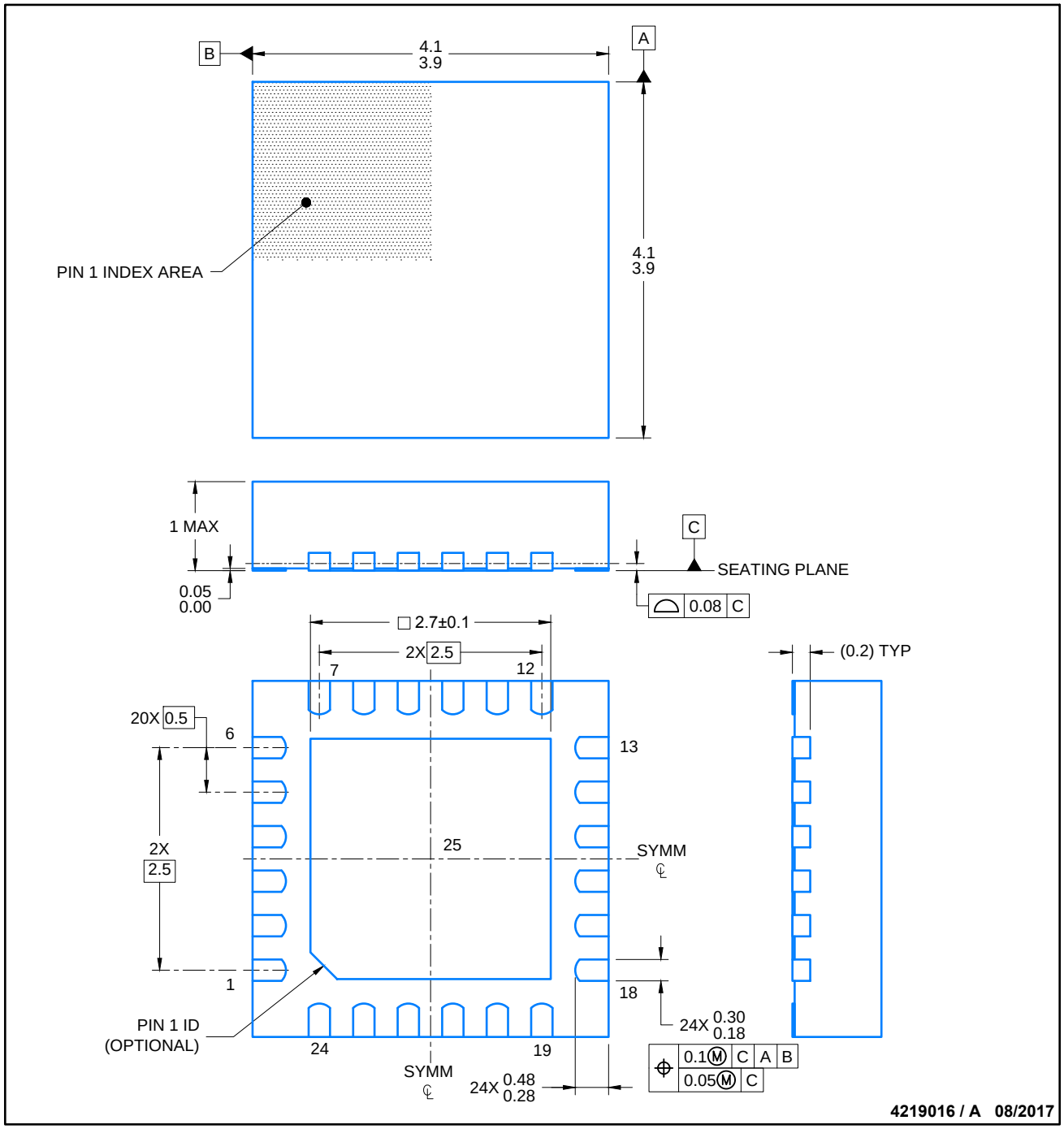
4204104/H

PACKAGE OUTLINE

RGE0024H

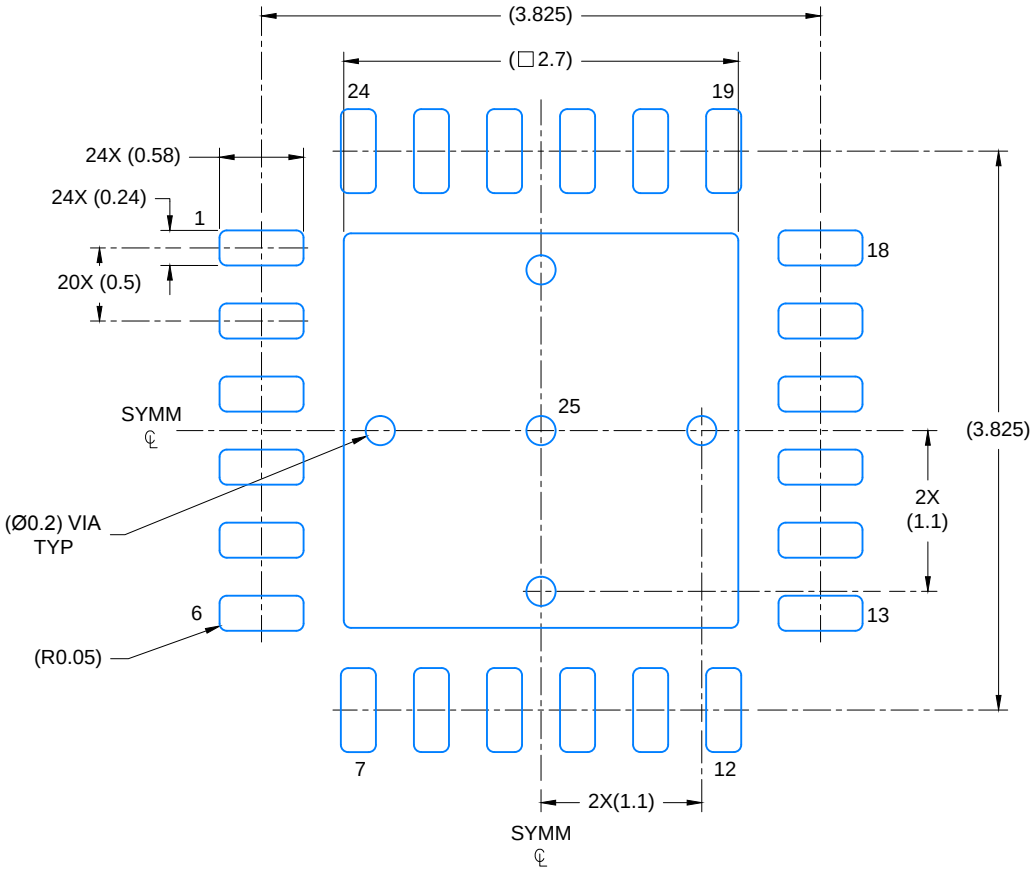
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



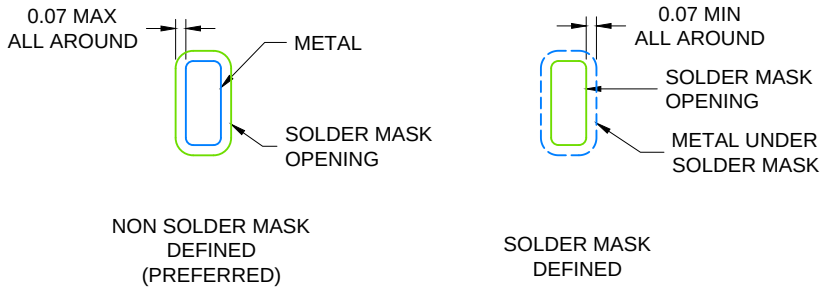
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

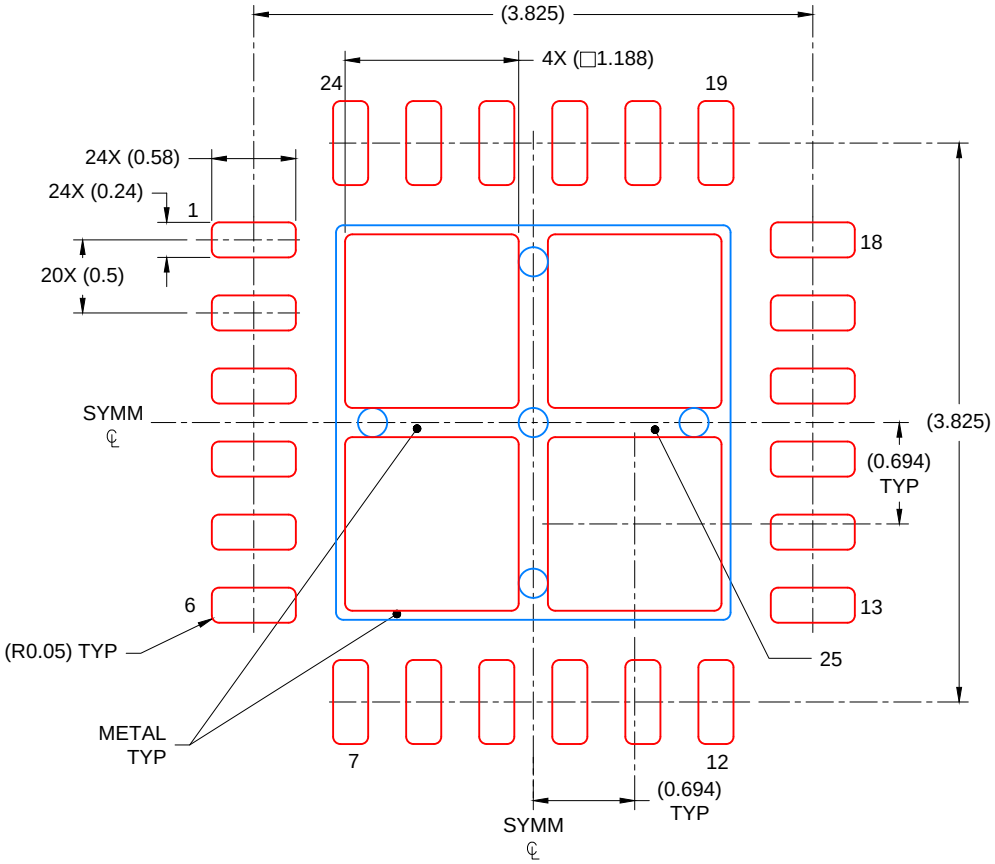


SOLDER MASK DETAILS

4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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