TPS20xxC and TPS20xxC-2 Current Limited, Power-Distribution Switches

1 Features

- Single Power Switch Family
- Pin-for-Pin With Existing TI Switch Portfolio
- Rated Currents of 0.5A, 1A, 1.5A, 2A
- ±20% Accurate, Fixed, Constant Current Limit
- Fast Overcurrent Response: 2µs
- Deglitched Fault Reporting
- Selected Parts With (TPS20xxC) and Without (TPS20xxC-2) Output Discharge
- Reverse Current Blocking
- Built-In Soft Start
- Ambient Temperature Range: –40°C to 85°C
- UL Listed and CB-File No. E169910

2 Applications

- USB Ports and Hubs, Laptops, and Desktops
- High-Definition Digital TVs
- Set-Top Boxes
- Short-Circuit Protection

3 Description

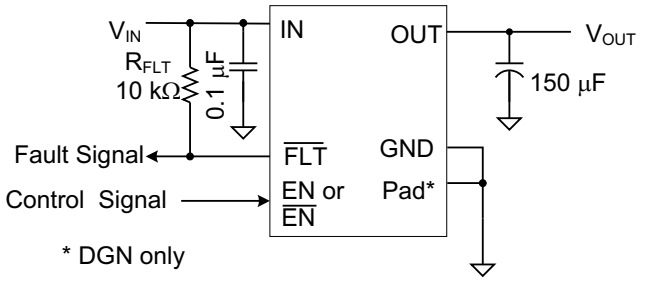
The TPS20xxC and TPS20xxC-2 power-distribution switch family is intended for applications, such as USB, where heavy capacitive loads and short circuits are likely to be encountered. This family offers multiple devices with fixed current-limit thresholds for applications from 0.5A to 2A.

The TPS20xxC and TPS20xxC-2 family limits the output current to a safe level by operating in a constant-current mode when the output load exceeds the current limit threshold. This provides a predictable fault current under all conditions. The fast overload response time eases the burden on the main 5V supply to provide regulated power when the output is shorted. The power-switch rise and fall times are controlled to minimize current surges during turnon and turnoff.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS20xxC, TPS20xxC-2	SOT-23 (5)	2.90mm × 1.60mm
	VSSOP (8)	3.00mm × 3.00mm
	MSOP-PowerPAD (8)	3.00mm × 3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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Typical Application Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Device Comparison Table

MAXIMUM OPERATING CURRENT	OUTPUT DISCHARGE	ENABLE	BASE PART NUMBER	PACKAGED DEVICE AND MARKING(1)		
				MSOP-8 (DGN) PowerPAD™	SOT23-5 (DBV)	VSSOP-8 (DGK)
0.5	Y	Low	TPS2041C	—(2)	PYJI	—
0.5	Y	High	TPS2051C	—	VBYQ	—
1	Y	Low	TPS2061C	PXMI	PXLI	—
1	Y	High	TPS2065C	VCAQ	VCAQ	—
1	N	High	TPS2065C-2	PYRI	PYQI	—
1.5	Y	Low	TPS2068C	PXNI	—	—
1.5	Y	High	TPS2069C	VBUQ	PYKI	—
1.5	N	High	TPS2069C-2	PYSI	—	—
2	Y	Low	TPS2000C	BCMS	—	PXFI
2	Y	High	TPS2001C	VBWQ	–	PXGI

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) "–" indicates the device is not available in this package.

5 Pin Configuration and Functions

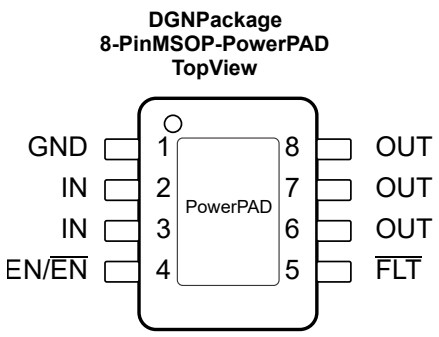


Figure 5-1. DGN Package 8-Pin MSOP-PowerPAD Top View

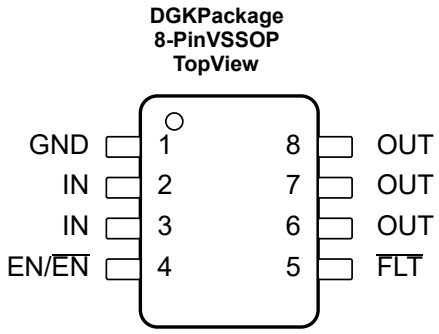


Figure 5-2. DGK Package 8-Pin VSSOP Top View

Table 5-1. Pin Functions - 8 Pins

PIN		I/O	DESCRIPTION
NAME	NO.		
EN/ $\overline{EN}$	4	I	Enable input, logic high turns on power switch
$\overline{FLT}$	5	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions
GND	1	—	Ground connection
IN	2, 3	PWR	Input voltage and power-switch drain; connect a 0.1-µF or greater ceramic capacitor from IN to GND close to the IC
OUT	6, 7, 8	PWR	Power-switch output, connect to load
PowerPAD (DGN Only)	PowerPAD	—	Internally connected to GND. Connect PAD to GND plane as a heatsink for the best thermal performance. PAD may be left floating if desired. See *Power Dissipation and Junction Temperature* for guidance.

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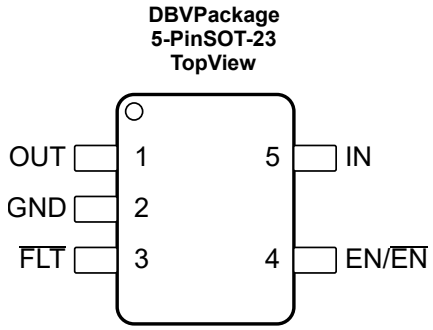


Figure 5-3. DBV Package 5-Pin SOT-23 Top View

Table 5-2. Pin Functions - 5 Pins

PIN		I/O	DESCRIPTION
NAME	NO.		
EN/ $\overline{EN}$	4	I	Enable input, logic high turns on power switch
$\overline{FLT}$	3	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions
GND	2	—	Ground connection
IN	5	PWR	Input voltage and power-switch drain; connect a 0.1-µF or greater ceramic capacitor from IN to GND close to the IC
OUT	1	PWR	Power-switch output, connect to load.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

	MIN	MAX	UNIT
Voltage on IN, OUT, EN or $\overline{EN}$, $\overline{FLT}$ (4)	–0.3	6	V
Voltage from IN to OUT	–6	6	V
Maximum junction temperature, T_J	Internally Limited		
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute maximum ratings apply over recommended junction temperature range.
(3) Voltages are with respect to GND unless otherwise noted.
(4) See *Input and Output Capacitance*.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		IEC 61000-4-2 contact discharge	±8000	
		IEC 61000-4-2 air-gap discharge(3)	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) V_{OUT} was surged on a PCB with input and output bypassing per the *Typical Application Diagram* on the first page (except input capacitor was 22 µF) with no device failures.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, IN		4.5		5.5	V
V_{EN}	Input voltage, EN or $\overline{EN}$		0		5.5	V
V_{IH}	High-level input voltage, EN or $\overline{EN}$		2			V
V_{IL}	Low-level input voltage, EN or $\overline{EN}$				0.7	V
I_{OUT}	Continuous output current, OUT(1)	TPS2041C and TPS2051C			0.5	A
		TPS2061C, TPS2065C and TPS2065C-2			1	
		TPS2068C, TPS2069C and TPS2069C-2			1.5	
		TPS2000C and TPS2001C			2	
T_J	Operating junction temperature		–40		125	°C
$I_{\overline{FLT}}$	Sink current into $\overline{FLT}$		0		5	mA

(1) Some package and current rating may request an ambient temperature derating of 85°C.

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6.4 Thermal Information: SOT-23

THERMAL METRIC[1]		TPS20xxC, TPS20xxC-2		UNIT
		DBV (SOT-23)[2]	DBV (SOT-23)[3]	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	224.9	220.4	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	95.2	89.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.4	46.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.3	46.2	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W
$R_{\theta JA}$Custom	See *Power Dissipation and Junction Temperature*	139.3	134.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Rated at 0.5 A or 1 A.
(3) Rated at 1.5 A or 2 A.

6.5 Thermal Information: MSOP-PowerPAD

THERMAL METRIC[1]		TPS20xxC, TPS20xxC-2			UNIT
		DGN (MSOP-PowerPAD)[2]	DGN (MSOP-PowerPAD)[3]	DGK (VSSOP)[4]	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.1	67.1	205.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.3	80.8	94.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.2	37.2	126.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.3	5.6	24.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42	36.9	125.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	39.2	32.1	—	°C/W
$R_{\theta JA}$Custom	See *Power Dissipation and Junction Temperature*	66.5	61.3	110.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Rated at 0.5 A or 1 A.
(3) Rated at 1.5 A or 2 A.
(4) Rated at 2 A.

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6.6 Electrical Characteristics: $T_J = T_A = 25°C$

Unless otherwise noted: V_{IN} = 5 V, V_{EN} = V_{IN} or $V_{\overline{EN}}$ = GND, I_{OUT} = 0 A. See *Device Comparison Table* for the rated current of each part number. Parametrics over a wider operational range are shown in *Electrical Characteristics: –40°C ≤ T_J ≤ 125°C* (1).

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
POWER SWITCH							
$R_{DS(on)}$	Input – output resistance	0.5-A rated output, 25°C	DBV		97	110	mΩ
		0.5-A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DBV		96	130	mΩ
		1-A rated output, 25°C	DBV		96	110	mΩ
			DGN		86	100	
		1-A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DBV		96	130	mΩ
			DGN		86	120	
		1.5-A rated output, 25°C	DBV		76	91	mΩ
			DGN		69	84	mΩ
		1.5-A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DBV		76	106	mΩ
			DGN		69	98	mΩ
		2-A rated output, 25°C	DGN, DGK		72	84	mΩ
		2-A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DGN, DGK		72	98	mΩ
CURRENT LIMIT							
I_{OS} (3)	Current limit, See Figure 6-6	0.5-A rated output	TPS20xxC	0.67	0.85	1.01	A
		1-A rated output	TPS20xxC	1.3	1.55	1.8	
			TPS20xxC-2	1.18	1.53	1.88	
		1.5-A rated output	TPS20xxC	1.7	2.15	2.5	
			TPS20xxC-2	1.71	2.23	2.75	
		2-A rated output	TPS20xxC	2.35	2.9	3.4	
SUPPLY CURRENT							
I_{SD}	Supply current, switch disabled	I_{OUT} = 0 A			0.01	1	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{IN} = 5.5 V, I_{OUT} = 0 A				2	
I_{SE}	Supply current, switch enabled	I_{OUT} = 0 A			60	70	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{IN} = 5.5 V, I_{OUT} = 0 A				85	
I_{lkg}	Leakage current	V_{OUT} = 0 V, V_{IN} = 5 V, disabled, measure I_{VIN}	TPS20xxC-2		0.05	1	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{OUT} = 0 V, V_{IN} = 5 V, disabled, measure I_{VIN}				2	
I_{REV}	Reverse leakage current	V_{OUT} = 5 V, V_{IN} = 0 V, measure I_{VOUT}			0.1	1	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{OUT} = 5 V, V_{IN} = 0 V, measure I_{VOUT}				5	
OUTPUT DISCHARGE							
R_{PD}	Output pulldown resistance(2)	V_{IN} = V_{OUT} = 5 V, disabled	TPS20xxC	400	470	600	Ω

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(2) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(3) See *Current Limit* section for explanation of this parameter.

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6.7 Electrical Characteristics: –40°C ≤ T_J ≤ 125°C

Unless otherwise noted:4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN} or $V_{\overline{EN}}$ = GND, I_{OUT} = 0 A, typical values are at 5 V and 25°C. See *Device Comparison Table* for the rated current of each part number.

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
POWER SWITCH							
$R_{DS(ON)}$	Input – output resistance	0.5-A rated output	DBV		97	154	mΩ
		1-A rated output	DBV		96	154	mΩ
			DGN		86	140	
		1.5-A rated output	DBV		76	121	mΩ
			DGN		69	112	mΩ
		2-A rated output	DGN, DGK		72	112	mΩ
ENABLE INPUT (EN or $\overline{EN}$)							
	Threshold	Input rising		1	1.45	2	V
	Hysteresis			0.07	0.13	0.2	V
	Leakage current	(V_{EN} or $V_{\overline{EN}}$) = 0 V or 5.5 V		–1	0	1	µA
CURRENT LIMIT							
I_{OS} [3]	Current limit, See Figure 8-1	0.5-A rated output	TPS20xxC	0.65	0.85	1.05	A
		1-A rated output	TPS20xxC	1.2	1.55	1.9	
			TPS20xxC-2	1.1	1.53	1.96	
		1.5-A rated output	TPS20xxC	1.6	2.15	2.7	
			TPS20xxC-2	1.6	2.23	2.86	
		2-A rated output	TPS20xxC	2.3	2.9	3.6	
t_{IOS}	Short-circuit response time[2]	V_{IN} = 5 V (see Figure 6-6), One-half full load → R_{SHORT} = 50 mΩ, Measure from application to when current falls below 120% of final value			2		µs
SUPPLY CURRENT							
I_{SD}	Supply current, switch disabled	I_{OUT} = 0 A			0.01	10	µA
I_{SE}	Supply current, switch enabled	I_{OUT} = 0 A			65	90	µA
I_{lkg}	Leakage current	V_{OUT} = 0 V, V_{IN} = 5 V, disabled, measure I_{VIN}	TPS20XXC-2		0.05		µA
I_{REV}	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = 0 V, measure I_{VOUT}			0.2	20	µA
UNDERVOLTAGE LOCKOUT							
V_{UVLO}	Rising threshold	V_{IN}↑		3.5	3.75	4	V
	Hysteresis[2]	V_{IN}↓			0.14		V
$\overline{FLT}$							
	Output low voltage, $\overline{FLT}$	$I_{\overline{FLT}}$ = 1 mA				0.2	V
	OFF-state leakage	$V_{\overline{FLT}}$ = 5.5 V				1	µA
$t_{\overline{FLT}}$	$\overline{FLT}$ deglitch	$\overline{FLT}$ assertion or deassertion deglitch		6	9	12	ms
OUTPUT DISCHARGE							
R_{PD}	Output pulldown resistance	V_{IN} = 4 V, V_{OUT} = 5 V, disabled	TPS20XXC	350	560	1200	Ω
		V_{IN} = 5 V, V_{OUT} = 5 V, disabled	TPS20XXC	300	470	800	
THERMAL SHUTDOWN							
	Rising threshold (T_J)	In current limit		135			°C
		Not in current limit		155			
	Hysteresis [2]				20		

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(2) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(3) See *Current Limit* for explanation of this parameter.

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6.8 Timing Requirements: $T_J = T_A = 25°C$

				MIN	NOM	MAX	UNIT
ENABLE INPUT (EN or $\overline{EN}$)							
t_{ON}	Turnon time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, EN ↑ or $\overline{EN}$ ↓. See Figure 6-1, Figure 6-3, and Figure 6-4	0.5-A and 1-A Rated	1	1.4	1.8	ms
			1.5-A and 2-A Rated	1.2	1.7	2.2	
t_{OFF}	Turnoff time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, EN ↓ or $\overline{EN}$ ↑. See Figure 6-1, Figure 6-3, and Figure 6-4	0.5-A and 1-A Rated	1.3	1.65	2	ms
			1.5-A and 2-A Rated	1.7	2.1	2.5	
t_R	Rise time, output	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V. See Figure 6-2	0.5-A and 1-A Rated	0.4	0.55	0.7	ms
			1.5-A and 2-A Rated	0.5	0.7	1	
t_F	Fall time, output	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V. See Figure 6-2	0.5-A and 1-A Rated	0.25	0.35	0.45	ms
			1.-5A and 2-A Rated	0.3	0.43	0.55	

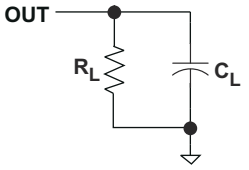


Figure 6-1. Output Rise and Fall Test Load

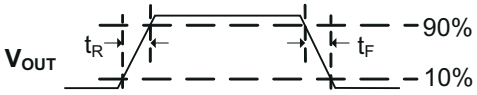


Figure 6-2. Power-On and Power-Off Timing

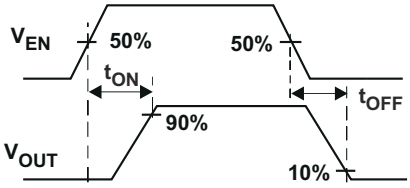


Figure 6-3. Enable Timing, Active High Enable

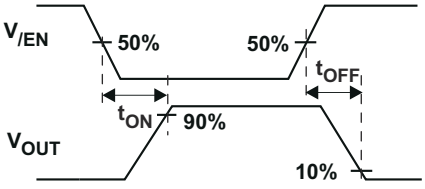


Figure 6-4. Enable Timing, Active Low Enable

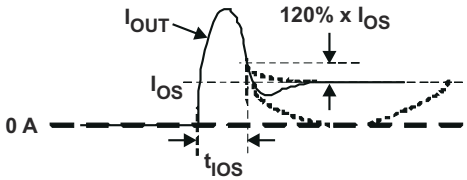


Figure 6-5. Output Short-Circuit Parameters

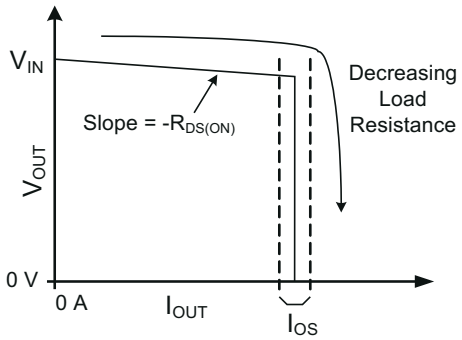


Figure 6-6. Output Characteristic Showing Current Limit

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6.9 Typical Characteristics

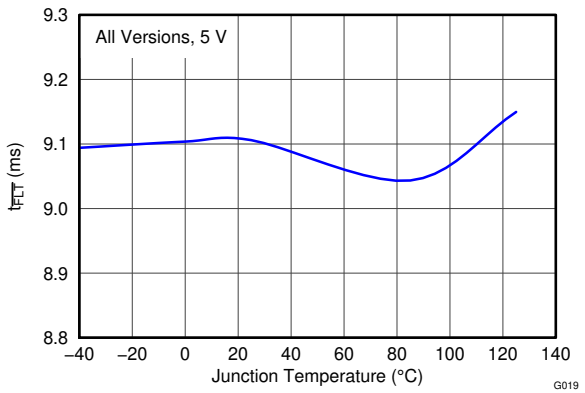


Figure 6-7. Deglitch Period ($T_{\overline{FLT}}$) vs Temperature

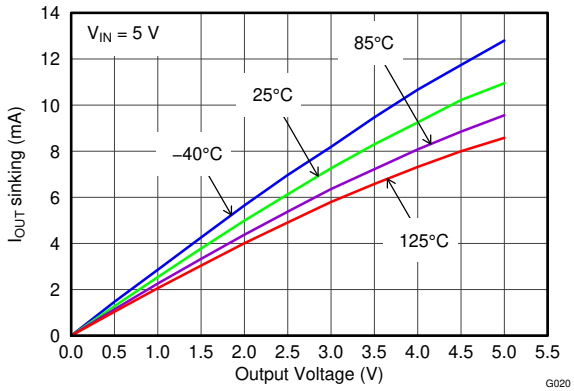


Figure 6-8. Output Discharge Current vs Output Voltage

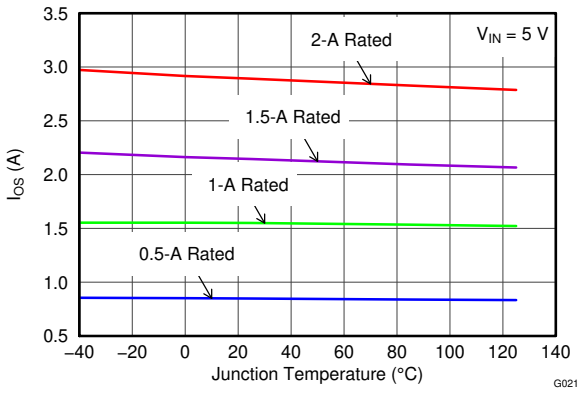


Figure 6-9. Short Circuit Current (I_{OS}) vs Temperature

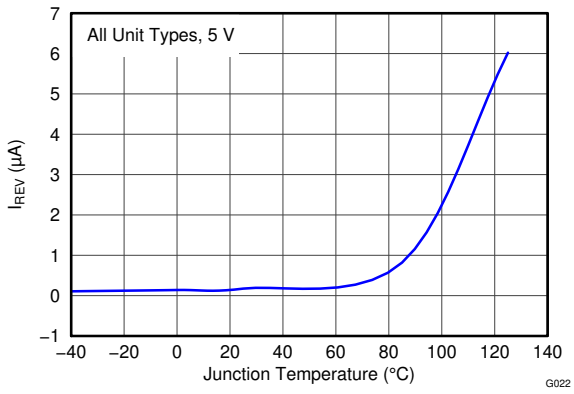


Figure 6-10. Reverse Leakage Current (I_{REV}) vs Temperature

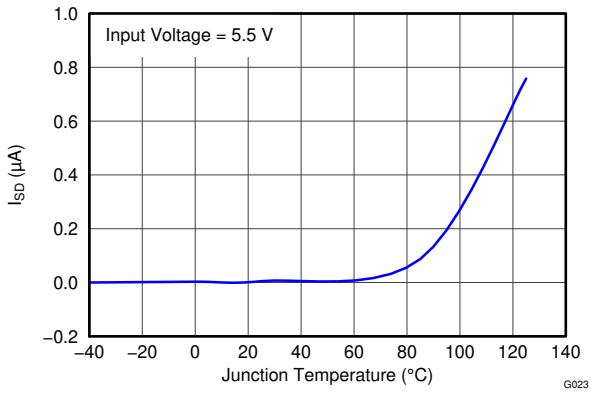


Figure 6-11. Disabled Supply Current (I_{SD}) vs Temperature

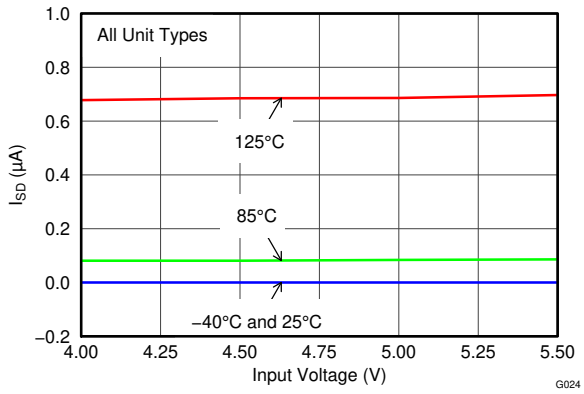


Figure 6-12. Disabled Supply Current (I_{SD}) vs Input Voltage

6.9 Typical Characteristics (continued)

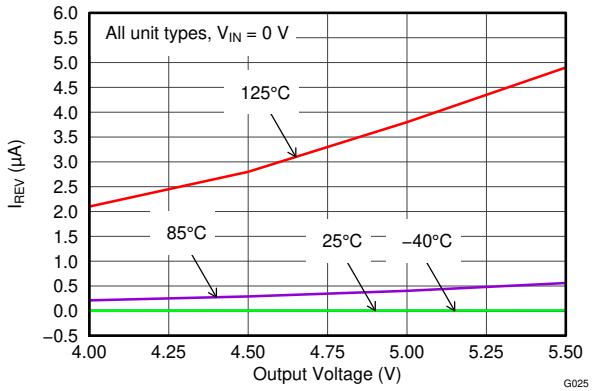


Figure 6-13. Reverse Leakage Current (I_{REV}) vs Output Voltage

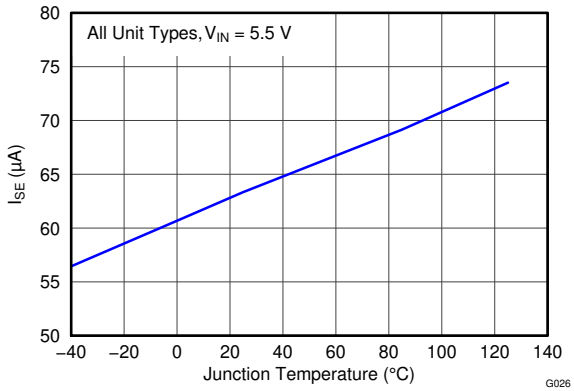


Figure 6-14. Enabled Supply Current (I_{SE}) vs Temperature

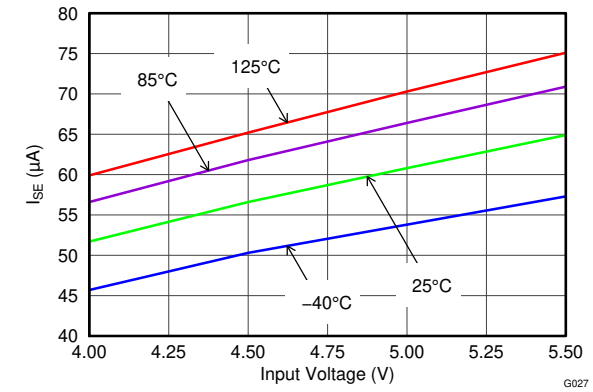


Figure 6-15. Enabled Supply Current (I_{SE}) vs Input Voltage

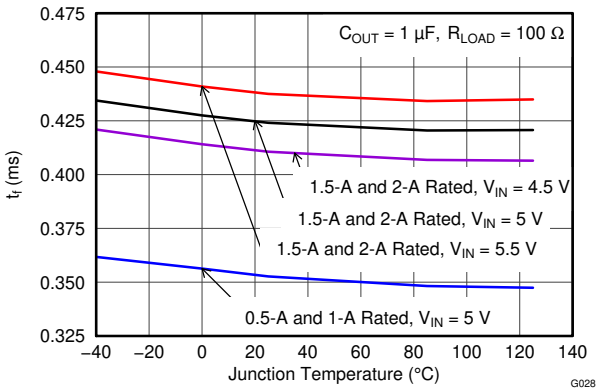


Figure 6-16. Output Fall Time (T_F) vs Temperature

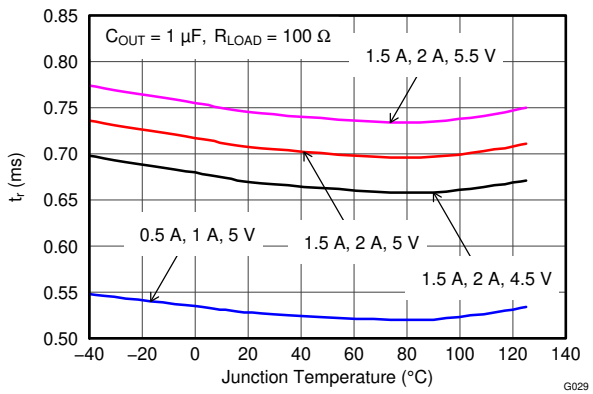


Figure 6-17. Output Rise Time (T_R) vs Temperature

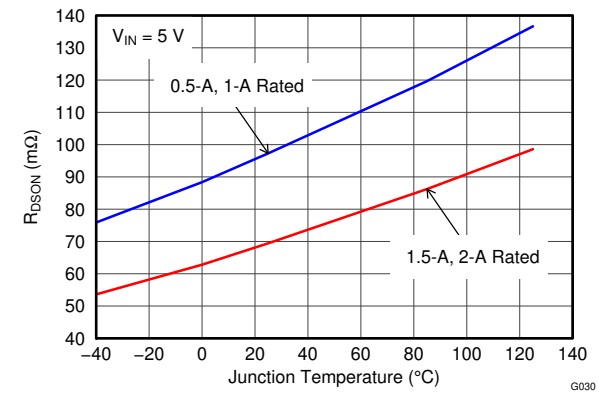


Figure 6-18. Input-Output Resistance ($R_{DS(ON)}$) vs Temperature

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6.9 Typical Characteristics (continued)

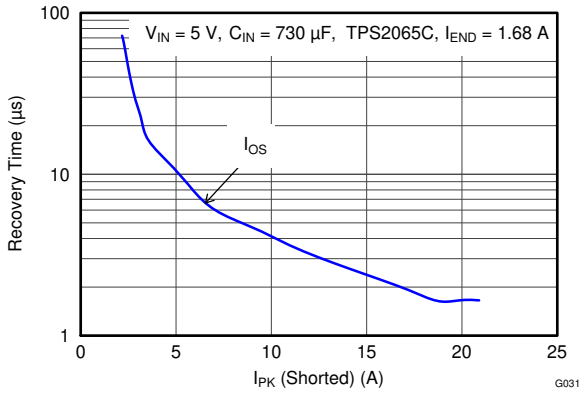


Figure 6-19. Recovery vs Current Peak

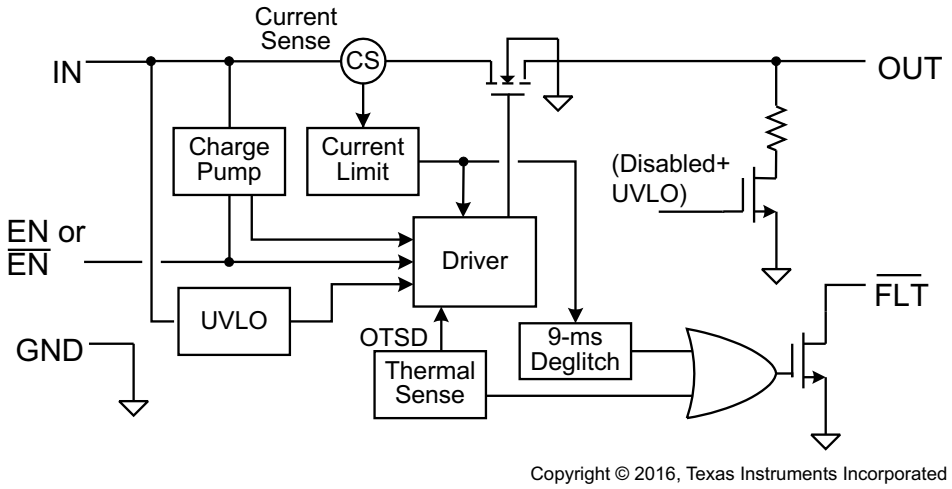
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7 Detailed Description

7.1 Overview

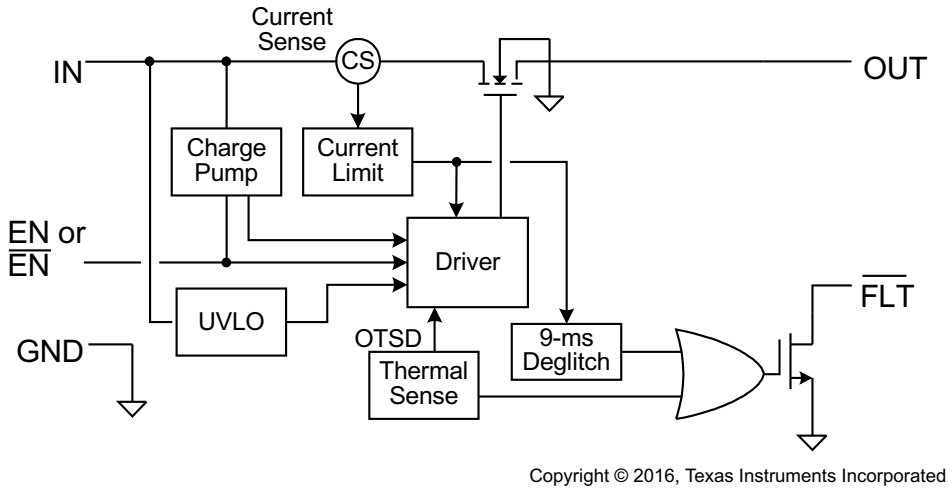
The TPS20xxC and TPS20xxC-2 are current-limited, power-distribution switches providing a range from 0.5 A and 2 A of continuous load current in 5-V circuits. These parts use N-channel MOSFETs for low resistance, maintaining voltage regulation to the load. They are designed for applications where short circuits or heavy capacitive loads are encountered. Device features include enable, reverse blocking when disabled, output discharge pulldown, overcurrent protection, overtemperature protection, and deglitched fault reporting.

7.2 Functional Block Diagram



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Figure 7-1. TPS20xxC Block Diagram



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Figure 7-2. TPS20xxC-2 Block Diagram

7.3 Feature Description

7.3.1 Undervoltage Lockout

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted ON/OFF cycling due to input voltage drop from large current surges. $\overline{FLT}$ is high impedance when the TPS20xxC and TPS20xxC-2 are in UVLO.

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7.3.2 Enable

The logic enable input (EN, or $\overline{EN}$), controls the power switch, bias for the charge pump, driver, and other circuits. The supply current is reduced to less than 1 µA when the TPS20xxC and TPS20xxC-2 are disabled. Disabling the TPS20xxC and TPS20xxC-2 immediately clears an active $\overline{FLT}$ indication. The enable input is compatible with both TTL and CMOS logic levels.

The turnon and turnoff times (t_{ON}, t_{OFF}) are composed of a delay and a rise or fall time (t_R, t_F). The delay times are internally controlled. The rise time is controlled by both the TPS20xxC and TPS20xxC-2 and the external loading (especially capacitance). TPS20xxC fall time is controlled by the loading (R and C), and the output discharge (R_{PD}). TPS20xxC-2 does not have the output discharge (R_{PD}), fall time is controlled by the loading (R and C). An output load consisting of only a resistor experiences a fall time set by the TPS20xxC and TPS20xxC-2. An output load with parallel R and C elements experiences a fall time determined by the (R × C) time constant if it is longer than the t_F TPS20xxC and TPS20xxC-2.

The enable must not be left open, and may be tied to VIN or GND depending on the device.

7.3.3 Internal Charge Pump

The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the gate driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges on the input supply, and provides built-in soft-start functionality. The MOSFET power switch blocks current from OUT to IN when turned off by the UVLO or disabled.

7.3.4 Current Limit

The TPS20xxC and TPS20xxC-2 responds to overloads by limiting output current to the static I_{OS} levels shown in *Electrical Characteristics: T_J = T_A = 25°C*. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by (I_{OS} × R_{LOAD}). Two possible overload conditions can occur. The first overload condition occurs when either:

1. input voltage is first applied, enable is true, and a short circuit is present (load which draws I_{OUT} > I_{OS})
2. input voltage is present and the TPS20xxC and TPS20xxC-2 are enabled into a short circuit.

The output voltage is held near zero potential with respect to ground and the TPS20xxC and TPS20xxC-2 ramps the output current to I_{OS}. The TPS20xxC and TPS20xxC-2 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle. This is demonstrated in Figure 8-4 where the device was enabled into a short, and subsequently cycles current OFF and ON as the thermal protection engages.

The second condition is when an overload occurs while the device is enabled and fully turned on. The device responds to the overload condition within t_{IOS} (Figure 6-5 and Figure 6-6) when the specified overload (see *Electrical Characteristics: –40°C ≤ T_J ≤ 125°C*) is applied. The response speed and shape varies with the overload level, input circuit, and rate of application. The current limit response will vary between simply settling to I_{OS}, or turnoff and controlled return to I_{OS}. Similar to the previous case, the TPS20xxC and TPS20xxC-2 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle. This is demonstrated by Figure 8-5, Figure 8-6, and Figure 8-7.

The TPS20xxC and TPS20xxC-2 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. This is due to the relatively large power dissipation [(V_{IN} – V_{OUT}) × I_{OS}] driving the junction temperature up. The device turns off when the junction temperature exceeds 135°C (minimum) while in current limit. The device remains off until the junction temperature cools 20°C and then restarts.

There are two kinds of current limit profiles typically available in TI switch products that are similar to the TPS20xxC and TPS20xxC-2. Many older designs have an output I vs V characteristic similar to the plot labeled *Current Limit with Peaking* in Figure 7-3. This type of limiting can be characterized by two parameters, the current limit corner (I_{OC}), and the short circuit current (I_{OS}). I_{OC} is often specified as a maximum value. The TPS20xxC and TPS20xxC-2 family of parts does not present noticeable peaking in the current limit,

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corresponding to the characteristic labeled *Flat Current Limit* in Figure 7-3. This is why the I_{OC} parameter is not present in *Electrical Characteristics: –40°C ≤ T_J ≤ 125°C*.

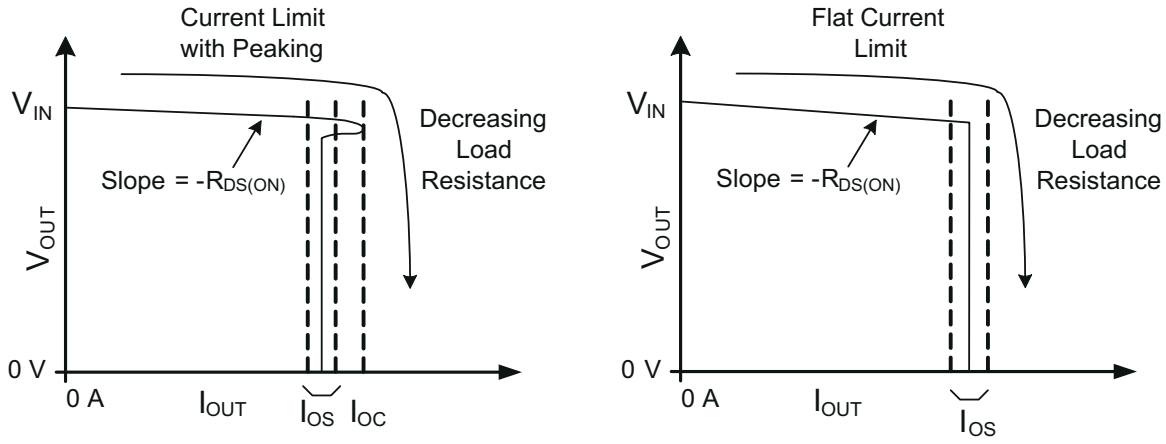


Figure 7-3. Current Limit Profiles

7.3.5 $\overline{FLT}$

The $\overline{FLT}$ open-drain output is asserted (active low) during an overload or overtemperature condition. A 9-ms deglitch on both the rising and falling edges avoids false reporting at start-up and during transients. A current limit condition shorter than the deglitch period clears the internal timer upon termination. The deglitch timer does not integrate multiple short overloads and declare a fault. This is also true for exiting from a faulted state. An input voltage with excessive ripple and large output capacitance may interfere with operation of $\overline{FLT}$ around I_{OS} as the ripple drives the TPS20xxC and TPS20xxC-2 in and out of current limit.

If the TPS20xxC and TPS20xxC-2 are in current limit and the overtemperature circuit goes active, $\overline{FLT}$ goes true immediately (see Figure 8-5); however, the exiting this condition is deglitched (see Figure 8-7). $\overline{FLT}$ is tripped just as the knee of the constant-current limiting is entered. Disabling the TPS20xxC and TPS20xxC-2 clears an active $\overline{FLT}$ as soon as the switch turns off (see Figure 8-4). $\overline{FLT}$ is high impedance when the TPS20xxC and TPS20xxC-2 are disabled or in undervoltage lockout (UVLO).

7.3.6 Output Discharge

A 470-Ω (typical) output discharge dissipates stored charge and leakage current on OUT when the TPS20xxC is in UVLO or disabled. The pulldown circuit loses bias gradually as V_{IN} decreases, causing a rise in the discharge resistance as V_{IN} falls towards 0 V. The TPS20xxC-2 does not have this function. The output is be controlled by an external loadings when the device is in ULVO or disabled.

7.4 Device Functional Modes

There are no other functional modes.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS20xxC and TPS20xxC-2 current-limited power switch uses N-channel MOSFETs in applications requiring continuous load current. The device enters constant-current mode when the load exceeds the current limit threshold.

8.2 Typical Application

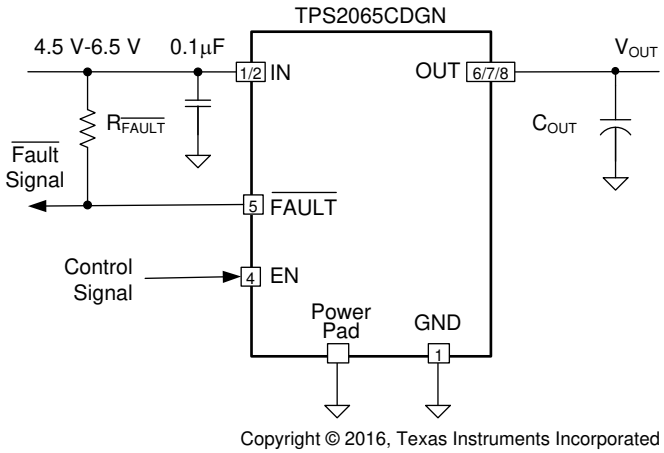


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the following input parameters:

1. The TPS2065CDGN operates from a 5-V to ±0.5-V input rail.
2. What is the normal operation current, for example, the maximum allowable current drawn by portable equipment for USB 3.0 port is 900 mA, so the normal operation current is 900 mA, and the minimum current limit of power switch must exceed 900 mA to avoid false trigger during normal operation. For the TPS2065C device, target 1-A continuous output current application.
3. What is the maximum allowable current provided by up-stream power, the maximum current limit of power switch that must lower it to ensure power switch can protect the up-stream power when overload is encountered at the output of power switch. For the TPS2065C device, the maximum I_{OS} is 1.8 A.

8.2.2 Detailed Design Procedure

To begin the design process a few parameters must be decided upon. The designer must know the following:

1. Normal input operation voltage
2. Output continuous current
3. Maximum up-stream power supply output current

8.2.2.1 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, TI recommends placing a 0.1-µF or greater ceramic bypass capacitor between IN and GND, as close to the device as possible for local noise decoupling.

All protection circuits such as the TPS20xxC and TPS20xxC-2 has the potential for input voltage overshoots and output voltage undershoots.

Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power bus inductance and input capacitance when the IN terminal is high impedance (before turnon). Theoretically, the peak voltage is 2× the applied. The second cause is due to the abrupt reduction of output short-circuit current when the TPS20xxC and TPS20xxC-2 turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the TPS20xxC and TPS20xxC-2 output is shorted. Applications with large input inductance (for example, connecting the evaluation board to the bench power-supply through long cables) may require large input capacitance reduce the voltage overshoot from exceeding the absolute maximum voltage of the device. The fast current limit speed of the TPS20xxC and TPS20xxC-2 to hard output short circuits isolates the input bus from faults. However, ceramic input capacitance in the range of 1 µF to 22 µF adjacent to the TPS20xxC and TPS20xxC-2 input aids in both speeding the response time and limiting the transient seen on the input power bus. Momentary input transients to 6.5 V are permitted.

Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the TPS20xxC and TPS20xxC-2 has abruptly reduced OUT current. Energy stored in the inductance drives the OUT voltage down and potentially negative as it discharges. Applications with large output inductance (such as from a cable) benefit from use of a high-value output capacitor to control the voltage undershoot. When implementing USB standard applications, a 120-µF minimum output capacitance is required. Typically a 150-µF electrolytic capacitor is used, which is sufficient to control voltage undershoots. However, if the application does not require 120 µF of capacitance, and there is potential to drive the output negative, then TI recommends a minimum of 10-µF ceramic capacitance on the output. The voltage undershoot must be controlled to less than 1.5 V for 10 µs.

8.2.3 Application Curves

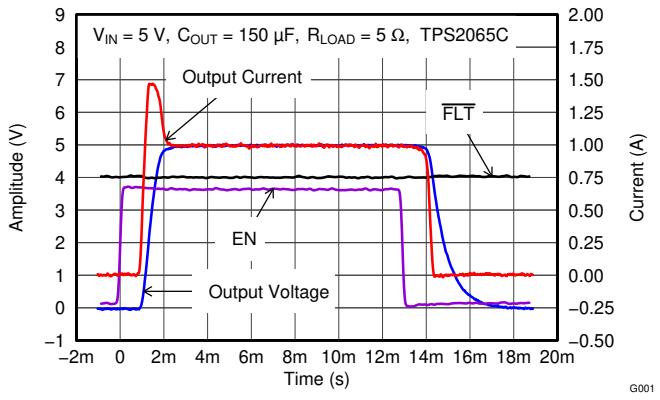


Figure 8-2. TPS2065C Output Rise / Fall 5 Ω

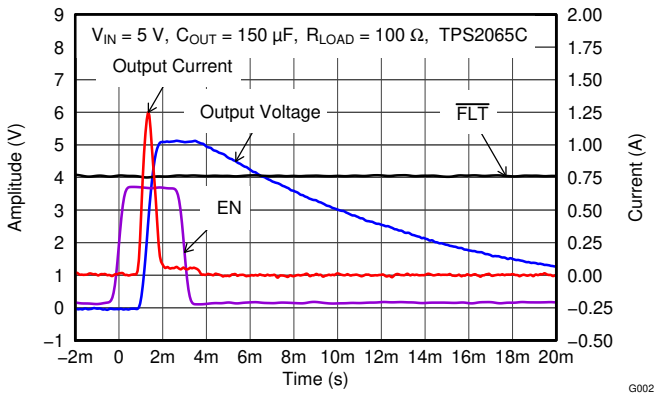


Figure 8-3. TPS2065C Output Rise / Fall 100 Ω

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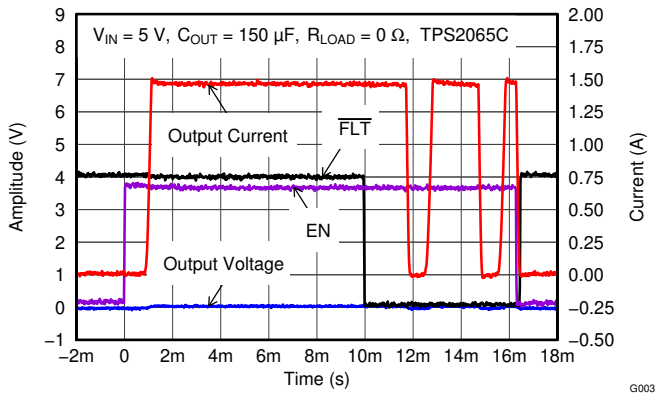


Figure 8-4. TPS2065C Enable into Output Short

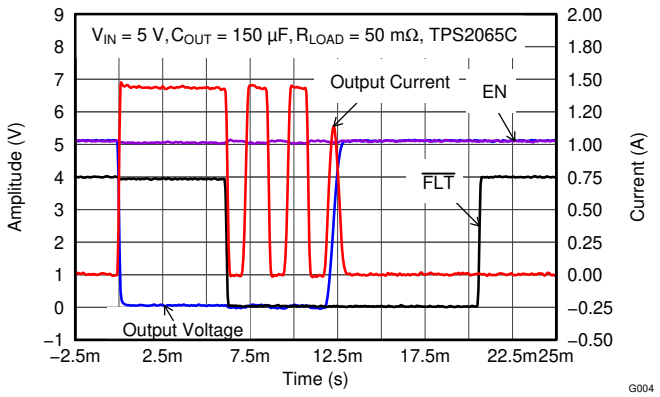


Figure 8-5. TPS2065C Pulsed Short Applied

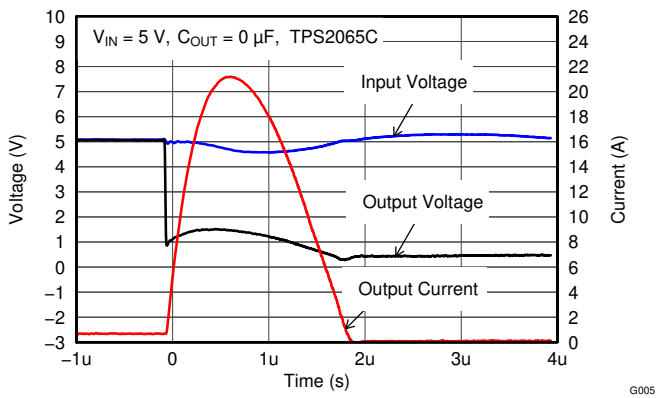


Figure 8-6. TPS2065C Short Applied

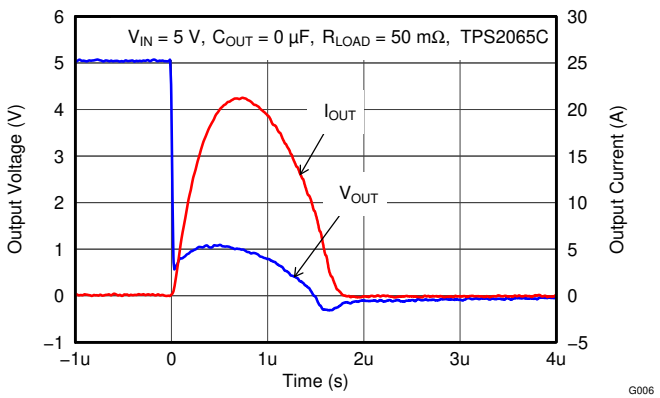


Figure 8-7. TPS2065C Pulsed 1.45-A Load

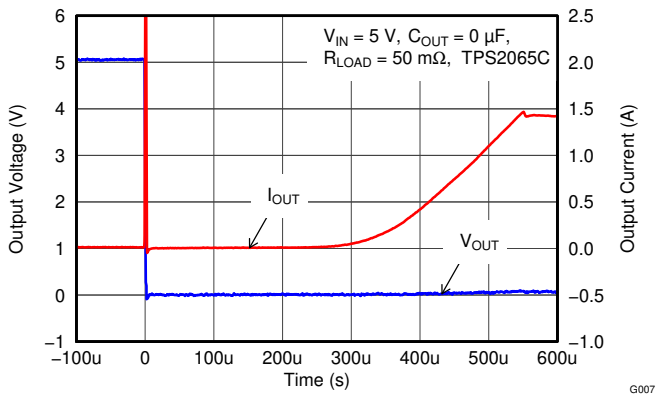


Figure 8-8. TPS2065C 50-mΩ Short Circuit

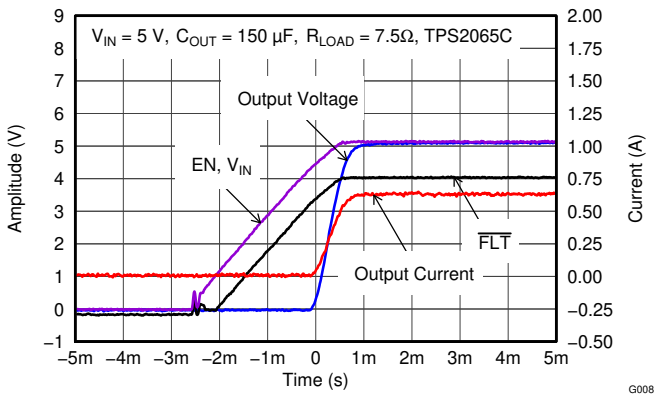


Figure 8-9. TPS2065C Power Up – Enabled

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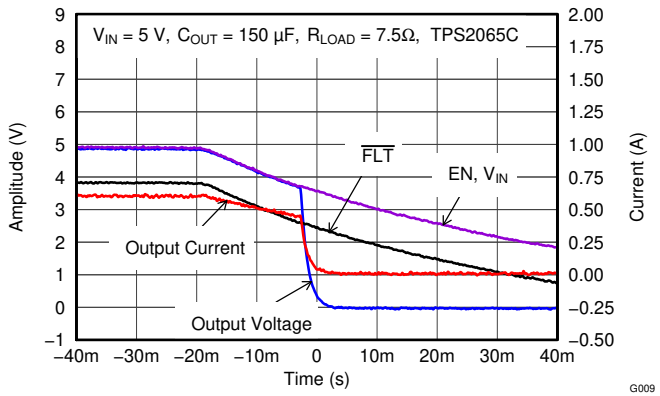


Figure 8-10. TPS2065C Power Down – Enabled

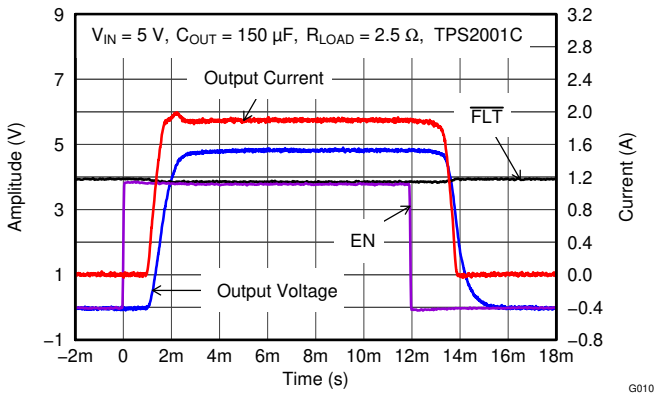


Figure 8-11. TPS2001C Turnon into 2.5 Ω

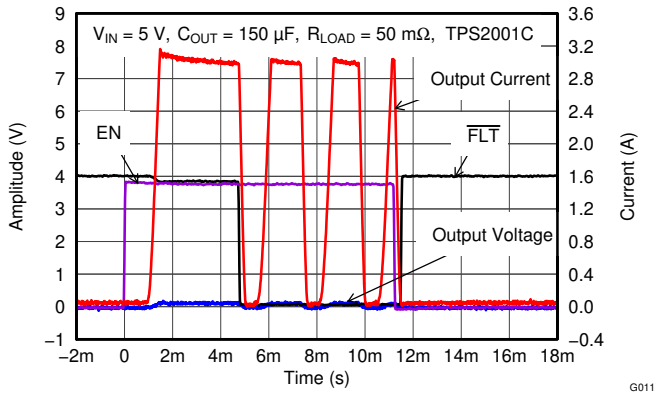


Figure 8-12. TPS2001C Enable into Short

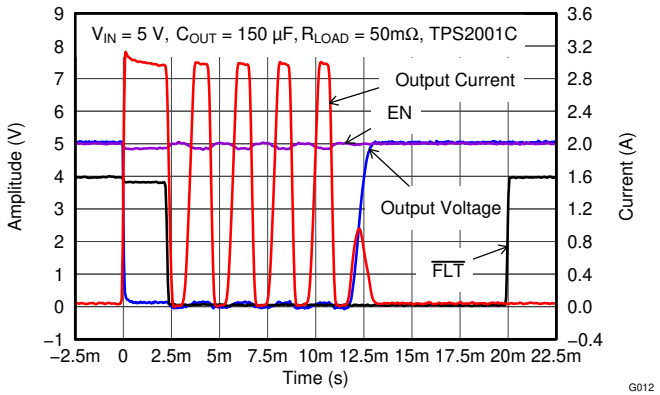


Figure 8-13. TPS2001C Pulsed Output Short

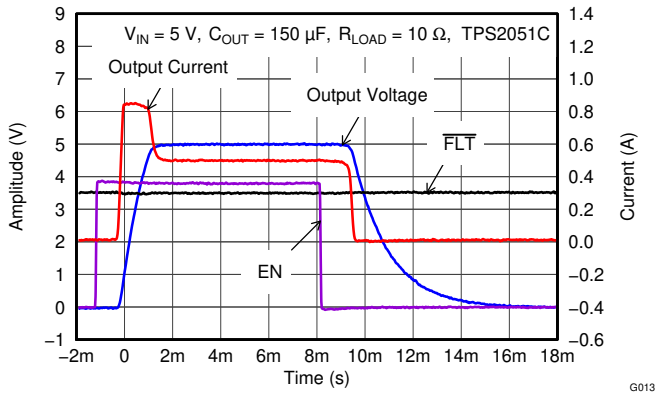


Figure 8-14. TPS2051C Turnon into 10 Ω

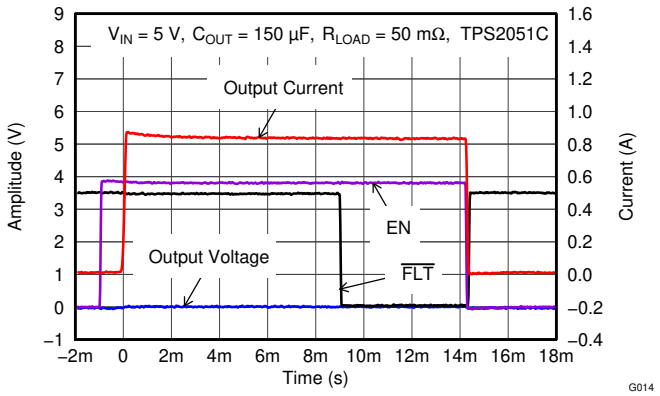


Figure 8-15. TPS2051C Enable into Short

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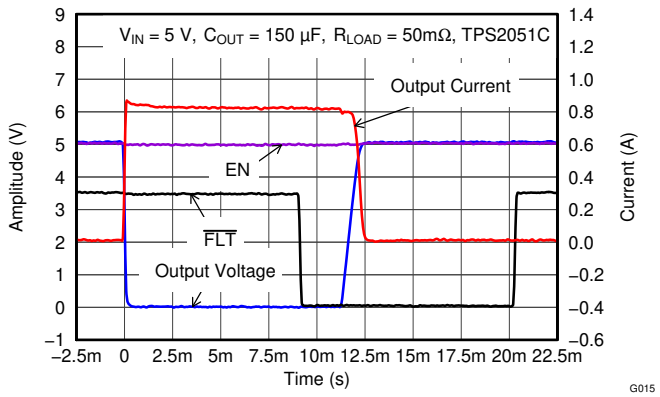


Figure 8-16. TPS2051C Pulsed Output Short

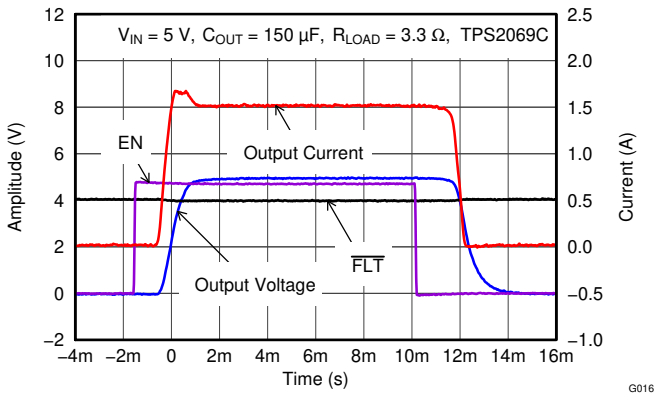


Figure 8-17. TPS2069C Turnon into 3.3 Ω

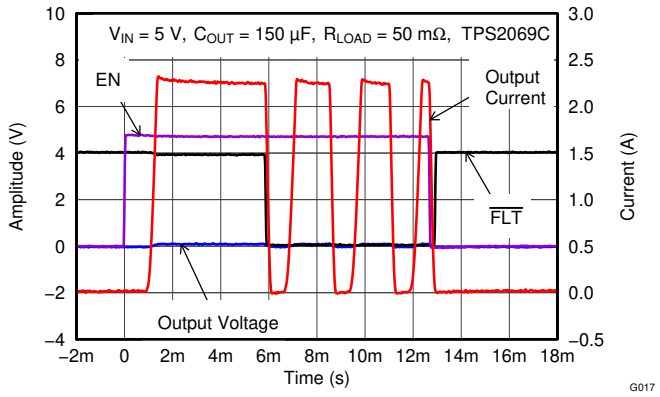


Figure 8-18. TPS2069C Enable into Short

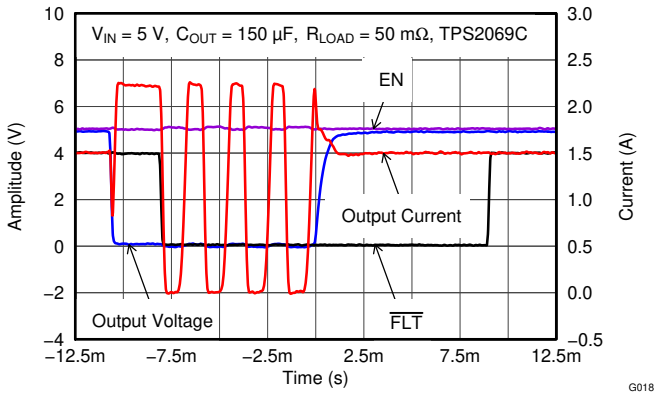


Figure 8-19. TPS2069C Pulsed Output Short

9 Power Supply Recommendations

Design of the devices is for operation from an input voltage supply range of 4.5 V to 5.5 V. The current capability of the power switch should exceed the maximum current limit of the power switch.

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10 Layout

10.1 Layout Guidelines

1. Place the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low inductance trace.
2. Place at least 10-µF low ESR ceramic capacitor near the OUT and GND pins, and make the connections using a low inductance trace.
3. The PowerPAD must be directly connected to PCB ground plane using wide and short copper trace.

10.2 Layout Example

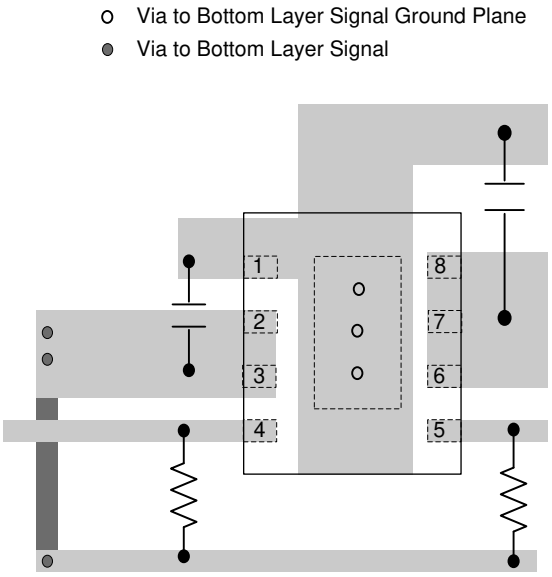


Figure 10-1. Recommended Layout

10.3 Power Dissipation and Junction Temperature

It is good design practice to estimate power dissipation and maximum expected junction temperature of the TPS20xxC and TPS20xxC-2. The system designer can control choices of package, proximity to other power dissipating devices, and printed-circuit board (PCB) design based on these calculations. These have a direct influence on maximum junction temperature. Other factors, such as airflow and maximum ambient temperature, are often determined by system considerations. It is important to remember that these calculations do not include the effects of adjacent heat sources, and enhanced or restricted air flow.

Addition of extra PCB copper area around these devices is recommended to reduce the thermal impedance and maintain the junction temperature as low as practical. The lower junction temperatures achieved by soldering the pad improve the efficiency and reliability of both TPS20xxC and TPS20xxC-2 parts and the system. The following examples were used to determine the θ_{JA}Custom thermal impedances noted in *Thermal Information: SOT-23* and *Thermal Information: MSOP-PowerPAD*. They were based on use of the JEDEC high-k circuit board construction (2 signal and 2 plane) with 4, 1-oz. copper weight, layers.

While TI recommends that the DGN package PAD be soldered to circuit board copper fill and vias for low thermal impedance, there may be cases where this is not desired. For example, use of routing area under the IC. Some devices are available in packages without the PowerPAD (DGK) specifically for this purpose. The θ_{JA} for the DGN package with the pad not soldered and no extra copper, is approximately 141°C/W for 0.5-A and 1-A rated parts, and 139°C/W for the 1.5-A and 2-A rated parts. The θ_{JA} for the DGK mounted per Figure 10-4 is 110.3°C/W. These values may be used in Equation 1 to determine the maximum junction temperature.

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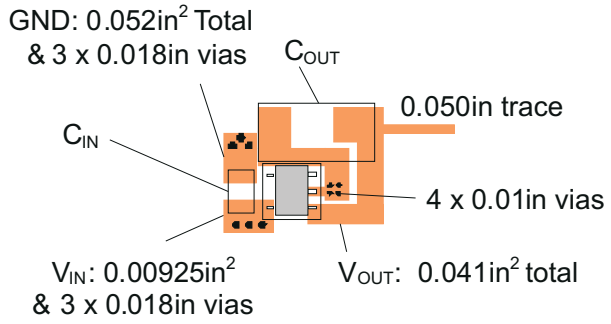


Figure 10-2. DBV Package PCB Layout Example

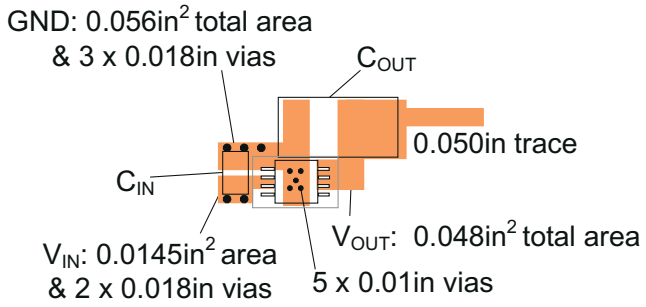


Figure 10-3. DGN Package PCB Layout Example

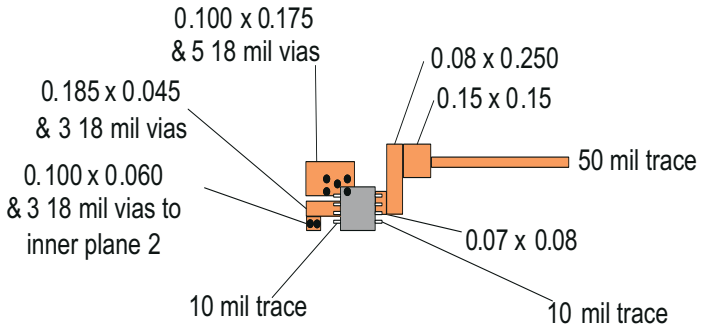


Figure 10-4. DGK Package PCB Layout Example

As shown in Equation 1, the following procedure requires iteration because power loss is due to the internal MOSFET $I^2 \times R_{DS(ON)}$, and $R_{DS(ON)}$ is a function of the junction temperature. As an initial estimate, use the $R_{DS(ON)}$ at 125°C from the *Typical Characteristics*, and the preferred package thermal resistance for the preferred board construction from the *Thermal Information: SOT-23* table.

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$$T_J = T_A + ((I_{OUT}{}^2 \times R_{DS(ON)}) \times \theta_{JA}) \quad (1)$$

where

- I_{OUT} = rated OUT pin current (A)
- $R_{DS(ON)}$ = Power switch ON-resistance at an assumed T_J (Ω)
- T_A = Maximum ambient temperature (°C)
- T_J = Maximum junction temperature (°C)
- θ_{JA} = Thermal resistance (°C/W)

If the calculated T_J is substantially different from the original assumption, estimate a new value of $R_{DS(ON)}$ using the typical characteristic plot and recalculate.

If the resulting T_J is not less than 125°C, try a PCB construction or a package with lower θ_{JA}.

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.3 Trademarks

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All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (April 2016) to Revision I (May 2026) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1

Changes from Revision G (July 2013) to Revision H (April 2016) **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Deleted *Devices* table (previously Table 1) 3

Changes from Revision F (August 2012) to Revision G (July 2013) **Page**

- Deleted (See Table 1) from Feature: UL Listed and CB-File No. E169910..... 1
- Changed From: PXKI To: PYKI in the DEVICE INFORMATION table SOT23-5 (DBV) column (TPS2069C)... 3
- Deleted Note 2 from : "UL listed and CB complete"..... 3

Changes from Revision E (April 2012) to Revision F (August 2012) **Page**

- Added device TPS20xxC-2 1
- Changed Feature From: Ouput Discharge When TPS20XXC is Disabled To: Selected parts with (TPS20xxC) and without (TPS20xxC-2) Output Discharge..... 1
- Added devices TPS2041C, TPS2061C, TPS2065C-2, TPS2068C, and TPS2069C-2 to the Device Information table..... 3
- Added the TPS2069C-2 Device..... 3
- Added PXKI in the DEVICE INFORMATION table SOT23-5 (DBV) column (TPS2069C)..... 3
- Added devices TPS2041C, TPS2061C, TPS2065C-2, TPS2068C, and TPS2069C-2 to and removed Product Preview..... 3
- Added Note 1 to the RECOMMENDED OPERATING CONDITIONS table..... 5
- Added TPS2041C, TPS2061C, TPS2068C, TPS2065C-2 and TPS2069C-2 devices to I_{OUT} in the RECOMMENDED OPERATING CONDITIONS table..... 5
- Added the DBV option to Power Switch $R_{DS(on)}$ 1.5 A rated output, 25°C mΩ..... 7
- Added the DBV option to Power Switch $R_{DS(on)}$ 1.5 A rated output 7
- Changed I_{SO} Current Limit 7
- Added Leakage Current..... 7
- Added the DBV option to Power Switch $R_{DS(on)}$ 1.5 A rated output 8
- Changed I_{SO} Current Limit 8
- Added Leakage Current..... 8
- Changed the second para graph of the ENABLE section..... 15
- Added sentence to end of paragraph in the OUTPUT DISCHARGE section..... 16

Changes from Revision D (February 2012) to Revision E (April 2012) **Page**

- Changed the POWER DISSIPATION AND JUNCTION TEMPERATURE section. Replaced paragraph " While it is recommended..."..... 22

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Changes from Revision C (October 2011) to Revision D (February 2012) **Page**

- Added Feature UL Listed and CB-File No. E169910 1
- Added table Note 2, UL listed and CB complete..... 3
- Added V_{IH} and V_{IL} information to the ROC Table..... 5

Changes from Revision B (September 2011) to Revision C (October 2011) **Page**

- Changed From: PXF1 To: PXFI and From: PSG1 To: PXGI in the DEVICE INFORMATION table MOSP-8 (DGK) column..... 3
- Changed TPS2000C (MSOP-8) status From: Preview To: Active in Table 1..... 3
- Changed the θJACustom 2 A Rated DGK value from N/A to 110.3..... 6
- Added Figure 10-4 - DGK Package PCB Layout Example..... 22

Changes from Revision A (July 2011) to Revision B (September 2011) **Page**

- Added the DGK Package Information throughout the data sheet..... 3
- Changed title of Figure 8-8 From: NEW FIG To: TPS2065C 50 Ω Short Circuit..... 18

Changes from Revision * (June 2011) to Revision A (July 2011) **Page**

- Changed the TPS2051C, TPS2065C, and TPS2069C Devices Status From: Preview To: Active..... 3
- Corrected pinout numbers for the 5-PIN PACKAGE 3

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
905X0205100	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VBYQ
TPS2000CDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	PXFI
TPS2000CDGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXFI
TPS2000CDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXFI
TPS2000CDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXFI
TPS2000CDGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BCMS
TPS2000CDGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BCMS
TPS2000CDGN.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BCMS
TPS2000CDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BCMS
TPS2000CDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BCMS
TPS2000CDGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BCMS
TPS2001CDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	PXGI
TPS2001CDGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXGI
TPS2001CDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXGI
TPS2001CDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXGI
TPS2001CDGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	VBWQ
TPS2001CDGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBWQ
TPS2001CDGN.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBWQ
TPS2001CDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	VBWQ
TPS2001CDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBWQ
TPS2001CDGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBWQ
TPS2041CDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	PYJI
TPS2041CDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PYJI
TPS2041CDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PYJI
TPS2041CDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYJI
TPS2041CDBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYJI
TPS2041CDBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYJI
TPS2041CDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYJI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2041CDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYJI
TPS2041CDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYJI
TPS2051CDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBYQ
TPS2051CDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBYQ
TPS2051CDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBYQ
TPS2051CDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBYQ
TPS2051CDBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBYQ
TPS2051CDBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBYQ
TPS2051CDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBYQ
TPS2051CDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBYQ
TPS2051CDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBYQ
TPS2061CDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	PXLI
TPS2061CDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PXLI
TPS2061CDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PXLI
TPS2061CDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXLI
TPS2061CDBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXLI
TPS2061CDBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXLI
TPS2061CDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXLI
TPS2061CDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXLI
TPS2061CDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXLI
TPS2061CDGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXMI
TPS2061CDGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXMI
TPS2061CDGN.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXMI
TPS2061CDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXMI
TPS2061CDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXMI
TPS2061CDGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXMI
TPS2065CDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2065CDBVR-2	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYQI
TPS2065CDBVR-2.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYQI
TPS2065CDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2065CDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCAQ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2065CDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2065CDBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2065CDBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2065CDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2065CDBVT-2	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYQI
TPS2065CDBVT-2.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYQI
TPS2065CDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2065CDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2065CDGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2065CDGN-2	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYRI
TPS2065CDGN-2.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYRI
TPS2065CDGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2065CDGN.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2065CDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2065CDGNR-2	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYRI
TPS2065CDGNR-2.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYRI
TPS2065CDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2065CDGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCAQ
TPS2068CDGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXNI
TPS2068CDGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXNI
TPS2068CDGN.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXNI
TPS2068CDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXNI
TPS2068CDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXNI
TPS2068CDGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PXNI
TPS2069CDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYKI
TPS2069CDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYKI
TPS2069CDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYKI
TPS2069CDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYKI
TPS2069CDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYKI
TPS2069CDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYKI
TPS2069CDBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYKI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2069CDBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYKI
TPS2069CDBVTG4.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYKI
TPS2069CDGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	VBUQ
TPS2069CDGN-2	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYSI
TPS2069CDGN-2.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYSI
TPS2069CDGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBUQ
TPS2069CDGN.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBUQ
TPS2069CDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	VBUQ
TPS2069CDGNR-2	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYSI
TPS2069CDGNR-2.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYSI
TPS2069CDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBUQ
TPS2069CDGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VBUQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

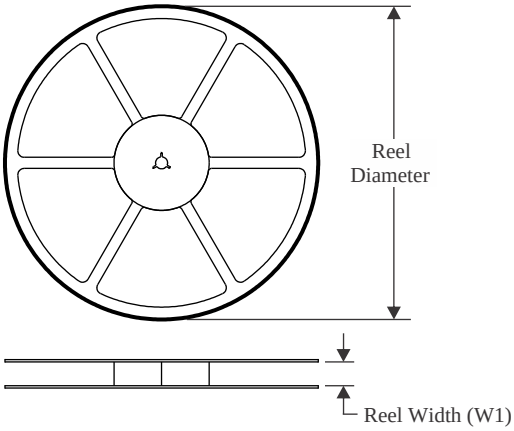
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

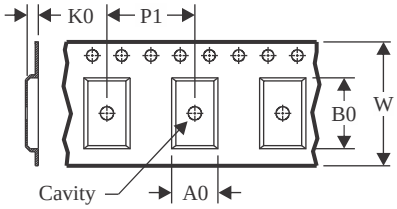
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

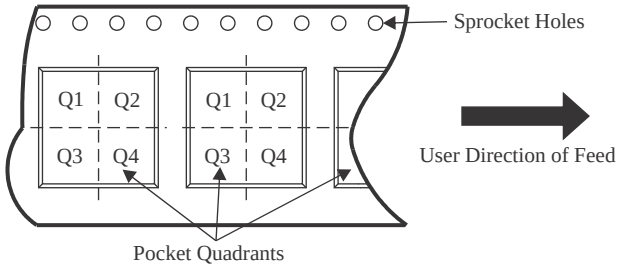


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

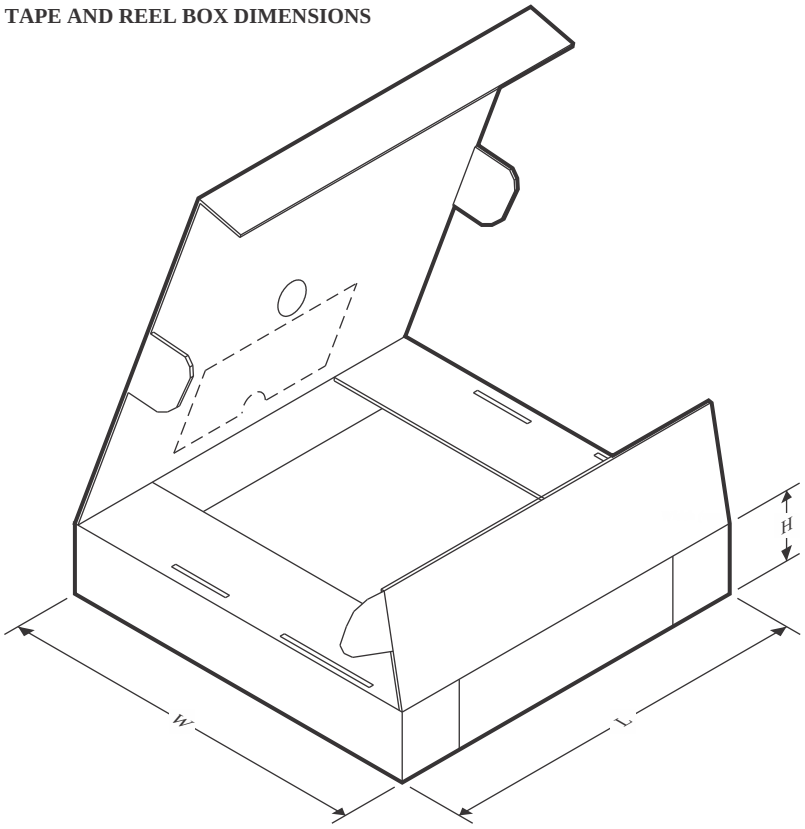


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2000CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2000CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2001CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2001CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2001CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2041CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2041CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2041CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2041CDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2041CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2051CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2051CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2051CDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2051CDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2051CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2061CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2061CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2061CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2061CDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2061CDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS2061CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2061CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2065CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2065CDBVR-2	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2065CDBVR-2	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2065CDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2065CDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS2065CDBVT-2	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS2065CDBVT-2	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2065CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2065CDGNR-2	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2068CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2069CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2069CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS2069CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2069CDBVTG4	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2069CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2069CDGNR-2	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

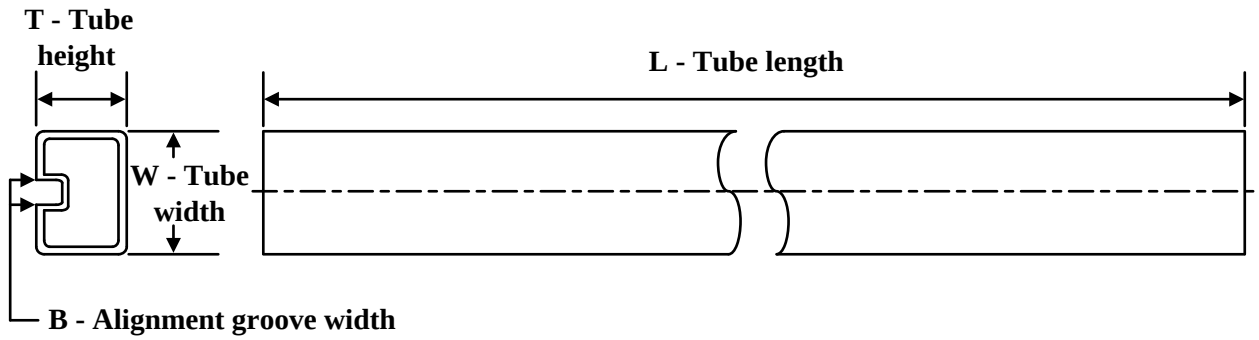


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2000CDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TPS2000CDGNR	HVSSOP	DGN	8	2500	360.0	162.0	98.0
TPS2001CDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TPS2001CDGNR	HVSSOP	DGN	8	2500	370.0	355.0	55.0
TPS2001CDGNR	HVSSOP	DGN	8	2500	360.0	162.0	98.0
TPS2041CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2041CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2041CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2041CDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2041CDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS2051CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2051CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2051CDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2051CDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2051CDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS2061CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2061CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2061CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2061CDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2061CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS2061CDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS2061CDGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS2065CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2065CDBVR-2	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2065CDBVR-2	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2065CDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2065CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS2065CDBVT-2	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS2065CDBVT-2	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS2065CDGNR	HVSSOP	DGN	8	2500	360.0	162.0	98.0
TPS2065CDGNR-2	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS2068CDGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS2069CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2069CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2069CDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS2069CDBVTG4	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS2069CDGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS2069CDGNR-2	HVSSOP	DGN	8	2500	366.0	364.0	50.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2000CDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TPS2000CDGK.B	DGK	VSSOP	8	80	330	6.55	500	2.88
TPS2000CDGN	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2000CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2000CDGN.A	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2000CDGN.A	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2000CDGN.B	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2000CDGN.B	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2001CDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TPS2001CDGK.B	DGK	VSSOP	8	80	330	6.55	500	2.88
TPS2001CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2001CDGN	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2001CDGN.A	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2001CDGN.A	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2001CDGN.B	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2001CDGN.B	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2061CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2061CDGN.A	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2061CDGN.B	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2065CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2065CDGN	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2065CDGN-2	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2065CDGN-2.A	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2065CDGN.A	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2065CDGN.A	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2065CDGN.B	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2065CDGN.B	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2068CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2068CDGN.A	DGN	HVSSOP	8	80	330	6.55	500	2.88

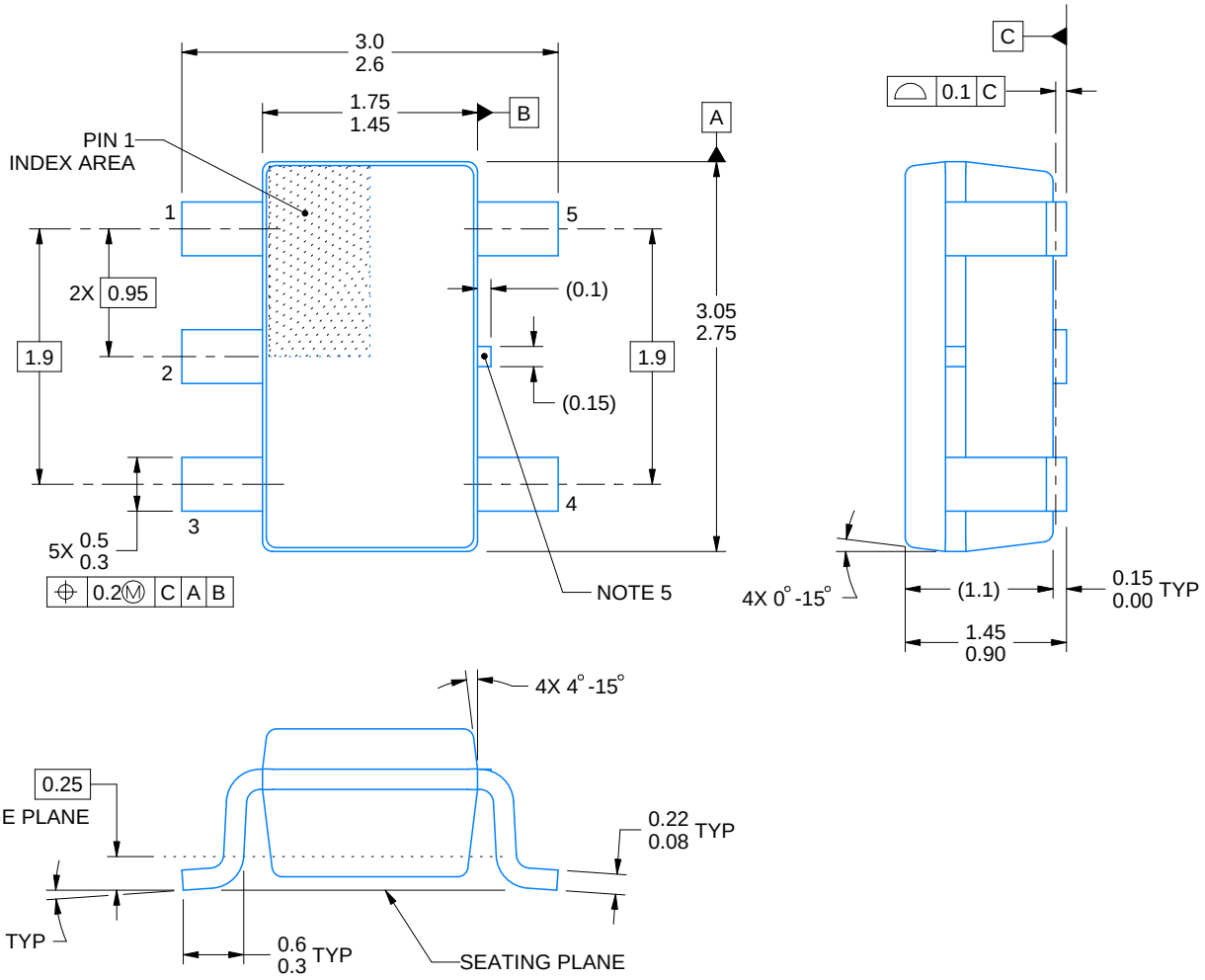
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2068CDGN.B	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2069CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2069CDGN	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2069CDGN-2	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2069CDGN-2.A	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2069CDGN.A	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2069CDGN.A	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2069CDGN.B	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2069CDGN.B	DGN	HVSSOP	8	80	330	6.55	500	2.88

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

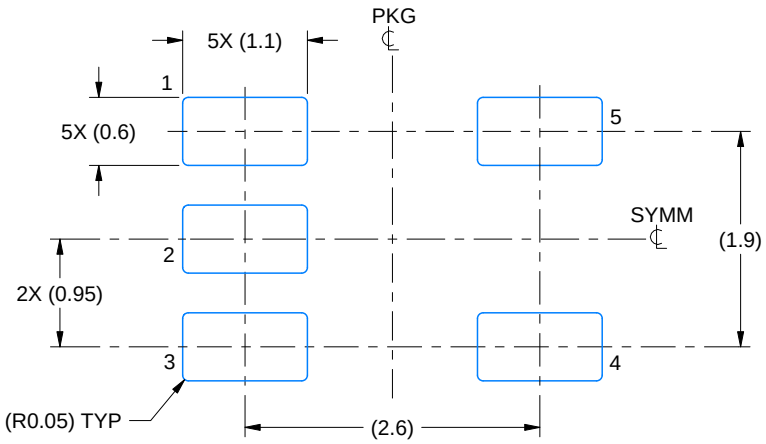
SMALL OUTLINE TRANSISTOR



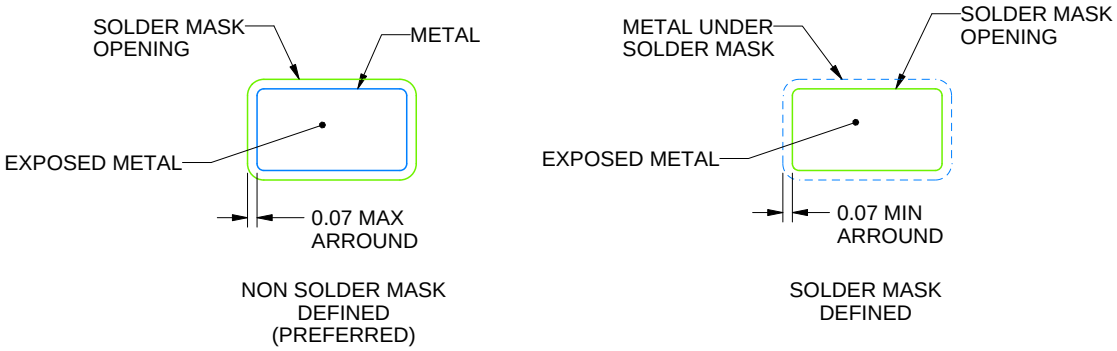
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

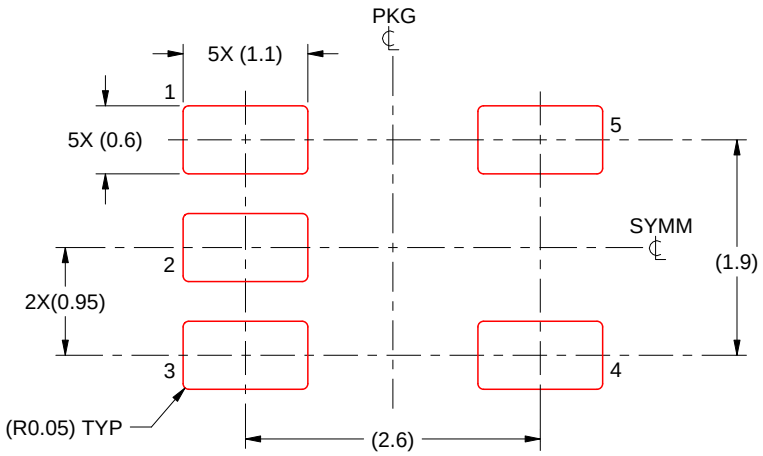


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

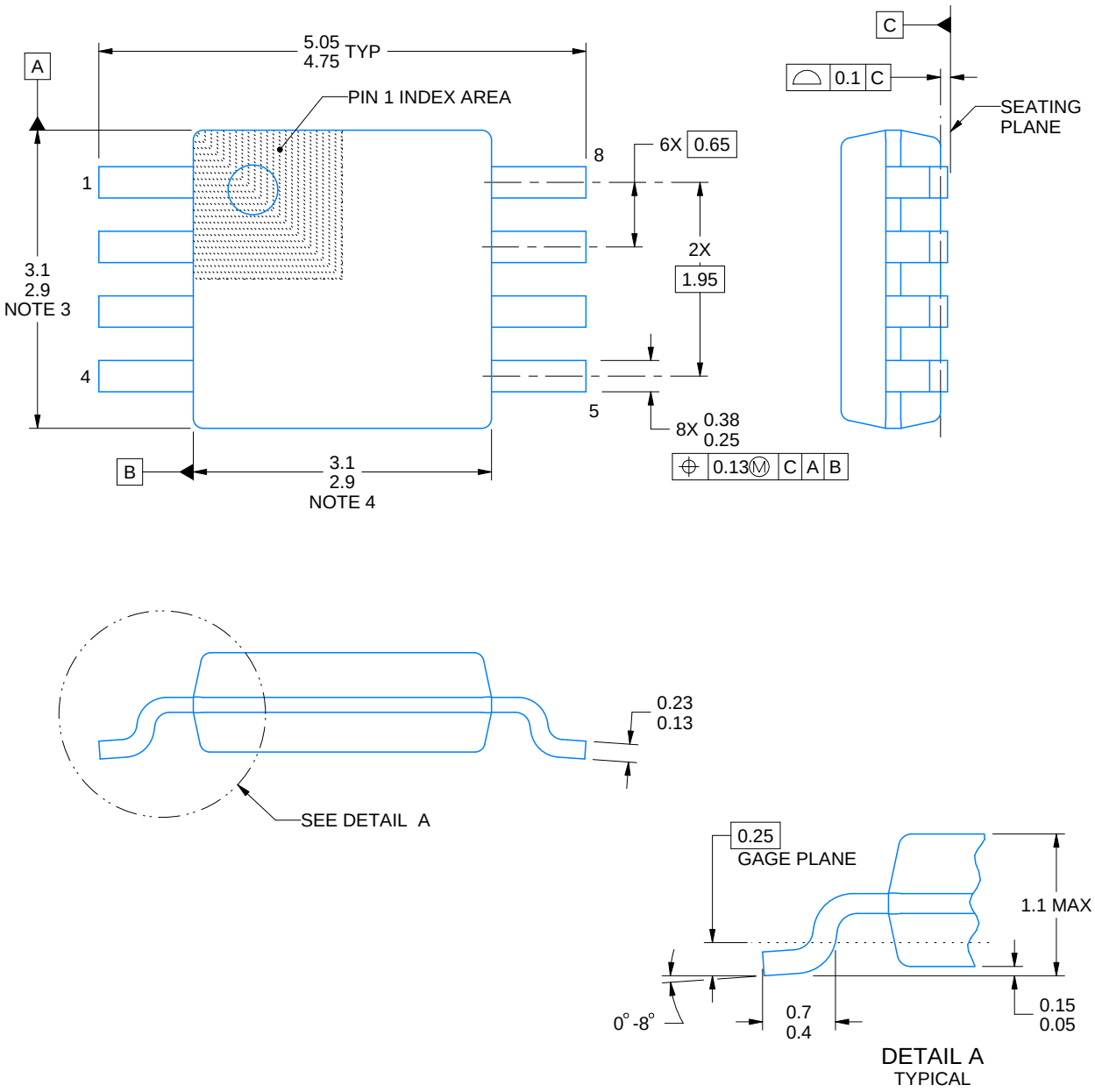
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

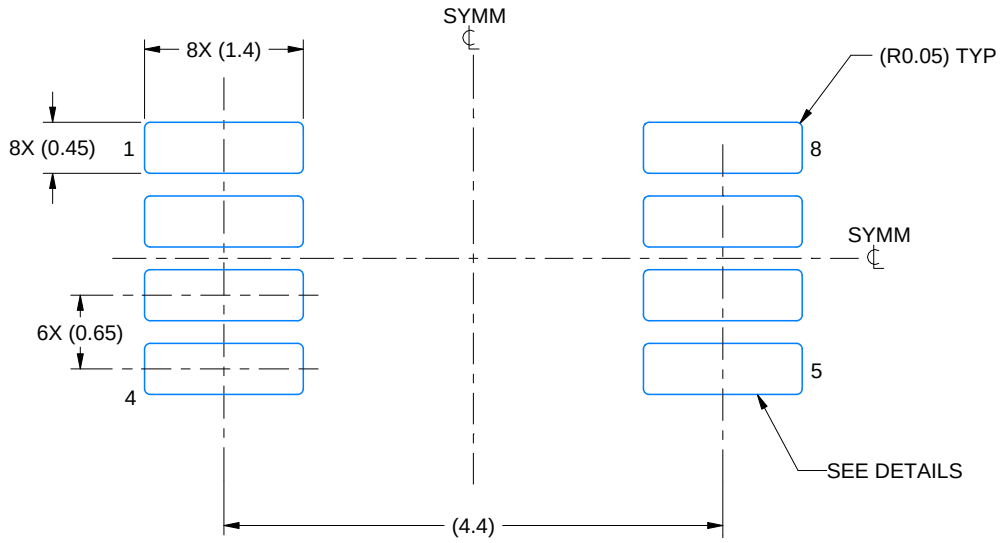
SMALL OUTLINE PACKAGE



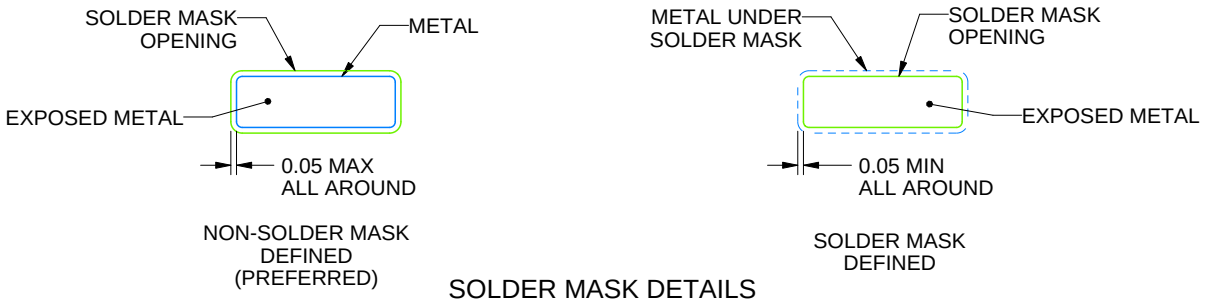
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

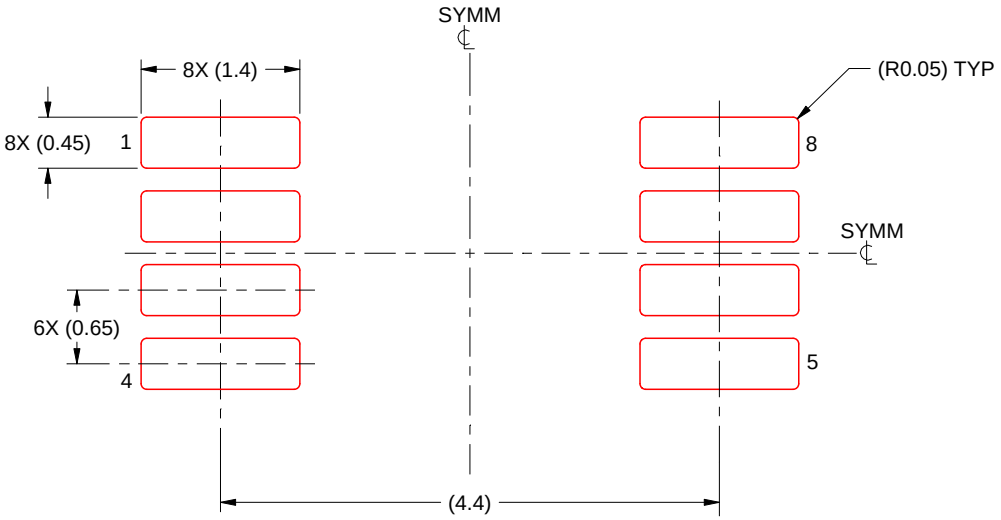


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

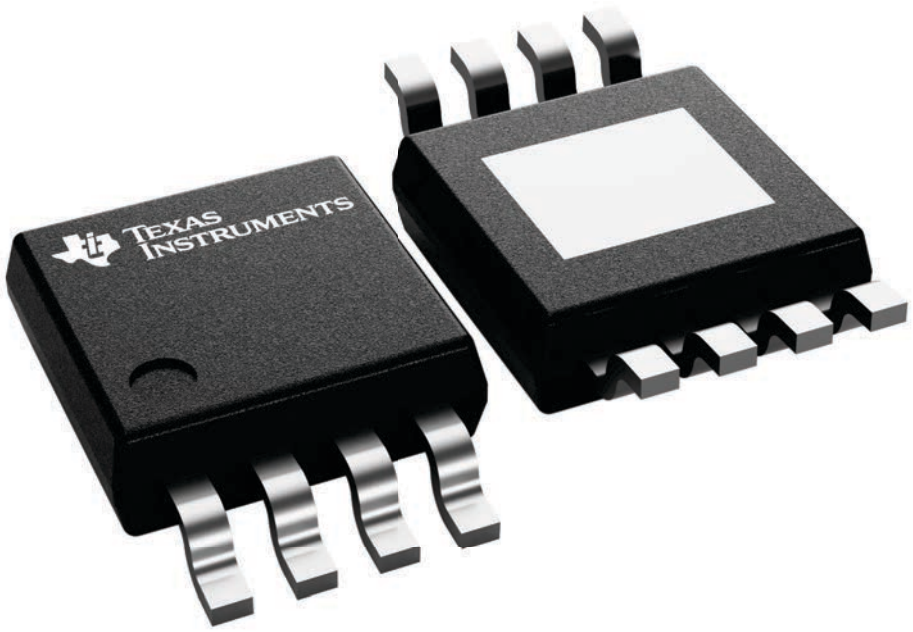
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

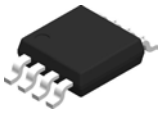
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

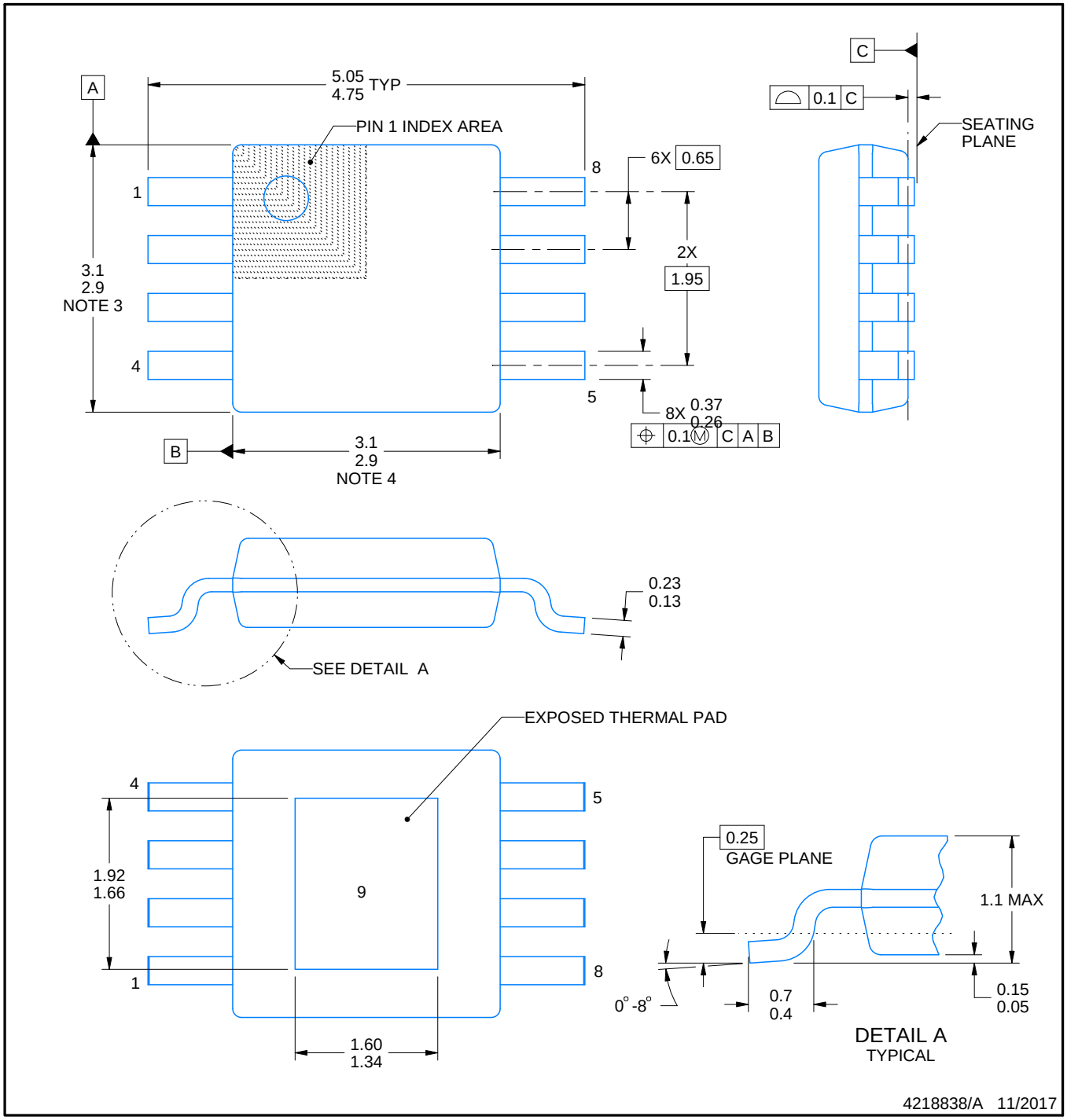
PACKAGE OUTLINE

DGN0008C



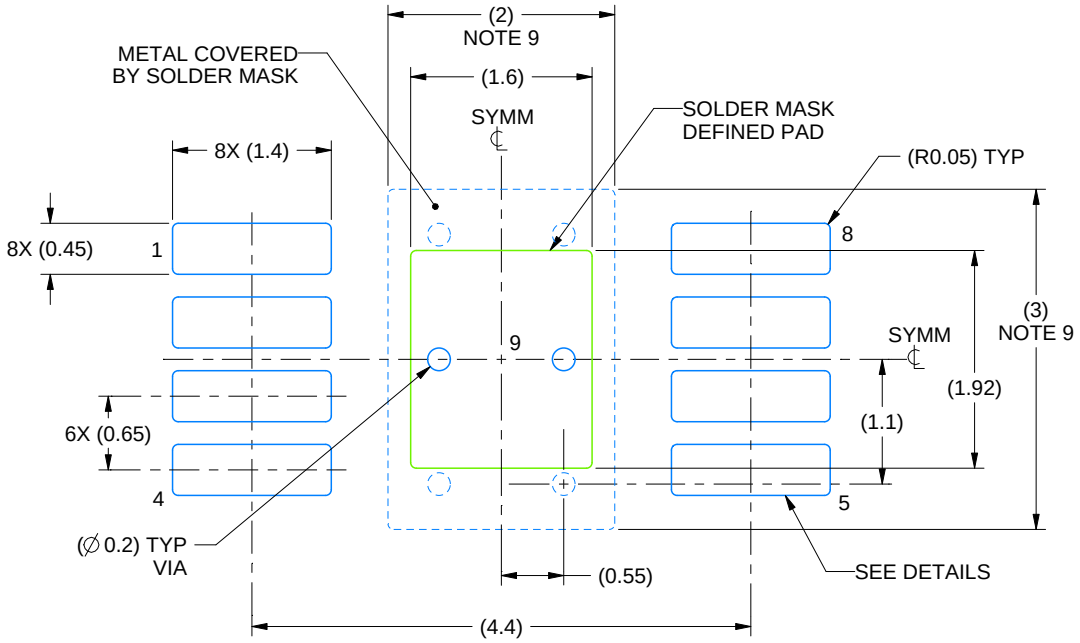
HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

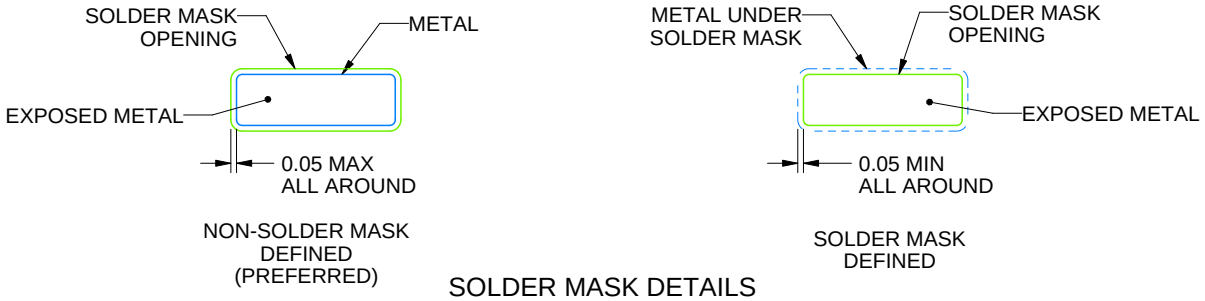


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

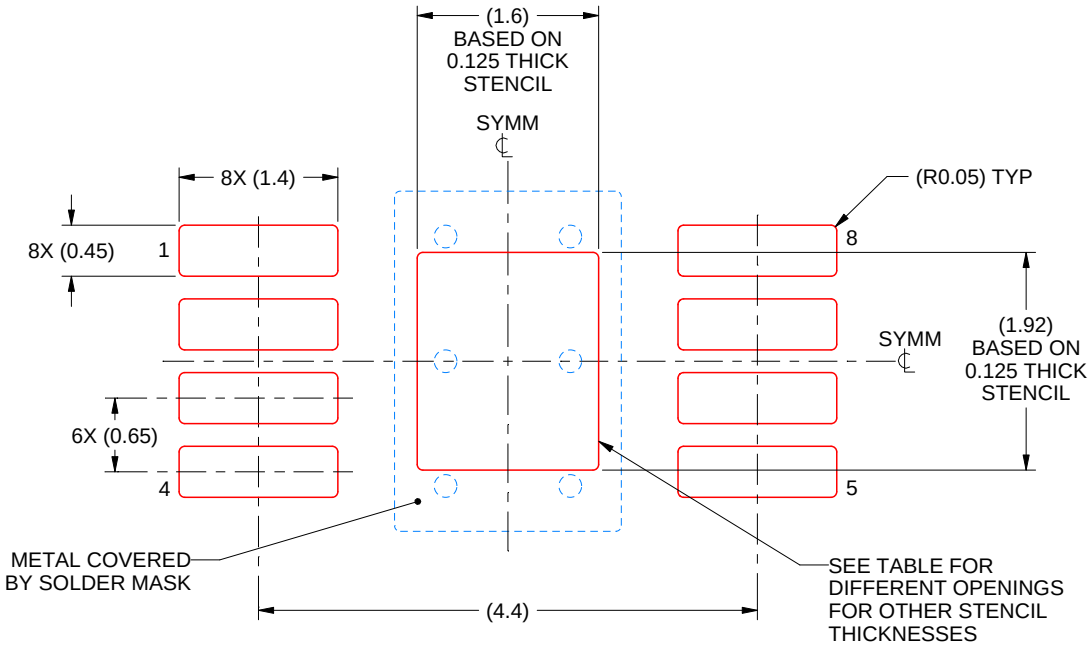


SOLDER MASK DETAILS

4218838/A 11/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.79 X 2.15
0.125	1.60 X 1.92 (SHOWN)
0.15	1.46 X 1.75
0.175	1.35 X 1.62

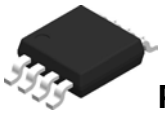
4218838/A 11/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

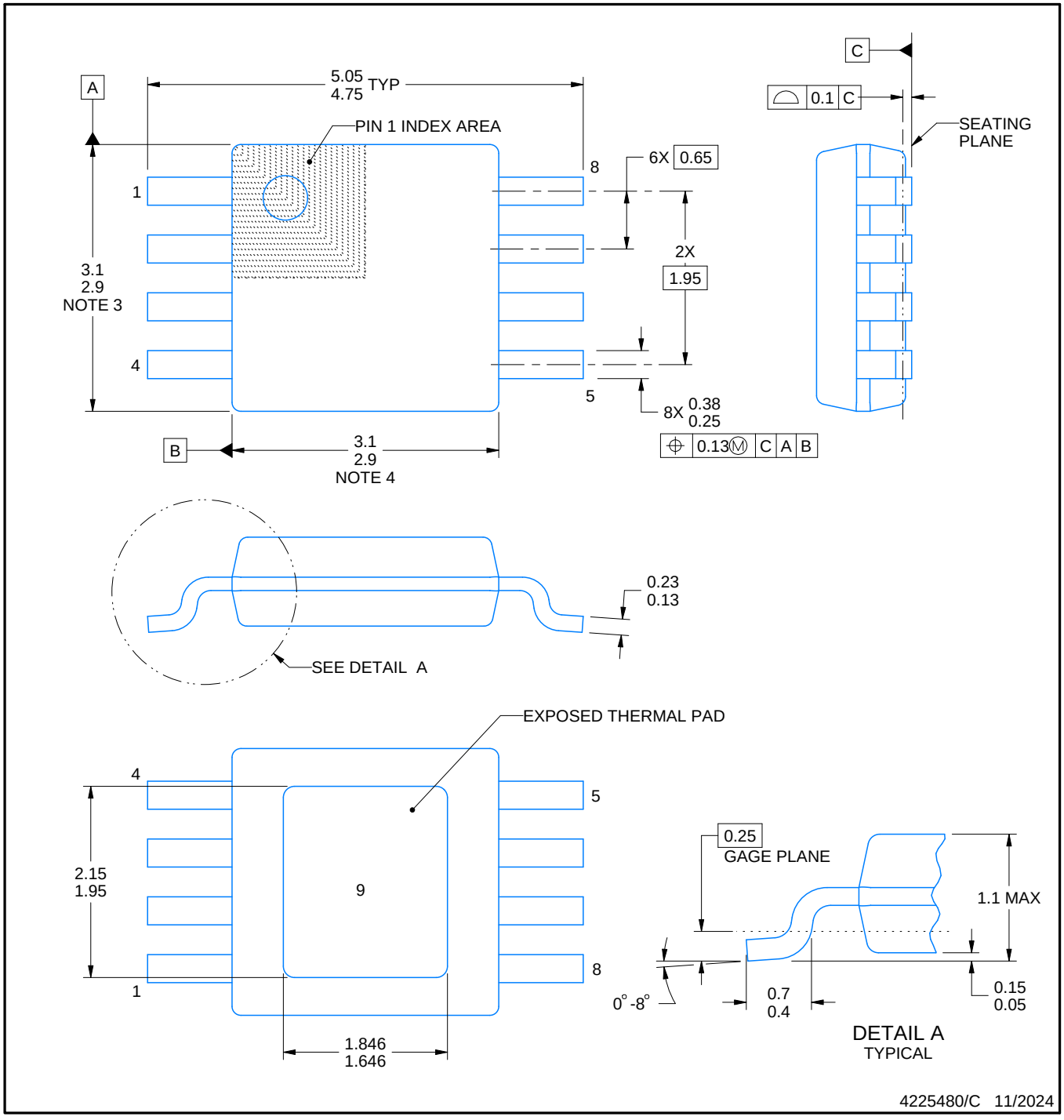
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

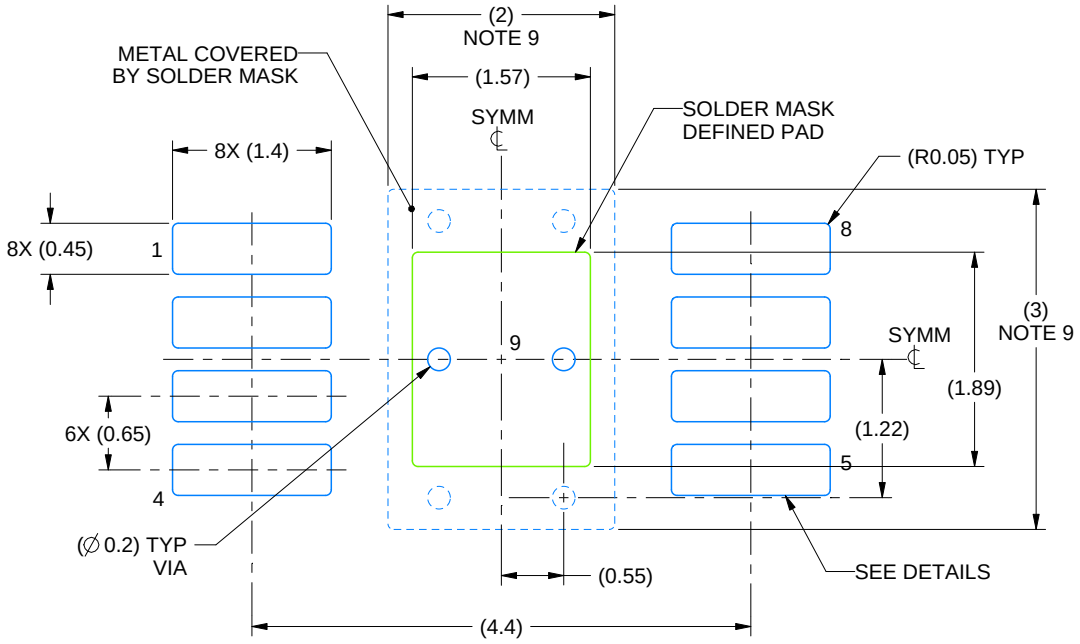
SMALL OUTLINE PACKAGE



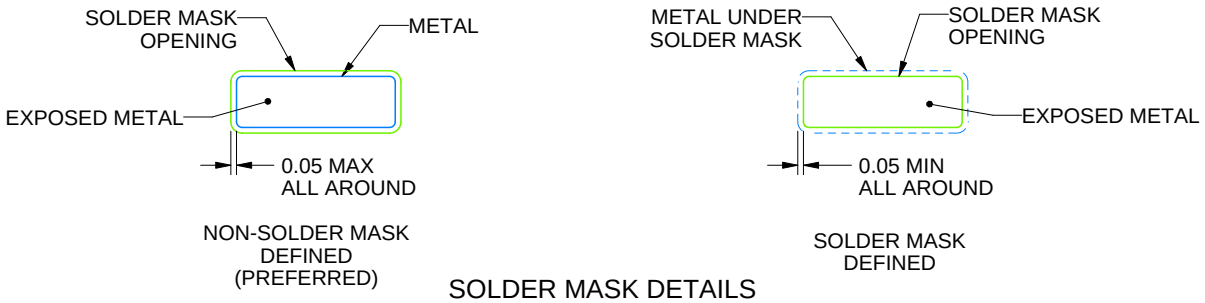
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

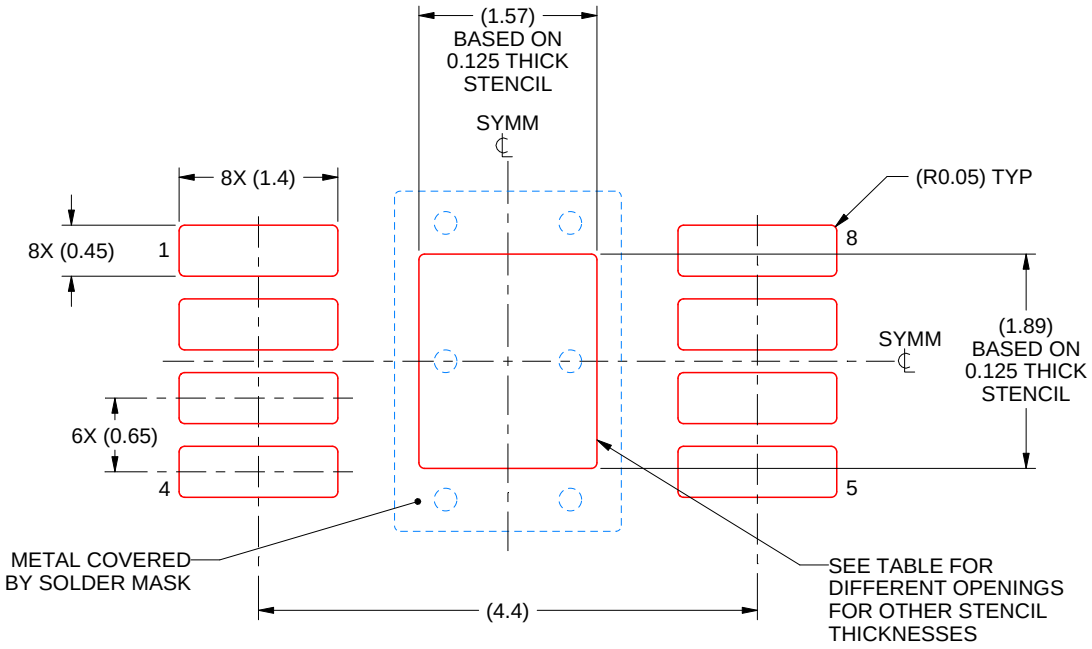


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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