TPS22991L02 5.5V, 2A, 22mΩ On-Resistance Ultra Low IQ Load Switch With Quick Output discharge

1 Features

- Integrated Single Channel Load Switch
- Input operating voltage range (VIN): 1.05V – 5.5V
- Low On-Resistance (R_{ON})
  - R_{ON} = 18.6mΩ (Typ) at VIN ≥ 3.3V
  - R_{ON} = 20.1mΩ (Typ) at VIN = 1.8V
  - R_{ON} = 23.3mΩ (Typ) at VIN = 1.05V
- Low power consumption:
  - ON state (I_Q): 90nA (typ.)
  - OFF state (I_{SD}): 1.6nA (typ.)
- Maximum continuous current: 2A
- Controlled Turn on time of 130µs
- Quick Output Discharge (QOD): 235Ω (typ.)
- Thermal shutdown for self protection
- Smart EN pin pulldown ($R_{PD,EN}$):
- – EN ≥ VIH (I_{ON}): 25nA (max.)
  – EN ≤ VIL ($R_{PD,ON}$): 530kΩ (typ)
- Ultra small Wafer Chip Scale Package
  - 0.616mm × 0.616mm , 0.35mm pitch, 0.35mm Height DSBGA(YCJ)
- ESD performance tested per JESD 22
  - 2kV HBM and 1kV CDM

2 Applications

- Notebook PC
- Tablets
- Wearable technology
- Digital Cameras
- Gaming Consoles
- Solid State Drives

3 Description

The TPS2291L02 is a compact low IQ, low R_{ON} load switch with controlled turn on time . The device contains an N-channel MOSFET that can operate over an input voltage range of 1.05V to 5.5V and can support a maximum continuous current of 2A. The switch is controlled by an on and off input (EN), which is capable of interfacing directly with low voltage control signals. The TPS2291L02 also has a Quick Output Discharge when the switch is turned off, pulling the output voltage down to a known 0V state. The switch is controlled by an on and off input, which is capable of interfacing directly with low-voltage control signals.

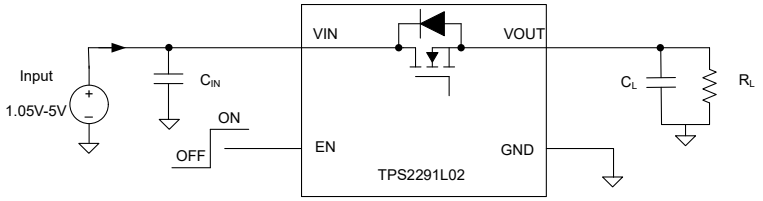
The small size and low RON makes the device designed for being use in space-constrained, battery-powered applications. The wide input voltage range of the switch makes the device a versatile design for many different voltage rails. The controlled rise time of the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The TPS2291L02 further reduces the total system size by integrating a pulldown resistor for quick output discharge (QOD) when the switch is turned off.

The TPS2291L02 is available in a small, space-saving 0.616mm × 0.616mm, 0.35mm pitch, 0.35mm height 4-pin Wafer-Chip-Scale (DSBGA) package (YCJ). The device is characterized for operation over the free-air temperature range of –40°C to +105°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS2291L02	YCJ (DSBGA, 4)	0.616mm × 0.616mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

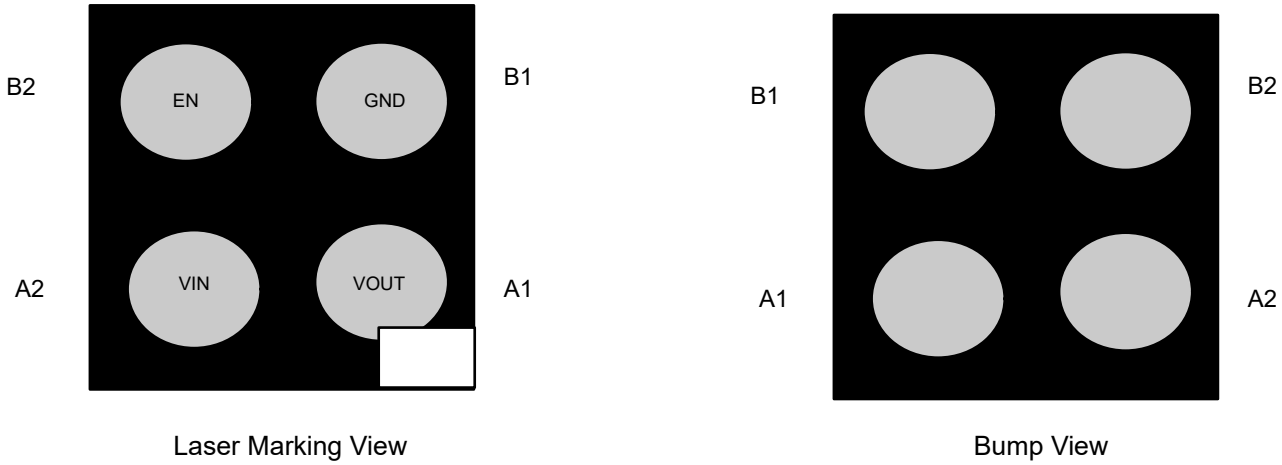


Figure 4-1. TPS2291L02 YCJ, 4-Pin WCSP Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VIN	A2	Input	Switch input. Place a ceramic bypass capacitor between this pin and GND
VOUT	A1	Output	Switch output
EN	B2	Input	Active high control input
GND	B1	Ground	Device Ground

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{VIN}	Maximum Input Voltage Range	–0.3	6	V
V_{VOUT}	Maximum Output Voltage Range	–0.3	6	V
V_{EN}	Maximum EN Pin Voltage Range	–0.3	6	V
I_{MAX}	Maximum Continuous Current		2	A
I_{PLS}	Maximum Pulsed Current (2 ms, 2% Duty Cycle)		2.5	A
T_J	Junction temperature	–40	125	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime..

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less is possible with the necessary precautions. Pins listed may actually have higher performance.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{VIN}	Input Voltage Range	1.05		5.5	V
V_{VOUT}	Output Voltage Range	0		5.5	V
V_{IH}	EN Pin High Voltage Range	0.8		5.5	V
V_{IL}	EN Pin Low Voltage Range	0		0.35	V
T_A	Ambient temperature	-40		105	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS2291L02	UNIT
		YCJ	
		4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	216	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	79	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

Test conditions values are at -40℃ ≤T_J ≤ 105℃, VIN = 3.3V, VOUT= Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Input Supply (VIN)							
$I_{Q, VIN}$	VIN Quiescent Current	$V_{EN} \geq V_{IH}$, VOUT = Open	25°C		90	225	nA
			-40°C to 85°C			330	nA
			T_A = 105°C		200		nA
$I_{SD, VIN}$	VIN Shutdown Current	$V_{EN} \leq V_{IL}$, VOUT = Open	25°C		1.5	12	nA
			-40°C to 65°C			150	nA
			T_A = 105°C		33		nA
ON-Resistance (RON)							
R_{ON}	ON-State Resistance	VIN = 3.3 V	25°C		22	27	mΩ
			-40°C to 85°C			40	mΩ
			T_A = 105°C		30		mΩ
Thermal Protection							
T_{SD}	Thermal Shutdown		Rising		175		℃
			Falling		153		℃
Enable Pin (ON)							
I_{EN}	EN Pin Leakage	$V_{EN} \geq V_{IH}$	25°C		1	11	nA
			-40°C to 85°C			15	nA
			T_A = 105°C		3.5		nA
$R_{PD, EN}$	Smart Pull Down Resistance		-40°C to 105°C		530		kΩ
$V_{IH,EN}$	EN Pin Threshold (VIH Rising)		-40°C to 105°C			0.8	V
$V_{Hys,EN}$	EN Pin Threshold (Hysteresis)		-40°C to 105°C		0.124		V
$V_{IL,EN}$	EN Pin Threshold (VIL Falling)		-40°C to 105°C	0.35			V
Quick-output Discharge (QOD)							
R_{QOD}	QOD Pin Internal Discharge Resistance	1.05V ≤VIN ≤ 5.5V	-40°C to 105°C		235	350	Ω

5.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table apply to an ambient temperature of 25°C, C_{IN} = 1µF and a load of C_L = 0.1µF, R_L = 10Ω. Timing parameter measurement details are shown in the timing diagram in the datasheet.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	VIN = 5.0 V		126		µs
		VIN = 3.3 V		123		µs
		VIN = 1.8 V		138		µs
		VIN = 1.05 V		205		µs
t_R	Output Rise Time	VIN = 5.0 V		15.5		µs
		VIN = 3.3 V		18		µs
		VIN = 1.8 V		22		µs
		VIN = 1.05 V		51		µs
t_D	Delay Time	VIN = 5.0 V		123		µs
		VIN = 3.3 V		116.5		µs
		VIN = 1.8 V		128		µs
		VIN = 1.0 V		182		µs

Unless otherwise noted, the typical characteristics in the following table apply to an ambient temperature of 25°C, C_{IN} = 1µF and a load of C_L = 0.1µF, R_L = 10Ω. Timing parameter measurement details are shown in the timing diagram in the datasheet.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFF}	Turn OFF Time	VIN = 5.0 V		1.6		µs
		VIN = 3.3 V		2		µs
		VIN = 1.8 V		2		µs
		VIN = 1.0 V		2.5		µs
t_F	Output Fall Time	VIN = 5.0 V		2.3		µs
		VIN = 3.3 V		2.2		µs
		VIN = 1.8 V		2.2		µs
		VIN = 1.0 V		2.1		µs

5.7 Typical Characteristics

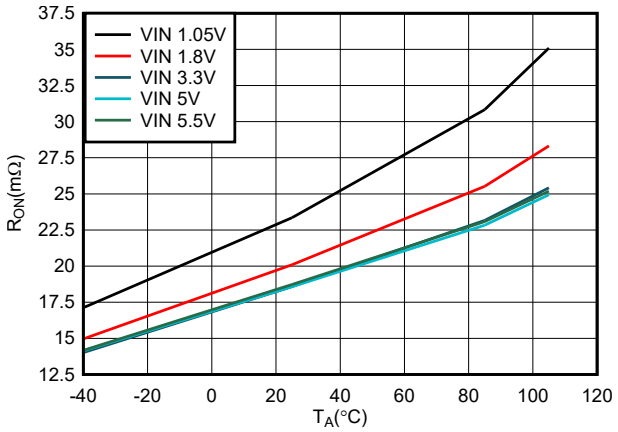


Figure 5-1. On-Resistance vs Temperature

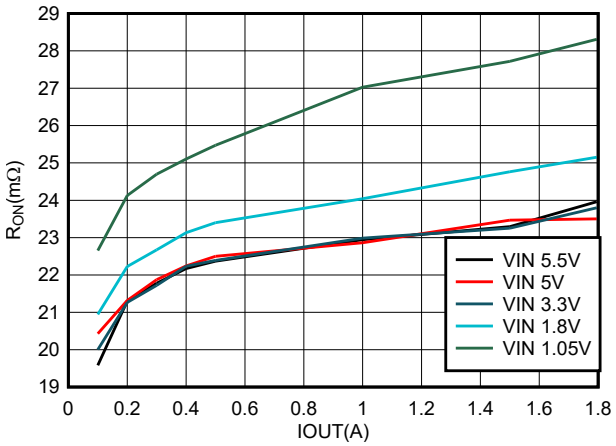


Figure 5-2. On-Resistance vs IOUT

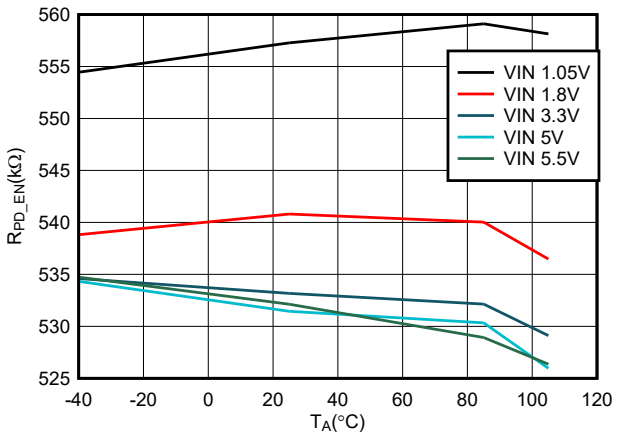


Figure 5-3. R_{PD_EN} Temperature

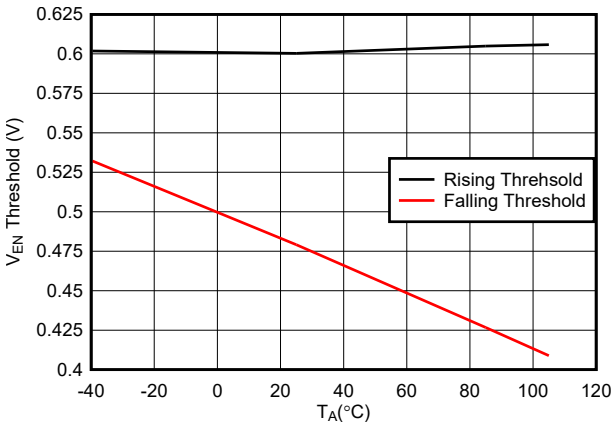


Figure 5-4. EN Pin Thresholds vs Temperature

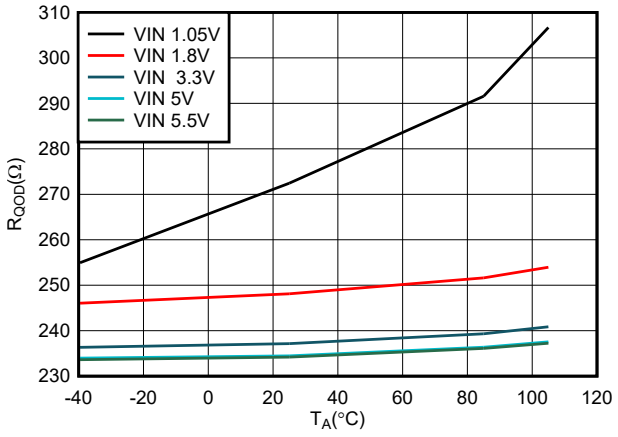


Figure 5-5. QOD Resistance vs Temperature

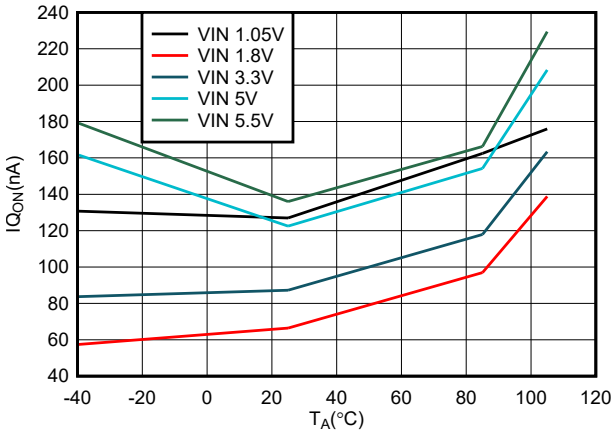


Figure 5-6. IQ(ON) vs Temperature

5.7 Typical Characteristics (continued)

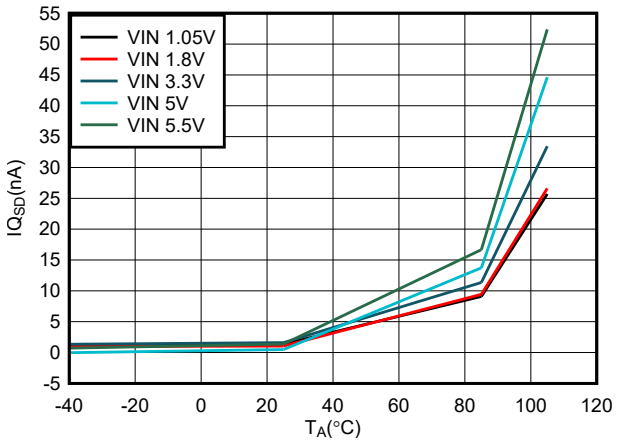
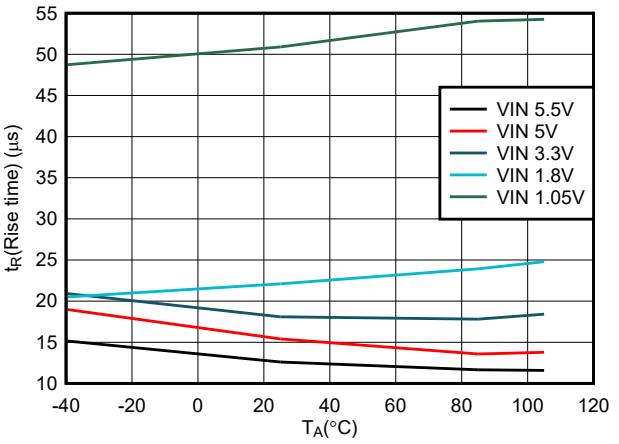
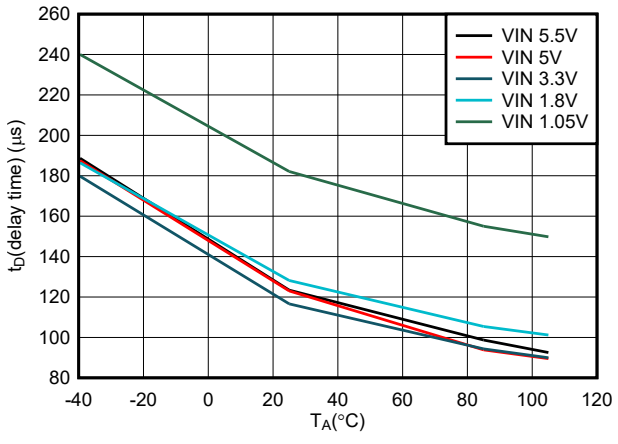


Figure 5-7. IQ(SD) Current vs Temperature



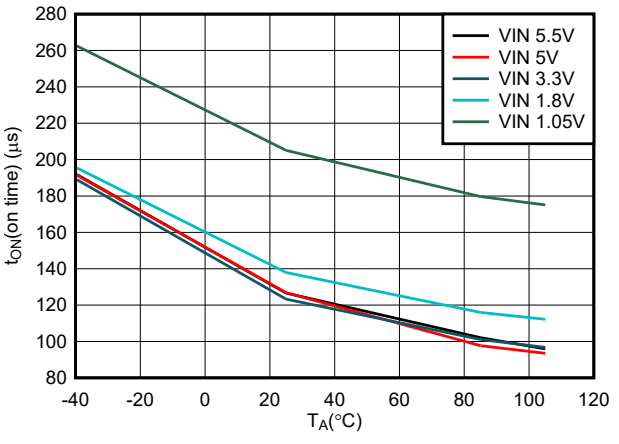
C_L = 0.1µF R_L = 10Ω C_{IN}= 1µF

Figure 5-8. Rise Time (t_R)vs Temperature



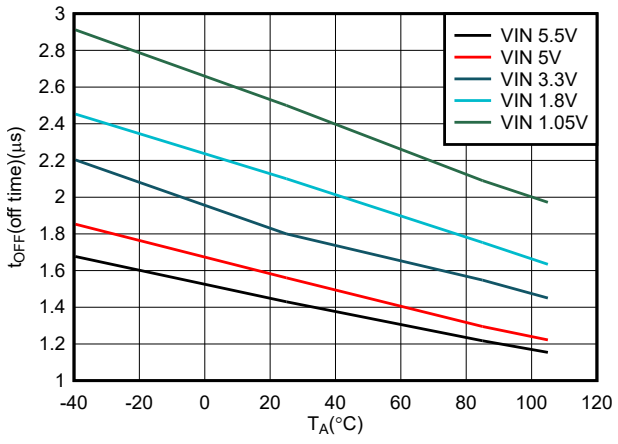
C_L = 0.1µF R_L = 10Ω C_{IN}= 1µF

Figure 5-9. Delay Time (t_D) vs Temperature



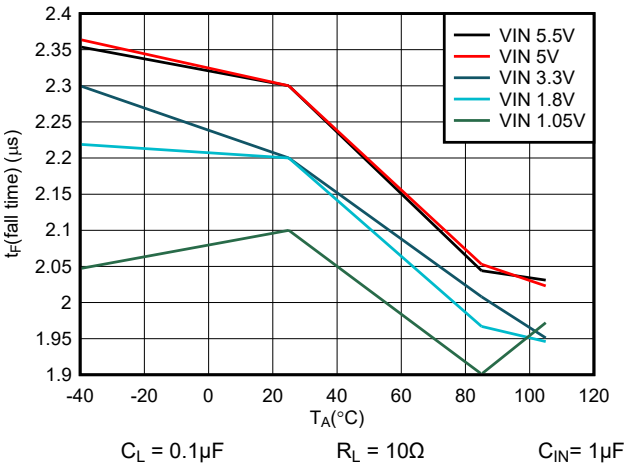
C_L = 0.1µF R_L = 10Ω C_{IN}= 1µF

Figure 5-10. Turn-On Time (T_{ON}) vs Temperature



C_L = 0.1µF R_L = 10Ω C_{IN}= 1µF

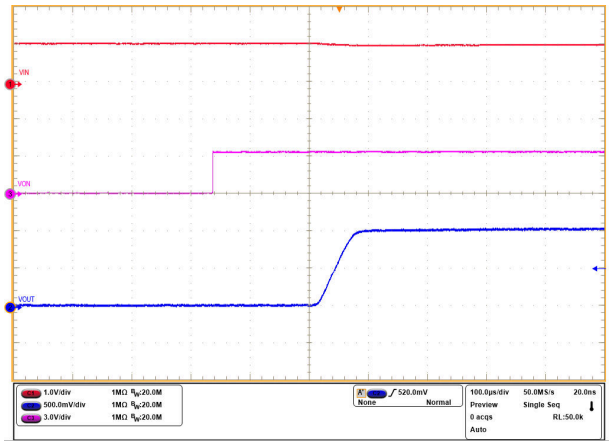
Figure 5-11. Turn-off time t_{Off} Time vs Temperature



C_L = 0.1µF R_L = 10Ω C_{IN}= 1µF

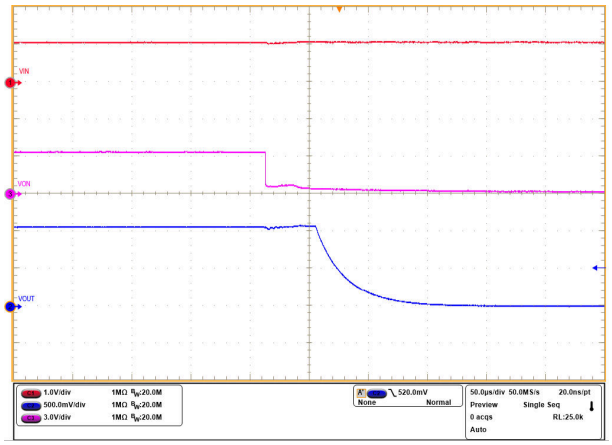
Figure 5-12. Fall Time (t_F) vs Temperature

5.7 Typical Characteristics (continued)



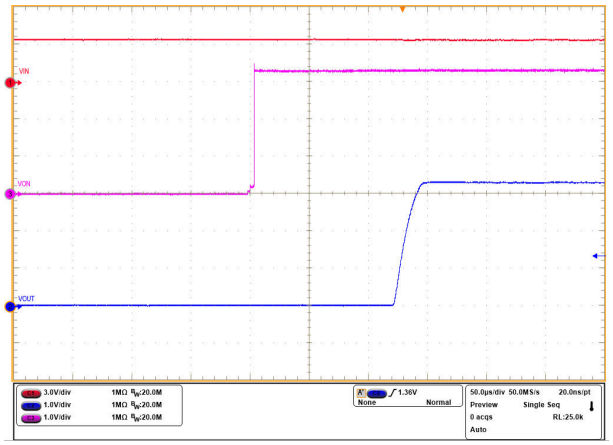
C_{IN}=1µF C_L = 0.1µF

Figure 5-13. t_R at VIN = 1.05V



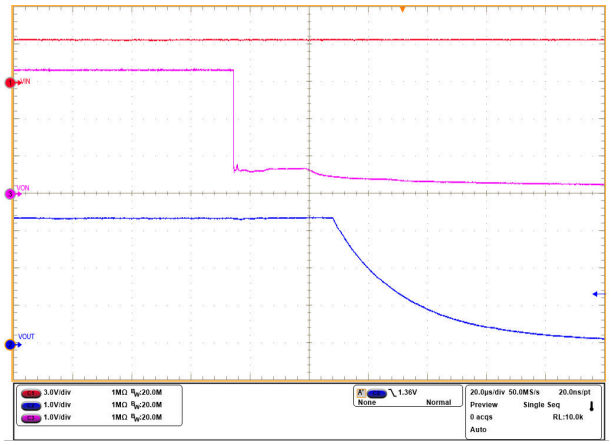
C_{IN}=1µF C_L = 0.1µF

Figure 5-14. t_F at VIN = 1.05V



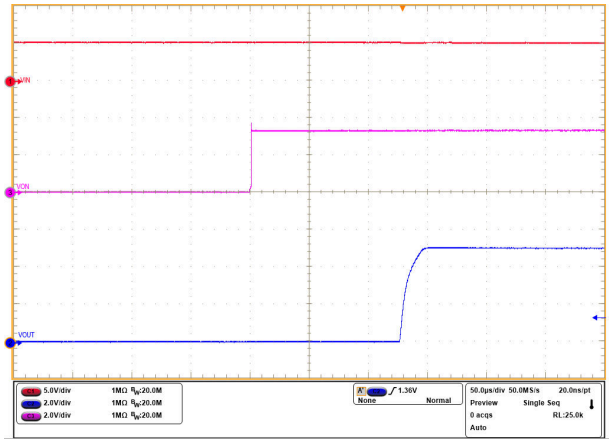
C_{IN}=1µF C_L = 0.1µF

Figure 5-15. t_R at VIN = 3.3V



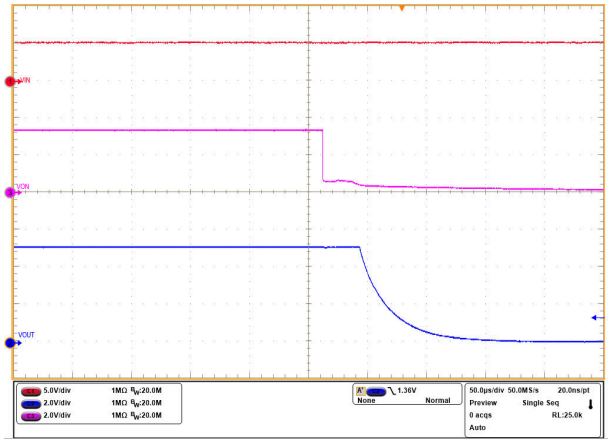
C_{IN}=1µF C_L = 0.1µF

Figure 5-16. t_F at VIN = 3.3V



C_{IN}=1µF C_L = 0.1µF

Figure 5-17. t_R at VIN = 5V



C_{IN}=1µF C_L = 0.1µF

Figure 5-18. t_F at VIN = 5V

6 Parameter Measurement Information

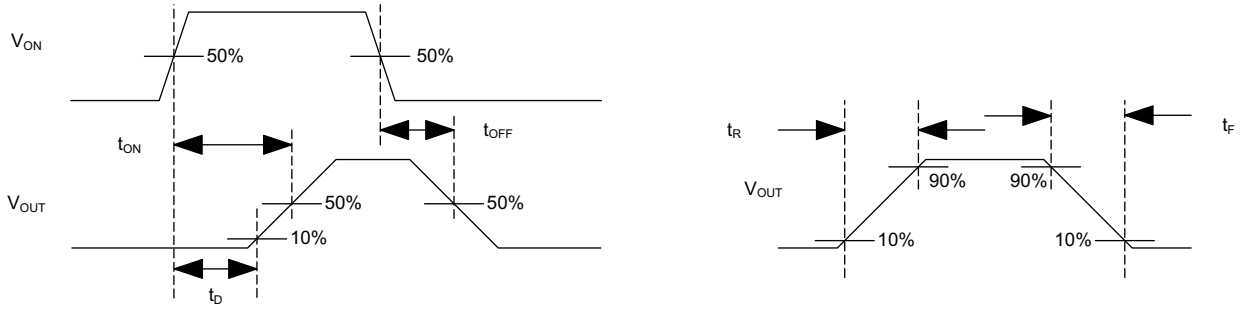


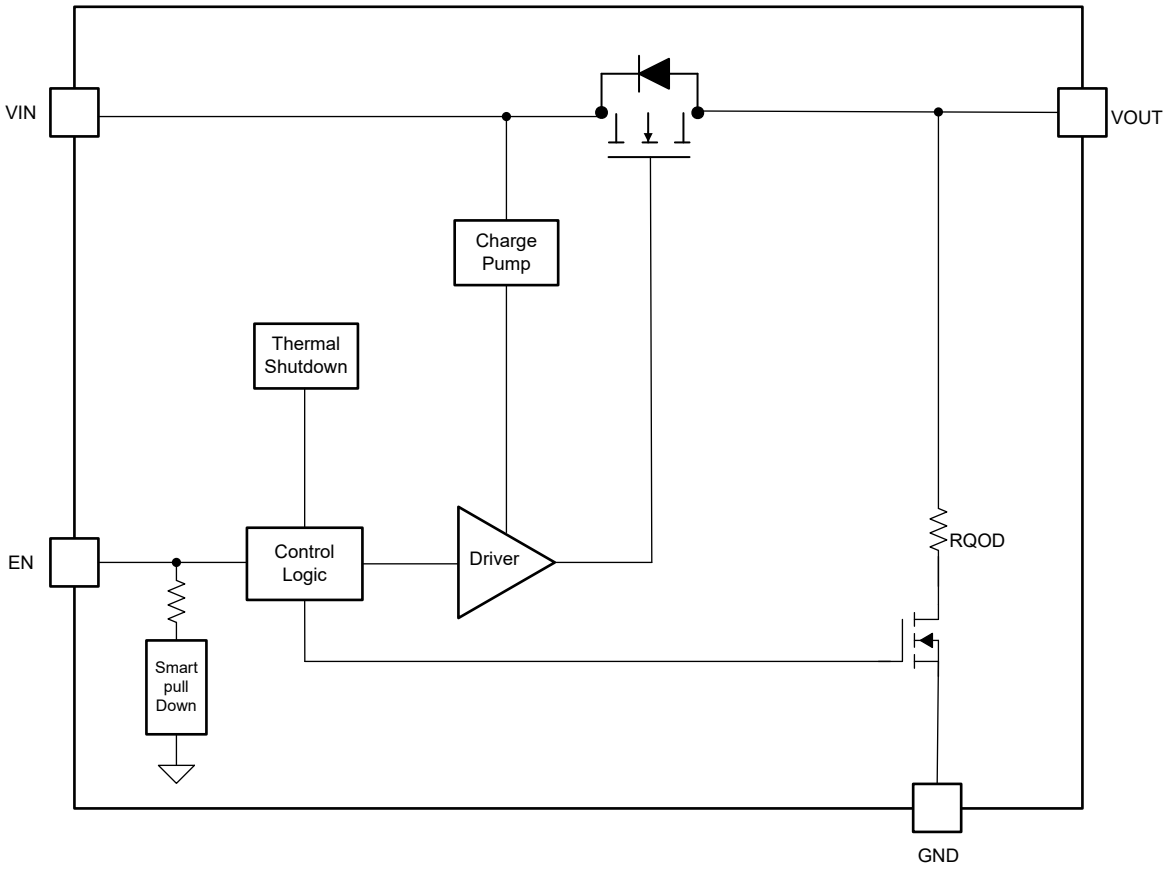
Figure 6-1. TPS2291L02 Timing Parameters

7 Detailed Description

7.1 Overview

The TPS2291L02 is a 5.5V, 2A load switch in a 4-pin WCSP package with 0.35mm pin pitch option. To reduce voltage drop for low voltage and high-current rails, the device implements a low-resistance N-channel MOSFET, which reduces the dropout voltage through the device. The device has a controlled rise time , which helps reduce or eliminate power supply droop because of large inrush currents. The TPS2291L02 also integrates a Quick Output Discharge circuit that is activated when the switch is turned off, pulling the output voltage down to a known 0V state. TPS2291L02 increases circuit robustness by integrating thermal shutdown that protects the device in high-temperature conditions. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components, which reduces system size and bill of materials (BOM) count.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 ON and OFF Control

The EN pin controls the state of the switch. The EN pin is compatible with standard GPIO logic threshold so the device can be used in a wide variety of applications. When power is first applied to VIN, a Smart Pulldown is used to keep the EN pin from floating until the system sequencing is complete. After the EN pin is deliberately driven high (≥ V_{IH}), the Smart Pulldown is disconnected to prevent unnecessary power loss. See the below table when the EN Pin Smart Pulldown is active.

Table 7-1. EN Pin Control

ON Pin Voltage	ON Pin Function
≤ V_{IL}	Pulldown active
≥ V_{IH}	No pulldown

7.3.2 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1µF ceramic capacitor, C_{IN}, placed close to the pins, is typically sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, use an input capacitor approximately 10 times higher than the output capacitor to avoid excessive voltage drop

7.3.3 Reference

Due to the integrated body diode in the MOSFET, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause VOUT to exceed VIN when the system supply is removed. This can result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing VIN dip caused by inrush currents during startup.

7.3.4 Quick Output Discharge

TPS2291L02 integrates Quick Output Discharge. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor prevents the output from floating while the switch is disabled

7.3.5 Thermal Shutdown

When the device temperature reaches 175°C (typical), the device shuts off to prevent thermal damage. After the device cools off by about 22°C, the device turns back on. If the device is kept in a thermally stressful environment, then the device oscillates between these two states until the device can keep the temperature below the thermal shutdown point.

7.4 Device Functional Modes

Table 7-2. Device Functional Modes

EN	Fault Condition	VOUT State
L	N/A	Hi-Z
H	None	VIN through R_{ON}
X	Thermal shutdown	Hi-Z

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

This section highlights some of design considerations for implementing the device in various applications.

Standby Power Reduction

Battery powered end equipments often have strict power budgets, in which there is a need to reduce current consumption. The TPS2291L02 significantly reduces system current consumption by disabling the supply voltage to subsystems in standby states. Alternatively, the TPS2291L02 reduces the leakage current overhead of the modules in standby mode as shown inFigure 8-1 . Additionally the small form factor of TPS2291L02 allows it to be used in space constrained battery operated devices.

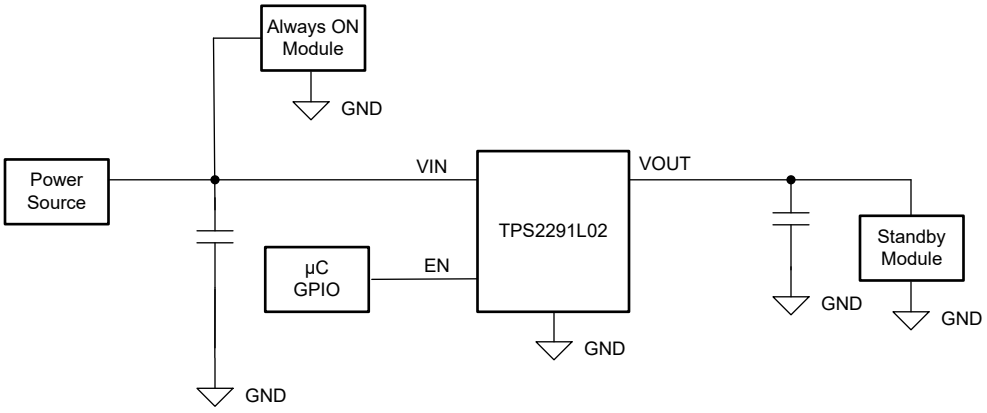


Figure 8-1. Standby Power Reduction Illustrative Diagram

8.2 Typical Application

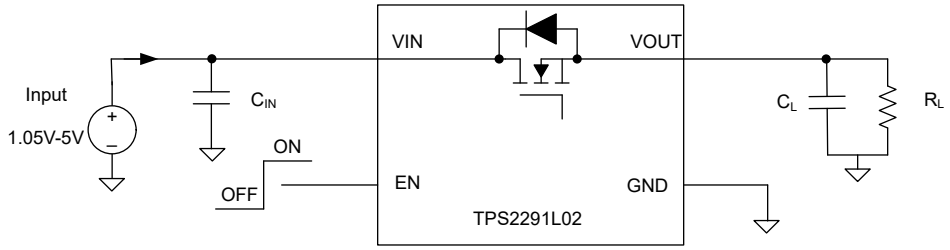


Figure 8-2. Typical Application Diagram

8.2.1 Design Requirements

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VIN	5.5V
C_L	22µF

8.2.2 Detailed Design Procedure

The input to output voltage drop in the device is determined by the RON of the device and the load current. The RON of the device depends upon the VIN condition of the device. After the RON of the device is determined based upon the VIN condition, use the below equation to calculate the input to output voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON} \quad (1)$$

where

- ΔV is the voltage drop from VIN to VOUT.
- ILOAD is the load current.
- RON is the on-resistance of the device for a specific VIN.

An appropriate ILOAD must be chosen such that the IMAX specification of the device is not violated. To determine how much inrush current is caused by the load capacitance, use below equation.

$$I_{INRUSH} = C_L \times dV_{OUT} / dt \quad (2)$$

where

- I_{INRUSH} is amount of inrush current caused by C_L
- C_L is the load capacitance on V_{OUT}
- dt is the rise time for V_{OUT} when the device is enabled
- • dV_{OUT} is change in the V_{OUT} voltage after the device is enabled.

The slew rate of the device dVOUT/dt at a given VIN voltage can be found in the electrical characteristic table for a given version. IINRUSH has to be within the IMAX and IPLS limits.

8.2.3 Application Curves

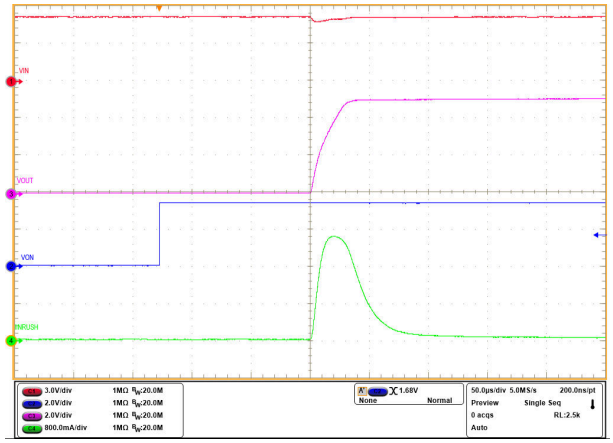


Figure 8-3. Typical Turn On for TPS22991L02 for VIN= 5V and C_L=22µF

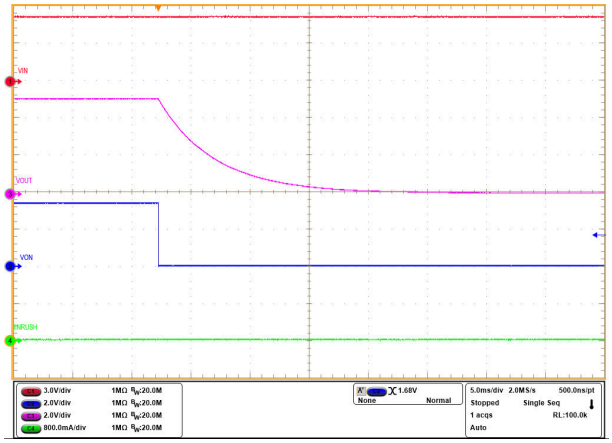


Figure 8-4. Typical Turn OFF for TPS22991L02 for VIN= 5V and C_L=22µF

8.3 Power Supply Recommendations

The TPS2291L02 device is designed to operate with a VIN range of 1.05V to 5.5V. Regulate the VIN power supply well and place as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1µF is sufficient to prevent the supply voltage from drooping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input.

8.4 Layout

8.4.1 Layout Guidelines

- For best performance, all traces must be as short as possible. To be most effective, place the input and output capacitors close to the device to minimize the effects that parasitic trace inductances can have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects
- The VIN pin must be connected with low ESR ceramic bypass capacitors to ground. The typical recommended bypass capacitance is 1µF ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.
- The VOUT pin must be connected with low ESR ceramic bypass capacitors to ground. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor must be placed as close to the device pins as possible.

Thermal Considerations

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, PD(max) for a given output current and ambient temperature, use equation x

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \tag{3}$$

where

- $P_{D(MAX)}$ = maximum allowable power dissipation
- $T_{J(MAX)}$ = maximum allowable junction temperature (125°C for the TPS2291L02)
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. Refer to the *Section 5.4* table. This parameter is highly dependent upon board layout.

8.4.2 Layout Example

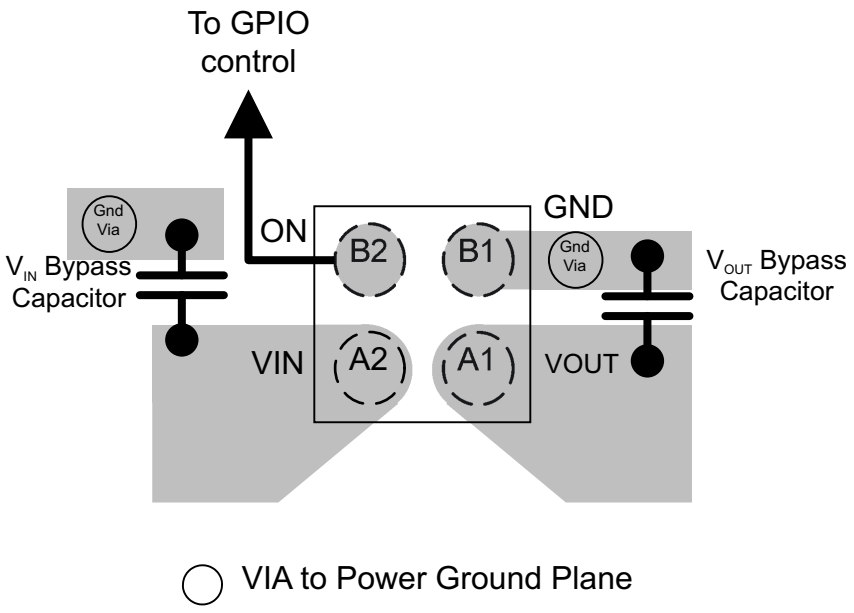


Figure 8-5. TPS2291L02 Layout Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, TPS2291L02 Evaluation Module EVM User's Guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

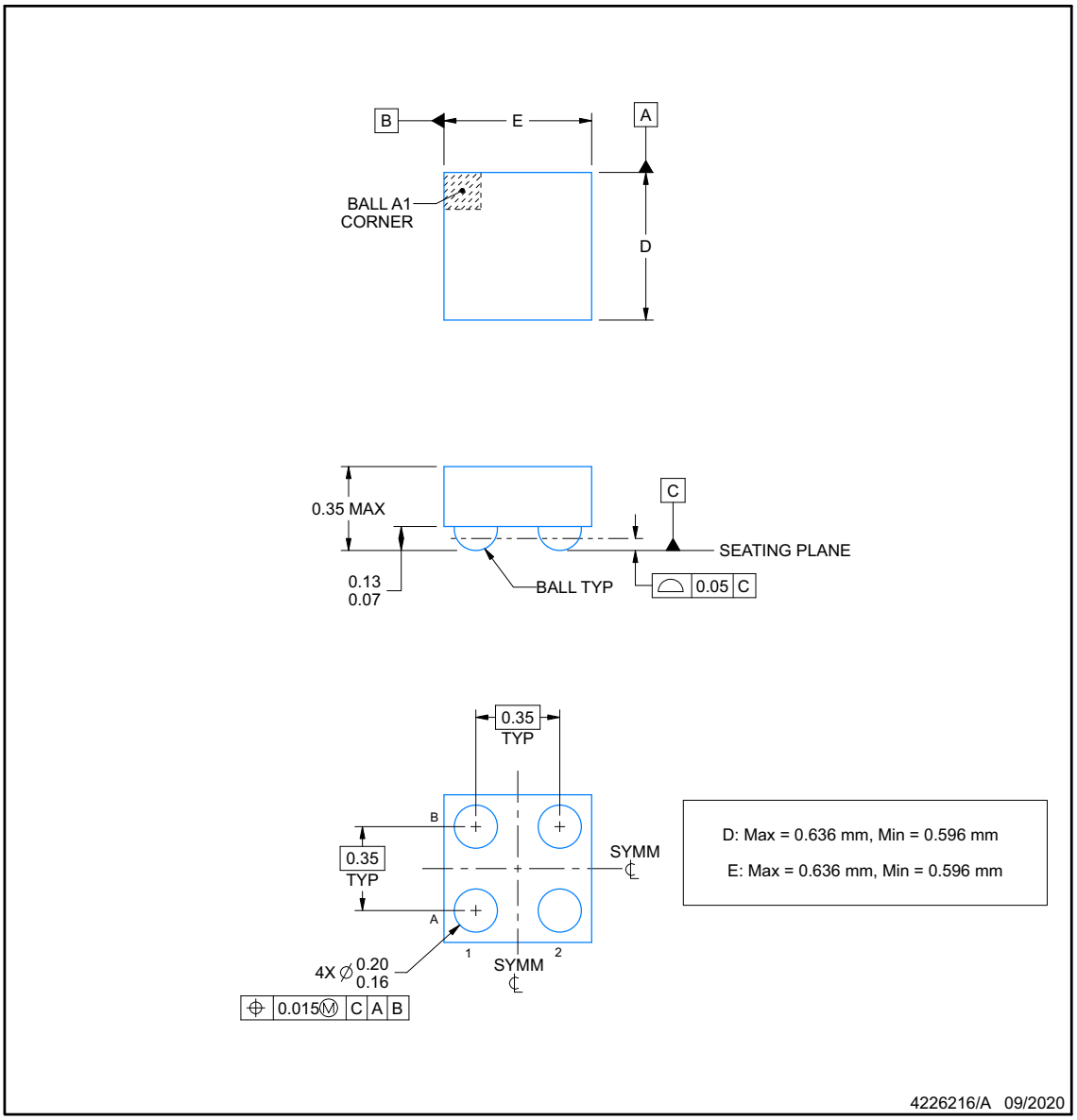
11.1 Mechanical Data

PACKAGE OUTLINE

YCJ0004-C02

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

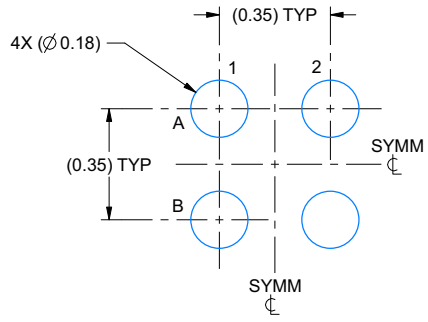
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

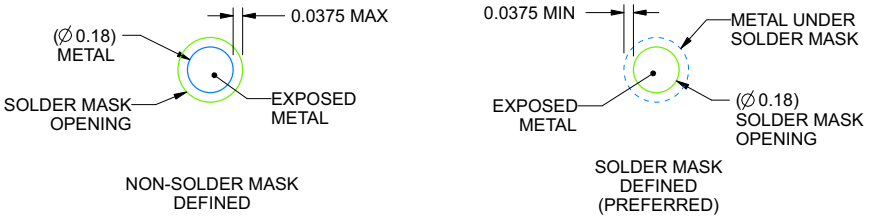
YCJ0004-C02

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4226216/A 09/2020

NOTES: (continued)

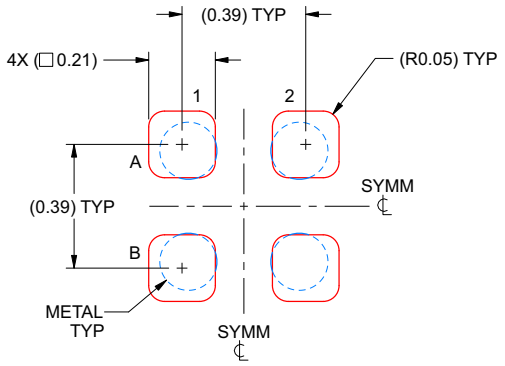
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCJ0004-C02

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4226216/A 09/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2291L02BYCJR	Active	Production	DSBGA (YCJ) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	O

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

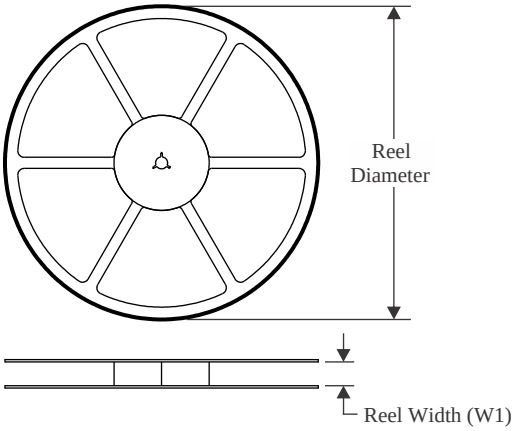
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

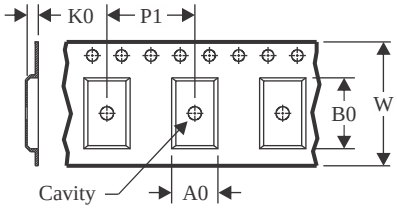
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

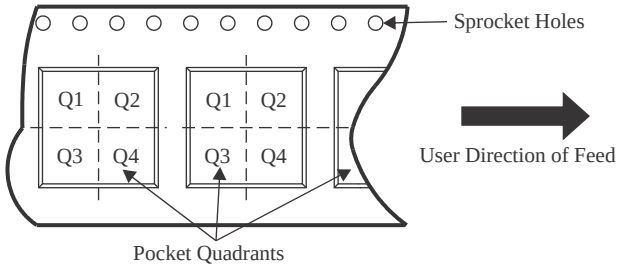


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

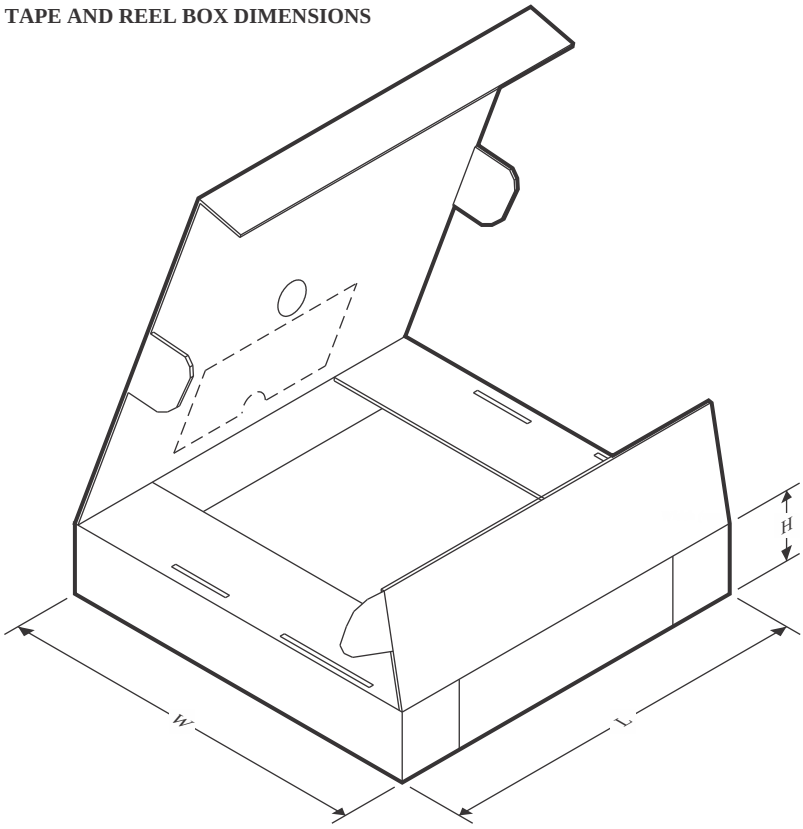
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2291L02BYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2291L02BYCJR	DSBGA	YCJ	4	12000	182.0	182.0	20.0

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