TPS25200 5V eFuse With Precision Adjustable Current Limit and Overvoltage Clamp

1 Features

- 2.5V to 6.5V operation
- Input withstands up to 20V
- 7.6V input overvoltage shutoff
- 5.25V to 5.55V fixed overvoltage clamp
- 0.6µs overvoltage lockout response
- 3.5µs short circuit response
- Integrated 60mΩ high-side MOSFET
- Up to 2.6A continuous load current
- ±6% current-limit accuracy at 2.9A
- Reverse current blocking while disabled
- Built-in soft start
- Pin-to-pin compatible with TPS2553
- UL 2367 recognized
  - File no. 169910
  - R_{ILIM} ≥ 33kΩ (3.12A maximum)

2 Applications

- USB power switches
- USB target devices
- Cell, smart phones
- 3G, 4G wireless data cards
- Solid-state drives (SSD)
- 3V or 5V adapter powered devices

3 Description

The TPS25200 is a 5V eFuse with precision current limit and overvoltage clamp. The device provides robust protection for load and source during overvoltage and overcurrent events.

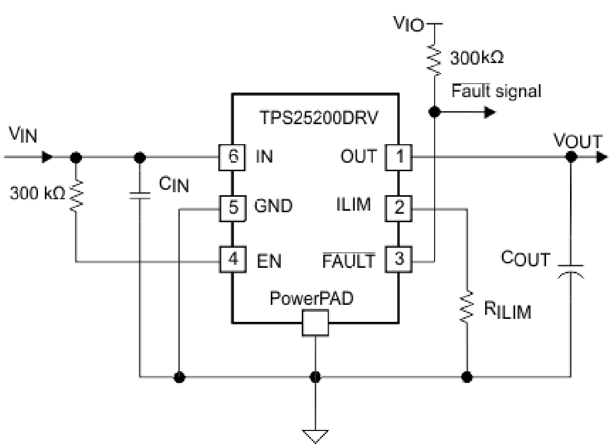
The TPS25200 is an intelligent protected load switch with V_{IN} tolerant to 20V. In the event that an incorrect voltage is applied at IN, the output clamps to 5.4V to protect the load. If the voltage at IN exceeds 7.6V, the device disconnects the load to prevent damage to the device and/or load.

The TPS25200 has an internal 60mΩ power switch and is intended for protecting source, device, and load under a variety of abnormal conditions. The device provides up to 2.6A of continuous load current. Current limit is programmable from 85mA to 2.9A with a single resistor to ground. During overload events output current is limited to the level set by R_{ILIM}. If a persistent overload occurs the device eventually goes into thermal shutoff to prevent damage to the TPS25200.

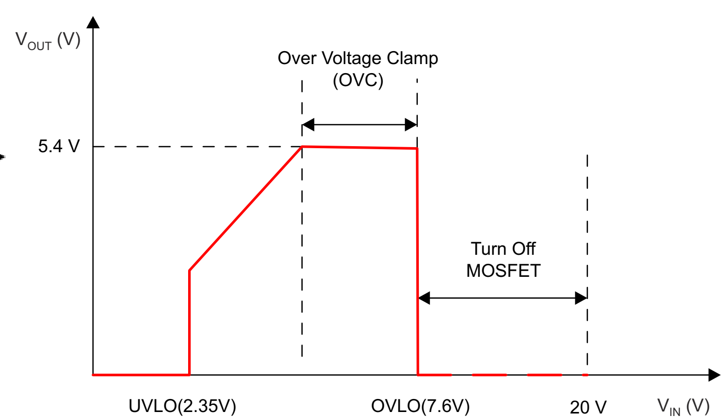
Package Information

ORDER NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TPS25200	DRV (WSON, 6)	2mm × 2mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic



V_{OUT} vs V_{IN}

Table of Contents

4 Pin Configuration and Functions

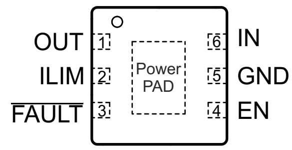


Figure 4-1. DRV Package 6-Pin WSON Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	4	I	Logic-level control input. When is driven high, the power switch is enabled. When it is driven low, turn power switch off. This pin cannot be left floating and it must be limited below the absolute maximum rating if tied to V_{IN}
$\overline{FAULT}$	3	O	Active-low open-drain output, asserted during overcurrent, overvoltage or overtemperature. Connect a pull up resistor to the logic I/O voltage
GND	5	—	Ground connection; connect externally to PowerPAD
ILIM	2	O	External resistor used to set current-limit threshold; Recommended 33 kΩ ≤ R_{ILIM} ≤ 1100 kΩ
IN	6	I	Input voltage; connect a 0.1-µF or greater ceramic capacitor from IN to GND as close to the IC as possible
OUT	1	O	Protected power switch V_{OUT}
PowerPAD™	PAD	—	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND terminal externally

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range, voltage are referenced to GND (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
	Voltage on IN	–0.3	20	V
	Voltage on OUT, EN, ILIM, $\overline{FAULT}$	–0.3	7	V
	Voltage from IN to OUT	–7	20	V
I_O	Continuous output current	Thermally Limited		
	Continuous $\overline{FAULT}$ output sink current		25	mA
	Continuous ILIM output source current		150	µA
T_J	Operating junction temperature	Internally limited		
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum- rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range, voltage are referenced to GND (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage of IN	2.5	6.5	V
V_{EN}	Enable terminal voltage	0	6.5	V
$I_{\overline{FAULT}}$	Continuous $\overline{FAULT}$ sink current	0	10	mA
I_{OUT}	Continuous output current of OUT		2.6	A
R_{ILIM}	Current-limit set resistors	33	1100	kΩ
T_J	Operating junction temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		TPS25200 DRV (WSON) 6 PINS	UNIT
$θ_{JA}$	Junction-to-ambient thermal resistance	66.5	°C/W
$θ_{JCtop}$	Junction-to-case (top) thermal resistance	83.4	°C/W
$θ_{JB}$	Junction-to-board thermal resistance	36.1	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	1.6	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	36.5	°C/W
$θ_{JCbot}$	Junction-to-case (bottom) thermal resistance	7.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

Conditions are –40°C ≤ T_J ≤ +125°C and 2.5 V ≤ V_{IN} ≤ 6.5 V. V_{EN} = V_{IN}, R_{ILIM} = 33 kΩ. Positive current into terminals. Typical value is at 25°C. All voltages are with respect to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	IN–OUT resistance[(1)]	2.5 V ≤ V_{IN} ≤ 5 V, I_{OUT} = 2.5 A	T_J = 25°C		60	70	mΩ
			–40°C ≤ T_J ≤ +85°C		60	90	
			–40°C ≤ T_J ≤ +125°C		60	99	
ENABLE INPUT EN							
	EN terminal turnon threshold	Input rising				1.9	V
	EN terminal turnoff threshold	Input falling		0.6			V
	Hysteresis				330[(2)]		mV
I_{EN}	Leakage current	V_{EN} = 0 V or 5.5 V		–2		2	μA
DISCHARGE							
R_{DCHG}	OUT discharge resistance	V_{OUT} = 5 V, V_{EN} = 0 V			480	625	Ω
CURRENT LIMIT							
I_{OS}	Current - limit, See Figure 6-4	R_{ILIM} = 33 kΩ		2773	2952	3127	mA
		R_{ILIM} = 40.2 kΩ		2270	2423	2570	
		R_{ILIM} = 56 kΩ		1620	1740	1860	
		R_{ILIM} = 80.6 kΩ		1110	1206	1300	
		R_{ILIM} = 150 kΩ		590	647	710	
		R_{ILIM} = 1100 kΩ		40	83	130	

5.5 Electrical Characteristics (continued)

Conditions are –40°C ≤ T_J ≤ +125°C and 2.5 V ≤ V_{IN} ≤ 6.5 V. V_{EN} = V_{IN}, R_{ILIM} = 33 kΩ. Positive current into terminals. Typical value is at 25°C. All voltages are with respect to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OVERVOLTAGE LOCKOUT, IN							
$V_{(OVLO)}$	IN rising OVLO threshold voltage	IN rising		6.8	7.6	8.45	V
	Hysteresis				70[2]		mV
VOLTAGE CLAMP, OUT							
$V_{(OVC)}$	OUT clamp voltage threshold	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 6.5 V		5.25	5.4	5.55	V
SUPPLY CURRENT							
$I_{IN(off)}$	Supply current, low-level output	V_{EN} = 0 V, V_{IN} = 5 V			0.8	5	µA
		V_{EN} = 0 or 5 V, V_{IN} = 20 V			1000	1700	
$I_{IN(on)}$	Supply current, high-level output	V_{IN} = 5 V, No load on OUT	R_{ILIM} = 33 kΩ		143	200	µA
			R_{ILIM} = 150 kΩ		134	190	
I_{REV}	Reverse leakage current	V_{OUT} = 6.5V, V_{IN} = V_{EN} = 0 V, T_J = 25°C, measure I_{OUT}			3	5	µA
UNDERVOLTAGE LOCKOUT, IN							
V_{UVLO}	IN rising UVLO threshold voltage	IN rising			2.35	2.45	V
	Hysteresis				30[2]		mV
$\overline{\text{FAULT}}$ FLAG							
V_{OL}	Output low voltage, $\overline{\text{FAULT}}$	$I_{\overline{FAULT}}$ = 1 mA			50	180	mV
	Off-state leakage	$V_{\overline{FAULT}}$ = 6.5 V				1	µA
THERMAL SHUTDOWN							
	Thermal shutdown threshold, OTSD2			155			°C
	Thermal shutdown threshold only in current-limit, OTSD1			135			
	Hysteresis				20[2]		

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.
(2) These parameters are provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

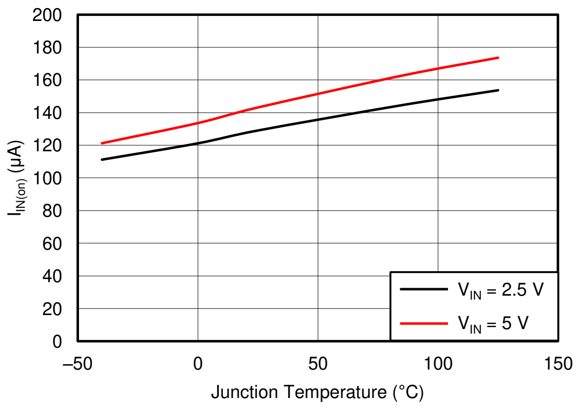
5.6 Timing Requirements

Conditions are –40°C ≤ T_J ≤ +125°C and 2.5 V ≤ V_{IN} ≤ 6.5 V. V_{EN} = V_{IN}, R_{ILIM} = 33 kΩ. Positive current are into terminals. Typical value is at 25°C. All voltages are with respect to GND (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
t_r	OUT voltage rise time	C_L = 1 µF, R_L = 100 Ω, (see Figure 6-2)		2.05	3.2	ms
t_f	OUT voltage fall time			0.18	0.2	
ENABLE INPUT EN						
t_{on}	Turnon time	2.5 V ≤ V_{IN} ≤ 5 V, C_L = 1 µF, R_L = 100 Ω, (see Figure 6-2)		5.12	7.3	ms
t_{off}	Turnoff time			0.22	0.3	ms
CURRENT LIMIT						
$t_{(IOS)}$	Short-circuit response time	V_{IN} = 5 V (see Figure 6-4)		3.5[1]		µs
OVERVOLTAGE LOCKOUT, IN						
$t_{(OVLO\_off\_delay)}$	Turnoff delay for OVLO	V_{IN} 5 V to 10 V with 1-V/µs ramp up rate, V_{OUT} with 100-Ω load		0.6[1]		µs
$\overline{\text{FAULT}}$ FLAG						
	$\overline{\text{FAULT}}$ deglitch	$\overline{\text{FAULT}}$ assertion or de-assertion due to overcurrent condition	5	8	12	ms

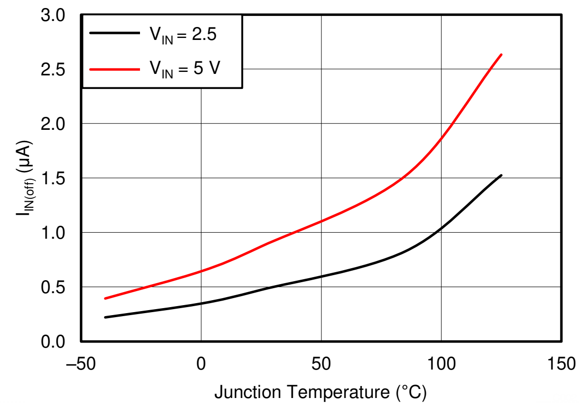
(1) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

5.7 Typical Characteristics



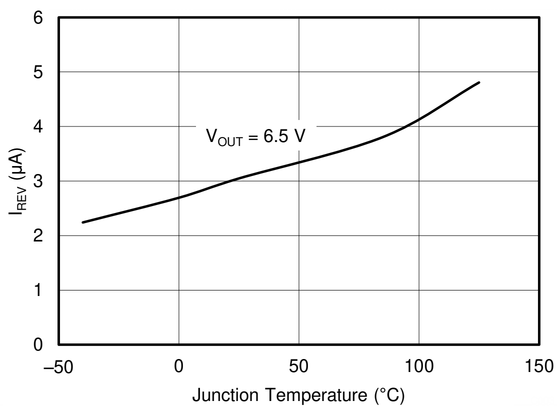
R_{ILIM} = 33 kΩ

Figure 5-1. $I_{IN(on)}$ vs Junction Temperature



R_{ILIM} = 33 kΩ

Figure 5-2. $I_{IN(off)}$ vs Junction Temperature



$V_{EN} = V_{IN}$ = 0 V

Figure 5-3. I_{REV} vs Junction Temperature

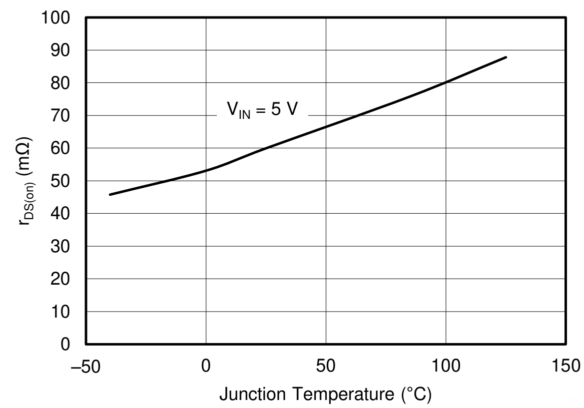
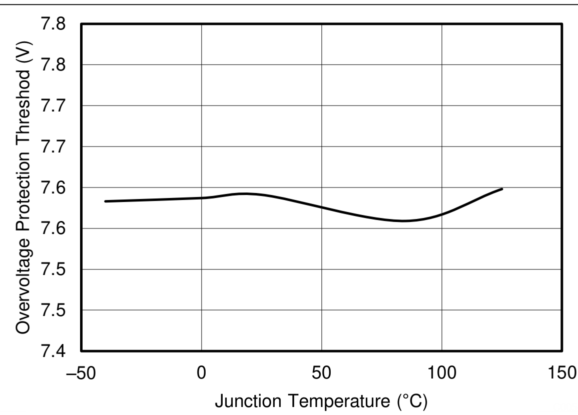
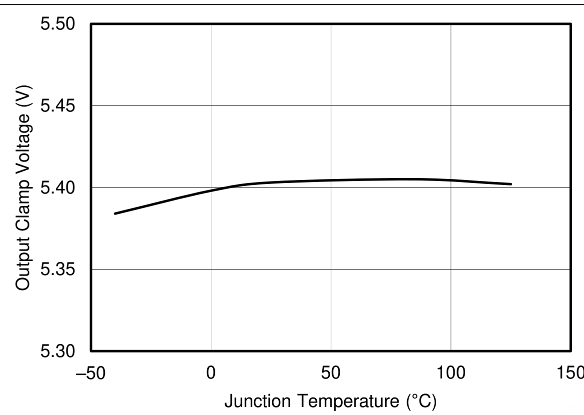


Figure 5-4. $r_{DS(ON)}$ vs Junction Temperature



$V_{EN} = V_{IN}$ = 0 V

Figure 5-5. $V_{(OVLO)}$ vs Junction Temperature



C_L = 1 µF, R_L = 100 Ω, V_{IN} = 6.5 V

Figure 5-6. $V_{O(VC)}$ vs Junction Temperature

5.7 Typical Characteristics (continued)

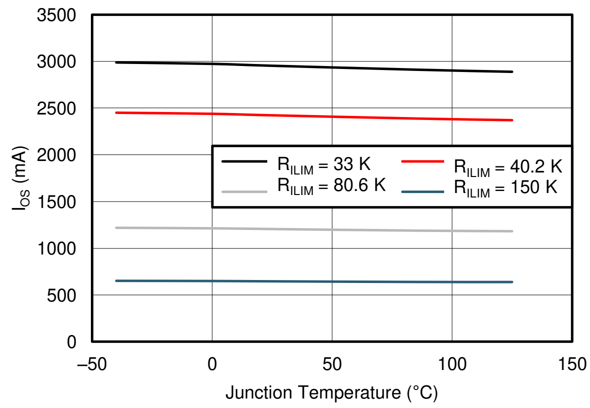


Figure 5-7. I_{OS} vs Junction Temperature

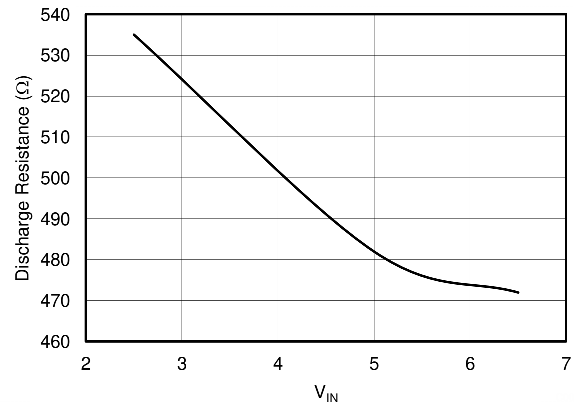


Figure 5-8. Discharge Resistance vs V_{IN}

6 Parameter Measurement Information

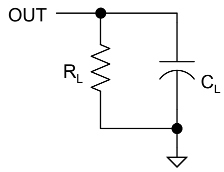


Figure 6-1. Output Rise-Fall Test Load

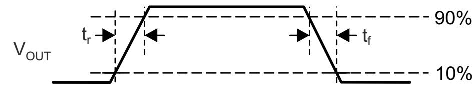


Figure 6-2. Power-On and Off Timing

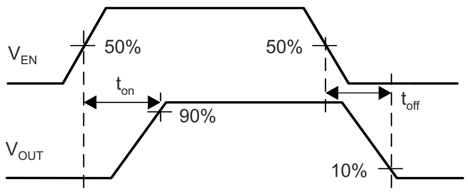


Figure 6-3. Enable Timing, Active High Enable

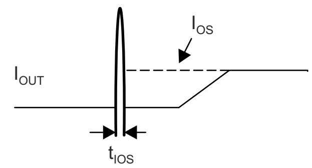


Figure 6-4. Output Short Circuit Parameters

7 Detailed Description

7.1 Overview

The TPS25200 is an intelligent low voltage switch or e-Fuse with robust overcurrent and overvoltage protection which is designed for a variety of applications.

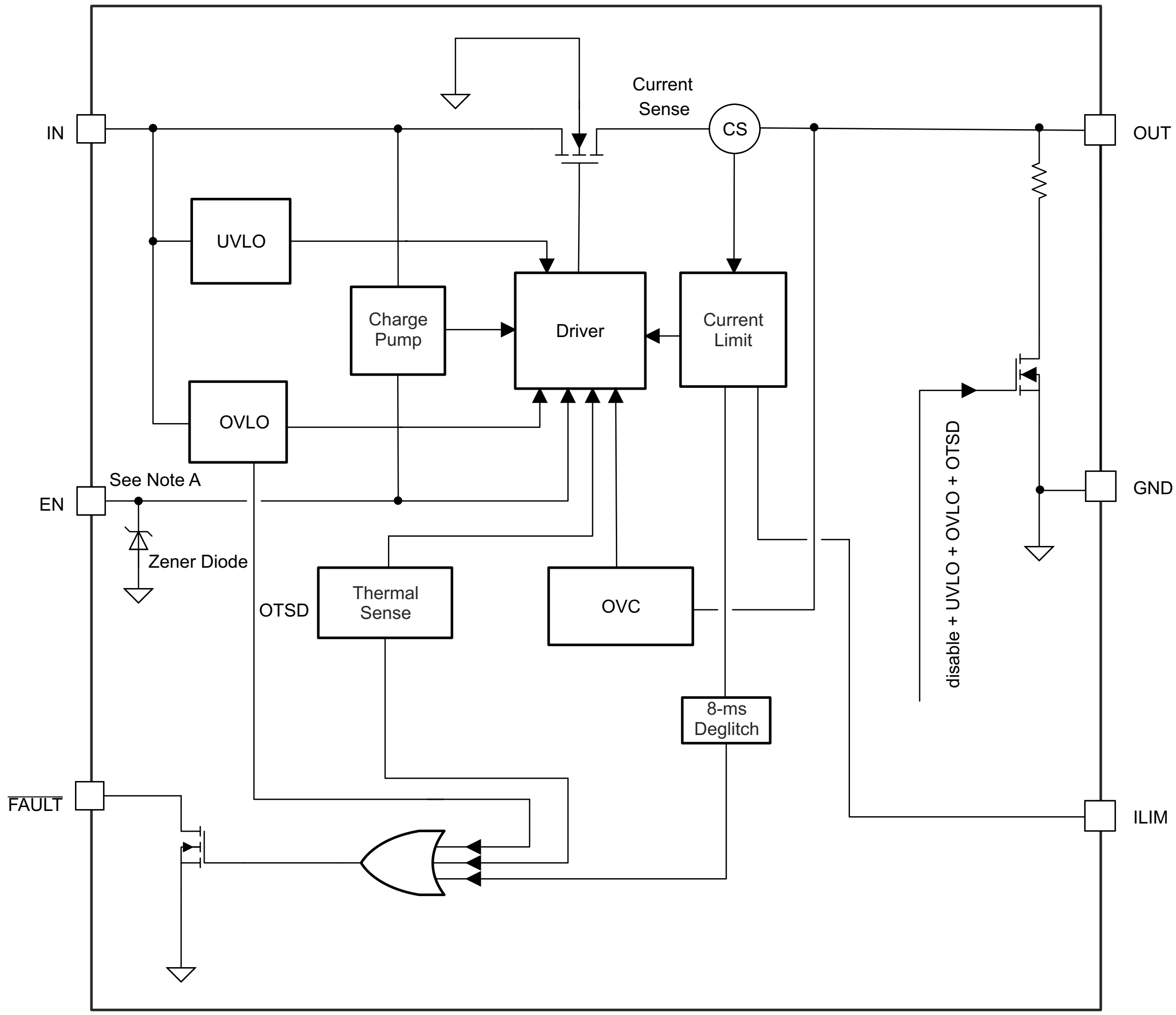
The TPS25200 current limited power switch uses N-channel MOSFETs in applications requiring up to 2.6 A of continuous load current. The device allows the user to program the current-limit threshold between 85 mA and 2.9 A (typical) via an external resistor. The device enters constant-current mode when the load exceeds the current-limit threshold.

The TPS25200 input can withstand 20-V DC voltage, but clamps V_{OUT} to a precision regulated 5.4 V and shuts down in the event V_{IN} exceeds 7.6 V. The device also integrates overcurrent and short circuit protection. The precision overcurrent limit helps to minimize over design of the input power supply while the fast response short circuit protection isolates the load when a short circuit is detected.

The additional features include:

- Enable the device can be put into a sleep mode for portable applications.
- Overtemperature protection to safely shutdown in the event of an overcurrent event or a slight overvoltage event where the V_{OUT} clamp is engaged over and extended period of time.
- Deglitched fault reporting to filter the Fault signal to verify the TPS25200 does not provide false fault alerts.
- Output discharge pull-down to help ensue a load is in fact off and not in some undefined operational state.
- Reverse blocking when disabled to prevent back-drive from an active load inadvertently causing undetermined behavior in the application.

7.2 Functional Block Diagram



A. 6.4-V Typical Clamp Voltage

7.3 Feature Description

7.3.1 Enable

This logic enable input controls the power switch and device supply current. A logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

EN can be tied to V_{IN} with a pull up resistor, and is protected with an integrated zener diode. Use a sufficiently large (300-kΩ) pull up resistor to ensure that the $V_{(EN)}$ is limited below the absolute maximum rating.

7.3.2 Thermal Sense

The TPS25200 self protects by using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. The TPS25200 device operates in constant-current mode during an overcurrent condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor (OTSD1) turns off the power switch when the die temperature exceeds 135°C (minimum) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C.

The TPS25200 also has a second ambient thermal sensor (OTSD2). The ambient thermal sensor turns off the power switch when the die temperature exceeds 155°C (minimum) regardless of whether the power switch is in current limit and turns on the power switch after the device has cooled approximately 20°C. The TPS25200 continues to cycle off and on until the fault is removed.

7.3.3 Overcurrent Protection

The TPS25200 thermally protects itself by thermal cycling during an extended overcurrent condition. The device turns off when the junction temperature exceeds 135°C (typical) while in current limit. The device remains off until the junction temperature cools 20°C (typical) and then restarts. The TPS25200 cycles on/off until the overload is removed (see Figure 9-13 and Figure 8-16).

The TPS25200 responds to an overcurrent condition by limiting their output current to the I_{OS} levels shown in Figure 6-4. When an overcurrent condition is detected, the device maintains a constant output current and the output voltage is reduced accordingly. During an over current event, two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS25200 ramps the output current to I_{OS}. The TPS25200 devices limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time t_{IOS} (see Figure 6-4). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and limits the output current to I_{OS}. Similar to the previous case, the TPS25200 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

7.3.4 $\overline{\text{FAULT}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an overcurrent, overtemperature or overvoltage condition. The TPS25200 asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the device resumes normal operation. The TPS25200 is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal delay "deglitch" circuit for overcurrent (8-ms typical) conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limit induced fault conditions.

The $\overline{\text{FAULT}}$ signal is not deglitched when the MOSFET is disabled due to an overtemperature condition but is deglitched after the device has cooled and begins to turnon. This unidirectional deglitch prevents $\overline{\text{FAULT}}$ oscillation during an overtemperature event.

The $\overline{\text{FAULT}}$ signal is not deglitched when the MOSFET is disabled into OVLO or out of OVLO. The TPS25200 does not assert the $\overline{\text{FAULT}}$ during output voltage clamp mode.

Connect $\overline{\text{FAULT}}$ with a pull up resistor to a low voltage I/O rail.

7.3.5 Output Discharge

A 480-Ω (typical) output discharge dissipates stored charge and leakage current on OUT when the TPS25200 is in UVLO, disabled or OVLO. The pull down capability decreases as V_{IN} decreases (Figure 6-8).

7.4 Device Functional Modes

The TPS25200 V_{IN} can withstand up to 20 V. Within 0 V to 20 V range, it can be divided to four modes as shown in Figure 7-1.

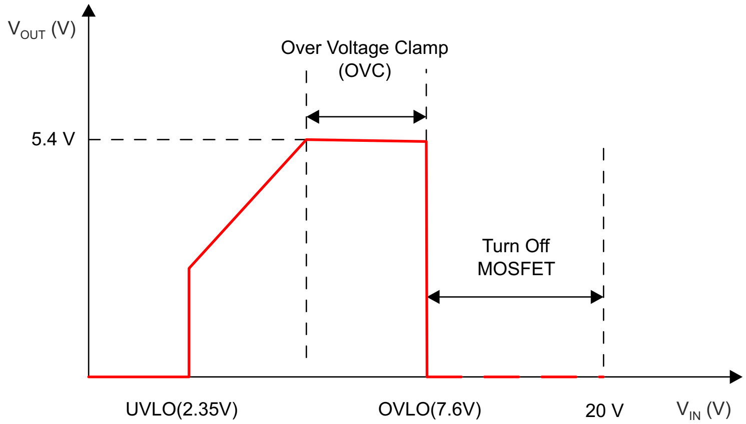


Figure 7-1. Output vs Input Voltage

7.4.1 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted on and off cycling due to input voltage droop during turnon.

7.4.2 Overcurrent Protection (OCP)

When 2.35 V < V_{IN} < 5.4 V, the TPS25200 is a traditional power switch, providing overcurrent protection.

7.4.3 Overvoltage Clamp (OVC)

When 5.4 V < V_{IN} < 7.6 V, the overvoltage clamp (OVC) circuit clamps the output voltage to 5.4 V. Within this V_{IN} range, the overcurrent protection remains active.

7.4.4 Overvoltage Lockout (OVLO)

When V_{IN} exceeds 7.6 V, the overvoltage lockout (OVLO) circuit turns off the protected power switch.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS25200 is a 5-V eFuse with precision current limit and over-voltage clamp. When a target device such as a mobile data-card device is hot plugged into a USB port as shown in Figure 8-1, an input transient voltage could damage the target device due to the cable inductance. Placing the TPS25200 at the input of mobile device as overvoltage and overcurrent protector can safeguard these target devices. Input transients also occur when the current through the cable parasitic inductance changes abruptly. This can occur when the TPS25200 turns off the internal MOSFET in response to an overvoltage or overcurrent event. The TPS25200 can withstand the transient without a bypass bulk capacitor, or other external overvoltage protection components at input side. The TPS25200 also can be used at host side as a traditional power switch pin-to-pin compatible with the TPS2553.

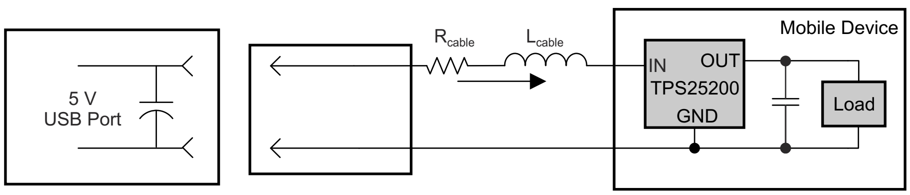


Figure 8-1. Hot Plug Into 5V USB port with Parasitic Cable Resistance and Inductance

8.2 Typical Application

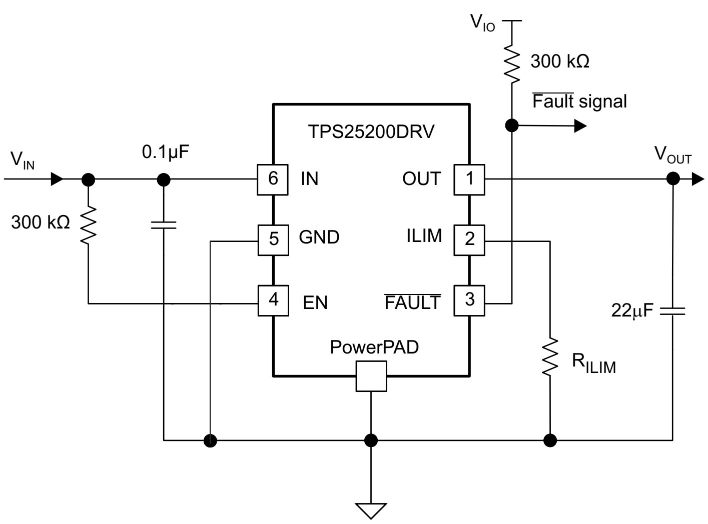


Figure 8-2. Overvoltage and Overcurrent Protector—Typical Application Schematic

Use the I_{OS} in the *Electrical Characteristics* table or I_{OS} in Equation 1 to select the R_{ILIM}.

8.2.1 Design Requirements

For this design example, use the desgin parameters in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Normal input operation voltage	5 V
Output transient voltage	6.5 V
Minimum current limit	2.1 A
Maximum currnt limit	2.9 A

8.2.2 Detailed Design Procedure

8.2.2.1 Step by Step Design Produce

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Normal Input Operation Voltage
- Output transient voltage
- Minimum Current Limit
- Maximum Current Limit

8.2.2.2 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, a 0.1-µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.

When V_{IN} ramp up exceed 7.6 V, V_{OUT} follows V_{IN} until the TPS25200 turns off the internal MOSFET after $t_{(OVLO\_off\_delay)}$. Since $t_{(OVLO\_off\_delay)}$ largely depends on the V_{IN} ramp rate, V_{OUT} sees some peak voltage. Increasing the output capacitance can lower the output peak voltage as shown in Figure 8-3.

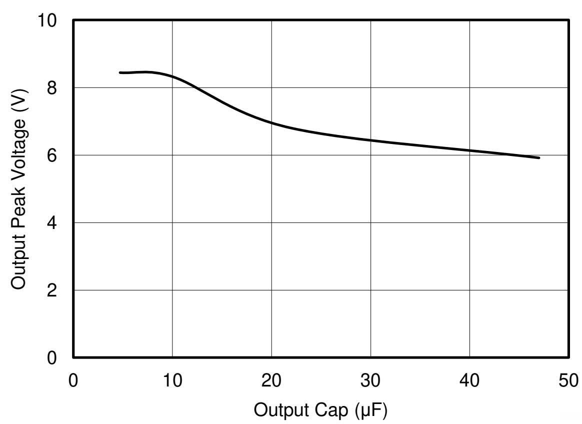


Figure 8-3. V_{OUT} Peak Voltage vs C_{OUT} (V_{IN} Step From 5 V to 15 V with 1-V/µs Ramp Up Rate)

8.2.2.3 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable via an external resistor. The TPS25200 uses an internal regulation loop to provide a regulated voltage on the ILIM terminal. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is 33 kΩ ≤ R_{ILIM} ≤ 1100 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM}. The current-limit threshold equations (IOS) in Equation 1 approximate the resulting overcurrent threshold for a given external resistor value R_{ILIM}. See the *Electrical Characteristics* table for specific current limit settings. The traces routing the R_{ILIM} resistor to the TPS25200 must be as short as possible to reduce parasitic effects on the current-limit accuracy.

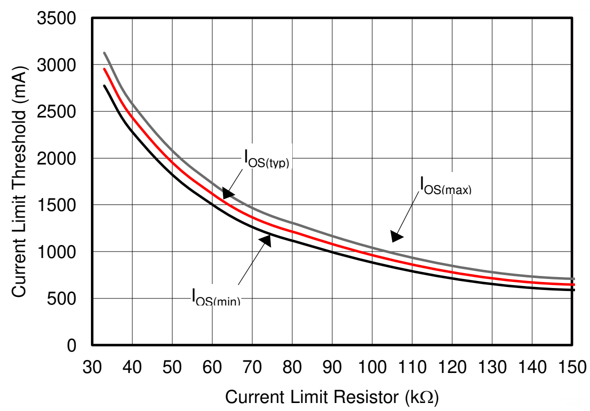
R_{ILIM} can be selected to provide a current-limit threshold that occurs 1) above a minimum load current or 2) below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(min)}$ curve and choose a value of R_{ILIM} below this value. Programming the current limit above a minimum threshold is important to ensure start up into full load or heavy capacitive loads. The resulting maximum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(max)}$ curve.

To design below a maximum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(max)}$ curve and choose a value of R_{ILIM} above this value. Programming the current limit below a maximum threshold is important to avoid current limiting upstream power supplies causing the input voltage bus to droop. The resulting minimum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(min)}$ curve. See Figure 9-4 and Figure 9-5 .

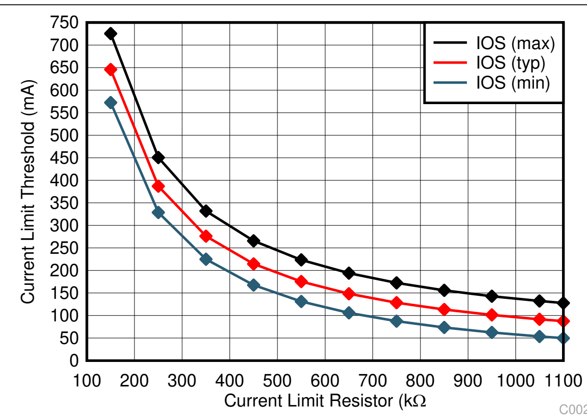
$$I_{OSmax}(mA) = \frac{96754V}{R_{ILIM}{}^{0.985}k\Omega} + 30$$
$$I_{OSnom}(mA) = \frac{98322V}{R_{ILIM}{}^{1.003}k\Omega}$$
$$I_{OSmin}(mA) = \frac{97399}{R_{ILIM}{}^{1.015}k\Omega} - 30 \quad (1)$$

Where 33 kΩ ≤ R_{ILIM} ≤ 1100 kΩ.



33 kΩ ≤ R_{ILIM} ≤ 150 kΩ

Figure 8-4. Current-Limit Threshold vs R_{ILIM} I



150 kΩ ≤ R_{ILIM} ≤ 1100 kΩ

Figure 8-5. Current-Limit Threshold vs R_{ILIM} II

8.2.2.4 Design Above a Minimum Current Limit

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 2.1 A must be delivered to the load so that the minimum desired current-limit threshold is 2100 mA. Use the I_{OS} equations (Equation 1) and Figure 9-4 to select R_{ILIM} as shown in Equation 2.

$$I_{OSmin}(mA) = 2100\ mA$$
$$I_{OSmin}(mA) = \frac{97399V}{R_{ILIM}{}^{1.015}k\Omega} - 30$$
$$R_{ILIM}(k\Omega) = \left(\frac{97399}{I_{OS(min)} + 30}\right)^{\frac{1}{1.015}} = \left(\frac{97399}{2100 + 30}\right)^{\frac{1}{1.015}} = 43.22\ k\Omega \quad (2)$$

Select the closest 1% resistor less than the calculated value: R_{ILIM} = 42.2 kΩ. This sets the minimum current-limit threshold at 2130 mA as shown in Equation 3.

$$I_{OS\,min}(mA) = \frac{97399V}{R_{ILIM}{}^{1.015}k\Omega} - 30 = \frac{97399}{(42.2 \text{ x } 1.01)^{1.015}} - 30 = 2130mA \tag{3}$$

Use the I_{OS} equations (Equation 1), Figure 9-4, and the previously calculated value for R_{ILIM} to calculate the maximum resulting current-limit threshold as shown in Equation 4.

$$I_{OS\,max}(mA) = \frac{96754}{R_{ILIM}{}^{0.985}} + 30$$

$$I_{OS\,max}(mA) = \frac{96754}{(42.2 \times 0.99)^{0.985}} + 30 = 2479 \text{ mA} \tag{4}$$

The resulting current-limit threshold minimum is 2130 mA and maximum is 2479 mA with R_{ILIM} = 42.2kΩ ± 1%.

8.2.2.5 Design Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that 2.9 A must be delivered to the load so that the minimum desired current-limit threshold is 2900 mA. Use the I_{OS} equations (Equation 1) and Figure 9-5 to select R_{ILIM} as shown in Equation 5.

$$I_{OS\,max}(mA) = 2900mA$$

$$I_{OS\,max}(mA) = \frac{96754}{R_{ILIM}{}^{0.985}k\Omega} + 30$$

$$R_{ILIM}(k\Omega) = \left(\frac{96754}{I_{OS(max)} - 30}\right)^{\frac{1}{0.985}} = \left(\frac{96754}{2900 - 30}\right)^{\frac{1}{0.985}} = 35.57 \text{ k}\Omega \tag{5}$$

Select the closest 1% resistor greater than the calculated value: R_{ILIM} = 36 kΩ. This sets the maximum current-limit threshold at 2894 mA as shown in Equation 6.

$$I_{OS\,max}(mA) = \frac{96754V}{R_{ILIM}{}^{0.985}k\Omega} + 30 = \frac{96754}{(36 \text{ x } 0.99)^{0.985}} + 30 = 2894mA \tag{6}$$

Use the I_{OS} equations, Figure 9-5, and the previously calculated value for R_{ILIM} to calculate the minimum resulting current-limit threshold as shown in Equation 7.

$$I_{OS\,min}(mA) = \frac{97399}{R_{ILIM}{}^{1.015}} - 30$$

$$I_{OS\,min}(mA) = \frac{97399}{(36 \times 1.01)^{1.015}} - 30 = 2508mA \tag{7}$$

The resulting minimum current-limit threshold minimum is 2592 mA and maximum is 2894 mA with R_{ILIM} = 36 kΩ ± 1%.

8.2.2.6 Power Dissipation and Junction Temperature

The low on-resistance of the internal N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. When V_{IN} is lower than $V_{(OVC)}$, the TPS2500 is an traditional power switch. Using this value, the power dissipation can be calculated by usnig Equation 8.

$$P_D = r_{DS(on)} \times I_{OUT}{}^2 \quad (8)$$

When V_{IN} exceed $V_{(OVC)}$, but lower than $V_{(OVLO)}$, the TPS25200 clamp output to fixed $V_{(OVC)}$, the power dissipation can be calculated by using Equation 9.

$$P_D = (V_{IN} – V_{(OVC)}) \times I_{OUT} \quad (9)$$

where

- P_D = Total power dissipation (W)
- $r_{DS(on)}$ = Power switch on-resistance (Ω)
- $V_{(OVC)}$ = Overvoltage clamp voltage (V)
- I_{OUT} = Maximum current-limit threshold (A)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature using Equation 10.

$$T_J = P_D \times \theta_{JA} + T_A \quad (10)$$

where

- T_A = Ambient temperature (°C)
- θ_{JA} = Thermal resistance (°C /W)
- P_D = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance θ_{JA}, and thermal resistance is highly dependent on the individual package and board layout.

8.2.3 Application Curves

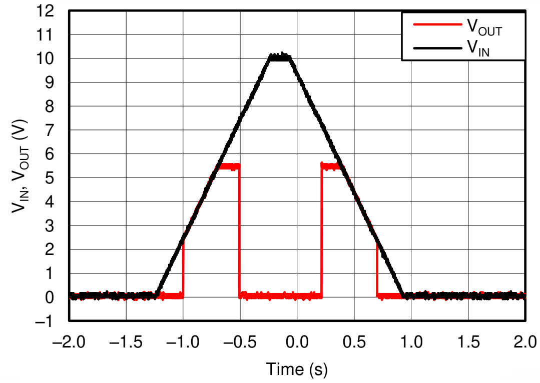


Figure 8-6. V_{OUT} vs V_{IN} (0 V to 10 V)

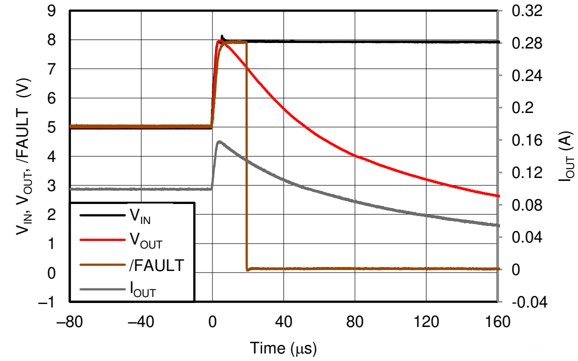


Figure 8-7. V_{IN} Step 5 V to 8 V with 4.7 µF // 100 Ω

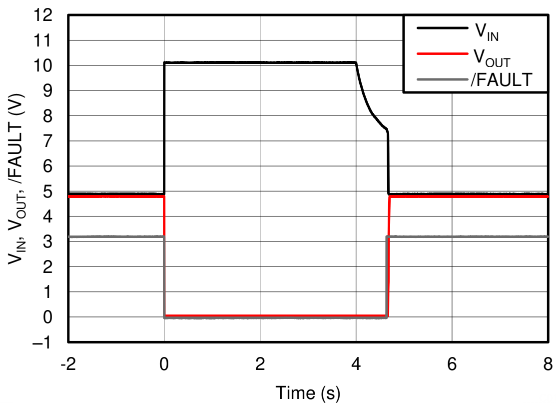


Figure 8-8. Pulse Overvoltage with 100 Ω

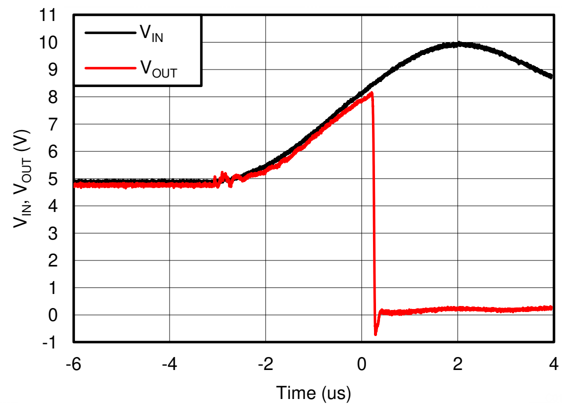


Figure 8-9. 5-V to 10-V OVLO Response Time

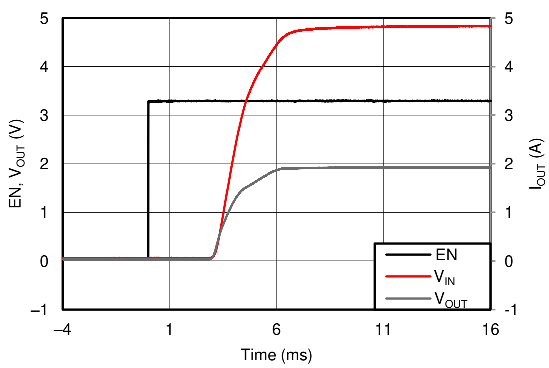


Figure 8-10. Turnon Delay and Rise Time 150 µF || 2.5 Ω

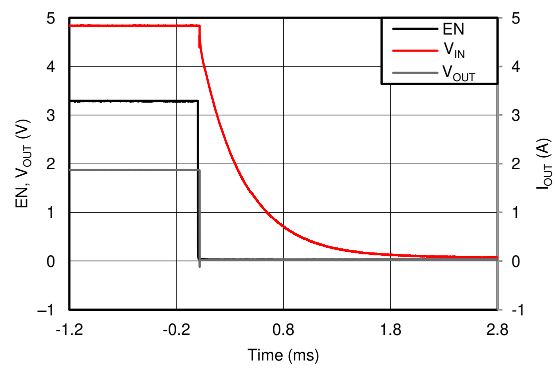


Figure 8-11. Turnoff Delay and Fall Time 150 µF || 2.5 Ω

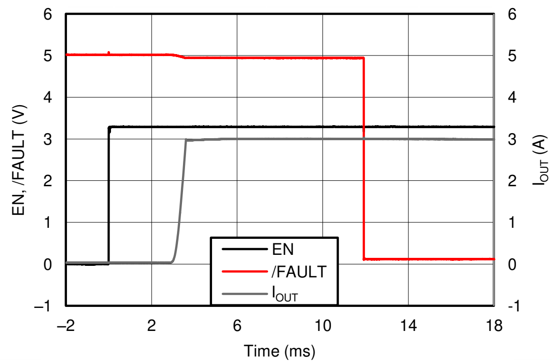


Figure 8-12. Enable into Output Short

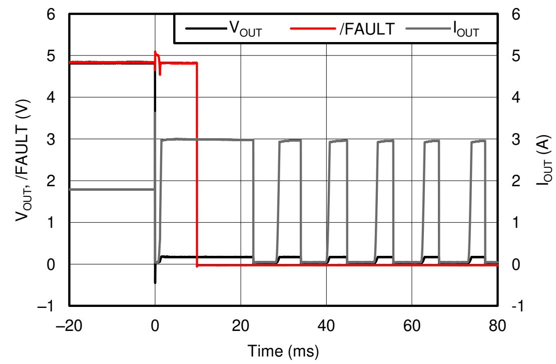


Figure 8-13. 2.5 Ω to Output Short Transient Response

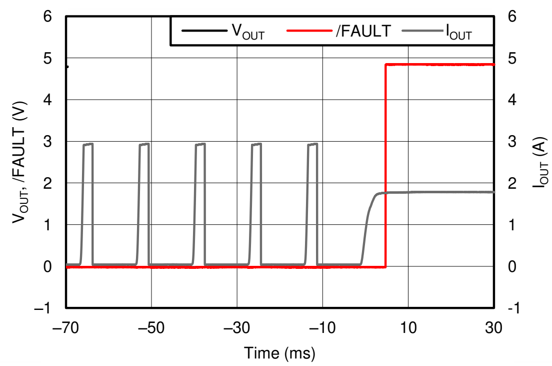


Figure 8-14. Output Short to 2.5-Ω Load Recovery Response

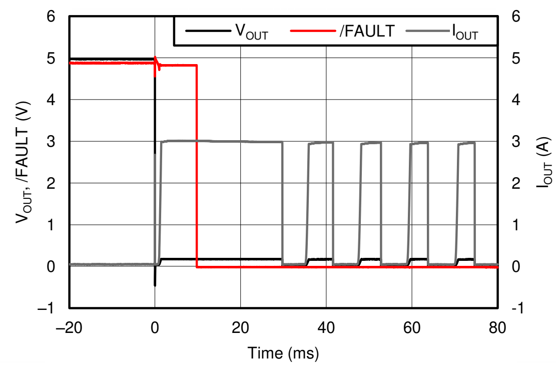


Figure 8-15. No Load to Output Short Transient Response

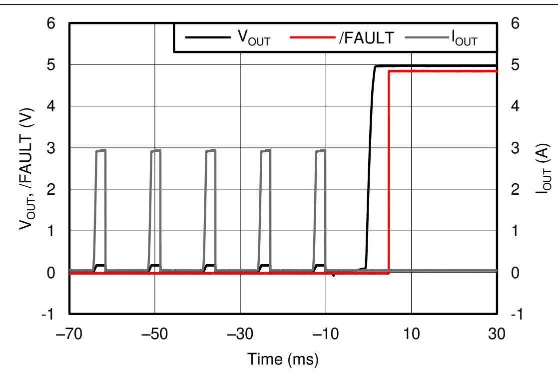


Figure 8-16. Output Short to No Load Recovery Response

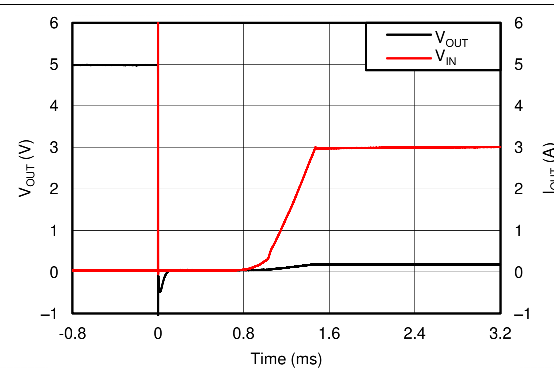


Figure 8-17. Hot-Short With 50 mΩ

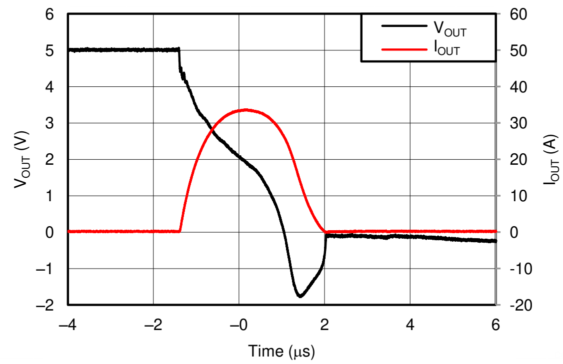


Figure 8-18. 50-mΩ Hot-Short Response Time

8.3 Power Supply Recommendations

The TPS25200 is designed for 2.7 V < V_{IN} < 5 V (typical) voltage rails. While there is a V_{OUT} clamp, it is not intended to be used to regulate V_{OUT} at approximately 5.4 V with 6 V < V_{IN} < 7 V. This is a protection feature only.

8.4 Layout

8.4.1 Layout Guidelines

- For all applications, a 0.1-µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.
- For output capacitance, refer to Figure 8-3, low ESR ceramic cap is recommended.
- The traces routing the R_{ILIM} resistor to the device must be as short as possible to reduce parasitic effects on the current limit accuracy.
- The PowerPAD must be directly connected to PCB ground plane using wide and short copper trace.

8.4.2 Layout Example

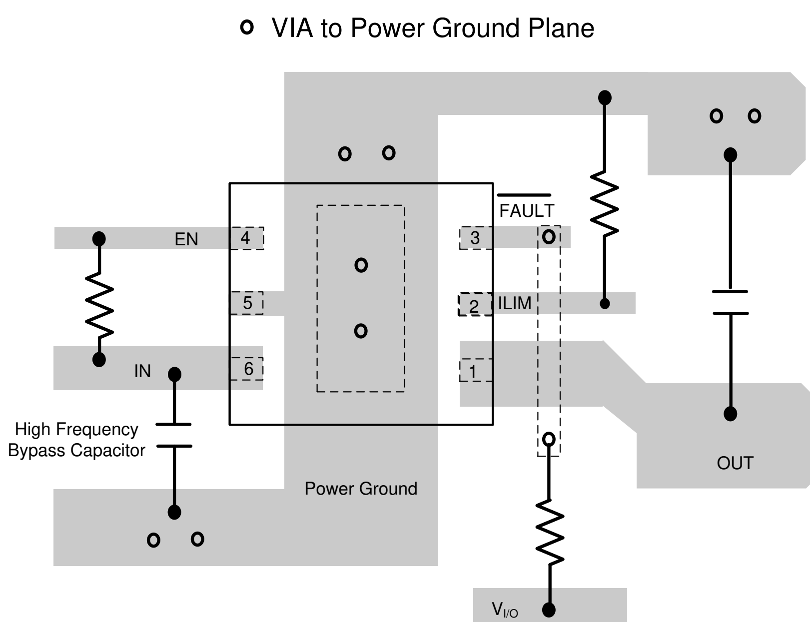


Figure 8-19. TPS25200 Board Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

TPS25200 EVM User's Guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2021) to Revision F (July 2025) — **Page**

- Changed all instances of legacy terminology to *target* where USB is mentioned 1
- Changed continuous load current from *2.5A* to *2.6A* throughout document 1
- Changed title and format of *Package Information* table 1

Changes from Revision D (February 2020) to Revision E (June 2021) — **Page**

- Updated the numbering format for tables, figures and cross-references throughout the document 1
- Corrected package type 3
- Corrected package type 4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25200DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKB
TPS25200DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKB
TPS25200DRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKB
TPS25200DRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKB
TPS25200DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKB
TPS25200DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS25200 :

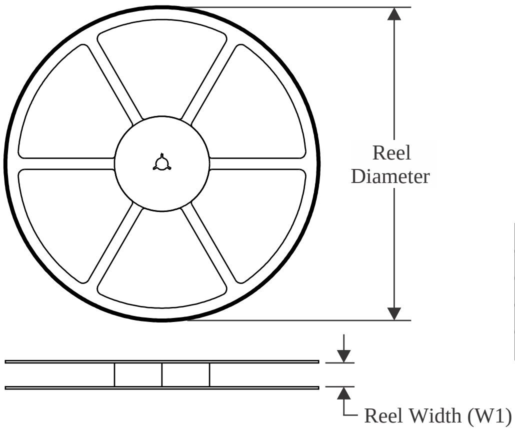
- Automotive : TPS25200-Q1

NOTE: Qualified Version Definitions:

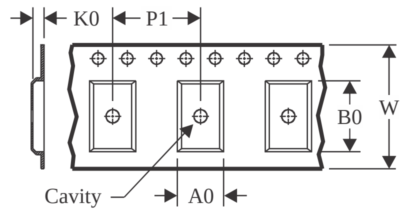
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

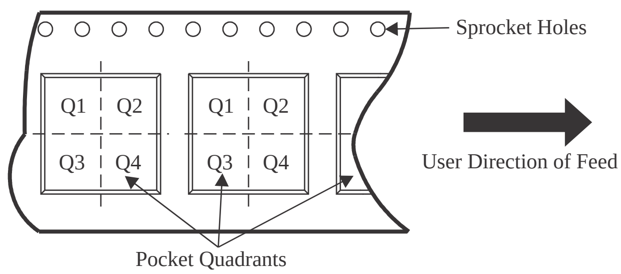


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

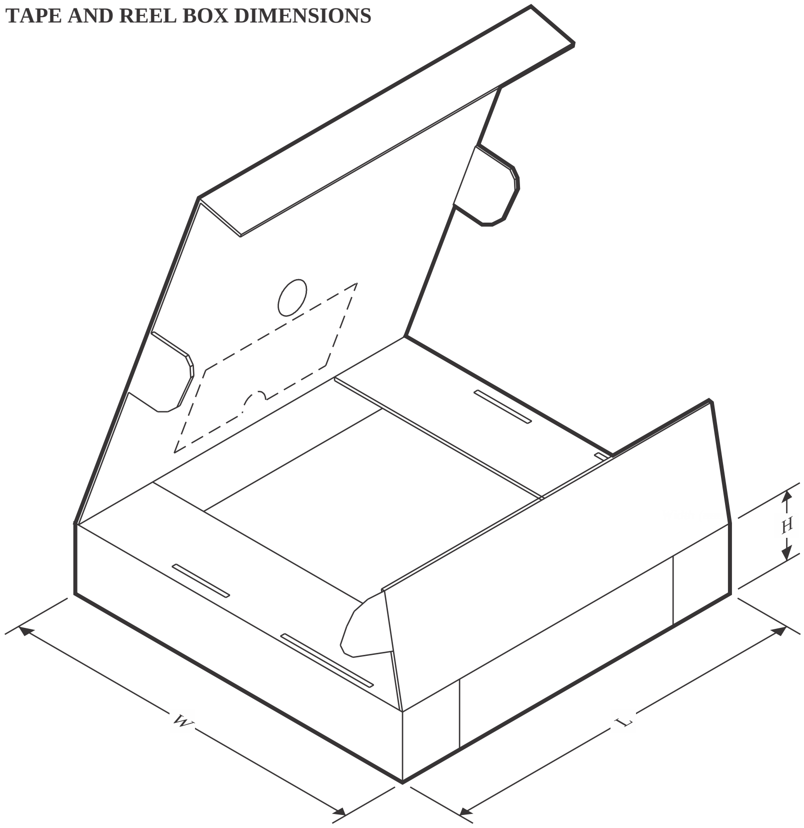
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25200DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS25200DRVRG4	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS25200DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



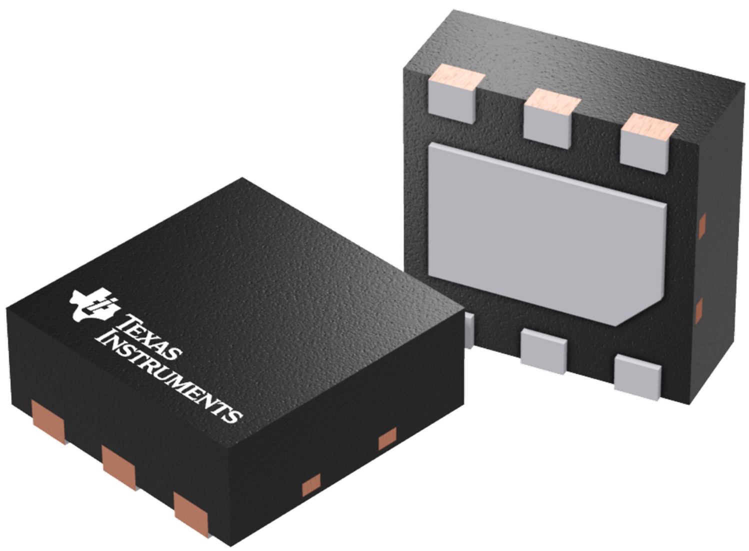
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25200DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS25200DRVRG4	WSON	DRV	6	3000	210.0	185.0	35.0
TPS25200DRVT	WSON	DRV	6	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

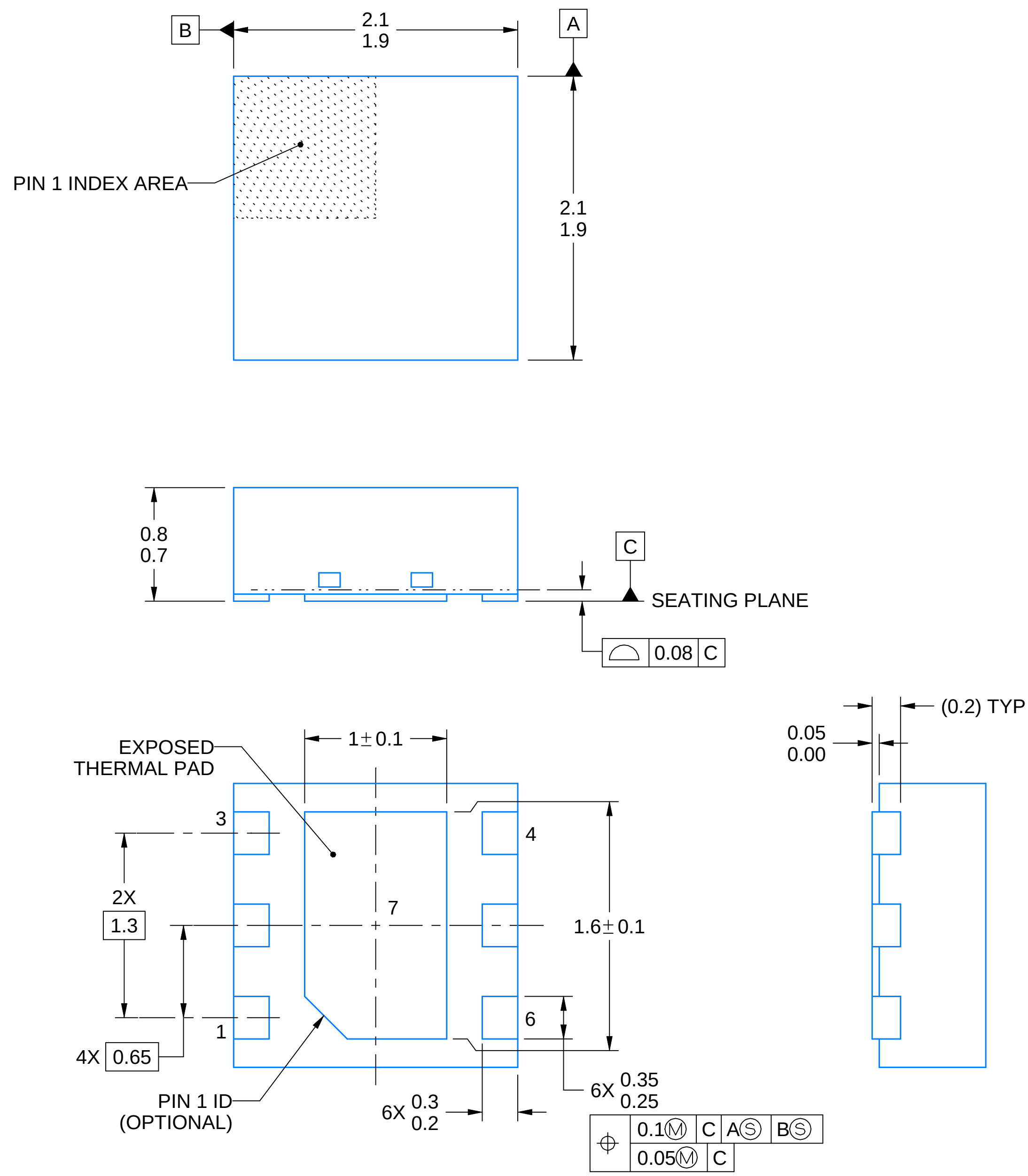
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

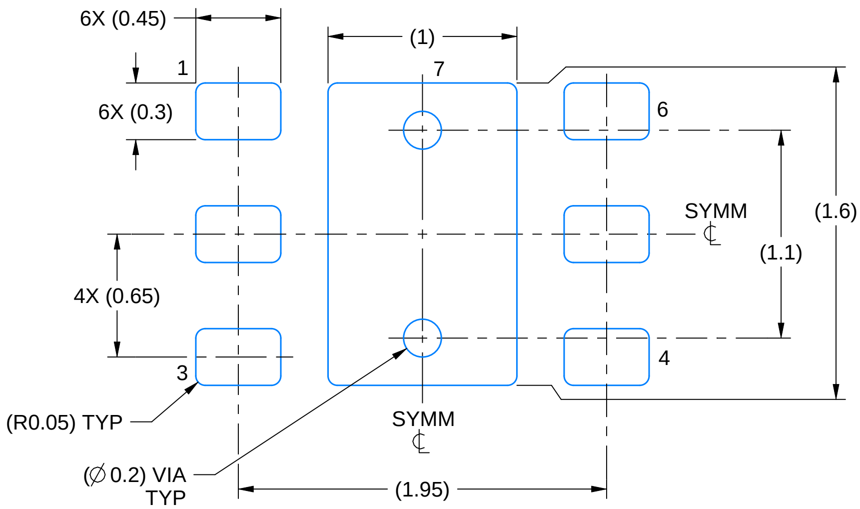
4206925/F



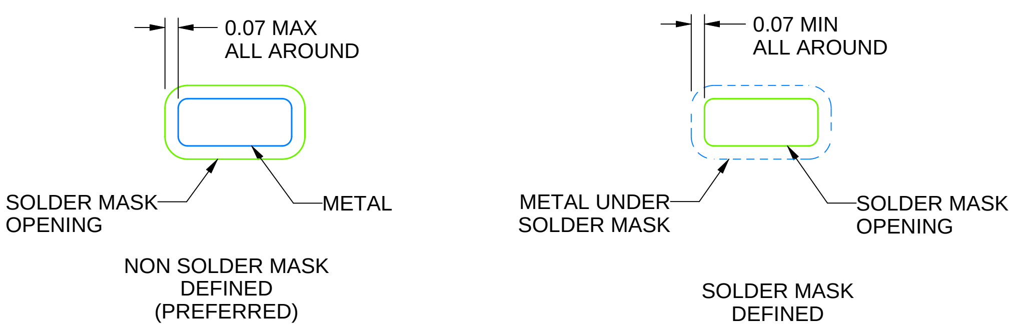
4222173/B 04/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X

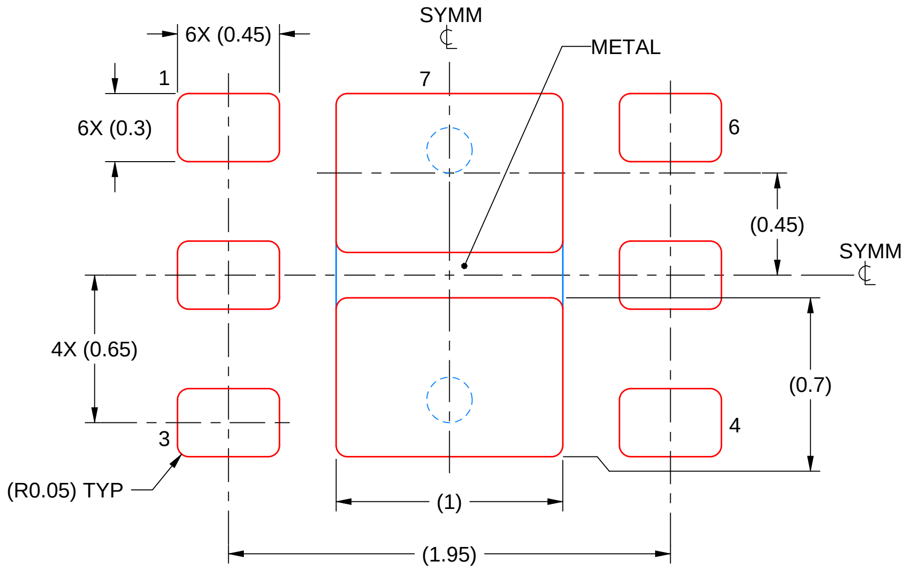


SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.