

# TPS2561A-Q1 Dual Channel Precision Automotive Adjustable Current-Limited Power Switches

## 1 Features

- AEC-Q100 Qualified
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C5
- Two separate current limiting channels
- Meets USB Current-Limiting Requirements
- Adjustable Current Limit, 250 mA–2.8 A (Typ.)
- Accurate 2.1A Min / 2.5A Max Setting
- Fast Short Circuit Response - 3.5- $\mu$ s (typ)
- Two 44-m $\Omega$  High-Side MOSFETs
- Operating Range: 2.5 V to 6.5 V
- 2- $\mu$ A Maximum Standby Supply Current
- Built-in Soft-Start
- 15 kV / 8 kV System-Level ESD Capable

## 2 Applications

## Automotive USB Charging Ports

### 3 Description

The TPS2561A-Q1 is dual-channel power-distribution switch intended for automotive applications where precision current limiting is required or heavy capacitive loads and short circuits are encountered. These devices offer a programmable current-limit threshold between 250 mA and 2.8 A (typ) per channel via an external resistor. The power-switch rise and fall times are controlled to minimize current surges during turn on/off.

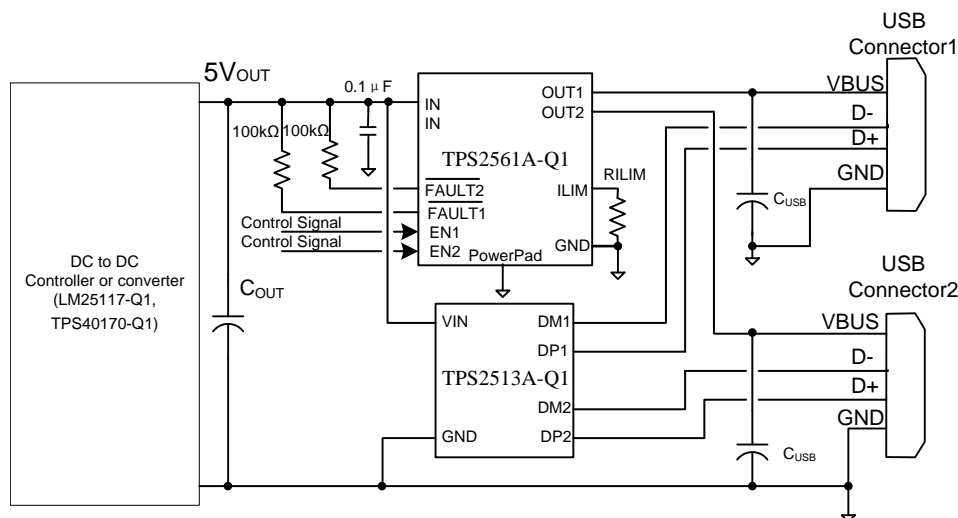
Each channel of the TPS2561A-Q1 devices limits the output current to a safe level by switching into a constant-current mode when the output load exceeds the current-limit threshold. The FAULTx logic output for each channel independently asserts low during overcurrent and over temperature conditions.

Use with the TPS2511-Q or TPS2513A-Q1 for a low loss, automotive qualified, USB Charging Port Solution capable of charging all of today's popular phones and tablets.

## Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2561A-Q1	SON (10)	3.00mm x 3.00mm

## Typical Application as Power Switch of Dual Port Automotive USB Charge Port Solution



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## 4 Revision History

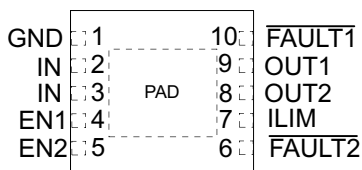
Changes from Original (March 2014) to Revision A	Page
• Changed Feature From: Accurate 2.1A Min / 2.5A Max Setting (Including Resistor) To: Accurate 2.1A Min / 2.5A Max Setting .....	<b>1</b>
• Changed $I_{OS}$ , Current-limit. to include additional $R_{ILIM}$ values. ....	<b>5</b>
• Changed <a href="#">Equation 1</a> .....	<b>11</b>
• Changed the <a href="#">Designing Above a Minimum Current Limit</a> section .....	<b>12</b>
• Changed the <a href="#">Designing Below a Maximum Current Limit</a> section .....	<b>13</b>

## 5 Device Comparison Table

DEVICE	MAXIMUM OPERATING CURRENT (A)	OUTPUTS	ENABLES	TYPICAL $R_{DS(on)}$ (m $\Omega$ )	PACKAGE
TPS2556-Q1	5	1	Active-low	22	SON-8 (DRB)
TPS2557-Q1	5	1	Active-high	22	SON-8 (DRB)
TPS2561A-Q1	2.5	2	Active-high	44	SON-10 (DRC)

## 6 Pin Functions and Configurations

**DRC PACKAGE  
(TOP VIEW)**



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NUMBER		
EN1	4	I	Enable input, logic high turns on channel one power switch
EN2	5	I	Enable input, logic high turns on channel two power switch
GND	1		Ground connection; connect externally to PowerPAD
IN	2, 3	I	Input voltage; connect a 0.1 $\mu$ F or greater ceramic capacitor from IN to GND as close to the IC as possible.
$\overline{\text{FAULT1}}$	10	O	Active-low open-drain output, asserted during overcurrent or overtemperature condition on channel one.
$\overline{\text{FAULT2}}$	6	O	Active-low open-drain output, asserted during overcurrent or overtemperature condition on channel two
OUT1	9	O	Power-switch output for channel one
OUT2	8	O	Power-switch output for channel two
ILIM	7	O	External resistor used to set current-limit threshold; recommended $20 \text{ k}\Omega \leq R_{ILIM} \leq 187 \text{ k}\Omega$ .
PowerPAD™	PAD		Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND pin externally.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted<sup>(1) (2)</sup>

	MIN	MAX	UNIT
Voltage range on IN, OUTx, ENx, ILIM, $\overline{\text{FAULTx}}$	−0.3	7	V
Voltage range from IN to OUTx	−7	7	V
Continuous output current	Internally Limited		
Continuous $\overline{\text{FAULTx}}$ sink current		25	mA
ILIM source current	Internally Limited		mA
T <sub>J</sub> Maximum junction temperature	−40	Internally Limited	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltages are referenced to GND unless otherwise noted.

### 7.2 Handling Ratings

	MIN	MAX	UNIT
T <sub>STG</sub> Storage temperature range	−65	150	°C
V <sub>ESD</sub> <sup>(1)</sup>	Human Body Model (HBM)	AEC-Q100 Classification Level H2	2
	Charged Device Model (CDM)	AEC-Q100 Classification Level C5	750
	System level (contact/air)	8/15 <sup>(2)</sup>	kV

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- (2) Surges per EN61000-4-2, 1999 applied between USB connection for V<sub>BUS</sub> and GND of the TPS2560EVM (HPA424, replacing TPS2560 with TPS2561A-Q1) evaluation module (documentation available on the Web.) These were the test level, no the failure threshold.

### 7.3 Recommended Operating Conditions

	MIN	MAX	UNIT
V <sub>IN</sub> Input voltage, IN	2.5	6.5	V
V <sub>ENx</sub> Enable voltage	0	6.5	V
V <sub>IH</sub> High-level input voltage on ENx	1.1	0.66	V
V <sub>IL</sub> Low-level input voltage on ENx			
I <sub>OUTx</sub> Continuous output current per channel, OUTx	0	2.5	A
Continuous $\overline{\text{FAULTx}}$ sink current	0	10	mA
T <sub>J</sub> Operating junction temperature	−40	125	°C
R <sub>ILIM</sub> Recommended resistor limit range	20	187	kΩ

### 7.4 Thermal Information<sup>(1)</sup>

THERMAL METRIC		TPS2561A-Q1	UNIT
		DRC (10 TERMINALS)	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	38.1	°C/W
θ <sub>JCTop</sub>	Junction-to-case (top) thermal resistance	40.5	
θ <sub>JB</sub>	Junction-to-board thermal resistance	13.6	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.6	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	13.7	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	3.4	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over recommended operating conditions,  $V_{ENx} = V_{IN}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP	MAX	UNIT	
POWER SWITCH								
r <sub>DS(on)</sub>	Static drain-source on-state resistance per channel, IN to OUTx	T <sub>J</sub> = 25°C			44	50	mΩ	
		−40°C ≤T <sub>J</sub> ≤125 °C				70		
t <sub>r</sub>	Rise time, output	V <sub>IN</sub> = 6.5 V	C <sub>Lx</sub> = 1 μF, R <sub>Lx</sub> = 100 Ω, (see Figure 9)	1.5	3	4	ms	
		V <sub>IN</sub> = 2.5 V		0.5	2	3		
t <sub>f</sub>	Fall time, output	V <sub>IN</sub> = 6.5 V		0.5	0.8	1.0		
		V <sub>IN</sub> = 2.5 V		0.3	0.6	0.8		
ENABLE INPUT EN								
	Enable pin turn on/off threshold			0.66		1.1	V	
	Hysteresis				55 <sup>(2)</sup>		mV	
I <sub>EN</sub>	Input current	V <sub>ENx</sub> = 0 V or 6.5 V		−0.5		0.5	μA	
t <sub>on</sub>	Turnon time	C <sub>Lx</sub> = 1 μF, R <sub>Lx</sub> = 100 Ω, (see Figure 9)				9	ms	
t <sub>off</sub>	Turnoff time					6	ms	
CURRENT LIMIT								
I <sub>OS</sub>	Current-limit (see Figure 11)	OUTx connected to GND	R <sub>ILIM</sub> = 20 kΩ	2560	2750	2980	mA	
			R <sub>ILIM</sub> = 24.3 kΩ	2100	2250	2500		
			R <sub>ILIM</sub> = 61.9 kΩ	800	900	1005		
			R <sub>ILIM</sub> = 100 kΩ	470	560	645		
		OUT1 and OUT2 connected to GND	R <sub>ILIM</sub> = 47.5 kΩ	2100	2300	2500		
t <sub>IOS</sub>	Response time to short circuit	V <sub>IN</sub> = 5 V (see Figure 10)			3.5 <sup>(2)</sup>		μs	
SUPPLY CURRENT								
I <sub>IN(off)</sub>	Supply current, low-level output	V <sub>IN</sub> = 6.5 V, No load on OUTx, V <sub>ENx</sub> = 0 V			0.1	2.0	μA	
I <sub>IN(on)</sub>	Supply current, high-level output	V <sub>IN</sub> = 6.5 V, No load on OUT	R <sub>ILIM</sub> = 20 kΩ		100	125	μA	
			R <sub>ILIM</sub> = 100 kΩ		85	110	μA	
I <sub>REV</sub>	Reverse leakage current	V <sub>OUTx</sub> = 6.5 V, V <sub>IN</sub> = 0 V	T <sub>J</sub> = 25°C		0.01	1.0	μA	
UNDERVOLTAGE LOCKOUT								
V <sub>UVLO</sub>	Low-level input voltage, IN	V <sub>IN</sub> rising			2.35	2.45	V	
	Hysteresis, IN	T <sub>J</sub> = 25°C			35 <sup>(2)</sup>		mV	
FAULTx FLAG								
V <sub>OL</sub>	Output low voltage, FAULTx	I $\overline{\text{FAULTx}}$ = 1 mA				180	mV	
	Off-state leakage	V $\overline{\text{FAULTx}}$ = 6.5 V				1	μA	
	$\overline{\text{FAULTx}}$ deglitch	$\overline{\text{FAULTx}}$ assertion or de-assertion due to overcurrent condition			6	9	13	ms
THERMAL SHUTDOWN								
	Thermal shutdown threshold, OTSD2				155		°C	
	Thermal shutdown threshold in current-limit, OTSD				135		°C	
	Hysteresis				20 <sup>(2)</sup>		°C	

- (1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
- (2) These parameters are provided for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

## 7.6 Typical Characteristics

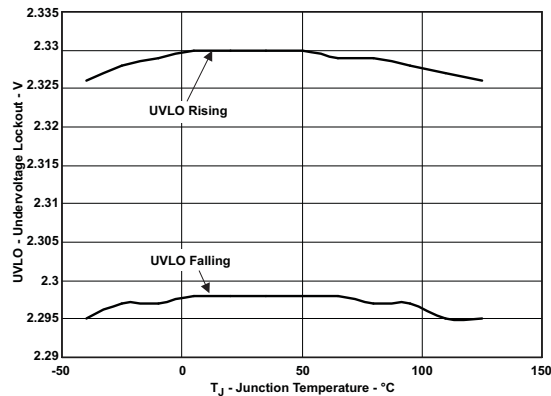


Figure 1. UVLO – Undervoltage Lockout – V

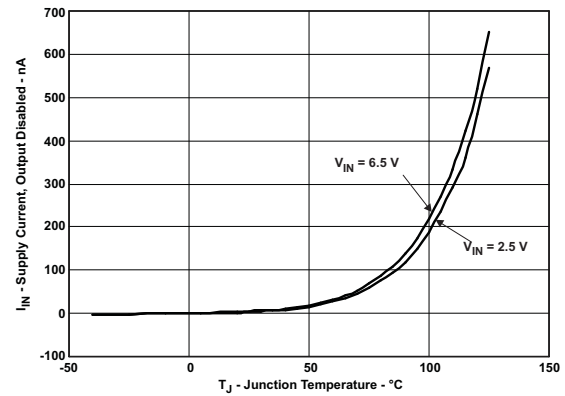
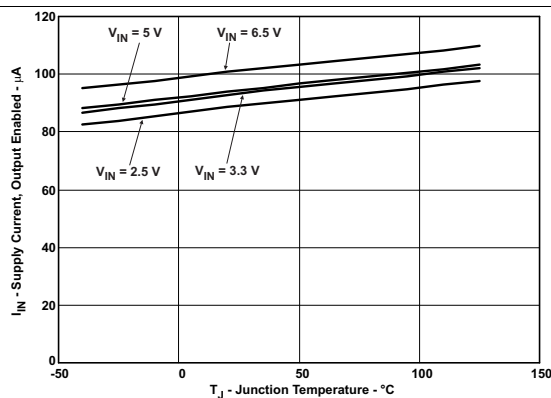
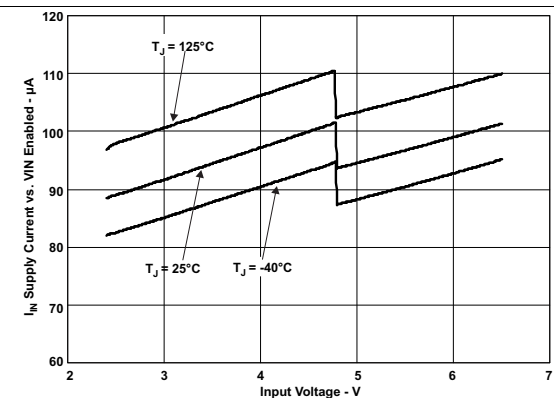


Figure 2.  $I_{IN}$  – Supply Current, Output Disabled – nA



$R_{LIM} = 20\text{ k}\Omega$

Figure 3.  $I_{IN}$  – Supply Current, Output Enabled –  $\mu A$



$R_{LIM} = 20\text{ k}\Omega$

Figure 4.  $I_{IN}$  – Supply Current, Output Enabled –  $\mu A$

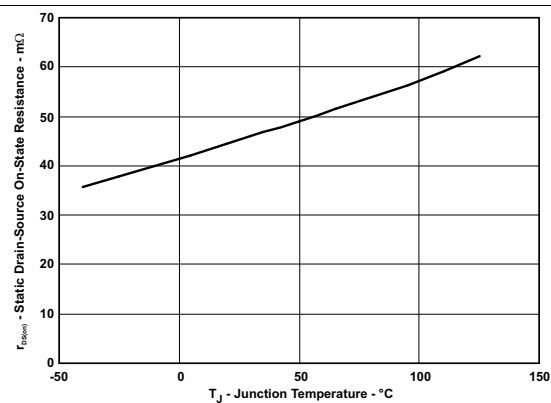
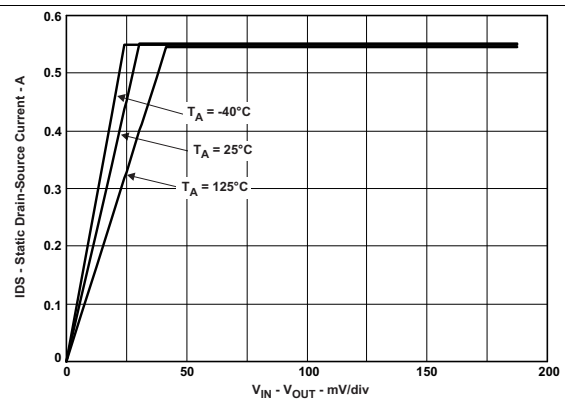


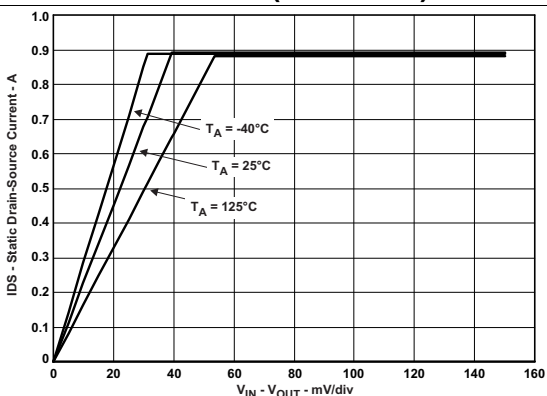
Figure 5. MOSFET  $r_{DS(on)}$  Vs. Junction Temperature



$R_{LIM} = 100\text{ k}\Omega$

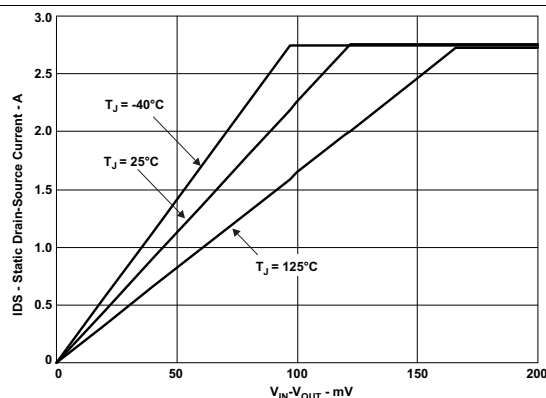
Figure 6. Switch Current Vs. Drain-Source Voltage Across Switch

## Typical Characteristics (continued)



$R_{LIM} = 61.9 \text{ k}\Omega$

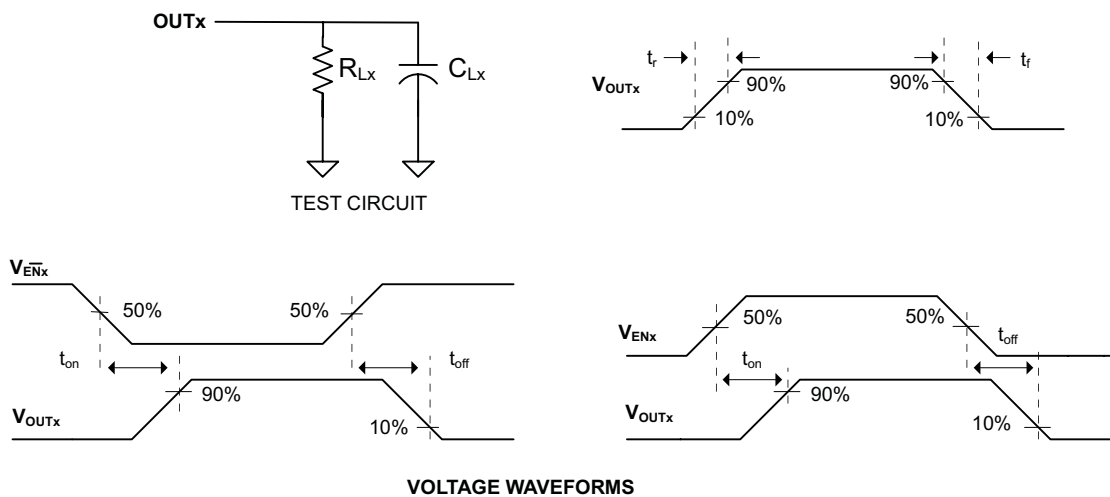
**Figure 7. Switch Current Vs. Drain-Source Voltage Across Switch**



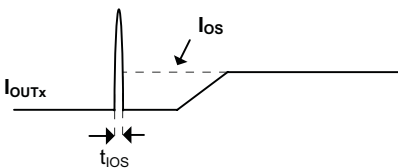
$R_{LIM} = 20 \text{ k}\Omega$

**Figure 8. Switch Current vs. Drain-Source Voltage Across Switch**

## 8 Parameter Measurement Information

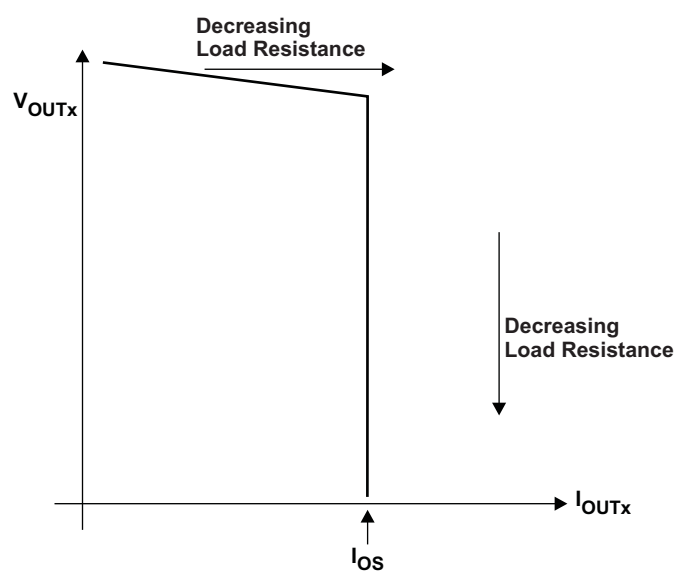


**Figure 9. Test Circuit and Voltage Waveforms**



**Figure 10. Response Time to Short Circuit Waveform**

# Parameter Measurement Information (continued)



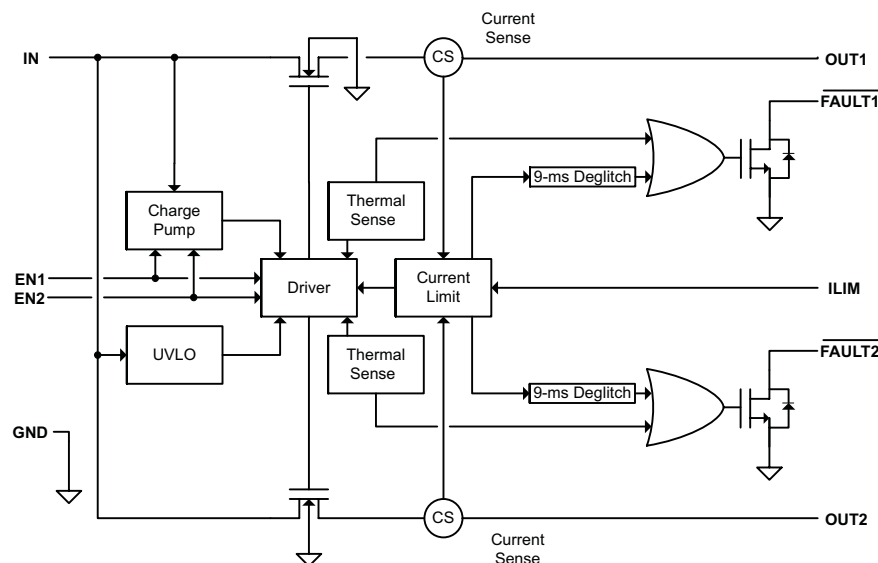
**Figure 11. Output Voltage vs. Current-Limit Threshold**

## 9 Detailed Description

### 9.1 Overview

The TPS2561A-Q1 is a dual-channel, current-limited power-distribution switch using N-channel MOSFETs for automotive applications where short circuits or heavy capacitive loads will be encountered. This device allows the user to program the current-limit threshold between 250 mA and 2.8 A (typ) per channel via an external resistor. This device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFETs. The charge pump supplies power to the driver circuit for each channel and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.5 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. Each channel of the TPS2561A-Q1 limits the output current to the programmed current-limit threshold  $I_{OS}$  during an overcurrent or short-circuit event by reducing the charge pump voltage driving the N-channel MOSFET and operating it in the linear range of operation. The result of limiting the output current to  $I_{OS}$  reduces the output voltage at OUTx because the N-channel MOSFET is no longer fully enhanced.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

#### 9.3.1 Overcurrent Conditions

The TPS2561A-Q1 responds to overcurrent conditions by limiting the output current per channel to  $I_{OS}$ . When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS2561A-Q1 ramps the output current to  $I_{OS}$ . The TPS2561A-Q1 devices will limit the current to  $I_{OS}$  until the overload condition is removed or the device begins to thermal cycle.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time  $t_{IOS}$  (see Figure 10). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and ramps the output current to  $I_{OS}$ . Similar to the previous case, the TPS2561A-Q1 will limit the current to  $I_{OS}$  until the overload condition is removed or the device begins to thermal cycle.

## Feature Description (continued)

The TPS2561A-Q1 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (min) while in current limit. The device remains off until the junction temperature cools 20°C (typ) and then restarts. The TPS2561A-Q1 cycles on/off until the overload is removed (see [Figure 20](#)).

### 9.3.2 FAULTx Response

The FAULTx open-drain outputs are asserted (active low) on an individual channel during an overcurrent or overtemperature condition. The TPS2561A-Q1 asserts the FAULTx signal until the fault condition is removed and the device resumes normal operation on that channel. The TPS2561A-Q1 is designed to eliminate false FAULTx reporting by using an internal delay "deglitch" circuit (9-ms typ) for overcurrent conditions without the need for external circuitry. This ensures that FAULTx is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limited induced fault conditions. The FAULTx signal is not deglitched when the MOSFET is disabled due to an overtemperature condition but is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch prevents FAULTx oscillation during an overtemperature event.

### 9.3.3 Thermal Sense

The TPS2561A-Q1 self protects by using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. Each channel of the TPS2561A-Q1 operates in constant-current mode during an overcurrent condition, which increases the voltage drop across the power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor (OTSD) turns off the individual power switch channel when the die temperature exceeds 135°C (min) and the channel is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C.

The TPS2561A-Q1 also has a second ambient thermal sensor (OTSD2). The ambient thermal sensor turns off both power switch channels when the die temperature exceeds 155°C (min) regardless of whether the power switch channels are in current limit and will turn on the power switches after the device has cooled approximately 20°C. The TPS2561A-Q1 continues to cycle off and on until the fault is removed.

## 9.4 Device Functional Mode

### 9.4.1 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage droop during turn on.

### 9.4.2 Enable (ENx)

The logic enables control the power switches and device supply current. The supply current is reduced to less than 2-μA when a logic low is present on ENx. A logic high input on ENx enables the driver, control circuits, and power switches. The enable inputs are compatible with both TTL and CMOS logic levels.

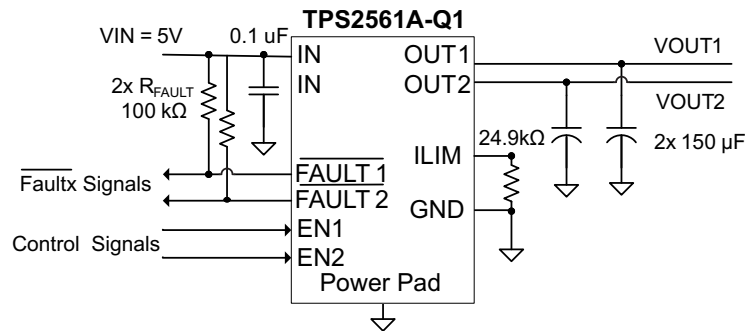
## 10 Application and Implementation

### 10.1 Application Information

The device is current-limited, power-distribution switch. It would limit the output current to IOS when short circuits or heavy capacitive loads are encountered.

### 10.2 Typical Application

#### 10.2.1 Design Current Limit



**Figure 12. Typical Characteristics Reference Schematic**

##### 10.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

**Table 1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	5V
Minimum current limit	2A
Maximum current limit	1A

##### 10.2.1.2 Detailed Design Procedure

###### 10.2.1.2.1 Determine Design Parameters

Beginning the design process requires deciding on a few parameters. The designer must know the following:

- Input voltage
- Minimum current limit
- Maximum current limit

###### 10.2.1.2.2 Programming the Current-Limit Threshold

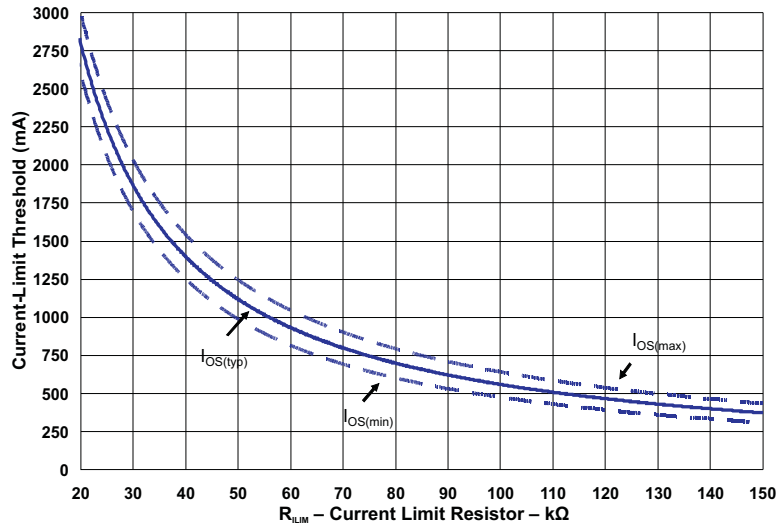
The overcurrent threshold is user programmable via an external resistor,  $R_{ILIM}$ .  $R_{ILIM}$  sets the current-limit threshold for both channels. The TPS2561A-Q1 use an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for  $R_{ILIM}$  is  $20\text{ k}\Omega \leq R_{ILIM} \leq 187\text{ k}\Omega$  to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for  $R_{ILIM}$ . The following equations calculates the resulting overcurrent threshold for a given external resistor value ( $R_{ILIM}$ ). The traces routing the  $R_{ILIM}$  resistor to the TPS2561A-Q1 should be as short as possible to reduce parasitic effects on the current-limit accuracy.

$$I_{OSmax}(mA) = \frac{49497V}{R_{(ILIM)}^{0.933}k\Omega} - 37$$

$$I_{OSnom}(mA) = \frac{53098V}{R_{(ILIM)}^{0.989}k\Omega}$$

$$I_{OSmin}(mA) = \frac{50576V}{R_{(ILIM)}^{0.987}k\Omega} - 64$$

(1)



**Figure 13. Current-Limit Threshold vs.  $R_{ILIM}$**

#### 10.2.1.2.3 Designing Above a Minimum Current Limit

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 2 A must be delivered to the load so that the minimum desired current-limit threshold is 2000 mA. Use the  $I_{OS}$  equations and [Figure 13](#) to select  $R_{ILIM}$ .

$$I_{OSmin}(mA) = 2000 \text{ mA}$$

$$I_{OSmin}(mA) = \frac{50576V}{R_{(ILIM)}^{0.987}k\Omega} - 64$$

$$R_{(ILIM)}(k\Omega) = \left( \frac{50576}{I_{OS(min)} + 64} \right)^{\frac{1}{0.987}} = \left( \frac{50576}{2000 + 64} \right)^{\frac{1}{0.987}} = 25.56k\Omega$$

Select the closest 1% resistor less than the calculated value:  $R_{ILIM} = 25.5 \text{ k}\Omega$ . This sets the minimum current-limit threshold at 2005 mA .

$$I_{OSmin}(mA) = \frac{50576}{R_{(ILIM)}^{0.987}k\Omega} - 64 = \frac{50576}{(25.5)^{0.987}} - 64 = 2005 \text{ mA}$$

Use the  $I_{OS}$  equations, [Figure 13](#), and the previously calculated value for  $R_{ILIM}$  to calculate the maximum resulting current-limit threshold at 2374 mA.

$$I_{OSmax}(mA) = \frac{49497}{R_{(ILIM)}^{0.933}} - 37 = \frac{49497}{(25.5)^{0.933}} - 37 = 2374 \text{ mA}$$

#### 10.2.1.2.4 Designing Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that 1 A must be delivered to the load so that the minimum desired current-limit threshold is 1000 mA. Use the  $I_{OS}$  equations and [Figure 13](#) to select  $R_{ILIM}$ .

$$I_{OSmax}(mA) = 1000 \text{ mA}$$

$$I_{OSmax}(mA) = \frac{49497}{R_{(ILIM)}^{0.933} k\Omega} - 37$$

$$R_{(ILIM)}(k\Omega) = \left( \frac{49497}{I_{OS(max)}} \right)^{\frac{1}{0.933}} = \left( \frac{49497}{1000 + 37} \right)^{\frac{1}{0.933}} = 63k\Omega \quad (5)$$

Select the closest 1% resistor greater than the calculated value:  $R_{ILIM} = 63.4 \text{ k}\Omega$ . This sets the maximum current-limit threshold at 994 A.

$$I_{OSmax}(mA) = \frac{49497}{R_{(ILIM)}^{0.933} k\Omega} - 37 = \frac{49497}{(63.4)^{0.933}} - 37 = 994 \text{ mA} \quad (6)$$

Use the  $I_{OS}$  equations, [Figure 13](#), and the previously calculated value for  $R_{ILIM}$  to calculate the minimum resulting current-limit threshold at 778 mA.

$$I_{OSmin}(mA) = \frac{50576}{R_{(ILIM)}^{0.987}} - 64 = \frac{50576}{(63.4)^{0.987}} - 64 = 778 \text{ mA} \quad (7)$$

#### 10.2.1.2.5 Accounting for Resistor Tolerance

The previous sections described the selection of  $R_{ILIM}$  given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focused only on the TPS2561A-Q1 performance and assumed an exact resistor value. However, resistors sold in quantity are not exact and are bounded by an upper and lower tolerance centered around a nominal resistance. The additional  $R_{ILIM}$  resistance tolerance directly affects the current-limit threshold accuracy at a system level. The following table shows a process that accounts for worst-case resistor tolerance assuming 1% resistor values. Step one follows the selection process outlined in the application examples above. Step two determines the upper and lower resistance bounds of the selected resistor. Step three uses the upper and lower resistor bounds in the  $I_{OS}$  equations to calculate the threshold limits. It is important to use tighter tolerance resistors, that is, 0.5% or 0.1%, when precision current limiting is desired.

**Table 2. Common  $R_{ILIM}$  Resistor Selections**

Desired Nominal Current Limit (mA)		Ideal Resistor (kΩ)	Closest 1% Resistor (kΩ)	Resistor Tolerance		Actual Limits		
				1% low (kΩ)	1% high (kΩ)	IOS MIN (mA)	IOS Nom (mA)	IOS MAX (mA)
300		187.5	187	185.1	188.9	223	301	342
550		101.6	102	101.0	103.0	457	548	631
800		69.5	69.8	69.1	70.5	694	797	914
1050		52.8	52.3	51.8	52.8	944	1060	1208
1300		42.6	42.2	41.8	42.6	1182	1311	1484
1550		35.6	35.7	35.3	36.1	1406	1547	1741
1800		30.6	30.9	30.6	31.2	1631	1784	1998
2050		26.9	26.7	26.4	27.0	1894	2062	2295
2300		23.9	23.7	23.5	23.9	2138	2320	2569
2550		21.5	21.5	21.3	21.7	2360	2554	2817
2800		19.6	19.6	19.4	19.8	2592	2799	3075

### 10.2.1.2.6 Power Dissipation and Junction Temperature

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

Begin by determining the  $r_{DS(on)}$  of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read  $R_{DS(on)}$  from the typical characteristics graph. Using this value, the power dissipation can be calculated by:

$$P_D = (R_{DS(on)} \times I_{OUT1}^2) + (R_{DS(on)} \times I_{OUT2}^2)$$

Where:

$P_D$  = Total power dissipation (W)

$r_{DS(on)}$  = Power switch on-resistance of one channel ( $\Omega$ )

$I_{OUTx}$  = Maximum current-limit threshold set by  $R_{ILIM}(A)$

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A$$

Where:

$T_A$  = Ambient temperature ( $^{\circ}C$ )

$\theta_{JA}$  = Thermal resistance ( $^{\circ}C/W$ )

$P_D$  = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined"  $R_{DS(on)}$  from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance  $\theta_{JA}$ , and thermal resistance is highly dependent on the individual package and board layout. The [Thermal Characteristics Table](#) provides example thermal resistances for specific packages and board layouts.

#### 10.2.1.2.7 Auto-Retry Functionality

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This auto-retry functionality can be implemented with an external resistor and capacitor. During a fault condition,  $\overline{\text{FAULTx}}$  pulls  $\text{ENx}$  low disabling the part. The part is disabled when  $\text{ENx}$  is pulled below the turn-off threshold, and  $\overline{\text{FAULTx}}$  goes high impedance allowing  $\text{C}_{\text{RETRY}}$  to begin charging. The part re-enables when the voltage on  $\text{ENx}$  reaches the turn-on threshold, and the auto-retry time is determined by the resistor, capacitor time constant. The part will continue to cycle in this manner until the fault condition is removed.

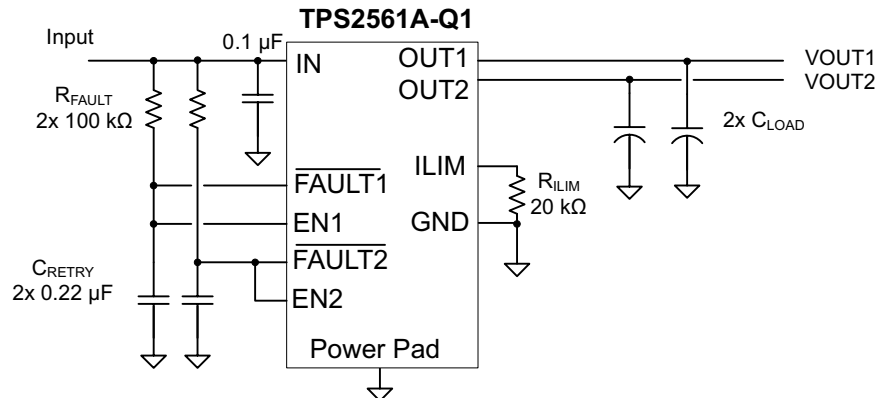


Figure 14. Auto-Retry Functionality

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. The figure below shows how an external logic signal can drive  $\text{EN}$  through  $\text{R}_{\text{FAULT}}$  and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

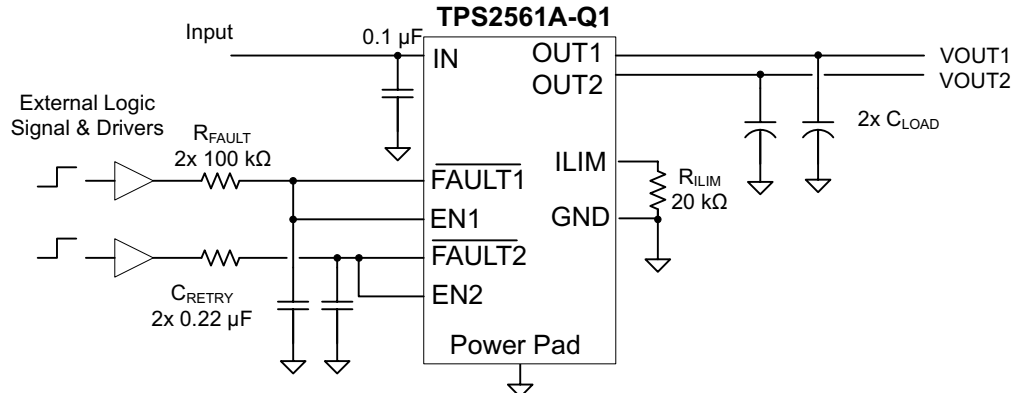


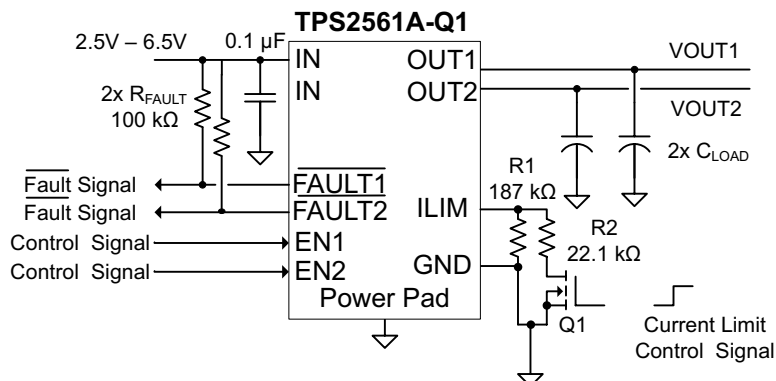
Figure 15. Auto-Retry Functionality With External EN Signal

### 10.2.1.2.8 Two-Level Current-Limit Circuit

Some applications require different current-limit thresholds depending on external system conditions. [Figure 16](#) shows an implementation for an externally controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see previously discussed *Programming the Current-Limit Threshold* section). A logic-level input enables/disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND. Additional MOSFET/resistor combinations can be used in parallel to Q1/R2 to increase the number of additional current-limit levels.

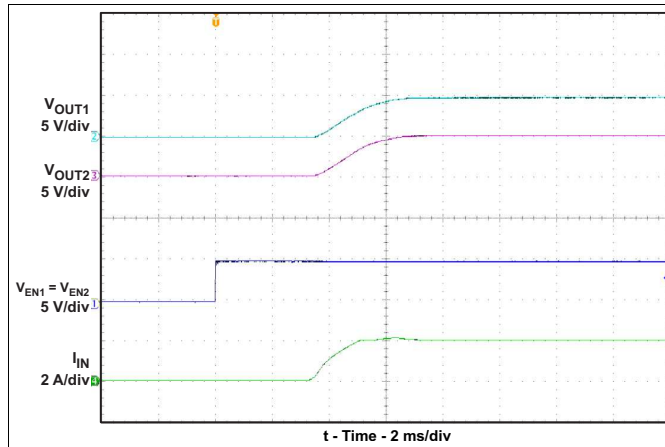
#### NOTE

ILIM should never be driven directly with an external signal.

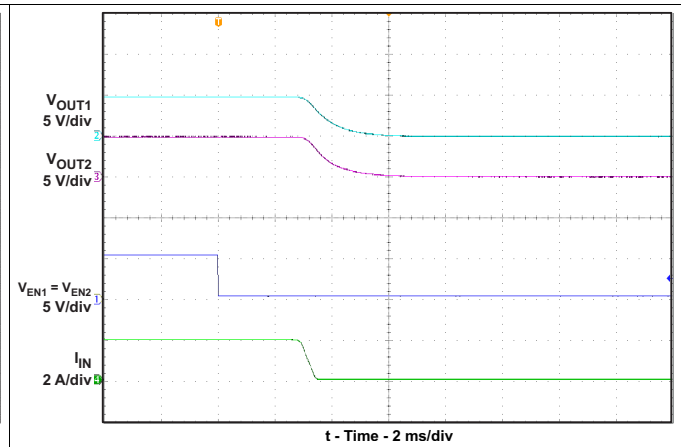


**Figure 16. Two-Level Current-Limit Circuit**

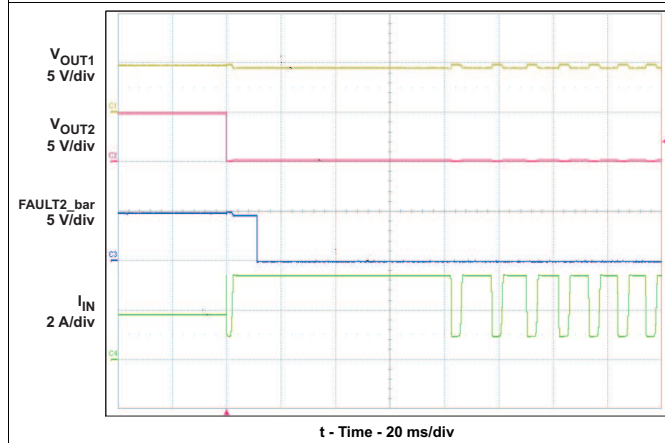
## 10.2.2 Application Curves



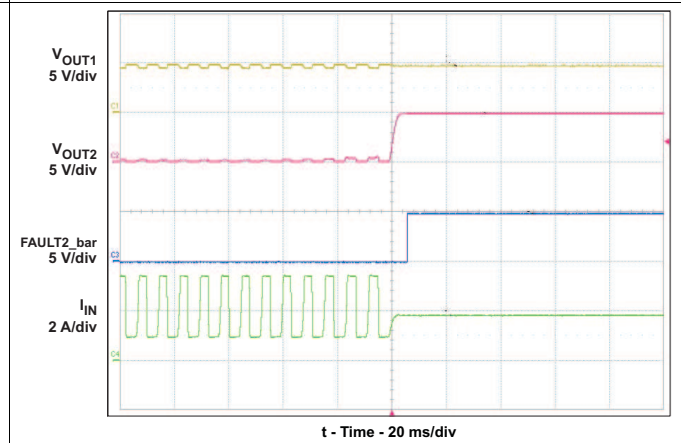
**Figure 17. Turn-on Delay and Rise Time**



**Figure 18. Turn-off Delay and Fall Time**



**Figure 19. Full-Load to Short-Circuit Transient Response**



**Figure 20. Short-Circuit to Full-Load Recovery Response**

## 11 Power Supply Requirements

The device is designed to operate from an input voltage supply range of 2.5 V to 6.5 V. The current capability of upper power should exceed the max current limit of the power switch.

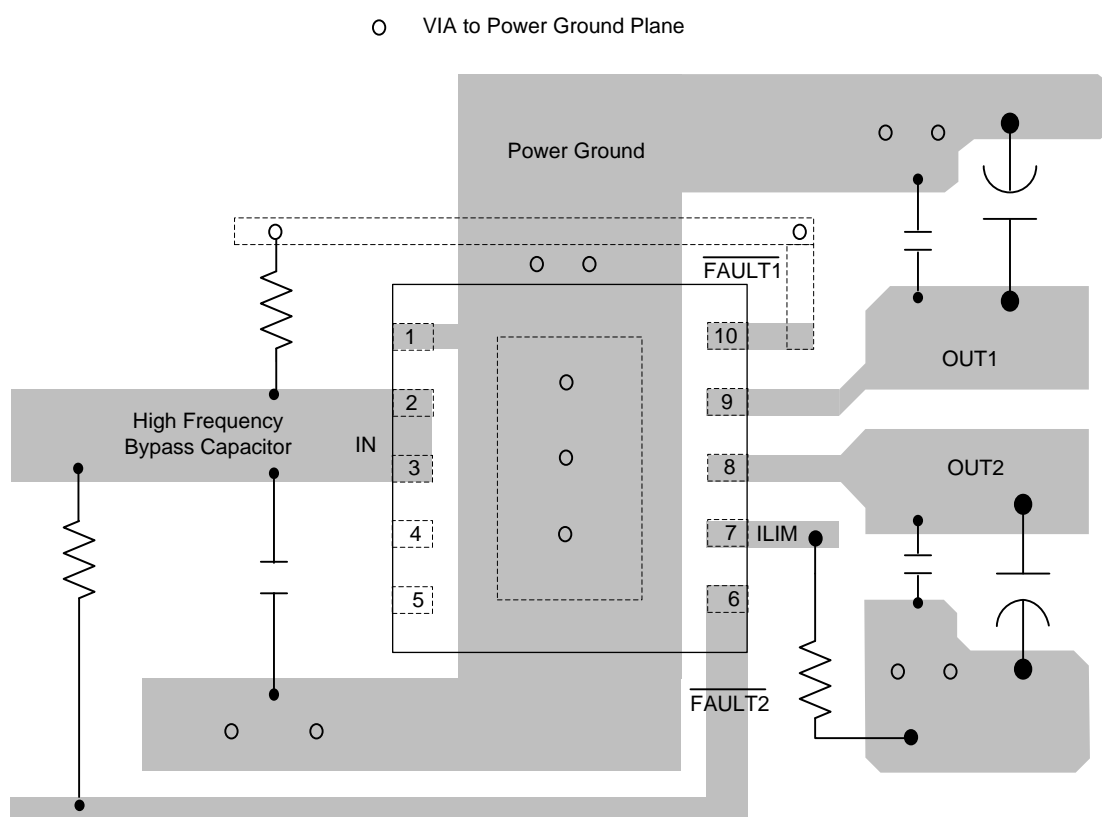
## 12 Layout

### 12.1 Layout Guidelines

For all applications, a 0.1- $\mu$ F or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute-maximum voltage of the device during heavy transient conditions.

- Output capacitance is not required, but placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.
- The traces routing the  $R_{ILIM}$  resistor to the device should be as short as possible to reduce parasitic effects on the current limit accuracy.
- The PowerPAD™ should be directly connected to PCB ground plane using wide and short copper trace.

### 12.2 Layout Example



## 13 Device and Documentation Support

### 13.1 Trademarks

PowerPAD is a trademark of Texas Instruments.

### 13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS2561AQDRCRQ1</a>	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2561AQ
TPS2561AQDRCRQ1.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2561AQ
<a href="#">TPS2561AQDRCTQ1</a>	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2561AQ
TPS2561AQDRCTQ1.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2561AQ

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS2561A-Q1 :**

- Catalog : [TPS2561A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2561AQDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2561AQDRCTQ1	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2561AQDRCRQ1	VSON	DRC	10	3000	346.0	346.0	33.0
TPS2561AQDRCTQ1	VSON	DRC	10	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

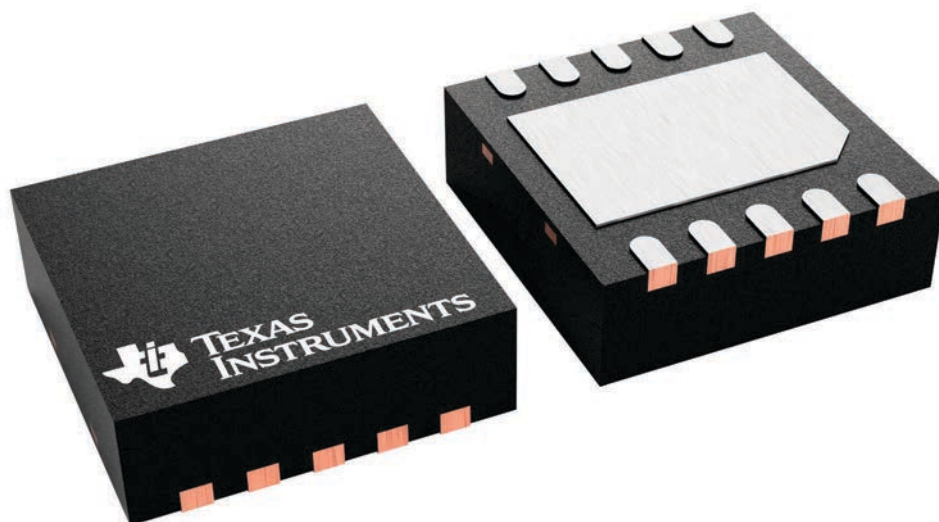
**DRC 10**

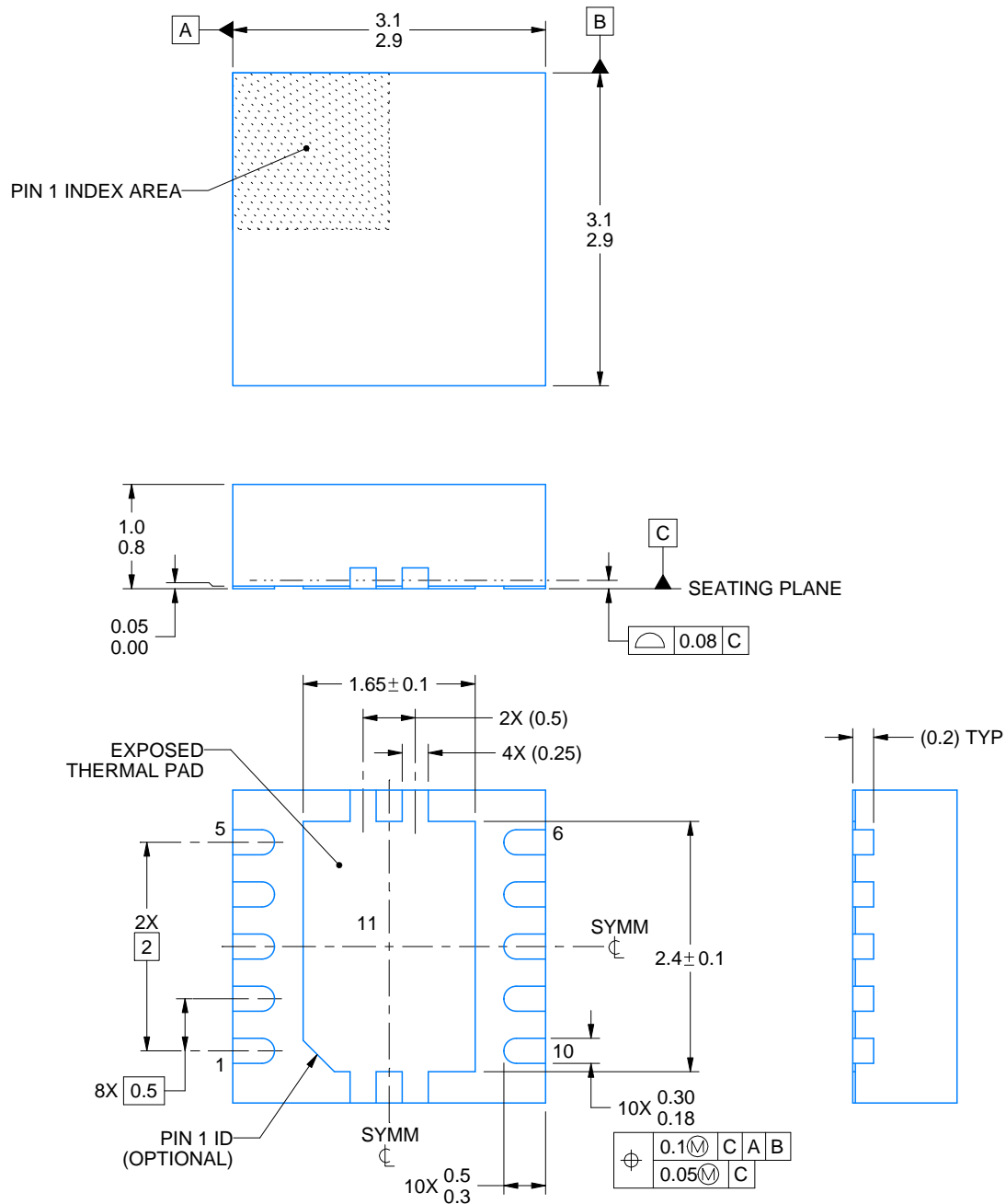
**VSON - 1 mm max height**

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.





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## NOTES:

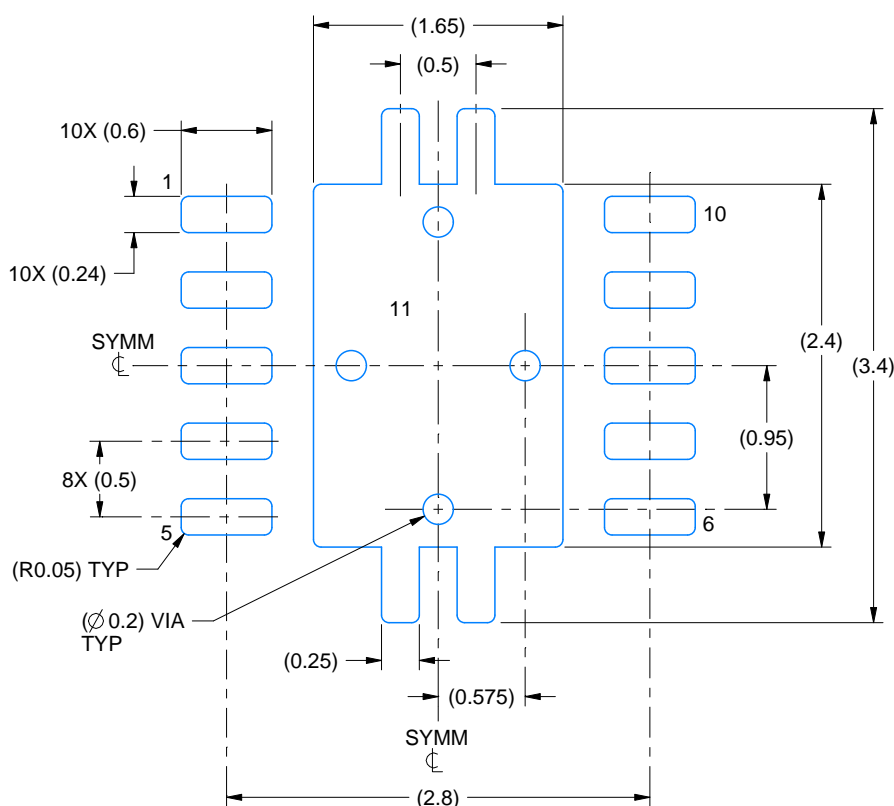
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

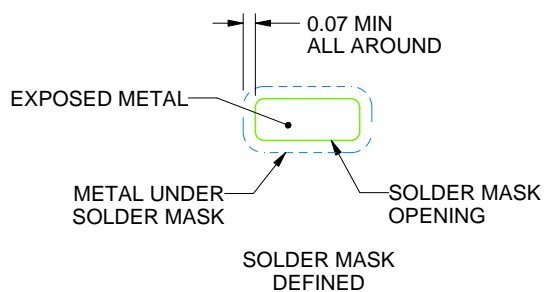
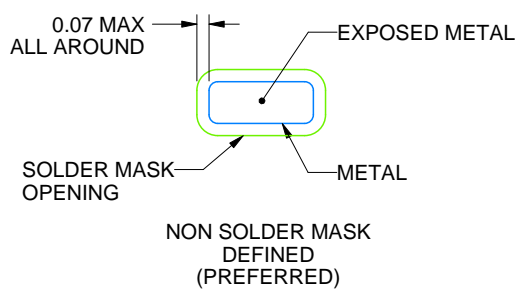
DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

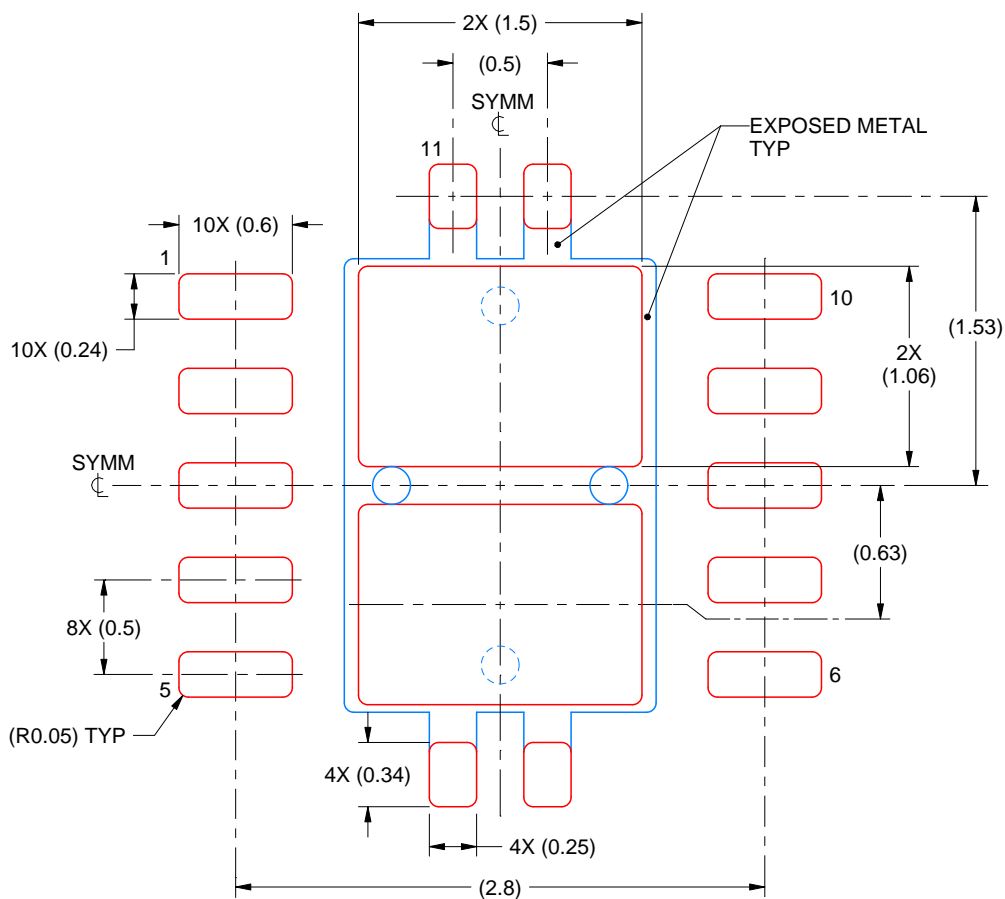
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**DRC0010J**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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