

TPS25730A USB Type-C® and USB PD Controller With Integrated Power Switches Optimized for Sink Power Applications

1 Features

- This device is certified by the USB-IF for PD3.2
 - TPS25730A TID#: 15340
 - Article on [PD2.0 vs. PD3.0](#)
- Fully configurable single port PD controller
 - Optimized for sink only USB Type-C and USB PD applications
 - Complete barrel jack replacement for to USB Type-C
 - Fully configurable with pin strapping
 - Industrial temperature range supported
- Fully managed integrated power path
 - Integrated overvoltage protection and reverse current protection
- Additional features
 - 6 GPIO set functions
 - Cable attach and orientation detection
 - Integrated dead battery Rd
 - Physical layer and policy engine
 - 3.3V LDO output for dead battery support
 - Power supply from 3.3V or VBUS source
 - I2C access for external microcontroller

2 Applications

- [WLAN/Wi-Fi access point, power banks, retail automation and payment](#)
- [Wireless speakers, headphones](#)
- Other [personal electronics](#) and [industrial applications](#)

3 Description

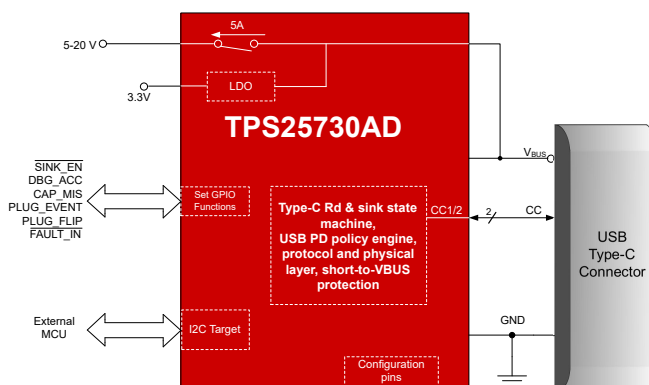
The TPS25730A is a highly integrated stand-alone USB Type-C and power delivery (PD) controller optimized for applications supporting USB-C PD power. The TPS25730A integrates fully managed power paths with robust protection for a complete USB-C PD application. The TPS25730A also has the ability to control an external power path through the use of internal gate drivers. The TPS25730A is best suited for sink only applications that have previously been powered by a barrel jack. Using resistor pin strapping, a user can implement a fully featured USB Type-C PD port with the TPS25730A. There is no need for an external EEPROM, an external microcontroller, or any type of firmware development.

The TPS25730A is intended to make setting up a sink only USB Type-C application simple yet robust. A user has all of the benefits of a barrel jack port, while now taking advantage of the benefits of USB Type-C and USB Type-C PD.

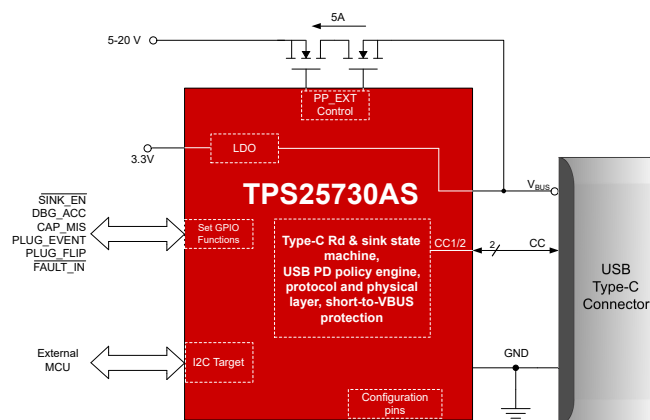
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TPS25730AD	38-WQFN (REF)	4.00mm x 6.00mm
TPS25730A S	32-VQFN (RSM)	4.00mm x 4.00mm

- For all available packages, see the orderable addendum at the end of the datasheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.



TPS25730AD Schematic



TPS25730AS Schematic



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4 Device Comparison Table

DEVICE NUMBER	INTEGRATED HIGH VOLTAGE SINK LOAD SWITCH (PPHV)	HIGH VOLTAGE GATE DRIVER FOR EXTERNAL SINK PATH (PP_EXT)
TPS25730AD	Yes	No
TPS25730AS	No	Yes

5 Pin Configuration and Functions

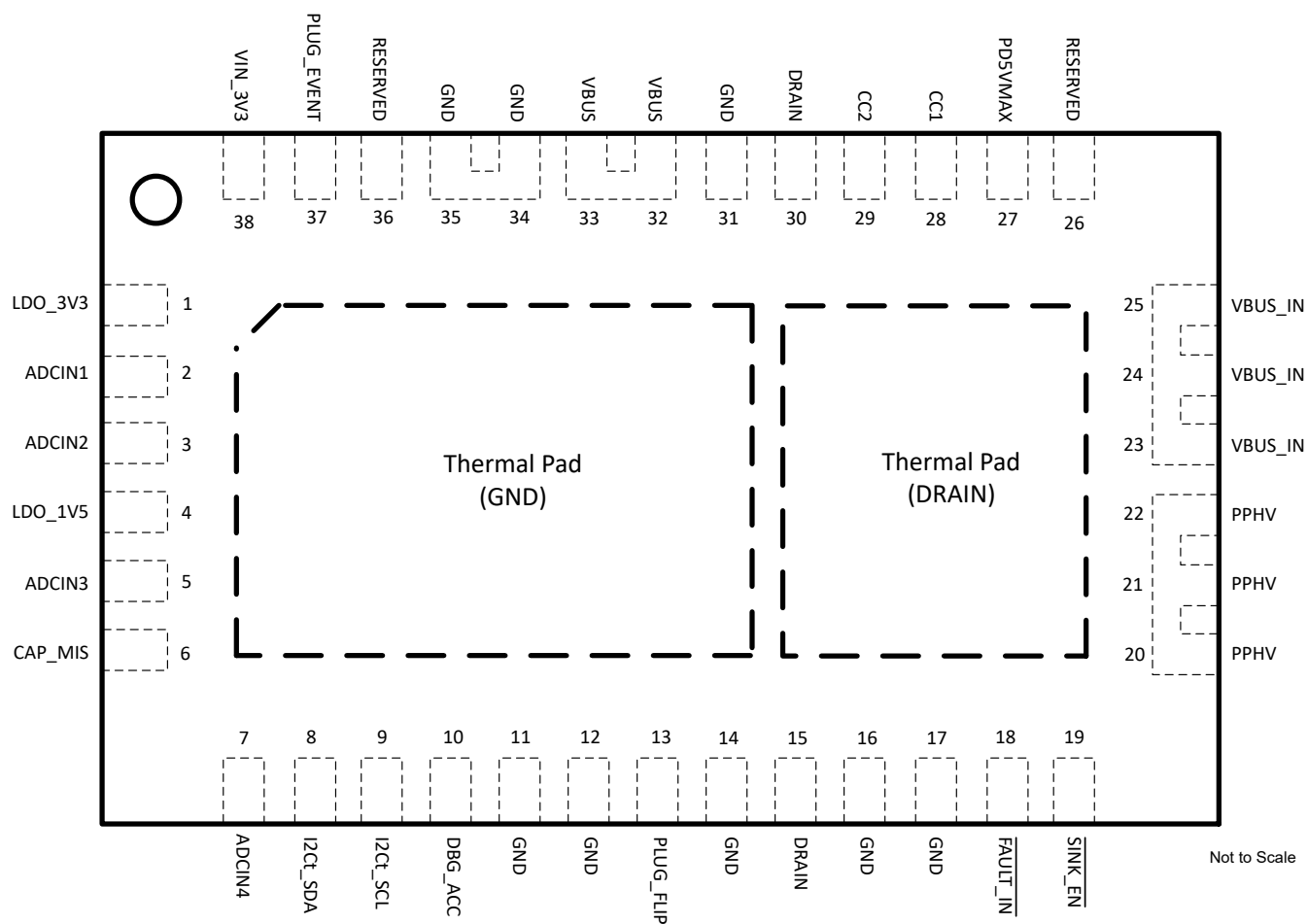


Figure 5-1. TPS25730AD QFN Package, 38-Pin (Top View)

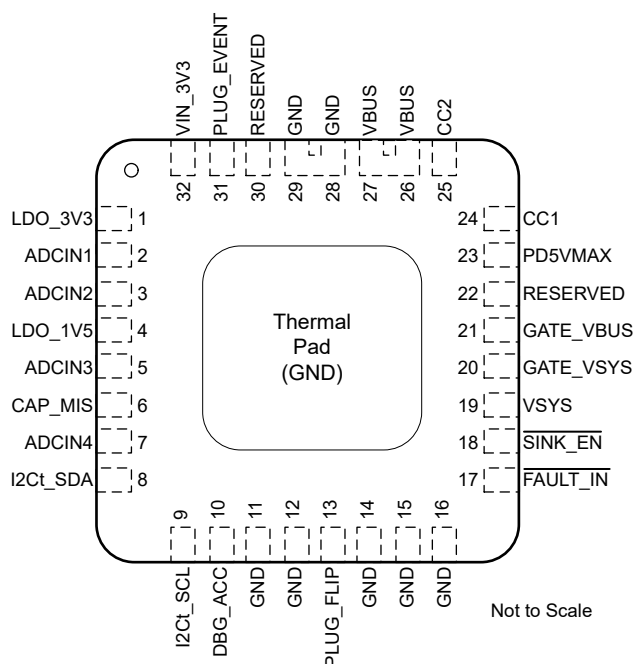


Figure 5-2. TPS25730AS QFN Package, 32-Pin (Top View)

Table 5-1. TPS25730AD Pin Functions

PIN		TYPE ⁽¹⁾	RESET	DESCRIPTION
NAME	NO.			
ADCIN1	2	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
ADCIN2	3	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CC1	28	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (C _{CC}).
CC2	29	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (C _{CC}).
GND	11, 12, 14, 16, 17, 31, 34, 35	—	—	Ground. Connect to ground plane.
ADCIN3	5	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CAP_MIS	6	O	Hi-Z	Open Drain Output, Capability Mismatch indicator. Toggled Output: Capability Mismatch in negotiated PD contract, No Toggled Output: No Capability Mismatch in negotiated PD contract.
ADCIN4	7	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
SINK_EN	19	O	Hi-Z	Open Drain Output, Sink path enabled indicator. Used to control an external load switch. 0: Sink Path Enabled, 1: Sink Path Disabled
PD5VMAX	27	I	Hi-Z	Configuration Input. Tie to ground or LDO_3V3.
RESERVED	26, 36	I	Hi-Z	Tie to ground or LDO_3V3.
PLUG_EVENT	37	O	Hi-Z	Open Drain Output, 1: Connection Present 0: No Connection Present
I2Ct_SCL	9	I	Hi-Z	I2C target serial clock input. Tie to pullup voltage through a resistor. Tie to ground when pin is unused.
I2Ct_SDA	8	I/O	Hi-Z	I2C target serial data. Open-drain input/output. Tie to pullup voltage through a resistor. Tie to ground when pin is unused.
DBG_ACC	10	O	Hi-Z	Open Drain Output, Debug Accessory attached Rp/Rp. 1: Debug Accessory Present, 0: No Debug Accessory Present
PLUG_FLIP	13	O	Hi-Z	Open Drain Output, Cable plug orientation indicator. 1: CC2 connected (upside-down), 0: CC1 connected (upside-up)
FAULT_IN	18	I	Hi-Z	Fault Input to trigger Type-C error recovery and disconnect from the port. 1: Maintain connection - no fault. Connect to fault signal from peripheral MCU or protection device. Tie up to LDO3V3 using a pullup resistor.

Table 5-1. TPS25730AD Pin Functions (continued)

PIN		TYPE ⁽¹⁾	RESET	DESCRIPTION
NAME	NO.			
LDO_1V5	4	O	—	Output of the CORE LDO. Bypass with capacitance C_{LDO_1V5} to GND. This pin cannot source current to external circuits.
LDO_3V3	1	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance C_{LDO_3V3} to GND.
DRAIN	15, 30	N/A	—	Connects to drain of internal FET.
PPHV	20, 21, 22	I/O		High-voltage sinking node in the system.
VBUS_IN	23, 24, 25	I/O		5V to 20V input.
VBUS	32, 33	O		VBUS input to LDO. Bypass with capacitance C_{VBUS} to GND.
VIN_3V3	38	I	—	Supply for core circuitry and I/O. Bypass with capacitance C_{VIN_3V3} to GND. Tie to GND if device is VBUS powered only.

(1) I = input, O = output, I/O = input and output, GPIO = general purpose digital input and output

Table 5-2. TPS25730A S Pin Functions

PIN		TYPE ⁽¹⁾	RESET	DESCRIPTION
NAME	NO.			
ADCIN1	2	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
ADCIN2	3	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CC1	24	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (C _{CC}).
CC2	25	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (C _{CC}).
GATE_VSYS	20	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to VSYS
GATE_VBUS	21	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to VBUS
GND	11, 12, 14, 15, 16, 28, 29	—	—	Ground. Connect to ground plane.
ADCIN3	5	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CAP_MIS	6	O	Hi-Z	Open Drain Output, Capability Mismatch indicator. Toggled Output: Capability Mismatch in negotiated PD contract, No Toggled Output: No Capability Mismatch in negotiated PD contract.
ADCIN4	7	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
SINK_EN	18	O	Hi-Z	Open Drain Output, Sink path enabled indicator. Used to control an external load switch. 0: Sink Path Enabled, 1: Sink Path Disabled
PD5VMAX	23	I	Hi-Z	Configuration Input. Tie to ground or LDO_3V3.
RESERVED	22, 30	I	Hi-Z	Tie to ground.
PLUG_EVENT	31	O	Hi-Z	Open Drain Output, 1: Connection Present 0: No Connection Present
I2Ct_SCL	9	I	Hi-Z	I2C target serial clock input. Tie to pullup voltage through a resistor. Tie to ground if unused.
I2Ct_SDA	8	I/O	Hi-Z	I2C target serial data. Open-drain input/output. Tie to pullup voltage through a resistor. Tie to ground if unused.
DBG_ACC	10	O	Hi-Z	Open Drain Output, Debug Accessory attached Rp/Rp or Rd/Rd. 1: Debug Accessory Present, 0: No Debug Accessory Present
PLUG_FLIP	13	O	Hi-Z	Open Drain Output, Cable plug orientation indicator. 1: CC2 connected (upside-down), 0: CC1 connected (upside-up)
FAULT_IN	17	I	Hi-Z	Fault Input to trigger Type-C error recovery and disconnect from the port. 0: Disconnect from port, 1: Maintain connection - no fault. Connect to fault signal from peripheral MCU or protection device. Tie up to LDO3V3 using a pullup resistor.
LDO_1V5	4	O	—	Output of the CORE LDO. Bypass with capacitance C _{LDO_1V5} to GND. This pin cannot source current to external circuits.
LDO_3V3	1	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance C _{LDO_3V3} to GND.
VSYS	19	I	—	System side high voltage sensing node. High-voltage sinking node in the system. Used to implement reverse current protection (RCP) for the external sink path controlled by GATE_VSYS.
VBUS	26, 27	I/O		5V to 20V input. Bypass with capacitance C _{VBUS} to GND.
VIN_3V3	32	I	—	Supply for core circuitry and I/O. Bypass with capacitance C _{VIN_3V3} to GND. Tie to GND if device is VBUS powered only.

(1) I = input, O = output, I/O = input and output, GPIO = general purpose digital input and output

6 Specifications

6.1 Absolute Maximum Ratings

6.1.1 TPS25730AD and TPS25730AS - Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)¹

PARAMETER		MIN	MAX	UNIT
Input voltage range ²	VIN_3V3	−0.3	4	V
Input voltage range ²	ADCINx	−0.3	4	V
Input voltage range ²	VBUS_IN, VBUS ⁴	−0.3	28	V
Input voltage range ²	CC1, CC2 ⁴	−0.5	26	V
Input voltage range ²	GPIOx	−0.3	6	V
Input voltage range ²	I2Ct_SCL, I2Ct_SDA	−0.3	4	V
Output voltage range ²	LDO_1V5 ³	−0.3	2	V
	LDO_3V3 ³	−0.3	4	
Source current	Sink current VBUS	internally limited		A
	Positive source current for LDO_3V3, LDO_1V5	internally limited		
Source current	GPIOx	0.005		A
T _J Operating junction temperature		−40	175	°C
T _{STG} Storage temperature		−55	150	°C

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent damage to the device. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
- (3) Do not apply voltage to these pins.
- (4) A TVS with a break down voltage falling between the Recommended max and the Abs max value is recommended such as TVS2200.

6.1.2 TPS25730AD - Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNIT
Input voltage range ¹	PPHV	−0.3	28	V
V _{PPHV_VBUS_IN}	Source-to-source voltage		28	V
Sink current	Continuous current to/from VBUS_IN to PPHV		7	A
	Pulsed current to/from VBUS_IN to PPHV ²		10	
T _{J_PPHV} Operating junction temperature	PP_HV switch	−40	175	°C

- (1) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
- (2) Pulse duration ≤ 100 μs and duty-cycle ≤ 1%.

6.1.3 TPS25730AS - Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNIT
Output voltage range ¹	GATE_VBUS, GATE_VSYS ²	−0.3	40	V
V _{GS}	V _{GATE_VBUS} - V _{VBUS} , V _{GATE_SYS} - V _{VSYS}	−0.5	12	V

- (1) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
- (2) Do not apply voltage to these pins.

6.2 ESD Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3.1 TPS25730AD - Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER			MIN	MAX	UNIT
V _I	Input voltage range ⁽¹⁾	VIN_3V3	3.0	3.6	V
V _I	Input voltage range ⁽¹⁾	ADCIN1, ADCIN2, VBUS_IN, VBUS	4	22	V
V _I	Input voltage range ⁽¹⁾	PPHV	0	22	V
V _{IO}	I/O voltage range ⁽¹⁾	I2Ct_SDA, I2Ct_SCL, ADCINx	0	3.6	V
		GPIOx	0	5.5	
		CC1, CC2	0	5.5	
I _{PP_HV}	Current from VBUS_IN to PPHV			7	A
I _O	Output current (from LDO_3V3)	GPIOx		1	mA
I _O	Output current (from VBUS LDO)	Sum of current from LDO_3V3		5	mA
T _A	Ambient operating temperature	I _{PP_HV} ≤ 7A	−40	45	°C
		I _{PP_HV} ≤ 6A	−40	65	
T _{J_PPHV}	Operating junction temperature	PP_HV switch	−40	150	°C
T _J	Operating junction temperature		−40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

6.3.2 TPS25730AS - Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER			MIN	MAX	UNIT
V _I	Input voltage range ⁽¹⁾	VIN_3V3	3.0	3.6	V
V _I	Input voltage range ⁽¹⁾	VBUS ²	4	22	V
V _I	Input voltage range ⁽¹⁾	VSYS	0	22	V
V _{IO}	I/O voltage range ⁽¹⁾	I2Cx_SDA, I2Cx_SCL, ADCINx	0	3.6	V
		GPIOx	0	5.5	
		CC1, CC2	0	5.5	
I _O	Output current (from LDO_3V3)	GPIOx		1	mA
I _O	Output current (from VBUS LDO)	Sum of current from LDO_3V3 and GPIOx		5	mA
T _J	Operating junction temperature		–40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

(2) Short all VBUS pins together.

6.4 Recommended Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER ⁽¹⁾		VOLTAGE RATING	MIN	NOM	MAX	UNIT
C _{VIN_3V3}	Capacitance on VIN_3V3	6.3V	5	10		μF
C _{LDO_3V3}	Capacitance on LDO_3V3	6.3V	5	10	25	μF
C _{LDO_1V5}	Capacitance on LDO_1V5	4V	4.5		12	μF
C _{VBUS}	Capacitance on VBUS ⁽³⁾	25V	1	4.7	10	μF
C _{VSYS} TPS25730AS	Capacitance on VSYS Sink from VBUS ⁽⁴⁾	25V		47	100	μF
C _{PPHV} TPS25730AD	Capacitance on PPHV Sink from VBUS ⁽⁴⁾	25V		47	100	μF
C _{CCy}	Capacitance on CCy pins ⁽²⁾	6.3V	200	400	480	pF

(1) Capacitance values do not include any derating factors. For example, if 5μF is required and the external capacitor value reduces by 50% at the required operating voltage, then the required external capacitor value is 10μF.

(2) Capacitance includes all external capacitance to the Type-C receptacle.

(3) The device can be configured to quickly disable the sinking power path upon certain events. When such a configuration is used, a capacitance on the higher side of this range is recommended.

(4) USB PD specification for cSnkBulkPd (100μF) is the maximum bulk capacitance allowed on a VBUS sink after a PD contract is in place. The capacitance is sufficient for all power conversion devices deriving power from the PD Controller sink path. For systems requiring greater than 100μF, VBUS surge current limiting is implemented as described in the USB3.2 specification.

6.5.1 TPS25730AD - Thermal Information

THERMAL METRIC ¹		TPS25730AD		UNIT
		QFN (REF)		
		38 PINS		
R _{θJA}	Junction-to-ambient thermal resistance (sinking through PP_HV)	57.4		°C/W
R _{θJC} (top)	Junction-to-case (top) thermal resistance (sinking through PP_HV)	30.5		°C/W
R _{θJB}	Junction-to-board thermal resistance (sinking through PP_HV)	21.1		°C/W
Ψ _{JT}	Junction-to-top characterization parameter (sinking through PP_HV)	18.2		°C/W

6.5.1 TPS25730AD - Thermal Information (continued)

THERMAL METRIC ¹		TPS25730AD	UNIT
		QFN (REF)	
		38 PINS	
Ψ _{JB}	Junction-to-board characterization parameter (sinking through PP_HV)	21.1	°C/W
R _{θJC} (bot_GND)	Junction-to-board (bottom GND pad) thermal resistance	1.8	°C/W
R _{θJC} (bot_DRAIN)	Junction-to-board (bottom DRAIN pad) thermal resistance	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5.2 TPS25730AS Thermal Information

THERMAL METRIC ⁽¹⁾		TPS25730AS		UNIT
		QFN (RSM)		
		32 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	30.5		°C/W
R _{θJC} (top)	Junction-to-case (top) thermal resistance	24.5		°C/W
R _{θJC}	Junction-to-board (bottom) thermal resistance	2		°C/W
R _{θJB}	Junction-to-board thermal resistance	9.8		°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.2		°C/W
Ψ _{JB}	Junction-to-board characterization parameter	9.7		°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Power Supply Characteristics

Operating under these conditions unless otherwise noted: $3.0V \leq V_{LDO_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN_3V3, VBUS						
VVBUS_UVLO	VBUS UVLO threshold	rising	3.6		3.9	V
		falling	3.5		3.8	
		hysteresis	0.1			
VVIN3V3_UVLO	Voltage required on VIN_3V3 for power on	rising, VVBUS = 0	2.56	2.66	2.76	V
		falling, VVBUS = 0	2.44	2.54	2.64	
		hysteresis	0.12			
LDO_3V3, LDO_1V5						
VLDO_3V3	Voltage on LDO_3V3	VVIN_3V3 = 0V, 10μA ≤ ILOAD ≤ 18mA, VVBUS ≥ 3.9V	3.0	3.4	3.6	V
RLDO_3V3	Rdson of VIN_3V3 to LDO_3V3	ILDO_3V3 = 50mA	1.4			Ω
VLDO_1V5	Voltage on LDO_1V5	up to maximum internal loading condition	1.49	1.5	1.65	V

6.7 Power Consumption

Operating under these conditions unless otherwise noted: $3V \leq V_{LDO_3V3} \leq 3.6V$, no GPIO loading

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VIN_3V3,ActSnk}$	Current into VIN_3V3	Active PPHV mode: $22V \geq V_{VBUS} \geq 4V$, $V_{VIN_3V3} = 3.3V$		3	6	mA
$I_{VIN_3V3,IdISnk}$	Current into VIN_3V3	Idle PPHV mode: $22V \geq V_{VBUS} \geq 4V$, $V_{VIN_3V3} = 3.3V$		1.0		mA
$I_{VIN_3V3,Sleep}$	Current into VIN_3V3	Sleep mode: $V_{VBUS} = 0V$, $V_{VIN_3V3} = 3.3V$		56		μA

6.8 PPHV Power Switch Characteristics - TPS25730AD

Operating under these conditions unless otherwise noted: $3.0V \leq V_{LDO_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PPHV}	Resistance from VBUS_IN to PPHV power switch resistance	$T_J \text{ PPHV} = 25^\circ C$, $I_{PPHV} = 6.5A$		16	19	m Ω
		$T_J \text{ PPHV} = 125^\circ C$, $I_{PPHV} = 6.5A$		24	29	
		$T_J \text{ PPHV} = 150^\circ C$, $I_{PPHV} = 6.5A$		27	32	m Ω
V_{RCP}	Comparator mode RCP threshold, $V_{PPHV} - V_{VBUS}$	$4V \leq V_{VBUS} \leq 22V$, $V_{VIN_3V3} \leq 3.63V$	2	6	10	mV
SS	Soft start slew rate for GATE_VSYS	$4V \leq V_{VBUS} \leq 22V$, $I_{LOAD} = 100mA$, $500pF < C_{GATE_VSYS} < 16nF$, measure slope from 10% to 90% of final VSYS value	2.8	3.3	3..80	V/ms
t_{PPHV_OFF}	Time allowed to disable the internal PPHV switch in normal shutdown mode	$V_{VBUS} = 20V$, $V_{PPHV} = 20V$ (initially), $C_{PPHV} < 1nF$, $I_{PPHV} = 0.1A$, switch is off when $V_{VBUS_IN} - V_{PPHV} > 1V$	400		1000	μs
t_{PPHV_OVP}	Time allowed to disable the internal PPHV switch in fast shutdown mode ($V_{OVP4RCP}$ exceeded), this includes the response time of the comparator	OVP: $V_{OVP4RCP} =$ setting 57, $V_{VBUS} = 20V$ initially, then raised to 23V in 50ns, $V_{PPHV} = V_{VBUS_IN}$ (initially), $C_{PPHV} < 1nF$, $I_{PPHV} = 0.1A$, switch is off when $V_{VBUS_IN} - V_{PPHV} > 0.1V$	2		4	μs
t_{PPHV_RCP}	Time allowed to disable the internal PPHV switch in fast shutdown mode (V_{RCP} exceeded), this includes the response time of the comparator	RCP: $V_{RCP} =$ setting 0, $V_{VBUS} = 5V$, $V_{VSYS} = 5V$ initially, then raised to 6V with $dV/dt = 0.1V/\mu s$, $C_{VBUS} = 10\mu F$, measure time from $V_{VSYS} > V_{VBUS} + V_{RCP}$ to the time of peak voltage on VBUS	1		2	μs
t_{PPHV_FSD}	Time allowed to disable the internal PPHV switch in fast shutdown mode (OVP)	$V_{PPHV} = 20V$ (initially), $V_{VBUS} = 20V$ then raised to 23V in 50ns, $r_{OVP} = 1$, $C_{PPHV} < 1nF$, $I_{PPHV} = 0.1A$, switch is off when $V_{VBUS_IN} - V_{PPHV} > 0.5V$	0.25		20	μs
t_{PPHV_ON}	Time to enable the internal PPHV switch	$V_{VBUS_IN} = 5V$, $C_{PPHV} = 0$, $I_{PPHV} = 0$, measure time from register write to enable PPHV until $V_{VBUS_IN} - V_{PPHV} < 0.1V$, soft start setting 3	1500	1800	2100	μs

6.9 PP_EXT Characteristics - TPS25730AS

Operating under these conditions unless otherwise noted: , $3V \leq V_{LDO_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{GATE_ON}	Gate driver sourcing current	$0V \leq V_{GATE_V_{SYS}} - V_{V_{SYS}} \leq 6V$, $V_{V_{SYS}} \leq 22V$, $V_{V_{BUS}} > 4V$, measure $I_{GATE_V_{SYS}}$	8.5		11.5	μA
		$0V \leq V_{GATE_V_{BUS}} - V_{V_{BUS}} \leq 6V$, $4V \leq V_{V_{BUS}} \leq 22V$, measure $I_{GATE_V_{BUS}}$	8.5		11.5	μA
V_{GATE_ON}	Sourcing voltage (ON)	$0V \leq V_{V_{SYS}} \leq 22V$, $I_{GATE_V_{SYS}} < 4\mu A$, measure $V_{GATE_V_{SYS}} - V_{V_{SYS}}$, $V_{V_{BUS}} > 4V$	6		12	V
		$4V \leq V_{V_{BUS}} \leq 22V$, $I_{GATE_V_{BUS}} < 4\mu A$, measure $V_{GATE_V_{BUS}} - V_{V_{BUS}}$	6		12	V
V_{RCP}	Comparator mode RCP threshold, $V_{V_{SYS}} - V_{V_{BUS}}$	$4V \leq V_{V_{BUS}} \leq 22V$, $V_{VIN_3V3} \leq 3.63V$	2	6	10	mV
I_{GATE_OFF}	Sinking strength	Normal turnoff: $V_{V_{SYS}} = 5V$, $V_{GATE_V_{SYS}} = 6V$, measure $I_{GATE_V_{SYS}}$	13			μA
		Normal turnoff: $V_{V_{BUS}} = V_{V_{SYS}} = 5V$, $V_{GATE_V_{BUS}} = 6V$, measure $I_{GATE_V_{BUS}}$	13			μA
R_{GATE_FSD}	Sinking strength	Fast turnoff: $V_{V_{SYS}} = 5V$, $V_{GATE_V_{SYS}} = 6V$, assert PPHV1_FAST_DISABLE, measure $R_{GATE_V_{SYS}}$			85	Ω
		Fast turnoff: $V_{V_{BUS}} = V_{V_{SYS}} = 5V$, $V_{GATE_V_{BUS}} = 6V$, assert PPHV1_FAST_DISABLE, measure $R_{GATE_V_{BUS}}$			85	Ω
$R_{GATE_OFF_UVLO}$	Sinking strength in UVLO (safety)	$V_{VIN_3V3} = 0V$, $V_{V_{BUS}} = 3V$, $V_{GATE_V_{SYS}} = 0.1V$, measure resistance from GATE_VSYS to GND			1.5	M Ω
SS	Soft start slew rate for GATE_VSYS	$4V \leq V_{V_{BUS}} \leq 22V$, $I_{LOAD} = 100mA$, $500pF < C_{GATE_V_{SYS}} < 16nF$, measure slope from 10% to 90% of final VSYS value	2.8	3.3	3.80	V/ms
$t_{GATE_V_{BUS_OFF}}$	Time allowed to disable the external FET via GATE_VBUS in normal shutdown mode. ⁽¹⁾	$V_{V_{BUS}} = 20V$, Q_G of external FET = 40nC or $C_{GATE_V_{BUS}} < 3nF$, gate is off when $V_{GATE_V_{BUS}} - V_{V_{BUS}} < 1V$		450	4000	μs
$t_{GATE_V_{BUS_OVP}}$	Time allowed to disable the external FET via GATE_VBUS in fast shutdown mode ($V_{OVP4RCP}$ exceeded), this includes the response time of the comparator ⁽¹⁾	OVP: $V_{OVP4RCP} =$ setting 57, $V_{V_{BUS}} = 20V$ initially, then raised to 23V in 50ns, Q_G of external FET = 40nC or $C_{GATE_V_{BUS}} < 3nF$, gate is off when $V_{GATE_V_{BUS}} - V_{V_{BUS}} < 1V$		3	5	μs

6.9 PP_EXT Characteristics - TPS25730AS (continued)

Operating under these conditions unless otherwise noted: $3V \leq V_{LDO_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{GATE_VBUS_RCP}$	Time allowed to disable the external FET via GATE_VBUS in fast shutdown mode (V_{RCP} exceeded), this includes the response time of the comparator ⁽¹⁾	RCP: V_{RCP} = setting 0, V_{VBUS} = 5V, V_{VSYS} = 5V initially, then raised to 5.5V in 50ns, Q_G of external FET = 40 nC or $C_{GATE_VBUS} < 3nF$, gate is off when $V_{GATE_VBUS} - V_{VBUS} < 1V$		1	2	μs
$t_{GATE_VSYS_OFF}$	Time allowed to disable the external FET via GATE_VSYS in normal shutdown mode ⁽¹⁾	V_{VSYS} = 20V, Q_G of external FET = 40nC or $C_{GATE_VBUS} < 3nF$, gate is off when $V_{GATE_VSYS} - V_{VSYS} < 1V$		450	4000	μs
$t_{GATE_VSYS_FSD}$	Time allowed to disable the external FET via GATE_VSYS in fast shutdown mode (OVP) ⁽¹⁾	V_{VBUS} = 20V initially, then raised to 23V in 50ns, Q_G of external FET = 40 nC or $C_{GATE_VBUS} < 3nF$, gate is off when $V_{GATE_VSYS} - V_{VSYS} < 1V$, $r_{OVP} = 1$		0.25	20	μs
$t_{GATE_VBUS_ON}$	Time to enable GATE_VBUS ⁽¹⁾	Measure time from when $V_{GS} = 0V$ until $V_{GS} > 3V$, where $V_{GS} = V_{GATE_VBUS} - V_{VBUS}$		0.25	2	ms

(1) These values depend upon the characteristics of the external N-ch MOSFET. The typical values measured are when Px_GATE_VSYS and Px_GATE_VBUS are used to drive two CSD17571Q2 in common drain back-to-back configuration.

6.10 Power Path Supervisory

Operating under these conditions unless otherwise noted: $3V \leq V_{LDO_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OVP4RCP}$	VBUS overvoltage protection for RCP programmable range	OVP detected when $V_{VBUS} > V_{OVP4RCP}$	5.0		24	V
$V_{OVP4RCPH}$	Hysteresis		1.75	2	2.25	%
r_{OVP}	Ratio of OVP4RCP input used for OVP4VSYS comparator. $r_{OVP} \times V_{OVP4VSYS} = V_{OVP4RCP}$			1		V/V
$V_{OVP4VSYS}$	VBUS overvoltage protection range for VSYS protection	OVP detected when $r_{OVP} \times V_{VBUS} > V_{OVP4RCP}$	5		27.5	V
$V_{OVP4VSYS}$	Hysteresis	VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP} setting 0	2	2.3	2.6	%
I_{DSCH}	VBUS discharge current	$V_{VBUS} = 22V$, measure I_{VBUS}	4		15	mA

6.11 CC Cable Detection Parameters

Operating under these conditions unless otherwise noted: $3V \leq V_{LDO_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Type-C Sink (Rd pulldown)						
V_{SNK1}	Open/Default detection threshold when Rd applied to CCy	rising	0.2		0.24	V
	Open/Default detection threshold when Rd applied to CCy	falling	0.16		0.20	V
	Hysteresis			0.04		V
V_{SNK2}	Default/1.5A detection threshold	falling	0.62		0.68	V
	Default/1.5A detection threshold	rising	0.63	0.66	0.69	V
	Hysteresis			0.01		V

6.11 CC Cable Detection Parameters (continued)

Operating under these conditions unless otherwise noted: $3V \leq V_{LDO_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{SNK3}	1.5A/3.0A detection threshold when Rd applied to CCy	falling	1.17		1.25	V
	1.5A/3.0A detection threshold when Rd applied to CCy	rising	1.22		1.3	V
	Hysteresis			0.05		V
R _{SNK}	Rd pulldown resistance	0.25V ≤ V _{CCy} ≤ 2.1V, measure resistance on CCy	4.6		5.6	kΩ
R _{VCONN_DIS}	VCONN discharge resistance	0V ≤ V _{CCy} ≤ 5.5V, measure resistance on CCy	4.0		6.12	kΩ
V _{CLAMP}	Dead battery Rd clamp	V _{VIN_3V3} = 0V, 64μA < I _{CCy} < 96μA	0.25		1.32	V
		V _{VIN_3V3} = 0V, 166μA < I _{CCy} < 194μA	0.65		1.32	
		V _{VIN_3V3} = 0V, 304μA < I _{CCy} < 356μA	1.20		2.18	
R _{Open}	Resistance from CCy to GND when configured as open	V _{VBUS} = 0V, V _{VIN_3V3} = 3.3V, V _{CCy} = 5V, measure resistance on CCy	500			kΩ
		V _{VBUS} = 5V, V _{VIN_3V3} = 0V, V _{CCy} = 5V, measure resistance on CCy	500			kΩ
Common Comparator						
t _{CC}	deglitch time for comparators on Px_CCy			3.2		ms

6.12 CC PHY Parameters

Operating under these conditions unless otherwise noted: and ($3V \leq V_{VIN_3V3} \leq 3.6V$ or $V_{VBUS} \geq 3.9V$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmitter						
V _{TXHI}	Transmit high voltage on CCy	Standard External load	1.05	1.125	1.2	V
V _{TXLO}	Transmit low voltage on CCy	Standard External load	-75		75	mV
Z _{DRIVER}	Transmit output impedance while driving the CC line using CCy	measured at 750kHz	33	54	75	Ω
t _{Rise}	Rise time. 10% to 90% amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	$C_{CCy} = 520pF$	300			ns
t _{Fall}	Fall time. 90% to 10% amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	$C_{CCy} = 520pF$	300			ns
V _{PHY_OVP}	OVP detection threshold for USB PD PHY	$0V \leq V_{VIN_3V3} \leq 3.6V, 0V \leq V_{PP5V} \leq 5.5V, V_{VBUS} \geq 4V$. Initially $V_{CC1} \leq 5.5V$ and $V_{CC2} \leq 5.5V$, then V_{CCx} rises	5.5		8.5	V
Receiver						
Z _{BMC RX}	Receiver input impedance on CCy	Does not include pullup or pulldown resistance from cable detect. Transmitter is Hi-Z	1			MΩ
C _{CC}	Receiver capacitance on CCy ¹	Capacitance looking into the CC pin when in receiver mode			120	pF
V _{RX_SNK_R}	Rising threshold on CCy for receiver comparator	Sink mode (rising)	499	525	551	mV

6.12 CC PHY Parameters (continued)

Operating under these conditions unless otherwise noted: and ($3V \leq V_{IN_3V3} \leq 3.6V$ or $V_{VBUS} \geq 3.9V$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{RX_SNK_F}$	Falling threshold on CCy for receiver comparator	Sink mode (falling)	230	250	270	mV

- (1) C_{CC} includes only the internal capacitance on a CCy pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications (cReceiver). Therefore, TI recommends adding C_{CCy} externally.

6.13 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_MAIN}	Temperature shutdown threshold	Temperature rising	145	160	175	°C
		Hysteresis		15		°C

6.14 ADC Characteristics

Operating under these conditions unless otherwise noted: $3V \leq V_{LDO_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LSB	Least significant bit	3.6V max scaling, voltage divider of 3		14		mV
		25.2V max scaling, voltage divider of 21		98		mV
		4.07A max scaling		16.5		mA
GAIN_ERR	Gain error	$0.05V \leq V_{ADCINx} \leq 3.6V$, $V_{ADCINx} \leq V_{LDO_3V3}$	-2.7		2.7	%
		$0.05V \leq V_{GPIOx} \leq 3.6V$, $V_{GPIOx} \leq V_{LDO_3V3}$				
		$2.7V \leq V_{LDO_3V3} \leq 3.6V$	-2.4		2.4	
		$0.6V \leq V_{VBUS} \leq 22V$	-2.1		2.1	
		$1A \leq I_{VBUS} \leq 3A$	-2.1		2.1	
VOS_ERR	Offset error ¹	$0.05V \leq V_{ADCINx} \leq 3.6V$, $V_{ADCINx} \leq V_{LDO_3V3}$	-4.1		4.1	mV
		$0.05V \leq V_{GPIOx} \leq 3.6V$, $V_{GPIOx} \leq V_{LDO_3V3}$				
		$2.7V \leq V_{LDO_3V3} \leq 3.6V$	-4.5		4.5	
		$0.6V \leq V_{VBUS} \leq 22V$	-4.1		4.1	
		$1A \leq I_{VBUS} \leq 3A$	-4.5		4.5	mA

- (1) The offset error is specified after the voltage divider.

6.15 Input/Output (I/O) Characteristics

Operating under these conditions unless otherwise noted: $3V \leq V_{LDO_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO0-7 (Inputs)						
GPIO_VIH	GPIOx high-level input voltage	$V_{LDO_3V3} = 3.3V$	1.3			V
GPIO_VIL	GPIOx low-level input voltage	$V_{LDO_3V3} = 3.3V$			0.54	V
GPIO_HYS	GPIOx input hysteresis voltage	$V_{LDO_3V3} = 3.3V$	0.09			V
GPIO_ILKG	GPIOx leakage current	$V_{GPIOx} = 3.45V$	-1		1	μA
GPIO_RPU	GPIOx internal pullup	Pullup enabled	50	100	150	kΩ

6.15 Input/Output (I/O) Characteristics (continued)

Operating under these conditions unless otherwise noted: $3V \leq V_{LDO_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO_RPD	GPIOx internal pulldown	Pulldown enabled	50	100	150	kΩ
GPIO_DG	GPIOx input deglitch			20	50	ns
GPIO0-9 (Outputs)						
GPIO_VOH	GPIOx output high voltage	$V_{LDO_3V3} = 3.3V$, $I_{GPIOx} = -2mA$	2.9			V
GPIO_VOL	GPIOx output low voltage	$V_{LDO_3V3} = 3.3V$, $I_{GPIOx} = 2mA$			0.4	V
ADCINx						
ADCIN_ILKG	ADCINx leakage current	$V_{ADCINx} \leq V_{LDO_3V3}$	-1		1	μA
t _{BOOT}	Time from LDO_3V3 going high until ADCINx is read for configuration			10		ms

6.16 I2C Requirements and Characteristics

Operating under these conditions unless otherwise noted: $3V \leq V_{LDO_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I2Ct_IRQ						
OD_VOL_IRQ	Low level output voltage	$I_{OL} = 2mA$			0.4	V
OD_LKG_IRQ	Leakage Current	Output is Hi-Z, $V_{I2Cx_IRQ} = 3.45V$	-1		1	μA
SDA and SCL Common Characteristics (Common Characteristics)						
V _{IL}	Input low signal	$V_{LDO_3V3} = 3.3V$			0.54	V
V _{IH}	Input high signal	$V_{LDO_3V3} = 3.3V$	1.3			V
V _{HYS}	Input hysteresis	$V_{LDO_3V3} = 3.3V$	0.165			V
V _{OL}	Output low voltage	$I_{OL} = 3mA$			0.36	V
I _{LEAK}	Input leakage current	Voltage on pin = V_{LDO_3V3}	-3		3	μA
I _{OL}	Max output low current	$V_{OL} = 0.4V$	15			mA
I _{OL}	Max output low current	$V_{OL} = 0.6V$	20			mA
t _f	Fall time from $0.7 \times V_{DD}$ to $0.3 \times V_{DD}$	$V_{DD} = 1.8V$, $10pF \leq C_b \leq 400pF$	12		80	ns
		$V_{DD} = 3.3V$, $10pF \leq C_b \leq 400pF$	12		150	ns
t _{SP}	I ² C pulse width suppressed				50	ns
C _I	Pin capacitance (internal)				10	pF
C _b	Capacitive load for each bus line (external)				400	pF
SDA and SCL Standard Mode Characteristics (Target)						
f _{SCLS}	Clock frequency for target	$V_{DD} = 1.8V$ or $3.3V$			100	kHz
t _{VD;DAT}	Valid data time	Transmitting Data, $V_{DD} = 1.8V$ or $3.3V$, SCL low to SDA output valid			3.45	μs
t _{VD;ACK}	Valid data time of ACK condition	Transmitting Data, $V_{DD} = 1.8V$ or $3.3V$, ACK signal from SCL low to SDA (out) low			3.45	μs
SDA and SCL Fast Mode Characteristics (Target)						
f _{SCLS}	Clock frequency for target	$V_{DD} = 1.8V$ or $3.3V$	100		400	kHz
t _{VD;DAT}	Valid data time	Transmitting data, $V_{DD} = 1.8V$, SCL low to SDA output valid			0.9	μs

6.16 I2C Requirements and Characteristics (continued)

Operating under these conditions unless otherwise noted: $3V \leq V_{LDO_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{VD,ACK}$	Valid data time of ACK condition	Transmitting data, $V_{DD} = 1.8V$ or $3.3V$, ACK signal from SCL low to SDA (out) low			0.9	μs

6.17 Typical Characteristics

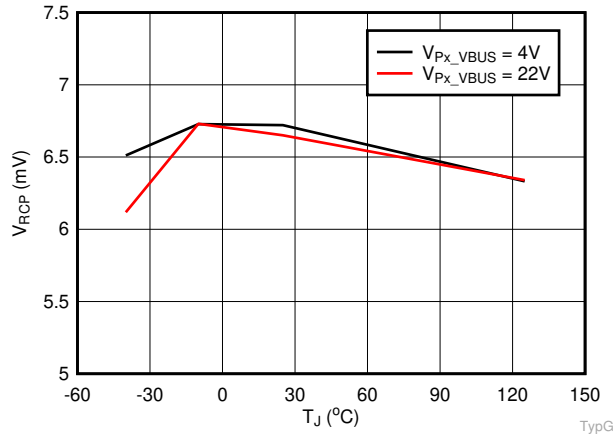


Figure 6-1. V_{RCP} vs Temperature

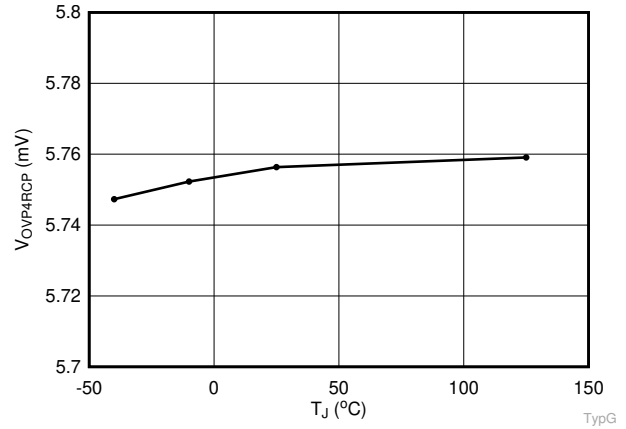


Figure 6-2. V_{OVP4RCP} (Setting 2) vs Temperature

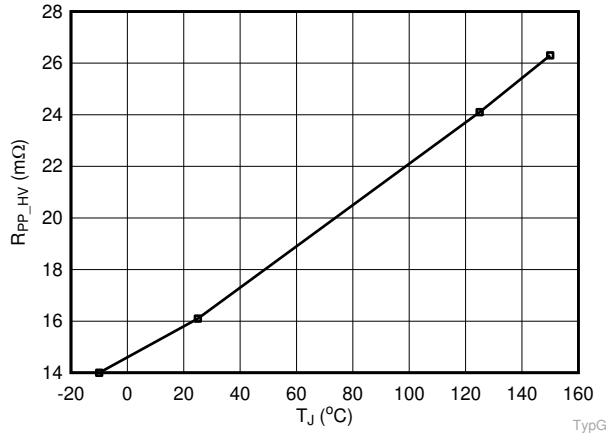


Figure 6-3. R_{PPHV} vs. Temperature for TPS25730AD

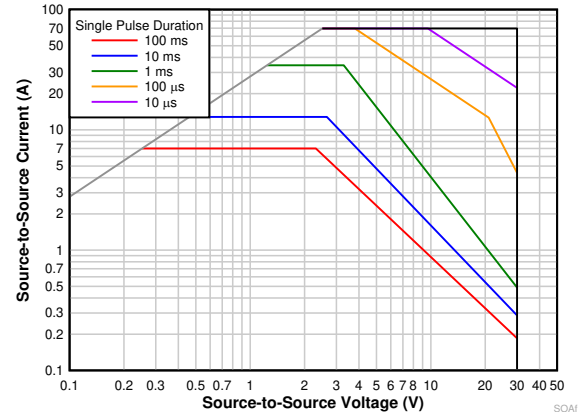


Figure 6-4. Safe-Operating-Area (SOA) of PPHV for TPS25730AD

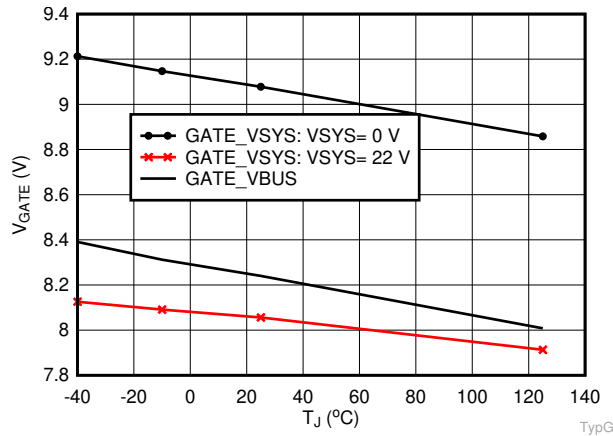


Figure 6-5. V_{GATE_VBUS_ON} vs Temperature for TPS25730AS

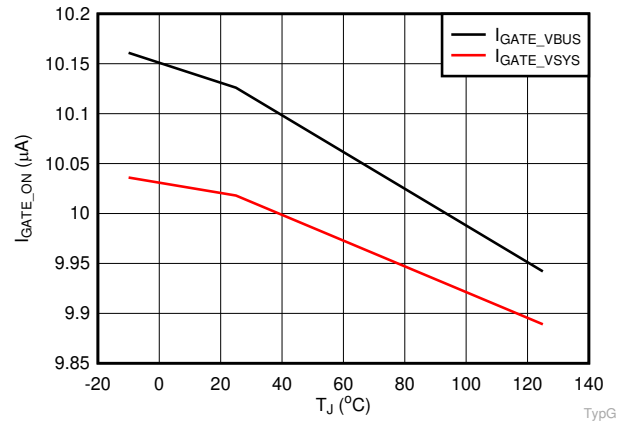


Figure 6-6. I_{GATE_ON} vs Temperature for TPS25730AS

7 Parameter Measurement Information

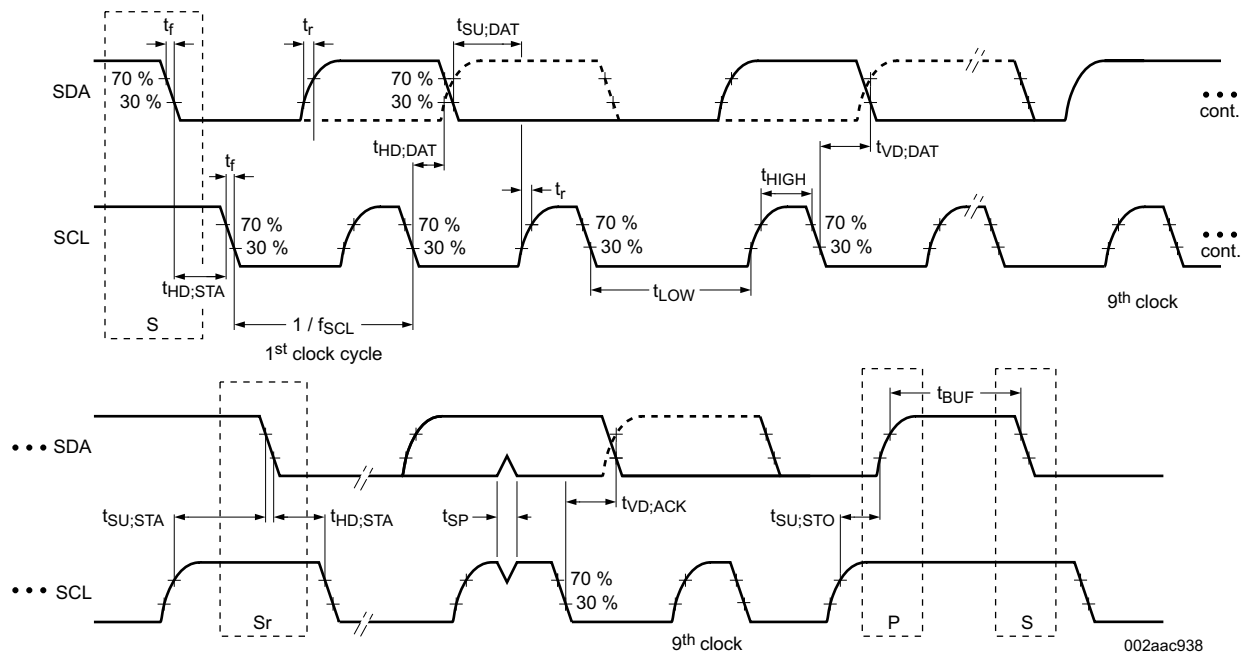


Figure 7-1. I²C Target Interface Timing

8 Detailed Description

8.1 Overview

The TPS25730A is a fully-integrated USB Power Delivery (USB-PD) management device providing cable plug and orientation detection for USB Type-C and PD receptacles. The TPS25730A communicates with the other USB Type-C and PD port partner at the opposite end of the cable. The device also integrates a high current port power switch for sinking.

The TPS25730A is divided into several main sections:

- USB-PD controller
- Cable plug and orientation detection circuitry
- Port power switch
- Power management circuitry
- Digital core

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the CC1 pin or the CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of features, and more detailed circuitry, see [Section 8.3.1](#).

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of features, and more detailed circuitry, see [Section 8.3.4](#).

For a high-level block diagram of the port power switch, a description of features, and more detailed circuitry, see [Section 8.3.3](#).

The power management circuitry receives and provides power to the TPS25730A internal circuitry and LDO_3V3 output. See [Section 8.3.2](#) for more information.

The digital core provides the engine for receiving, processing, and sending all USB-PD packets as well as handling control of all other TPS25730A functionality. For a high-level block diagram of the digital core, a description of features, and more detailed circuitry, see [Section 8.3.9](#).

The TPS25730A also integrates a thermal shutdown mechanism and runs off of accurate clocks provided by the integrated oscillator.

8.2 Functional Block Diagram

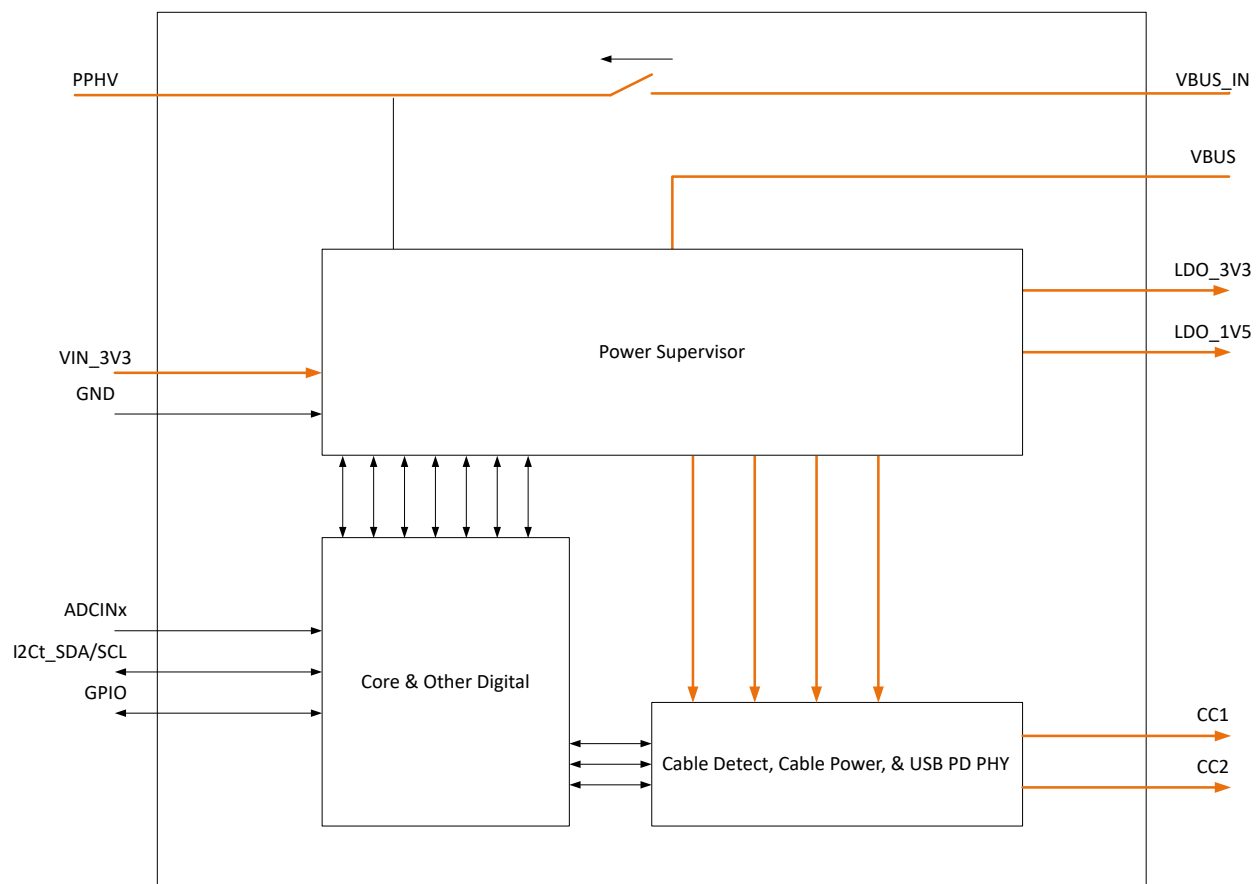


Figure 8-1. TPS25730AD

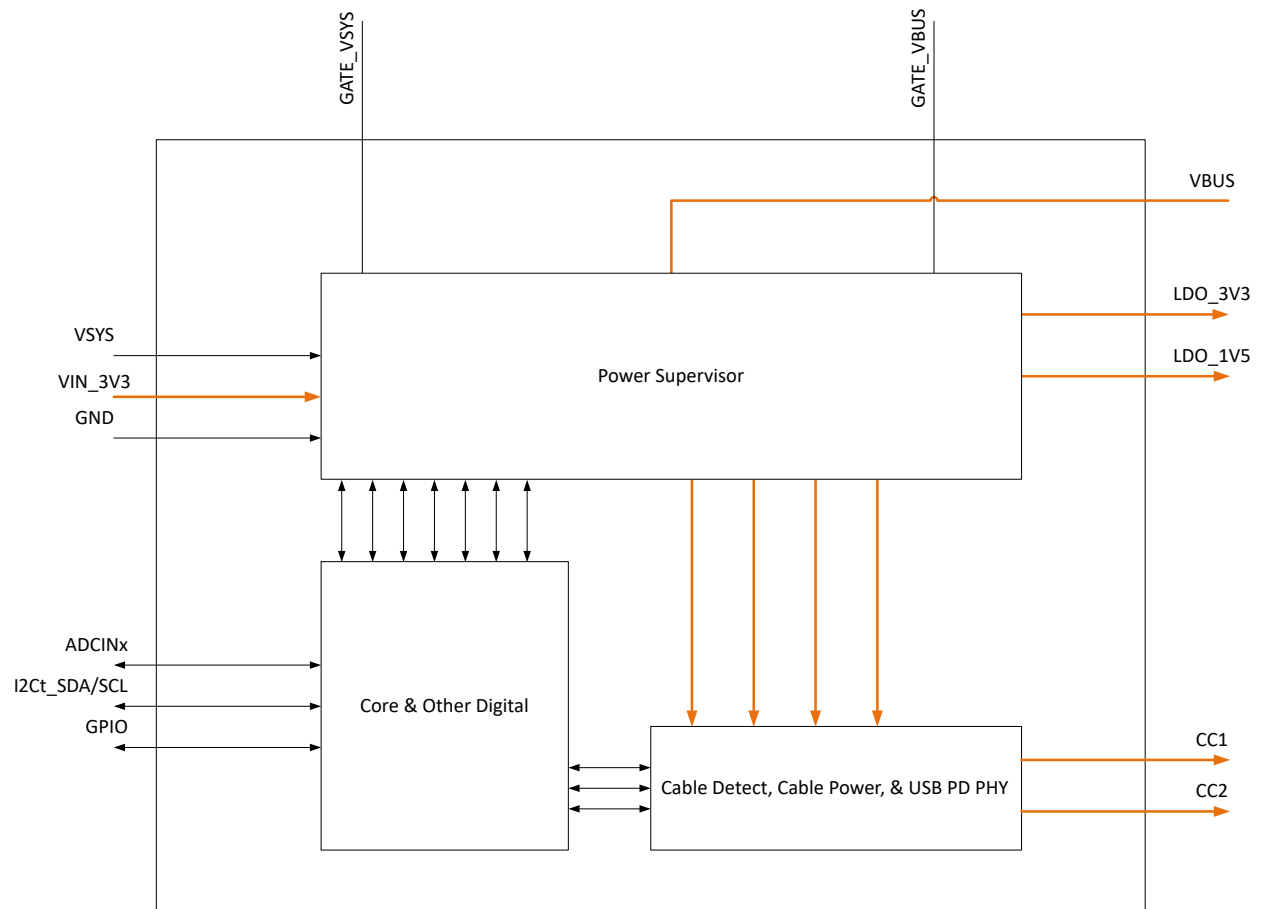


Figure 8-2. TPS25730AS

8.3 Feature Description

8.3.1 USB-PD Physical Layer

Figure 8-3 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block.

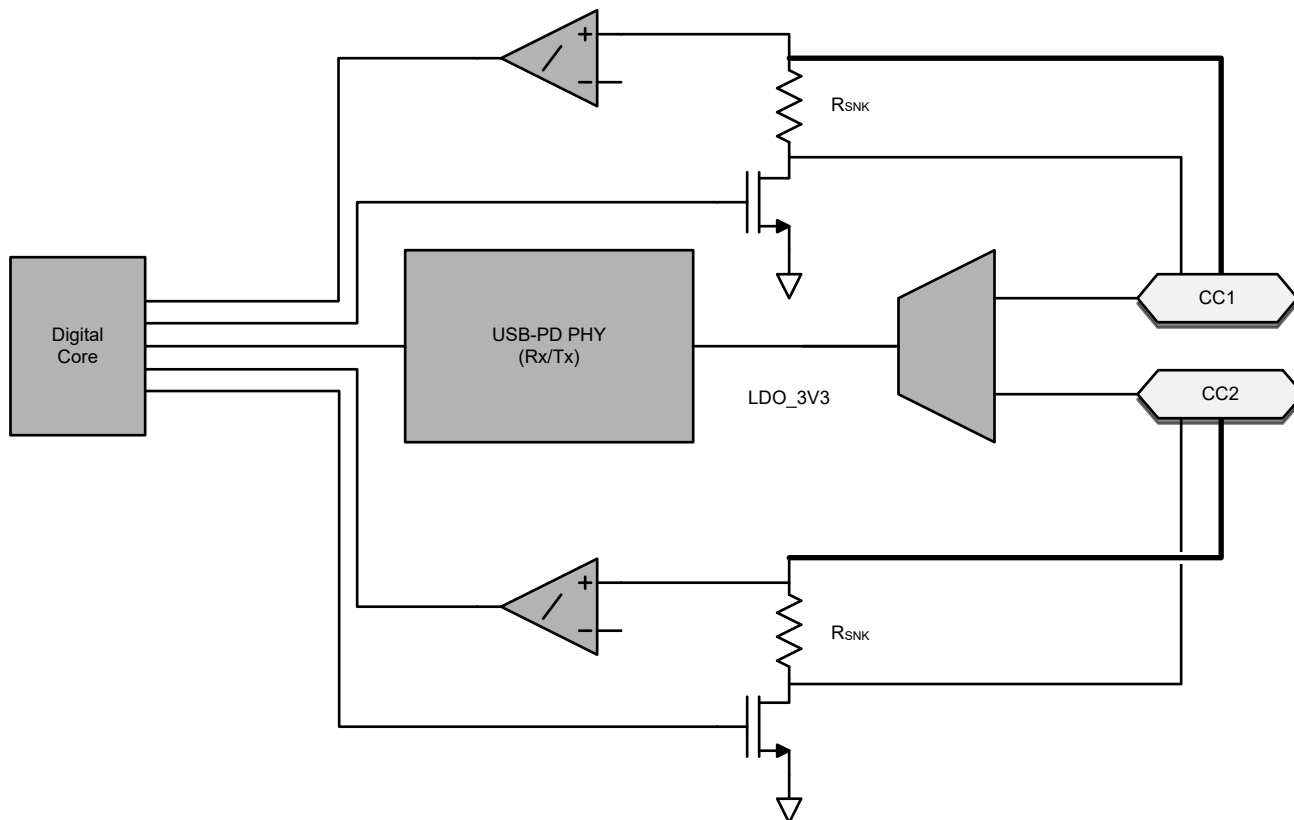


Figure 8-3. USB-PD Physical Layer and Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (CC1 or CC2) that is DC biased due to the R_p (or R_d) cable attach mechanism.

8.3.1.1 USB-PD Encoding and Signaling

Figure 8-4 illustrates the high-level block diagram of the baseband USB-PD transmitter. Figure 8-5 illustrates the high-level block diagram of the baseband USB-PD receiver.

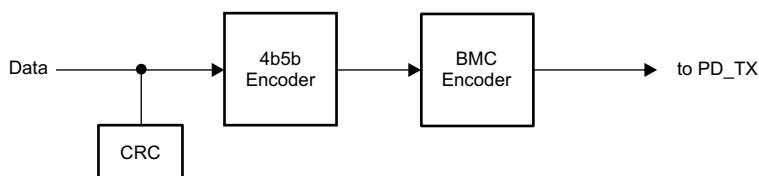


Figure 8-4. USB-PD Baseband Transmitter Block Diagram

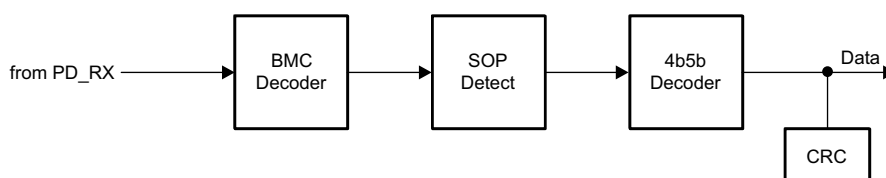


Figure 8-5. USB-PD Baseband Receiver Block Diagram

8.3.1.2 USB-PD Bi-Phase Marked Coding

The USB-PD physical layer implemented in the TPS25730A is compliant to the [USB-PD Specifications](#). The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphasic Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). [Biphase Mark Coding Example](#) illustrates Biphasic Mark Coding.

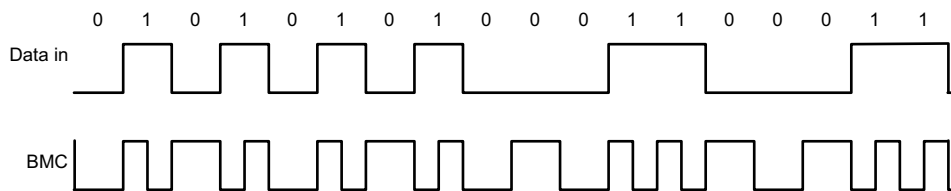


Figure 8-6. Biphasic Mark Coding Example

The USB PD baseband signal is driven onto the CC1 or CC2 pin with a tri-state driver. The tri-state driver is slew rate limited to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to make sure the receiver clocks the final bit of EOP.

8.3.1.3 USB-PD BMC Transmitter

The TPS25730A transmits and receives USB-PD data over one of the CCy pins for a given CC pin pair (one pair per USB Type-C port). The CCy pins are also used to determine the cable orientation and maintain the cable/device attach detection. Thus, a DC bias exists on the CCy pins. The transmitter driver overdrives the CCy DC bias while transmitting, but returns to a Hi-Z state, allowing the DC voltage to return to the CCy pin when not transmitting. While either CC1 or CC2 can be used for transmitting and receiving, during a given connection only, the one that mates with the CC pin of the plug is used, so there is no dynamic switching between CC1 and CC2. [USB-PD BMC TX/RX Block Diagram](#) shows the USB-PD BMC TX and RX driver block diagram.

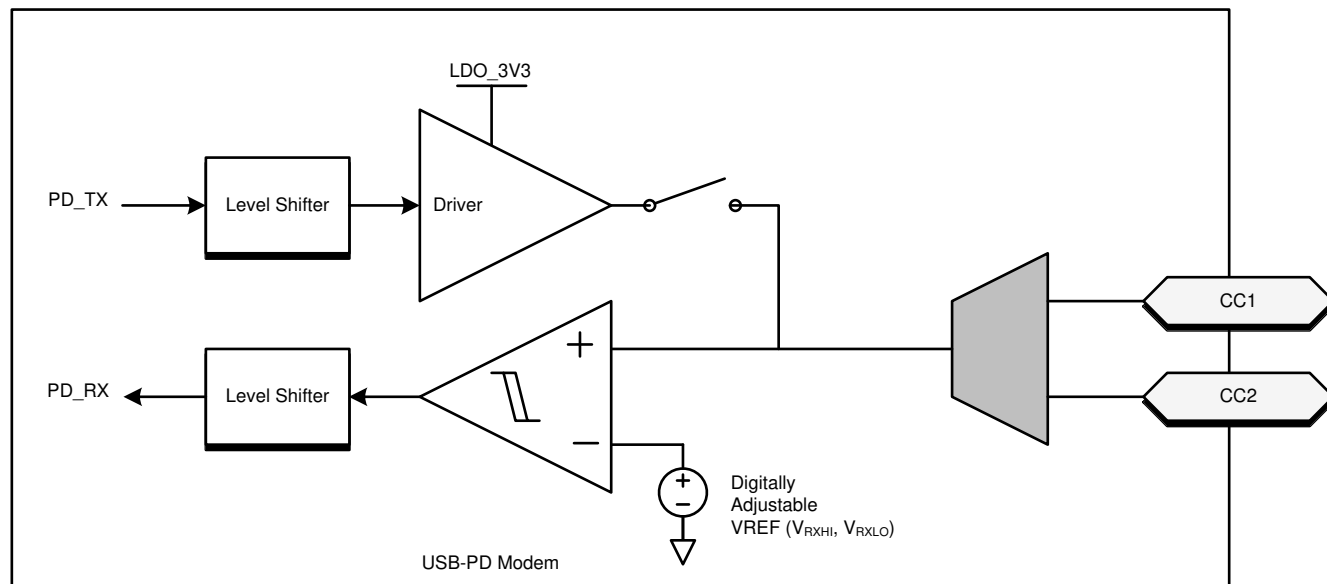


Figure 8-7. USB-PD BMC TX/RX Block Diagram

[Figure 8-8](#) shows the transmission of the BMC data on top of the DC bias. Note that the DC bias can be anywhere between the minimum and maximum threshold for detecting a Sink attach. This note means that the DC bias can be above or below the V_{OH} of the transmitter driver.

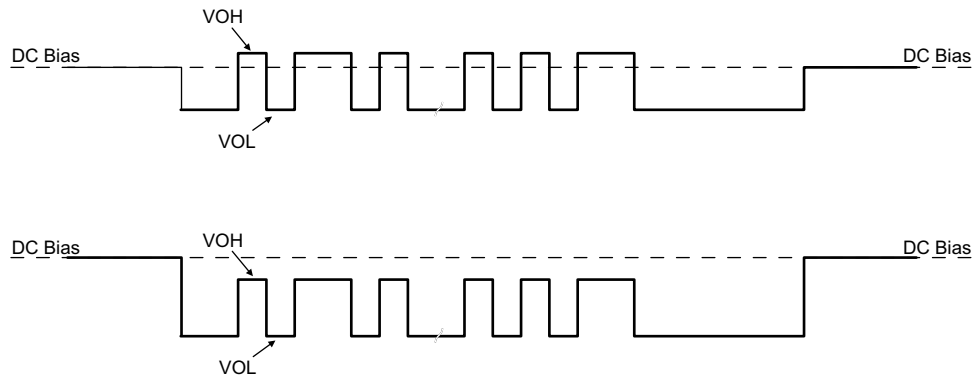


Figure 8-8. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the CCy lines. The signal peak, V_{TXHI} , is set to meet the TX masks defined in the [USB-PD Specifications](#). Note that the TX mask is measured at the far-end of the cable.

When driving the line, the transmitter driver has an output impedance of Z_{DRIVER} . Z_{DRIVER} is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. Z_{DRIVER} impacts the noise ingress in the cable.

[ZDRIVER Circuit](#) shows the simplified circuit determining Z_{DRIVER} . The circuit is specified such that noise at the receiver is bounded.

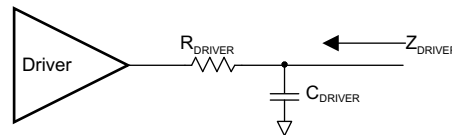


Figure 8-9. ZDRIVER Circuit

8.3.1.4 USB-PD BMC Receiver

The receiver block of the TPS25730A receives a signal that follows the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask.

[Example USB-PD Multi-Drop Configuration](#) shows an example of a multi-drop USB-PD connection (only the CC wire). This connection has the typical Sink (device) to Source (host) connection, but also includes cable USB-PD Tx/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (Z_{BMCRX}). The [USB-PD Specification](#) also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

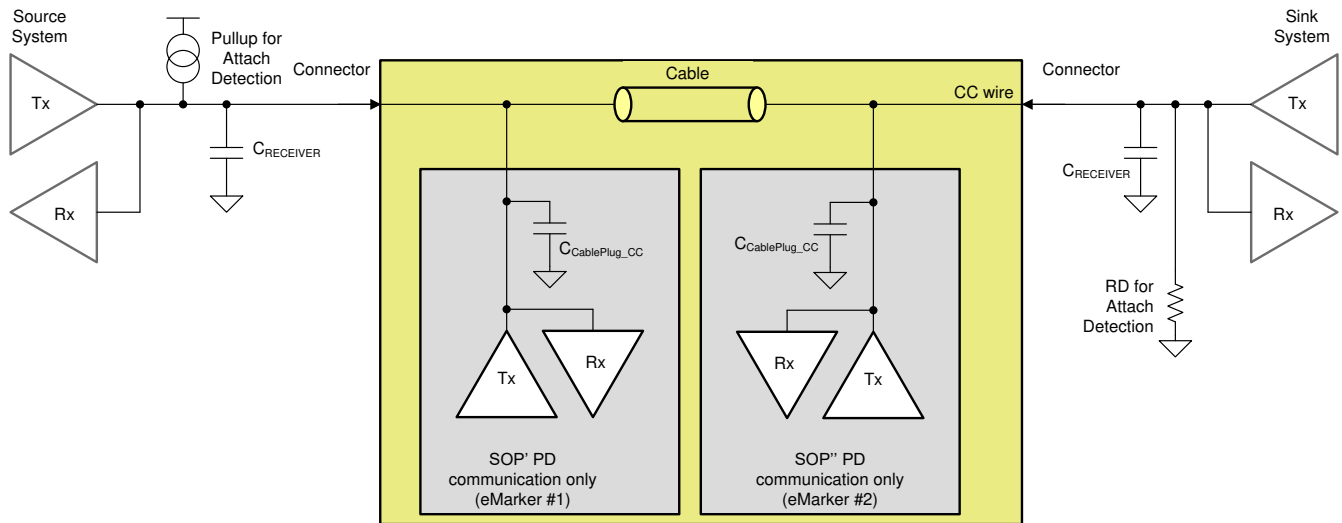


Figure 8-10. Example USB-PD Multi-Drop Configuration

8.3.1.5 Squelch Receiver

The TPS25730A has a squelch receiver to monitor for the bus idle condition as defined by the USB PD specification.

8.3.2 Power Management

The TPS25730A power management block receives power and generates voltages to provide power to the TPS25730A internal circuitry. These generated power rails are LDO_3V3 and LDO_1V5. LDO_3V3 can also be used as a low power output for external EEPROM memory. The power supply path is shown in [Figure 8-11](#).

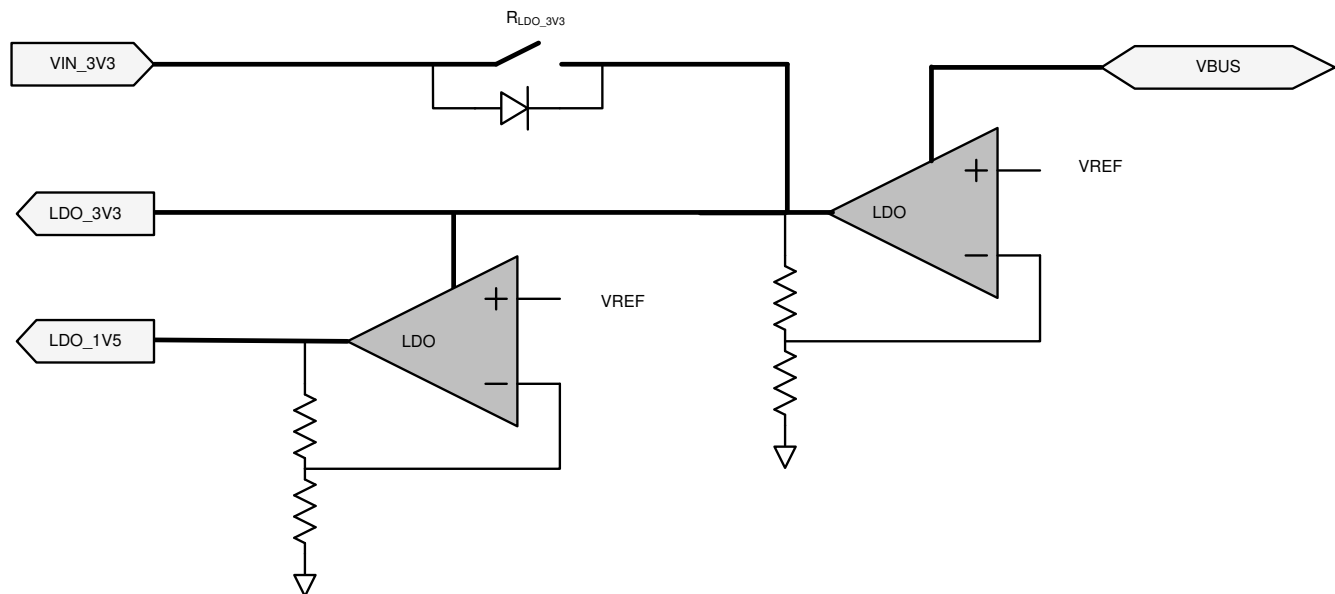


Figure 8-11. Power Supplies

The TPS25730A is powered from either VIN_3V3 or VBUS. The normal power supply input is VIN_3V3. When powering from VIN_3V3, current flows from VIN_3V3 to LDO_3V3 to power the core 3.3V circuitry and I/Os. A second LDO steps the voltage down from LDO_3V3 to LDO_1V5 to power the 1.5V core digital circuitry. When VIN_3V3 power is unavailable and power is available on VBUS, the device is considered to be in the dead-battery start-up condition. In a dead-battery start-up condition, the TPS25730A opens the VIN_3V3 switch

until the host clears the dead-battery flag through I²C. Therefore, the TPS25730A is powered from the VBUS input with the higher voltage during the dead-battery start-up condition and until the dead-battery flag is cleared. When powering from a VBUS input, the voltage on VBUS is stepped down through an LDO to LDO_3V3.

8.3.2.1 Power-On And Supervisory Functions

A power-on reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present.

8.3.2.2 VBUS LDO

The TPS25730A contains an internal high-voltage LDO which is capable of converting VBUS to 3.3V for powering internal device circuitry. The VBUS LDO is used when in the dead-battery condition. (VIN_3V3 is low and the dead-battery flag is active). The VBUS LDO is powered from VBUS.

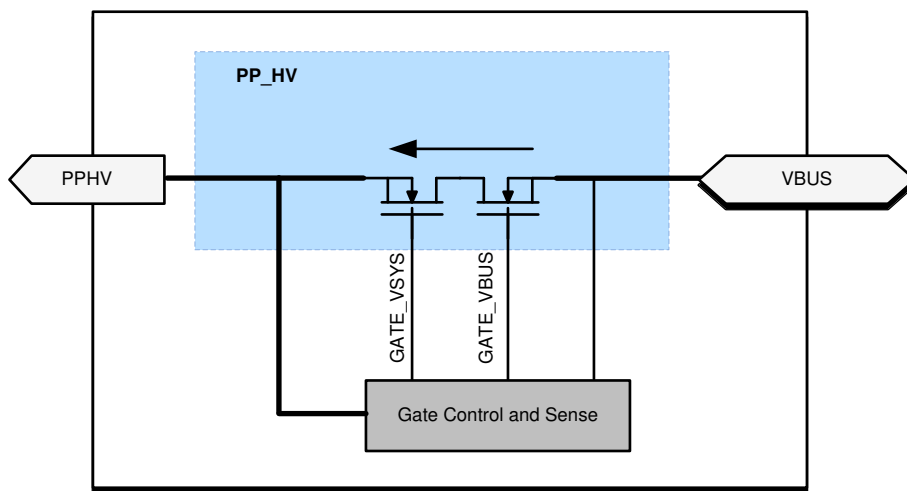
8.3.3 Power Paths

TPS25730AD has an integrated high voltage load switch for sinking power path: PPHV. TPS25730AS has a high voltage gate driver for sink path control: PP_EXT. Each power path is described in detail in this section.

8.3.3.1 TPS25730AD Internal Powerpath

The TPS25730AD has internal controls for internal FETs (GATE_VSYS and GATE_VBUS as shown in [Internal Powerpath](#)) that require that VBUS_IN be above V_{VBUS_UVLO} before being able to enable the powerpath. [Internal Powerpath](#) shows a diagram of the powerpath. When a powerpath is enabled, the circuitry includes a slew rate control loop to make sure that external switches do not turn on too quickly (SS). The TPS25730AD senses the PPHV and VBUS voltages to control the gate voltages to enable or disable the FETs.

The powerpath control includes overvoltage protection (OVP) and reverse current protection (RCP).



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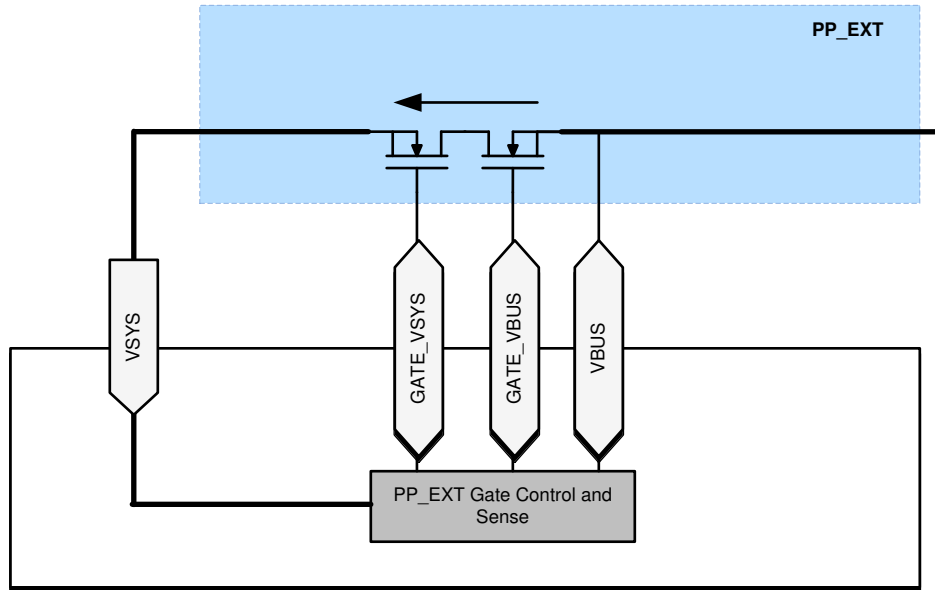
Figure 8-12. Internal Powerpath

8.3.3.2 External Powerpath Control PP_EXT

The TPS25730A TPS25730AS has two N-ch gate drivers designed to control a sinking path from VBUS to VSYS and. The charge pump for these gate drivers requires VBUS to be above V_{VBUS_UVLO} . When a sink path is enabled, the circuitry includes a slew rate control loop to make sure that external switches do not turn on too quickly (SS). The TPS25730A TPS25730AS senses the VSYS and VBUS voltages to control the gate voltages to enable or disable the external FETs.

The high voltage power path control includes overvoltage protection (OVP), and reverse current protection (RCP). Adding resistance in series with a GATE pin of the TPS25730A TPS25730AS and the gate pin of the

N-ch MOSFET slows down the turnoff time when OVP or RCP occurs. Any such resistance must be minimized, and not allowed to exceed 3Ω .



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Figure 8-13. PP_EXT External Powerpath Control

Details of the [VSYS Gate Driver](#) shows the GATE_VSYS gate driver in more detail.

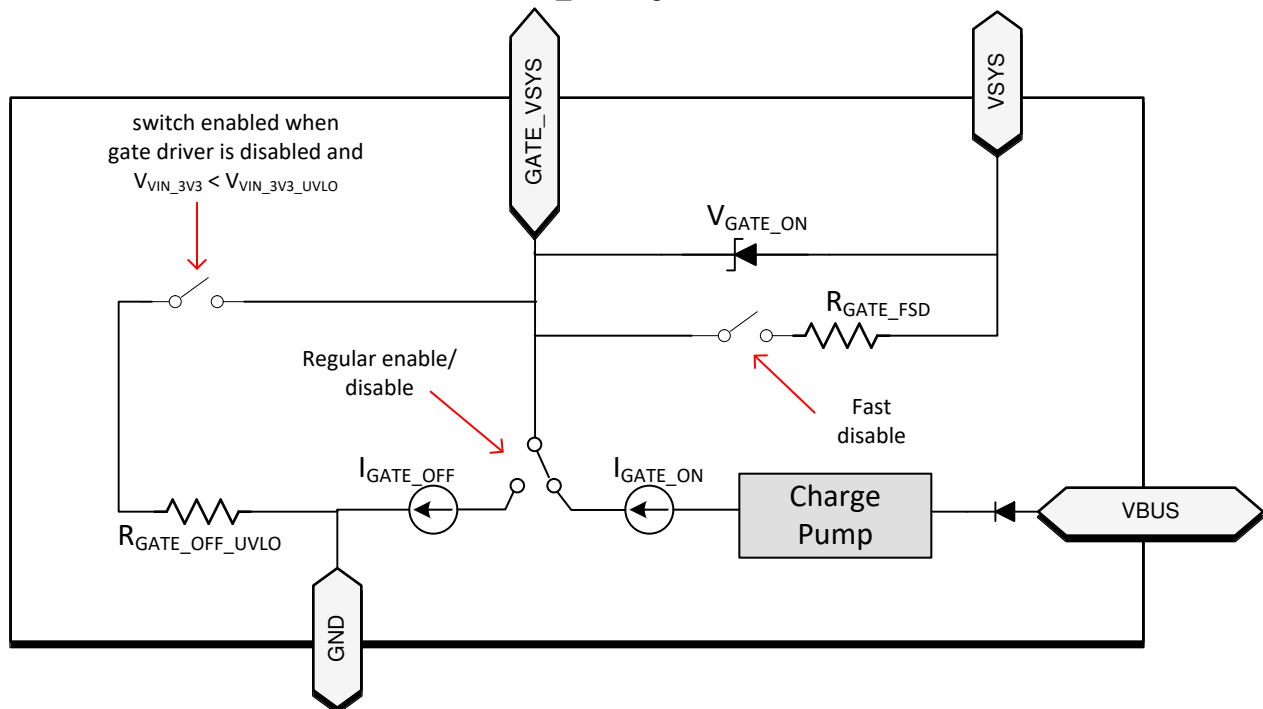


Figure 8-14. Details of the VSYS Gate Driver

8.3.4 Cable Plug and Orientation Detection

Figure 8-15 shows the plug and orientation detection block at each CCy pin (CC1, CC2). Each pin has identical detection circuitry.

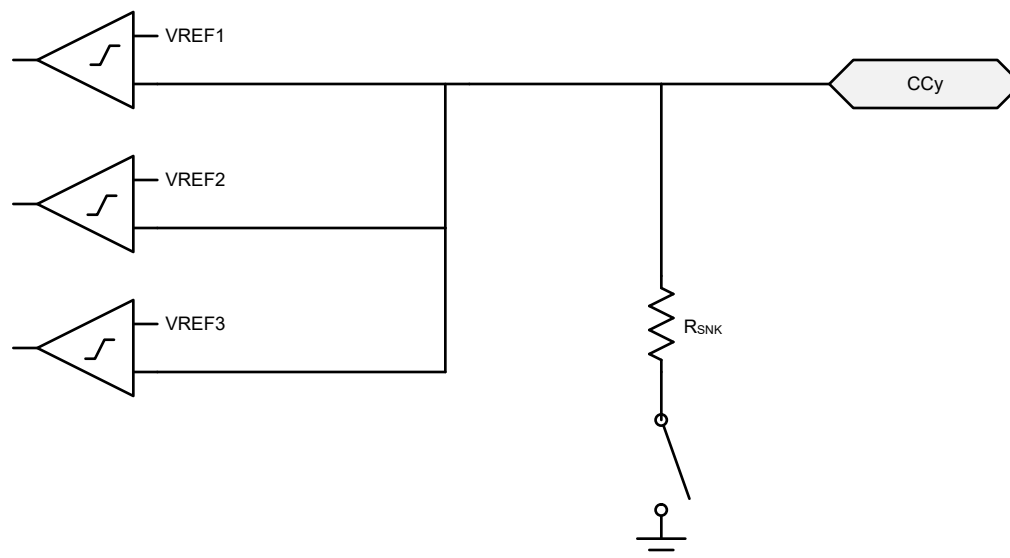


Figure 8-15. Plug and Orientation Detection Block

8.3.5 Overvoltage Protection (CC1, CC2)

The TPS25730A detects when the voltage on the CC1 or CC2 pin is too high and takes action to protect the system. The protective action is to disable the USB PD transmitter.

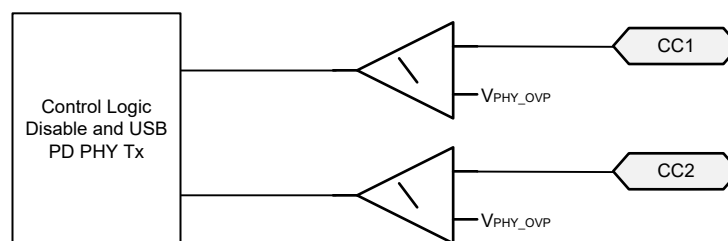


Figure 8-16. Overvoltage and Reverse Current Protection for CC1 and CC2

8.3.6 Default Behavior Configuration (ADCINx)

The ADCINx inputs to the internal ADC control the behavior of the TPS25730A. The ADCINx pins must be externally tied to the LDO_3V3 pin via a resistive divider as shown in the following figure. At power-up the ADC converts the ADCINx voltage and the digital core uses these four values, along with PD5VMAX, to determine start-up behavior. The available start-up configurations include options for I²C target address of I2Ct_SCL/SDA and default configuration.

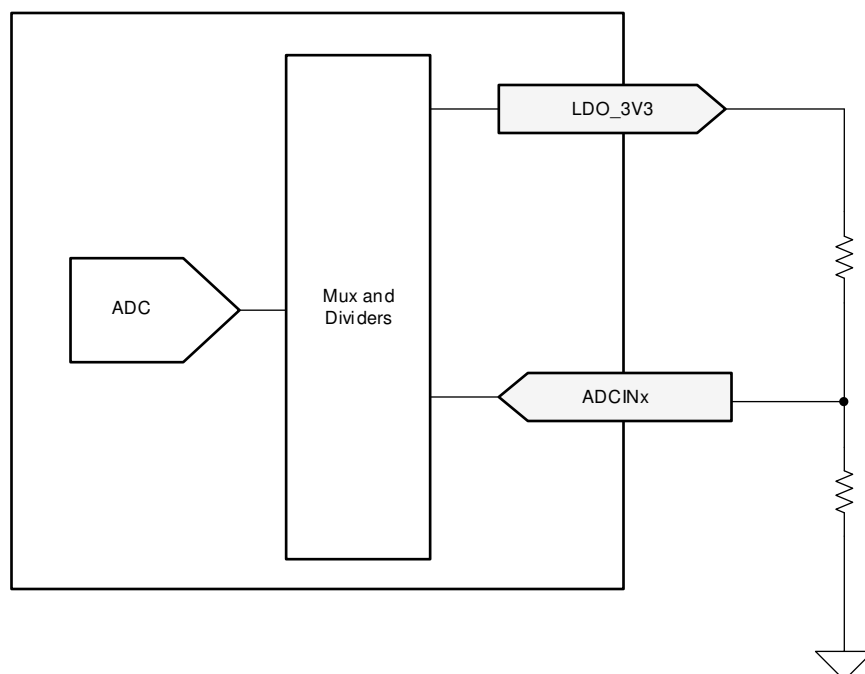


Figure 8-17. ADCINx Resistor Divider

The device behavior is determined in several ways depending upon the decoded value of the ADCINx pins. The following table shows the decoded values for different resistor divider ratios. See *I²C Address Setting* for details on how ADCINx decoded values affects default I²C target address.

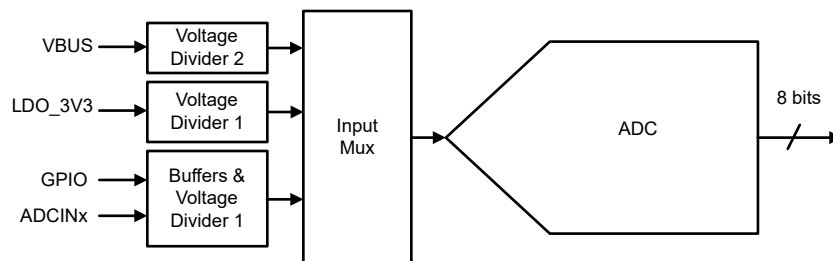
Table 8-1. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R _{DOWN} / (R _{UP} + R _{DOWN}) ⁽¹⁾			Without Using R _{UP} or R _{DOWN}	ADCINx Decoded Value
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

(1) See *I²C Address Setting* to see the exact meaning of I²C Address Index.

8.3.7 ADC

The TPS25730A ADC is shown in [Figure 8-18](#). The ADC is an 8-bit successive approximation ADC. The input to the ADC is an analog input mux that supports multiple inputs from various voltages and currents in the device.

**Figure 8-18. SAR ADC**

8.3.8 Digital Interfaces

The TPS25730A contains several different digital interfaces which can be used for communicating with other devices. The available interfaces include an I2C target and preconfigured GPIO.

8.3.8.1 GPIO

The supported GPIO functions are natively supported by the PD Controller and do not need any configuration.

Table 8-2. GPIO Functionality Table

PIN NAME	TYPE	SPECIAL FUNCTIONALITY
CAP_MIS	O	Blinking indicator when the connected source cannot supply enough power to the systems, the Capability Mismatch bit is set in the PD Request
SINK_EN	O	Active low signal used to control an external load switch to sink power into the system. SINK_EN when the PP_HV or PP_EXT path is not used in the system.
PLUG_EVENT	O	Indicates to the system that there is a connection on the Type-C port.
DBG_ACC	O	Indicates to the system that a debug accessory has been detected on the Type-C port.
PLUG_FLIP	O	Indicates to the system the cable orientation, where CC1 = 0 and CC2 = 1
FAULT_IN	I	Active low signal which indicates to the PD Controller that the system is in a fault condition. The PD Controller disconnects from the Type-C port and enters the Type-C Error Recovery state.

8.3.8.2 I²C Interface

The TPS25730A has one I2C target interface port: I2Ct. I2C port I2Ct is comprised of the I2Ct_SDA and I2Ct_SCL pins. This interface provides general status information about the TPS25730A, as well as the ability to control the TPS25730A behavior, supporting communications to/from a connected device and/or cable supporting BMC USB-PD, and providing information about connections detected at the USB-C receptacle.

When the TPS25730A is in 'APP' mode TI recommends to use standard mode or Fast mode (that is a clock speed no higher than 400kHz).

Table 8-3. I²C Summary

I ² C BUS	TYPE	TYPICAL USAGE
I2Ct	Target	Optionally can be connected to an external MCU.

8.3.8.2.1 I²C Interface Description

The TPS25730A supports Standard and Fast mode I²C interfaces. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pullup resistor. Data transfer can be initiated only when the bus is not busy.

A controller sending a Start condition, a high-to-low transition on the SDA input and output, while the SCL input is high initiates I²C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred

during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The controller sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met to maintain proper operation.

A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target. The controller receiver holding the SDA line high does signals the end of the data transfer. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.

[I2C Definition of Start and Stop Conditions](#) shows the start and stop conditions of the transfer. [I2C Bit Transfer](#) shows the SDA and SCL signals for transferring a bit. [Figure 8-21](#) shows a data transfer sequence with the ACK or NACK at the last clock pulse.

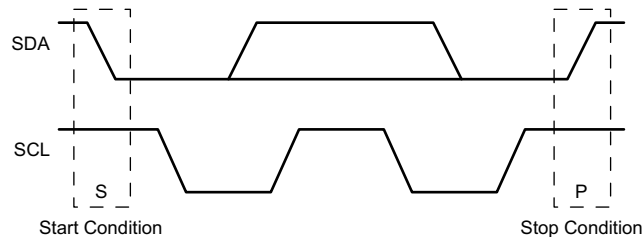


Figure 8-19. I²C Definition of Start and Stop Conditions

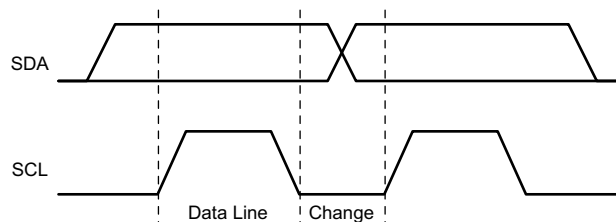


Figure 8-20. I²C Bit Transfer

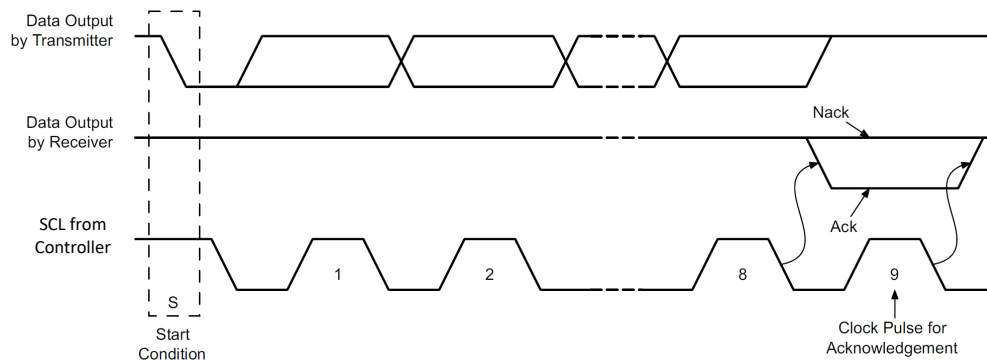


Figure 8-21. I²C Acknowledgment

8.3.8.2.1.1 I²C Clock Stretching

The TPS25730A features clock stretching for the I²C protocol. The TPS25730A target I²C port can hold the clock line (SCL) low after receiving (or sending) a byte, indicating that the bus is not yet ready to process more data. The controller communicating with the target must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the target is clock stretching, the clock line remains low.

The controller must wait until the clock line transitions high plus an additional minimum time (4μs for standard 100kbps I²C) before pulling the clock low again.

Any clock pulse can be stretched and typically the clock pulse before or after the acknowledgment bit is stretched.

8.3.8.2.1.2 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C controller and a single TPS25730A. The I²C target sub-address is used to receive or respond to Host Interface protocol commands. [Figure 8-22](#) and [Figure 8-23](#) show the write and read protocol for the I²C target interface, and a key is included in [Figure 8-24](#) to explain the terminology used. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

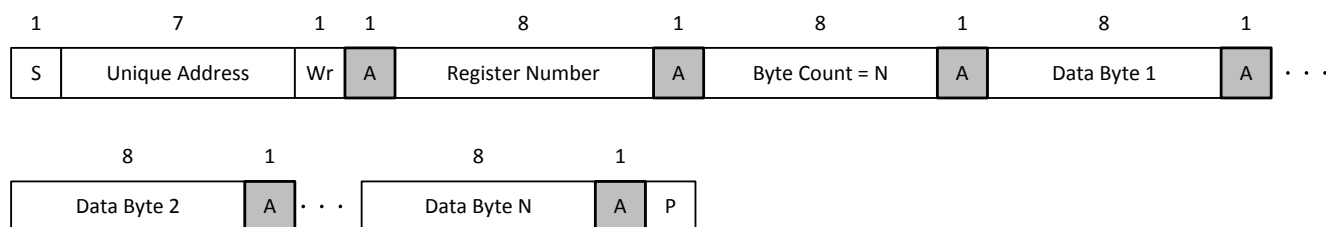


Figure 8-22. I²C Unique Address Write Register Protocol

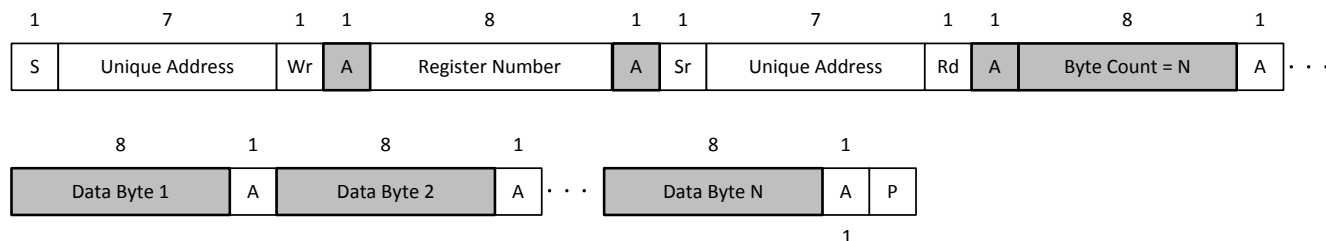


Figure 8-23. I²C Unique Address Read Register Protocol

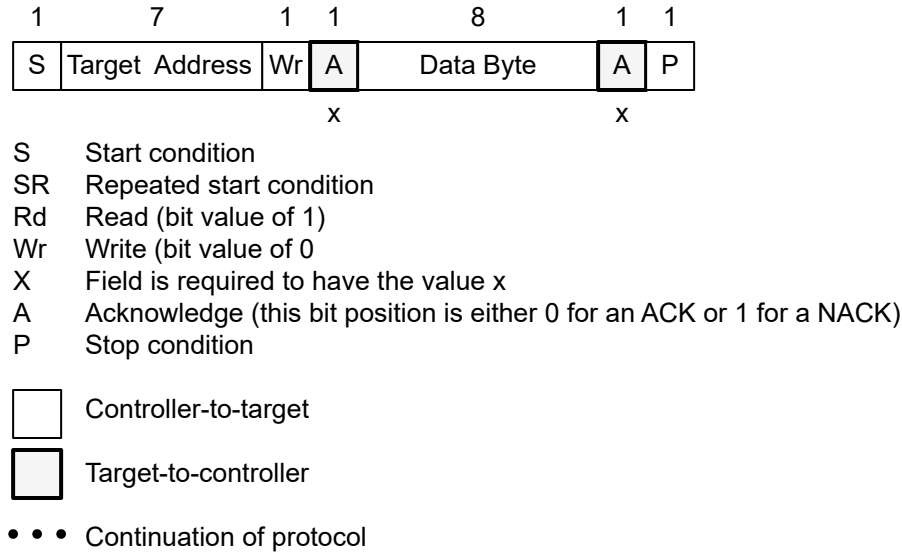


Figure 8-24. I²C Read/Write Protocol Key

8.3.8.2.1.3 Pin Strapping to Configure Default Behavior

During the boot procedure, the device reads the ADCINx pins and sets the I²C address and configuration based on the table below.

Table 8-4. Device I2C Configuration using ADCIN1

ADCIN1 DECODED VALUE (MIN VOLTAGE) (1)	I ² C ADDRESS	DEAD BATTERY CONFIGURATION
0 (5V)	0x20	EnableSinkAfterContract: The device enables the sink path upon entering a power contract. The device evaluates power upon implicit and explicit contract negotiations.
1 (9V)	0x21	
2 (12V)	0x20	
3 (15V)	0x21	
4 (20V)	0x20	

(1) See [Section 8.3.6](#) for how to configure a given ADCINx decoded value.

8.3.9 Digital Core

Figure 8-25 shows a simplified block diagram of the digital core.

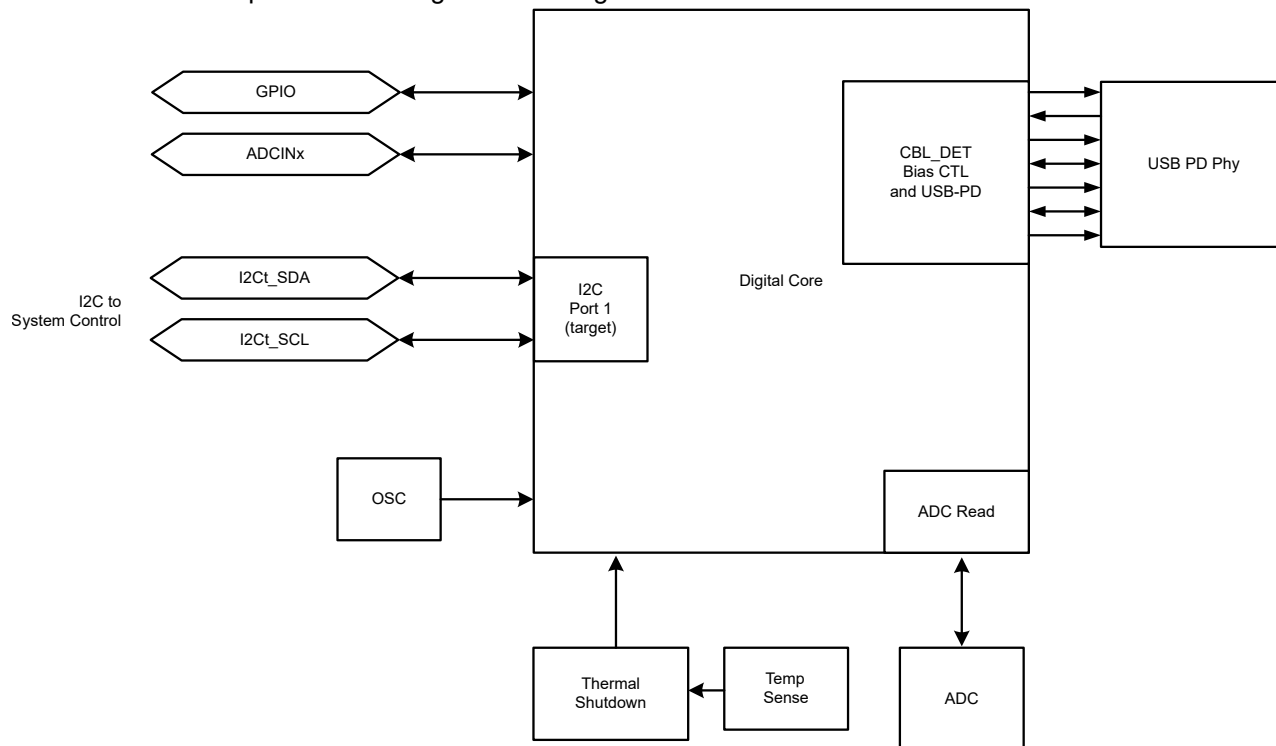


Figure 8-25. Digital Core Block Diagram

8.3.10 Minimum Voltage Configuration

The minimum voltage for the USB Power Delivery Sink Capabilities can be set according to the table below. When the received USB PD Source Capabilities do not meet the required power range based on the minimum and maximum voltage, as well as the operating and maximum current, the Capabilities Mismatch bit is set on the USB PD request. When the Minimum Voltage is set greater than 5V the Higher Capability bit is set in the Sink Capabilities.

Table 8-5. Minimum Voltage Configuration for Sink Capabilities - ADCIN1 Decoded

ADCIN1 Decoded Value	Minimum Voltage Configuration
0	5V
1	9V
2	12V
3	15V
4	20V
5	Reserved
6	Reserved
7	Reserved

8.3.11 Maximum Voltage Configuration

The maximum voltage for the USB Power Delivery Sink Capabilities is set according to the table below. When the received USB PD Source Capabilities do not meet the minimum and maximum voltage range the Capabilities Mismatch bit is set on the USB PD request.

Table 8-6. Maximum Voltage Configuration for Sink Capabilities - ADCIN2 Decoded

ADCIN2 Decoded Value	PD5VMAX Decoded Value	Maximum Voltage Configuration	Auto disable Sink Upon Capmismatch
0	1	5V	Yes
1	1	5V	No
0	0	9V	Yes
1	0	9V	No
2	0	12V	Yes
3	0	12V	No
4	0	15V	Yes
5	0	15V	No
6	0	20V	Yes
7	0	20V	No

8.3.12 Sink Current Configuration

The sink current is configured according to [Table 8-7](#). The configuration sets maximum current in the USB PD request message. The operating current is defined as the current required for the sink to be functional. The maximum current is defined as the maximum current the sink can use. The operating and maximum current can be the same if the operational current is the maximum current required for the sink to be functional. The capabilities mismatch bit is set when the PD source capabilities do not meet the power required for the device, defined by the minimum voltage and operating current settings. When the operating current is set to 0A the capability mismatch bit is not set.

Note

If Operating Current is set to 0A, ADCIN2 must be designed to set Auto disable Sink Upon Capamismatch to 0.

Table 8-7. ADCIN3 & ADCIN4 Sink Current Configuration

ADCIN3	ADCIN4	Operating Current	Maximum Current
0	0	0	1.5A
0	1	0	3A
0	2	0	4A
0	3	0	5A
0	4	0.5A	1.5A
0	5	0.5A	3A
0	6	0.5A	4A
0	7	0.5A	5A
1	0	1A	1.5A
1	1	1A	3A
1	2	1A	4A
1	3	1A	5A
1	4	1.5A	1.5A

Table 8-7. ADCIN3 & ADCIN4 Sink Current Configuration (continued)

ADCIN3	ADCIN4	Operating Current	Maximum Current
1	5	1.5A	3A
1	6	1.5A	4A
1	7	1.5A	5A
2	1	2A	3A
2	2	2A	4A
2	3	2A	5A
2	5	2.5A	3A
2	6	2.5A	4A
2	7	2.5A	5A
3	1	3A	3A
3	2	3A	4A
3	3	3A	5A
3	6	3.5A	4A
3	7	3.5A	5A
4	2	4A	4A
4	3	4A	5A
4	7	4.5A	5A
5	3	5A	5A

8.3.13 Auto-negotiate Sink Minimum Power

The minimum power required is determined by the operating current configuration multiplied by the minimum voltage configuration. When the received PD source capabilities power do not meet the auto-negotiate sink minimum power the capability mismatch bit is set in the PD request message.

Note

Align power requirements to PD power requirements for current and voltage if the system must only be powered off of PD power.

Table 8-8. Auto-Negotiate Sink Minimum Power Example

ADCIN1	ADCIN2	Minimum Voltage	Maximum Voltage	ADCIN3	ADCIN4	Operating Current	Maximum Current	Minimum Power
0	5	5V	15V	3	1	3A	3A	15W
0	7	5V	20V	5	3	5A	5A	25W

8.3.14 Extended Sink Capabilities Power Delivery Power

The Extend Sink Capabilities Power Delivery Power for Minimum, Operational, and Maximum PDP are determined by the configured Maximum/Minimum Voltage Configuration and the Current Configuration.

Table 8-9. Extended Sink Capabilities Power Delivery Power Example

Power Delivery Power	ADCIN3/4 = 3/3	ADCIN1/2 = 0/6
Minimum PDP = 25W	Maximum Current = 5A	Minimum Voltage = 5V
Operational PDP = 100W	Maximum Current = 5A	Maximum Voltage = 20V
Maximum PDP = 100W	Maximum Current = 5A	Maximum Voltage = 20V

8.4 Device Functional Modes

8.4.1 Power States

The TPS25730A can operate in one of three different power states: Active, Idle, or Sleep. The Modern Standby mode is a special case of the Idle mode. The functionality available in each state is summarized in [Table 8-10](#). The device automatically transitions between the three power states based on the circuits that are active and required. See [Figure 8-26](#). In the Sleep state, the TPS25730A detects a Type-C connection. Transitioning between the Active mode to Idle mode requires a period of time (T) without any of the following activity:

- Incoming USB PD message
- Change in CC status
- GPIO input event
- I²C transactions
- Voltage alert
- Fault alert

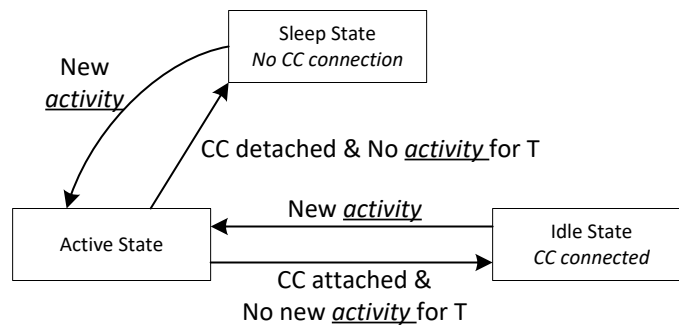


Figure 8-26. Flow Diagram for Power States

Table 8-10. Power Consumption States

	ACTIVE SINK MODE ⁽²⁾	IDLE SINK MODE	SLEEP MODE ⁽¹⁾
PP_HV (TPS25730AD)	enabled	enabled	disabled
PP_EXT (TPS25730AS)	enabled	enabled	disabled
external CC1 termination	Rp 3.0A	Rp 3.0A	open
external CC2 termination	open	open	open

(1) This mode is used for: I_{VIN_3V3,Sleep}

(2) This mode is used for: I_{VIN_3V3,ActSnk}

8.4.2 Schottky for Current Surge Protection

To prevent the possibility of large ground currents into the TPS25730A during sudden disconnects due to inductive effects in a cable, TI recommends that a Schottky diode be placed from VBUS to ground.

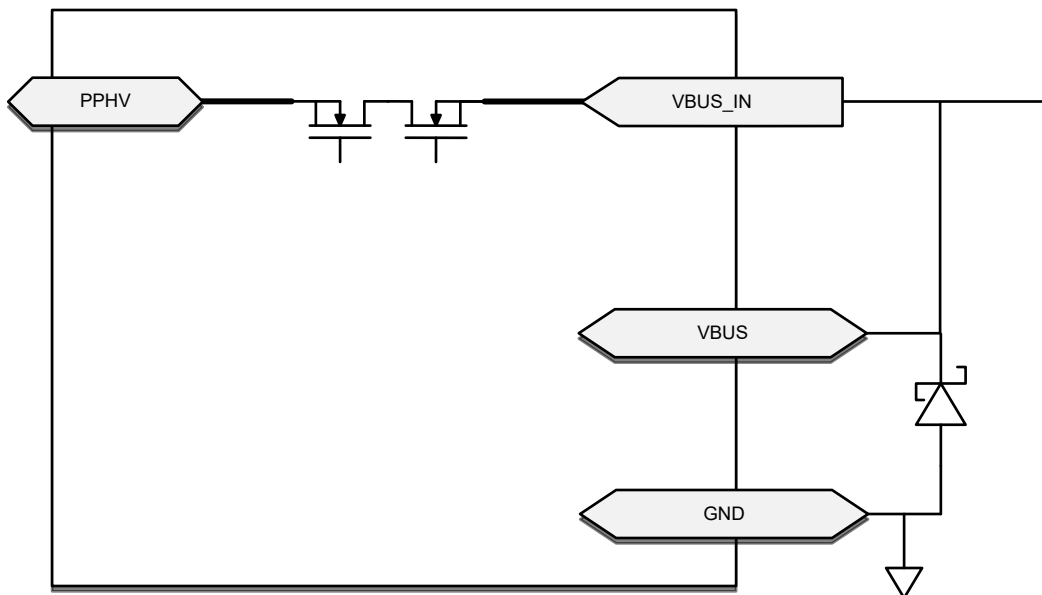


Figure 8-27. TPS25730AD Schottky for Current Surge Protection

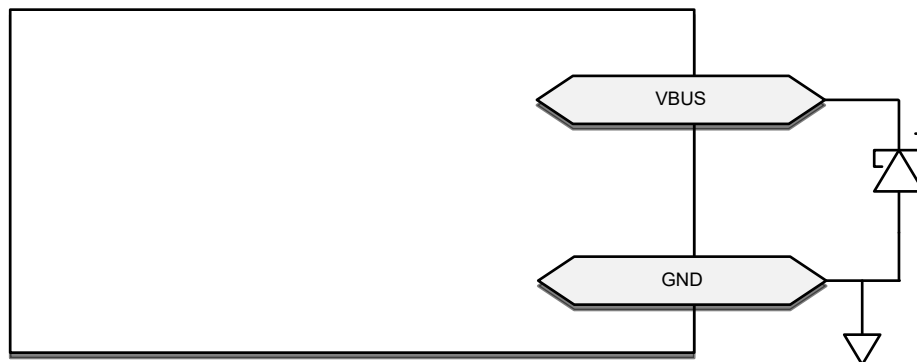


Figure 8-28. TPS25730AS Schottky for Current Surge Protection

8.4.3 Thermal Shutdown

The TPS25730A features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all functions except for supervisory circuitry when die temperature goes above a rising temperature of T_{SD_MAIN} . The temperature shutdown has a hysteresis of T_{SDH_MAIN} and when the temperature falls back below this value, the device resumes normal operation.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS25730A is a highly integrated stand-alone USB Type-C and Power Delivery (PD) optimized for sink only applications. The TPS25730A voltage and current requirements are fully configurable with resistor pin strapping. There is no need for an external EEPROM, an external microcontroller, or any firmware development.

Sink Power Configurations

The TPS25730A chooses which Power Data Object (PDO) to request based on the sink capability configuration. The sink capabilities are configured based on the ADCINx settings as shown in Table below.

Table 9-1. TPS25730A Transmit Sink Capabilities

Power Data Object (PDO)	Sink Capabilities
PDO 1	Fixed Supply Operating Current = ADCIN3 Voltage = 5V
PDO 2	Variable Supply Operating Current = ADCIN4 Minimum Voltage = ADCIN1 Maximum Voltage = ADCIN2 ⁽¹⁾

(1) Maximum Voltage is set to PD5VMAX for 5V-only applications

9.2 Typical Application

9.2.1 Design Requirements

For barrel jack replacement applications, the TPS25730A is configured to negotiate a PD contract according to the voltage required by the system. The TPS25730A supports 5V, 9V, 12V, 15V, and 20V up to 5A. Power is provided to the system from VBUS through the power path on the PD controller.

9.2.2 Detailed Design Procedure

The ADCINx pin configurations on the TPS25730A allows the user to select the supported voltage and current range. The following table shows two examples of the sink path behavior for a 9V system.

Example	ADCIN1	ADCIN2	Minimum Voltage	Maximum Voltage	ADCIN3	ADCIN4	Operating Current	Maximum Current	Minimum Power	Auto Disable Sink Path Upon Cap Mis
A	1	1	9V	9V	3	1	3A	3A	27W	No
B	1	0	9V	9V	3	1	3A	3A	27W	Yes

A : If a 5V/3A PD Source Adapter is plugged in, the TPS25730A asserts the capability mismatch bit. The sink path is enabled and allows 5V to pass through to the system. Refer to [Figure 9-1](#)

B: If a 5V/3A PD Source Adapter is plugged in, the TPS25730A asserts the capability mismatch bit. The sink path is disabled and prevents 5V to pass through to the system. Refer to [Figure 9-2](#)

9.2.3 Application Curves

The following figures show the GPIO, VBUS, CC1, CC2 and PPHV behavior for various conditions.

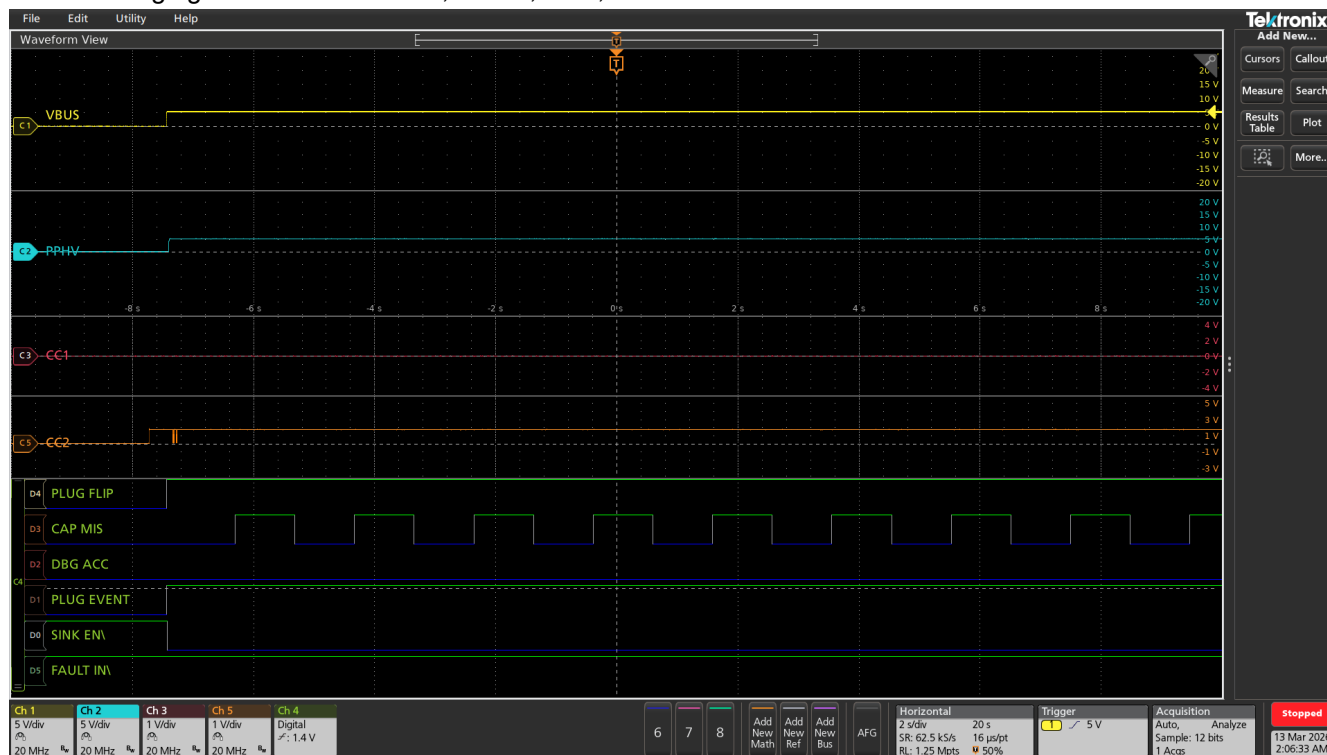


Figure 9-1. PD Contract with Capability Mismatch and PPHV Enabled

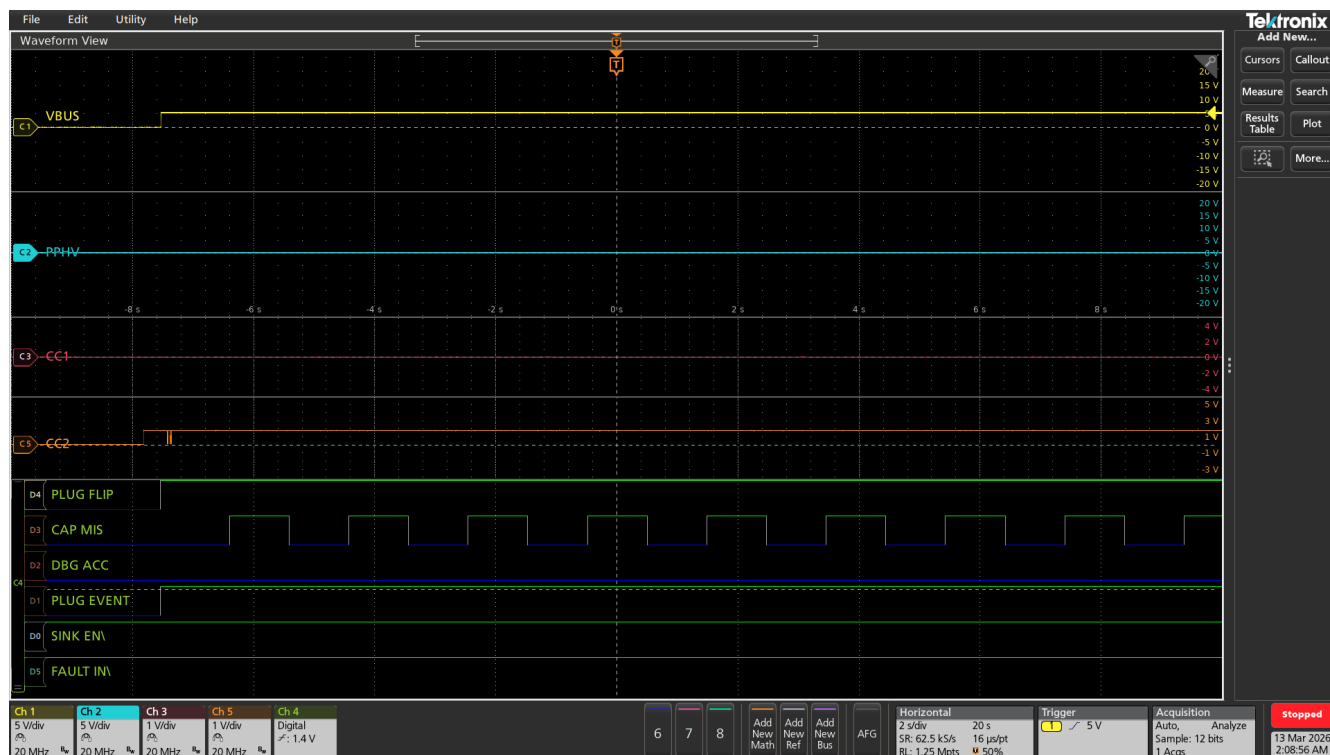


Figure 9-2. PD Contract with Capability Mismatch and PPHV Disabled

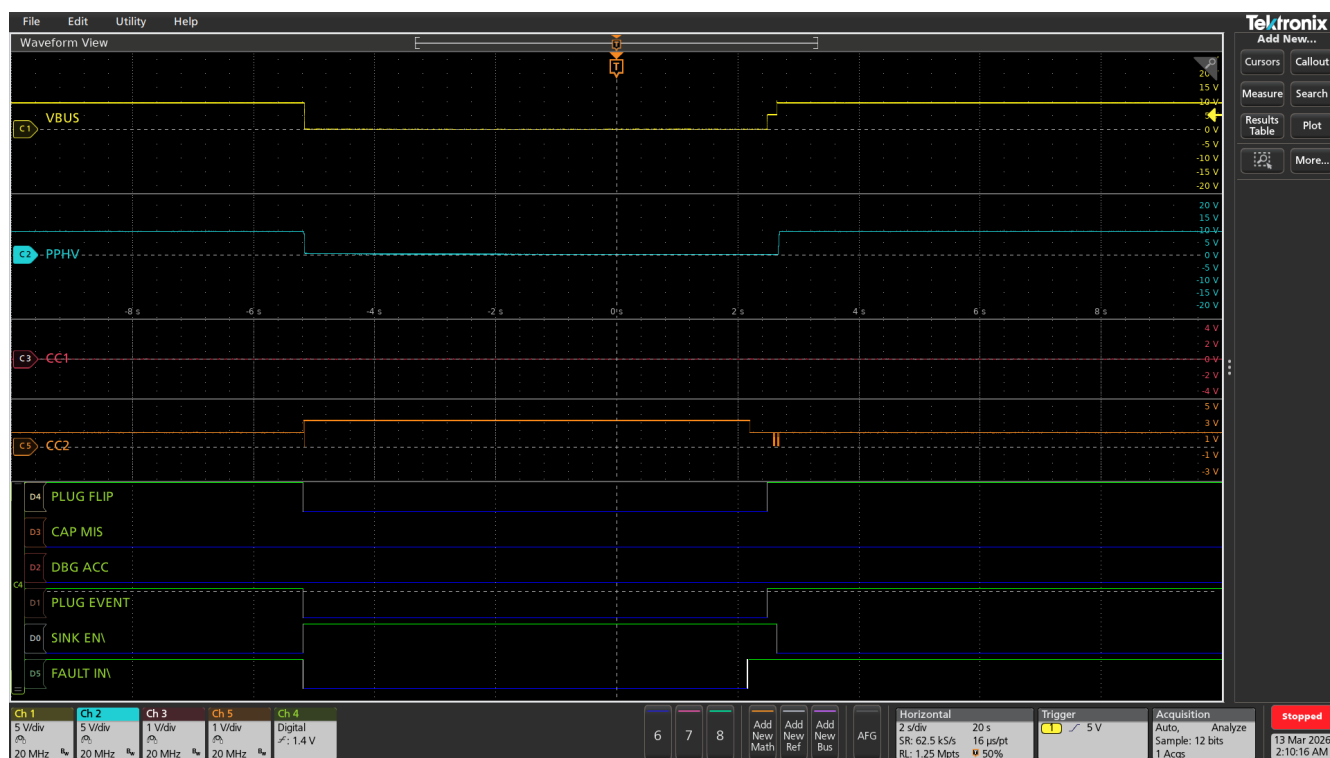


Figure 9-3. PD Contract with FAULT_IN asserted and VBUS disconnected

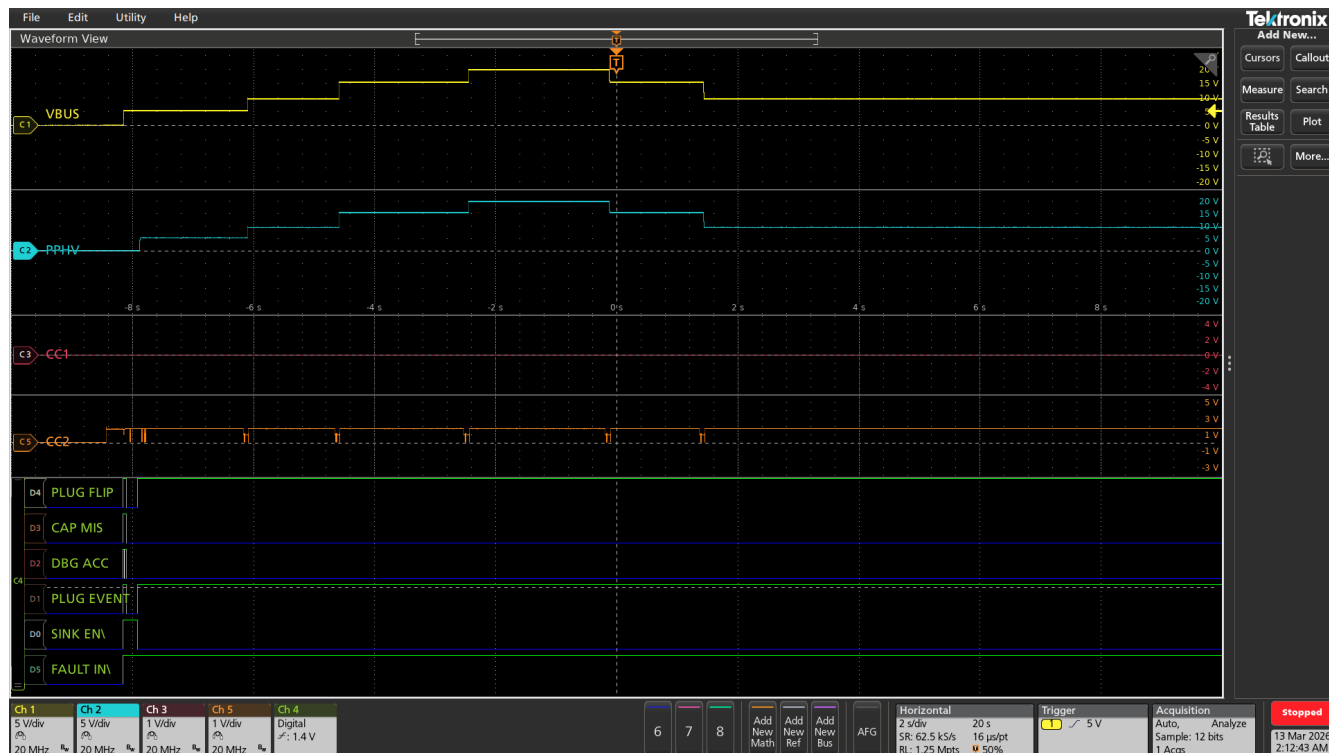


Figure 9-4. PD Contract Negotiation of 5V, 9V, 15V, and 20V

9.3 Power Supply Recommendations

9.3.1 3.3V Power

9.3.1.1 VIN_3V3 Input Switch

The VIN_3V3 input is the main supply of the TPS25730A device. The VIN_3V3 switch (see [Section 8.3.2](#)) is a uni-directional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when the 3.3V supply is available. The recommended capacitance C_{VIN_3V3} (see [Section 6.4](#)) must be connected from the VIN_3V3 pin to the GND pin. Do not power VIN_3V3 from VBUS.

9.3.2 1.5V Power

The internal circuitry is powered from 1.5V. The 1.5V LDO steps the voltage down from LDO_3V3 to 1.5V. The 1.5V LDO provides power to all internal low-voltage digital circuits which includes the digital core and memory. The 1.5V LDO also provides power to all internal low-voltage analog circuits. Connect the recommended capacitance C_{LDO_1V5} (see [Section 6.4](#)) from the LDO_1V5 pin to the GND pin.

9.3.3 Recommended Supply Load Capacitance

[Section 6.4](#) lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowed for tolerances and voltage derating ensuring proper operation.

9.4 Layout

9.4.1 TPS25730AD - Layout

9.4.1.1 Layout Guidelines

Proper routing and placement maintain signal integrity for high speed signals and improve the heat dissipation from the power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. Best practice is to consult with board manufacturing to verify manufacturing capabilities.

9.4.1.1.1 Top Placement and Bottom Component Placement and Layout

When the TPS25730A is placed on top and its components on bottom, the solution size is at its smallest.

9.4.1.2 Layout Example

Follow the differential impedances for Super / High Speed signals defined by their specifications (USB2.0). All I/O are fanned out to provide an example for routing out all pins, not all designs utilize all of the I/O on the TPS25730A.

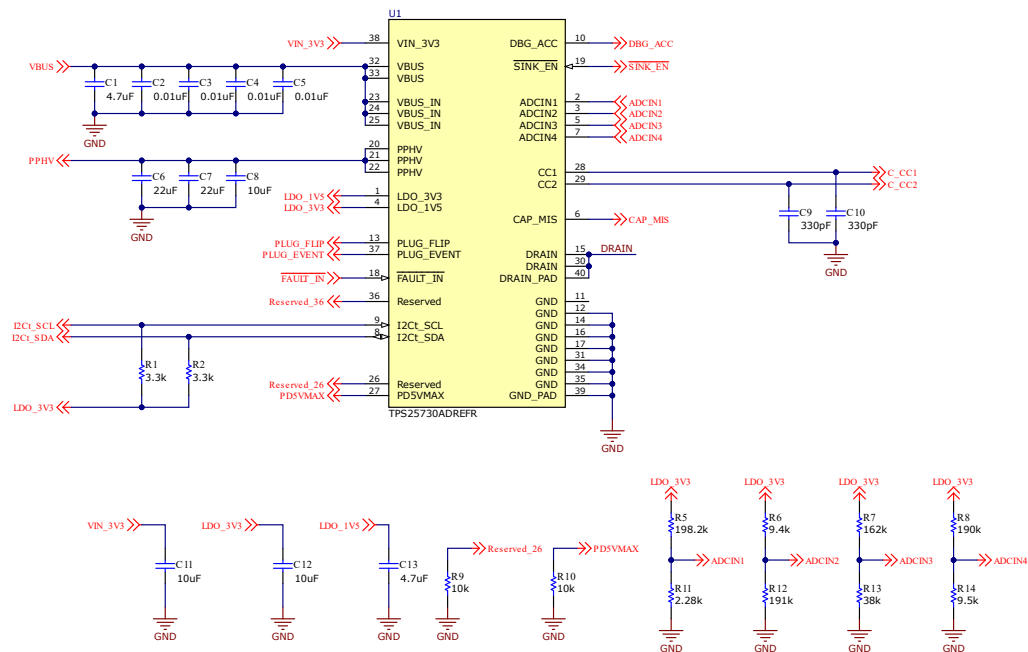


Figure 9-5. Example Schematic

9.4.1.3 Component Placement

Top and bottom placement is used for this example to minimize solution size. The TPS25730AD is placed on the top side of the board and the majority of its components are placed on the bottom side. When placing the components on the bottom side, TI recommends that the components are placed directly under the TPS25730AD. When placing the VBUS and PPHV capacitors, it is easiest to place them with the GND terminal of the capacitors to face outward from the TPS25730AD or to the side because the drain connection pads on the bottom layer must not be connected to anything and left floating. All other components that are for pins on the GND pad side of the TPS25730AD must be placed where the GND terminal is underneath the GND pad.

The CC capacitors must be placed on the same side as the TPS25730AD close to the respective CC1 and CC2 pins. Do NOT via to another layer in between the CC pins to the CC capacitor, placing a via after the CC capacitor is recommended.

Figure 9-6 through Figure 9-7 show the placement in 2D and 3D.

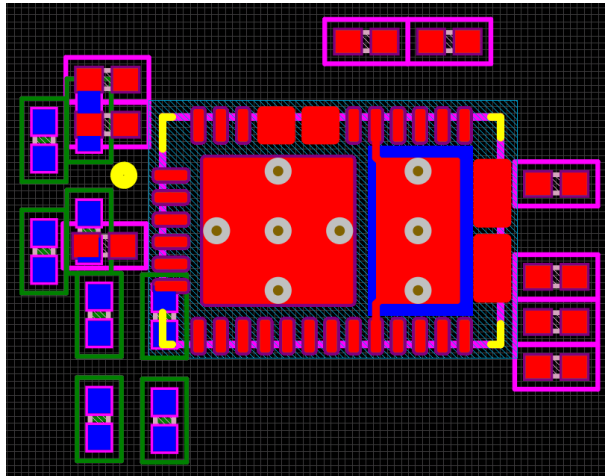


Figure 9-6. Top View Layout

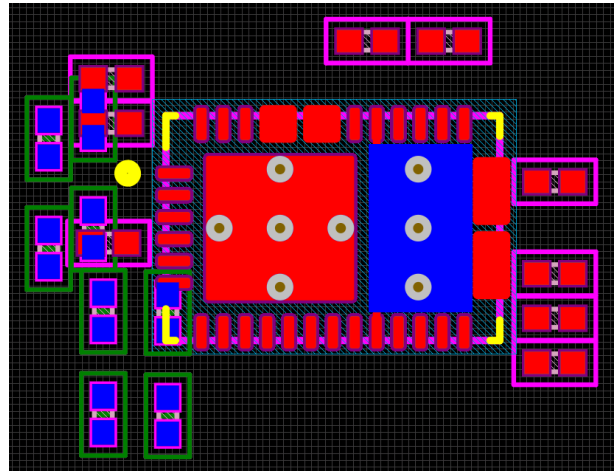


Figure 9-7. Bottom View Layout

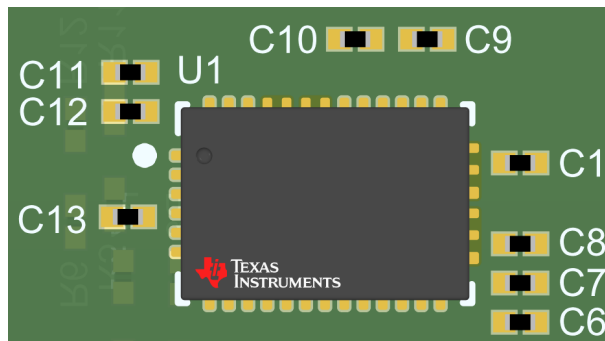


Figure 9-8. Top View 3D

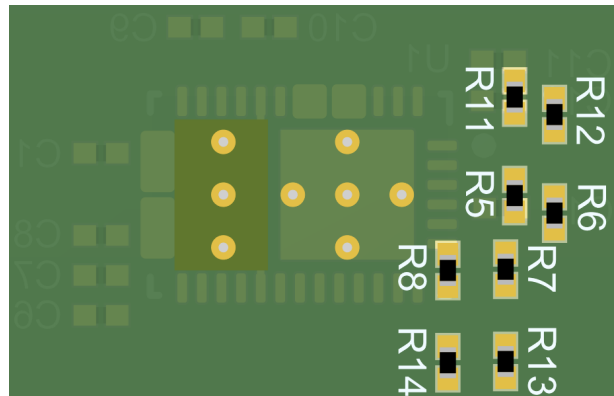


Figure 9-9. Bottom View 3D

9.4.1.4 Routing VBUS, VIN_3V3, LDO_3V3, LDO_1V5

On the top side, create pours for VBUS, VBUS_IN, and PPHV. Connect VBUS from the top layer to the bottom layer using at least 6 8-mil hole and 16-mil diameter vias. See [Figure 9-10](#) for the recommended via sizing. For VBUS_IN and PPHV, connect from the top to bottom layer using 15 8-mil hole and 16-mil diameter vias. The via placement and copper pours are highlighted in [Figure 9-11](#).



Figure 9-10. Recommended Minimum Via Sizing

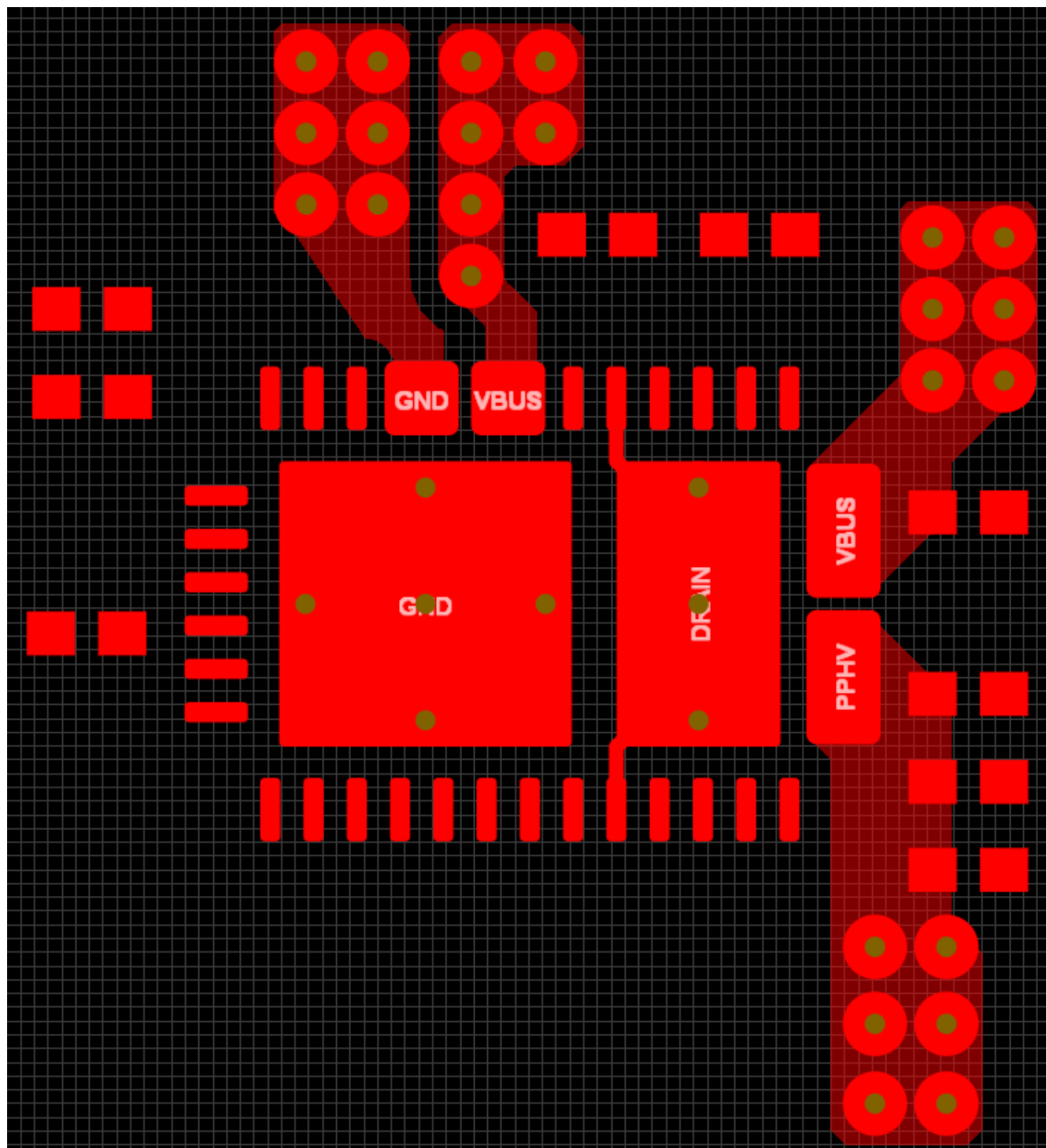


Figure 9-11. VBUS, VBUS_IN, and PPHV Copper Pours and Via Placement

Next, VIN_3V3, LDO_3V3, and LDO_1V5 route to their respective decoupling capacitors. Additionally, a copper pour on the bottom side is added to connect PPHV to their decoupling capacitors located on the bottom of the PCB. This action is highlighted in [Figure 9-12](#).

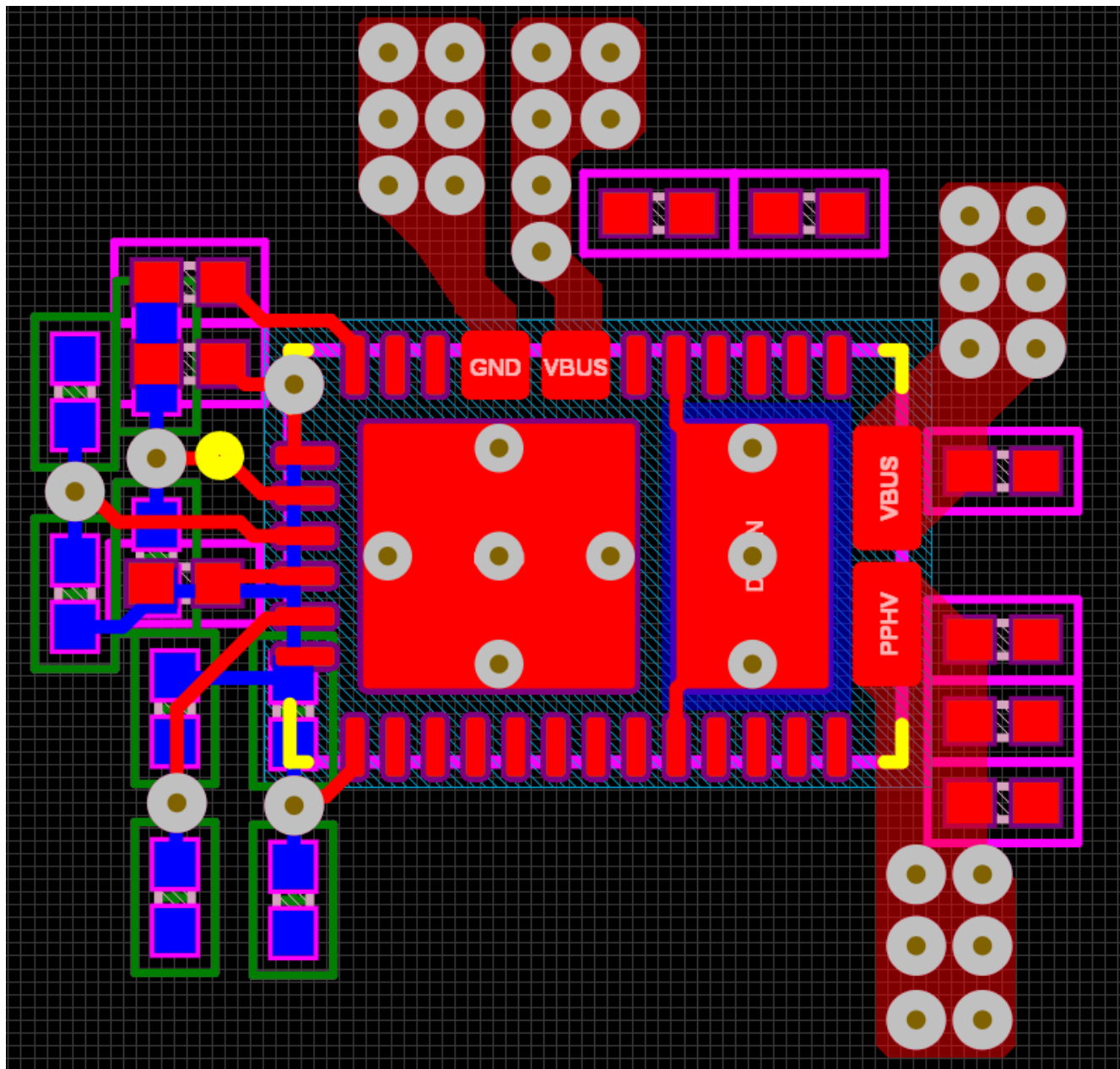


Figure 9-12. VIN_3V3, LDO_3V3, and LDO_1V5 Routing

9.4.1.5 Routing CC and GPIO

Routing the CC lines with a 10-mil trace ensures the needed current for supporting powered Type-C cables through VCONN. For more information on VCONN refer to the Type-C specification. For capacitor GND pin use a 16-mil trace if possible.

Most of the GPIO signals can be fanned out on the top or bottom layer using either a 8-mil or 10-mil trace. The following images highlights how the CC lines and GPIOs are routed out.

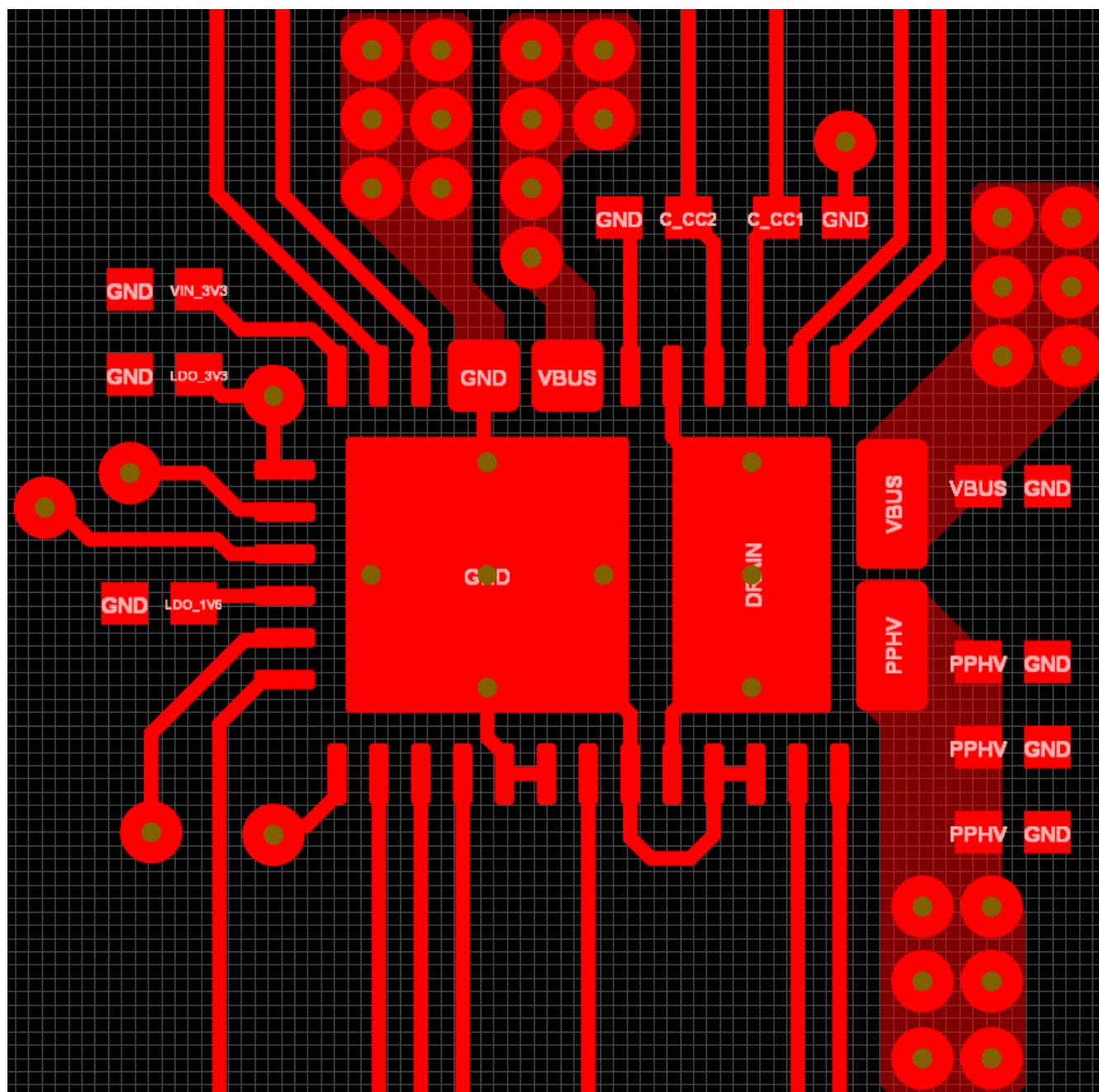


Figure 9-13. Top Layer GPIO Routing

Table 9-2. Routing Widths

ROUTE	WIDTH (MIL MINIMUM)
CC1, CC2	8
VIN_3V3, LDO_3V3, LDO_1V8	8
Component GND	10
GPIO	8

9.4.2 TPS25730AS - Layout

9.4.2.1 Layout Guidelines

Proper routing and placement maintain signal integrity for high speed signals and improve the heat dissipation from the power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. Best practice is to consult with board manufacturing to verify manufacturing capabilities.

9.4.2.1.1 Top Placement and Bottom Component Placement and Layout

When the TPS25730A is placed on top and its components on bottom, the solution size is at its smallest.

9.4.2.2 Layout Example

Follow the differential impedances for Super / High Speed signals defined by their specifications (USB2.0). All I/O are fanned out to provide an example for routing out all pins, not all designs utilize all of the I/O on the TPS25730AS.

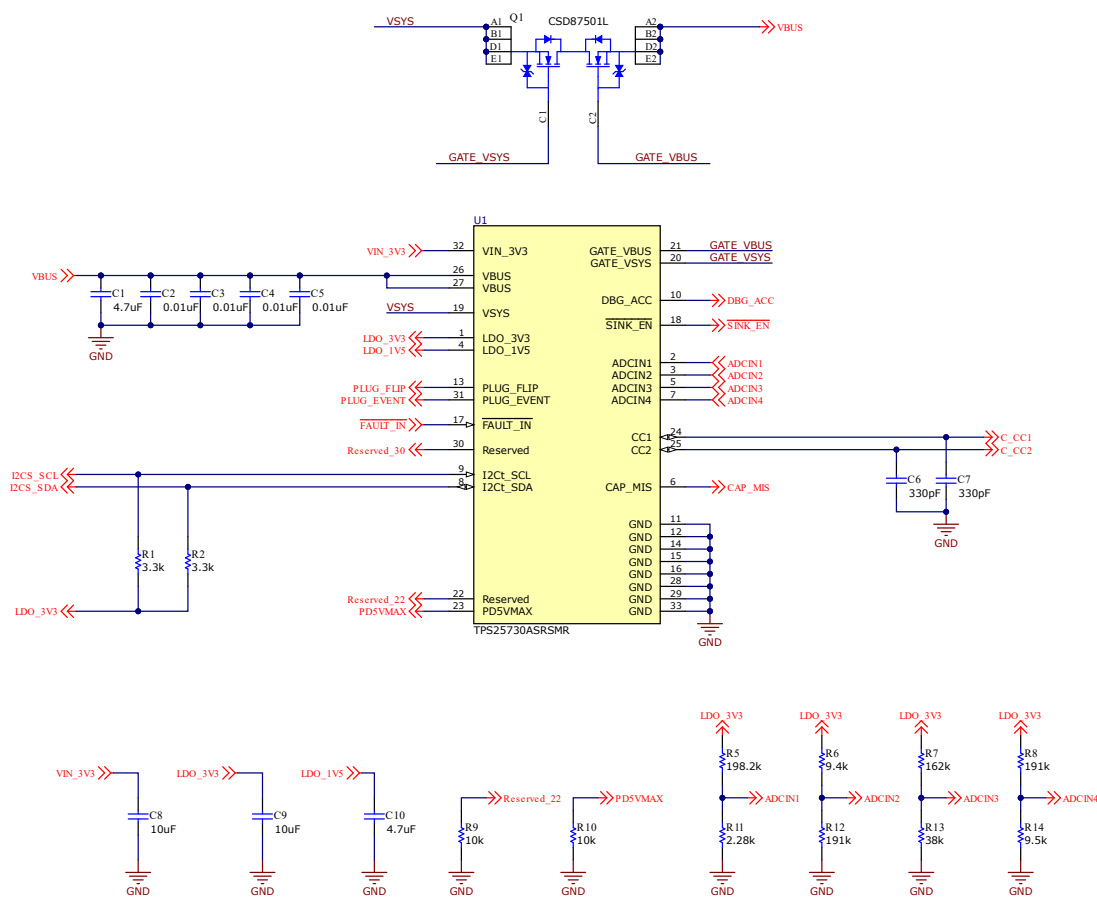
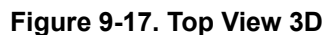


Figure 9-14. Example Schematic

9.4.2.3 Component Placement

Top and bottom placement is used for this example to minimize solution size. The TPS25730AS is placed on the top side of the board and the majority of its components are placed on the bottom side. When placing the components on the bottom side, TI recommends that they are placed directly under the TPS25730AS. All other components that are for pins on the GND pad side of the TPS25730AS must be placed where the GND terminal is underneath the GND pad.

Figure 9-15 through Figure 9-16 show the placement in 2D and 3D.



8mil 16mil

51

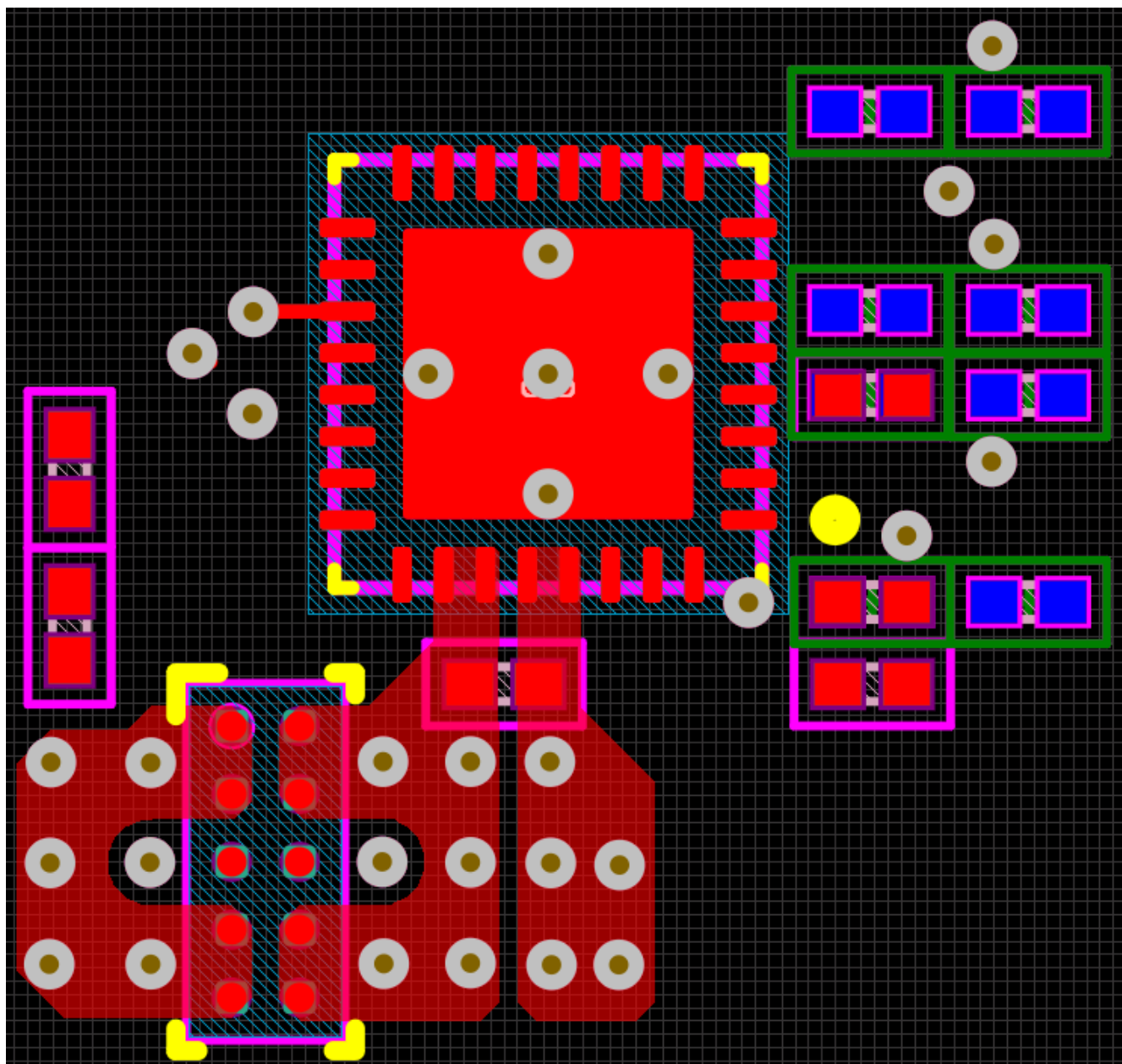


Figure 9-20. VBUS Copper Pours and Via Placement

Next, VIN_3V3, LDO_3V3, and LDO_1V5 are routed to their respective decoupling capacitors. This action is highlighted in [Figure 9-21](#).

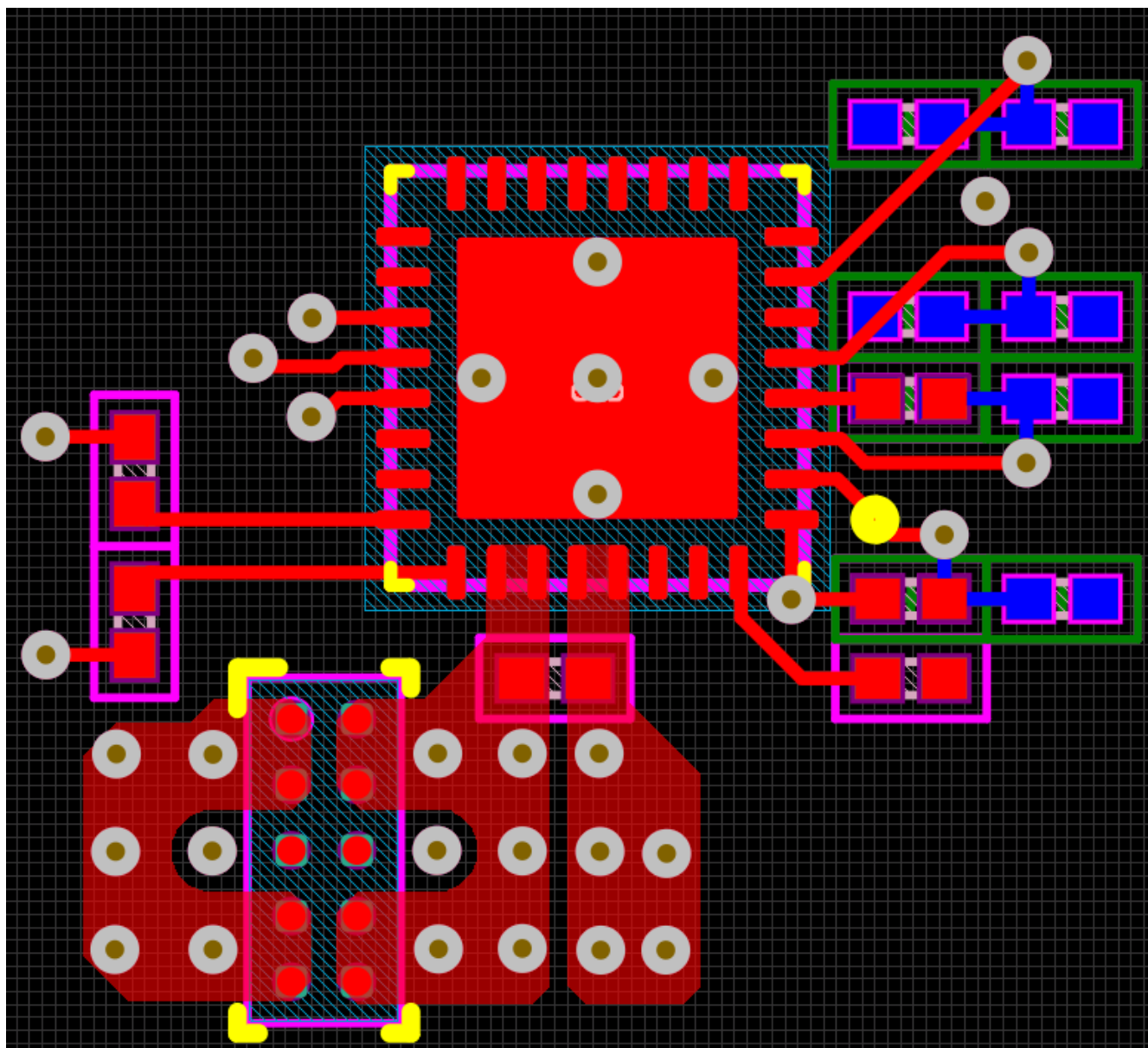


Figure 9-21. VIN_3V3, LDO_3V3, and LDO_1V5 Routing

Figure 9-22 and Figure 9-23 show how to properly connect V_{SY} and the SYS_Gate control signals for the external N-FETs. The control signals can be routed on an internal layer using a 12-mil trace, and the trace going to V_{SY} must be as short as possible to minimize impedance, so placing a via directly on the high-voltage power path is ideal.

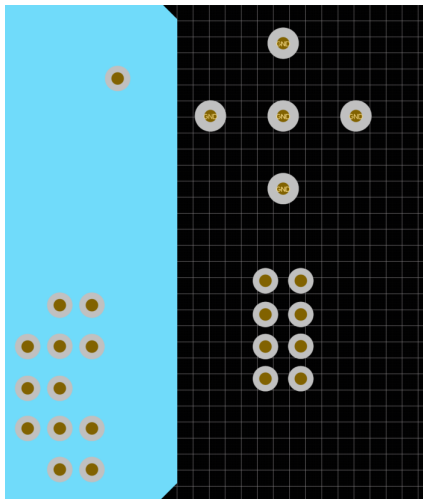


Figure 9-22. Top Polygon Pours

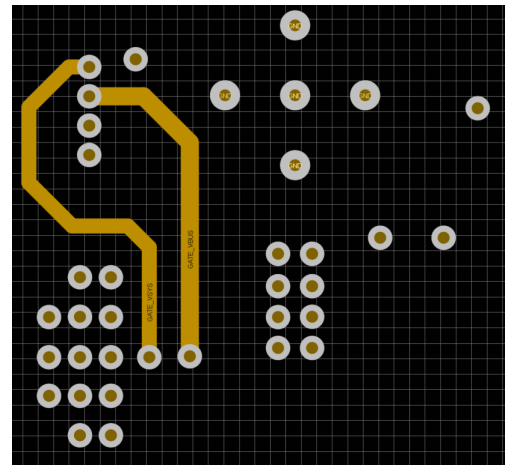


Figure 9-23. Bottom Polygon Pours

9.4.2.5 Routing CC and GPIO

Routing the CC lines with a 10-mil trace ensures the needed current for supporting powered Type-C cables through VCONN. For more information on VCONN refer to the Type-C specification. For capacitor GND pin use a 16-mil trace if possible.

Most of the GPIO signals can be fanned out on the top or bottom layer using either a 8-mil trace or a 10-mil trace. The following images highlight how the CC lines and GPIOs are routed out.

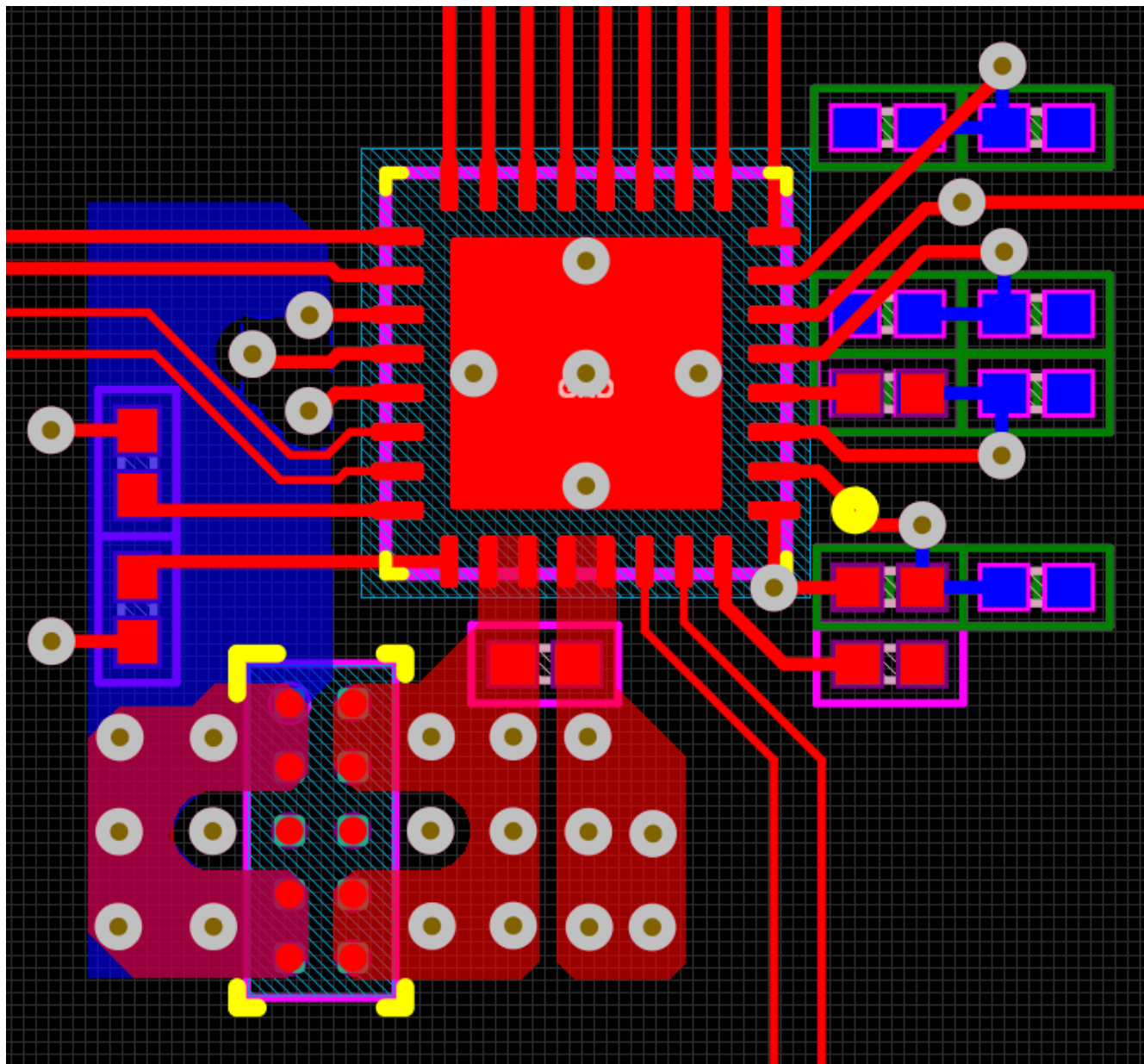


Figure 9-24. Top Layer GPIO Routing

Table 9-3. Routing Widths

ROUTE	WIDTH (MIL MINIMUM)
PA_CC1, PA_CC2, PB_CC1, PB_CC2	8
VIN_3V3, LDO_3V3, LDO_1V8	6
Component GND	10
GPIO	4

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.2 Documentation Support

10.2.1 Related Documentation

- [USB-PD Specifications](#)
- [USB Power Delivery Specification](#)

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.5 Trademarks

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USB Type-C® is a registered trademark of USB Implementers Forum.

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10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2026) to Revision A (July 2026)	Page
• Added PD 3.2 certification TID #.....	1
• Added "additional features".....	1
• Updated applications for the device.....	1
• Updated Section 5 I2C controller capitalization for consistency.....	4
• Updated table formatting.....	8
• Deleted source current absolute maximum on I2C SCL/SDA.....	8
• Changed voltage for GPIOx from 6.0 to 6.....	8
• Updated table heading to include 'parameter' description.....	8

• Updated table column to include 'parameter' heading.....	8
• Updated table formatting	9
• Updated table formatting.....	10
• Changed C _{V_{SS}} device from TPS25730A to TPS25730AS.....	10
• Updated title to include part number.....	11
• Updated formatting in part number in table.....	11
• Updated operating conditions for clarity.....	11
• Deleted standby power modes.....	12
• Updated operating conditions.....	12
• Updated table formatting.....	14
• Updated operating conditions.....	16
• Updated operating conditions.....	16
• Updated table formatting	16
• Deleted fast mode plus characteristics.....	17
• Updated section to revise sink path to be named powerpath.....	28
• Updated section to revise sink path to be named powerpath.....	28
• Updated dead battery configuration column in table for clarity.....	35
• Updated I ² C address definition in table.....	35
• Added note about the relationship between Auto Disable on Capabilities Mismatch and Operating Current..	37
• Added note for minimum power PD requirements.....	38
• Updated Table 8-10 Table 8-10	39
• Deleted redundant information from VIN_3V3 power requirements.....	44

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25730ADREFR	Active	Production	WQFN (REF) 38	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25730A D
TPS25730ASRSMR	Active	Production	VQFN (RSM) 32	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25730A S

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

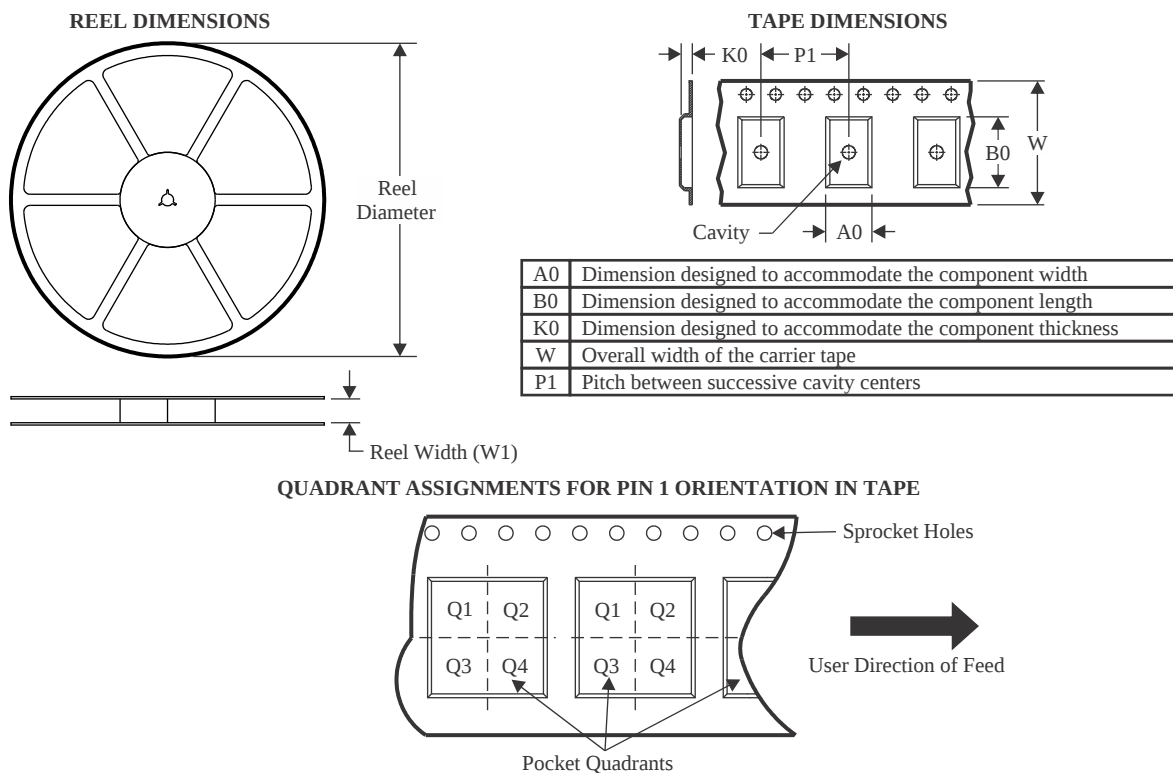
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

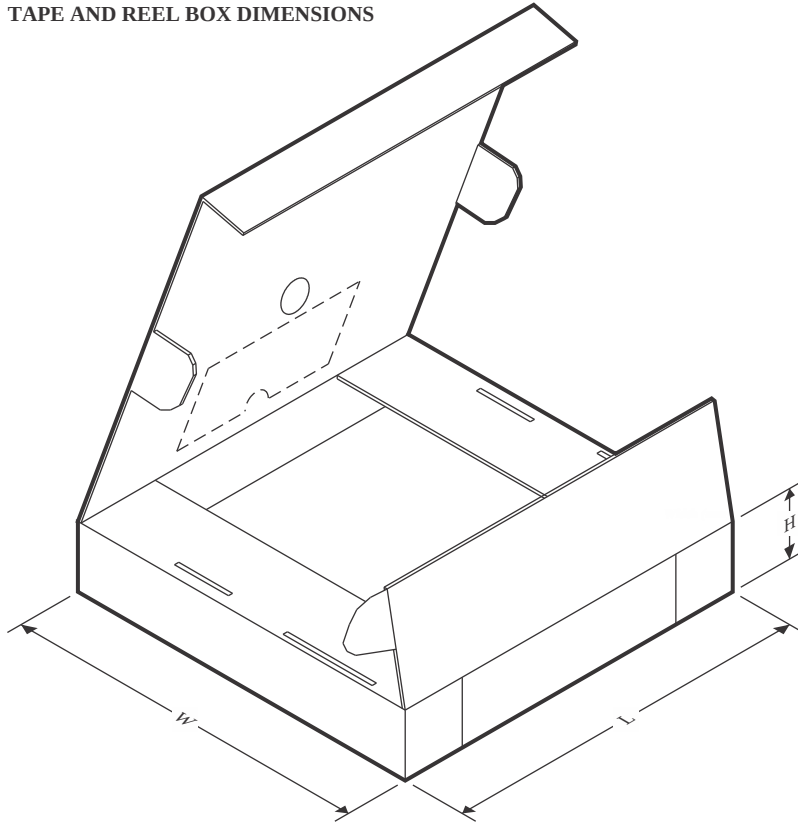
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25730ADREFR	WQFN	REF	38	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TPS25730ASRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25730ADREFR	WQFN	REF	38	3000	360.0	360.0	36.0
TPS25730ASRSMR	VQFN	RSM	32	3000	360.0	360.0	36.0



PACKAGE OUTLINE

WQFN - 0.8 mm max height

The drawing illustrates the mechanical specifications of a 24-pin LQFP package. The top view shows a square body with a pin 1 index area in the top-left corner. Dimensions include a total width of 6.1 mm (5.9 mm to the center of the pins) and a total height of 4.1 mm (3.9 mm to the center of the pins). A detail view of a pin shows a top width of 0.45 mm and a bottom width of 0.25 mm, with a thickness of 0.15 mm.

The side view shows a package height of 0.8 mm (0.7 mm to the top of the body, 0.05 mm to the bottom of the pins) and a seating plane at the base. A cross-section symbol indicates a view through the package.

The bottom view shows the pin layout with 24 pins (12 on each long side). Key dimensions include a pin pitch of 0.4 mm (30X), a pin width of 0.25 mm (38X), and a pin-to-pin distance of 0.15 mm (38X). The package is symmetrical (SYMM) about a centerline. A detail view of the pin 1 ID is shown as a 45-degree chamfer with a width of 0.3 mm. A table of dimensions is provided at the bottom right:

0.07	C	A	B
0.05			

The package is labeled with 'PKG' and a centerline symbol.

NOTES:

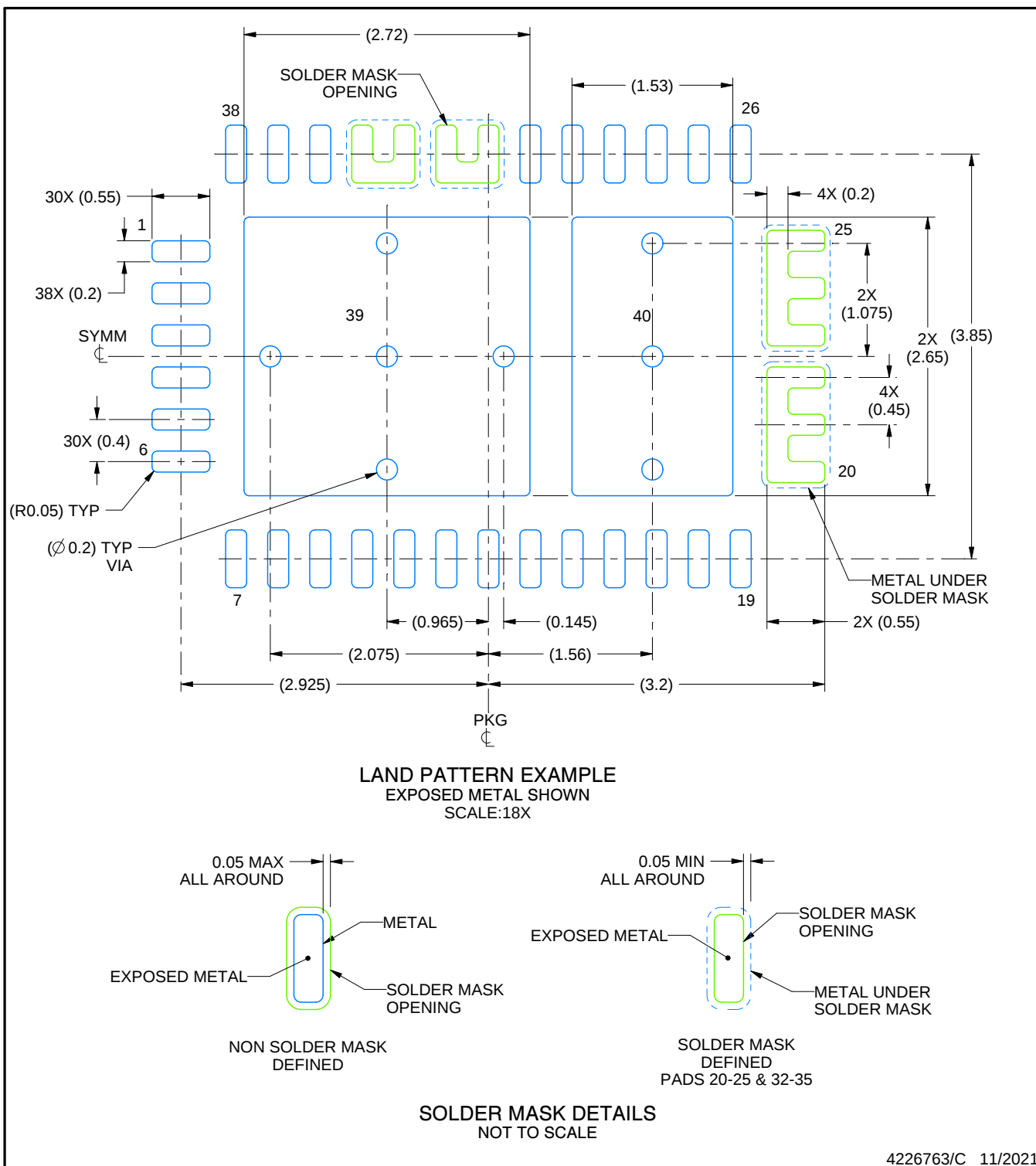
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

REF0038A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4226763/C 11/2021

NOTES: (continued)

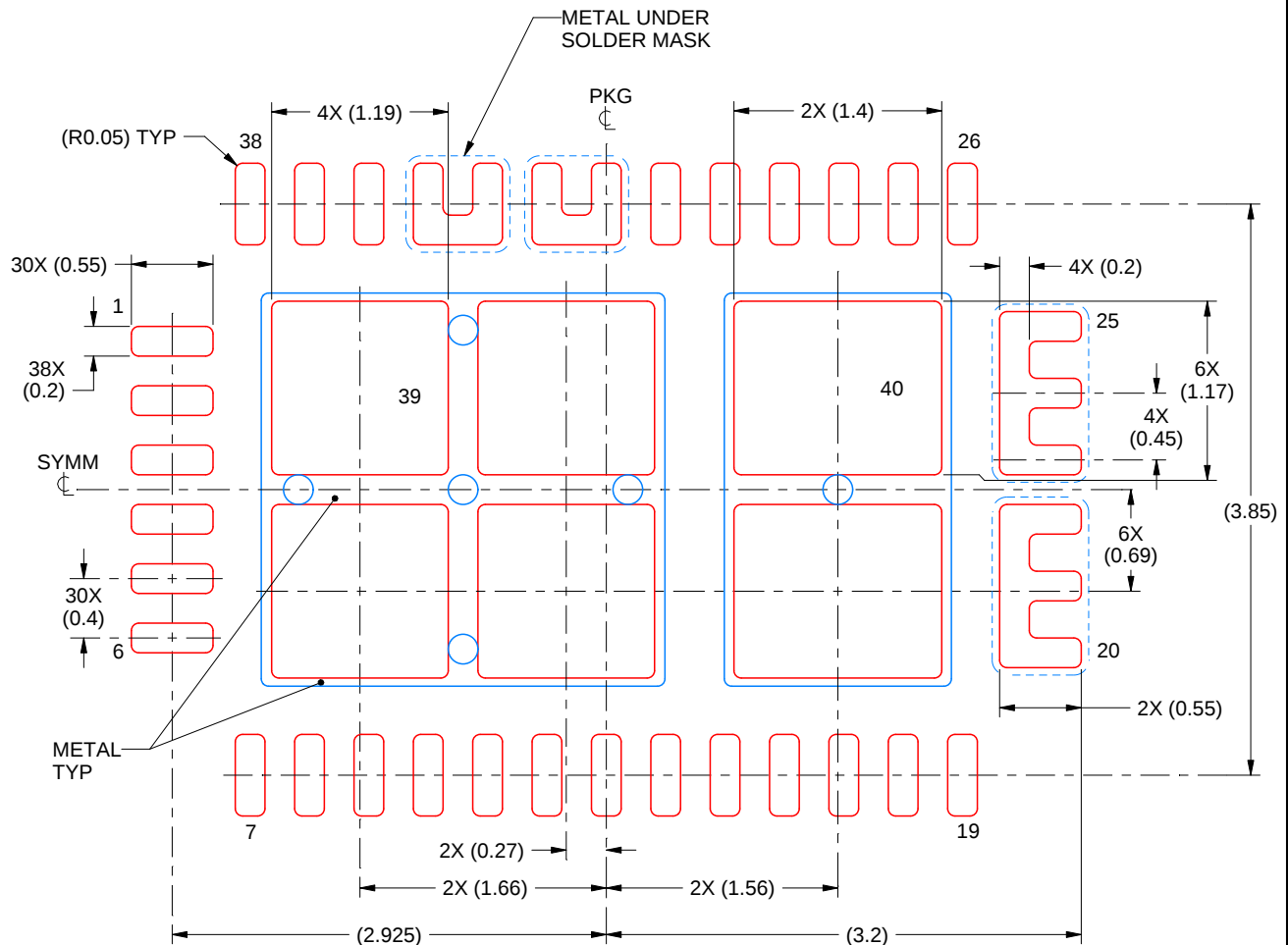
- This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

REF0038A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 39
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

EXPOSED PADS 40
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

SCALE:20X

4226763/C 11/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

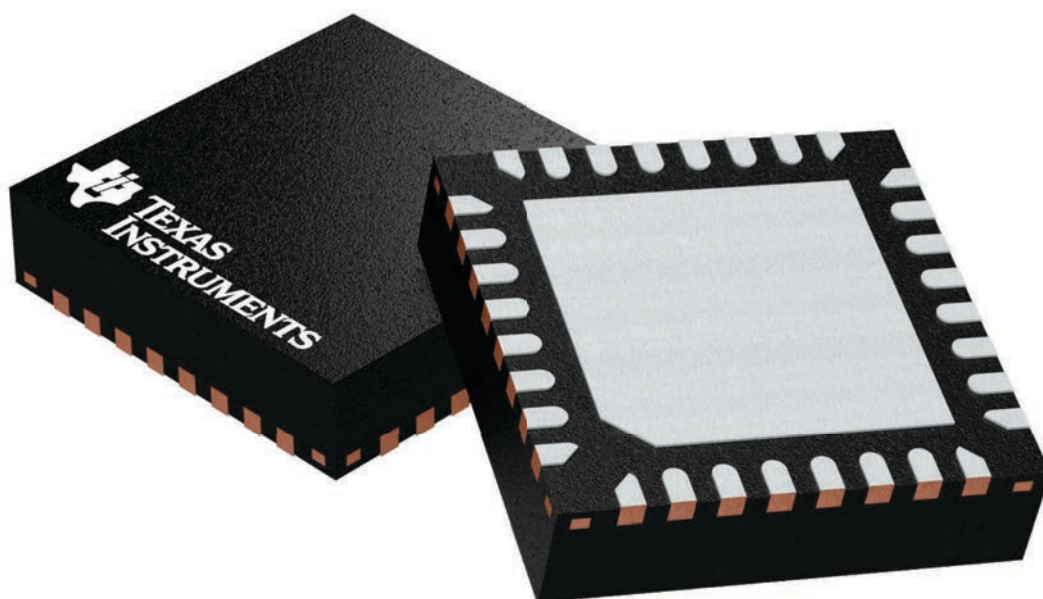
RSM 32

VQFN - 1 mm max height

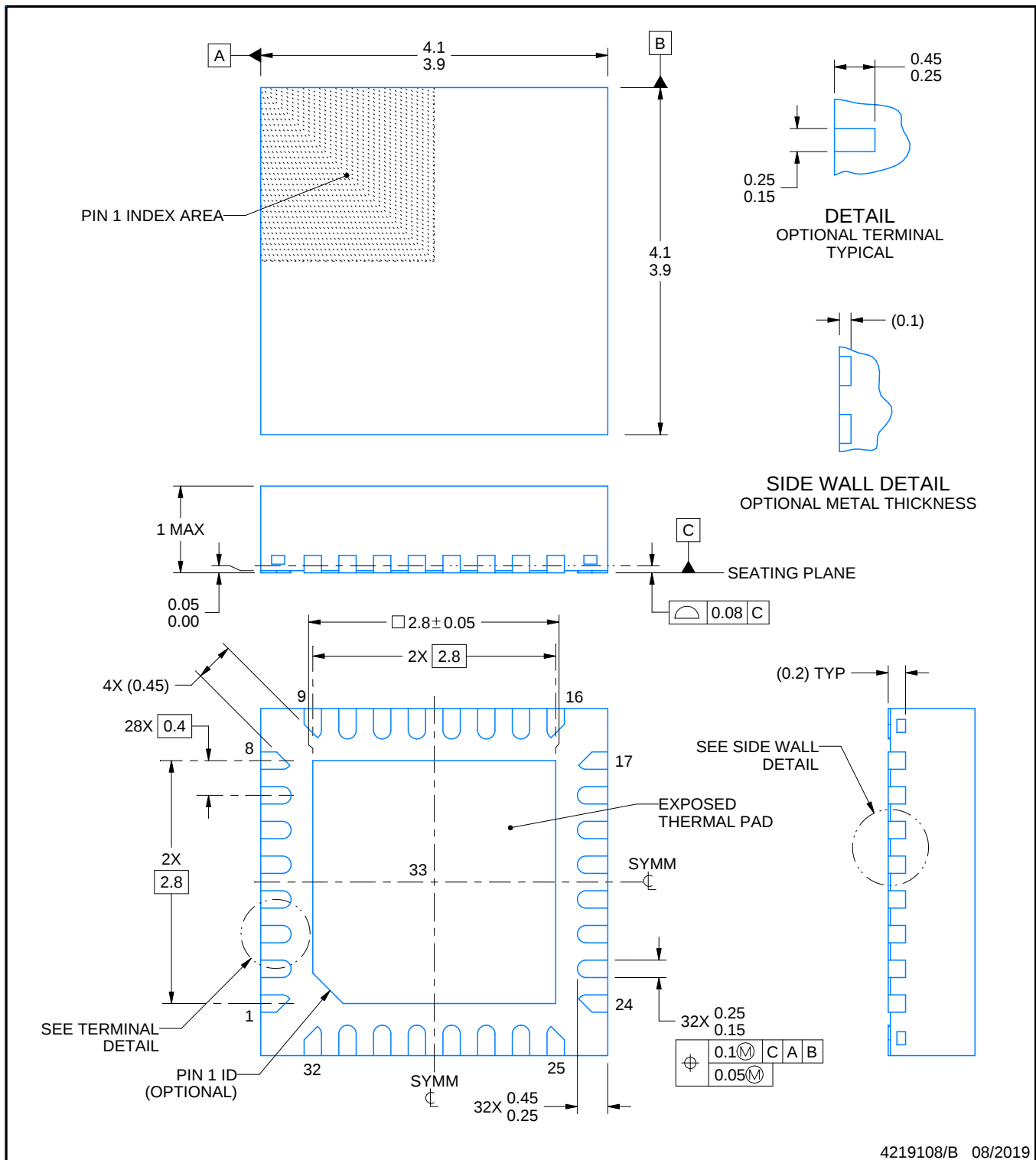
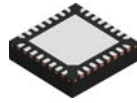
4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224982/A



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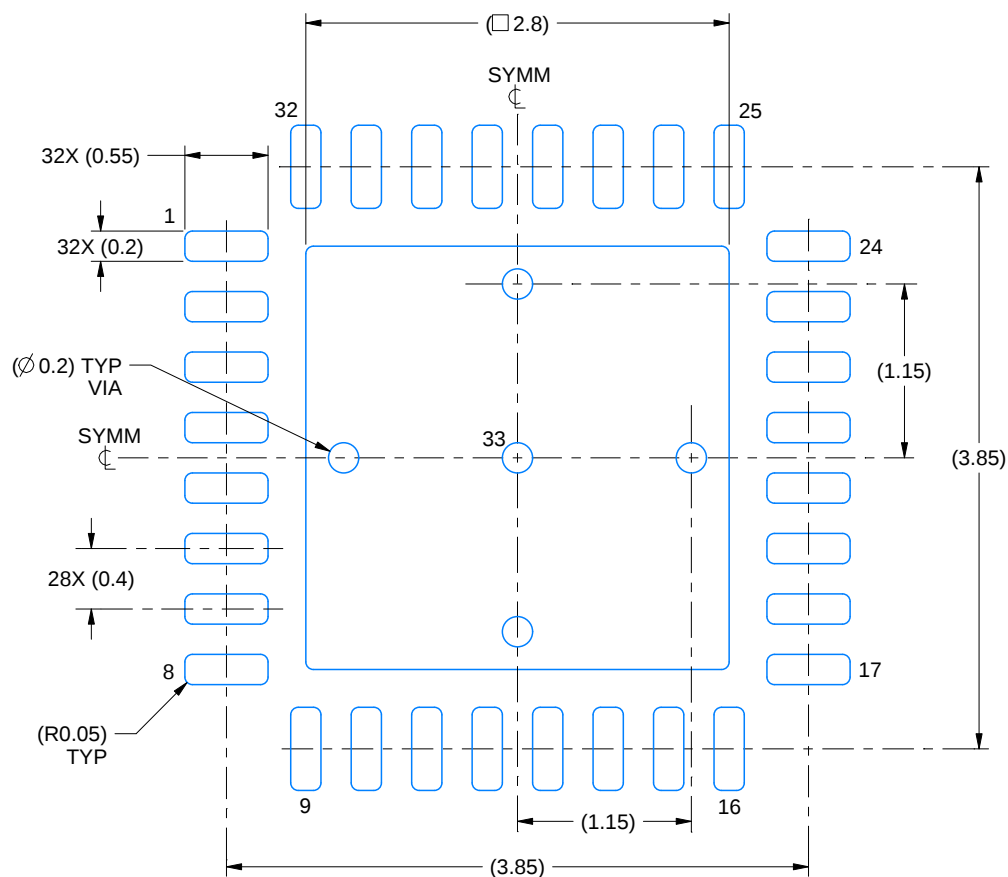
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

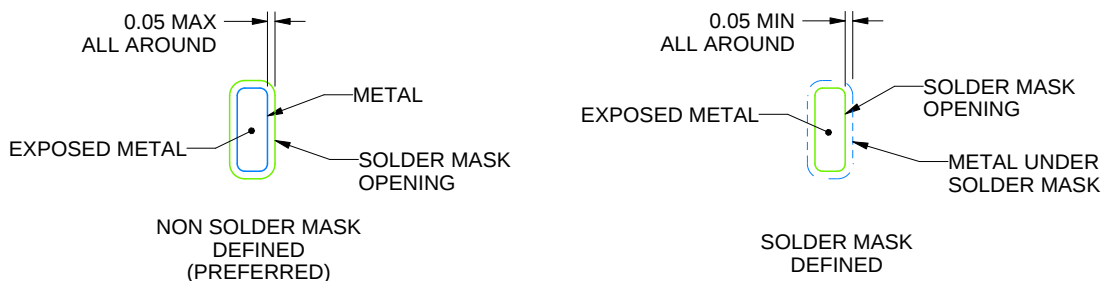
RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

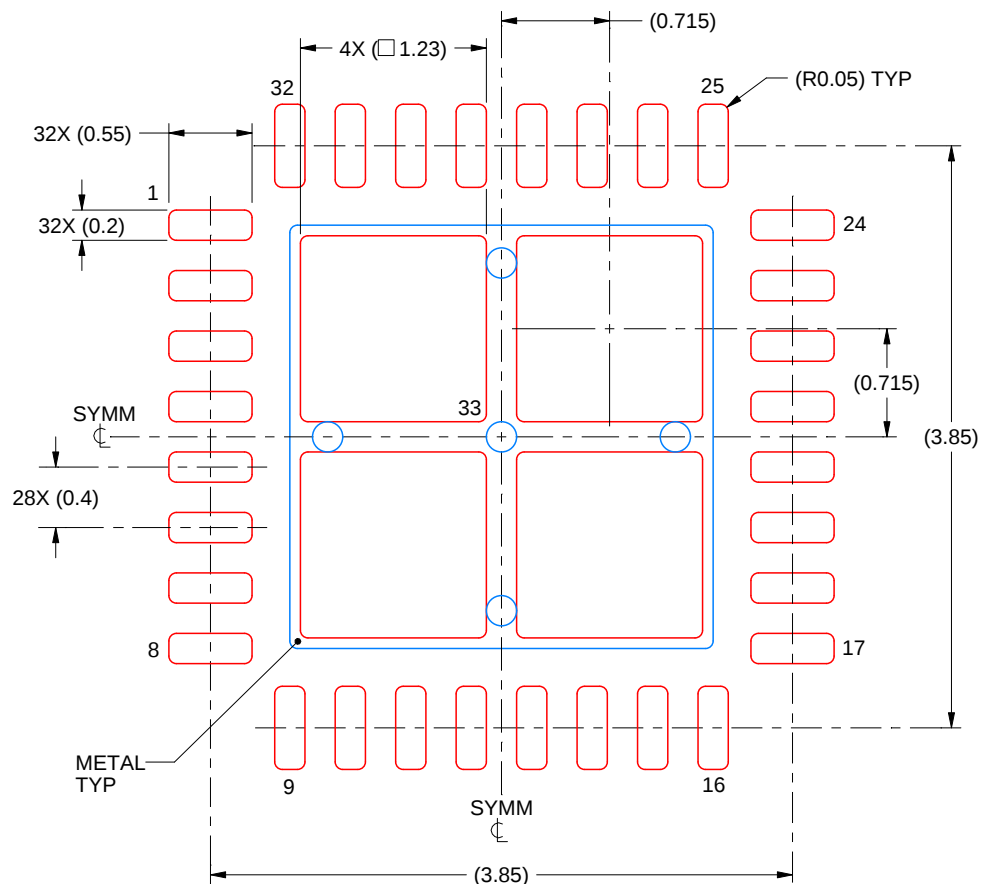
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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