TPS371K-Q1 Automotive 1500V Window (OV and UV) Supervisor with Integrated Buffer for 400V and 800V DC-Link Voltage Measurements

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C
- Functional Safety-Compliant Targeted (Preview)
  - Development targeted for functional safety applications
  - Documentation to aid ISO 26262 system design
- Overvoltage and undervoltage fault monitor for 400V & 800V BMS and DC-Link
  - 1% overvoltage and undervoltage outputs
  - Fast detection time (<5µs) to help minimize system fault tolerant time interval
  - 30V to 60V Low UV output
- Device flexibility to meet design requirements
  - User selectable adjustable overvoltage and undervoltage thresholds
  - User programmable capacitor-based glitch rejection and deassertion delay
- Integrated buffer for ADC monitoring
  - High accuracy 0.35% (maximum) scaled down voltage of sense pin
  - VSENSE pin can directly drive high-speed ADC inputs
- Designed for safety applications (Preview)
  - Output latching feature to help bring system to safe state
  - Built-In Self-Test to monitor device functionality and enhance system protection

2 Applications

- High-voltage battery system
- Traction inverter
- Integrated high voltage (OBC & DC/DC)
- DC/DC converter system

3 Description

TPS371K-Q1 is an automotive supervisor for voltage monitoring with an integrated buffer for 400V and 800V DC-link voltage measurements. The TPS371K-Q1 eliminates large resistor ladders with the integrated high voltage ladder. This device's SENSE pin can be directly connected to 400V or 800V automotive battery systems and DC-Link for continuous monitoring of overvoltage (OV), undervoltage (UV), and low undervoltage (LUV) conditions. The TPS371K-Q1 offers CTS for programmable glitch rejection for noisy environments.

The TPS371K-Q1 has a integrated high-speed buffer VSENSE for supply voltage measurements. The buffer has a low output impedance which can directly drive ADC inputs. VSENSE is a scaled down voltage of the SENSE pin input.

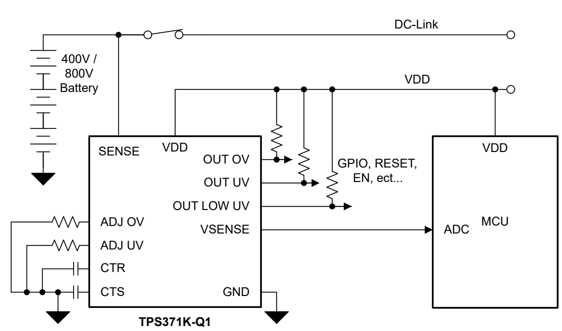
The combination of voltage supervisor and integrated buffer allows for the smallest signal chain size for direct monitoring of 400V and 800V systems. This combination also allows for redundant digital and analog always on voltage fault monitoring.

The TPS371K-Q1 is available in a 12.8mm × 7.4mm SOIC 15-pin package. TPS371K-Q1 operates over -40°C to +125°C T_A.

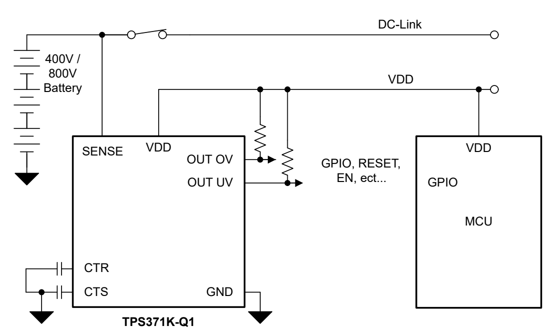
Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TPS371K-Q1	SOIC (15) (DFX)	12.8mm × 7.4mm

(1) For package details, see the mechanical drawing addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit Adjustable Version



Typical Application Circuit Fixed Version

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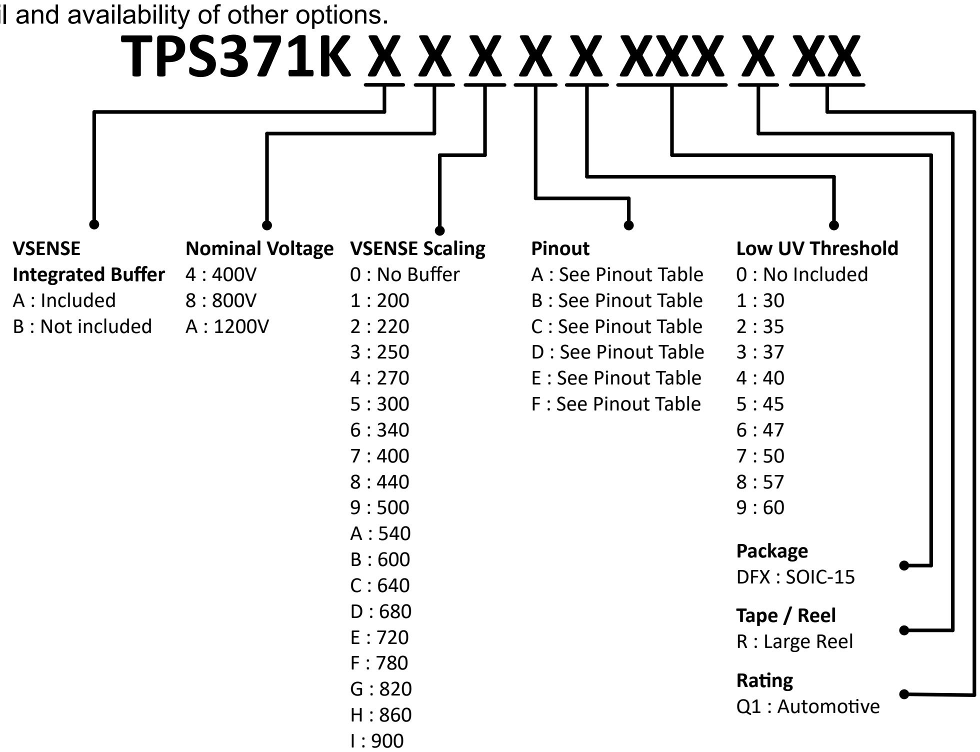
4 Device Comparison

Device Decoder shows some of the device naming nomenclature of the TPS371K-Q1 adjustable option. Not all device namings follow this nomenclature table. For a detailed breakdown of every adjustable and fixed voltage threshold variant see Device Nomenclature for more details. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options.



1. Not all TPS371K-Q1 devices can be decoded by this table. Refer to Device Nomenclature for a decoding table by part number and for fixed threshold variants.
2. For 400V TPS371K-Q1, the undervoltage threshold can be between 180V to 300V and overvoltage can be between 440V to 540V.
3. For 800V TPS371K-Q1, the undervoltage threshold can be between 360V to 600V and overvoltage can be between 860V to 1080V.
4. For 1200V TPS371K-Q1, the undervoltage threshold can be between 540V to 900V and overvoltage can be between 1290V to 1500V.

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5 Pin Configuration and Functions

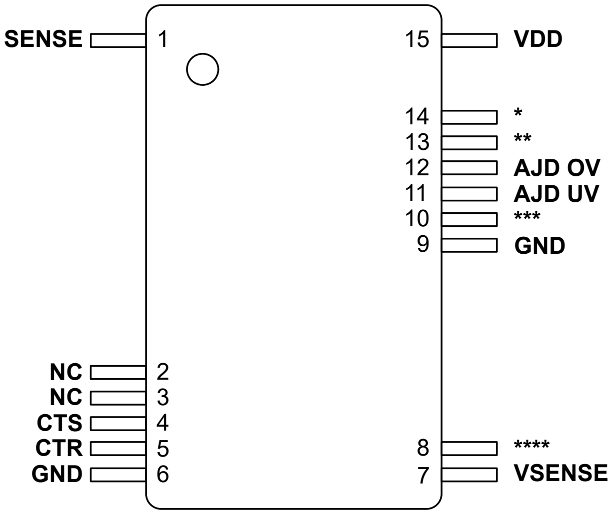

Figure 5-1. DFX Package, 15-Pin SOIC, TPS371KA-Q1 Adjustable Version (Top View)

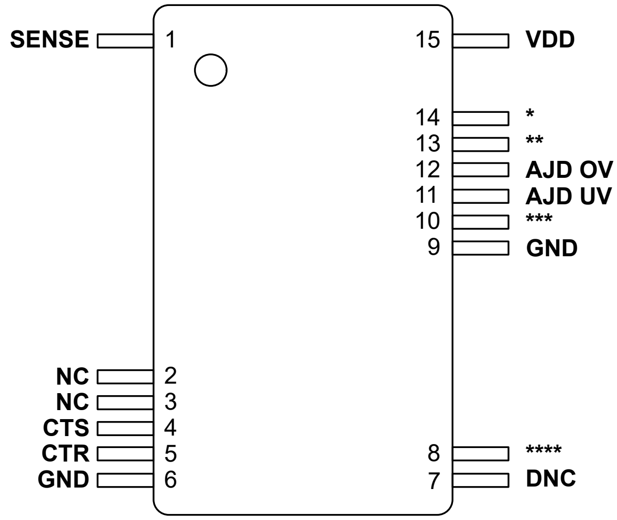

Figure 5-2. DFX Package, 15-Pin SOIC, TPS371KB-Q1 Adjustable Version (Top View)

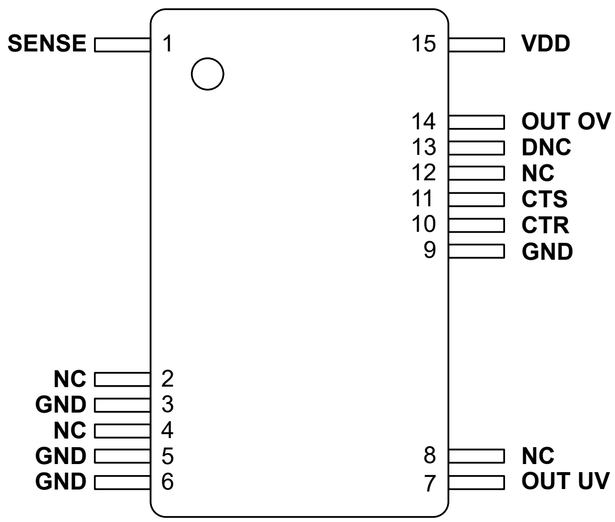

Figure 5-3. DFX Package, 15-Pin SOIC, TPS371K -Q1 Fixed Version (Top View)

Table 5-1. Pinout Table

OPN Pinout	Pin 8****	Pin 10 ***	Pin 13 **	Pin 14 *
A	BIST EN	BIST	OUT UV	OUT OV
B	NC	NC	OUT UV	OUT OV
C	BIST EN	LOW UV & BIST	OUT UV	OUT OV
D	NC	LOW UV	OUT UV	OUT OV
E	BIST EN	BIST	LOW UV	OUT OV
F	NC	NC	LOW UV	OUT OV

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Table 5-2. Pin Functions

PIN				I/O	DESCRIPTION
NAME	TPS371 KANO.	TPS371 KBNO.	TPS371 K Fixed NO.		
SENSE	1	1	1	I	**Sense Voltage:** Connect this pin to the voltage rail that must be monitored.
GND	4, 7	4, 7	4,5,6,9	-	**Ground.** All GND pins must be electrically connected to the board ground.
CTR	5	5	10	O	**Release Time Delay:** User-programmable release time delay for output pins. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Device Nomenclature table for output pin configurations.
CTS	6	6	11	O	**SENSE Time Delay:** User-programmable sense time delay for SENSE. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Device Nomenclature table for output pin configurations.
VSENSE	9	-	-	O	**Voltage SENSE**: The output of the integrated buffer that is a scaled down voltage of the SENSE pin. See Device Nomenclature table for output pin configurations.
ADJ UV	11	11	-	I	**Adjustable Undervoltage Threshold**: User can program the internal undervoltage thresholds by using external resistors to set a voltage at start-up. See voltage threshold table for selectable threshold options.
ADJ OV	12	12	-	I	**Adjustable Overvoltage Threshold**: User can program the internal overvoltage threshold by using external resistors to set a voltage at start-up. See voltage threshold table for selectable threshold options.
OUT UV	See Pinout Table	See Pinout Table	7	O	**Output Undervoltage Signal:** OUT UV asserts when SENSE crosses the undervoltage threshold. Assertion time delay is either fixed or set by CTS. OUT UV remains asserted for the release time delay period after SENSE transitions out of a fault condition. The active low open-drain release output requires an external pullup resistor. See Device Nomenclature table for OUT UV threshold and timing configurations. Output topology: **Open-Drain Active-Low**
OUT OV	See Pinout Table	See Pinout Table	14	O	**Output Overvoltage Signal:** OUT OV asserts when SENSE crosses the Overvoltage threshold. Assertion time delay is either fixed or set by CTS. OUT OV remains asserted for the release time delay period after SENSE transitions out of a fault condition. The active low open-drain release output requires an external pullup resistor. See Device Nomenclature table for OUT OV threshold and timing configurations. Output topology: **Open-Drain Active-Low**
LOW UV	See Pinout Table	See Pinout Table	-	O	**Output Low Undervoltage Signal:** OUT Low UV asserts when SENSE crosses the Low Overvoltage threshold after the sense time delay, set by CTS. OUT Low UV remains asserted for the release time delay period after SENSE transitions out of a fault condition. The active low open-drain release output requires an external pullup resistor. Output topology: **Open-Drain Active-Low**
BIST	See Pinout Table	See Pinout Table	-	O	**Output Built-in Self-test (BIST):** BIST asserts when BIST is in operation. BIST operation is initiated at device start-up and by a rising edge on BIST_EN pin. BIST is a device diagnostic test that checks for internal failures. If there is a failure, BIST stays asserted. Upon successful BIST, BIST pin de-asserts. Output topology: **Open-Drain Active-Low**
BIST_EN	See Pinout Table	See Pinout Table	-	I	**Built-in Self-test Enable (BIST EN):** A rising edge on BIST enable pin initiates the BIST. For variants with latch, BIST EN also enables and disables latch.
VDD	15	15	15	I	**Input Supply Voltage:** Supply voltage pin. Bypass with a 0.1µF capacitor to GND for noisy environments.

Table 5-2. Pin Functions (continued)

PIN				I/O	DESCRIPTION
NAME	TPS371 KANO.	TPS371 KBNO.	TPS371 K Fixed NO.		
NC	2, 3, 8	2, 3, 8	2, 4, 8, 12	-	**No Connect:** Leave pins floating or connect to GND.
DNC	-	7	13	-	**Do Not Connect:** Leave pins floating for proper operation.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted [(1)]

		MIN	MAX	UNIT
Voltage	V_{SENSE}	–0.3	1500	V
Voltage	V_{DD}, V_{OUTOV}, V_{OUTUV}, V_{LOWUV}, V_{VSENSE}, V_{ADJOV}, V_{ADJUV}, V_{CTS}, V_{CTR}, V_{BIST}, V_{BIST_EN}	–0.3	6	V
Current	I_{OUTOV}, I_{OUTUV}, I_{LOWUV}, I_{BIST}		10	mA
Temperature	Operating junction temperature, T_J	–40	150	°C
Temperature	Operating Ambient temperature, T_A	–40	150	°C
Temperature	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 [(1)]	2000	V
		Charged device model (CDM), per AEC Q100-011	750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	V_{SENSE}	0		1500	V
Voltage	V_{DD}, V_{OUTOV}, V_{OUTUV}, V_{LOWUV}, V_{VSENSE}, V_{ADJOV}, V_{ADJUV}, V_{CTS}, V_{CTR}, V_{BIST}, V_{BIST_EN}	0		5.5	V
Current	I_{OUTOV}, I_{OUTUV}, I_{LOWUV}, I_{BIST}	0		5	mA
T_J	Junction temperature (free air temperature)	–40		125	°C

6.4 Thermal Information

THERMAL METRIC [(1)]		TPS371K-Q1	UNIT
		DFX	
		15-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD\ (MAX)}$, CTR = CTS = open, R_{Pullup} = 10 kΩ, $V_{Pullup} = V_{DD}$, C_L = 10 pF. Minimum and maximum specifications at T_A = – 40°C to 125°C, typical values are at T_A = 25°C and V_{DD} = 3.3 V. VSENSE = Nominal voltage / Scale factor. Nominal voltage = 400V, 800V, 1.2kV; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD						
V_{DD}	Supply Voltage(1)		2.7		5.5	V
UVLO	Undervoltage Lockout	V_{DD} rising above $V_{DD\ (MIN)}$			2.7	V
UVLO	Undervoltage Lockout	V_{DD} falling below $V_{DD\ (MIN)}$			2.65	V
V_{POROV}	Power on Reset Voltage (2) OUT OV Active Low (Open-Drain)	$V_{OUTOV(MAX)}$ = 300 mV $I_{OUT\ (Sink)}$ = 15 µA			0.7	V
V_{PORUV}	Power on Reset Voltage (2) OUT UV Active Low (Open-Drain)	$V_{OUTUV(MAX)}$ = 300 mV $I_{OUT\ (Sink)}$ = 15 µA			0.7	V
$V_{PORBIST}$	Power on Reset Voltage (2) BIST Active Low (Open-Drain)	$V_{BIST(MAX)}$ = 300 mV $I_{OUT\ (Sink)}$ = 15 µA			0.7	V
$V_{PORLOWUV}$	Power on Reset Voltage (2) LOW UV Active Low (Open-Drain)	$V_{LOWUV(MAX)}$ = 300 mV $I_{OUT\ (Sink)}$ = 15 µA			0.7	V
I_{DD}	Supply current into VDD pin	$V_{DD\ (MIN)} \leq V_{DD} \leq V_{DD\ (MAX)}$ VSENSE included		700	850	µA
I_{DD}	Supply current into VDD pin	$V_{DD\ (MIN)} \leq V_{DD} \leq V_{DD\ (MAX)}$ VSENSE not included		40	50	µA
SENSE (Input)						
R_{SENSE}	Internal resistance (RSENSE)			50		Mohm
V_{ITN}	Input Threshold Negative for OUT UV (Undervoltage)	VTH = ADJ	-1		1	%
V_{ITP}	Input Threshold Positive for OUT OV (Overvoltage)	VTH = ADJ	-1		1	%
V_{ITLN}	Input Threshold Negative for LOW UV (Undervoltage)	400V Variant VTH = 30V to 60V	-2		2	%
V_{ITLN}	Input Threshold Negative for LOW UV (Undervoltage)	800V Variant VTH = 30V to 60V	-3		3	%
V_{ITLN}	Input Threshold Negative for LOW UV (Undervoltage)	1.2kV Variant VTH = 30V to 60V	-4		4	%
V_{HYS}	Hysteresis Accuracy for OUT UV, OUT OV (3)	V_{HYS} = VTH * 2.5% Vth = Fixed	2	2.5	3	%
V_{HYS}	Hysteresis Accuracy for OUT UV, OUT OV (3)	V_{HYS} = Nominal * 2.5% Vth = ADJ	2	2.5	3	%
V_{HYS}	Hysteresis Accuracy for LOW UV (3)	Nominal = 400V $V_{THLOWUV}$ = 30V - 60V	1.5	3	5	V
V_{HYS}	Hysteresis Accuracy for LOW UV (3)	Nominal = 800V $V_{THLOWUV}$ = 30V - 60V	3	6	9	V
V_{HYS}	Hysteresis Accuracy for LOW UV (3)	Nominal = 1200V $V_{THLOWUV}$ = 30V - 60V	5	9	13	V
OUT OV, OUT UV, LOW UV (Output)						
I_{lkg_OV}	Open-Drain leakage	V_{OUTOV} = 5.5 V $V_{SENSE} < V_{ITP}$		5	300	nA

6.5 Electrical Characteristics (continued)

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD\ (MAX)}$, CTR = CTS = open, R_{Pullup} = 10 kΩ, $V_{Pullup} = V_{DD}$, C_L = 10 pF. Minimum and maximum specifications at T_A = – 40°C to 125°C, typical values are at T_A = 25°C and V_{DD} = 3.3 V. VSENSE = Nominal voltage / Scale factor. Nominal voltage = 400V, 800V, 1.2kV; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{lkg_UV}	Open-Drain leakage	V_{OUTUV} = 5.5 V $V_{ITN} < V_{SENSE}$		5	300	nA
I_{lkg_LOWUV}	Open-Drain leakage	V_{LOWUV} = 5.5 V $V_{ITN} < V_{SENSE}$		5	300	nA
V_{OL_OV} (4)	Low level output voltage	2.7 V ≤ VDD ≤ 5.5 V I_{OUTOV} = 2.7 mA			300	mV
V_{OL_UV} (4)	Low level output voltage	2.7 V ≤ VDD ≤ 5.5 V I_{OUTUV} = 2.7 mA			300	mV
V_{OL_LOWUV} (4)	Low level output voltage	2.7 V ≤ VDD ≤ 5.5 V I_{LOWUV} = 2.7 mA			300	mV

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6.5 Electrical Characteristics (continued)

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR = CTS = open, R_{Pullup} = 10 kΩ, $V_{Pullup} = V_{DD}$, C_L = 10 pF. Minimum and maximum specifications at T_A = – 40°C to 125°C, typical values are at T_A = 25°C and V_{DD} = 3.3 V. VSENSE = Nominal voltage / Scale factor. Nominal voltage = 400V, 800V, 1.2kV; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Capacitor Timing (CTS, CTR)						
R_{CTR}	Internal resistance (CTR)			3600		Kohm
R_{CTS}	Internal resistance (CTS)			3600		Kohm
VSENSE						
I_{SC}	Short-circuit current			57		mA
V_{DO_VDD}	Voltage output drop out from VDD	Iout = 1mA sink. shorted to VDD Measure drop out between VDD and AOUT. SENSE = VDD * Scale factor For Scale factor ≤ 220 for 400V variant For Scale factor ≤ 440 for 800V variant			40	mV
V_{DO_VDD}	Voltage output drop out from VDD	Iout = 1mA sink. shorted to VDD Measure drop out between VDD and AOUT. SENSE = VDD * Scale factor For Scale factor > 220 for 400V variant For Scale factor > 440 for 800V variant			800	mV
V_{DO_GND}	Voltage output drop out from GND	Iout = 1mA source. shorted to GND Measure drop out between GND and AOUT. AOUT = GND. VDD = MIN / MAX VDD (any gain)			40	mV
	Scale factor accuracy over Temp	I_{OUT} = 0 µA, T_A = -40℃ to 125℃ +/- 30% from nominal Variants = 400V, 800V	-0.35		0.35	%
	Scale factor accuracy over Temp	I_{OUT} = 0 µA, T_A = -40℃ to 125℃ +/- 50% from nominal Variants = 400V, 800V, 1200V	-0.5		0.5	%
	Line Regulation	VDD = 2.7V to 5.5V	-0.15		0.15	%
	Load Regulation (source)	Iload = 0mA to 1mA			0.01	%/µA
	Load Regulation (sink)	Iload = 0mA to -1mA			0.01	%/µA
	Stability	Maximum load cap for stability		100		pF
Built-in Self-test						
$I_{lkg(BIST\_OD)}$	Open-Drain leakage	V_{BIST} = 5.5 V $V_{ITN} < V_{SENSE} < V_{ITP}$			500	nA
V_{BIST_OL}	Low level output voltage	2.7 V ≤ VDD ≤ 5.5 V I_{BIST} = 5 mA			300	mV
V_{BIST_EN}	BIST_EN pin logic low input				500	mV
V_{BIST_EN}	BIST_EN pin logic high input		1300			mV

6.5 Electrical Characteristics (continued)

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR = CTS = open, R_{Pullup} = 10 kΩ, $V_{Pullup} = V_{DD}$, C_L = 10 pF. Minimum and maximum specifications at T_A = – 40°C to 125°C, typical values are at T_A = 25°C and V_{DD} = 3.3 V. VSENSE = Nominal voltage / Scale factor. Nominal voltage = 400V, 800V, 1.2kV; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ADJ}	Maximum external capacitance on ADJ UV & ADJ OV				1	nF

(1) V_{DD} slew rate ≤ 0.1 V/µs
(2) V_{POR} is the minimum V_{DD} voltage for a controlled output state. Below VPOR, the output cannot be determined
(3) Hysteresis is with respect to V_{ITP}, V_{ITN}, V_{ITLN} voltage threshold. V_{ITP} has negative hysteresis. V_{ITN} and V_{ITLN} has positive hysteresis.
(4) For V_{OH} and V_{OL} relation to output variants refer to **Timing Figures after the Timing Requirement Table**

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6.6 Switching Requirements

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD\ (MAX)}$, CTR = CTS = open, R_{Pullup} = 10 kΩ, $V_{Pullup} = V_{DD}$, C_L = 10 pF. Minimum and maximum specifications at T_A = – 40°C to 125°C, typical values are at T_A = 25°C and V_{DD} = 3.3 V. VSENSE = Nominal voltage / Scale factor. Nominal voltage = 400V, 800V, 1.2kV; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT OV						
t_{pdHL_OV}	OUT OV propagation delay	4% Overdrive (1)		7		µs
t_{FDHL_OV}	OUT OV fixed time delay	Fixed Time delay = 150us		150		µs
t_{FDHL_OV}	OUT OV fixed time delay	Fixed Time delay = 1ms		1		ms
t_{pdLH_OV}	OUT OV propagation release time delay			40		µs
t_{FDLH_OV}	OUT OV fixed release time delay	Fixed Time delay = 1ms		1		ms
t_{FDLH_OV}	OUT OV fixed release time delay	Fixed Time delay = 10ms		10		ms
t_{FDLH_OV}	OUT OV fixed release time delay	Fixed Time delay = 200ms		200		ms
OUT UV						
t_{pdHL_UV}	OUT UV propagation delay	4% Overdrive (1) CTS disabled		7		µs
t_{CTS_UV}	OUT UV capacitor time delay (CTS)	4% Overdrive (1) CTS = Open		100		µs
t_{pdLH_UV}	OUT UV propagation release time delay	CTR = Disabled		40		µs
t_{CTR_UV}	OUT UV capacitor release time delay (CTR)	C_{CTR} = Open		350		µs
Low UV						
t_{pdHL_LUV}	Low UV propagation delay Pin Out Pinout C, D	10% Overdrive (1)		9	12	µs
t_{pdHL_LUV}	Low UV propagation delay Pinout E, F	10% Overdrive (1) CTS disabled		7	14	µs
t_{CTS_LUV}	Low UV propagation delay Pinout E, F	10% Overdrive (1) C_{CTS} = Open		150		µs
t_{pdLH_LUV}	Low UV propagation release time delay Pinout C, D			18	27	µs
t_{pdLH_LUV}	Low UV propagation release time delay Pinout E, F	C_{CTR} = Disabled		40	60	µs
t_{CTS_LUV}	Low UV propagation delay Pinout E, F	C_{CTR} = Open		350		µs
Common Switching Requirements						
t_{SD}	Supervisor startup delay			1.8		ms
LATCH Switching Requirements						
$t_{latch\_recover}$	Rising edge of BIST_en to output valid	C_{CTR} = Open, BIST = Disabled		10		µs
BIST Switching Requirements						
$t_{BIST\_en\_pd}$	Rising edge of BIST_EN to BIST asserting			5		µs

6.6 Switching Requirements (continued)

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD\ (MAX)}$, CTR = CTS = open, R_{Pullup} = 10 kΩ, $V_{Pullup} = V_{DD}$, C_L = 10 pF. Minimum and maximum specifications at T_A = – 40°C to 125°C, typical values are at T_A = 25°C and V_{DD} = 3.3 V. VSENSE = Nominal voltage / Scale factor. Nominal voltage = 400V, 800V, 1.2kV; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{BIST\_en\_out}$	Rising edge of BIST_EN to OUT OV, OUT UV asserting			5		µs
$t_{BIST\_recover}$	Rising edge of BIST to SENSE input valid	C_{CTR} = Open, BIST = Enabled		350	600	µs
t_{BIST}	BIST run time			2.8		ms
$t_{SD+BIST}$	Supervisor startup delay with BIST enabled			3.3		ms
VSENSE						
T_{VSSD}	VSENSE Startup Delay	To 1% Iout = 100uA, Vout = 2V.		8		µs

(1) Overdrive % = [(V_{SENSE}/ V_{IT}) - 1] × 100%, V_{IT} refers to either V_{ITN}, V_{ITLN}, or V_{ITP}

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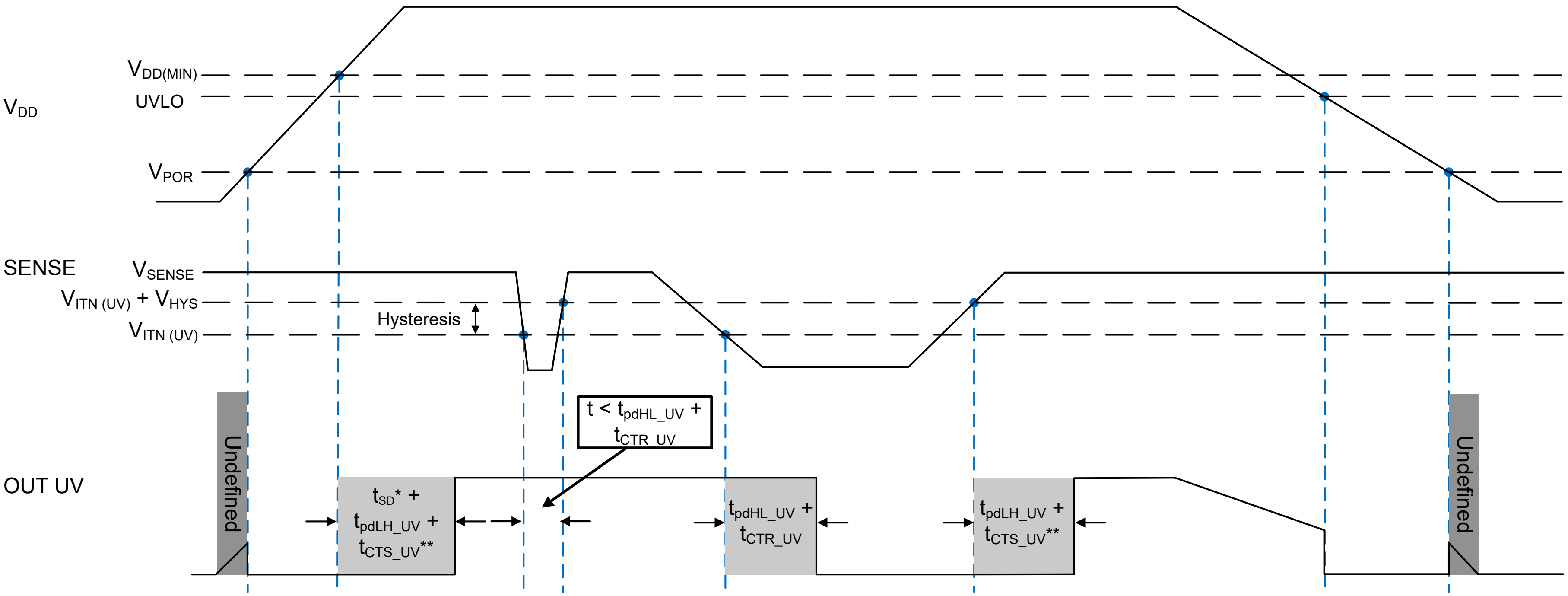
6.7 Timing Requirements

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD\ (MAX)}$, CTR = CTS = open, R_{Pullup} = 10kΩ, $V_{Pullup} = V_{DD}$, C_L = 10pF. Minimum and maximum specifications at T_A = – 40°C to 125°C, typical values are at T_A = 25°C and V_{DD} = 3.3 V. VSENSE = Nominal voltage / Scale factor. Nominal voltage = 400V, 800V, 1.2kV; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common timing parameters						
BIST timing parameters						
$t_{BIST\_en\ Glitch}$	BIST_EN Glitch immunity			5		µs
t_{BIST_en}	Minimum BIST_EN input width to initate BIST			4.5	5	µs
LATCH timing parameters						
$t_{Latch\ Glitch}$	Latch Glitch immunity			4.3		µs
t_{Latch_clr}	Latch input width to clear latch			5.3		µs

6.8 Timing Diagrams



A. The timing diagram assumes the open-drain output OUT UV pin is connected via an external pull-up resistor to V_{Pullup}.

B. *Use $t_{SD+BIST}$ for variants with BIST.

C. **Use t_{CTS_UV} and t_{CTR_UV} for devices with t_{CTS_UV} and t_{CTR_UV} enabled.

Figure 6-1. SENSE Undervoltage (UV) Timing Diagram

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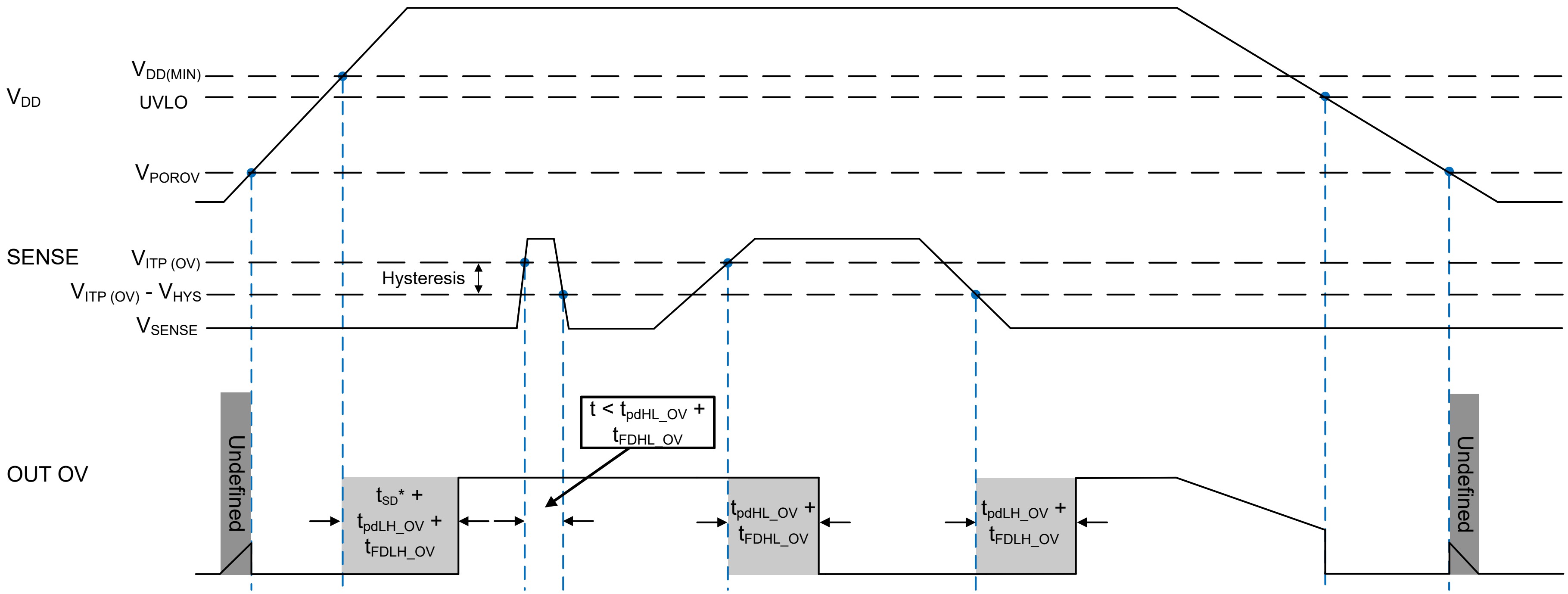
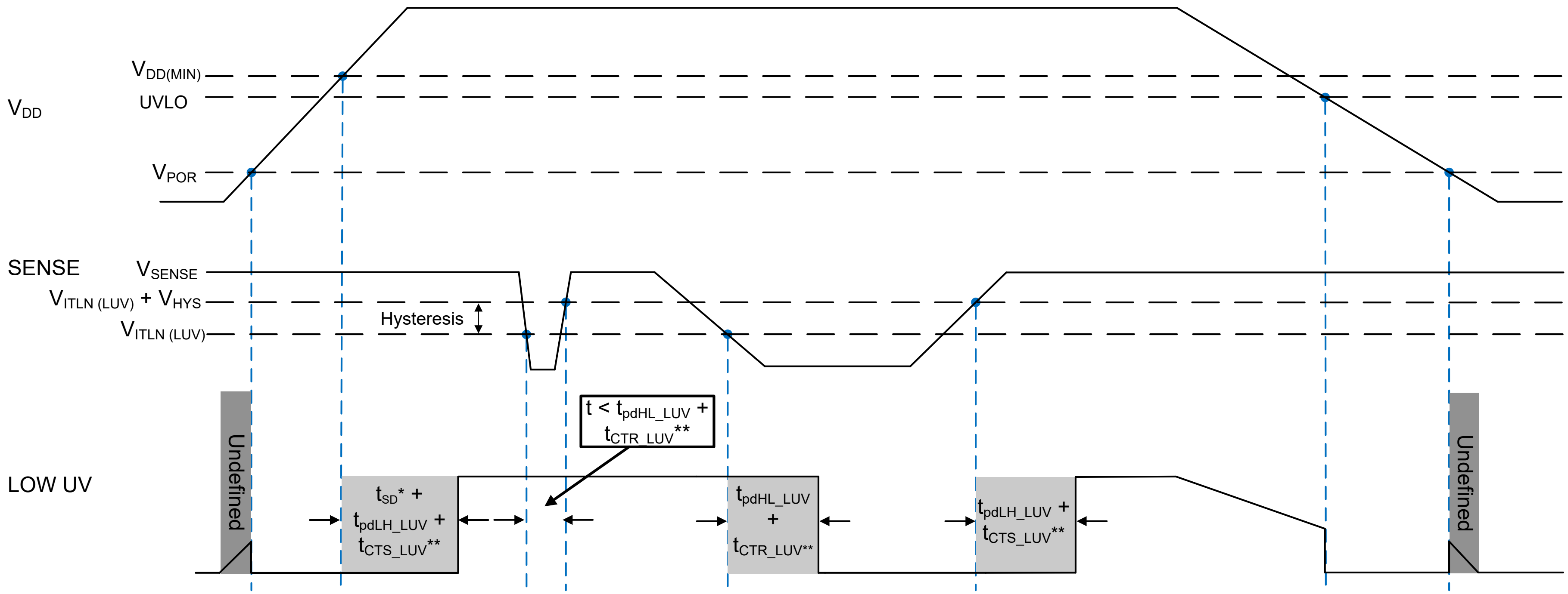


A. The timing diagram assumes the open-drain output OUT OV pin is connected via an external pull-up resistor to V_{Pullup}.

B. *Use $t_{SD+BIST}$ for variants with BIST.

C. ** Use t_{FDLH_OV} and t_{FDHL_OV} for devices with t_{FDLH_OV} and t_{FDHL_OV} are enabled..

Figure 6-2. SENSE Overvoltage (OV) Timing Diagram



A. The timing diagram assumes the open-drain output LOW UV pin is connected via an external pull-up resistor to V_{Pullup}.

B. *Use $t_{SD+BIST}$ for variants with BIST.

C. **Use t_{CTS_LUV} and t_{CTR_LUV} for devices with t_{CTS_LUV} and t_{CTR_LUV} are enabled.

Figure 6-3. SENSE Low Undervoltage (LUV) Timing Diagram

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6.9 Typical Characteristics

Typical characteristics show the typical performance of the TPS371K-Q1 device. Test conditions are taken at T_A = 25°C, unless otherwise noted.

V_{ITP} = 900V

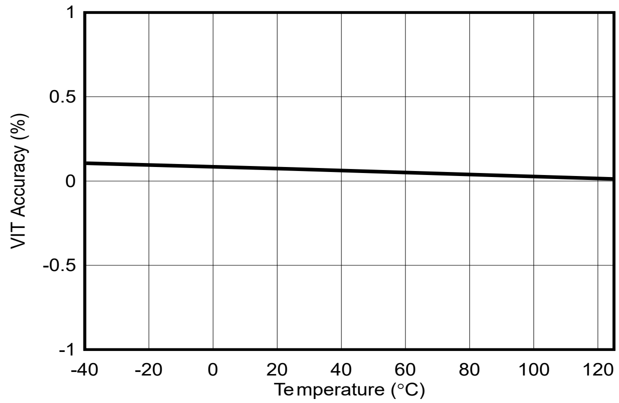


Figure 6-4. Overvoltage Accuracy vs Temperature

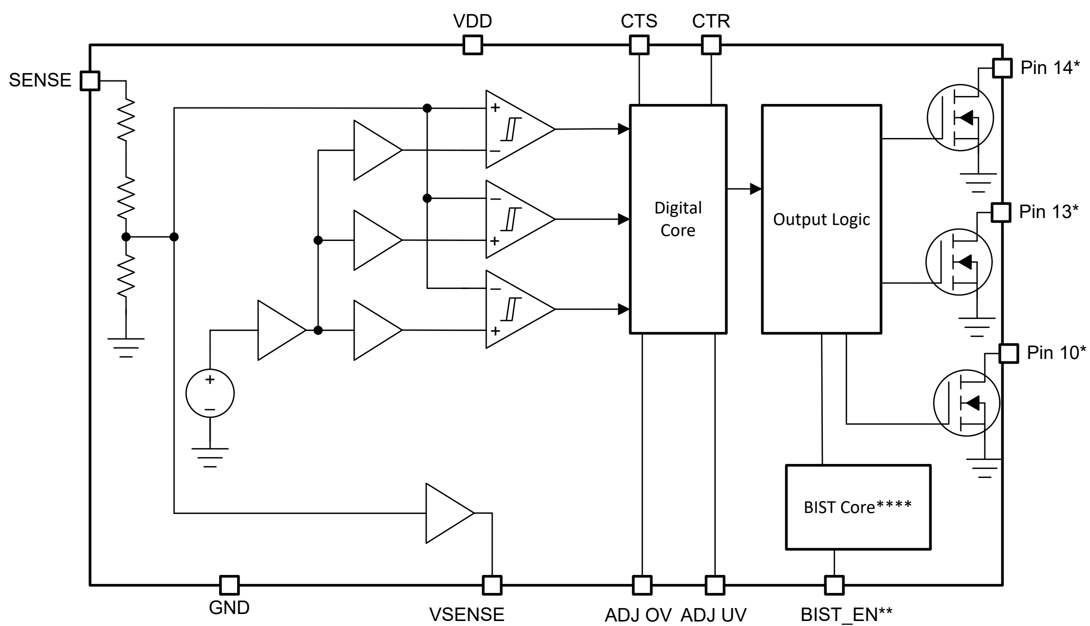
7 Detailed Description

7.1 Overview

The TPS371K-Q1 is a high voltage window (OV & UV) supervisor with and integrated buffer for 400V and 800V DC-Link Voltage Measurements. This device can be connected directly to 400V or 800V automotive battery systems and DC-Link for continuous monitoring of overvoltage (OV), undervoltage (UV) conditions, and low undervoltage (LUV) conditions.

The Overvoltage and Undervoltage thresholds are user selectable from a selection of 1% accuracy thresholds with the ADJ OV and ADJ UV pins. The low undervoltage threshold is OTP programmed and varies per orderable. When the SENSE voltage goes into a fault mode, the OUT OV, OUT UV, or LOW UV asserts. The TPS371K-Q1 has an integrated high-speed buffer for supply voltage measurements with the VSENSE pin. The buffer has a low output impedance which can directly drive ADC inputs and sufficient high-frequency for fast reaction time to minimize conversation error.

7.2 Functional Block Diagram



A. *Check Table 5-1 for pin functions.

B. **Only available in BIST variants.

Figure 7-1. Functional Block Diagram

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7.3 Feature Description

7.3.1 Input Voltage (V_{DD})

V_{DD} operating voltage ranges from 2.7V to 5.5V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1µF capacitor between the V_{DD} and GND for noisy environments.

V_{DD} needs to be at or above $V_{DD(MIN)}$ for at least the start-up time delay (t_{SD}) for the device to be fully functional.

V_{DD} voltage is independent of V_{SENSE}, V_{OUTOV}, V_{OUTUV}, and V_{LOWOV} meaning that VDD can be higher or lower than the other pins. This also means that V_{SENSE} can be connected while the device V_{DD} is not turned on. The V_{OUTOV}, V_{OUTUV}, and V_{LOWOV} are open drain pins that connect to a V_{Pullup} based on the load requirements.

7.3.1.1 Undervoltage Lockout (V_{POR} < V_{DD} < UVLO)

When the voltage on V_{DD} is less than the UVLO voltage, but greater than the power-on reset voltage (V_{POR}), the OUT OV, OUT UV, LOW UV, and BIST pins assert, regardless of the voltage at SENSE pins.

7.3.1.2 Power-On Reset (V_{DD} < V_{POR})

When the voltage on VDD is lower than the power on reset voltage (V_{POR}), the output signals (OUT OV, OUT UV, LOW UV, BIST) are undefined and are not to be relied upon for proper device function.

7.3.2 SENSE

The SENSE pin connects to the voltage rail that is to be monitored. The sense pin can be directly connected to 400V or 800V voltage rails. The SENSE pin is connected internall with a 50MΩ. Each TPS371K-Q1 is configured to monitor either overvoltage (OV), undervoltage (UV), low undervoltage (LOW UV), or a combination of the conditions based on the orderable. TPS371K-Q1 device offers built-in hysteresis that provides noise immunity and maintains stable operation.

7.3.2.1 SENSE Hysteresis

TPS371K-Q1 device offers built-in hysteresis around the UV, OV, LOW UV thresholds to avoid erroneous de-assertions. The hysteresis is opposite to the threshold voltage; for overvoltage options the hysteresis is subtracted from the positive threshold (V_{ITP}), for undervoltage options hysteresis is added to the negative threshold (V_{ITN}, V_{ITLN}).

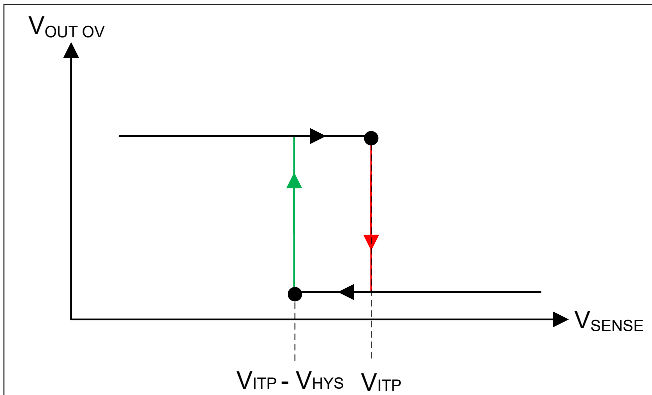

Figure 7-2. Overvoltage Hysteresis (V_{ITP})

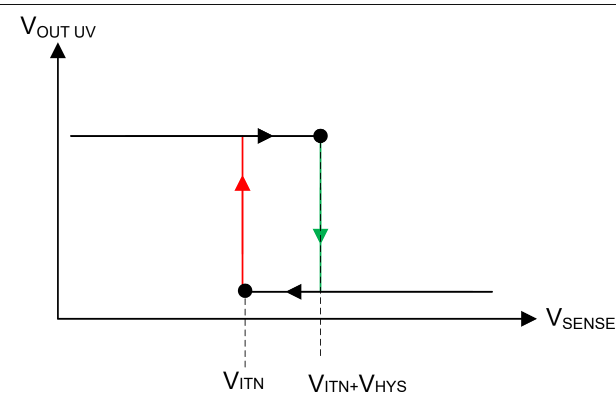

Figure 7-3. Undervoltage Hysteresis (V_{ITN})

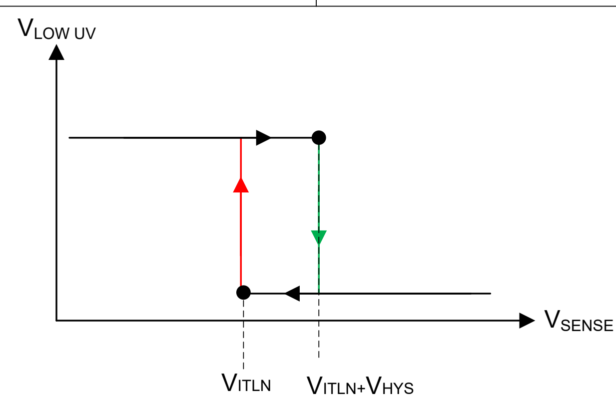

Figure 7-4. Low Undervoltage Hysteresis (V_{ITLN})

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7.3.3 Adjustable Voltage Thresholds

The TPS371K-Q1 has user adjustable thresholds for overvoltage and undervoltage. The thresholds are preselected based on the nominal voltage of the device variant and are selectable by using the ADJ OV and ADJ UV pins with external resistors R_{ADJOV} and R_{ADJUV}.

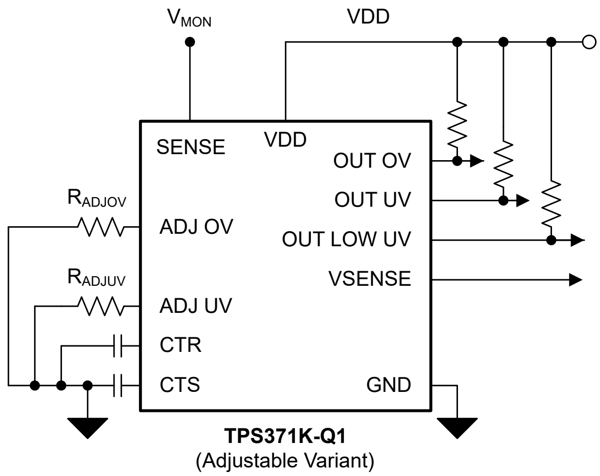

Figure 7-5. TPS371K-Q1 with External Resistors

Table 7-1. 400V Nominal TPS371K-Q1 Adjustable Thresholds

VOLTAGE THRESHOLD SETTING (V)		RESISTANCE TO VDD [kΩ]		
ADJ OV (V_{ITP})	ADJ UV (V_{ITN})	MIN	NOM	MAX
Disabled	Disabled	>150	>150	>150
430	300	61.2	68	74.8
435	290	35.1	39	42.9
440	280	19.8	22	24.2
445	270	10.8	12	13.2
450	260	6.12	6.8	7.48
455	250	3.51	3.9	4.29
460	240	<1.980	<1.980	<1.980

VOLTAGE THRESHOLD SETTING (V)		RESISTANCE TO GND [kΩ]		
ADJ OV (V_{ITP})	ADJ UV (V_{ITN})	MIN	NOM	MAX
500	160	>150	>150	>150
495	170	61.2	68	74.8
490	180	35.1	39	42.9
485	190	19.8	22	24.2
480	200	10.8	12	13.2
475	210	6.12	6.8	7.48
470	220	3.51	3.9	4.29
465	230	<1.980	<1.980	<1.980

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Table 7-2. 800V Nominal TPS371K-Q1 Adjustable Thresholds

VOLTAGE THRESHOLD SETTING (V)		RESISTANCE TO VDD [kΩ]		
ADJ OV (V_{ITP})	ADJ UV (V_{ITN})	MIN	NOM	MAX
Disabled	Disabled	>150	>150	>150
860	600	61.2	68	74.8
870	580	35.1	39	42.9
880	560	19.8	22	24.2
890	540	10.8	12	13.2
900	520	6.12	6.8	7.48
910	500	3.51	3.9	4.29
920	480	<1.980	<1.980	<1.980

VOLTAGE THRESHOLD SETTING (V)		RESISTANCE TO GND [kΩ]		
ADJ OV (V_{ITP})	ADJ UV (V_{ITN})	MIN	NOM	MAX
1000	320	>150	>150	>150
990	340	61.2	68	74.8
980	360	35.1	39	42.9
970	380	19.8	22	24.2
960	400	10.8	12	13.2
950	420	6.12	6.8	7.48
940	440	3.51	3.9	4.29
930	460	<1.980	<1.980	<1.980

Table 7-3. 1200V Nominal TPS371K-Q1 Adjustable Thresholds

VOLTAGE THRESHOLD SETTING (V)		RESISTANCE TO VDD [kΩ]		
ADJ OV (V_{ITP})	ADJ UV (V_{ITN})	MIN	NOM	MAX
Disabled	Disabled	>150	>150	>150
1290	900	61.2	68	74.8
1305	870	35.1	39	42.9
1320	840	19.8	22	24.2
1335	810	10.8	12	13.2
1350	780	6.12	6.8	7.48
1365	750	3.51	3.9	4.29
1380	720	<1.980	<1.980	<1.980

VOLTAGE THRESHOLD SETTING (V)		RESISTANCE TO GND [kΩ]		
ADJ OV (V_{ITP})	ADJ UV (V_{ITN})	MIN	NOM	MAX
1500	480	>150	>150	>150
1485	510	61.2	68	74.8
1470	540	35.1	39	42.9
1455	570	19.8	22	24.2
1440	600	10.8	12	13.2
1425	630	6.12	6.8	7.48
1410	660	3.51	3.9	4.29
1395	690	<1.980	<1.980	<1.980

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7.3.4 Release Time Delay

TPS371K-Q1 has several options of release time delay based on output pin. Check the Section 9.1 to verify variant specific timing.

- Pin 10 has no additional release time delay options.
- For pin 10 the release time delay is t_{pdLH_LUV} for LOW UV variants.
- Pin 13 has the option for capacitor adjustable release time delay or no additional release time delay.
- For pin 13 capacitor adjustable release time delay, the time delay is indicated by t_{CTR_UV} or t_{CTR_LUV}.
- Pin 13 capacitor adjustable release time delay has a capacitor discharge circuit check to provides that consecutive faults have the full programmed capacitor release time delay.
- For pin 13 the no additional release time delay disables the CTR circuitry and has the timing t_{pdLH_UV} or t_{pdLH_LUV} .
- Pin 14 has the option for fixed release time delay or no additional release time delay
- For pin 14 the fixed released time delay is t_{FDLH_OV}.
- For pin 14 the no additional release time delay is $_{tpdLH\_OV}$.

7.3.4.1 Capacitor Adjustable Release Time Delay Configuration

The time delay (t_{CTR_UV} or T_{CTR_LUV}) can be programmed by connecting a capacitor between CTR pin and GND.

The relationship between external capacitor $C_{CTR\_EXT\ (typ)}$ and the time delay $t_{CTR\ (typ)}$ is given by Equation 1.

$$t_{CTR\ (typ)} = R_{CTR\ (typ)} \times C_{CTR\_EXT\ (typ)} + t_{CTR\ (no\ cap)} \quad (1)$$

$R_{CTR\ (typ)}$ = is in kilo ohms (kΩ)

$C_{CTR\_EXT\ (typ)}$ = is given in microfarads (μF)

$t_{CTR\ (no\ cap)}$ = is either t_{CTR_UV} or t_{CTR_LUV}.

$t_{CTR\ (typ)}$ = is the release time delay (ms)

The release delay varies according to three variables: the external capacitor (C_{CTR_EXT}), CTR pin internal resistance (R_{CTR}) provided in Section 6.5, and a constant $t_{CTR\ (no\ cap)}$. The minimum and maximum variance due to the constant is show in Equation 2 and Equation 3:

$$t_{CTR\ (min)} = R_{CTR\ (min)} \times C_{CTR\_EXT\ (min)} + t_{CTR\ (no\ cap)} \quad (2)$$

$$t_{CTR\ (max)} = R_{CTR\ (max)} \times C_{CTR\_EXT\ (max)} + t_{CTR\ (no\ cap)} \quad (3)$$

There is no limit to the capacitor on CTR pin. Having a too large of a capacitor value can cause very slow charge up (rise times) due to capacitor leakage and system noise can cause the internal circuit to hold the output active.

7.3.5 Sense Time Delay

TPS371K-Q1 has several options of sense time delay based on output pin. Sense time delay is a programmable deglitch filter that helps in noisy environments. Check the Section 9.1 to verify variant specific timing.

- Pin 10 has no additional sense time delay options.
- For pin 10 the sense time delay is t_{pdHL_LUV} for LOW UV variants.
- Pin 13 has the option for capacitor adjustable sense time delay or no additional sense time delay.
- For pin 13 capacitor adjustable sense time delay, the time delay is indicated by t_{CTS_UV} or t_{CTS_LUV}.
- For pin 13 the no additional sense time delay disables the CTS circuitry and has the timing t_{pdHL_UV} or t_{pdHL_LUV} .
- Pin 14 has the option for fixed sense time delay or no additional sense time delay.
- For pin 14 the fixed sense time delay is t_{FDHL_OV}.
- For pin 14 the no additional sense time delay is $_{tpdHL\_OV}$.

7.3.5.1 Sense Time Delay Configuration

The time delay (t_{CTS_UV} or T_{CTS_LUV}) can be programmed by connecting a capacitor between CTS pin and GND.

The relationship between external capacitor $C_{CTS\_EXT\ (typ)}$ and the time delay $t_{CTS\ (typ)}$ is given by Equation 4.

$$t_{CTS(typ)} = R_{CTS\ (typ)} \times C_{CTR\_EXS\ (typ)} + t_{CTS\ (no\ cap)} \quad (4)$$

$R_{CTS\ (typ)}$ = is in kilo ohms (kΩ)

$C_{CTS\_EXT\ (typ)}$ = is given in microfarads (µF)

$t_{CTS\ (no\ cap)}$ = is either t_{CTS_UV} or t_{CTS_LUV}.

$t_{CTS\ (typ)}$ = is the sense time delay (ms)

The sense delay varies according to three variables: the external capacitor (C_{CTS_EXT}), CTS pin internal resistance (R_{CTS}) provided in Section 6.5, and a constant $t_{CTS\ (no\ cap)}$. The minimum and maximum variance due to the constant is show in Equation 5 and Equation 6:

$$t_{CTS\ (min)} = R_{CTS\ (min)} \times C_{CTS\_EXT\ (min)} + t_{CTS\ (no\ cap)} \quad (5)$$

$$t_{CTS\ (max)} = R_{CTS\ (max)} \times C_{CTS\_EXT\ (max)} + t_{CTS\ (no\ cap)} \quad (6)$$

There is no limit to the capacitor on CTS pin. Having a too large of a capacitor value can cause very slow charge up (rise times) due to capacitor leakage.

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7.3.6 Built-In Self-Test (BIST)

The TPS371K-Q1 has a Built-In Self-Test (BIST) feature that runs diagnostics internally in the device. This feature is only included in certain variants, check the Section 9.1 to verify variant features.

BIST Diagnostics:

- SENSE ladder open detect
- Comparators stick high or stuck low
- Internal VREF stuck high or stuck low
- CTR/CTS functionality checks
- Pin 10, Pin 13, Pin 14 stuck high
- Latch functionality checks
- ADJ OV / ADJ UV decoding properly
- Optional ADJ OV / ADJ UV code output for MCU verification

Startup BIST is initiated automatically after crossing $V_{DD(min)}$. During power-up, the BIST test asserts and holds OUT OV, OUT UV, LOW UV, and BIST low until the BIST test completes successfully. The length of the BIST is specified by t_{BIST}. If BIST is not successful due to the internal blocks not working properly, the BIST is held low signifying a fault internal to the device. See Figure 7-6 for more details.

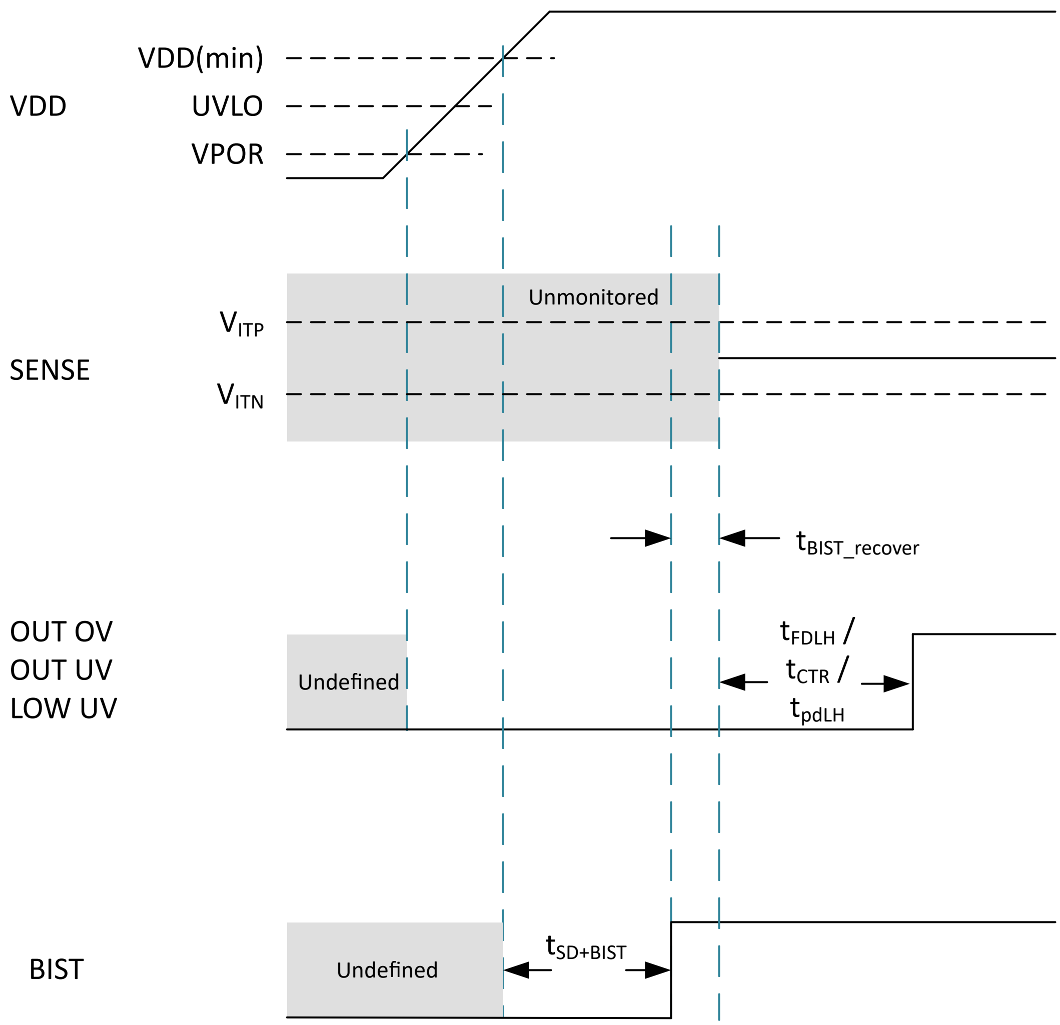

Figure 7-6. TPS371K-Q1 with BIST Start-Up Sequence

After a successful power-up sequence, BIST can be initiated any time with a positive edge transition on the BIST EN pin. BIST only initiates if the SENSE pin is not in a fault mode. During this BIST test time period, t_{BIST}, BIST pin asserts low to signify that BIST has started and OUT OV, OUT UV, LOW UV assert. During BIST the device is not monitoring the SENSE pin for faults and the OUT OV, OUT UV, LOW UV pin is not dependent on the SENSE pin voltage. Upon successful BIST the BIST pin and OUT OV, OUT UV, LOW UV pin are deasserted. If BIST is not successful due to the internal device not working properly, the OUT OV, OUT UV, LOW UV pin and BIST pin are asserted low signifying a fault internal to the device. See Figure 7-7 and Figure 7-8 for more details.

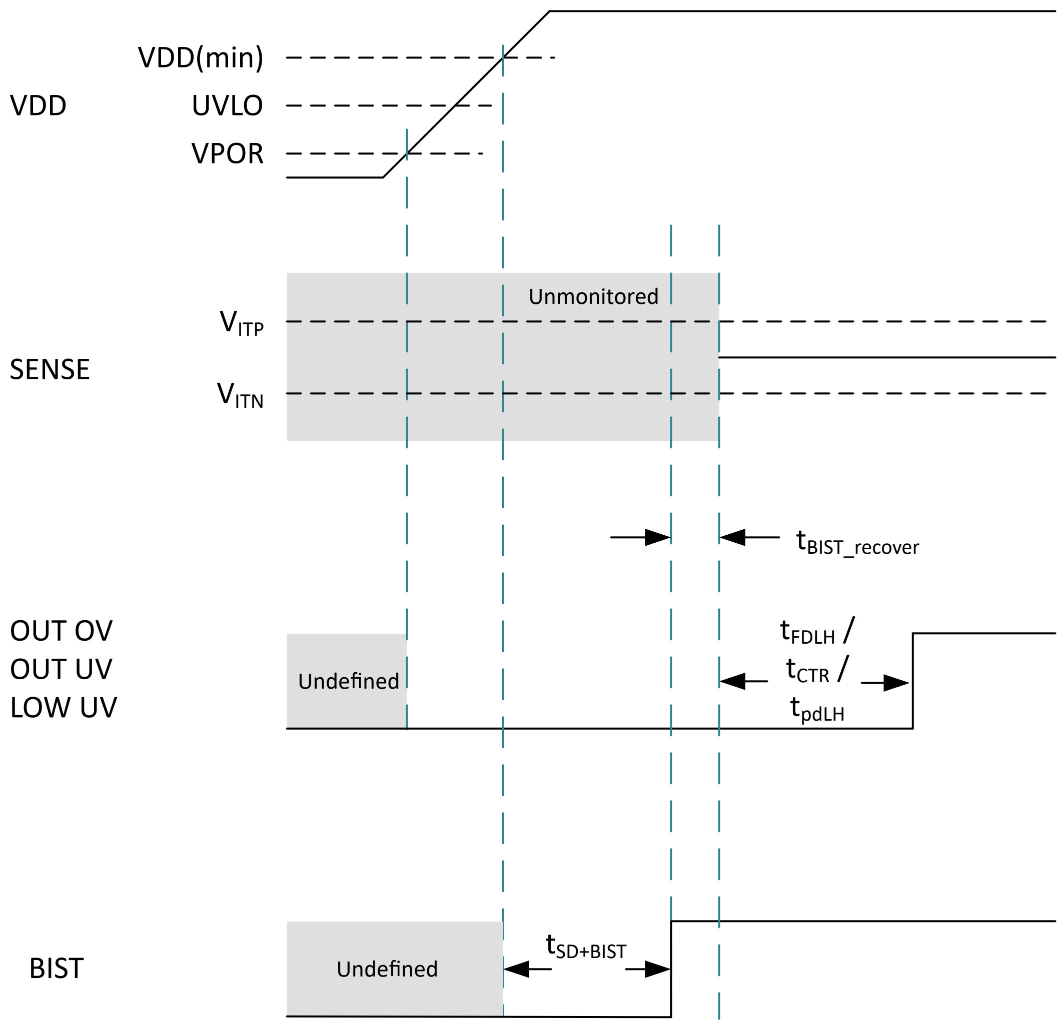

Figure 7-7. BIST Enable

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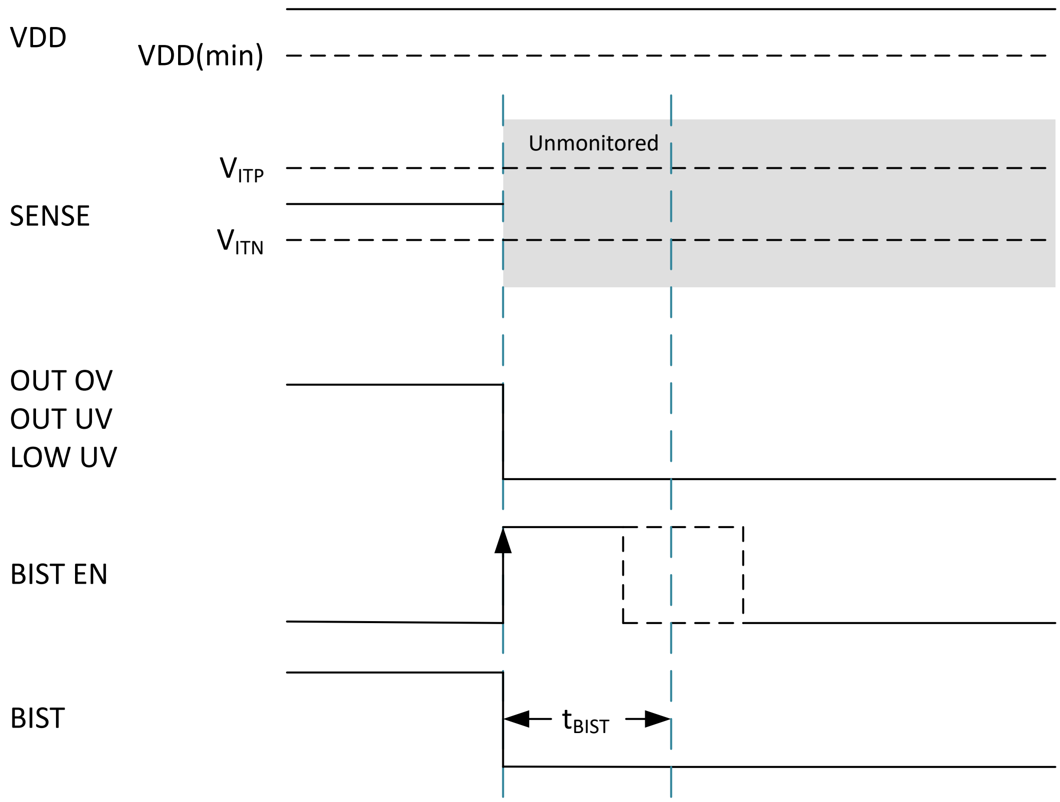

Figure 7-8. BIST Fail

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

8.2 Typical Application

8.2.1 Design 1: DC-Link Monitoring

This application is intended for the initial power stage in applications with the 800V DC-Links. The TPS371K-Q1 utilizes high-voltage SENSE inputs to monitor an automotive high voltage DC-Link rail without needing external resistors. This keeps the overall size low while still achieving voltage fault monitoring.

Figure 8-1 illustrates an example of how the TPS371K-Q1 is monitoring the battery voltage for faults while providing a buffer for voltage telemetry.

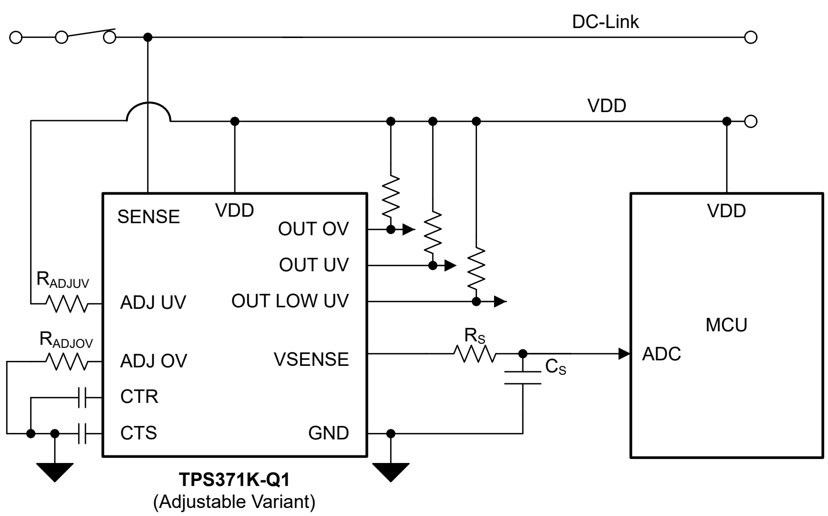

Figure 8-1. 800V DC-Link Monitor

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8.2.1.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Voltage Threshold	Overvoltage: 900V Undervoltage: 580V	R_{ADJOV} = 3.9kΩ to GND R_{ADJUV} = 39kΩ to VDD
Maximum Input Power	Operates with power supply input up to 5V	The TPS371K-Q1 can support a V_{DD} of up to 5.5V.
Output Logic	Open-Drain	Open-Drain
SENSE Delay	100µs for overvoltage 1ms for undervoltage	7µs for overvoltage 100µs for undervoltage
ADC Voltage	3.3V full scale range 800V scaled down to 1.85V	TPS371K-Q1 can support 800V a 3.3V ADC with the 440 buffer output ratio
ADC bit-rate and sampling speed	12-b ADC sampling at 500ksps	R_S = 180Ω C_S = 150pF

8.2.1.2 Detailed Design Procedure

The TPS371K-Q1 utilizes high-voltage SENSE inputs to monitor an automotive battery without needing external resistors. This keeps the overall system I_Q of the design low while still achieving the desired rail monitoring.

8.2.1.2.1 Setting Voltage Threshold

The voltage rail monitoring is done by connecting the SENSE input directly to the 800V rail without the need for external resistor dividers. The threshold voltage options are set by the device variant. Threshold voltage decoding can be found in Section 4 in combination with the Section 7.3.3. In this example, the nominal supply voltage from the battery is 800V and the variation of the DC-Link is commonly between 720V and 880V. Setting a overvoltage threshold of 940V specifies that the TPS371K-Q1 OUT UV asserts for overvoltage faults and transients that can signify a overvoltage transient in the system. The 940V V_{ITP} corresponds to a R_{ADJOV} = 3.9kΩ connected to GND. Setting an undervoltage threshold of 580V specifies the OUT UV to deassert once the DC-Link charges to voltages above 580V for sequencing purposes or discharged notifications. The 580V V_{ITN} corresponds to a R_{ADJOV} = 39kΩ to VDD.

8.2.1.2.2 Meeting the Sense and Reset Delay

The TPS371K-Q1 features two options for selecting sense and reset delays: fixed delays and capacitor-programmable delays. The application requires a fast sense reaction of <100µs for OV and <1ms UV. For OV, no additional time delay was added which meets the speed requirement. For UV, leaving CTS open solves the design challenge as this gives the fastest delay possible for OUT UV when CTS is enabled.

8.2.1.2.3 Setting Supply Voltage

Setting the supply voltage is done by connecting the V_{DD} input to a voltage below 5.5V. This means the TPS371K-Q1 can support common voltages used in low voltage designs. Good analog design practice recommends using a 0.1µF capacitor on the V_{DD} pin.

8.2.1.3 Application Curves

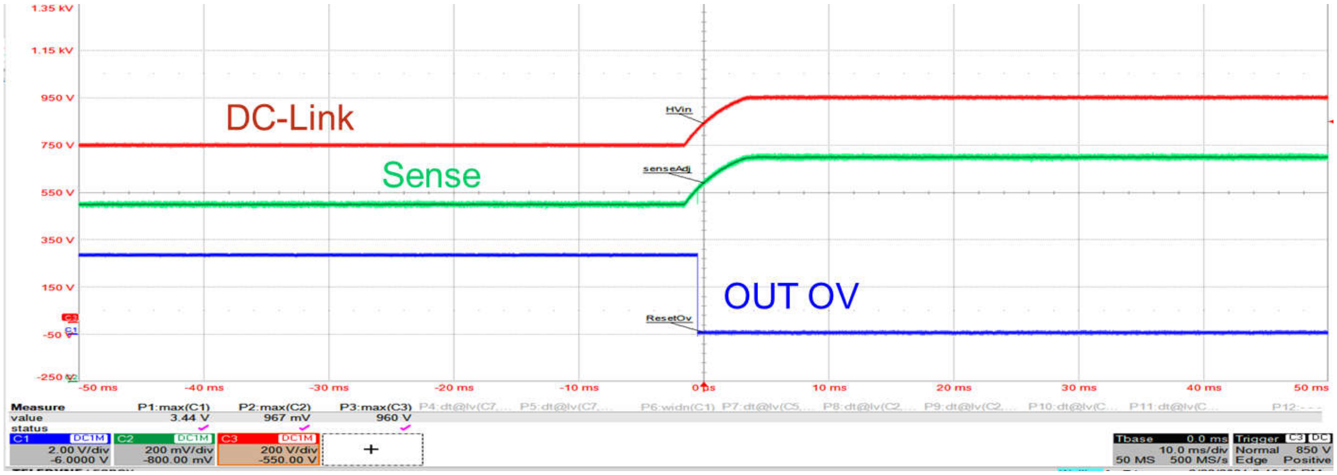

Figure 8-2. OUT UV Triggering

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8.3 Power Supply Recommendations

TPS371K-Q1 is designed to operate from an input supply with a V_{DD} voltage between 2.7V (minimum operation) to 5.5V (maximum operation). Good analog design practice recommends placing a minimum 0.1μF ceramic capacitor as near as possible to the V_{DD} pin.

8.3.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum continuous allowable power dissipation for the device in a given package can be calculated using Equation 7:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} – T_A) / R_{\theta JA}) \quad (7)$$

The actual power being dissipated in the device can be represented by Equation 8:

$$P_D = V_{DD} \times I_{DD} + p_{RESET} + p_{SENSE} \quad (8)$$

p_{RESET} is calculated by Equation 10. p_{SENSE} is calculated by Equation 10.

$$p_{RESET\ (OPEN\text{-}DRAIN)} = V_{RESET} \times I_{RESET} \quad (9)$$

$$p_{SENSE} = V_{SENSE} \times I_{SENSE} \quad (10)$$

Equation 7 and Equation 8 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations must be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) can be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) can be de-rated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by Equation 11:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})) \quad (11)$$

8.4 Layout

8.4.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1μF ceramic capacitor as near as possible to the VDD pin.
- If a capacitor is used on CTS or CTR, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance on the pins to less than 5pF.
- Place the pull-up resistors on OUT OV, OUT UV, LOW UV, and BIST as close to the pin as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible.

8.4.2 Layout Example

The layout example in Figure 8-3 shows how the TPS371K-Q1 is laid out on a printed circuit board (PCB) with user-defined delays.

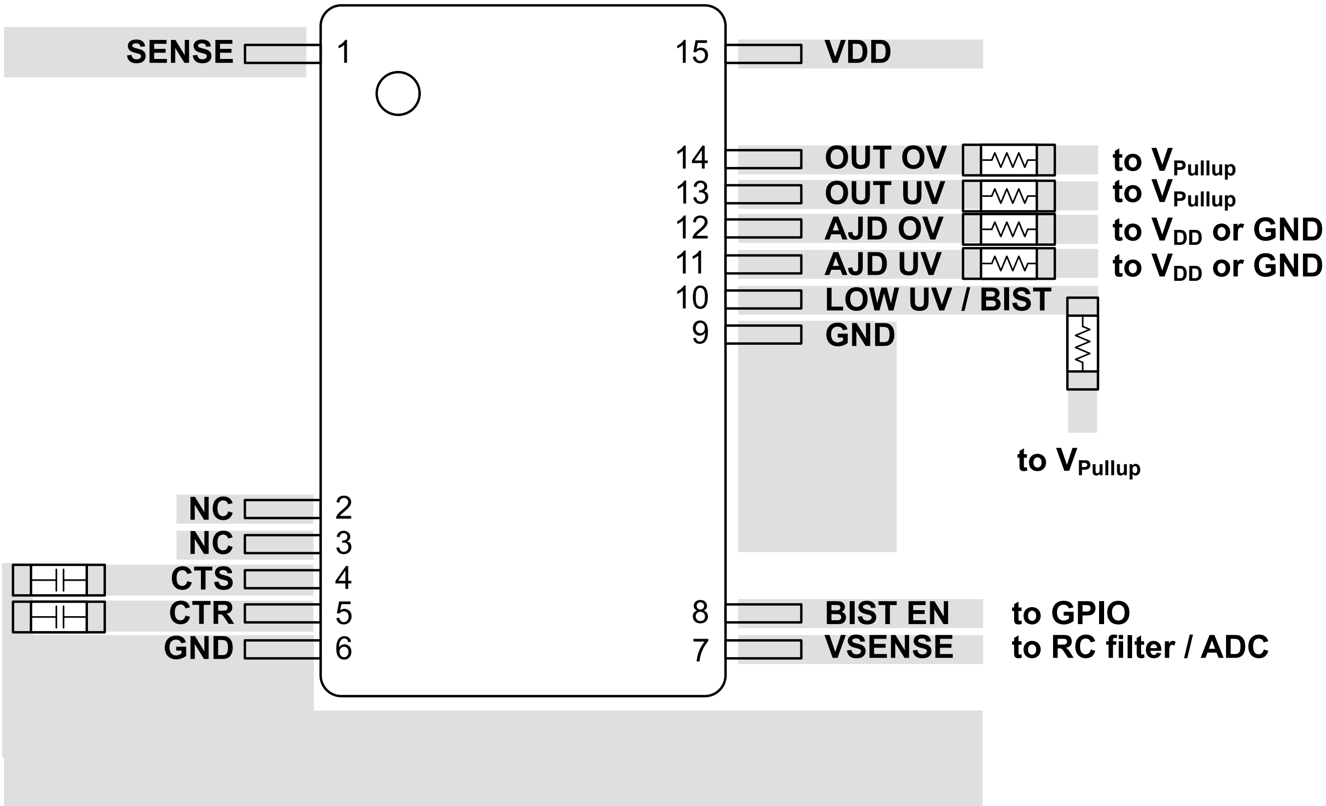

Figure 8-3. TPS371K-Q1 Recommended Layout

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9 Device and Documentation Support

9.1 Device Nomenclature

Device Decoder in Table 5-1 describe how to decode certain device function of the device based on the orderable part number. Not all part numbers follow this nomenclature. Use Table 9-1 as the part number decoding table for all devices.

Table 9-1. Device Configuration Table

ORDERABLE PART NAME	Thresholds	OV Threshold	OV Hysteresis	UV Threshold	UV Hysteresis	Low UV Threshold	Time Delay	VSENSE Scale
PTPS371KVM5DFXRQ1	Fixed	900V	2%	N/A	N/A	N/A	ADJ CTS ADJ CTR	N/A

9.2 Documentation Support

9.2.1 Related Documentation

The following related documents are available for download at www.ti.com:

- *Optimizing Resistor Dividers at a Comparator Input*, SLVA450
- *Sensitivity Analysis for Power Supply Design*, SLVA481

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2025) to Revision A (May 2026) — **Page**

- Changed document release status from NDA to public information...1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PPS371KA8C89DFXRQ1	Active	Preproduction	SSOP (DFX) | 15	750 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

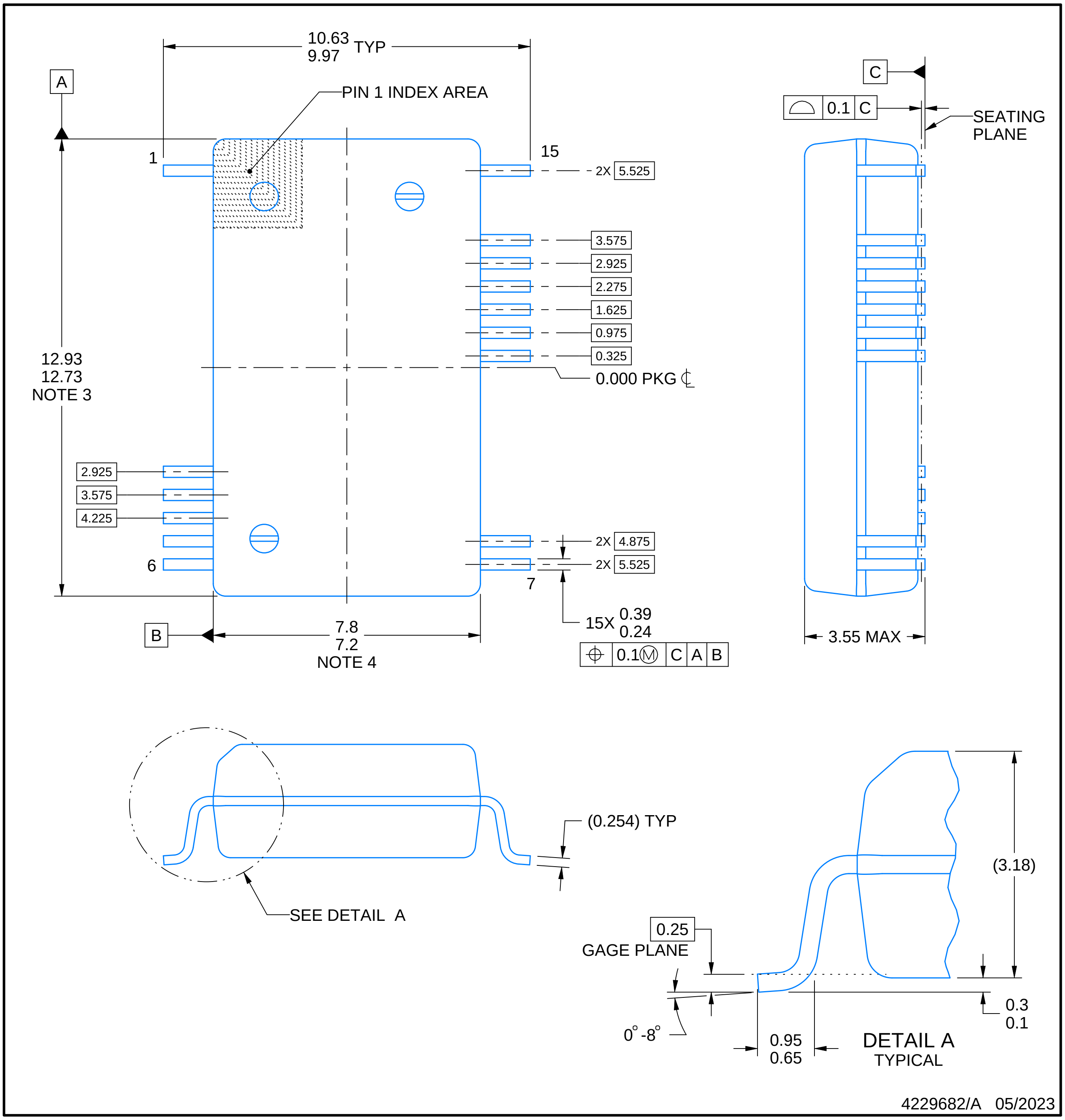
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

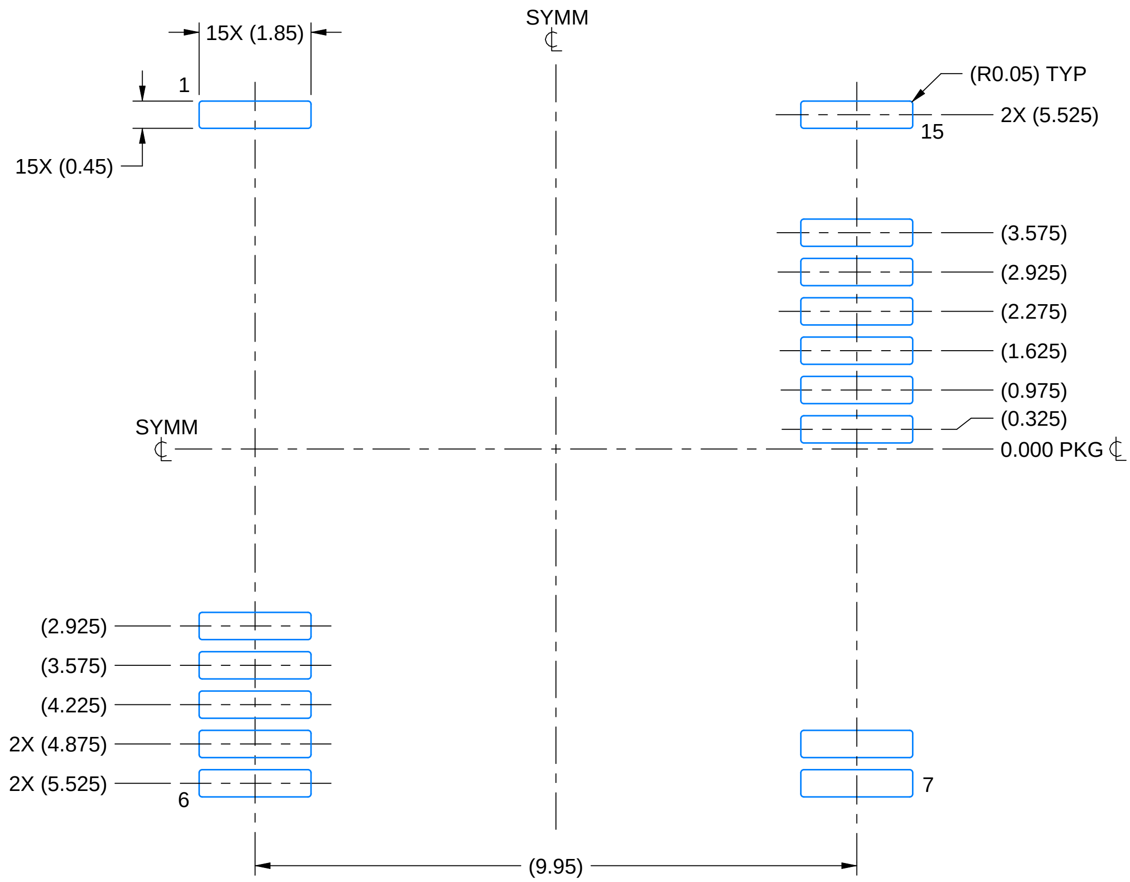
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

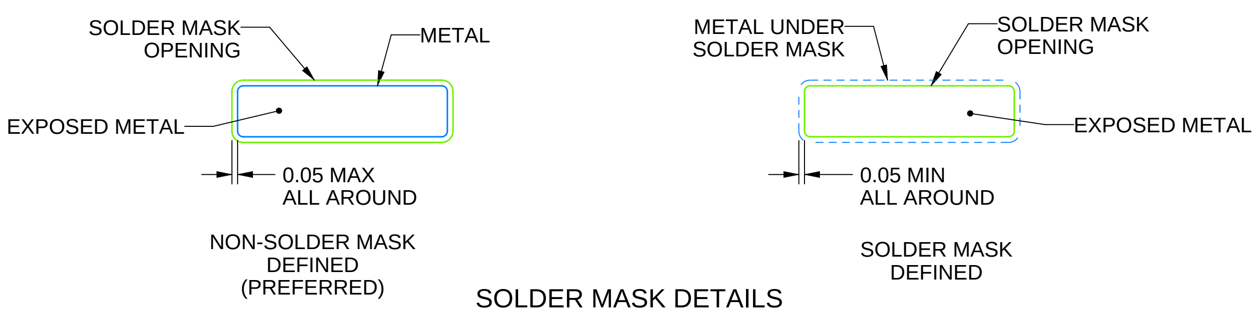


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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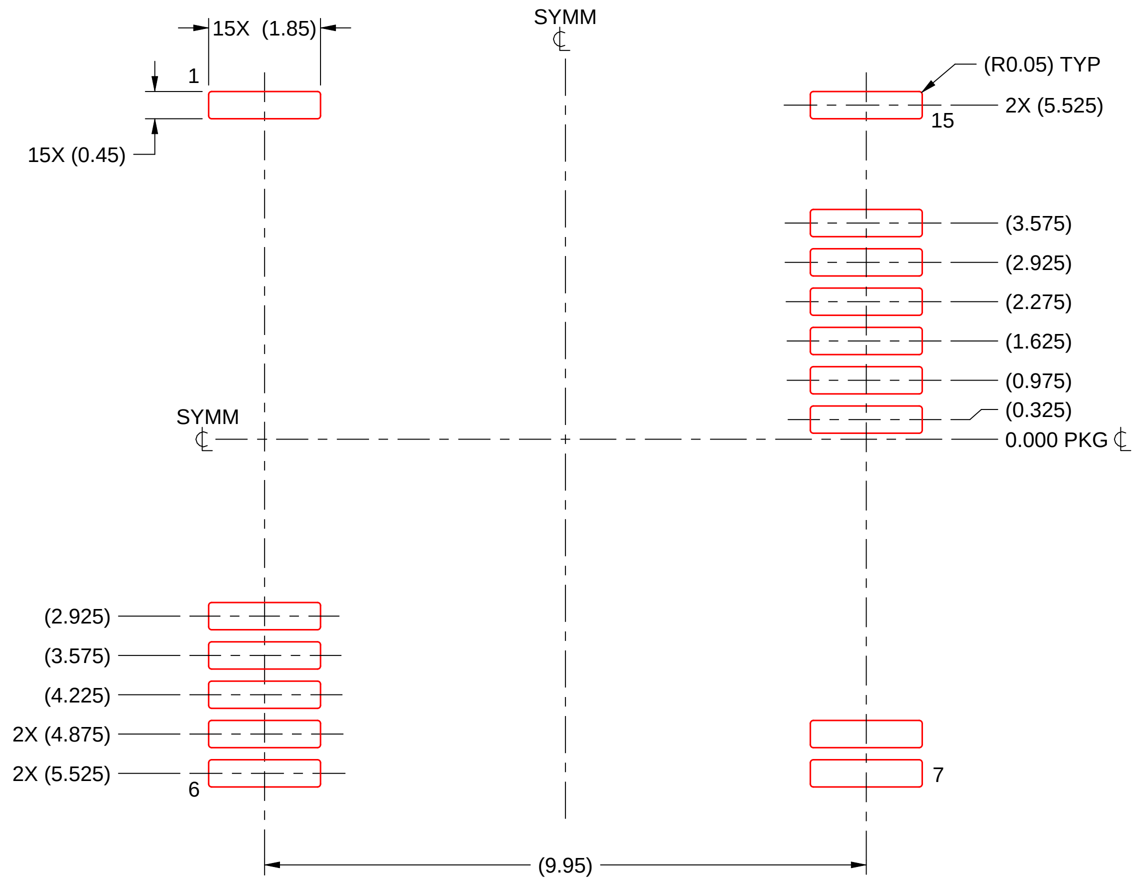
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.