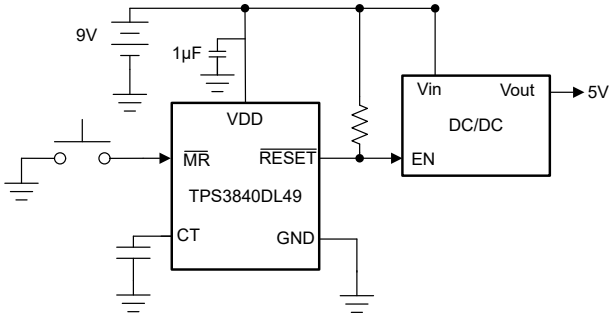
TPS3840 Nano Power, High Input Voltage Supervisor With $\overline{MR}$ and Programmable Delay

1 Features

- Wide operating voltage: 1.5V to 10V
- Nano supply current: 300nA (typical), 700nA (maximum)
- Fixed threshold voltage (V_{IT-})
  - Threshold from 1.6V to 4.9V in 0.1V steps
  - High accuracy: 1% (typical), 1.5% (maximum)
  - Built-in hysteresis (V_{IT+})
    - 1.6V ≤ V_{IT-} ≤ 3.0V = 100mV (typical)
    - 3.1V ≤ V_{IT-} ≤ 4.9V = 200mV (typical)
- Start-up delay (t_{STRT}): 220µs (typical), 350µs (maximum)
- Programmable reset time delay (t_D):
  - 50µs (no capacitor) to 6.2s (10µF)
- Active-low manual reset ($\overline{MR}$)
- Three output topologies:
  - TPS3840DL: open-drain, active-low ($\overline{RESET}$), requires pull-up resistor
  - TPS3840PL: push-pull, active-low ($\overline{RESET}$)
  - TPS3840PH: push-pull, active-high (RESET)
- Wide temperature range: –40°C to +125°C
- Package: SOT23-5 (DBV)

2 Applications

- Grid infrastructure: circuit breaker, smart meter, other monitoring and protection equipment
- Factory automation: field transmitter, PLC
- Building automation: fire safety, smoke detector, and HVAC
- Electronic point of sale
- Portable, battery-powered systems



Typical Application Circuit

3 Description

Wide Vin allows monitoring 9V rails or batteries without external components and 24V rails with external resistors. Nano-Iq extends battery life for low power applications and minimizes current consumption when using external resistors. Fast start-up delay allows the detection of a voltage fault before the rest of the system powers up providing maximum safety in hazardous start-up fault conditions. Low Power-on-Reset (V_{POR}) prevents false resets, premature enable or turn-on of next device, and proper transistor control during power-up and power-down.

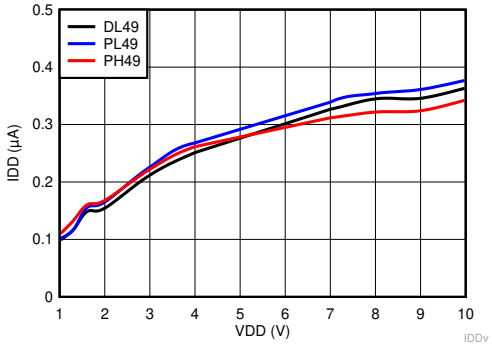
Reset output signal is asserted when the voltage at V_{DD} drops below the negative voltage threshold (V_{IT-}) or when manual reset ($\overline{MR}$) is pulled to a low logic ($V_{\overline{MR}\_L}$). Reset signal is cleared when V_{DD} rise above V_{IT-} plus hysteresis (V_{IT+}) and manual reset is floating or above $V_{\overline{MR}\_H}$ and the reset time delay (t_D) expires. Reset time delay can be programmed by connecting a capacitor between CT pin and ground. For a fast reset CT pin can be left floating.

Additional features: Built-in glitch immunity protection for $\overline{MR}$ and V_{DD}, built-in hysteresis, low open-drain output leakage current ($I_{LKG(OD)}$).

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS3840	SOT-23 (5) (DBV)	2.90mm × 1.60mm

(1) For package details, see the mechanical drawing addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPS3840 Typical Supply Current

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4 Device Comparison

Figure 4-1 shows the device nomenclature to determine the device variant. Other voltages from Table 9-2 at the end of datasheet can be sample upon request, please contact TI sales representative for details.

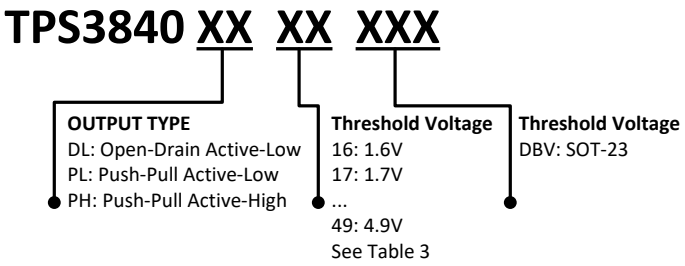


Figure 4-1. Device Nomenclature

5 Pin Configuration and Functions

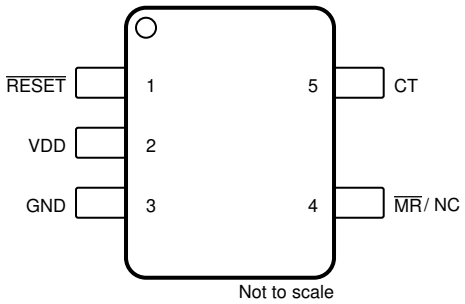


Figure 5-1. DBV Package 5-Pin SOT-23 TPS3840PL, TPS3840DL Top View

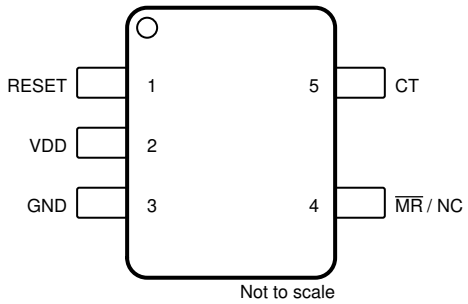


Figure 5-2. DBV Package 5-Pin SOT-23 TPS3840PH Top View

Table 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	TPS3840PL, TPS3840DL	TPS3840PH		
CT	5	5	-	**Capacitor Time Delay Pin**. The CT pin offers a user-programmable reset delay time. Connect an external capacitor on this pin to adjust the reset time delay. When not in use, leave pin floating for the smallest fixed reset time delay.
GND	3	3	_	**Ground**
$\overline{MR}$ / NC	4	4	I	**Manual Reset**. Pull this pin to a logic low ($V_{\overline{MR}\_L}$) to assert a reset signal at the $\overline{RESET}$/RESET pin. If the $\overline{MR}$ pin is left floating or pulled to V_{MR_H}, the output releases to the nominal state after the reset time delay (t_D) expires. **$\overline{MR}$ can be left floating when not in use. NC stands for "No Connection" or floating.**
RESET	N/A	1	O	**Active-High Output Reset Signal:** This pin is asserted to logic high when either the $\overline{MR}$ pin is pulled to a logic low or VDD voltage falls below the negative voltage threshold (V_{IT-}). When both $\overline{MR}$ is floating or above $V_{\overline{MR}\_H}$ and VDD voltage rises above V_{IT+}, RESET remains asserted to logic high (asserted) for the reset time delay (t_D) before releasing back to logic low.
$\overline{RESET}$	1	N/A	O	**Active-Low Output Reset Signal:** This pin is asserted to logic low when either the $\overline{MR}$ pin is pulled to a logic low or the VDD voltage falls below the negative voltage threshold (V_{IT-}). When both $\overline{MR}$ is floating or above $V_{\overline{MR}\_H}$ and VDD voltage rises above V_{IT+}, $\overline{RESET}$ remains asserted to logic low for the reset time delay (t_D) before releasing back to logic high.
VDD	2	2	I	**Input Supply Voltage.** TPS3840 monitors VDD voltage

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	12	V
	$\overline{\text{RESET}}$ (TPS3840PL)	–0.3	V_{DD} + 0.3	
	RESET (TPS3840PH)	–0.3	V_{DD} + 0.3	
	$\overline{\text{RESET}}$ (TPS3840DL)	–0.3	12	
	$\overline{\text{MR}}$ (2)	–0.3	12	
	CT	–0.3	5.5	
Current	$\overline{\text{RESET}}$ pin and RESET pin		±70	mA
Temperature(3)	Operating junction temperature, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If the logic signal driving MR is less than V_{DD}, then additional current flows into V_{DD} and out of MR. V_{MR} must not be higher than V_{DD}.
(3) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	± 750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Input supply voltage	1.5		10	V
$V_{\overline{\text{RESET}}}$, V_{RESET}	$\overline{\text{RESET}}$ pin and RESET pin voltage	0		10	V
$I_{\overline{\text{RESET}}}$, I_{RESET}	$\overline{\text{RESET}}$ pin and RESET pin current	0		±5	mA
T_J	Junction temperature (free air temperature)	–40		125	°C
$V_{\overline{\text{MR}}}$ (1)	Manual reset pin voltage	0		V_{DD}	V

(1) If the logic signal driving MR is less than V_{DD}, then additional current flows into V_{DD} and out of MR. V_{MR} must not be higher than V_{DD}.

6.4 Thermal Information

THERMAL METRIC(1)		TPS3840 DBV (SOT23-5) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	109.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	92.5	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		TPS3840 DBV (SOT23-5) 5 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

At 1.5V ≤ V_{DD} ≤ 10V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100kΩ to VDD, output reset load (C_{LOAD}) = 10pF and over the operating free-air temperature range – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
V_{DD}	Input supply voltage		1.5		10	V
V_{IT-}	Negative-going input threshold accuracy[1]	-40°C to 125°C	–1.5	1	1.5	%
V_{HYS}	Hysteresis on V_{IT-} pin	V_{IT-} = 3.1V to 4.9V	175	200	225	mV
V_{HYS}	Hysteresis on V_{IT-} pin	V_{IT-} = 1.6V to 3.0V	75	100	125	mV
I_{DD}	Supply current into VDD pin	VDD = 1.5V < V_{DD} < 10V VDD > V_{IT+} [3] T_A = -40°C to 125°C		300	700	nA
$V_{\overline{MR}\_L}$	Manual reset logic low input[2]				600	mV
$V_{\overline{MR}\_H}$	Manual reset logic high input[2]		0.7V_{DD}			V
$R_{\overline{MR}}$	Manual reset internal pull-up resistance			100		kΩ
R_{CT}	CT pin internal resistance		350	500	650	kΩ
TPS3840PL (Push-Pull Active-Low)						
V_{POR}	Power on Reset Voltage[4]	$V_{OL(max)}$ = 200mV $I_{OUT(Sink)}$ = 200nA			300	mV
V_{OL}	Low level output voltage	1.5V < V_{DD} < 5V V_{DD} < V_{IT-} $I_{OUT(Sink)}$ = 2mA			200	mV
V_{OH}	High level output voltage	1.5V < V_{DD} < 5V V_{DD} > V_{IT+} [3] $I_{OUT(Source)}$) = 2mA	0.8V_{DD}			V
		5V < V_{DD} < 10V V_{DD} > V_{IT+} [3] $I_{OUT(Source)}$ = 5mA	0.8V_{DD}			V
TPS3840PH (Push-Pull Active-High)						
V_{POR}	Power on Reset Voltage[4]	V_{OH}, $I_{OUT(Source)}$ = 500nA			950	mV
V_{OL}	Low level output voltage	1.5V < V_{DD} < 5V V_{DD} > V_{IT+} [3] $I_{OUT(Sink)}$ = 2mA			200	mV
		1.5V < V_{DD} < 5V V_{DD} > V_{IT+} [3] $I_{OUT(Sink)}$ = 5mA			200	mV
V_{OH}	High level output voltage	1.5V < V_{DD} < 5V, V_{DD} < V_{IT-}, $I_{OUT(Source)}$ = 2mA	0.8V_{DD}			V
TPS3840DL(Open-Drain)						
V_{POR}	Power on Reset Voltage[4]	$V_{OL(max)}$ = 0.2V $I_{OUT\ (Sink)}$ = 5.6 uA			950	mV
V_{OL}	Low level output voltage	1.5V < V_{DD} < 5V V_{DD} < V_{IT-} $I_{OUT(Sink)}$ = 2mA			200	mV

At 1.5V ≤ V_{DD} ≤ 10V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100kΩ to VDD, output reset load (C_{LOAD}) = 10pF and over the operating free-air temperature range – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{lkg(OD)}$	Open-Drain output leakage current	$\overline{RESET}$ pin in High Impedance, V_{DD} = V_{RESET} = 5.5V V_{IT+} < V_{DD}			90	nA

(1) V_{IT-} threshold voltage range from 1.6V to 4.9V in 100mV steps, for released versions see Device Voltage Thresholds table.
(2) If the logic signal driving $\overline{MR}$ is less than VDD, then additional current flows into VDD and out of $\overline{MR}$
(3) V_{IT+} = V_{HYS} + V_{IT-}
(4) V_{POR} is the minimum V_{DD} voltage level for a controlled output state. V_{DD} slew rate ≤ 100mV/µs

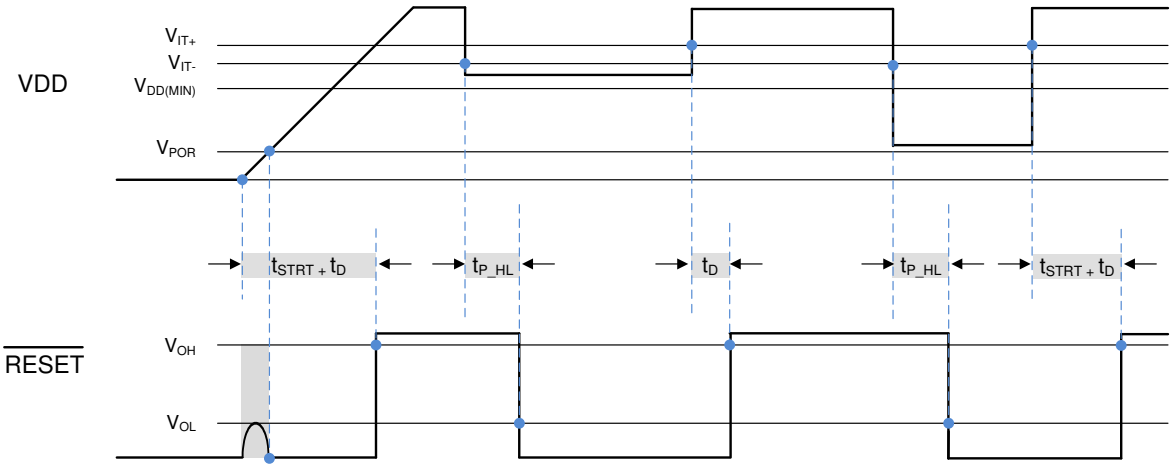
6.6 Timing Requirements

At 1.5V ≤ V_{DD} ≤ 10V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100kΩ to VDD, output reset load (C_{LOAD}) = 10pF and over the operating free-air temperature range – 40°C to 125°C, VDD slew rate < 100mV / us, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STRT}	Startup Delay(1)	CT pin open	100	220	350	µs
t_{P_HL}	Propagation detect delay for VDD falling below V_{IT-}	V_{DD} = V_{IT+} to (V_{IT-}) - 10%(2)		15	30	µs
t_D	Reset time delay(3)	CT pin = open			50	µs
		CT pin = 10nF		6.2		ms
		CT pin = 1 µF		619		ms
t_{GI_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive(4)		10		µs
t_{MR_PW}	$\overline{MR}$ pin pulse duration to initiate reset			300		ns
t_{MR_RES}	Propagation delay from $\overline{MR}$ low to reset	V_{DD} = 4.5V, $\overline{MR}$ < $V_{\overline{MR}\_L}$		700		ns
t_{MR_tD}	Delay from release $\overline{MR}$ to deasert reset	V_{DD} = 4.5V, $\overline{MR}$ = $V_{\overline{MR}\_L}$ to $V_{\overline{MR}\_H}$		t_D		ms

(1) When VDD starts from less than the specified minimum V_{DD} and then exceeds V_{IT+}, reset is release after the startup delay (t_{STRT}), a capacitor at CT pin adds t_D delay to t_{STRT} time
(2) t_{P_HL} measured from the threshold trip point (V_{IT-}) to V_{OL} for active low variants and V_{OH} for active high variants.
(3) The MIN and MAX reset time delay with external capacitor depends on R_{CT} and is calculated using Equation 5 and Equation 6 in Section 7.3.2

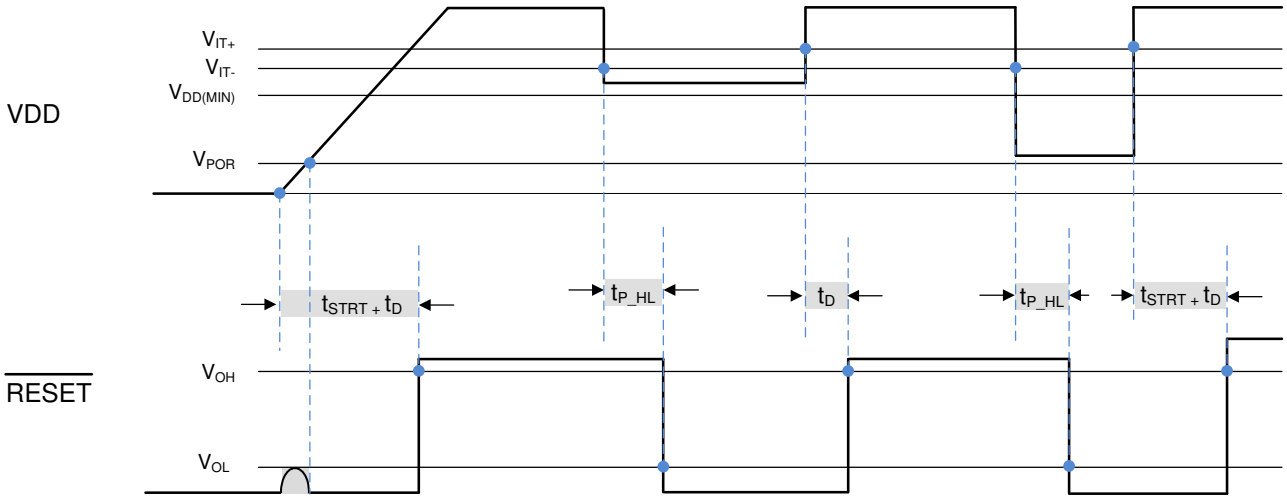
(4) $$\text{Overdrive\%} = \left(\frac{V_{DD}}{V_{IT-}} - 1\right) \times 100\% \quad (1)$$



A. $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin then t_D programmed time is added to the startup time, VDD slew rate = 100mV/µs.
B. Open-Drain timing diagram assumes pull-up resistor is connected to $\overline{RESET}$

C. $\overline{\text{RESET}}$ output is undefined when VDD is < V_{POR}

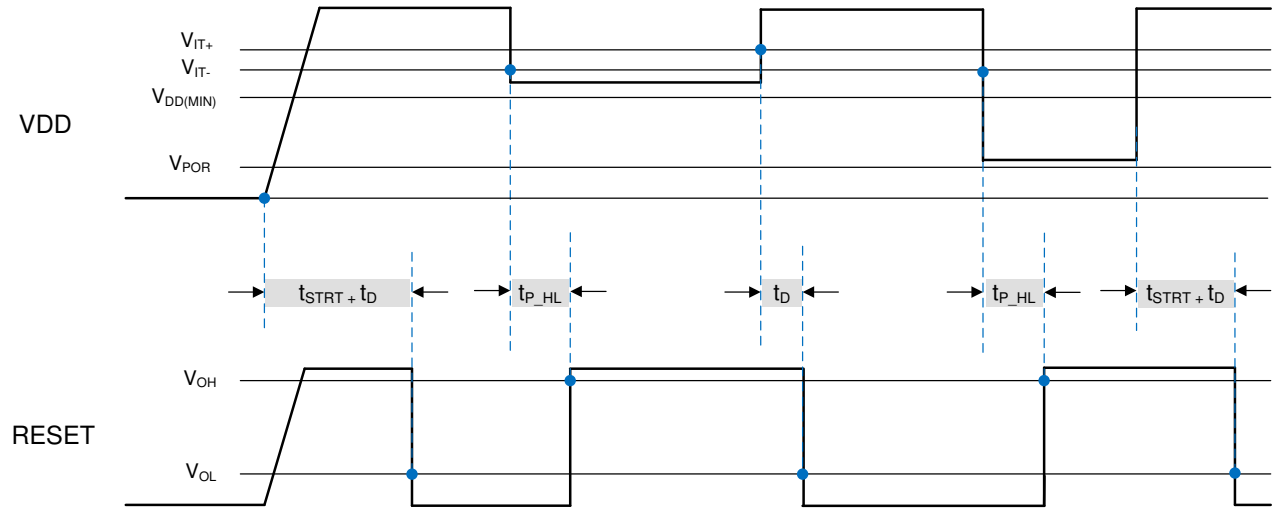
Figure 6-1. Timing Diagram TPS3840DL (Open-Drain Active-Low)



A. $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin, then t_D programmed time is added to the startup time. VDD slew rate = 100mV/µs.

B. $\overline{RESET}$ output is undefined when VDD < V_{POR} and limited to V_{OL} for VDD slew rate = 100mV/µs

Figure 6-2. Timing Diagram TPS3840PL (Push-Pull Active-Low)



A. $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin, then t_D programmed time is added to the total startup time. VDD slew rate = 100mV/µs.

Figure 6-3. Timing Diagram TPS3840PH (Push-Pull Active-High)

6.7 Typical Characteristics

Typical characteristics show the typical performance of the TPS3840 device. Test conditions are T_J = 25°C, V_{DD} = 3.3V, $R_{pull-up}$ = 100kΩ, C_{Load} = 50pF, unless otherwise noted.

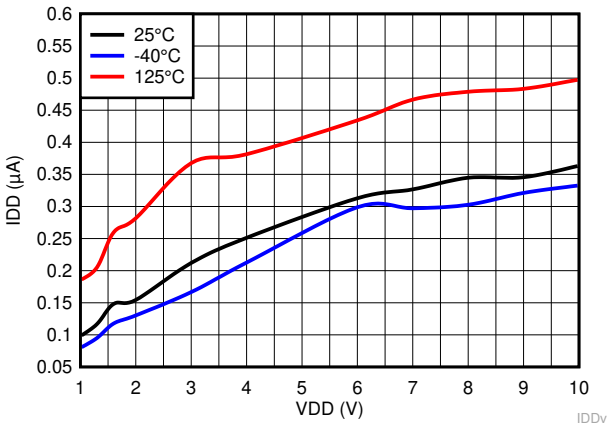


Figure 6-4. Supply Current vs Supply Voltage for TPS3840DL49

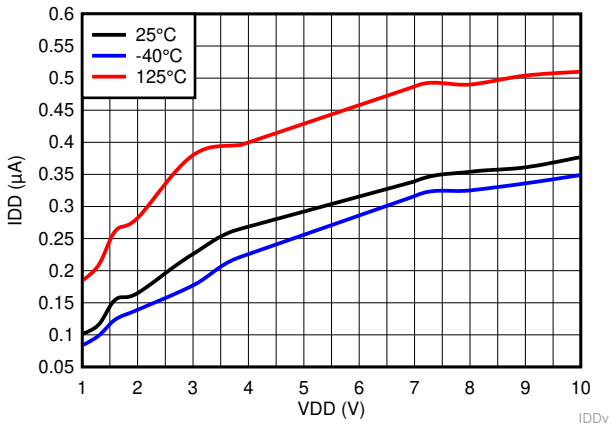


Figure 6-5. Supply Current vs Supply Voltage for TPS3840PL49

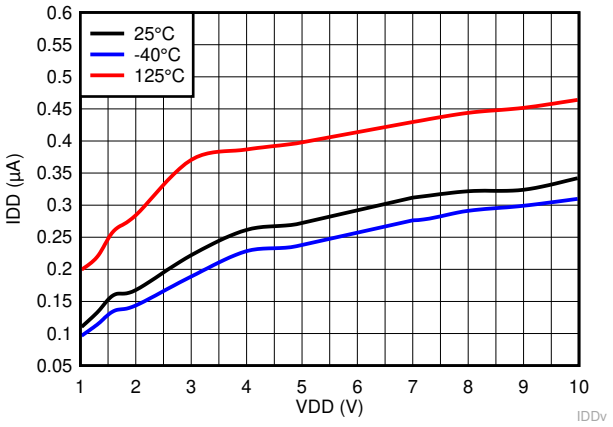


Figure 6-6. Supply Current vs Supply Voltage for TPS3840PH49

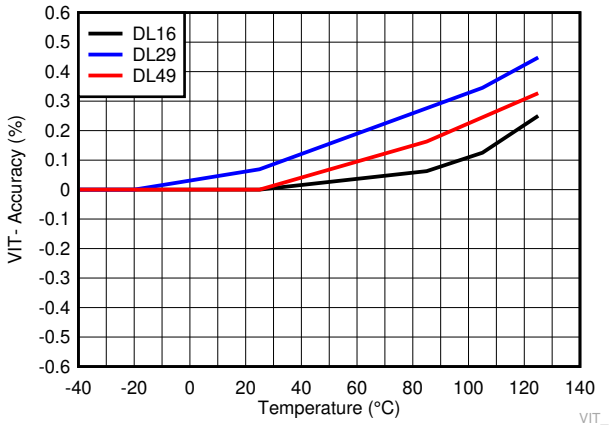


Figure 6-7. Negative-going Input Threshold Accuracy over Temperature for TPS3840DLXX

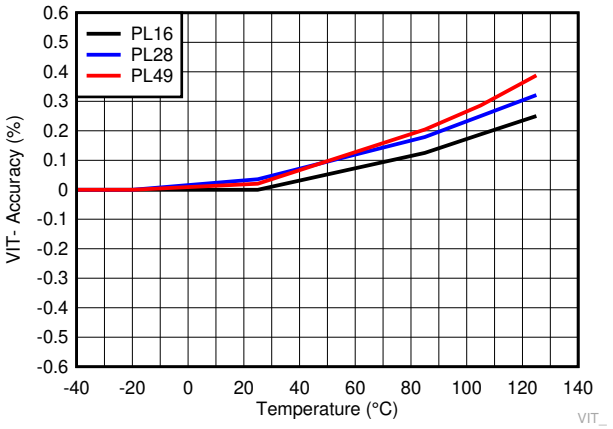


Figure 6-8. Negative-going Input Threshold Accuracy over Temperature for TPS3840PLXX

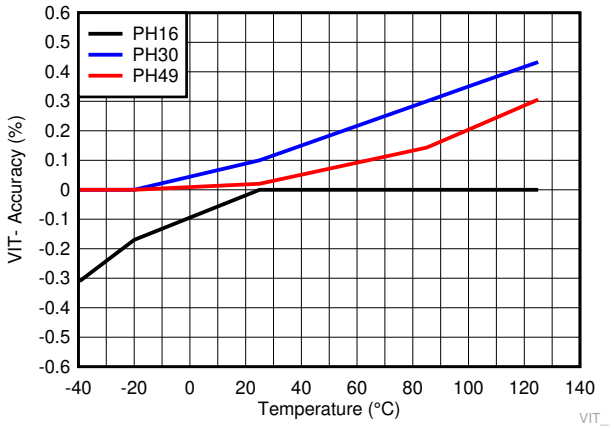


Figure 6-9. Negative-going Input Threshold Accuracy over Temperature for TPS3840PHXX

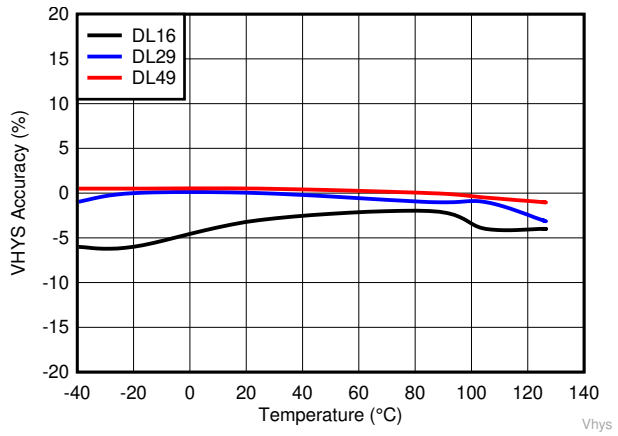


Figure 6-10. Input Threshold V_{IT-} Hysteresis Accuracy for TPS3840DLXX

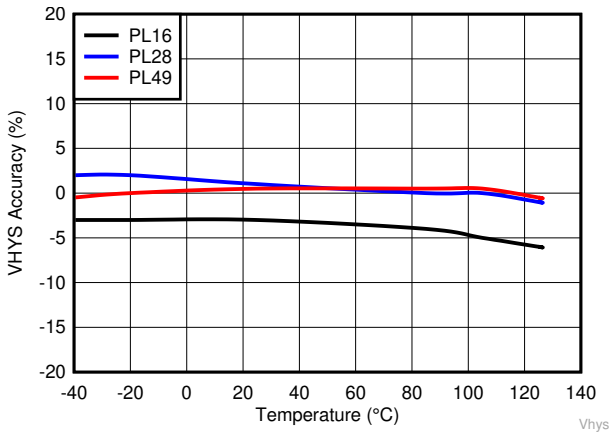


Figure 6-11. Input Threshold V_{IT-} Hysteresis Accuracy for TPS3840PLXX

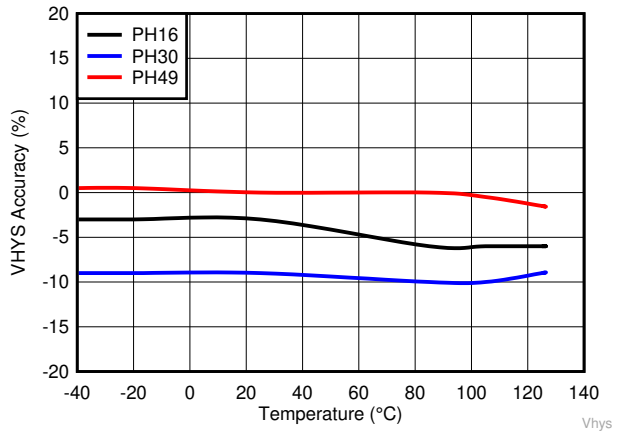


Figure 6-12. Input Threshold V_{IT-} Hysteresis Accuracy for TPS3840PHXX

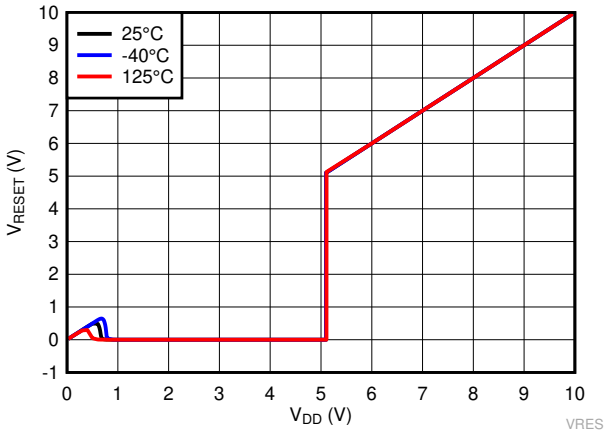


Figure 6-13. Output Voltage vs Input Voltage for TPS3840DL49

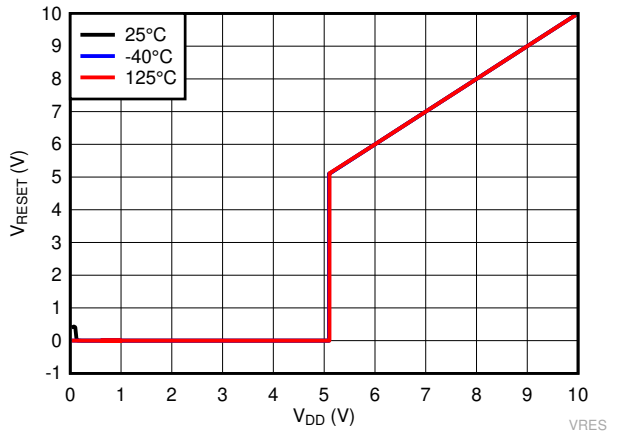


Figure 6-14. Output Voltage vs Input Voltage for TPS3840PL49

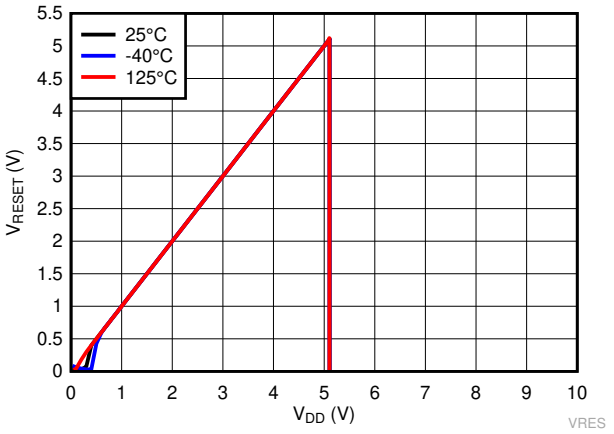


Figure 6-15. Output Voltage vs Input Voltage for TPS3840PH49

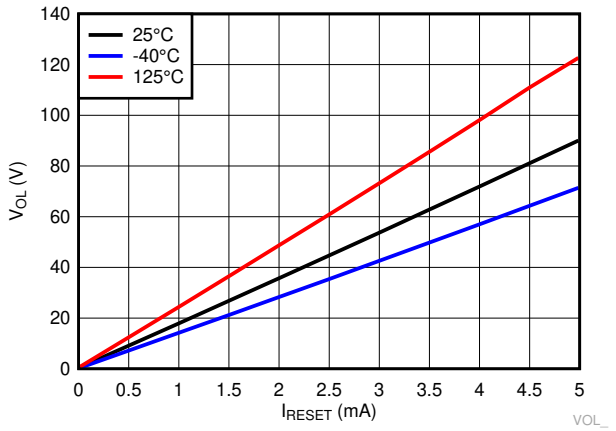


Figure 6-16. Low Level Output Voltage vs I_{RESET} for TPS3840DL49

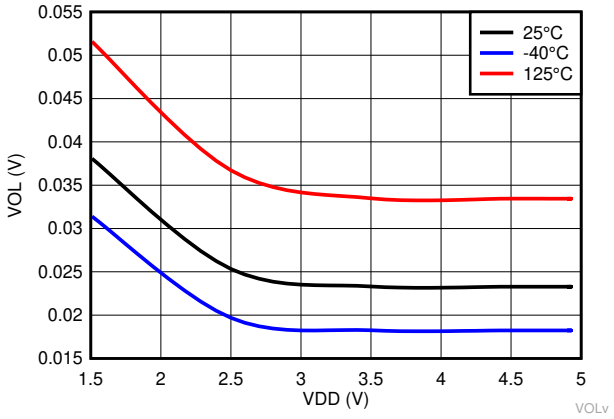


Figure 6-17. Low Level Output Voltage vs V_{DD} for TPS3840DL49

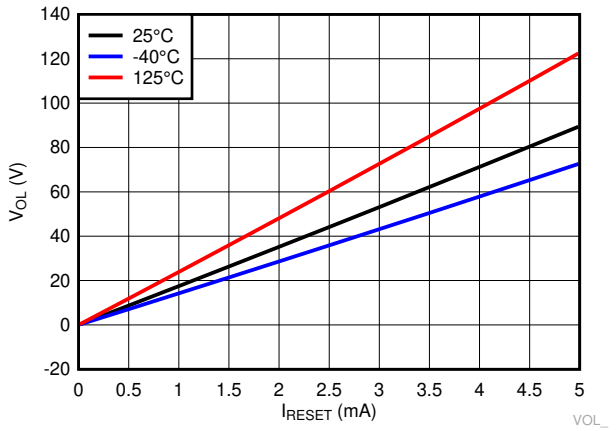


Figure 6-18. Low Level Output Voltage vs I_{RESET} for TPS3840PL49

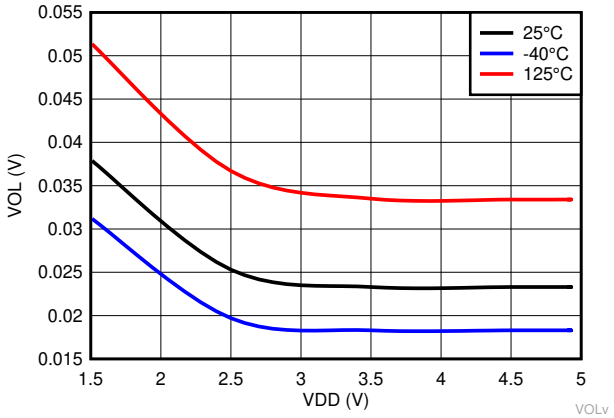


Figure 6-19. Low Level Output Voltage vs VDD for TPS3840PL49

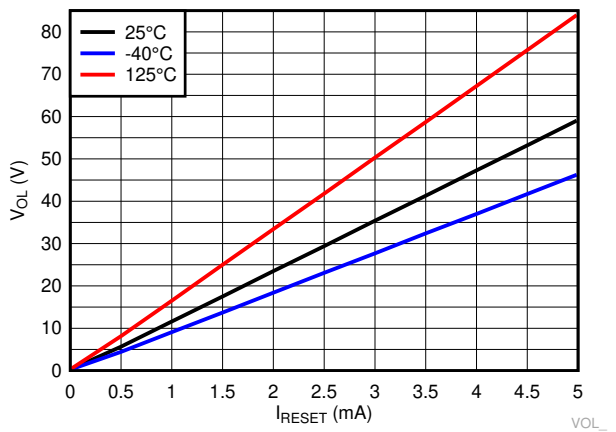


Figure 6-20. Low Level Output Voltage vs I_{RESET} for TPS3840PH49

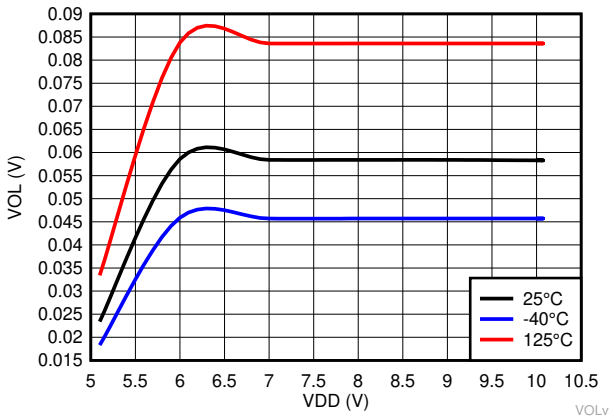


Figure 6-21. Low Level Output Voltage vs VDD for TPS3840PH49

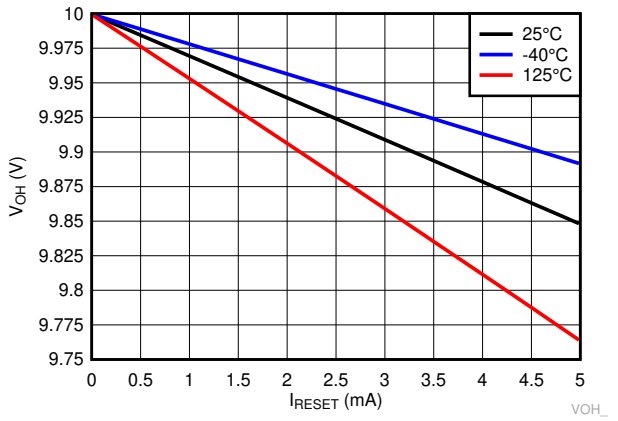


Figure 6-22. High Level Output Voltage vs I_{RESET} for TPS3840PL49

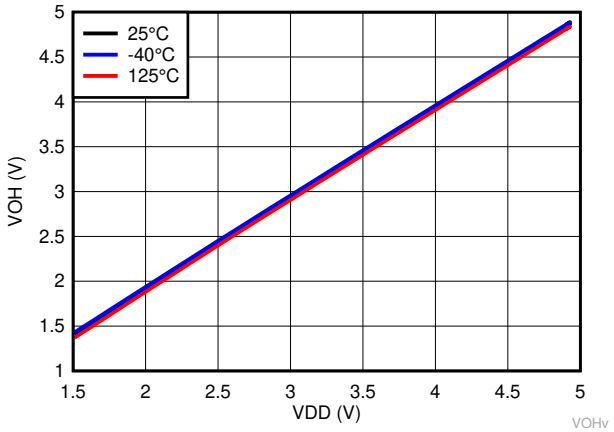


Figure 6-23. High Level Output Voltage over Temperature for TPS3840PL49

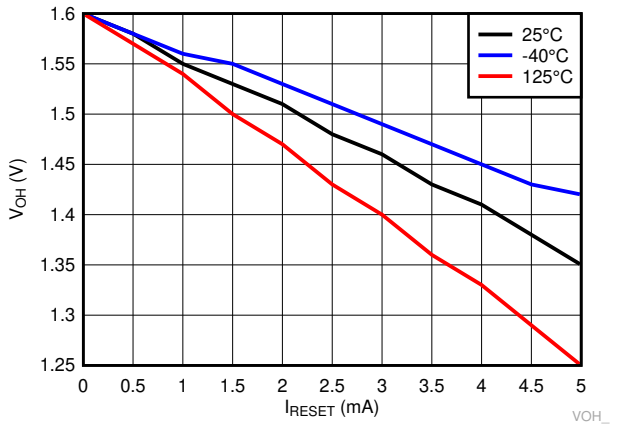


Figure 6-24. High Level Output Voltage vs I_{RESET} for TPS3840PH49

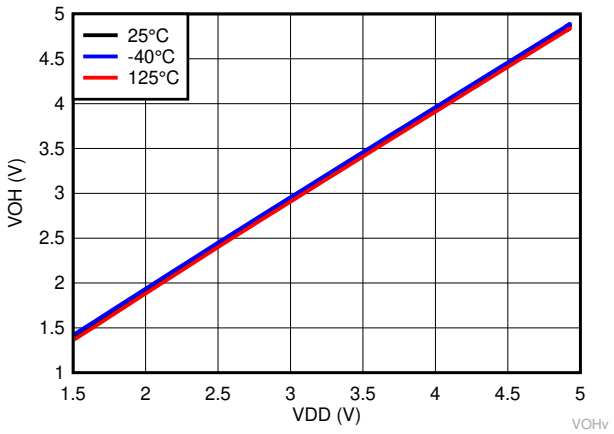


Figure 6-25. High Level Output Voltage over Temperature for TPS3840PH49

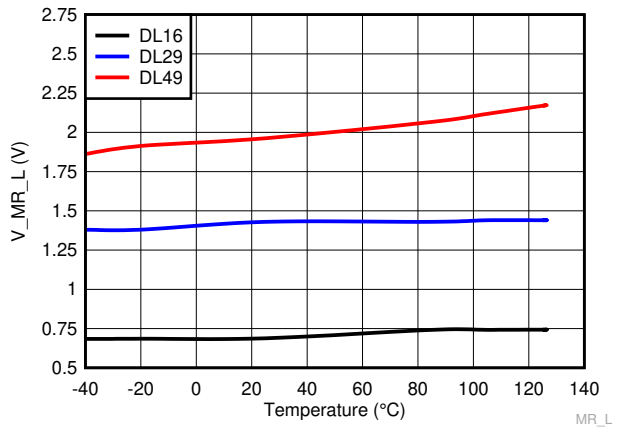


Figure 6-26. Manual Reset Logic Low Voltage Threshold over Temperature for TPS3840DLXX

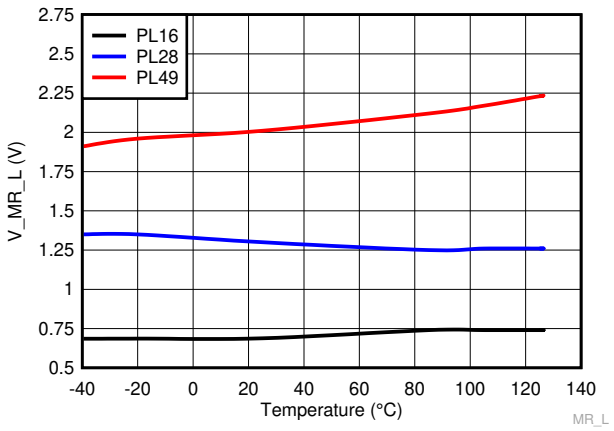


Figure 6-27. Manual Reset Logic Low Voltage Threshold over Temperature for TPS3840PLXX

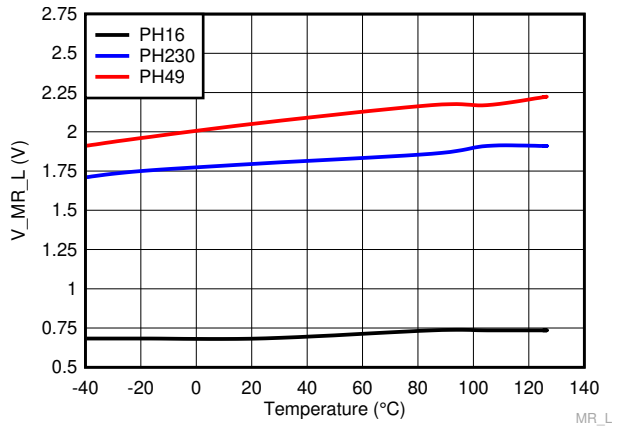


Figure 6-28. Manual Reset Logic Low Voltage Threshold over Temperature for TPS3840PHXX

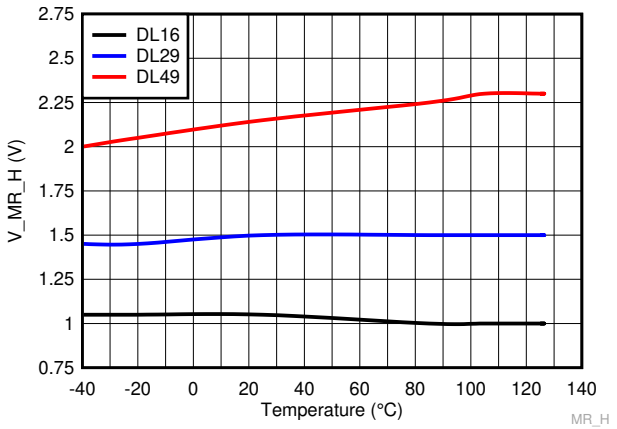


Figure 6-29. Manual Reset Logic High Voltage Threshold over Temperature for TPS3840DLXX

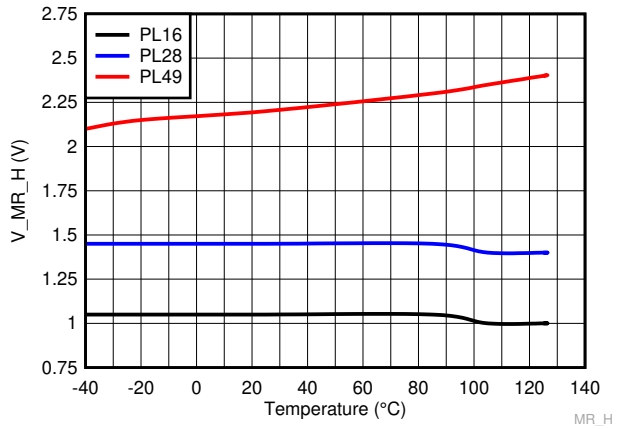


Figure 6-30. Manual Reset Logic High Voltage Threshold over Temperature for TPS3840PLXX

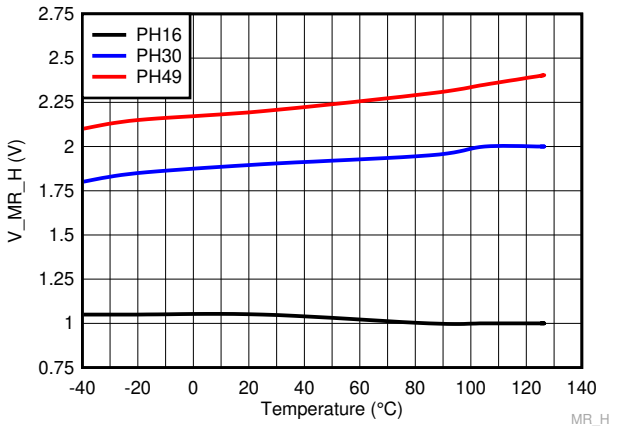


Figure 6-31. Manual Reset Logic High Voltage Threshold over Temperature for TPS3840PHXX

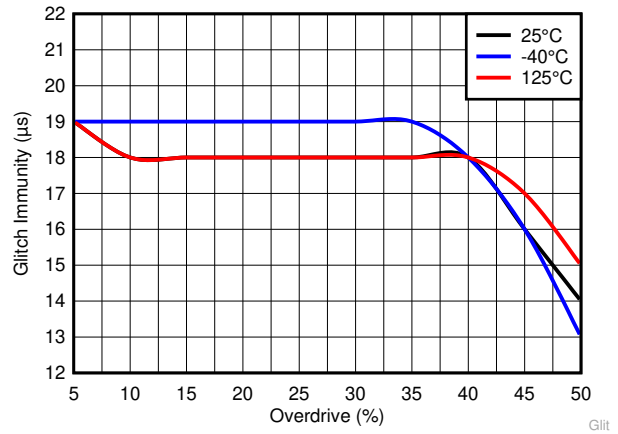


Figure 6-32. Glitch Immunity on V_{IT-} vs Overdrive (Data Taken with TPS3840PL28)

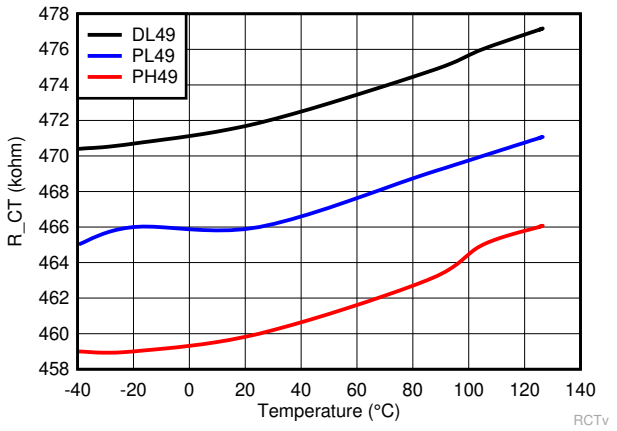


Figure 6-33. CT Pin Internal Resistance over Temperature

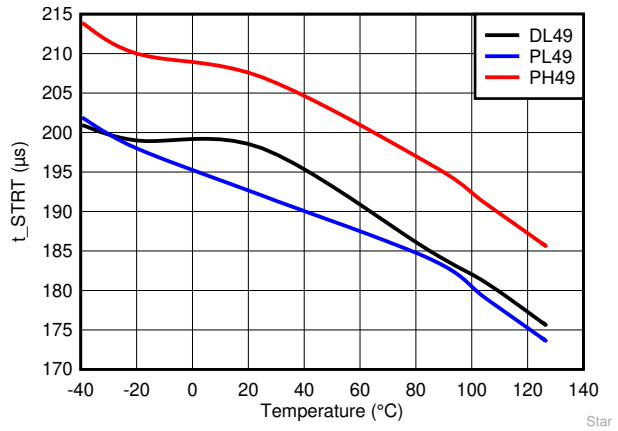


Figure 6-34. Startup Delay over Temperature

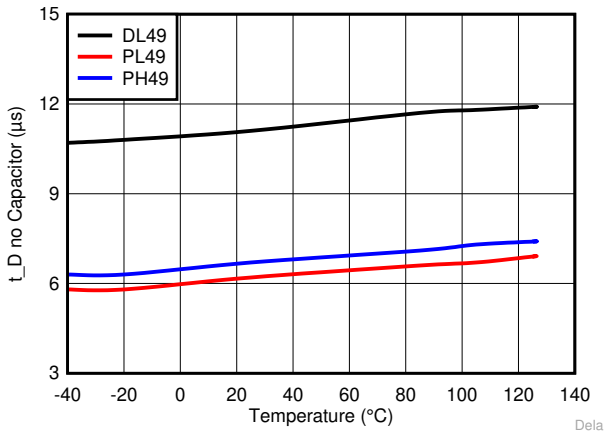


Figure 6-35. Reset Time Delay with No Capacitor over Temperature

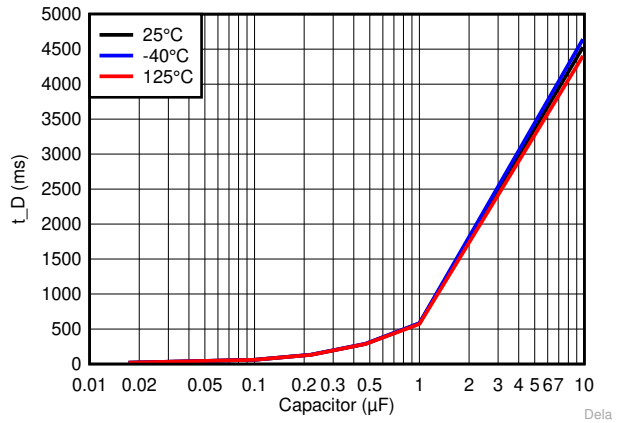


Figure 6-36. Reset Time Delay vs Capacitor Value (Data Taken with TPS3840PL16)

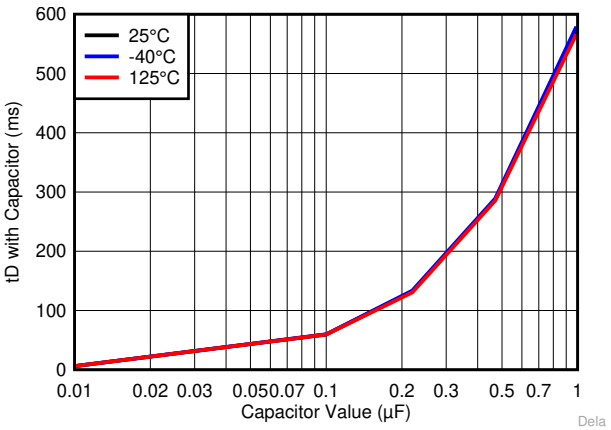


Figure 6-37. Reset Time Delay vs Small Capacitor Values (Data Taken with TPS3840PL16)

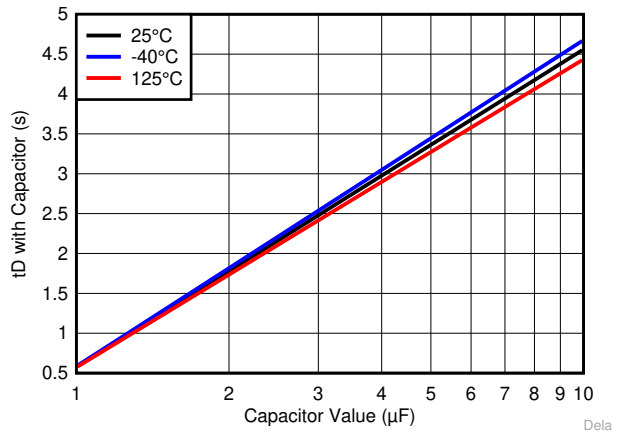


Figure 6-38. Reset Time Delay vs Large Capacitor Values (Data Taken with TPS3840PL16)

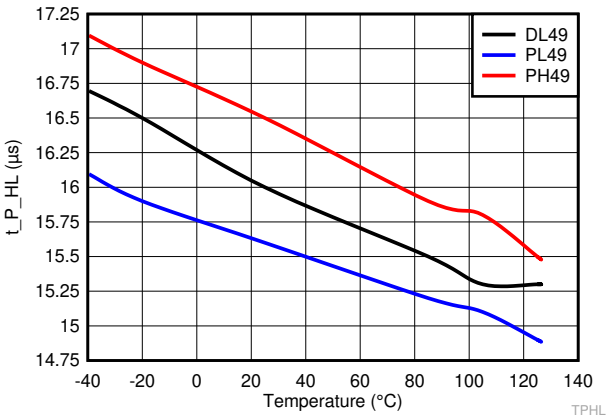


Figure 6-39. Propagation Detect Time Delay for VDD Falling Below V_{IT-} (High-to-Low) over Temperature

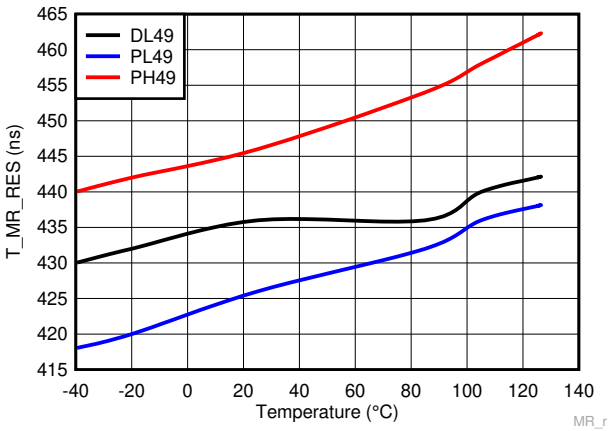


Figure 6-40. Propagation Time Delay from $\overline{MR}$ Asserted to Reset over Temperature

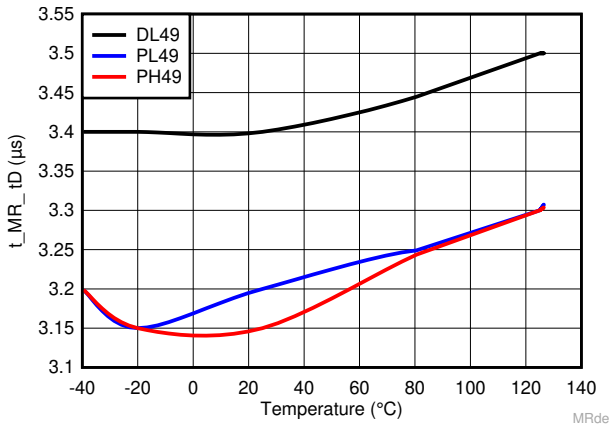


Figure 6-41. Propagation Time Delay from $\overline{MR}$ Release to Deasserted Reset over Temperature

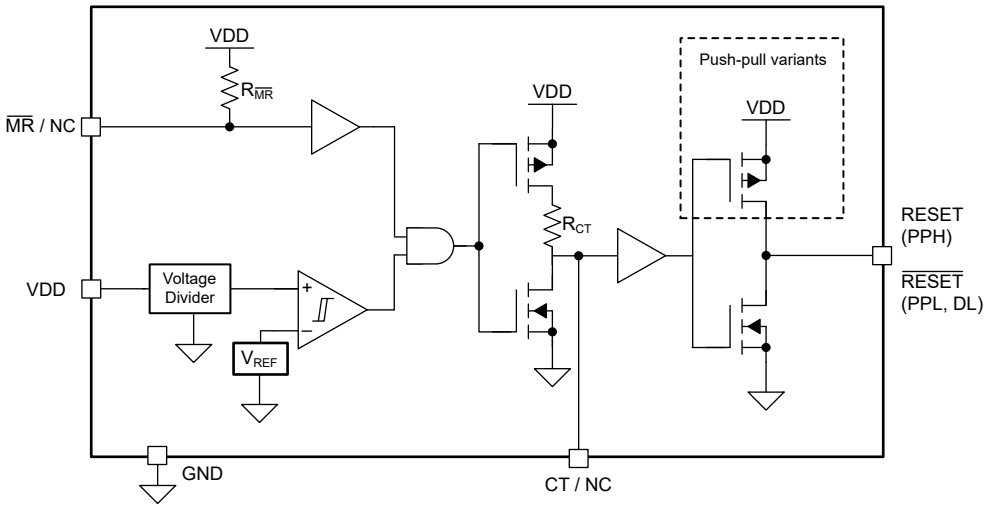
7 Detailed Description

7.1 Overview

The TPS3840 is a family of wide VDD and nano-quiescent current voltage detectors with fixed threshold voltage. TPS3840 features include programmable reset time delay using external capacitor, active-low manual reset, 1% typical monitor threshold accuracy with hysteresis and glitch immunity.

Fixed negative threshold voltages (V_{IT-}) can be factory set from 1.6 V to 4.9V (see Section 4 for available options). TPS3840 is available in SOT-23 5 pin industry standard package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage (VDD)

VDD pin is monitored by the internal comparator to indicate when VDD falls below the fixed threshold voltage. VDD also functions as the supply for the internal bandgap, internal regulator, state machine, buffers and other control logic blocks. Good design practice involve placing a 0.1uF to 1uF bypass capacitor at VDD input for noisy applications to ensure enough charge is available for the device to power up correctly.

7.3.1.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below V_{IT-} the output reset is asserted. When the voltage at the VDD pin goes above V_{IT-} plus hysteresis (V_{HYS}) the output reset is deasserted after t_D delay.

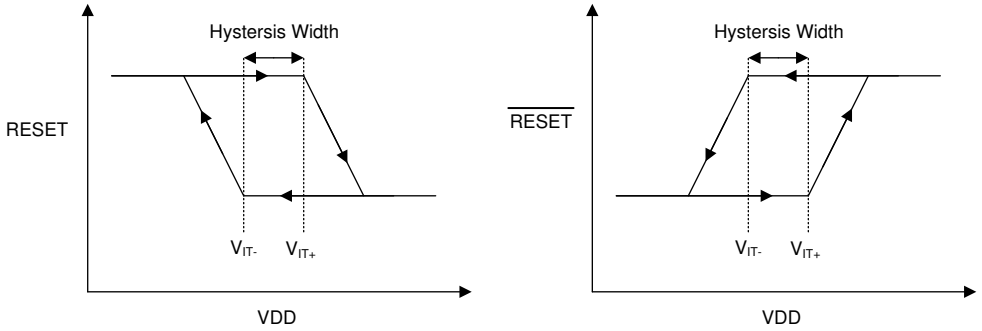


Figure 7-1. Hysteresis Diagram

7.3.1.2 VDD Transient Immunity

The TPS3840 is immune to quick voltage transients or excursion on VDD. Sensitivity to transients depends on both pulse duration and overdrive. Overdrive is defined by how much VDD deviates from the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 2.

$$\text{Overdrive} = \left|\left(\frac{V_{DD}}{V_{IT-}} - 1\right) \times 100\%\right| \quad (2)$$

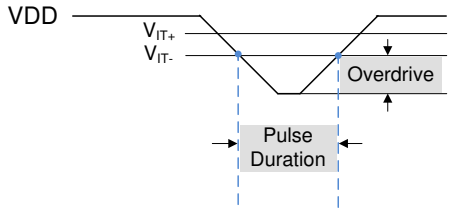


Figure 7-2. Overdrive vs Pulse Duration

7.3.2 User-Programmable Reset Time Delay

The reset time delay can be set to a minimum value of 50µs by leaving the CT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10µF delay capacitor. The reset time delay (t_D) can be programmed by connecting a capacitor no larger than 10µF between CT pin and GND.

The relationship between external capacitor (C_{CT_EXT}) in Farads at CT pin and the time delay (t_D) in seconds is given by Equation 3.

$$t_D = -\ln(0.29) \times R_{CT} \times C_{CT\_EXT} + t_D(\text{no cap}) \quad (3)$$

Equation 3 is simplified to Equation 4 by plugging R_{CT} and $t_{D(\text{no cap})}$ given in Section 6.5:

$$t_D = 618937 \times C_{CT\_EXT} + 50\mu s \quad (4)$$

Equation 5 solves for external capacitor value (C_{CT_EXT}) in units of Farads where t_D is in units of seconds.

$$C_{CT\_EXT} = \frac{(t_D - 50\mu s)}{618937} \quad (5)$$

The reset delay varies according to three variables: the external capacitor variance (C_{CT}), CT pin internal resistance (R_{CT}) provided in the Electrical Characteristics table, and a constant. The minimum and maximum variance due to the constant is shown in Equation 6 and Equation 7.

$$t_{D(\text{minimum})} = -\ln(0.36) \times R_{CT(\text{min})} \times C_{CT(\text{min})} + t_{D(\text{no cap, min})} \quad (6)$$

$$t_{D(\text{maximum})} = -\ln(0.26) \times R_{CT(\text{max})} \times C_{CT(\text{max})} + t_{D(\text{no cap, max})} \quad (7)$$

The recommended maximum delay capacitor for the TPS3840 is limited to 10µF as this ensures there is enough time for the capacitor to fully discharge when the reset condition occurs. When a voltage fault occurs, the previously charged up capacitor discharges, and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay capacitor begins charging from a voltage above zero volts and the reset delay is shorter than expected. Larger delay capacitors can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault.

7.3.3 Manual Reset ($\overline{MR}$) Input

The manual reset ($\overline{MR}$) input allows a processor GPIO or other logic circuits to initiate a reset. A logic low on $\overline{MR}$ with pulse duration longer than $t_{\overline{MR}\_RES}$ will causes reset output to assert. After $\overline{MR}$ returns to a logic high ($V_{\overline{MR}\_H}$) and VDD is above V_{IT+}, reset is deasserted after the user programmed reset time delay (t_D) expires.

If $\overline{MR}$ is not controlled externally, then $\overline{MR}$ can be left disconnected. If the logic signal controlling $\overline{MR}$ is less than VDD, then additional current flows from VDD into $\overline{MR}$ internally. For minimum current consumption, drive $\overline{MR}$ to either VDD or GND. $V_{\overline{MR}}$ must not be higher than VDD voltage.

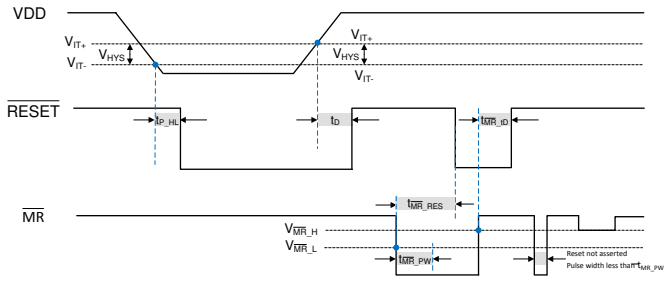


Figure 7-3. Timing Diagram $\overline{MR}$ and $\overline{RESET}$ (TPS3840DL)

7.3.4 Output Logic

7.3.4.1 $\overline{RESET}$ Output, Active-Low

$\overline{RESET}$ (Active-Low) applies to TPS3840D**L** (Open-Drain) and TPS3840P**L** (Push-Pull) hence the "**L**" in the device name. $\overline{RESET}$ remains high (deasserted) as long as VDD is above the negative threshold (V_{IT-}) and the $\overline{MR}$ pin is floating or above $V_{\overline{MR}\_H}$. If VDD falls below the negative threshold (V_{IT-}) or if $\overline{MR}$ is driven low, then $\overline{RESET}$ is asserted.

When $\overline{MR}$ is again logic high or floating and VDD rise above V_{IT+}, the delay circuit holds $\overline{RESET}$ low for the specified reset time delay (t_D). When the reset time delay has elapsed, the $\overline{RESET}$ pin goes back to logic high voltage (V_{OH}).

The TPS3840DL (Open-Drain) version, denoted with "**D**" in the device name, requires a pull-up resistor to hold $\overline{RESET}$ pin high. Connect the pull-up resistor to the desired pull-up voltage source and $\overline{RESET}$ can be pulled up to any voltage up to 10V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when selecting the pull-up resistor values. The pull-up resistor value determines the actual V_{OL}, the output capacitive loading, and the output leakage current ($I_{LKG(OD)}$).

The Push-Pull variants (TPS3840**P**L and TPS3840**P**H), denoted with "**P**" in the device name, does not require a pull-up resistor

7.3.4.2 RESET Output, Active-High

RESET (active-high), denoted with no bar above the pin label, applies only to TPS3840PH push-pull active-high version. RESET remains low (deasserted) as long as VDD is above the threshold (V_{IT-}) and the manual reset signal ($\overline{MR}$) is logic high or floating. If VDD falls below the negative threshold (V_{IT-}) or if $\overline{MR}$ is driven low, then RESET is asserted driving the RESET pin to high voltage (V_{OH}).

When $\overline{MR}$ is again logic high and VDD is above V_{IT+} the delay circuit holds RESET high for the specified reset time delay (t_D). When the reset time delay has elapsed, the RESET pin goes back to low voltage (V_{OL})

7.4 Device Functional Modes

Table 7-1 summarizes the various functional modes of the device. Logic high is represented by "H" and logic low is represented by "L".

Table 7-1. Truth Table

VDD	$\overline{MR}$	RESET	$\overline{RESET}$
VDD < V_{POR}	Ignored	Undefined	Undefined
V_{POR} < V_{DD} < V_{IT-} (1)	Ignored	H	L
VDD ≥ V_{IT-}	L	H	L
VDD ≥ V_{IT-}	H	L	H

Table 7-1. Truth Table (continued)

VDD	$\overline{MR}$	RESET	$\overline{RESET}$
VDD ≥ V_{IT-}	Floating	L	H

(1) When V_{DD} falls below $V_{DD(MIN)}$, undervoltage-lockout (UVLO) takes effect and output reset is held asserted until V_{DD} falls below V_{POR}.

7.4.1 Normal Operation (V_{DD} > $V_{DD(min)}$)

When VDD is greater than $V_{DD(min)}$, the reset signal is determined by the voltage on the VDD pin with respect to the trip point (V_{IT-}) and the logic state of $\overline{MR}$.

- $\overline{MR}$ high: the reset signal corresponds to VDD with respect to the threshold voltage.
- $\overline{MR}$ low: in this mode, the reset is asserted regardless of the threshold voltage.

7.4.2 VDD Between VPOR and $V_{DD(min)}$

When the voltage on VDD is less than the $V_{DD(min)}$ voltage, and greater than the power-on-reset voltage (V_{POR}), the reset signal is asserted.

7.4.3 Below Power-On-Reset (V_{DD} < V_{POR})

When the voltage on VDD is lower than V_{POR}, the device does not have enough bias voltage to internally pull the asserted output low or high and reset voltage level is undefined.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

8.2 Typical Application

8.2.1 Design 1: Dual Rail Monitoring with Power-Up Sequencing

A typical application for the TPS3840 is voltage rail monitoring and power-up sequencing as shown in Figure 8-1. The TPS3840 can be used to monitor any rail above 1.6V. In this design application, two TPS3840 devices monitor two separate voltage rails and sequences the rails upon power-up. The TPS3840PL30 is used to monitor the 3.3V main power rail and the TPS3840DL16 is used to monitor the 1.8V rail provided by the LDO for other system peripherals. The $\overline{\text{RESET}}$ output of the TPS3840PL30 is connected to the ENABLE input of the LDO. A reset event is initiated on either voltage supervisor when the VDD voltage is less than V_{IT-} or when $\overline{\text{MR}}$ is driven low by an external source.

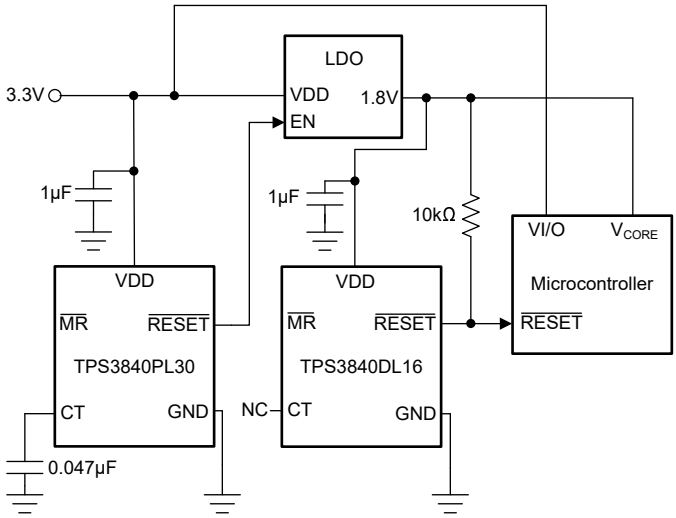


Figure 8-1. TPS3840 Voltage Rail Monitor and Power-Up Sequencer Design Block Diagram

8.2.1.1 Design Requirements

This design requires voltage supervision on two separate rails: 3.3V and 1.8V rails. The voltage rail needs to sequence upon power up with the 3.3V rail coming up first followed by the 1.8V rail at least 25ms after.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Two Rail Voltage Supervision	Monitor 3.3V and 1.8V rails	Two TPS3840 devices provide voltage monitoring with 1% accuracy with device options available in 0.1V variations
Voltage Rail Sequencing	Power up the 3.3V rail first followed by 1.8V rail 25ms after	The CT capacitor on TPS38240PL28 is set to 0.047 µF for a reset time delay of 29ms typical
Output logic voltage	3.3V Open-Drain	3.3V Open-Drain

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Maximum device current consumption	1µA	Each TPS3840 requires 350nA typical

8.2.1.2 Detailed Design Procedure

The primary constraint for this application is selecting the correct device to monitor the supply voltage of the microprocessor. The TPS3840 can monitor any voltage from 1.6V to 10V and is available in 0.1V increments. Depending on how far away from the nominal voltage rail the user wants the voltage supervisor to trigger determines the correct voltage supervisor variant to select. In this example, the first TPS3840 triggers when the 3.3V rail falls to 3.0V. The second TPS3840 triggers a reset when the 1.8V rail falls to 1.6V. The secondary constraint for this application is the reset time delay that must be at least 25ms to allow the microprocessor, and all other devices using the 3.3V rail, enough time to startup correctly before the 1.8V rail is enabled via the LDO. Because a minimum time is required, the user must account for capacitor tolerance. For applications with ambient temperatures ranging from –40°C to +125°C, C_{CT} can be calculated using R_{CT} and solving for C_{CT} in Equation 3. Solving Equation 3 for 25ms gives a minimum capacitor value of 0.04 µF which is rounded up to a standard value 0.047µF to account for capacitor tolerance.

A 1µF decoupling capacitor is connected to the VDD pin as a good analog design practice. The pull-up resistor is only required for the Open-Drain device variants and is calculated to maintain the $\overline{\text{RESET}}$ current within the ±5mA limit found in the *Section 6.3*: $R_{Pull\text{-}up} = V_{Pull\text{-}up} \div 5mA$. For this design, a standard 10kΩ pull-up resistor is selected to minimize current draw when $\overline{\text{RESET}}$ is asserted. Keep in mind the lower the pull-up resistor, the higher V_{OL}. The $\overline{\text{MR}}$ pin can be connected to an external signal if desired or left floating if not used due to the internal pull-up resistor to VDD.

8.2.1.3 Application Curves

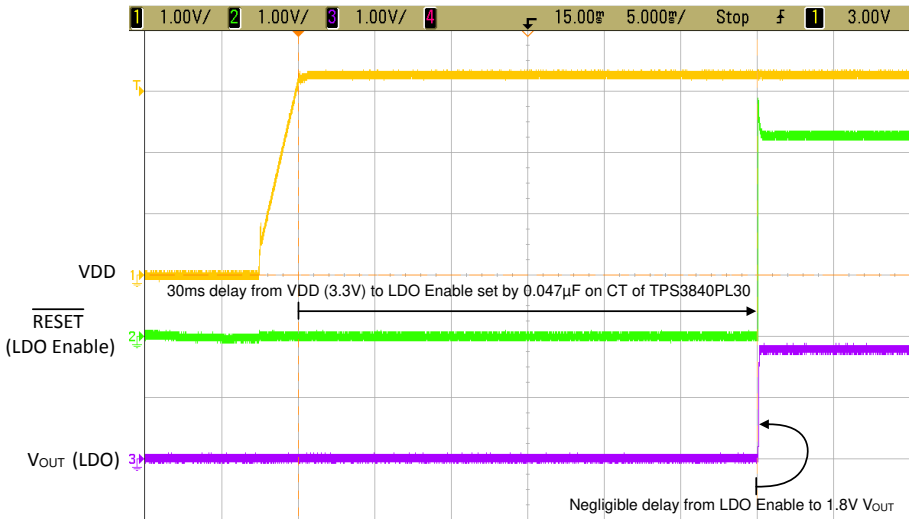


Figure 8-2. Startup Sequence Highlighting the Delay Between 3.3V and 1.8V Rails

8.2.2 Design 2: Battery Voltage and Temperature Monitor

A typical application for the TPS3840 is battery voltage and temperature monitoring. The TPS3840 is offered in active-low or active-high output topologies and can operate above or below the voltage threshold meaning the device can be used as an undervoltage monitor as shown in Figure 8-3 or overvoltage monitor as shown in Figure 8-4. The TPS3840 can be used to monitor any rail above 1.6V. In this design application, one TPS3840DL30 monitors the 3.3V battery voltage rail and triggers an active-low reset fault condition if the battery voltage falls below the 3V threshold. For overvoltage monitoring, another TPS3840DL30 monitors a 2.8V battery and triggers a logic high at the 3V threshold plus 100mV hysteresis so at 3.1V. Both applications monitor the battery temperature using TMP303, a push-pull, active-high temperature switch. A temperature fault is triggered

if the battery temperature falls outside of a defined window temperature range set by the TMP303 variant selected.

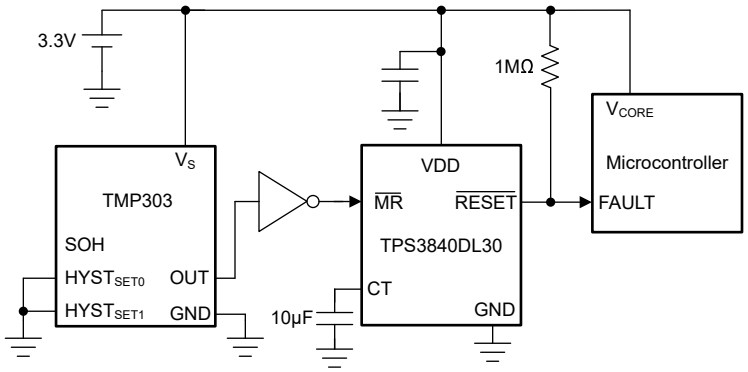


Figure 8-3. Low Battery Voltage and Window Temperature Monitoring Solution

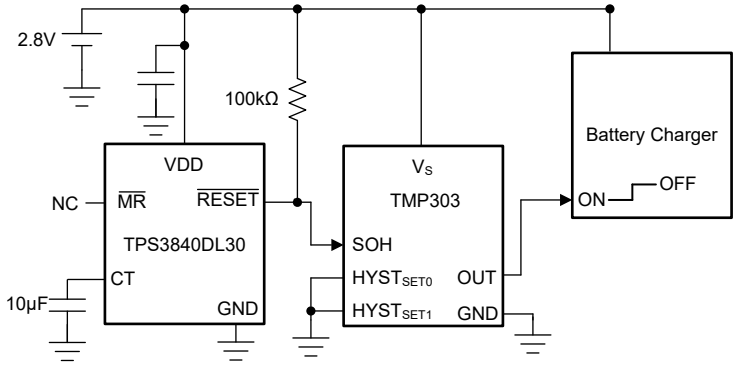


Figure 8-4. Overvoltage and Window Temperature Monitoring Solution

8.2.2.1 Design Requirements

This design requires voltage and temperature supervision on a battery voltage rail and the requirements can differ depending on if undervoltage or overvoltage monitoring is required. For this design, both requirements are considered to show the flexibility of the TPS3840 device. The first application example shown in Figure 8-3 uses TPS3840DL30, an open-drain active-low voltage supervisor to monitoring undervoltage and TMP303, a push-pull active-high window temperature switch to monitor under and over temperature. For the undervoltage application, the TPS3840DL30 is operating in the inactive logic high region so an overvoltage fault occurs when the battery voltage falls below V_{IT-} = 3.0V or when the battery temperature is outside the range from 0°C to 60°C. The second application example uses TPS3840DL30 operating in the active-low region to monitor overvoltage and TMP303 to monitor under and over temperature. For the overvoltage requirement, the fault occurs when the battery voltage rises above 3.1V or when the battery temperature is outside the range from 0°C to 60°C.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Battery Voltage Supervision	Monitor 3.3V battery for undervoltage condition	TPS3840 provides voltage monitoring with 1% accuracy with device options available in 0.1V variations. TPS3840DL30 triggers a reset when VDD falls below 3V. TPS3840PH30 triggers a reset when VDD rises above 3V plus hysteresis setting the overvoltage threshold to 3.1V.
	Monitor 2.8V battery for overvoltage condition	
Battery Temperature Supervision	Monitor battery temperature between 0°C and 60°C with 1°C resolution for undervoltage design	TMP303A monitors temperature within 0°C to 60°C with 1°C resolution. Note this is a push-pull, active-high output device.
Output Topology	Undervoltage: Active-Low, Open-Drain	TPS3840 is offered in Active-Low Open-drain, Active-Low Push-Pull, and Active-High Push-Pull topologies
	Overvoltage: Active-High, Push-Pull	

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Maximum device current consumption	10µA	TPS3840 requires 350nA (typical) and TMP303 requires 3.5µA (typical)
Delay when returning from fault condition	Delay of at least 6 seconds when returning from the fault to prevent operation in fault conditions	C_{CT} = 10µF sets 6.18 second delay

8.2.2.2 Detailed Design Procedure

The primary constraint for this application is selecting the correct device to monitor the battery supply voltage. The TPS3840 can monitor any voltage from 1.6V to 10V and is available in 0.1V increments. Depending on how far away from the nominal voltage rail the user wants the voltage supervisor to trigger determines the correct voltage supervisor variant to select. In this design example, the TPS3840DL30 is selected for both the undervoltage and overvoltage monitoring. For undervoltage monitoring, the undervoltage fault occurs when the 3.3V rail falls to 3V and for the overvoltage monitoring, the overvoltage fault occurs when the 2.8V rail rises above the 3V threshold (V_{IT-}) plus 100mV hysteresis (V_{HYS}). It is important to note that in the undervoltage application, the TPS3840 $\overline{\text{RESET}}$ output is logic high during normal conditions whereas in the overvoltage application, the TPS3840 $\overline{\text{RESET}}$ output is logic low during normal conditions which is the reason a single device can be used for either type of monitoring depending on the logic required at the output. The opposite $\overline{\text{RESET}}$ output logic is offered in the push-pull, active-high device TPS3840PH noted with the RESET output. The secondary constraint for this application is the battery temperature monitoring accomplished by the TMP303A. Typical Lithium Ion battery discharge temperature range is 0°C to 60°C which is accomplished by the 'A' variant of TMP303A. The TMP303A triggers a fault to the $\overline{\text{MR}}$ pin of the TPS3840 or directly to the battery charger whenever the temperature is outside of the temperature range. The TMP303A offers 1°C resolution to meet the high resolution requirement. Because the undervoltage monitor design uses TMP303A, a push-pull active-high output device, an additional inverter is required before the $\overline{\text{MR}}$ pin because during normal operation, the TMP303 output is low but the $\overline{\text{MR}}$ pin must be logic high during normal operation. If using two TPS3840 devices for both undervoltage and overvoltage monitoring on the same battery, only one single temperature monitoring device is required. The last constraint is the $\overline{\text{RESET}}$/RESET time delay set by C_{CT}. For applications with ambient temperatures ranging from –40°C to +125°C, C_{CT} can be calculated using R_{CT} and solving for C_{CT} in Equation 3. By selecting a standard 10% capacitor value of 10µF ensures the $\overline{\text{RESET}}$/RESET time delay is at least 6 seconds. Note: active-low devices use the output label $\overline{\text{RESET}}$ and active-high devices use the output label RESET.

A 0.1µF decoupling capacitor is connected to the VDD pin as a good analog design practice. The pull-up resistor is only required for the Open-Drain device variants and is calculated to maintain the $\overline{\text{RESET}}$ current within the ±5mA limit found in the *Section 6.3*: $R_{Pull\text{-}up} = V_{Pull\text{-}up} \div 5mA$. For this design, a 1MΩ pull-up resistor is selected to minimize current draw when $\overline{\text{RESET}}$ is asserted and to prevent the battery from unnecessary discharge. Keep in mind the lowering the pull-up resistor, increases V_{OL} and I_{OUT}. The $\overline{\text{MR}}$ pin is used for a second fault condition provided by the temperature switch.

8.2.3 Design 3: Fast Start Undervoltage Supervisor with Level-shifted Input

A typical application for the TPS3840 is a fast startup undervoltage supervisor that operates with an input power supply higher than the recommended maximum of 10V through the use of a resistor divider at the input as shown in Figure 8-5. The TPS3840 can be used to monitor any rail above 1.6V and only requires maximum 350µs upon startup before the device can begin monitoring a voltage. In this design application, a TPS3840 monitors a 12V rail and triggers a reset fault condition if the voltage rail voltage drops below 10V using a TPS3840 device with V_{IT-} of 4.9V. This design also accounts for a wide input range in the case the 12V rail rises higher, the resistor divider is set so that the voltage at the VDD pin never exceeds 10V. The resistor values must not be so large that the external resistor divider affects the accuracy or operation of the device. TPS3840 is available in both active-low and active-high topologies providing the flexibility to monitor undervoltage or overvoltage with either output logic. This design uses the active-low, open-drain TPS3840DL49 variant so that when the undervoltage condition occurs, that is when the voltage at VDD pin falls below the voltage threshold set by the external resistor divider, the output transitions to logic-low and can be used to flag an undervoltage condition or used to connect to the ENABLE of the next device to shut it off as a logic low on an ENABLE pin typically disables the device. In this design, the output of the TPS3840 simply connects to a MCU to flag an undervoltage condition.

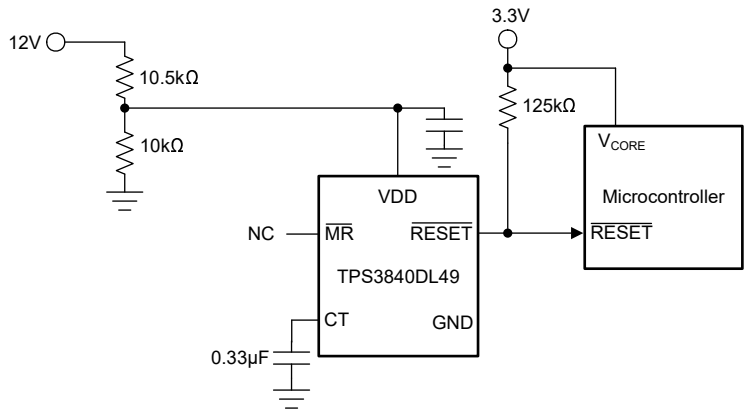


Figure 8-5. Fast Start Undervoltage Supervisor with Level-shifted Input

8.2.3.1 Design Requirements

This design requires voltage supervision on a 12V power supply voltage rail with possibility of the 12V rail rising up as high as 18V. The undervoltage fault occurs when the power supply voltage drops below 10V.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Power Rail Voltage Supervision	Monitor 12V power supply for undervoltage condition, trigger a undervoltage fault at 10V.	TPS3840 provides voltage monitoring with 1% accuracy with device options available in 0.1V variations. The TPS3840 monitors voltages above 1.6V.
Maximum Input Power	Operate with power supply input up to 18V.	The TPS3840 limits VDD to 10V but can monitor voltages higher than the maximum VDD voltage with the use of an external resistor divider.
Output logic voltage	3.3V Open-Drain	3.3V Open-Drain
Maximum device current consumption	35µA when power supply is at 18V maximum	TPS3840 requires 350nA (typical) and the external resistor divider will also consume current. There is a tradeoff between current consumption and voltage monitor accuracy but generally set the resistor divider to consume 100 times current into VDD.
Voltage Monitor Accuracy	Typical voltage monitor accuracy of 2.5%. This allows the voltage threshold to range from 11.75V to 10.25V.	The TPS3840 has 1% typical voltage monitor accuracy. By decreasing the ratio of resistor values, the resistor divider consumes more current but the accuracy increases. The resistor tolerance also needs to be accounted for.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Delay when returning from fault condition	$\overline{\text{RESET}}$ delay of at least 200ms when returning from a undervoltage fault.	C_{CT} = 0.33µF sets 204ms delay

8.2.3.2 Detailed Design Procedure

The primary constraint for this application is monitoring a 12V rail while preventing the VDD pin on TPS3840 from exceeding the recommended maximum of 10V. This is accomplished by sizing the resistor divider so that when the 12V rail drops to 10V, the VDD pin for TPS3840 is at 4.9V which is the V_{IT-} threshold for triggering a undervoltage condition for TPS3840DL49 as shown in Equation 8.

$$V_{rail\_trigger} = V_{IT-} \times \left(R_{top} + R_{bottom}\right) \div R_{bottom} \quad (8)$$

where $V_{rail\_trigger}$ is the trigger voltage of the rail being monitored, V_{IT-} is the falling threshold on the VDD pin of TPS3840, and R_{top} and R_{bottom} are the top and bottom resistors of the external resistor divider. Be sure to size the resistor values such that the current through the external resistor divider is much greater than IDD to preserve voltage monitoring accuracy. V_{IT-} is fixed per device variant and is 4.9V for TPS3840DL49. Substituting in the values from Figure 8-5, the undervoltage trigger threshold for the rail is set to 10.045V.

Since the undervoltage trigger of 10V on the rail corresponds to 4.9V undervoltage threshold trigger of the TPS3840 device, there is plenty of room for the rail to rise up while maintaining less than 10V on the VDD pin of the TPS3840. Equation 9 shows the maximum rail voltage that still meets the 10V maximum at the VDD pin for TPS3840.

$$V_{rail\_max} = 10 \times (10500 + 10000) \div 10000 = 20.5V \quad (9)$$

This means the monitored voltage rail can go as high as 20.5V and still not violate the recommended maximum for the VDD pin on TPS3840. This is useful when monitoring a voltage rail that has a wide range that can go much higher than the nominal rail voltage such as in this case with the specification that the 12V rail can go as high as 18V. Notice that the resistor values selected are less than 100kΩ to preserve the accuracy set by the internal resistor divider. Good design practice recommends using a 0.1µF capacitor on the VDD pin and this capacitance can require an increase when using an external resistor divider.

8.2.4 Design 4: Voltage Monitor with Back-up Battery Switchover

A typical application for the TPS3840 is to monitor a voltage rail and switch the power to a back-up battery if the main supply is in undervoltage condition. Because systems that use a back-up battery tend to require low quiescent current, TPS3840 serves as the perfect solution as this device only requires 350nA typically. The TPS3840 monitors the main power rail via the VDD pin and when the main power rail falls, the $\overline{\text{RESET}}$ output asserts causing a switch to close on the back-up battery rail. The diodes provide an ORing logic function to prevent reverse leakage and to allow either rail to connect to the output depending on the status of the main voltage rail.

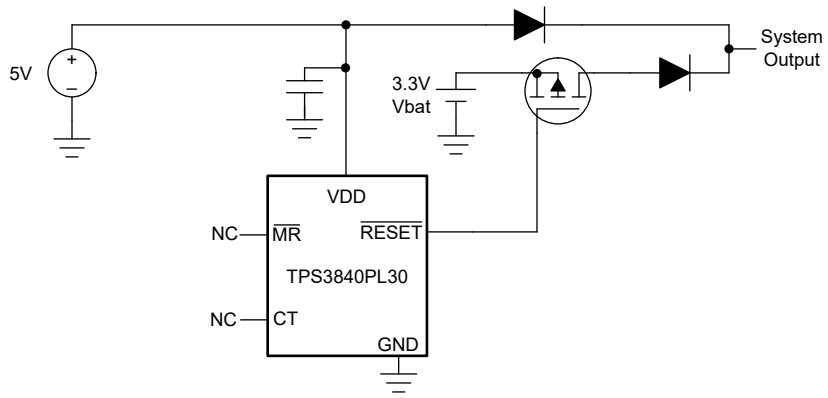


Figure 8-6. Voltage Monitor with Back-up Battery Switchover Solution

8.2.4.1 Design Requirements

This design requires voltage supervision on a 5V main supply voltage rail and when the main rail fails, switch to a back-up battery supply to prevent complete power loss in the system. The System Output must remain above 1.8V even when the main supply completely fails. The design requires less than 500nA of total current consumption and must prevent battery leakage when the battery is not being used. When the system is using the back-up battery and the main supply voltage rail comes back up, the system must switch back to the main power supply in less than 100µs to save battery power.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Main Supply Voltage Supervision	Monitor 5V main supply for undervoltage condition. When main supply drops below 3V, switch to back-up battery.	TPS3840 provides voltage monitoring with 1% accuracy with device options available in 0.1V variations. This design uses TPS3840PL30 to set the undervoltage trigger at 3V.
Back-up Battery Switchover	When undervoltage occurs on the main supply voltage rail, switch to the back-up batter.	When undervoltage occurs on the main supply rail, the PMOS switch closes allowing the back-up battery to connect to the system output. The diodes prevent reverse leakage and allow either power supply to connect to the system output.
Main Power Supply to Back-up Battery Switch Response Time	No more than 50µs to switch to the back-up battery when the main power supply falls to undervoltage condition.	TPS3840 provides a propagation delay for VDD falling below the undervoltage threshold (t_{P_HL}) of 50µs maximum to meet the requirement.
Back-up Battery to Main Power Supply Switch Back Response Time	Less than 100µs when switching from back-up battery back to main power supply when undervoltage condition is removed.	By leaving $\overline{MR}$ disconnected, the $\overline{RESET}$ delay is set to a maximum of 50µs to meet the requirement.
Device Current Consumption	500nA	TPS3840 requires 350nA (typical)
System Output Voltage	System Output must remain above 1.8V in all cases	When the main 5V rail is connected, the System Output is the rail voltage minus a diode voltage drop so at least 3V - 0.7V ≅ 2.3V. When the voltage rail drops below 3V, the back-up battery switches into the system and the System Output becomes the battery voltage minus a diode voltage drop so 3.3V - 0.7V ≅ 2.6V. The threshold at which the battery switches into the system directly depends on the TPS3840 variant selected.

8.2.4.2 Detailed Design Procedure

The primary constraints for this application are selecting the correct device variant for the monitored voltage and deciding the preferred solution to switch the back-up battery in and out of the system. For this design, the TPS3840PL30 provides an active-low, push-pull output topology that turns on the PFET when the 5V rail monitored by VDD drops to 3.0V. The diodes logically OR the power supply with the back-up battery and prevents reverse current leakage. Using this solution, the System Output remains above 1.8V in all circumstances unless both the 5V rail and back-up battery fail. The System Output voltage follows the 5V rail minus a diode drop until the 5V rail drops to 3V then the back-up battery switches into the system providing 3.3V minus a diode drop to the System Output. When the 5V rail comes back above 3.1V accounting for hysteresis, the PFET turns off to disconnect the back-up battery from the system. Since this design disconnects the battery when not being used, this solution maximizes battery life.

8.2.5 Application Curve: TPS3840EVM

These application curves are taken with the *TPS3840EVM*. Please see the *TPS3840EVM User Guide* for more information.

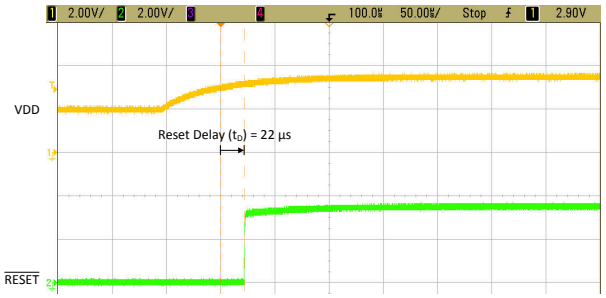


Figure 8-7. TPS3840EVM $\overline{\text{RESET}}$ Time Delay (t_D) with No Capacitor

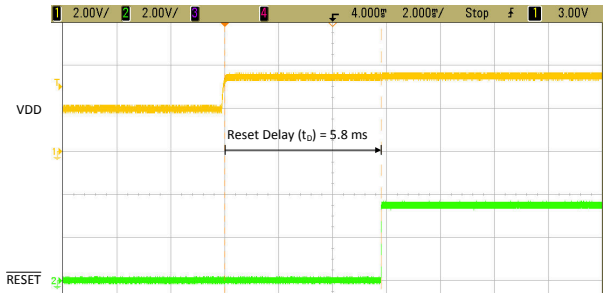


Figure 8-8. TPS3840EVM $\overline{\text{RESET}}$ Time Delay (t_D) with 0.01-µF Capacitor

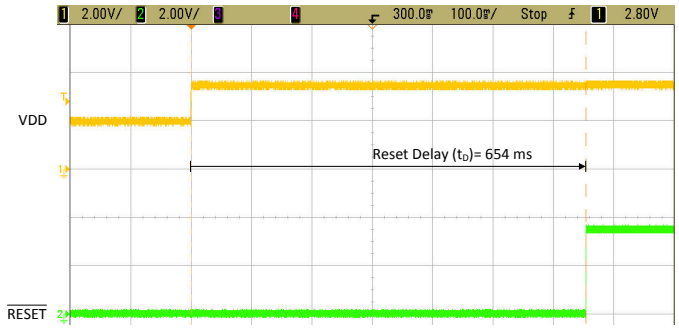


Figure 8-9. TPS3840EVM $\overline{\text{RESET}}$ Time Delay (t_D) with 1-µF Capacitor

8.3 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range from 1.5V to 10V. TI recommends an input supply capacitor between the VDD pin and GND pin. This device has a 12V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 12V, additional precautions must be taken.

8.4 Layout

8.4.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a minimum 0.1µF ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CT pin, then minimize parasitic capacitance on this pin so the rest time delay is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a >0.1µF ceramic capacitor as near as possible to the VDD pin.
- If a C_{CT} capacitor is used, place these components as close as possible to the CT pin. If the CT pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin to <5pF.
- Place the pull-up resistors on $\overline{\text{RESET}}$ pin as close to the pin as possible.
- For V_{DD} slew rate > 100mV/µs, increase input capacitor and pull-up resistor for OD variants.

8.4.2 Layout Example

The layout example in Figure 8-10 shows how the TPS3840 is laid out on a printed circuit board (PCB) with a user-defined delay.

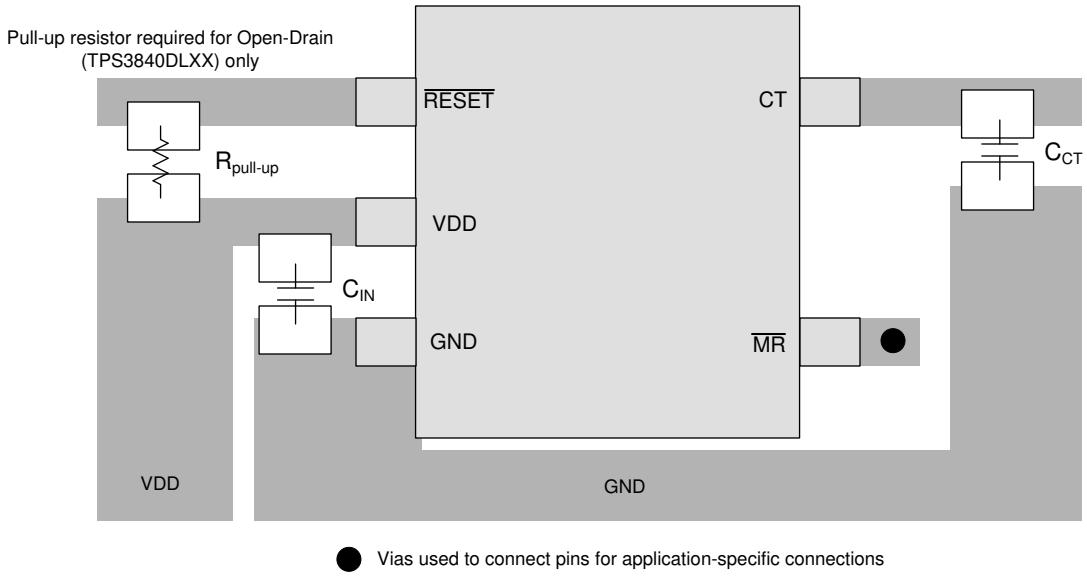


Figure 8-10. TPS3840 Recommended Layout

9 Device and Documentation Support

9.1 Device Nomenclature

Table 9-1 shows how to decode the function of the device based on its part number

Table 9-1. Device Naming Convention

DESCRIPTION	NOMENCLATURE	VALUE
Part number	TPS3840	TPS3840
Variant code (Output Topology)	DL	Open-Drain, Active-Low
	PH	Push-Pull, Active-High
	PL	Push-Pull, Active-Low
Detect Voltage Option	## (two characters)	Example: 16 stands for 1.6V threshold
Package	DBV	SOT23-5
Reel	R	Large Reel

Table 9-2 shows the possible variants of the TPS3840. Contact Texas Instruments for details and availability of other options shown; minimum order quantities apply.

Table 9-2. Device Threshold

PRODUCT			VOLTAGE THRESHOLD (V_{IT-})	HYSTERESIS (V_{HYST})
OPEN-DRAIN, ACTIVE-LOW	PUSH-PULL, ACTIVE-LOW	PUSH-PULL, ACTIVE-HIGH	TYP (V)	TYP (V)
TPS3840DL16	TPS3840PL16	TPS3840PH16	1.6	0.100
TPS3840DL17	TPS3840PL17	TPS3840PH17	1.7	0.100
TPS3840DL18	TPS3840PL18	TPS3840PH18	1.8	0.100
TPS3840DL19	TPS3840PL19	TPS3840PH19	1.9	0.100
TPS3840DL20	TPS3840PL20	TPS3840PH20	2.0	0.100
TPS3840DL21	TPS3840PL21	TPS3840PH21	2.1	0.100
TPS3840DL22	TPS3840PL22	TPS3840PH22	2.2	0.100
TPS3840DL23	TPS3840PL23	TPS3840PH23	2.3	0.100
TPS3840DL24	TPS3840PL24	TPS3840PH24	2.4	0.100
TPS3840DL25	TPS3840PL25	TPS3840PH25	2.5	0.100
TPS3840DL26	TPS3840PL26	TPS3840PH26	2.6	0.100
TPS3840DL27	TPS3840PL27	TPS3840PH27	2.7	0.100
TPS3840DL28	TPS3840PL28	TPS3840PH28	2.8	0.100
TPS3840DL29	TPS3840PL29	TPS3840PH29	2.9	0.100
TPS3840DL30	TPS3840PL30	TPS3840PH30	3.0	0.100
TPS3840DL31	TPS3840PL31	TPS3840PH31	3.1	0.200
TPS3840DL32	TPS3840PL32	TPS3840PH32	3.2	0.200
TPS3840DL33	TPS3840PL33	TPS3840PH33	3.3	0.200
TPS3840DL34	TPS3840PL34	TPS3840PH34	3.4	0.200
TPS3840DL35	TPS3840PL35	TPS3840PH35	3.5	0.200
TPS3840DL36	TPS3840PL36	TPS3840PH36	3.6	0.200
TPS3840DL37	TPS3840PL37	TPS3840PH37	3.7	0.200
TPS3840DL38	TPS3840PL38	TPS3840PH38	3.8	0.200
TPS3840DL39	TPS3840PL39	TPS3840PH39	3.9	0.200
TPS3840DL40	TPS3840PL40	TPS3840PH40	4.0	0.200
TPS3840DL41	TPS3840PL41	TPS3840PH41	4.1	0.200
TPS3840DL42	TPS3840PL42	TPS3840PH42	4.2	0.200

Table 9-2. Device Threshold (continued)

PRODUCT			VOLTAGE THRESHOLD (V_{IT-})	HYSTERESIS (V_{HYST})
OPEN-DRAIN, ACTIVE-LOW	PUSH-PULL, ACTIVE-LOW	PUSH-PULL, ACTIVE-HIGH	TYP (V)	TYP (V)
TPS3840DL43	TPS3840PL43	TPS3840PH43	4.3	0.200
TPS3840DL44	TPS3840PL44	TPS3840PH44	4.4	0.200
TPS3840DL45	TPS3840PL45	TPS3840PH45	4.5	0.200
TPS3840DL46	TPS3840PL46	TPS3840PH46	4.6	0.200
TPS3840DL47	TPS3840PL47	TPS3840PH47	4.7	0.200
TPS3840DL48	TPS3840PL48	TPS3840PH48	4.8	0.200
TPS3840DL49	TPS3840PL49	TPS3840PH49	4.9	0.200

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2020) to Revision E (May 2026) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Updated hysteresis range designator from < to ≤ 1
- Updated Device Threshold table to reflect correct device hysteresis 30

Changes from Revision C (August 2019) to Revision D (January 2020) — **Page**

- Deleted Device Comparison table 3
- Added Device Nomenclature figure 3

- Changed µF to Farads to fix the units for the delay equation.....18

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3840DL16DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL16
TPS3840DL16DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DL16
TPS3840DL16DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL16
TPS3840DL16DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL16
TPS3840DL17DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL17
TPS3840DL17DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DL17
TPS3840DL18DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL18
TPS3840DL18DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL18
TPS3840DL19DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL19
TPS3840DL19DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL19
TPS3840DL20DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL20
TPS3840DL20DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DL20
TPS3840DL22DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL22
TPS3840DL22DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DL22
TPS3840DL24DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL24
TPS3840DL24DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL24
TPS3840DL25DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL25
TPS3840DL25DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DL25
TPS3840DL27DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL27
TPS3840DL27DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL27
TPS3840DL28DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL28
TPS3840DL28DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DL28
TPS3840DL29DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL29
TPS3840DL29DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DL29
TPS3840DL30DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL30
TPS3840DL30DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL30
TPS3840DL30DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL30
TPS3840DL30DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL30
TPS3840DL31DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL31

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3840DL31DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL31
TPS3840DL35DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL35
TPS3840DL35DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL35
TPS3840DL40DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL40
TPS3840DL40DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL40
TPS3840DL42DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL42
TPS3840DL42DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL42
TPS3840DL44DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL44
TPS3840DL44DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL44
TPS3840DL45DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL45
TPS3840DL45DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DL45
TPS3840DL46DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL46
TPS3840DL46DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL46
TPS3840DL49DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL49
TPS3840DL49DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DL49
TPS3840PH18DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH18
TPS3840PH18DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PH18
TPS3840PH19DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH19
TPS3840PH19DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PH19
TPS3840PH27DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH27
TPS3840PH27DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PH27
TPS3840PH30DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH30
TPS3840PH30DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PH30
TPS3840PH40DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH40
TPS3840PH40DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PH40
TPS3840PH45DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH45
TPS3840PH45DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PH45
TPS3840PH49DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH49
TPS3840PH49DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PH49
TPS3840PL16DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL16
TPS3840PL16DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PL16

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3840PL18DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL18
TPS3840PL18DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL18
TPS3840PL20DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL20
TPS3840PL20DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL20
TPS3840PL25DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL25
TPS3840PL25DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL25
TPS3840PL26DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL26
TPS3840PL26DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL26
TPS3840PL27DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL27
TPS3840PL27DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL27
TPS3840PL27DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL27
TPS3840PL27DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL27
TPS3840PL28DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL28
TPS3840PL28DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL28
TPS3840PL29DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL29
TPS3840PL29DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL29
TPS3840PL30DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL30
TPS3840PL30DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL30
TPS3840PL31DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL31
TPS3840PL31DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PL31
TPS3840PL33DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL33
TPS3840PL33DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PL33
TPS3840PL34DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL34
TPS3840PL34DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL34
TPS3840PL40DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL40
TPS3840PL40DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL40
TPS3840PL41DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL41
TPS3840PL41DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL41
TPS3840PL42DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL42
TPS3840PL42DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL42
TPS3840PL43DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL43

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3840PL43DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PL43
TPS3840PL44DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PL44
TPS3840PL44DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PL44
TPS3840PL45DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL45
TPS3840PL45DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL45
TPS3840PL45DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL45
TPS3840PL45DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL45
TPS3840PL48DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL48
TPS3840PL48DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PL48

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3840 :

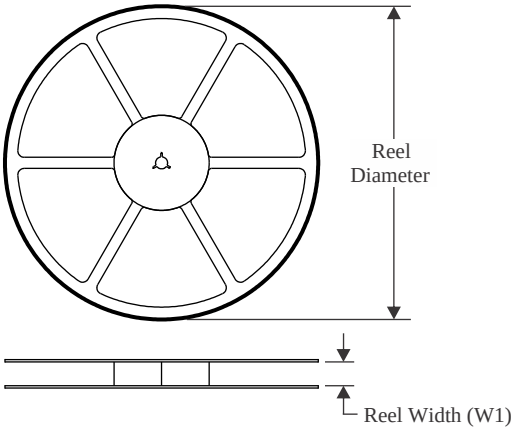
- Automotive : TPS3840-Q1

NOTE: Qualified Version Definitions:

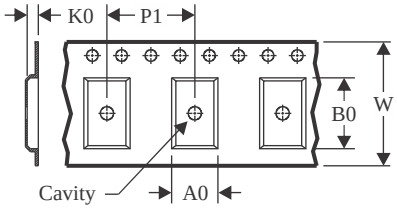
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

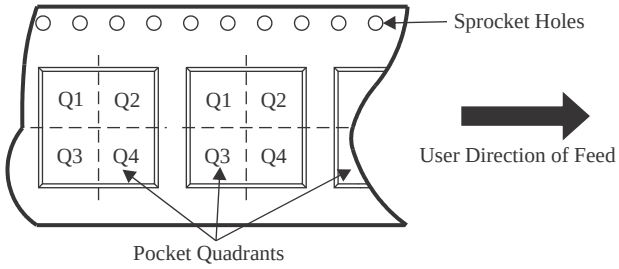


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



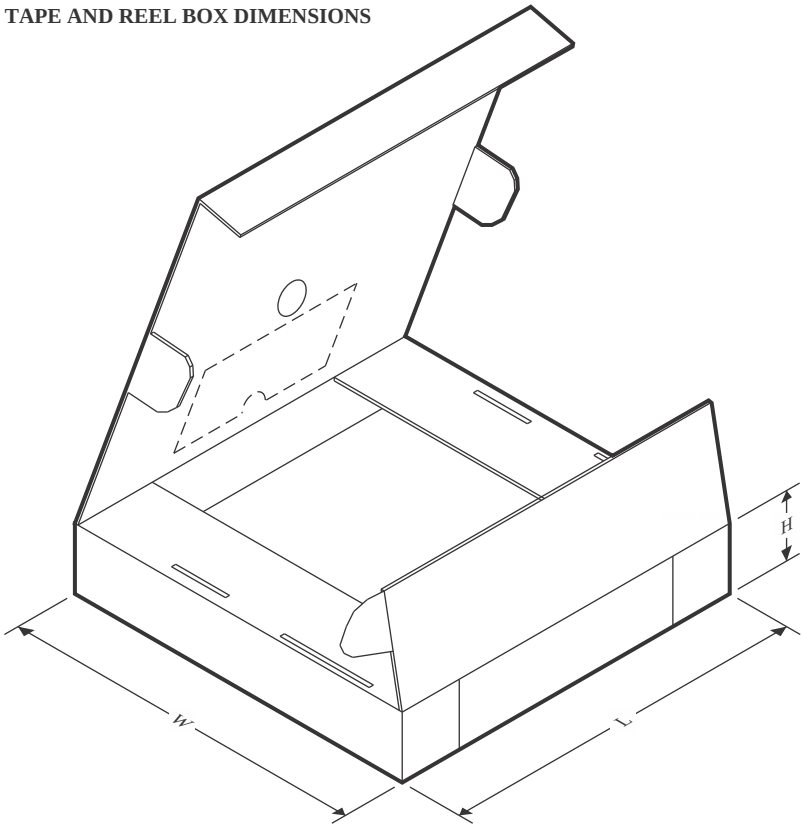
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3840DL16DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL16DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL16DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL17DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL17DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL18DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL19DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL19DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL20DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL22DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL22DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3840DL24DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL24DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL25DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL27DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL28DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3840DL29DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL30DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL30DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL31DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL35DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3840DL35DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL35DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL40DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL42DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL44DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL45DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL46DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL49DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH18DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3840PH18DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH19DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH19DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH27DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH27DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH30DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH30DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH40DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH40DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH45DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH45DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH49DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH49DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL16DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL18DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL20DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL25DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL26DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL26DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL27DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL27DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL27DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL28DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3840PL28DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL28DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL29DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL30DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3840PL31DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL33DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL34DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL40DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL41DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL42DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL42DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL43DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL43DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL44DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL44DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL45DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL45DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL48DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3840DL16DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL16DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL16DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL17DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL17DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL18DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL19DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL19DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL20DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840DL22DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL22DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3840DL24DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL24DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL25DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL27DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840DL28DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840DL29DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840DL30DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3840DL30DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL31DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840DL35DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3840DL35DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL35DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL40DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL42DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL44DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840DL45DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840DL46DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840DL49DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH18DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3840PH18DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH19DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH19DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH27DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH27DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH30DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH30DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH40DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH40DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH45DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH45DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH49DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH49DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL16DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840PL18DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840PL20DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840PL25DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840PL26DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL26DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL27DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL27DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL27DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL28DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3840PL28DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL28DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL29DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840PL30DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840PL31DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL33DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL34DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840PL40DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

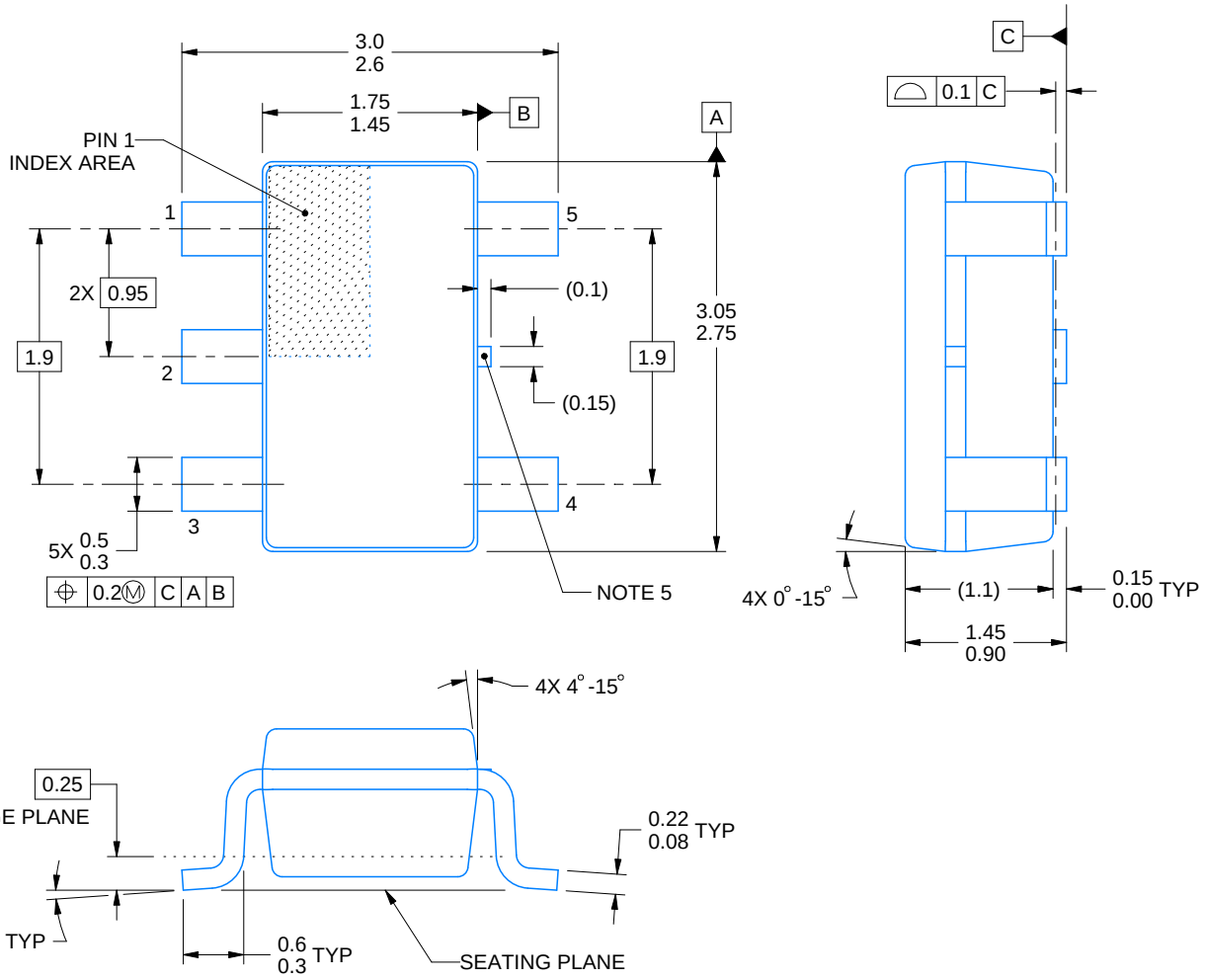
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3840PL41DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL42DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL42DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL43DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL43DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL44DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL44DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL45DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS3840PL45DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL48DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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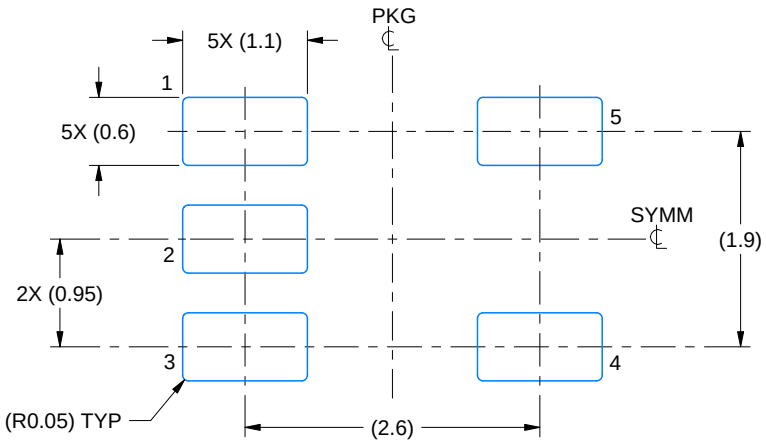
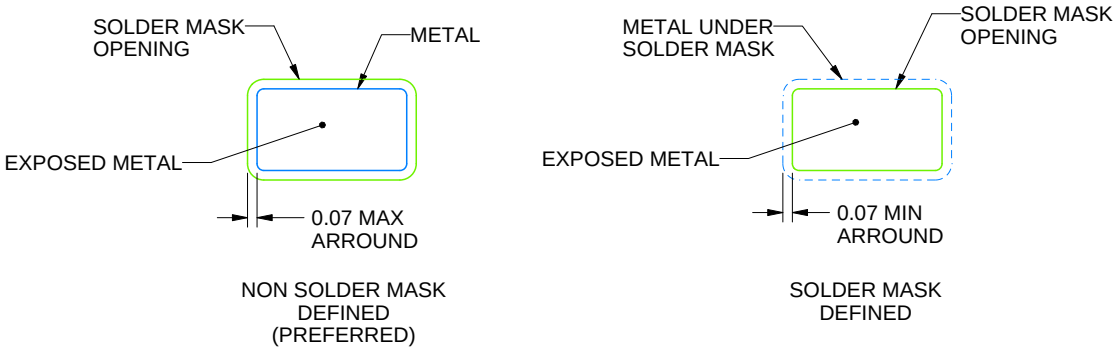
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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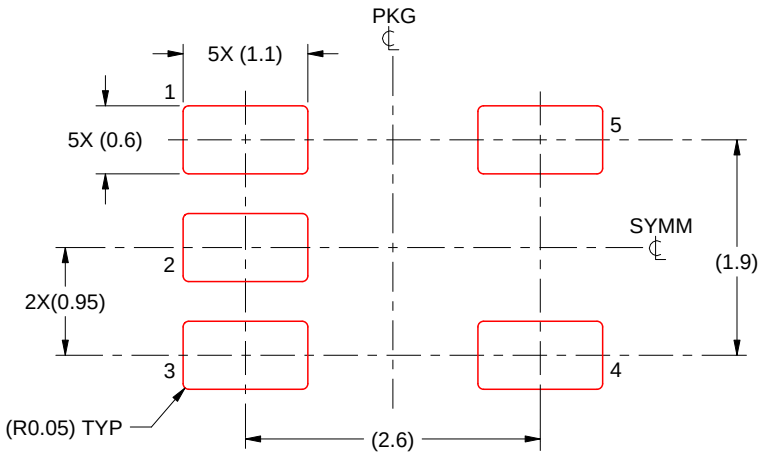
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025