# TPS389C03-Q1 Multichannel Overvoltage and Undervoltage I$^2$C Programmable Voltage Supervisor and Monitor with Q&A Watchdog

## 1 Features

- ASIL-D functional safety-compliant
  - Documentation to aid ISO 26262 system design
  - Systematic capability up to ASIL D
  - Hardware capability up to ASIL D
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C7B
- Q&A Watchdog to monitor SoC software operation
  - Programmable OPEN/CLOSE watchdog timing via I$^2$C (1 ms to 864 ms)
  - Start-up delay for SoC boot up initialization (2 ms to 3.46 s)
  - Programmable maximum violation count (up to 7) before WDO assertion
  - Watchdog disable pin (WDE)
- Monitor state-of-the art SOCs
  - 3 channels with 3 remote sense (TPS389C03-Q1)
  - Input voltage range: 2.6 V to 5.5 V
  - Undervoltage lockout (UVLO): 2.6 V
  - High threshold accuracy:
  - ± 5 mV (–40°C to +125°C)
  - Built-in ADC for voltage readouts
  - Fixed window threshold levels
    - 5 mV steps from 0.2 V to 1.475 V
    - 20 mV steps in other ranges
- Miniature solution and minimal component cost
  - 3 mm x 3 mm QFN package
  - User adjustable voltage threshold levels via I$^2$C
  - User adjustable glitch immunity and hysteresis levels via I$^2$C
- Designed for safety applications
  - Error Signal Monitoring (ESM)
    - Programmable ESM delay via I$^2$C (1 ms to 864 ms)

- Cyclic Redundancy Checking (CRC)
- Packet Error Checking (PEC)
- Active-low open-drain NIRQ, NRST, and WDO outputs

## 2 Applications

- Advanced driver assistance system (ADAS)
- Sensor fusion
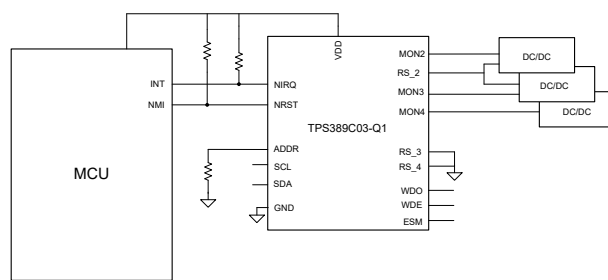  - Level 3 to Level 5 Autonomous Platforms

## 3 Description

The TPS389C03-Q1 device is an integrated multichannel window monitor reset IC with three remote sense pins available in a 16 pin 3 mm x 3 mm QFN package.

This highly accurate multichannel voltage supervisor is designed for systems that operate on low-voltage supply rails and have narrow margin supply tolerances. Internal glitch immunity and noise filters further eliminate false resets resulting from erroneous signals. This TPS389C03-Q1 device does not require any external resistors for setting overvoltage and undervoltage reset thresholds, which further optimizes overall accuracy, cost, solution size, and improves reliability for safety systems. I$^2$C functionality gives flexibility in selecting thresholds, reset delays, glitch filters, and pin functionality. This device offers CRC error checking and a built-in ADC for voltage readouts to provide redundant error checking. The device has a built in Q&A watchdog and Error Signal monitor with independent watchdog enable and watchdog output.

**Device Information**

| PART NUMBER | PACKAGE [(1)] | BODY SIZE (NOM) |
|---|---|---|
| TPS389C03-Q1 | WQFN (16) | 3 mm x 3 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**TPS389C03-Q1 Typical Circuit**

# Table of Contents

## 4 Device Comparison

Figure 4-1 shows the device nomenclature of the TPS389C03-Q1. Contact TI sales representatives or go online to TI's E2E forum for details and availability of other options; minimum order quantities apply.

See Figure 4-1 for more information regarding the device ordering codes. Table 10-1 and show how to decode the function of the device based on the part number.

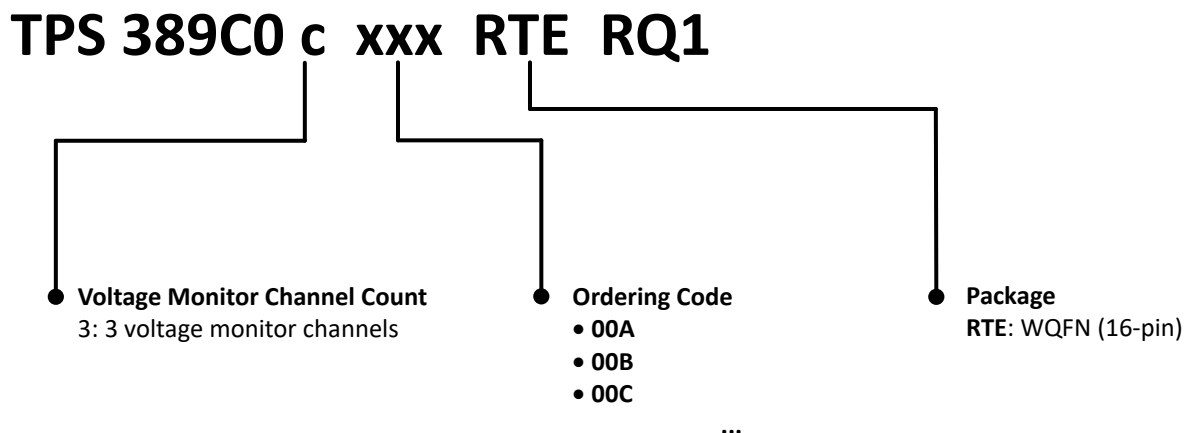**TPS 389C0 c  xxx  RTE  RQ1**

**Voltage Monitor Channel Count**
3: 3 voltage monitor channels

**Ordering Code**
- 00A
- 00B
- 00C
  ...

**Package**
**RTE**: WQFN (16-pin)

**Figure 4-1. TPS389C03-Q1 Device Nomenclature**

Product Folder Links: *TPS389C03-Q1*

# 5 Pin Configuration and Functions
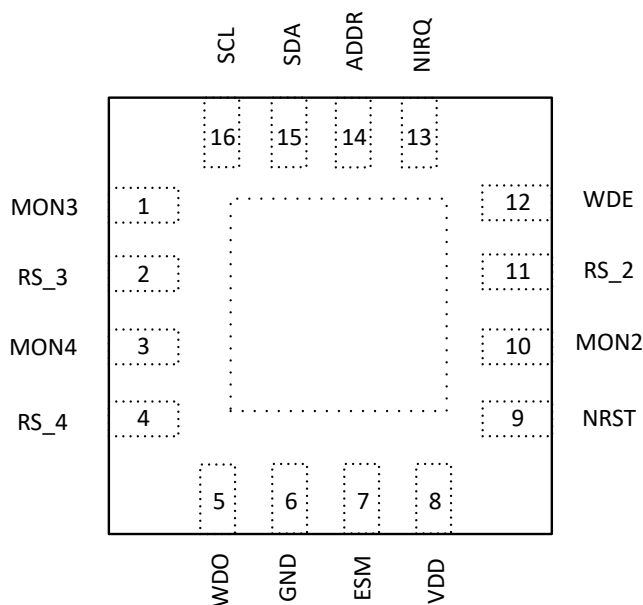


**Figure 5-1. RTE Package**
**16-Pin WQFN**
**TPS389C03-Q1 Top View**

**Table 5-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| **NO.** | **TPS389C03-Q1 NAME** | | |
| 1 | MON3 | I | Voltage monitor channel 3 |
| 2 | RS_3 | I | Remote sense for channel 3 |
| 3 | MON4 | I | Voltage monitor channel 4 |
| 4 | RS_4 | I | Remote sense for channel 4 |
| 5 | WDO | O | Open drain pin for Watch Dog errors |
| 6 | GND | - | Power ground |
| 7 | ESM | I | Error signal monitor |
| 8 | VDD | - | Power supply rail |
| 9 | NRST | O | Open drain Reset pin |
| 10 | MON2 | I | Voltage monitor channel 2 |
| 11 | RS_2 | I | Remote sense for channel 2 |
| 12 | WDE | I | Watch dog enable |
| 13 | NIRQ | O | Active-low open-drain interrupt output |
| 14 | ADDR | I | I$^2$C address select pin |
| 15 | SDA | I/O | I$^2$C data pin |
| 16 | SCL | I | I$^2$C clock pin |
| 17 | GND | - | Exposed power ground pad |

Product Folder Links: *TPS389C03-Q1*

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | VDD | −0.3 | 6 | V |
| Voltage | NIRQ,NRST,WDO,ESM,WDE | −0.3 | 6 | V |
| Voltage | SCL,SDA | −0.3 | VDD+0.3 | V |
| Voltage | ADDR | −0.3 | 2 | V |
| Voltage | MONx | −0.3 | 6 | V |
| Current | NIRQ,NRST,WDO |  | ±10 | mA |
| Temperature [2] | Continuous total power dissipation | See the Thermal Information | | |
| | Operating junction temperature, $T_J$ | -40 | 150 | °C |
| | Operating free-air temperature, $T_A$ | -40 | 125 | °C |
| | Storage temperature, $T_{stg}$ | -65 | 150 | °C |

(1)     Stresses beyond values listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2)     As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

## 6.2 ESD Ratings

|  |  |  |  | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1] | | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins | ±750 | |

(1)     AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

## 6.3 Recommended Operating Conditions

|  |  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VDD | Supply pin voltage | 2.6 | | 5.5 | V |
| NIRQ,NRST,WDO,ESM,WDE | Pin voltage | 0 | | 5.5 | V |
| $I_{NIRQ,NRST,WDO}$ | Pin Currents | 0 | | ±5 | mA |
| ADDR | Address pin voltage | 0 | | 1.8 | V |
| MONx | Monitor Pins | 0 | | 5.5 | V |
| SCL,SDA | Pin Voltage | 0 | | VDD | V |
| $R_{UP}$ [1] | Pull-up resistor (Open Drain config) | 1 | | 100 | kΩ |
| $T_J$ | Junction temperature (free-air temperature) | -40 | | 125 | °C |

Product Folder Links: *TPS389C03-Q1*

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPS389C03-Q1 | UNIT |
|---|---|---|---|
| | | RTE (WQFN) | |
| | | PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 53.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 51.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 17.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 20.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

At 2.6 V ≤ VDD≤ 5.5 V, NIRQ Voltage = 10 kΩ to $V_{DD}$, NIRQ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at $T_J$ = 25°C, typical conditions at VDD= 3.3 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **COMMON PARAMETERS** | | | | | | |
| VDD | Input supply voltage | | 2.6 | | 5.5 | V |
| $VDD_{UVLO}$ | Rising Threshold | | 2.67 | | 2.81 | V |
| | Falling Threshold | | 2.48 | | 2.6 | V |
| $V_{POR}$ | Power on Reset Voltage [2] | | | | 1.65 | V |
| $I_{DD\_Active}$ | Supply current into VDD pin | VDD≤5.5V | | 1550 | 2000 | µA |
| $V_{MONX}$ | MON voltage range | | 0.2 | | 5.5 | V |
| $I_{MONX}$ | Input current MONx pins | $V_{MON}$=5V | | | 20 | µA |
| VMON_LF | 1x mode (No scaling) | | 0.2 | | 1.475 | V |
| | 4x mode | | 0.8 | | 5.5 | V |
| VMON_HF | 1x mode (No scaling) | | 0.2 | | 1.475 | V |
| | 4x mode | | 0.8 | | 5.5 | V |
| Threshold Granularity_LF | 1x mode (No scaling) | | | 5 | | mV |
| | 4x mode | | | 20 | | mV |
| Threshold Granularity_HF | 1x mode (No scaling) | | | 5 | | mV |
| Threshold Granularity_HF | 4x mode | | | 20 | | mV |
| Accuracy_HF | VMON | 0.2V≤$V_{MONX}$≤1.0V | –6 | | 6 | mV |
| | | 1.0V<$V_{MONX}$≤1.475V | -7.5 | | 7.5 | mV |
| | | 1.475V<$V_{MONX}$≤2.95V | -0.6 | | 0.6 | % |
| | | $V_{MONX}$>2.95V | -0.7 | | 0.7 | % |
| $V_{HYS\_HF}$ | Hysteresis on UV,OV pin(Hysteresis is with respect of the tripoint ((UV),(OV)) [1] | 0.2V≤$V_{MONX}$≤1.475V | | 5 | 11 | mV |
| | | 1.475V<$V_{MONX}$≤2.95V | | 9 | 16 | mV |
| | | VMONX>2.95V | | 17 | 28 | mV |
| MON_OFF | OFF Voltage threshold | Monitored falling edge of $V_{MON}$ | 140 | | 215 | mV |
| NIRQ | On resistance- when asserted Low | Open Drain | | 12 | 17 | Ω |
| $V_{OL}$ | Low level output voltage-NIRQ | NIRQ, 5.5V/5mA | | | 100 | mV |

## 6.5 Electrical Characteristics (continued)

At 2.6 V ≤ VDD≤ 5.5 V, NIRQ Voltage = 10 kΩ to $V_{DD}$, NIRQ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at $T_J$ = 25°C, typical conditions at VDD= 3.3 V.

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{lkg(OD)}$ | Open-Drain output leakage current-NIRQ | NIRQ pin in High Impedance,VNIRQ= 5.5, Not asserted | | | 90 | nA |
| NRST | On resistance- when asserted Low | Open Drain | | 10 | 15 | Ω |
| $V_{OL}$ | Low level output voltage-NRST | NRST , 5.5V/5mA | | | 100 | mV |
| $I_{lkg(OD)}$ | Open-Drain output leakage current-NRST | NRST pin in High Impedance,VNRST= 5.5, Not asserted | | | 600 | nA |
| WDO | On resistance- when asserted Low | Open Drain | | 12 | 17 | Ω |
| $V_{OL}$ | Low level output voltage-WDO | WDO , 5.5V/5mA | | | 100 | mV |
| $I_{lkg(OD)}$ | Open-Drain output leakage current-WDO | WDO pin in High Impedance,VNRST= 5.5, Not asserted | | | 500 | nA |
| ESM_L | Logic Low Input | | | | 0.24 x VDD | V |
| ESM_H | Logic High Input | VDD>4.5 | 0.55 x VDD | | | V |
| | | VDD<4.5 | 0.6 x VDD | | | V |
| Ilkg(ESM) | Leakage current | ESM=5.5V | | | 75 | µA |
| WDE_L | Logic Low Input | | | | 0.36 | V |
| WDE_H | Logic High Input | | 1.26 | | | V |
| Ilkg(WDE) | Leakage current | WDE=5.5V | | | 5 | µA |
| $I_{ADDR}$ | ADDR pin current | | | 20 | | µA |
| I2C ADDR | (Hex format) | R=5.36k | | 0x30 | | |
| | | R=16.2k | | 0x31 | | |
| | | R=26.7k | | 0x32 | | |
| | | R=37.4k | | 0x33 | | |
| | | R=47.5k | | 0x34 | | |
| | | R=59.0k | | 0x35 | | |
| | | R=69.8k | | 0x36 | | |
| | | R=80.6k | | 0x37 | | |
| TSD | Thermal Shutdown | | | 155 | | ℃ |
| TSD Hys | Thernal Shutdown Hysterisis | | | 25 | | ℃ |
| RS | Remote sense range | | -100 | | 100 | mV |
| **ADC SPECIFICATION** | | | | | | |
| Vin | Input Range | | 0.2 | | 5.5 | V |
| Resolution | 1x mode | 0.2V≤VMON≤1.475V | | 5 | | mV |
| | 4x mode | VMON>1.475V | | 20 | | mV |
| $f_S$ | Sample Rate | | | 125 | | ksps |
| Accuracy_LF | VMON,1x mode | 0.2V≤VMON≤1.475V | -12 | | +12 | mV |
| | VMON, 4x mode | VMON>1.475V | -40 | | +40 | mV |
| **I2C ELECTRICAL SPECIFICATIONS** | | | | | | |
| $V_{HYS\_LF}$ | Hysteresis LF Faults, 1x mode | 0.2V≤VMON≤1.475V | | 10 | 15 | mV |
| | Hysteresis LF Faults, 4x mode | VMON>1.475V | | 40 | 55 | mV |
| $C_B$ | Capacitive load for SDA and SCL | | | | 400 | pF |
| SDA,SCL | Low Threshold | DEV_CONFIG.SOC_IF=0 | | | 0.84 | V |

Product Folder Links: TPS389C03-Q1

## 6.5 Electrical Characteristics (continued)

At 2.6 V ≤ VDD≤ 5.5 V, NIRQ Voltage = 10 kΩ to $V_{DD}$, NIRQ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at $T_J$ = 25°C, typical conditions at VDD= 3.3 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| SDA,SCL | High Threshold | DEV_CONFIG.SOC_IF=0 | 2.31 | | | V |

(1)   Hysteresis is with respect of the tripoint ($V_{IT-(UV)}$, $V_{IT+(OV)}$).
(2)   $V_{POR}$ is the minimum $V_{DDX}$ voltage level for a controlled output state.

## 6.6 Timing Requirements

At 2.6 V ≤ VDD ≤ 5.5 V, NIRQ Voltage  = 10 kΩ to VDD, NIRQ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at $T_J$ = 25°C, typical conditions at VDD = 3.3 V.

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **COMMON PARAMETERS** | | | | | | |
| $t_{BIST}$ | POR to ready with BIST, TEST_CFG.AT_POR=1 | includes OTP load | | | 12 | ms |
| tNBIST | POR to ready without BIST, TEST_CFG.AT_POR=0 | includes OTP load | | | 2 | ms |
| BIST | BIST time,TEST_CFG.AT_POR=1 or TEST_CFG.AT_SHDN=1 | | | | 10 | ms |
| $t_{I2C\_ACT}$ | I2C active from BIST complete | | | | 0 | µs |
| $t_{NRST}$ | Fault detection to NRST assertion latency | | | | 25 | µs |
| $t_{WDO}$ | Fault detection to WDO assertion latency | | | | 25 | µs |
| $t_{NIRQ}$ | Fault detection to NIRQ assertion latency (except OV/UV faults) | | | | 25 | µs |
| $t_{PD\_NIRQ\_1X}$ | HF fault Propagation detect delay (default deglitch filter) includes digitial delay | VIT_OV/UV +/- 100mV | | | 650 | ns |
| $t_{PD\_NIRQ\_4X}$ | HF fault Propagation detect delay (default deglitch filter) includes digitial delay | VIT_OV/UV +/- 400mV | | | 750 | ns |
| $t_D$ | RESET  time delay | I2C Register  time delay =000 | | 200 | | µs |
| | | I2C Register  time delay =001 | | 1 | | ms |
| | | I2C Register  time delay =010 | | 10 | | ms |
| | | I2C Register  time delay =011 | | 16 | | ms |
| | | I2C Register  time delay =100 | | 20 | | ms |
| | | I2C Register  time delay =101 | | 70 | | ms |
| | | I2C Register time delay =110 | | 100 | | ms |
| | | I2C Register  time delay =111 | | 200 | | ms |

Product Folder Links: *TPS389C03-Q1*

## 6.6 Timing Requirements (continued)

At 2.6 V ≤ VDD ≤ 5.5 V, NIRQ Voltage = 10 kΩ to VDD, NIRQ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at $T_J$ = 25°C, typical conditions at VDD = 3.3 V.

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{D\_WD}$ | WDO delay | I2C Register time delay =000 | | 200 | | µs |
| | | I2C Register time delay =001 | | 1 | | ms |
| | | I2C Register time delay =010 | | 10 | | ms |
| | | I2C Register time delay =011 | | 16 | | ms |
| | | I2C Register time delay =100 | | 20 | | ms |
| | | I2C Register time delay =101 | | 70 | | ms |
| | | I2C Register time delay =110 | | 100 | | ms |
| | | I2C Register time delay =111 | | 200 | | ms |
| $t_{debounce\_ESM}$ | Debounce time | I2C Register time delay =00 | | 10 | | µs |
| | | I2C Register time delay =01 | | 25 | | |
| | | I2C Register time delay =10 | | 50 | | |
| | | I2C Register time delay =11 | | 100 | | |
| $t_{GI\_R}$ | UV & OV debounce range via I2C | FLT_HF(N) | 0.1 | | 102.4 | µs |

## 6.6 Timing Requirements (continued)

At 2.6 V ≤ VDD ≤ 5.5 V, NIRQ Voltage = 10 kΩ to VDD, NIRQ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at $T_J$ = 25°C, typical conditions at VDD = 3.3 V.

|  |  |  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **I2C TIMING CHARACTERISTICS** | | | | | | |
| $f_{SCL}$ | Serial clock frequency | Standard mode | | | 100 | kHz |
| $f_{SCL}$ | Serial clock frequency | Fast mode | | | 400 | kHz |
| $f_{SCL}$ | Serial clock frequency | Fast mode + | | | 1 | MHz |
| $t_{LOW}$ | SCL low time | Standard mode | 4.7 | | | µs |
| $t_{LOW}$ | SCL low time | Fast mode | 1.3 | | | µs |
| $t_{LOW}$ | SCL low time | Fast mode + | 0.5 | | | µs |
| $t_{HIGH}$ | SCL high time | Standard mode | 4 | | | µs |
| $t_{HIGH}$ | SCL high time | Fast mode + | 0.26 | | | µs |
| $t_{SU;DAT}$ | Data setup time | Standard mode | 250 | | | ns |
| $t_{SU;DAT}$ | Data setup time | Fast mode | 100 | | | ns |
| $t_{SU;DAT}$ | Data setup time | Fast mode + | 50 | | | ns |
| $t_{HD;DAT}$ | Data hold time | Standard mode | 10 | | 3450 | ns |
| $t_{HD;DAT}$ | Data hold time | Fast mode | 10 | | 900 | ns |
| $t_{HD;DAT}$ | Data hold time | Fast mode + | 10 | | | ns |
| $t_{SU;STA}$ | Setup time for a Start or Repeated Start condition | Standard mode | 4.7 | | | µs |
| $t_{SU;STA}$ | Setup time for a Start or Repeated Start condition | Fast mode | 0.6 | | | µs |
| $t_{SU;STA}$ | Setup time for a Start or Repeated Start condition | Fast mode + | 0.26 | | | µs |
| $t_{HD:STA}$ | Hold time for a Start or Repeated Start condition | Standard mode | 4 | | | µs |
| $t_{HD:STA}$ | Hold time for a Start or Repeated Start condition | Fast mode | 0.6 | | | µs |
| $t_{HD:STA}$ | Hold time for a Start or Repeated Start condition | Fast mode + | 0.26 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | Standard mode | 4.7 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | Fast mode | 1.3 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | Fast mode + | 0.5 | | | µs |
| $t_{SU;STO}$ | Setup time for a Stop condition | Standard mode | 4 | | | µs |
| $t_{SU;STO}$ | Setup time for a Stop condition | Fast mode | 0.6 | | | µs |
| $t_{SU;STO}$ | Setup time for a Stop condition | Fast mode + | 0.26 | | | µs |
| trDA | Rise time of SDA signal | Standard mode | | | 1000 | |
| trDA | Rise time of SDA signal | Fast mode | 20 | | 300 | ns |
| trDA | Rise time of SDA signal | Fast mode + | | | 120 | ns |
| tfDA | Fall time of SDA signal | Standard mode | | | 300 | ns |
| tfDA | Fall time of SDA signal | Fast mode | 1.4 | | 300 | ns |
| tfDA | Fall time of SDA signal | Fast mode + | 6.5 | | 120 | ns |
| trCL | Rise time of SCL signal | Standard mode | | | 1000 | ns |
| trCL | Rise time of SCL signal | Fast mode | 20 | | 300 | ns |
| trCL | Rise time of SCL signal | Fast mode + | | | 120 | ns |
| tfCL | Fall time of SCL signal | Standard mode | | | 300 | ns |
| tfCL | Fall time of SCL signal | Fast mode | 6.5 | | 300 | ns |
| tfCL | Fall time of SCL signal | Fast mode + | 6.5 | | 120 | ns |
| tSP | Pulse width of SCL and SDA spikes that are suppressed | Standard mode, Fast mode and Fast mode + | | | 50 | ns |

# 7 Detailed Description

## 7.1 Overview

The TPS389C03-Q1 family of devices has three channels that can be configured for over voltage, under voltage or both in a window configuration. The TPS389C03-Q1 features a highly accurate window threshold voltages (up to ±5 mV) and a variety voltage thresholds which can be factory configured or set on boot up by I2C commands.

The TPS389C03-Q1 includes the resistors used to set the overvoltage and undervoltage thresholds internal to the device. These internal resistors allow for lower component counts and greatly simplifies the design because no additional margins are needed to account for the accuracy of external resistors.

The TPS389C03-Q1 is designed to assert active low output signals (NIRQ and/or NRST) when the monitored voltage is outside the safe window. The default configuration has the interrupts enabled for over voltage and under voltage faults, sequence timeout set for 1 ms, BIST enabled at POR, and over voltage and under voltage debounce set for 102.4 µs.

## 7.2 Functional Block Diagram
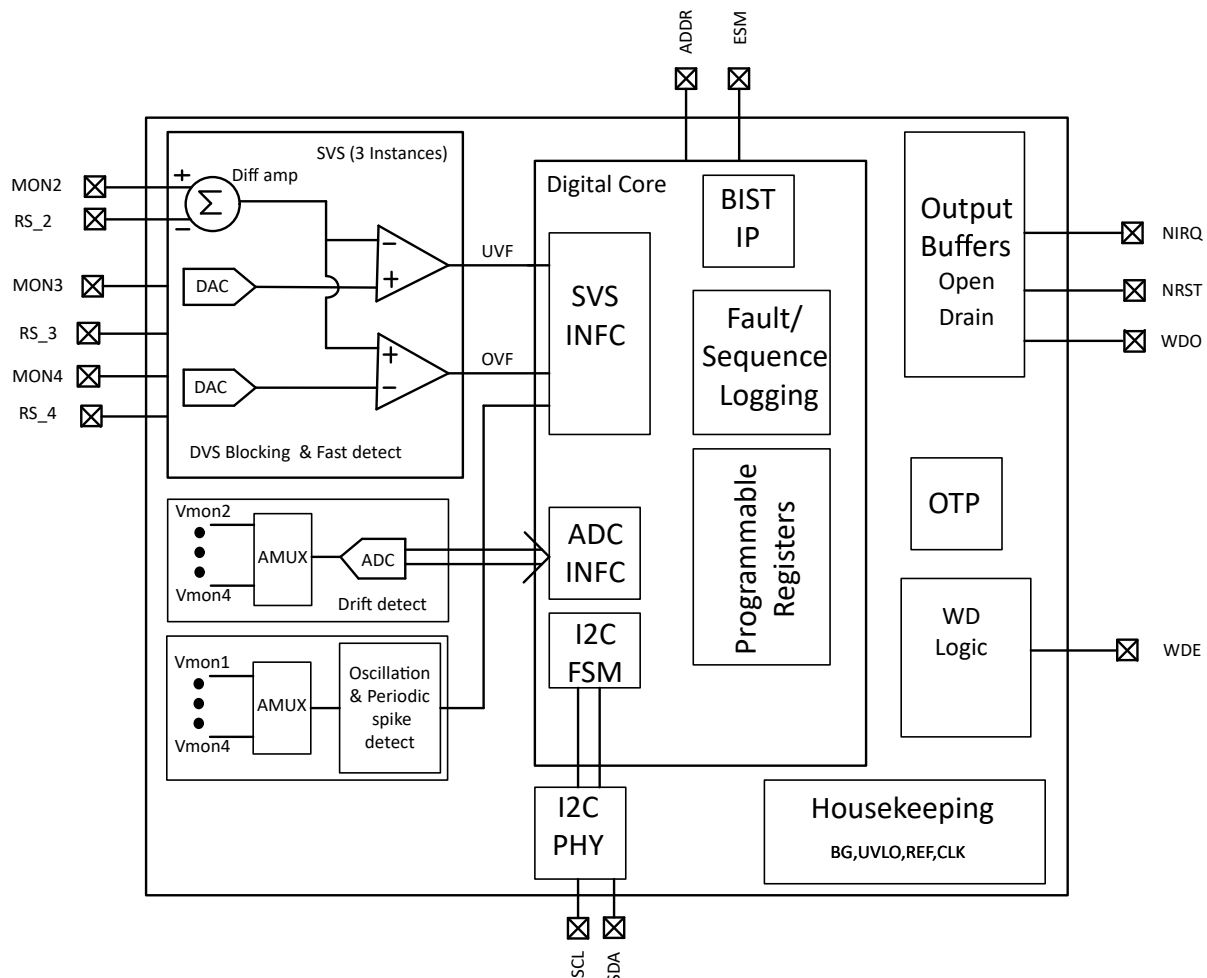


**Figure 7-1. TPS389C03-Q1 Block Diagram**

Product Folder Links: *TPS389C03-Q1*

## 7.3 Feature Description

### 7.3.1 I²C

The TPS389C03-Q1 device follows the I²C protocol (up to 1MHz) to manage communication with host devices such as an MCU or System on Chip (SoC). I²C is a two wire communication protocol implmented using two signals, clock (SCL) and data (SDA). The host device is primary controller of communication. TPS389C03-Q1 device responds over the data line during read or write operation as defined by I²C protocol. Both SCL and SDA signals are open drain topology and can be used in a wired-OR configuration with other devices to share the communication bus. Both SCL and SDA pins need an external pull up resistance to supply voltage (10kΩ recommended).

Figure 7-2 shows the timing relationship between SCL and SDA lines to transfer 1 byte of data. SCL line is always controlled by host. To transfer 1 byte data, host needs to send 9 clocks on SCL. 8 clocks for data and 1 clock for ACK or NACK. SDA line will be controlled by either host or TPS389C03-Q1 device based on the read or write operation. Figure 7-3 and Figure 7-4 highlight the communication protocol flow and which device controls SDA line at various instances during active communication.
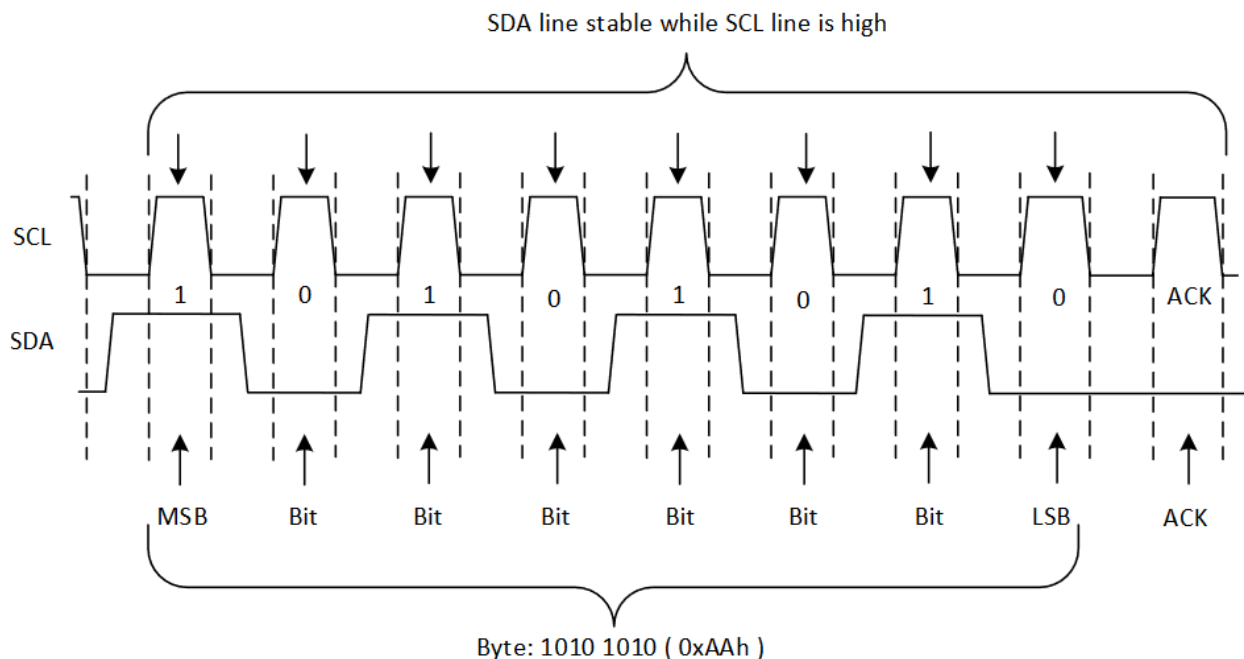


**Figure 7-2. SCL to SDA timing for 1 byte data transfer**
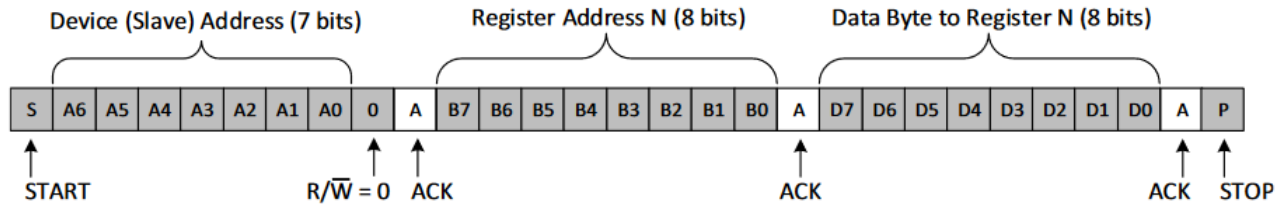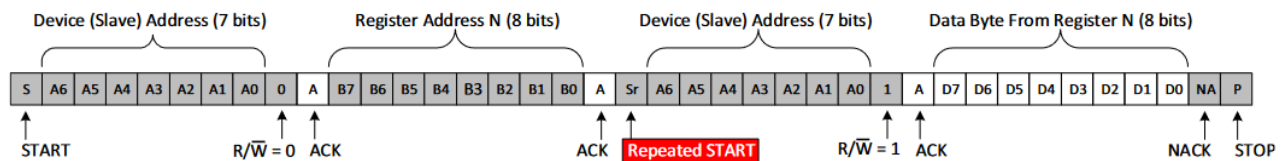
**Figure 7-3. I²C write protocol**



**Figure 7-4. I²C read protocol**

Before initiating communication over I²C protocol, host needs to confirm the I²C bus is available for communication. Monitor the SCL and SDA lines, if any line is pulled low, the I²C bus is occupied. Host needs to wait until the bus is available for communication. Once the bus is available for communication, the host can initiate read or write operation by issuing a START condition. Once the I²C communication is complete, release the bus by issuing STOP command. Figure 7-5 shows how to implement START and STOP condition.
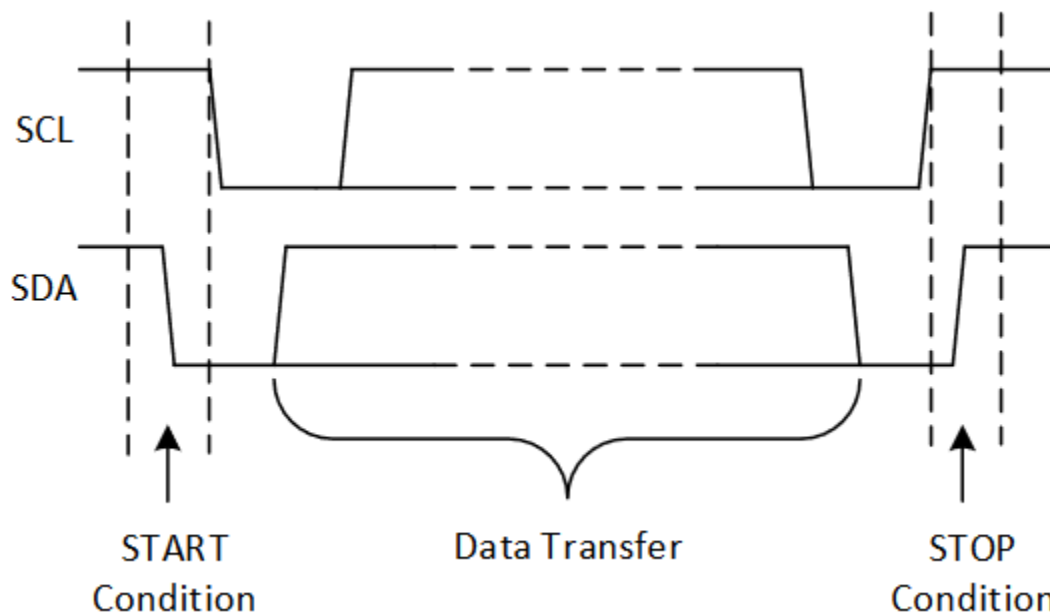
Product Folder Links: *TPS389C03-Q1*

**Figure 7-5. I²C START and STOP condition**

The SDA line may get stuck in logic low level if required number of clocks are not provided by the host. In this scenario, host should provide multiple clocks on SCL line until the SDA line goes high. After this event, host should issue I²C stop command. This will release the I²C bus and other devices can use the I²C bus.

Table 7-1 shows the different functionality available when programming with I²C.

**Table 7-1. User Programmable I²C Functions**

| FUNCTIONS | DESCRIPTION |
|---|---|
| Thresholds for OV/UV- HF | Adjustable in 5 mV steps from 0.2 V to 1.475 V and 20 mV steps from 0.8 V to 5.5 V |
| Thresholds for OV/UV - LF | Adjustable in 5 mV steps from 0.2 V to 1.475 V and 20 mV steps from 0.8 V to 5.5 V |
| Voltage Monitoring scaling | 1 or 4 |
| Glitch immunity for OV/UV- HF | 0.1 us to 102.4 us |
| Low Frequency Cutoff filter | 250 Hz to 4 kHz |
| Enable sequence timeout | 1 ms to 4 s |
| Packet error checking for I²C | Enabling or Disabling |
| Force NIRQ/NRST/WDO assertion | Controlled by I²C register |
| Individual channel MON | Enable or Disable |
| Interrupt disable functions | BIST, PEC, TSD, CRC |
| ESM Threshold | 1 ms to 864 ms |
| ESM Debounce | 10 us to 100us |
| Reset Delay | 200 us to 200 ms |
| MAX Violation Count | 0 to 7 |
| Watchdog Startup Delay Multiplier | 0 to 7 |
| Watchdog Open and Close Window Times | 1 ms to 864 ms |
| Watchdog Output Delay | 200 us to 200 ms (only applicable for non-latched WDO) |
| OV/UV/ESM/WDT | Mappable individually to NIRQ, NRST, and WDO |

### 7.3.2 Maskable Interrupt (AMSK)

In the case of power up, AMSK_ON register applies. AMSK_ON masks interrupts until the MON voltage crosses the UVLF threshold or sequence timeout expires whichever is sooner. In the case of power down AMSK_OFF register applies. AMSK_ON masks interrupts until the MON voltage is below the OFF threshold and then the OVLF interrupts are active.

Table 7-2 summarizes the auto-mask operation for power up and power down.

**Table 7-2. Auto-Mask Operation for the Power Up and Power Down**

| TRANSITION | AUTO-MASK APPLIED | AUTO-MASK APPLIES TO | AUTO-MASK INACTIVE | INTERRUPTS ACTIVE FOR MON CHANNELS NOT IN AUTO-MASK |
|---|---|---|---|---|
| Power Up | AMSK_ON | IEN_UVLF, IEN_UVHF, IEN_OVHF | SEQ_TOUT expires or rail crosses UVLF | At Power Up |
| Power Down | AMSK_OFF | | Auto-mask active in transition until SEQ_TOUT expires | Until SEQ_TOUT expires |

### 7.3.3 VDD

The TPS389C03-Q1 is designed to operate from an input voltage supply range between 2.6 V to 5.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 1-µF capacitor between the VDD pin and the GND pin.

$V_{DD}$ needs to be at or above $V_{DD(MIN)}$ for at least the start-up delay ($t_{SD}$+ $t_D$) for the device to be fully functional.

### 7.3.4 MON

The TPS389C03-Q1 combines two comparators with a precision reference voltage and a trimmed resistor divider per monitor (MON) channel. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Both comparators also include built-in hysteresis that provides noise immunity and provides stable operation.

Each MON channel can be configured for Low Frequency (LF) and High Frequency (HF) fault detection. HF fault detection uses a comparator for UV and OV measurements referenced to the threshold voltage. A debounce filter for glitch immunity can be configured for HF faults using the FLT_HF registers in BANK1 associated with each MON channel.

LF fault detection measures the voltage through an ADC that can be used to monitor voltage drift. The LF detection thresholds can be configured for various purposes. For example, the OVLF threshold can be set lower than the OVHF threshold for drift monitoring. Alternatively, the OVLF threshold can be set to overlap with the OVHF threshold for redundancy. LF and HF faults are configured using the UV_HF, OV_HF, UV_LF, and OV_LF registers in BANK1. Each MON channel has unique UV_HF, OV_HF, UV_LF, and OV_LF registers. The diagram shown in Figure 7-6 illustrates an example of how the LF and HF faults can be configured.

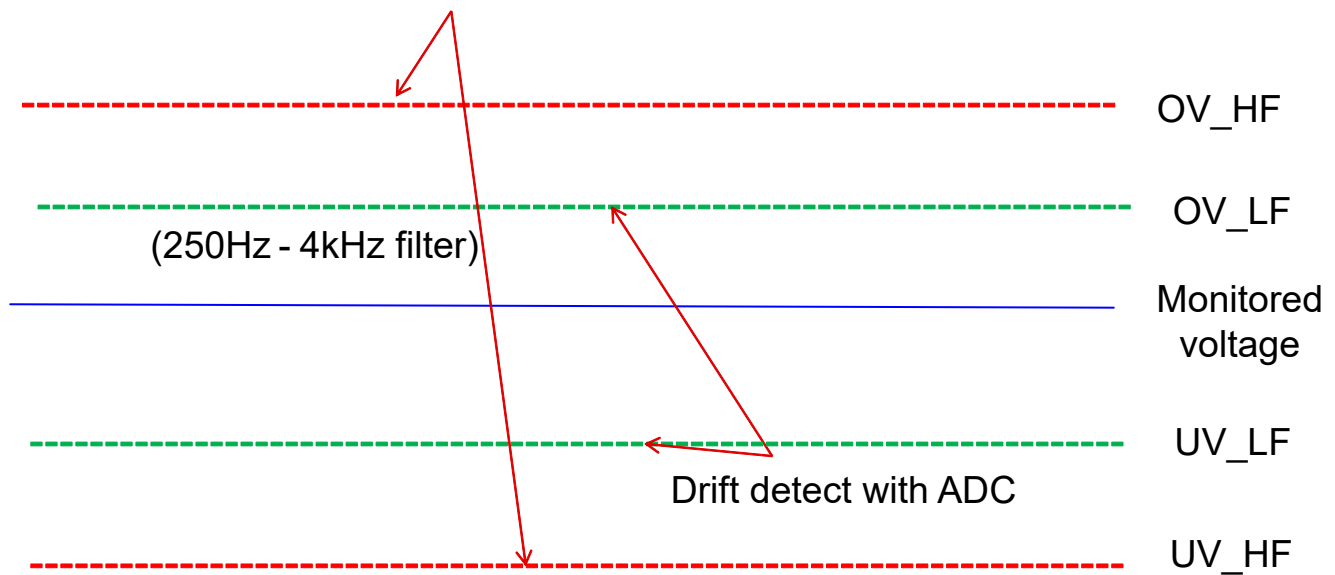Ultra fast detection with comparators with deglitch filters (0.1us to 102.4us)



– – – – – – – – – – – – – – – – – – – – – – – – – – – OV_HF

– – – – – – – – – – – – – – – – – – – – – – – – – – – OV_LF

(250Hz - 4kHz filter)

———————————————————————— Monitored voltage

– – – – – – – – – – – – – – – – – – – – – – – – – – – UV_LF

Drift detect with ADC

– – – – – – – – – – – – – – – – – – – – – – – – – – – UV_HF

**Figure 7-6. MON Channel State Diagram**

Although not required in most cases, for noisy applications good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the MON input to reduce sensitivity to transient voltages on the monitored signal. Specific debounce times or deglitch times can also be set independently for each MON via I$^2$C registers

When monitoring VDD supply voltage, the MON pin can be connected directly to VDD. The outputs NIRQ and NRST are high impedance when voltage at the MON pin is between upper and lower boundary of threshold.

The MON channel settings can be adjusted by using the associated registers listed in the register maps found in Section 8. Using the register maps, the code example in Figure 7-7 demonstrates how MON2 can be reconfigured.

```
ADDR 30
//              Go to Bank 1
WR F0 01
//              Check UVHF,OVHF thresholds for MON2 and MON3
RD 30 //MON2 UVHF
RD 31 //MON2 OVHF
RD 40 //MON3 UVHF
RD 41 //MON3 OVHF
//              Check UVLF,OVLF thresholds for MON2 and MON3
RD 32 //MON2 UVHF
RD 33 //MON2 OVHF
RD 42 //MON3 UVHF
RD 43 //MON3 OVHF
//              Example change OVHF threshold MON2 to 5.5V
WR 31 EB
//              Example change OVHF threshold MON2 to 5.48V
WR 31 EA
//              Example change OVHF threshold MON2 to 5.44V
WR 31 E8
//       Telemetry read the voltages being monitored
//              Go to Bank 0
WR F0 00
RD 41 // MON2 Voltage
RD 42 // MON3 Voltage
//      Simulate an OV fault on MON2
//              Go to Bank 1
WR F0 01
WR 31 C8 // Change OVHF threshold to 4.8V
//      NIRQ,NRST asserts (depends on mapping)
//      Clearing OVHF fault MON2
//              Go to Bank 0
WR F0 00
RD 16 // 02 READ SINCE OVHF on MON2
WR 16 02 // WRITE 1(bit 2) to clear
```

**Figure 7-7. MON2 Setting Software Example**

### 7.3.5 NRST

The NRST pin features a programmable reset delay time that can be adjusted from 0.2 ms to 200 ms when using TI_CONTROL register. NRST is an open-drain output that should be pulled up through a 1-kΩ to 100-kΩ pullup resistor. When the device is powered up and POR is complete, NRST is asserted low until the BIST is complete. After the BIST, NRST remains high (not asserted) until it is triggered by a mappable fault condition. An NRST_MISMATCH fault will be asserted if the NRST pin is pulled to an unexpected state. For example, if the NRST pin is in a high-impedance state (logic high) and is externally pulled low, then an NRST_MISMATCH fault will assert. During an NRST toggle NRST mismatch will be active after 2µs, NRST must exceed 0.6*VDD to be considered in a logic high state.

NRST is mappable to the watchdog fault, and the ESM fault when using the IEN_VENDOR register. If NRST is mapped to the ESM fault, the NRST pin will be asserted following the ESM delay and will be de-asserted after the reset delay ($t_D$). If NRST is mapped to the watchdog fault, the NRST pin will be asserted during a watchdog fault and de-assert following the reset delay ($t_D$).

NRST is also mappable to the OVHF and UVHF faults using the FC_LF[n] registers. If a monitored voltage falls or rises outside of the programmed OVHF and UVHF thresholds, then NRST is asserted, driving the NRST pin

low. When the monitored voltage comes back into the valid window, a reset delay circuit is enabled that holds NRST low for a specified reset delay period ($t_D$).

The $t_D$ period is determined by the RST_DLY[2:0] value found in the TI_CONTROL register. When the reset delay has elapsed, the NRST pin goes to a high-impedance state and uses a pullup resistor to hold NRST high. The pullup resistor must be connected to the proper voltage rail to allow other devices to be connected at the correct interface voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by output logic low voltage (VOL), capacitive loading, and leakage current.

### 7.3.6 NIRQ

In a typical TPS389C03-Q1 application, the NIRQ output is connected to a reset or enable input of a processor [such as a digital signal processor (DSP) or application-specific integrated circuit (ASIC), or other processor type].

The TPS389C03-Q1 has an open drain active low output that requires a pull-up resistor to hold these lines high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The pull-up resistor value is determined by $V_{OL}$, output capacitive loading, and output leakage current. These values are specified in Section 6. The open drain output can be connected as a wired-OR logic with other open drain signals such as another TPS389C03-Q1 NIRQ pin.

### 7.3.7 ADC

The ADC used in the TPS389C03Q-1 runs on a 1MHz clock with an effective sampling rate of 1/8 MHz (= 125 kHz). Initially, the ADC records with a resolution of 12 bits (1LSB = 0.41667mV) which is later round off to 8-bit data for I$^2$C transaction. (1LSB = 5mV) The ADC uses ping-pong architecture in which it requires 2us for both sampling and conversion per channel with a total of 2 sampling channels. While CH0 performs coarse conversion, CH1 does fine conversion and vice versa.

Digitized 8-bit data is updated once the fine conversion is completed, which occurs once every 8 μs. Each I$^2$C transaction initiated for reading 8-bit MON_LVL data (the ADC data of a particular channel), 8-bit data is paused from updating until the I$^2$C transaction completes.

Voltage scaling is done using a resistor ladder, but for differential mode channels, a chopping circuit is used to get the average of both of the voltages (VMON + VMON_RS)/2 since VMON_RS can be negative and can't be converted into an ADC code. VMON – VMON_RS is calculated digitally by subtracting ((VMON + VMON_RS) /2) from VMON and then multiplying by 2.

The MONX channels can be configured in 1x (0.2V to 1.475V) or 4x mode (0.8V to 5.5V). For differential mode channels configured in 1x mode, (MON1 and MON2) the ADC range is limited up to 1.7V. To configure an ADC channel above 1.7 V, please use 4x mode.

Real time voltage measurements use.

$$V_{lvl} = ((ADC[7:0] * 5mV) + 0.2) * (VRANGE\_MULT) \tag{1}$$

1. ADC[7:0] is translated to a corresponding decimal value. The value of ADC[7:0] corresponding to MON2-MON4 can be read from BANK0, registers 0x41 to 0x43 found in Section 8.1.1.
2. VRANGE_MULT corresponds to the selected monitor voltage multiplier set in BANK1, register 0x1F of Section 8.1.2.
3. VRANGE_MULT is set to a decimal 1 or 4 value depending on monitored value.

### 7.3.8 Packet Error Checking (PEC)

TPS389C03-Q1 supports Packet Error Checking (PEC) as a way to implement Cyclic Redundancy Checking (CRC). With the initial value of CRC set to 0x00, the PEC uses a CRC-8 represented by the polynomial:

$$C(x) = x^2 + x^2 + x + 1 \tag{2}$$

The PEC calculation includes all bytes in the transmission, including address, command and data. The PEC calculation does not include ACK or NACK bits or START, STOP or REPEATED START conditions. If PEC is enabled, and the TPS389C03-Q1 is transmitting data, then the TPS389C03-Q1 is responsible for sending the PEC byte. If PEC is enabled, and the TPS389C03-Q1 is reveiving data from the MCU, then the MCU is responsible for sending the PEC byte.

- If PEC is enabled by EN_PEC, and the PEC byte is present in the write transaction, the device will NACK and assert NIRQ if PEC byte is incorrect.
- If PEC is enabled by EN_PEC, and the PEC byte is not present in the write transaction.
    - If REQ_PEC = 0, missing PEC is treated as good PEC and register write succeeds. NIRQ is not asserted.
    - If REQ_PEC = 1, missing PEC is treated as incorrect PEC and register write fails. NIRQ is asserted.

### 7.3.9 Q&A Watchdog

The Question and Answer Watchdog requires specific data to be sent from the MCU to the TPS389C03-Q1 within a specific time interval.

The TPS389C03-Q1 generates questions for the MCU to read during the OPEN and CLOSE windows. Questions are read as the combination of ANSW_CNT[1:0] and TOKEN[3:0] status bits found in the WD_STAT_QA register in BANK0. After reading a question, the MCU calculates the Reference Answer using the logic equations shown in Figure 7-8 and responds by writing the 8-bit answer into the WDT_ANSWER register in BANK1. A code example for Reference Answer calculation is shown in Figure 7-11. For a typical application, changing the value of FDBK[1:0], found in the WDT_QA_CFG register in BANK1, from the default value of FDBK[1:0] = 00b is not required. However, FDBK[1:0] can be changed if a different Reference Answer calculation is needed. Question generation and answer calculations are explained in more detail in Section 7.3.9.1.
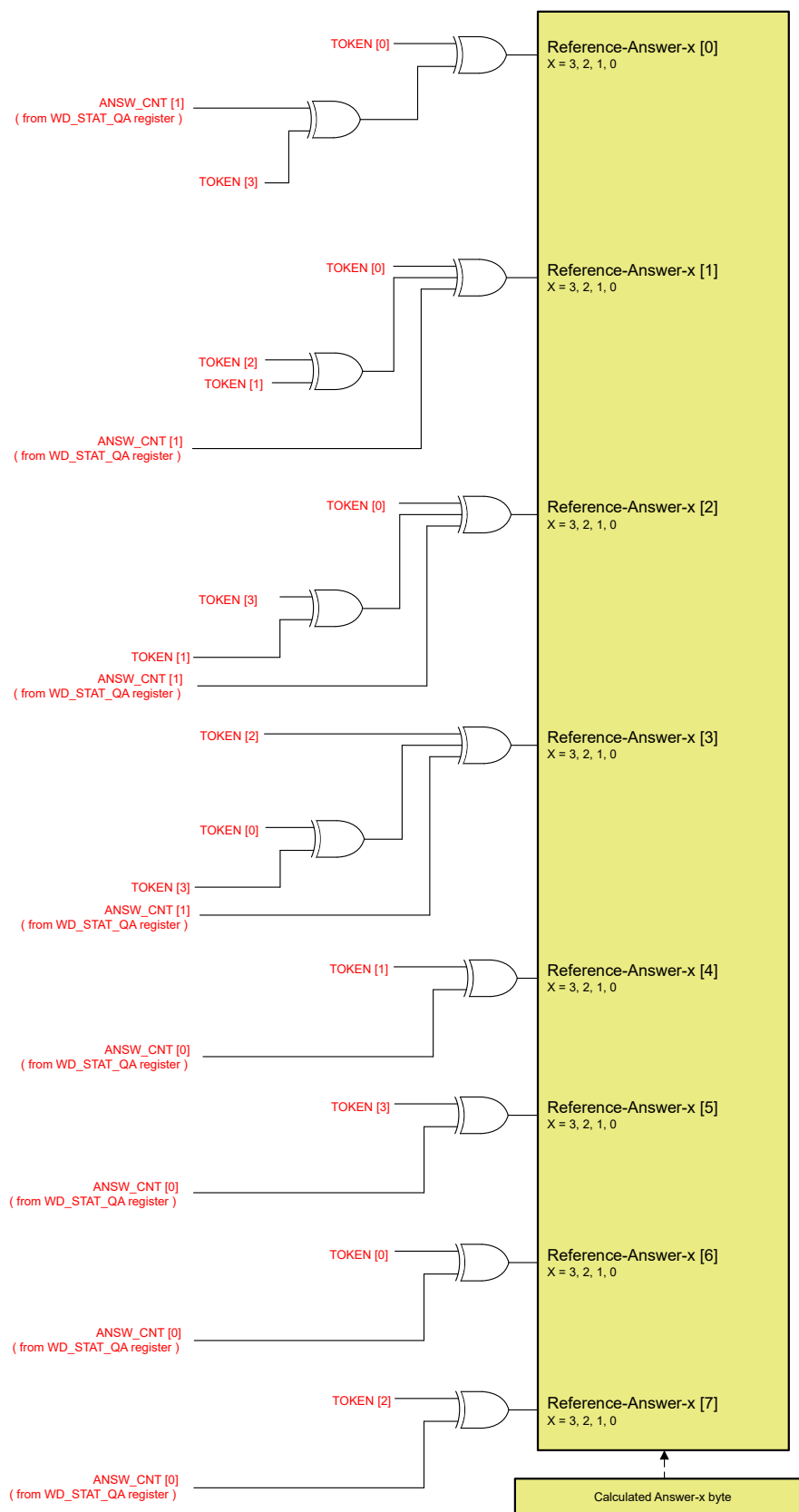
**Figure 7-8. Watchdog Answer Calculation for FDBK[1:0] = 00b**

Product Folder Links: *TPS389C03-Q1*

During one "event," the TPS389C03-Q1 generates three questions within the CLOSE window and one question within the OPEN window. The MCU must correctly read and answer all three questions within the specified CLOSE window and the question within the specified OPEN window for a "good event" to occur. At the start of an event, ANSW_CNT[1:0] = 11b. A correctly answered question decrements ANSW_CNT[1:0] to generate the next question. Once a good event occurs, ANSW_CNT[1:0] is reset to ANSW_CNT[1:0] = 11b, and the value of TOKEN[3:0] changes to generate a new set of questions for the next event.

An incorrectly answered question increments the violation count, resets the ANSW_CNT[1:0] to ANSW_CNT[1:0] = 11b, and restarts the CLOSE window. The maxmimum violation count, MAX_VIOLATION_COUNT[2:0], is programmed using the WDT_CFG register in BANK1. When the violation count reaches its maximum value, the TPS389C03-Q1 WDO (latched) low, and may assert NIRQ and NRST low depending on the fault mapping. A good event decrements the violation count if the violation count is not already equal to zero. When the watchdog enters the Idle state, the violation count is reset. When the the watchdog enters the suspend state, the violation count remains unchanged. The watchdog state diagram is illustrated in Figure 7-20.

Within an event, the CLOSE window time is a fixed value, and does not change if all three questions are answered faster than the set time. For example, if the CLOSE window time is set to 10 ms, and the three questions are correctly answered in 5 ms, then the TPS389C03-Q1 will wait the remaining 5 ms before transitioning to the OPEN window. During the OPEN window, if the question is answered faster than the selected OPEN window time, then the TPS389C03-Q1 automatically transitions on to the next event's CLOSE window. An incorrectly answered question within either the CLOSE or OPEN windows results in the TPS389C03-Q1 restarting the CLOSE window.
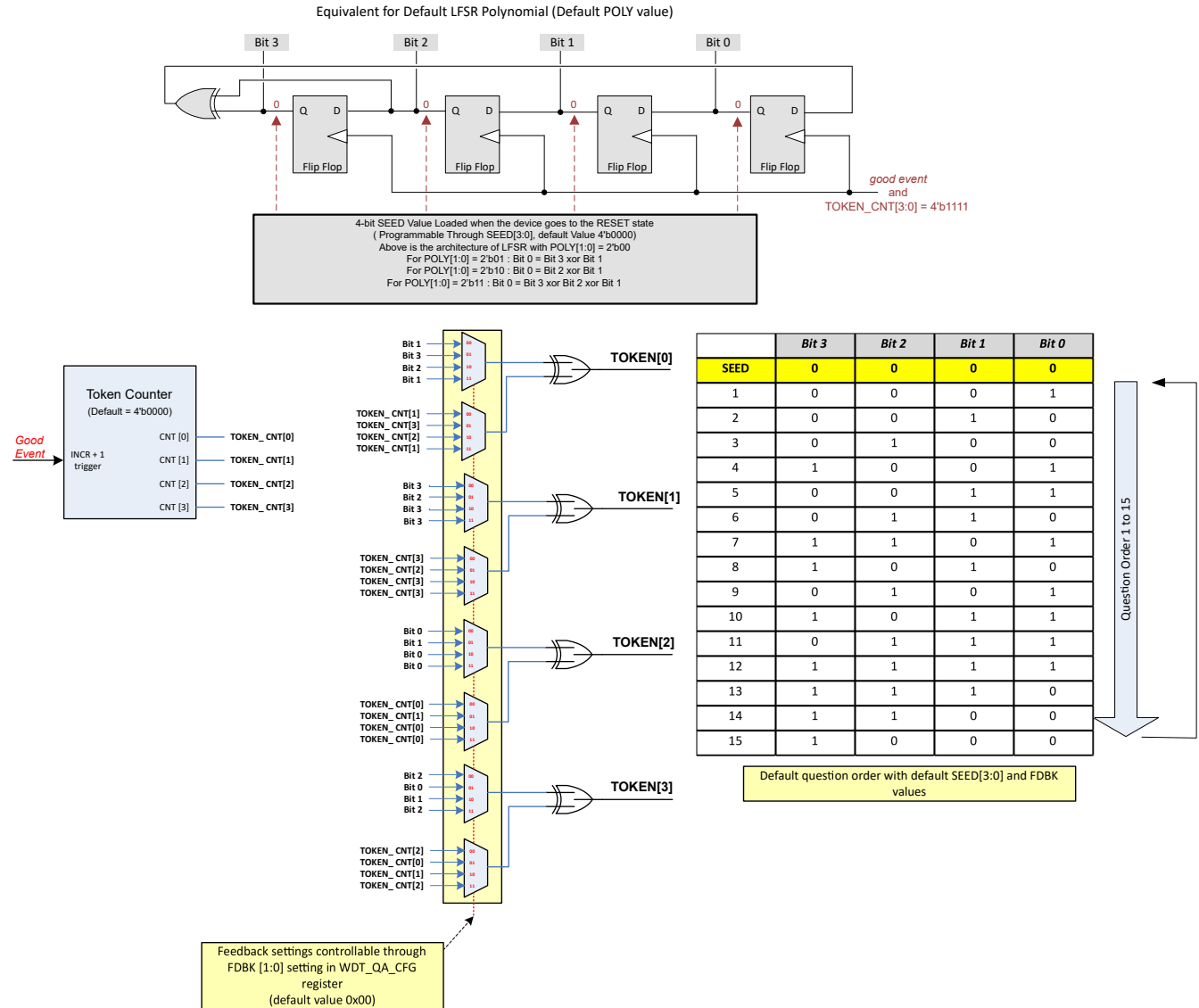
### 7.3.9.1 Question and Token Generation

A question is presented to the MCU as a combination of the TOKEN[3:0] and the ANSW_CNT[1:0] status bits found in the WD_STAT_WA register. ANSW_CNT[1:0] has a default value of ANSW_CNT[1:0] = 11b and is decremented when a question is answered correctly. The value of ANSW_CNT[1:0] is reset to ANSW_CNT[1:0] = 11b when a question is answered incorrectly or a good event is completed.

The watchdog uses the Token Counter (TOKEN_CNT[3:0] bits Figure 7-10) and a Linear Feedback Shift Register (LFSR) to generate the 4-bit TOKEN[3:0]. The LFSR architecture can be configured using POLY[1:0] in the WDT_QA_CFG register in BANK1 as shown in Figure 7-10. In a typical application, it is not necessary to change the value of POLY[1:0] from the default 00b. However, POLY[1:0] can be configured if a different LFSR architecture is required. The diagram illustrated in Figure 7-9 represents how questions are generated by the watchdog.

During the watchdog startup state, the LFSR is set with the initial value SEED[3:0], which is located in the WDT_QA_CFG register in BANK1. SEED[3:0] has a default value of 0000b.
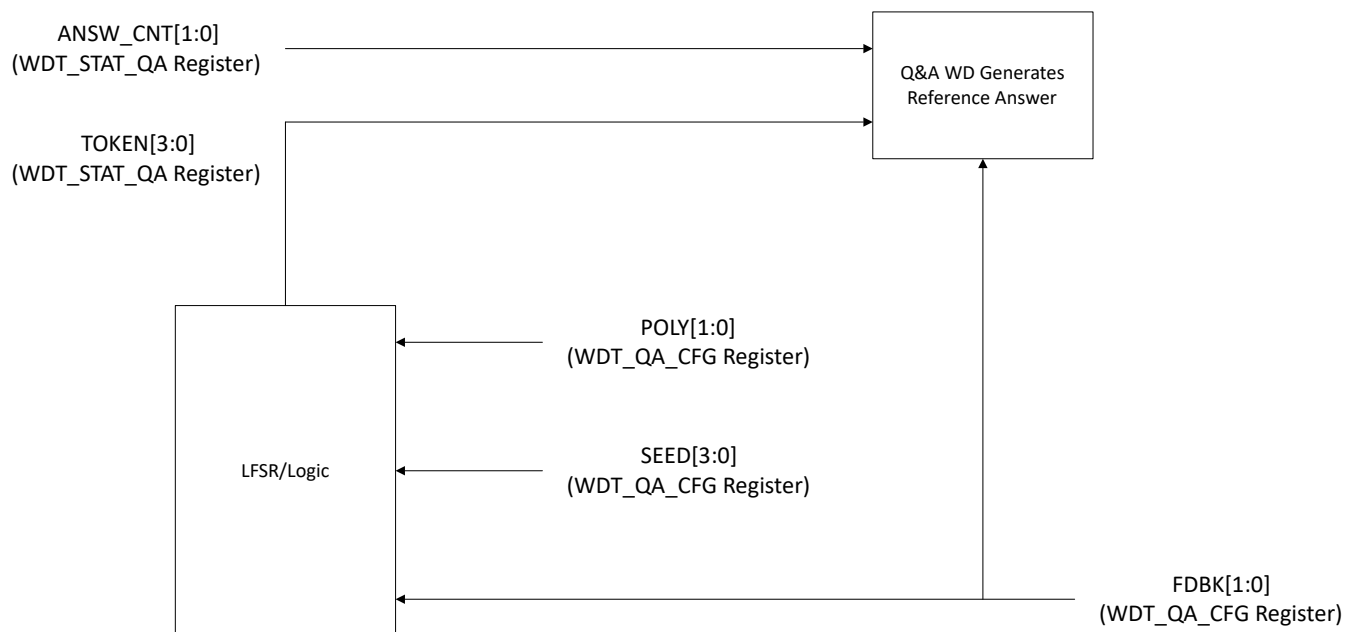
**Figure 7-9. Watchdog Question Generation**

At the end of a good event, the Token Counter is incremented, and the value of TOKEN[3:0] will change as a result of the mux and logic combinations shown in Figure 7-10.

**A.** A value of 0000b is a special seed and equates to 0001b, including the default loading of 0000b during power up.

**Figure 7-10. Watchdog Question and Token Generation**

Once the Token Counter has reached the maximum value of 1111b, the counter will reset and provide a clock pulse to the LFSR. The clock pulse will left shift the value stored in the LFSR, which changes the value of the TOKEN[3:0]. During the special case of SEED[3:0] = 0000b, Bit 0 of the LFSR will be incremented the first time the Token Counter resets. Subsequent Token Counter resets will provide the typical clock pulse that left-shifts the LFSR. While left shifting, the value of seed will cycle through values 1 to 15 as listed in Figure 7-10.

The mux devices that generate TOKEN[3:0] are configured using FDBK[1:0] (WDT_QA_CFG register in BANK1). It is not necessary to change the value of FDBK[1:0] from the default value of 00b, and it is important to note that changing FDBK[1:0] also changes the logic equations required to calculate the reference answer. The different reference answer logic equations are listed below:

For FDBK[1:0] = 00b :

- Reference-Answer[0] = TOKEN[0] XOR (TOKEN[3] XOR ANSW_CNT[1])
- Reference-Answer[1] = TOKEN[0] XOR (TOKEN[1] XOR TOKEN[2]) XOR ANSW_CNT[1]
- Reference-Answer[2] = TOKEN[0] XOR (TOKEN[3] XOR TOKEN[1]) XOR ANSW_CNT[1]
- Reference-Answer[3] = TOKEN[2] XOR (TOKEN[0] XOR TOKEN[3]) XOR ANSW_CNT[1]

- Reference-Answer[4] = TOKEN[1] XOR ANSW_CNT[0]
- Reference-Answer[5] = TOKEN[3] XOR ANSW_CNT[0]
- Reference-Answer[6] = TOKEN[0] XOR ANSW_CNT[0]
- Reference-Answer[7] = TOKEN[2] XOR ANSW_CNT[0]

For FDBK[1:0] = 01b :

- Reference-Answer[0] = TOKEN[1] XOR (TOKEN[2] XOR ANSW_CNT[1])
- Reference-Answer[1] = TOKEN[1] XOR (TOKEN[1] XOR TOKEN[1]) XOR ANSW_CNT[1]
- Reference-Answer[2] = TOKEN[3] XOR (TOKEN[2] XOR TOKEN[1]) XOR ANSW_CNT[1]
- Reference-Answer[3] = TOKEN[1] XOR (TOKEN[3] XOR TOKEN[3]) XOR ANSW_CNT[1]
- Reference-Answer[4] = TOKEN[0] XOR ANSW_CNT[0]
- Reference-Answer[5] = TOKEN[2] XOR ANSW_CNT[0]
- Reference-Answer[6] = TOKEN[3] XOR ANSW_CNT[0]
- Reference-Answer[7] = TOKEN[1] XOR ANSW_CNT[0]

For FDBK[1:0] = 10b :

- Reference-Answer[0] = TOKEN[2] XOR (TOKEN[1] XOR ANSW_CNT[1])
- Reference-Answer[1] = TOKEN[2] XOR (TOKEN[0] XOR TOKEN[1]) XOR ANSW_CNT[1]
- Reference-Answer[2] = TOKEN[1] XOR (TOKEN[1] XOR TOKEN[1]) XOR ANSW_CNT[1]
- Reference-Answer[3] = TOKEN[0] XOR (TOKEN[2] XOR TOKEN[3]) XOR ANSW_CNT[1]
- Reference-Answer[4] = TOKEN[2] XOR ANSW_CNT[0]
- Reference-Answer[5] = TOKEN[1] XOR ANSW_CNT[0]
- Reference-Answer[6] = TOKEN[2] XOR ANSW_CNT[0]
- Reference-Answer[7] = TOKEN[0] XOR ANSW_CNT[0]

For FDBK[1:0] = 11b

- Reference-Answer[0] = TOKEN[3] XOR (TOKEN[0] XOR ANSW_CNT[1])
- Reference-Answer[1] = TOKEN[3] XOR (TOKEN[3] XOR TOKEN[1]) XOR ANSW_CNT[1]
- Reference-Answer[2] = TOKEN[1] XOR (TOKEN[0] XOR TOKEN[1]) XOR ANSW_CNT[1]
- Reference-Answer[3] = TOKEN[3] XOR (TOKEN[1] XOR TOKEN[3]) XOR ANSW_CNT[1]
- Reference-Answer[4] = TOKEN[3] XOR ANSW_CNT[0]
- Reference-Answer[5] = TOKEN[0] XOR ANSW_CNT[0]
- Reference-Answer[6] = TOKEN[1] XOR ANSW_CNT[0]
- Reference-Answer[7] = TOKEN[3] XOR ANSW_CNT[0]

Example code for answer calcultion when FDBK[1:0] = 00b is included in Figure 7-11.



**Figure 7-11. Watchdog Answer Calculation Code for FDBK[1:0] = 00b**

### 7.3.9.2 Q&A Watchdog Open and Close Window Delay

Open and Close window delay can be adjusted through register 0xAC and 0xAB repectively. During a reset event, the Open and Close window delays do not change from the programmed value (default OTP or user changes). Table 7-3 lists delay time and associated register value.

**Table 7-3. Open and Close Window Delay**

| Reg Value | Time | Notes |
|---|---|---|
| 0-31 | 1-32 ms | 1 ms steps |
| 32-63 | 34-96 ms | 2 ms steps |
| 64-255 | 100-864 ms | 4 ms steps |

The startup delay is calculated using the WDT_Startup_DLY_MULTIPLIER[2:0] (register 0xAA), Close window delay, and the Open window delay. It is important to note that changing either the Close window delay or the Open window delay will change the resulting startup delay. Use Equation 3 to calculate total startup delay.

$$t_{Startup} = (WDT\_Startup\_DLY\_MULTIPLIER+1)*(WDT\_OPEN+WDT\_CLOSE) \tag{3}$$

### 7.3.9.3 Q&A Watchdog Status Register

Read status register 0x37 to determine watchdog state of operation. Table 7-4 provides the operating state with its associated value. Bits ST_WDUV and ST_WDEXP of register 0x37 are cleared when read.

**Table 7-4. Q&A Watchdog Operating State**

| OPERATING STATE | STATE DESCRIPTION | VALUE |
|---|---|---|
| IDLE | WD is wating for a fault to be cleared or WDE is low. The violation count is reset. | 0x00 |
| OPEN | WD open window. | 0x01 |
| CLOSE | WD close window. | 0x02 |
| START UP | WD startup window. | 0x03 |
| SUSPEND | WDE is high and another fault has asserted output pins unrelated to the WD, or I$^2$C MR bit is set to 1. Violation count remains unchanged. | 0x04 |

### 7.3.9.4 Q&A Watchdog Timing
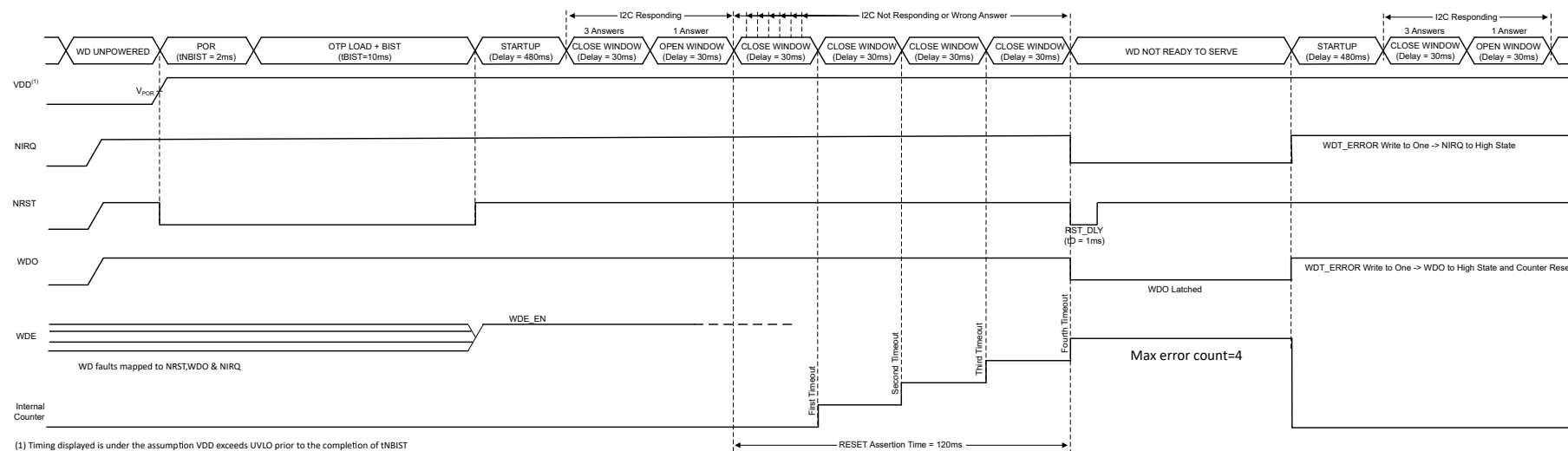


**Figure 7-12. TPS389C03 CLOSE Window Error WDO Latched**
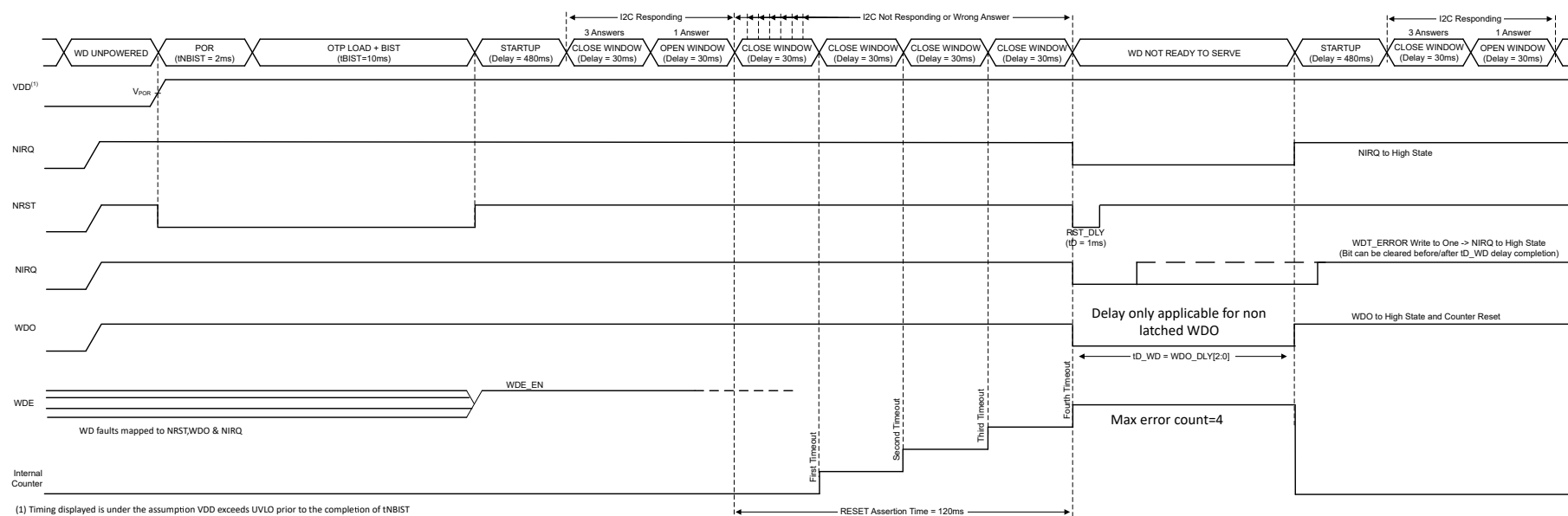
**Figure 7-13. TPS389C03 CLOSE Window Error WDO Delay**
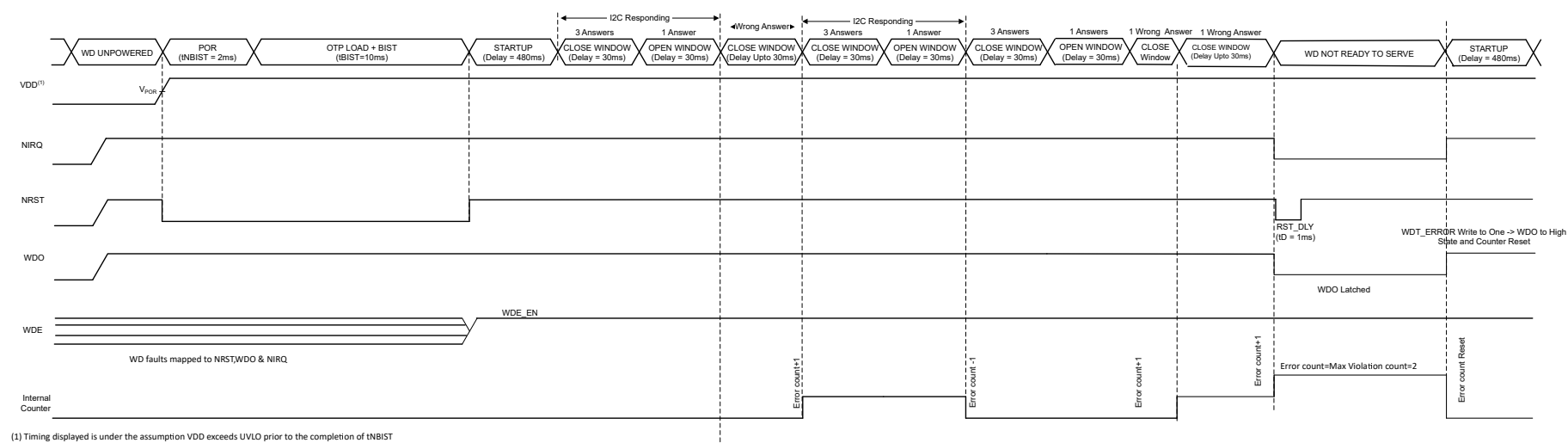


**Figure 7-14. TPS389C03 CLOSE Window Error WDO Delay with Max Violation Count Reached**
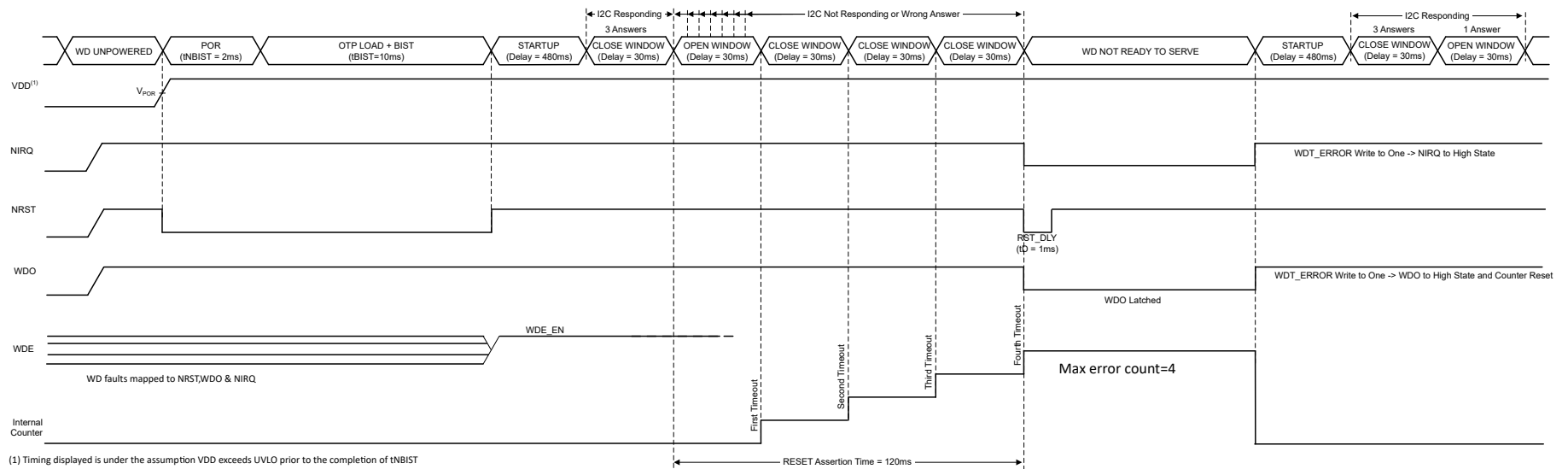
**Figure 7-15. TPS389C03 OPEN Window Error WDO Latched**
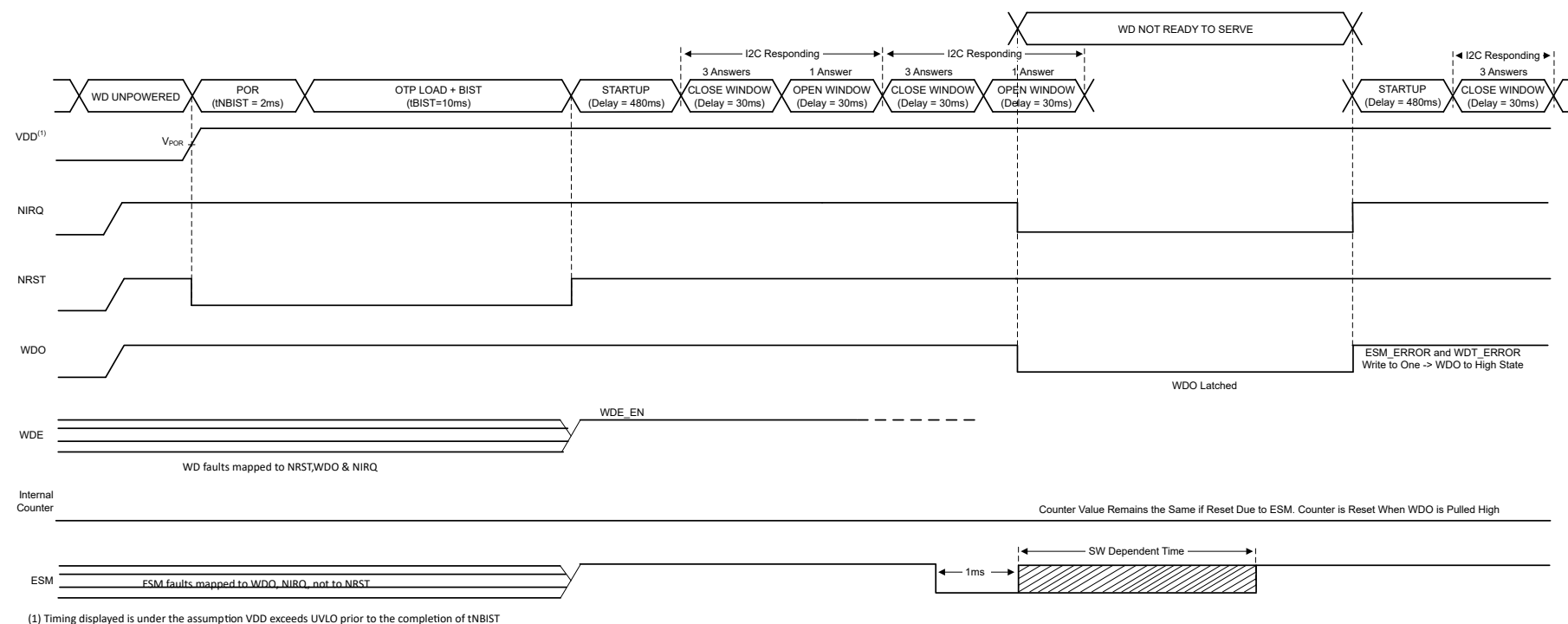
**Figure 7-16. TPS389C03 ESM Error with No WD Faults**
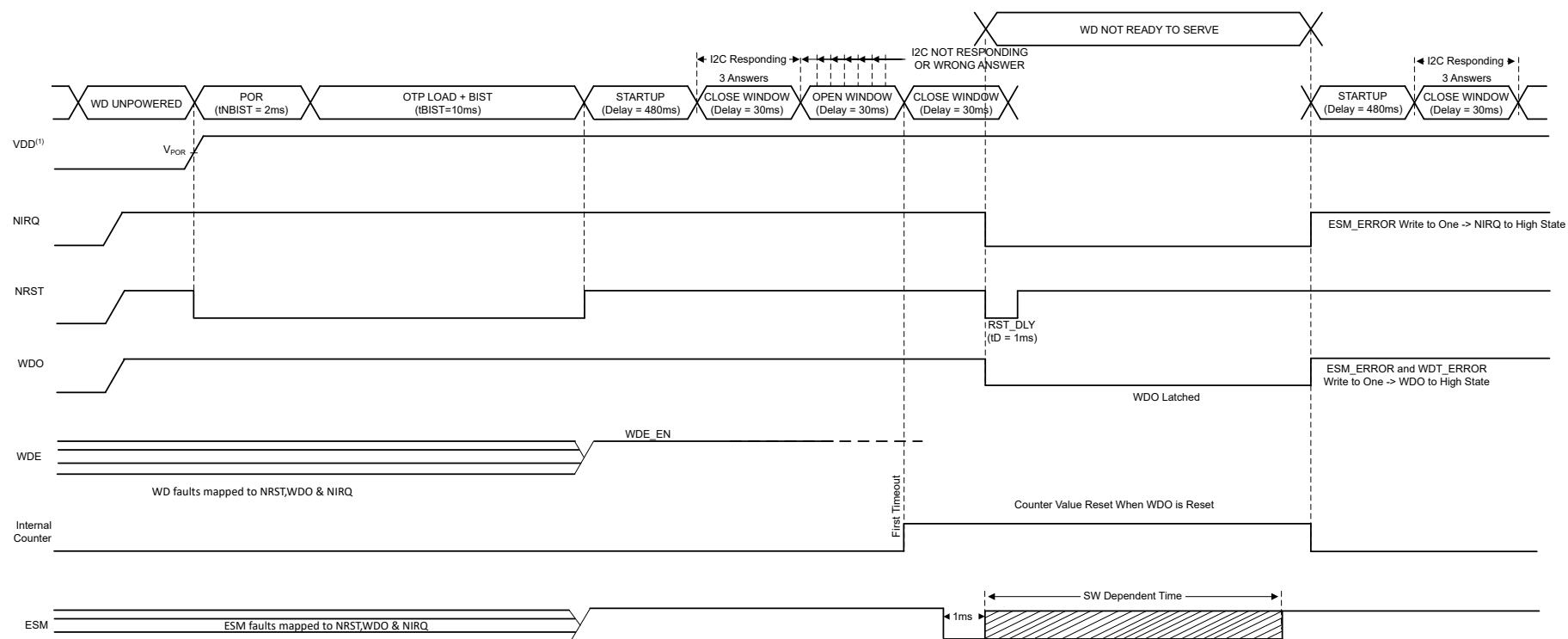
**Figure 7-17. TPS389C03 ESM Error After WD Time-out**

### 7.3.9.5 Q&A Watchdog State Machine and Test Program

The flowchart shown in Figure 7-18 and Figure 7-19 describes the operation of the Q&A watchdog with an MCU. The associated state machine diagram drawn in Figure 7-20 is referenced to Table 7-4 and describes the transition between states for the Q&A watchdog.

The single test program in Figure 7-21 to Figure 7-23 demonstrates how the watchdog can be tested.
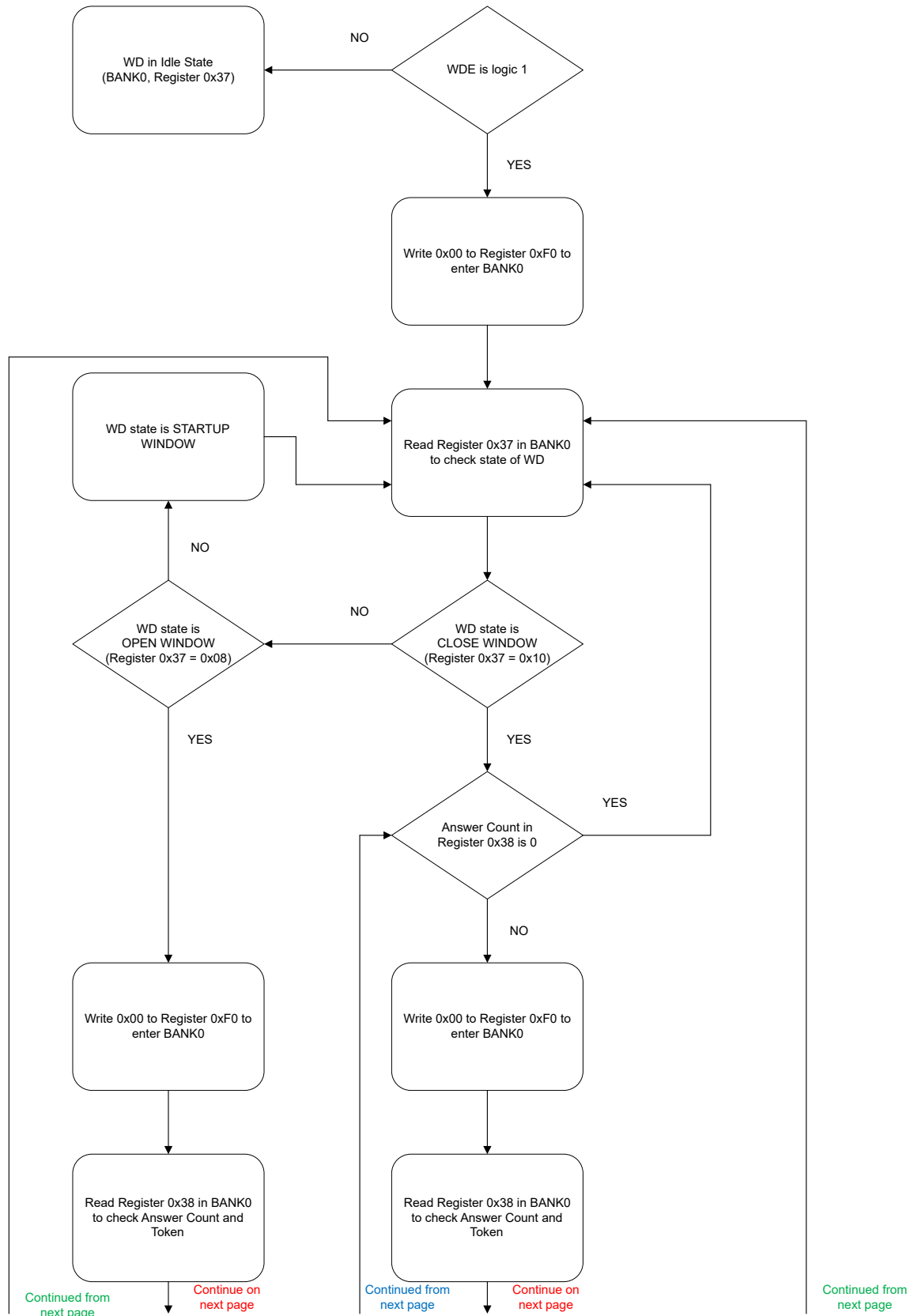
**Figure 7-18. Q&A Watchdog Operation Flowchart Page 1**
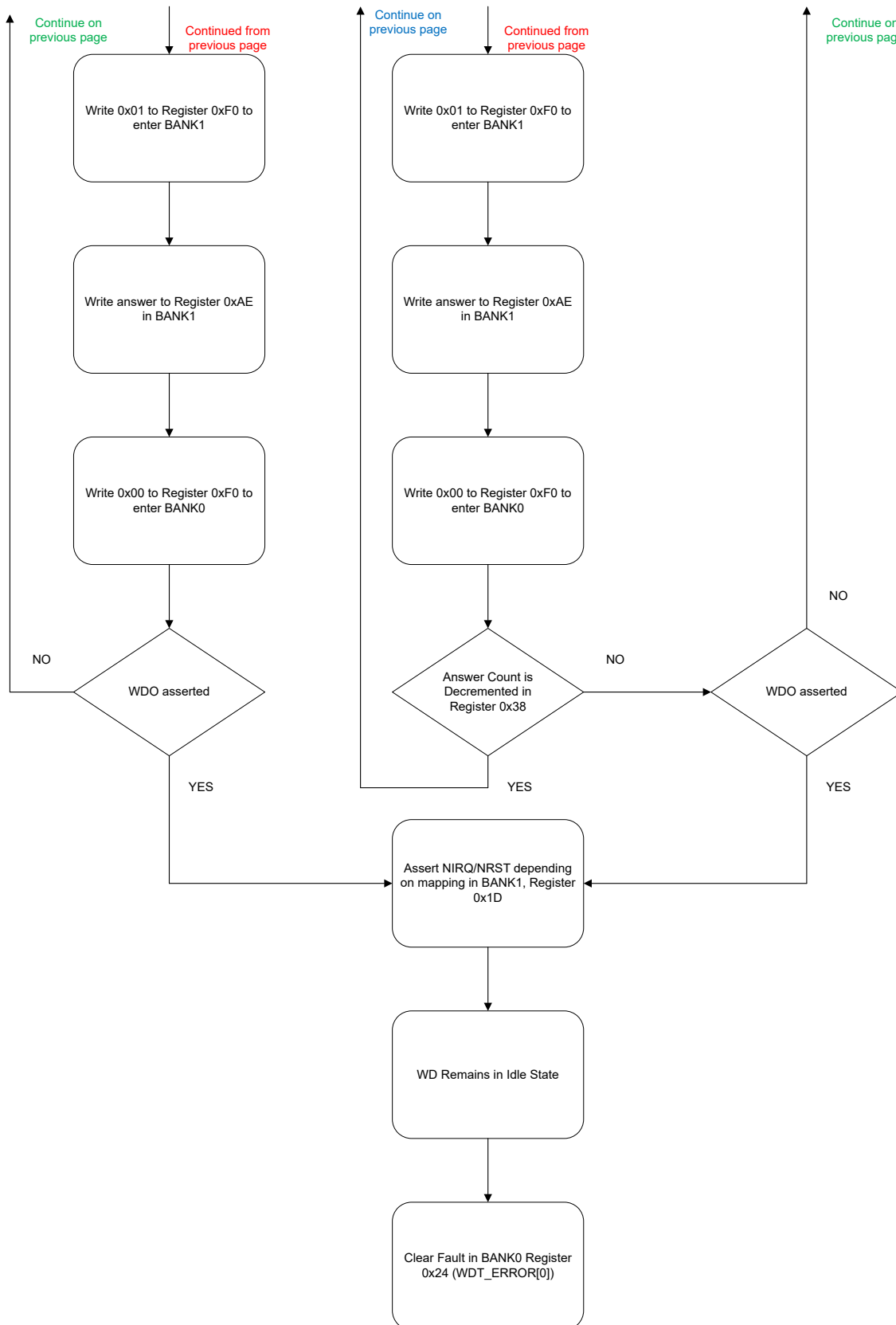
**Figure 7-19. Q&A Watchdog Operation Flowchart Page 2**
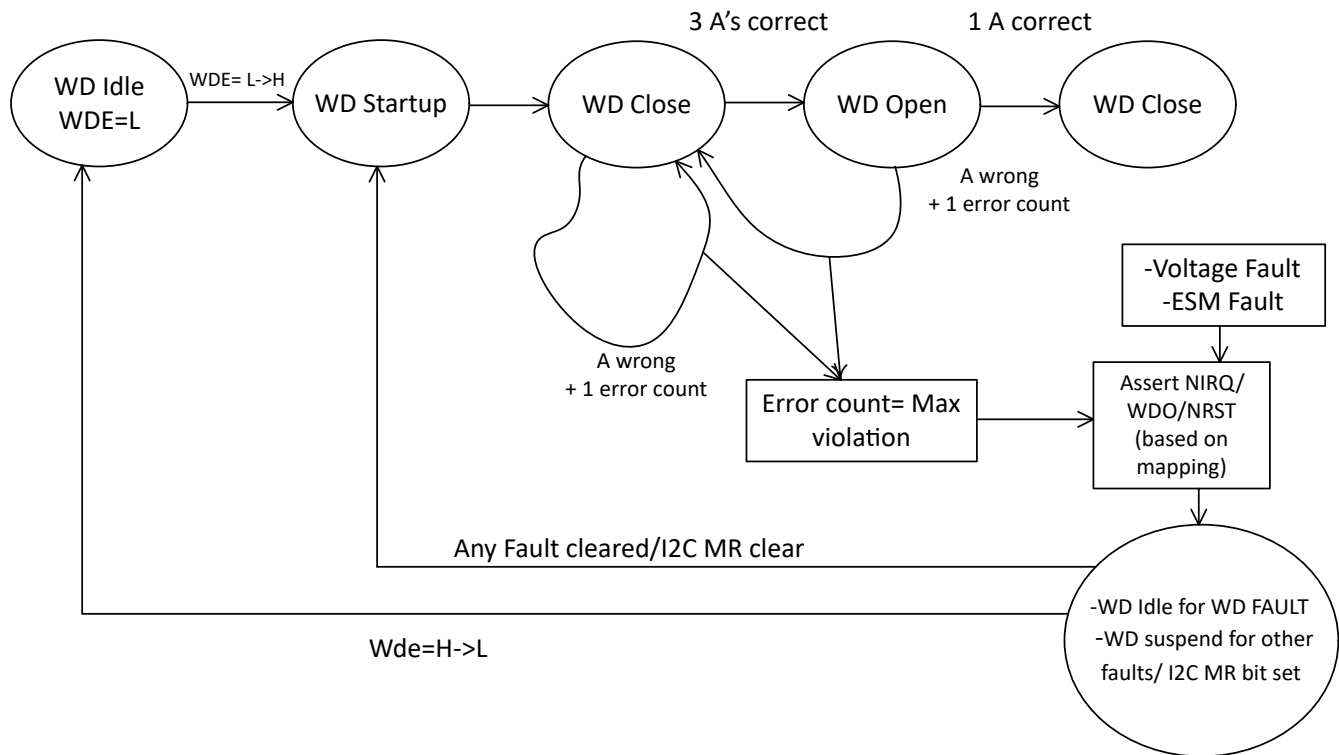
**Figure 7-20. Q&A Watchdog State Diagram**
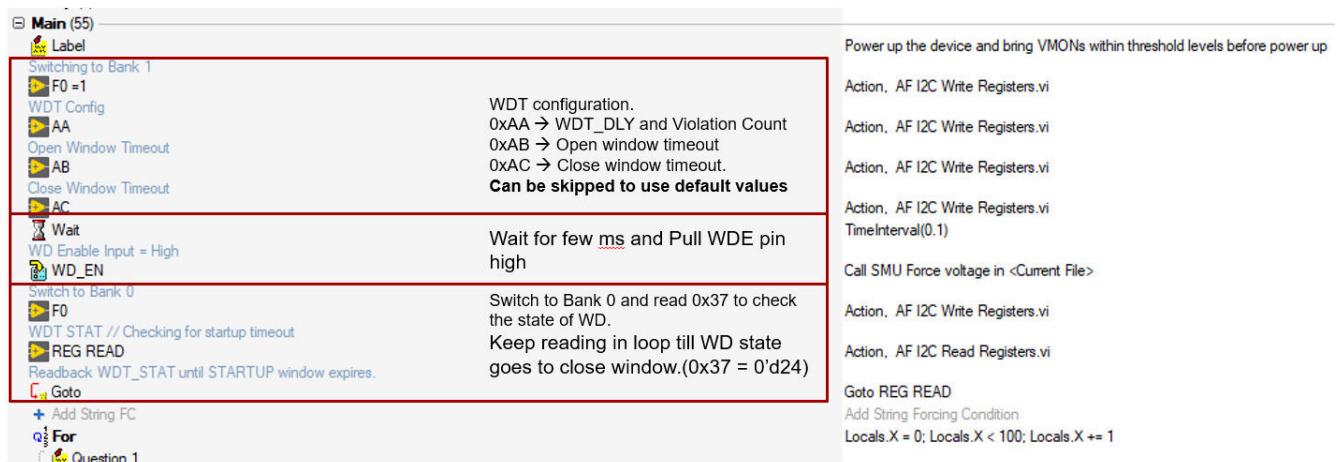


**Figure 7-21. Q&A Watchdog Test Program Page 1**
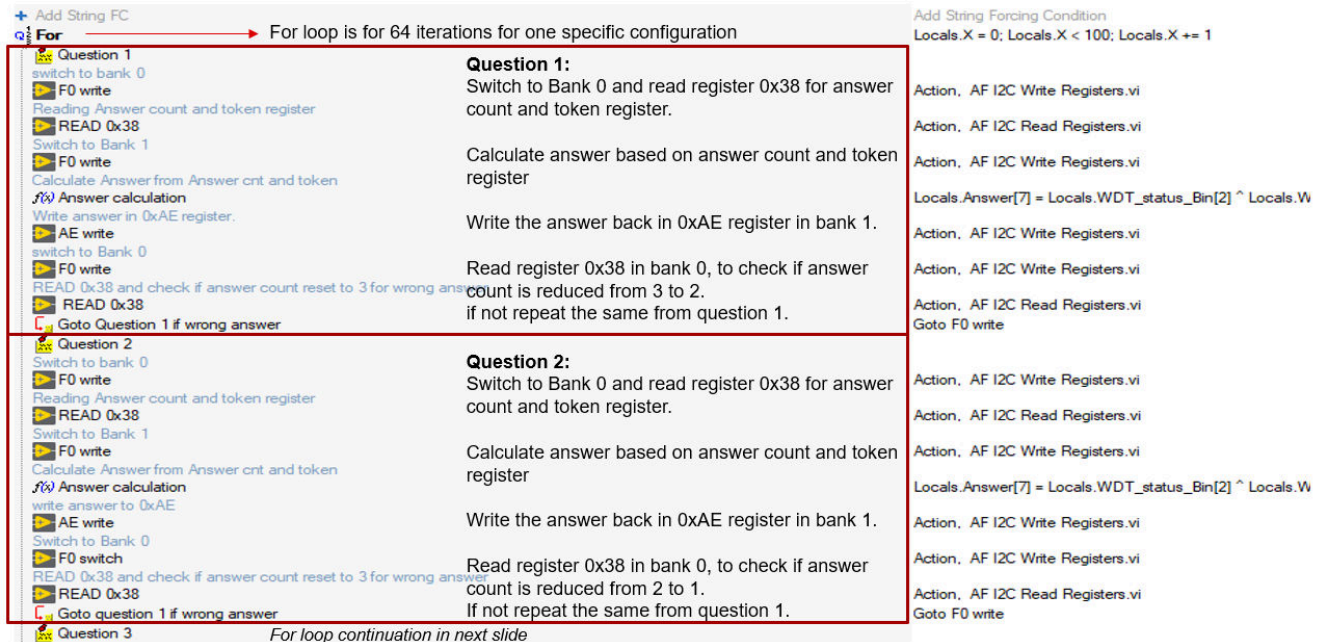
**Figure 7-22. Q&A Watchdog Test Program Page 2**
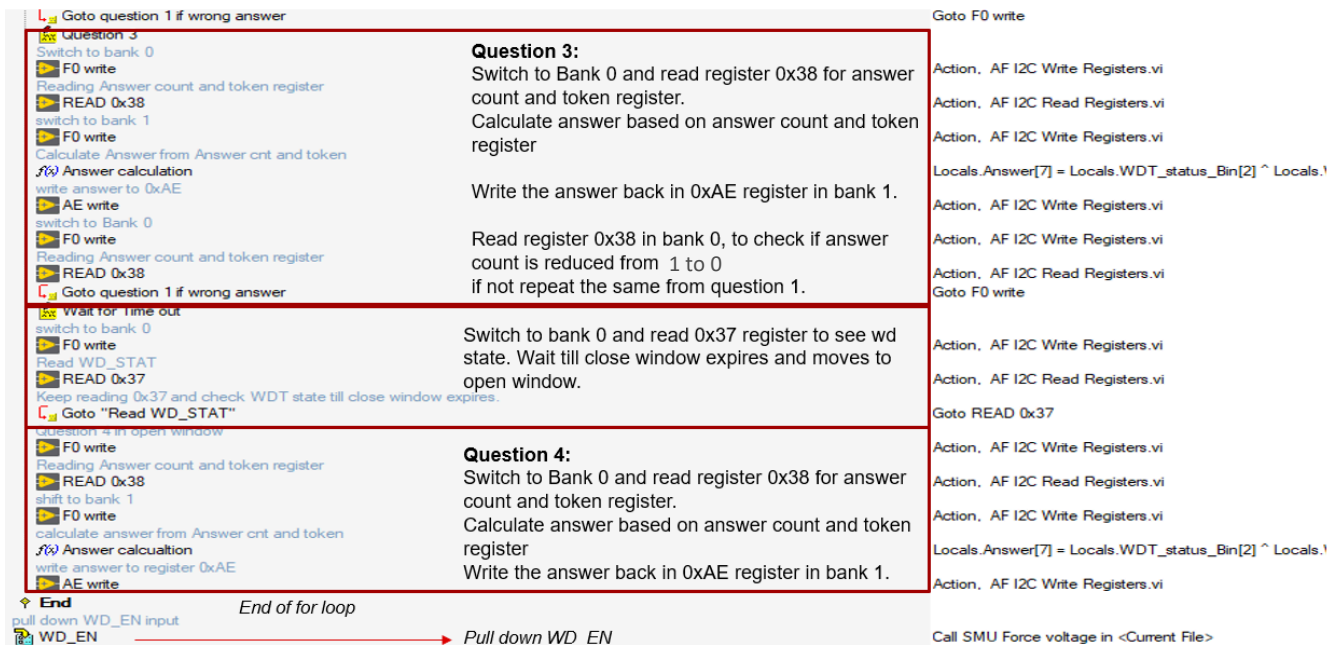


**Figure 7-23. Q&A Watchdog Test Program Page 3**

### 7.3.10 Error Signal Monitoring (ESM)

The Error Signal Monitoring (ESM) pin is used to monitor the error output of the SOC or microcontroller. The internal types of errors that need to happen to assert the ESM pin low can be configured in the microcontroller. Once the ESM pin is asserted low, the actions or results of the microcontroller cannot be relied on. The ESM pin has a programmable threshold delay (Bank 1_0x09E_Threshold) to prevent unintended false trips. The ESM pin also has a configurable debounce (Bank 1_0x09F_ESM_DEB). When the ESM pin of TPS389C03-Q1 is asserted low an ESM_ERROR will be flagged by a bit located in the INT_VENDOR register. The ESM pin is pulled low by default through an internal 100k pull-down resistance, thus an ESM_ERROR will be flagged by

default if no external source is applied to the ESM pin. Note the pull down resistor is only active when VDD has been applied, otherwise the pin is left floating.

**Table 7-5. ESM Threshold Delay Time**

| REG VALUE | TIME | NOTES |
|---|---|---|
| 0-31 | 1-32 ms | 1 ms steps |
| 32-63 | 34-96 ms | 2 ms steps |
| 64-255 | 100-864 ms | 4 ms steps |

The configurations listed in Table 7-6 to Table 7-12 demonstrate how TPS389C03-Q1 responds when mapped to different fault outputs such as NRST, NIRQ and WDO. Faults mapped to NIRQ are always latched. Faults mapped to WDO can be latched or have an associated WDO delay based on the OTP setting. If the ESM function is being used as a reset method, then it is recommended to map ESM to WDO to avoid NRST toggling. If WDE is pulled low in operation, it is recommended to have ESM fault mapped only to NIRQ.

When ESM is mapped to WDO, an ESM fault, with the resulting WDO assertion, will not be flagged in the WDT_ERROR bit. However, it is recommended to write 1 to the WDT_ERROR bit and the ESM_ERROR bit found in the INT_VENDOR (Section 8.1.1.9 ) register to clear all of the latched outputs. The WDO output can also be deasserted by toggling the WDE pin.

**Table 7-6. ESM Mapped to WDO, NIRQ, and NRST**

| | WDE | WDO | NIRQ | NRST |
|---|---|---|---|---|
| ESM fault | High | After ESM delay, WDO asserted and ESM fault set. I2C write to clear and deassert. | After ESM delay, NIRQ asserted and ESM fault set. I2C write to clear and deassert. | After ESM delay, NRST asserted and deasserted after reset delay. ESM pin state not checked until WDO is deasserted. |
| | Low | ESM fault not asserted WDO. | After ESM delay, NIRQ asserted and ESM fault set. I2C write to clear and deassert. | After ESM delay, NRST asserted and deasserted after reset delay. ESM pin state checked after ESM delay. If ESM stays low, NRST will toggle. |

**Table 7-7. ESM Mapped to NIRQ and NRST**

| | WDE | WDO | NIRQ | NRST |
|---|---|---|---|---|
| ESM fault | High | Not asserted. | After ESM delay, NIRQ asserted and ESM fault set. I2C write to clear and deassert. | After ESM delay, NRST asserted and deasserted after reset delay. ESM pin state checked after ESM delay. If ESM stays low, NRST will toggle. |
| | Low | Not asserted. | After ESM delay, NIRQ asserted and ESM fault set. I2C write to clear and deassert. | After ESM delay, NRST asserted and deasserted after reset delay. ESM pin state checked after ESM delay. If ESM stays low, NRST will toggle. |

**Table 7-8. ESM Mapped to WDO and NIRQ**

|  | WDE | WDO | NIRQ | NRST |
|---|---|---|---|---|
| ESM fault | High | After ESM delay, WDO asserted and ESM fault set. I2C write to clear and deassert. | After ESM delay, NIRQ asserted and ESM fault set. I2C write to clear and deassert. | Not asserted. |
|  | Low | Not asserted. | After ESM delay, NIRQ asserted and ESM fault set. I2C write to clear and deassert. | Not asserted. |

**Table 7-9. ESM Mapped to WDO and NRST**

|  | WDE | WDO | NIRQ | NRST |
|---|---|---|---|---|
| ESM fault | High | After ESM delay, WDO asserted and ESM fault set. I2C write to clear and deassert. | Not asserted. | After ESM delay, NRST asserted and deasserted after reset delay. ESM pin state not checked until WDO is deasserted. |
|  | Low | Not asserted. | Not asserted. | After ESM delay, NRST asserted and deasserted after reset delay. ESM pin state checked after ESM delay. If ESM stays low NRST will toggle. |

**Table 7-10. ESM Mapped to NRST**

|  | WDE | WDO | NIRQ | NRST |
|---|---|---|---|---|
| ESM fault | High | Not asserted. | Not asserted. | After ESM delay, NRST asserted and deasserted after reset delay. ESM pin state checked after ESM delay. If ESM stays low NRST will toggle. |
|  | Low | Not asserted. | Not asserted. | After ESM delay, NRST asserted and deasserted after reset delay. ESM pin state checked after ESM delay. If ESM stays low NRST will toggle. |

**Table 7-11. ESM Mapped to NIRQ**

|  | WDE | WDO | NIRQ | NRST |
|---|---|---|---|---|
| ESM fault | High | Not asserted. | After ESM delay, NIRQ asserted and ESM fault set. I2C write to clear and deassert. | Not asserted. |
|  | Low | Not asserted. | After ESM delay, NIRQ asserted and ESM fault set. I2C write to clear and deassert. | Not asserted. |

**Table 7-12. ESM Mapped to WDO**

|  | WDE | WDO | NIRQ | NRST |
|---|---|---|---|---|
| ESM fault | High | After ESM delay, WDO asserted and ESM fault set. I2C write to clear and deassert. | Not asserted. | Not asserted. |
|  | Low | ESM fault not asserted WDO. | Not asserted. | Not asserted. |

Product Folder Links: *TPS389C03-Q1*

### 7.3.10.1 ESM Timing

The timing diagrams starting from Figure 7-24 to Figure 7-27 show the behavior for a latched WDO fault pin. Faults mapped to NRST have an associated reset delay based on (Bank 1_0x9F_RST_DLY). For each diagram, the assumed system configuration is that once the microcontroller is reset, it restarts with ESM fault cleared or ESM pin high.



(1) Timing displayed is under the assumption VDD exceeds UVLO prior to the completion of tNBIST
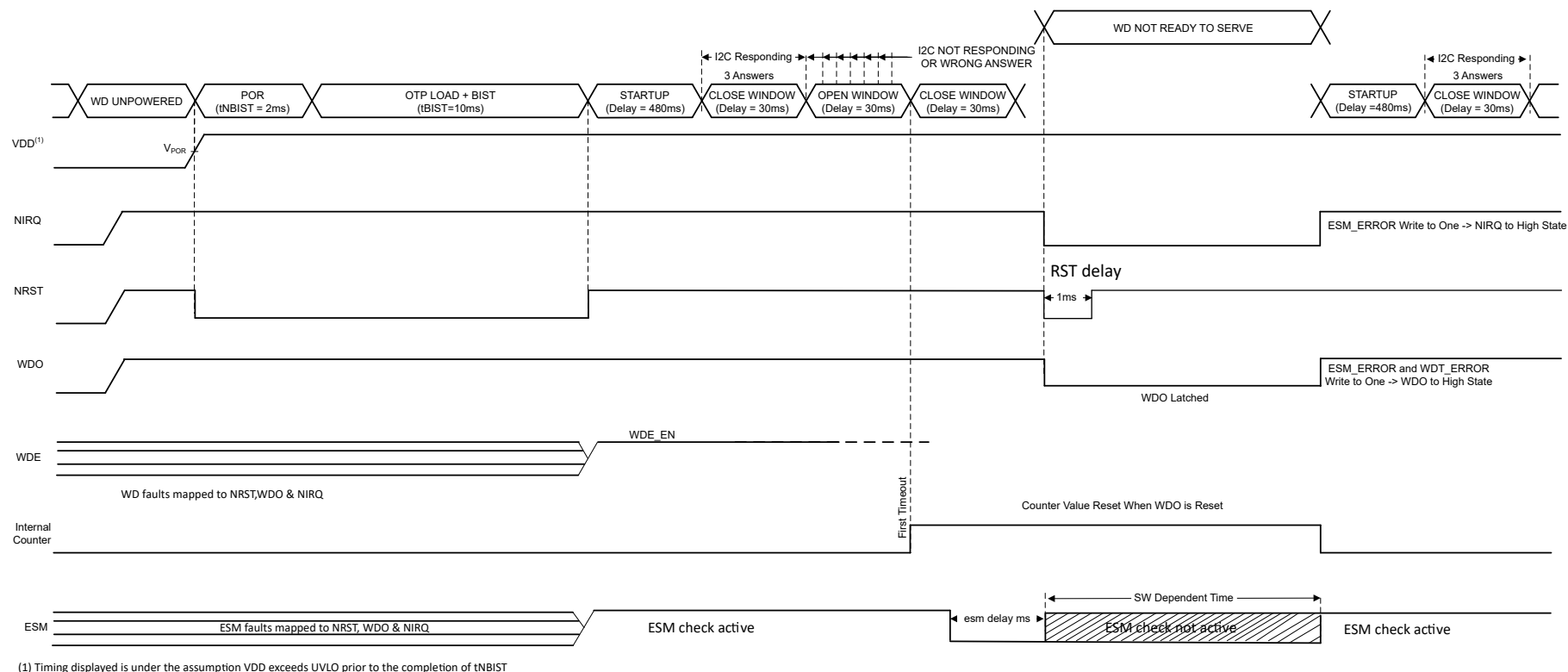
**Figure 7-24. WD Error Followed by ESM Fault (WD Enabled)**
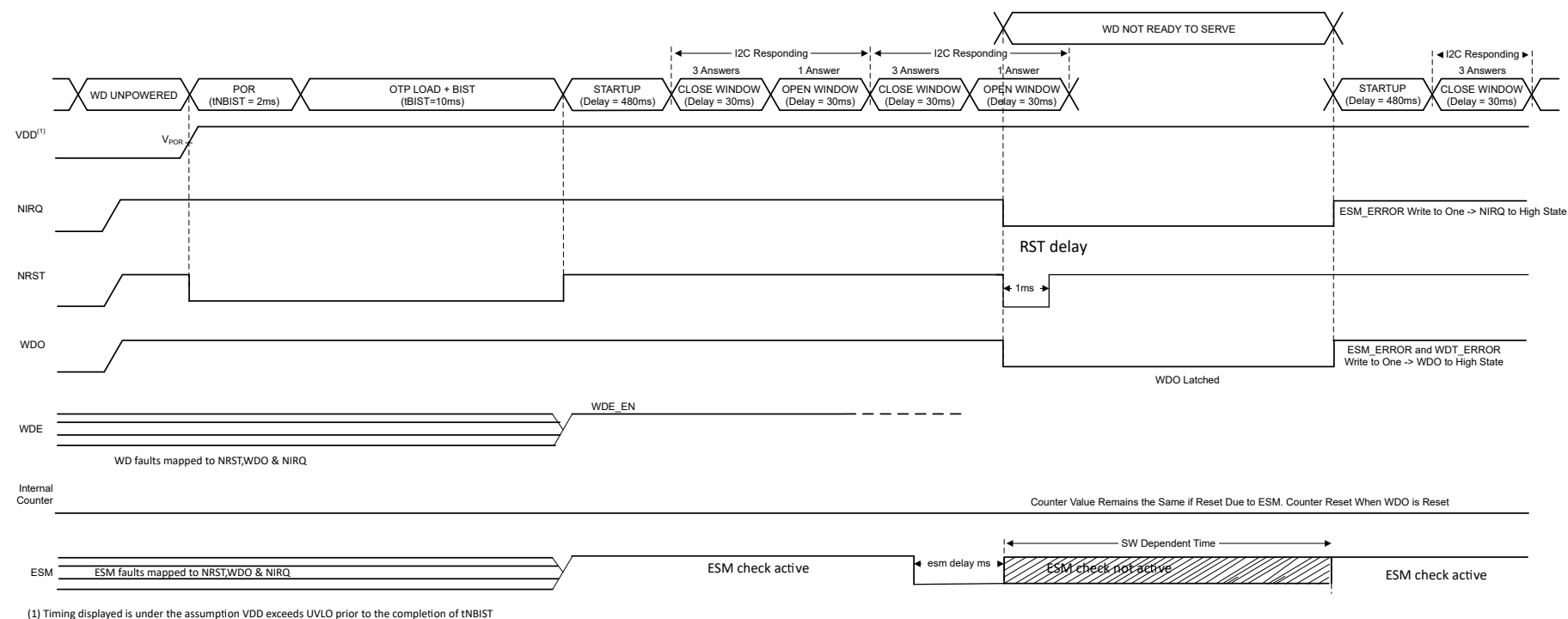
**Figure 7-25. ESM Fault (WD Enabled)**

(1) Timing displayed is under the assumption VDD exceeds UVLO prior to the completion of tNBIST
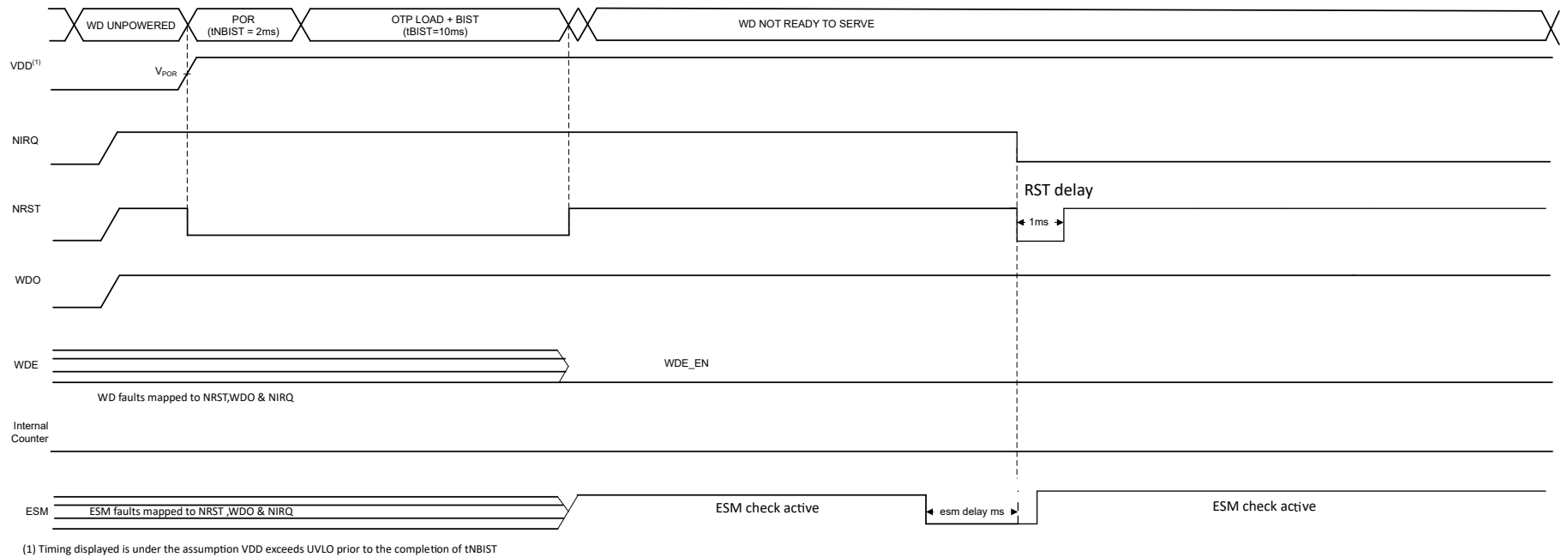
**Figure 7-26. Transient ESM Fault (WD Disabled)**
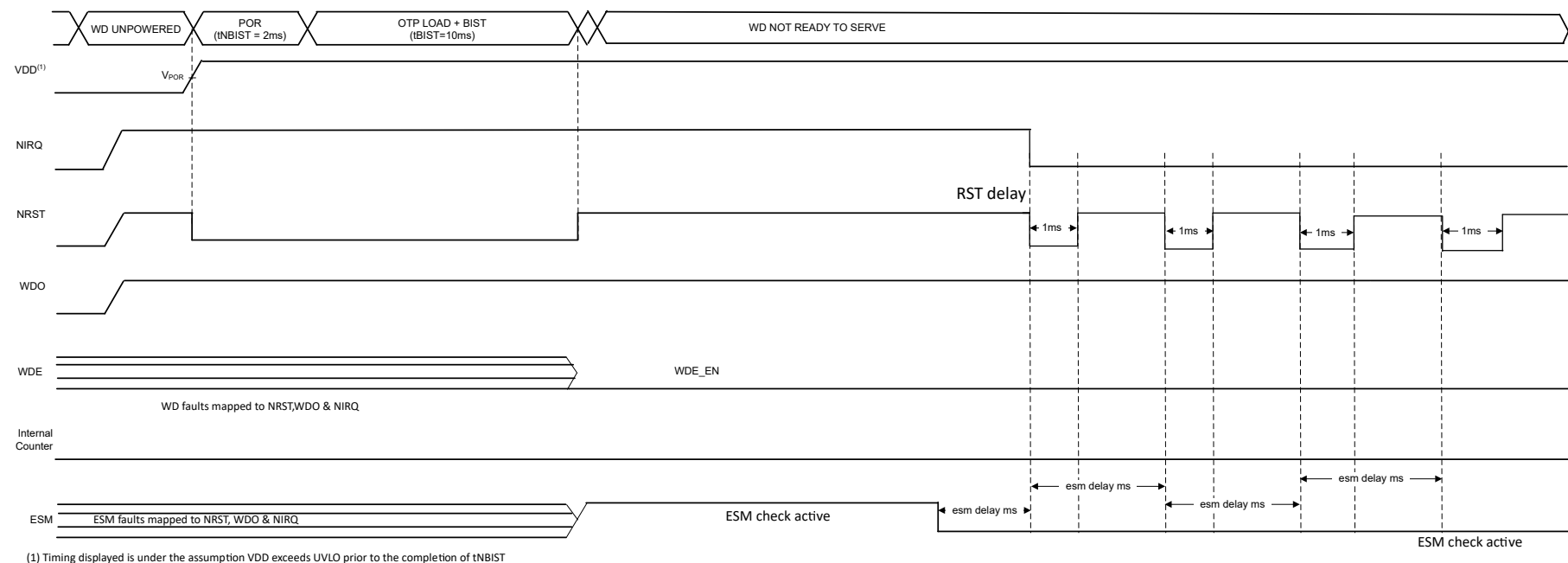
**Figure 7-27. Permanent ESM Fault (WD Disabled)**

## 7.4 Device Functional Modes

The TPS389C03-Q1 has three key functional modes that the device may enter over the course of operation. When no power is applied to the device, it will be in the OFF state where the monitoring channels and the watchdog will be inactive. Once VDD is greater than UVLO, the device will enter the ACTIVE state after the BIST and OTP loading have finished. During the ACTIVE state, the device will be capable of full monitoring and the watchdog will be active. If a BIST failure, double-error detect (DED) during the OTP loading, thermal shutdown, or an address pin fault occurs, the device will enter the FAILSAFE mode. Once in FAILSAFE, NRST and NIRQ are asserted low. To leave the FAILSAFE state, power to the TPS389C03-Q1 must be cycled. Reading register 0x30 in BANK0 provides information on the state of the device. See Section 8.1.1.10 for details. The state diagram drawn in Figure 7-28 follows the progression through each state.
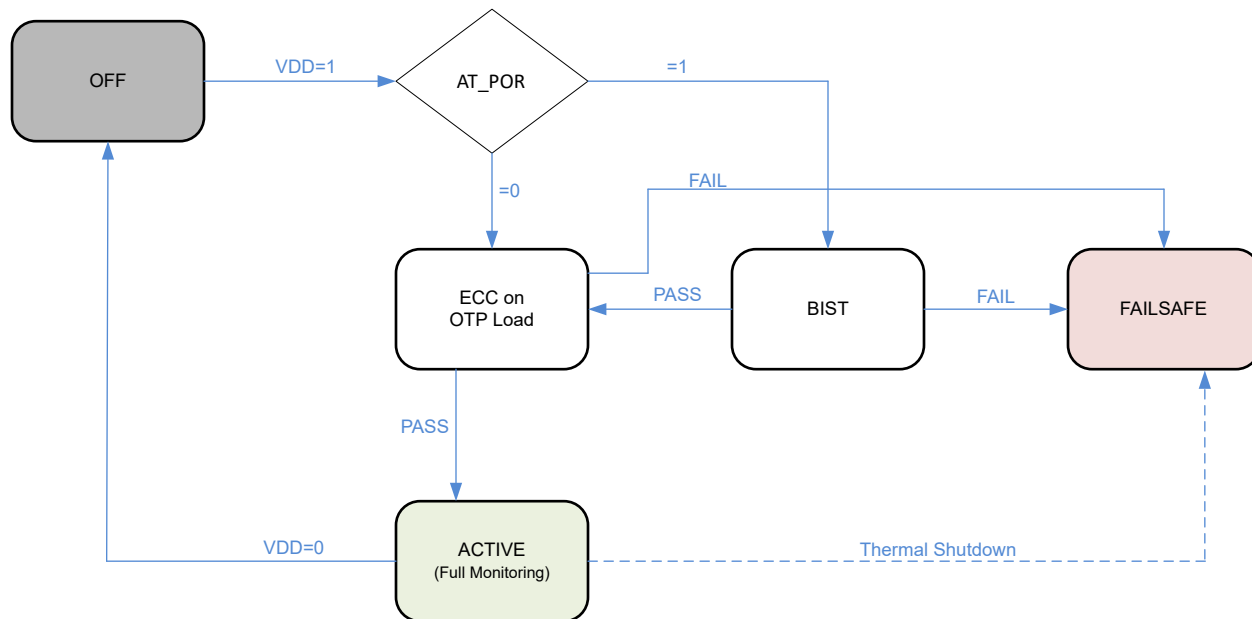


**Figure 7-28. TPS389C03-Q1 State Diagram**

### 7.4.1 Built-In Self Test and Configuration Load

Built-In Self Test (BIST) is performed at Power On Reset (POR), if TEST_CFG.AT_POR=1.

Configuration load from OTP is assisted by ECC (supporting SEC-DED). This is to protect against data integrity issues and to maximize system availability.

During BIST, NIRQ is de-asserted (asserted in case of failure), input pins are ignored, and the I$^2$C block is inactive with SDA and SCL de-asserted. The BIST includes device testing to meet the Technical Safety Requirements. Once BIST is completed without failure, I$^2$C is immediately active and the device enters the ACTIVE state after loading the configuration data from OTP. If BIST fails and/or ECC reports Double-Error Detection (DED), NIRQ is asserted low, NRST is asserted low, the device enters FAILSAFE state, and a best effort attempt is made to keep I$^2$C active. The TEST_INFO register found in Section 8.1.1.11 provides information on the test coverage and results.

The detailed behavior upon success/failure of the BIST is controlled by INT_TEST and IEN_TEST registers. Reporting of the BIST results is carried out through:
- NIRQ pin: pulled low depending on the test result and BIST_C and BIST bits in IEN_TEST
- I_BIST_C and BIST bits in INT_TEST register depending on IEN_TEST settings
- VMON_STAT.ST_BIST_C register bit
- TEST_INFO[3:0] register bits

### 7.4.1.1 Notes on BIST Execution

Upon POR the TPS389C03-Q1 needs to make a decision whether to run BIST or not, based on the value of the TEST_CFG.AT_POR register bit. Assuming that ECC on this register is performed after BIST has checked the ECC logic itself, it is not possible to guarantee its data integrity before running BIST.

BIST can be triggered manually during normal operation by writing 1 to the ENTER_BIST bit found in BANK1 Register 0x9F. It is not reccomended to use BIST when faults are asserted by the TPS389C03-Q1.

### 7.4.2 TPS389C03-Q1 Power ON

When the TPS389C03-Q1 is powered ON, BIST is optionally executed (depending on TEST_CFG.AT_POR register bit); I$^2$C and fault reporting (through NIRQ) become active as soon as BIST is complete and configuration is loaded from OTP (assisted by ECC, supporting SEC-DED).

The details of the configuration load ECC and BIST results are reported are reported in TEST_INFO register.

Upon detection of the VDD rising edge past UVLO, the TPS389C03-Q1 starts the sequence timeout timer. The UV faults are masked until the sequence timeout has expired.
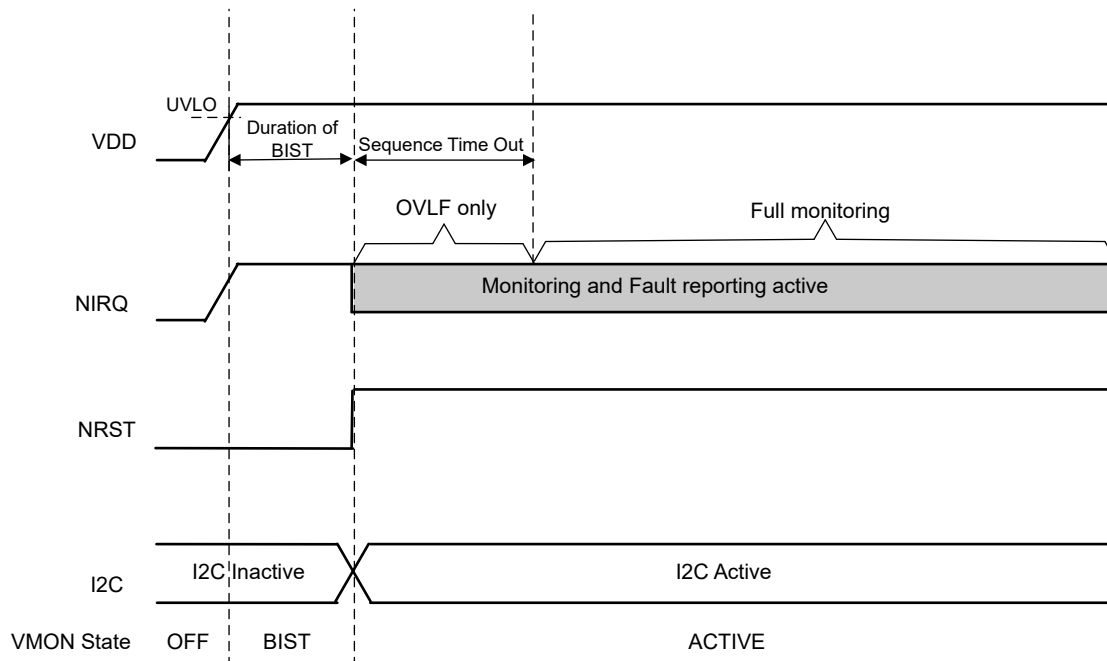


**Figure 7-29. TPS389C03-Q1 Power ON Signaling and Internal States**

BIST completion can be detected through interrupt or register polling:
- Interrupt: INT_TEST.I_BIST_C flag is set and NIRQ is asserted if IEN_TEST.BIST_C=1
- Polling: VMON_STAT register can be polled to read the ST_BIST_C bit

# 8 Register Maps

## 8.1 Registers Overview

The register map is designed to support up to 3 channels through register banks, with the following organization:

- Bank 0 - Status Register Set Summary

    - Vendor info and usage registers (bank independent)
    - Interrupt registers
    - Status registers
    - Bank selection register (bank independent)
    - Protection registers (bank independent)
    - Device configuration registers (bank independent)
- Bank 1 - Configuration Register Set Summary

    - Vendor info and usage registers (bank independent)
    - Control registers (device global registers)
    - Monitor configuration registers (channel specific registers)
    - Sequence configuration registers (both device global and channel specific registers)
    - Bank selection register (bank independent)
    - Protection registers (bank independent)
    - Device configuration registers (bank independent)

Bank independent registers are accessible at the same address irrespective of the current bank selection. Access to other registers requires the proper bank being selected.

All registers are 8-bit wide, and are loaded at boot with the default value described here or with the OTP value programmed at the factory. Unused registers addresses are reserved for future use and support up to 3 channels.

Write accesses to protected registers (see PROT1/2 details), invalid registers, or valid registers with invalid data, should be NACK'd.

If the default value found in the register map is listed as "X", then the value can be found in TPS389C0300CRTERQ1 OTP Configuration.

### 8.1.1 BANK0 Registers

Table 8-1 lists the memory-mapped registers for the BANK0 registers. All register offset addresses not listed in Table 8-1 should be considered as reserved locations and the register contents should not be modified.

**Table 8-1. BANK0 Registers**

| Offset | Acronym | Register Name | Section |
|--------|---------|---------------|---------|
| 10h | INT_SRC | Global Interrupt Source Status register. | Go |
| 11h | INT_MONITOR | Voltage Monitor Interrupt Status register. | Go |
| 12h | INT_UVHF | High Frequency channel Under-Voltage Interrupt Status register. | Go |
| 14h | INT_UVLF | Low Frequency channel Under-Voltage Interrupt Status register. | Go |
| 16h | INT_OVHF | High Frequency channel Over-Voltage Interrupt Status register | Go |
| 18h | INT_OVLF | Low Frequency channel Over-Voltage Interrupt Status register | Go |
| 22h | INT_CONTROL | Control and Communication Interrupt Status register. | Go |
| 23h | INT_TEST | Internal Test and Configuration Load Interrupt Status register. | Go |
| 24h | INT_VENDOR | Vendor Specific Internal Interrupt Status register. | Go |
| 30h | VMON_STAT | Status flags for internal operations and other non critical conditions. | Go |
| 31h | TEST_INFO | Internal Self-Test and ECC information. | Go |
| 32h | OFF_STAT | Channel OFF status. | Go |
| 37h | WDT_STAT | Watchdog Status | Go |
| 38h | WD_STAT_QA | Watchdog Answer Count and Token | Go |
| 41h | MON_LVL[2] | Channel 2 voltage level. | Go |
| 42h | MON_LVL[3] | Channel 3 voltage level. | Go |
| 43h | MON_LVL[4] | Channel 4 voltage level. | Go |
| F0h | BANK_SEL | Bank Select. | Go |
| F1h | PROT1 | Locks or unlocks register changes. Must match PROT2. | Go |
| F2h | PROT2 | Locks or unlocks register changes. Must match PROT1. | Go |
| F3h | PROT_MON | Locks MON registers in tandem with PROT1 and PROT2. | Go |
| F9h | I2CADDR | I2C Address | Go |
| FAh | DEV_CFG | Status of I2C interface voltage levels. | Go |

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

**Table 8-2. BANK0 Access Type Codes**

| Access Type | Code | Description |
|-------------|------|-------------|
| Read Type | | |
| R | R | Read |
| Write Type | | |
| W | W | Write |
| W1C | W 1C | Write 1 to clear |

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Product Folder Links: *TPS389C03-Q1*

**Table 8-2. BANK0 Access Type Codes (continued)**

| Access Type | Code | Description |
|---|---|---|
| Reset or Default Value | | |
| *-n* | | Value after reset or the default value |

### 8.1.1.1 INT_SRC Register (Offset = 10h) [Reset = 00h]

INT_SRC is shown in Table 8-3.

Return to the Summary Table.

Global Interrupt Source Status register.

**Table 8-3. INT_SRC Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | F_OTHER | R | 0h | Vendor internal defined faults. Details reported in INT_Vendor. Represents ORed value of all bits in INT_Vendor.<br>0 = No Vendor defined faults detected<br>1 = Vendor defined faults detected |
| 6-3 | RSVD | R | 0h | RSVD |
| 2 | TEST | R | 0h | Internal test or configuration load fault. Details reported in INT_TEST. Represents ORed value of all bits in INT_TEST.<br>0 = No test/configuration fault detected<br>1 = Test/configuration fault detected |
| 1 | CONTROL | R | 0h | Control status or communication fault. Details reported in INT_CONTROL. Represents ORed value of all bits in INT_CONTROL.<br>0 = No status or communication fault detected<br>1 = Status or communication fault detected |
| 0 | MONITOR | R | 0h | Voltage monitor fault. Details reported in INT_MONITOR. Represents ORed value of all bits in INT_MONITOR.<br>0 = No voltage fault detected<br>1 = Voltage fault detected |

### 8.1.1.2 INT_MONITOR Register (Offset = 11h) [Reset = 00h]

INT_MONITOR is shown in Table 8-4.

Return to the Summary Table.

Voltage Monitor Interrupt Status register.

**Table 8-4. INT_MONITOR Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RSVD | R | 0h | RSVD |
| 3 | OVLF | R | 0h | Over-Voltage Low Frequency Fault reported by ADC based measurement. Details reported in INT_OVLF. Represents ORed value of all bits in INT_OVLF.<br>0 = No OVLF fault detected<br>1 = OVLF fault detected |
| 2 | OVHF | R | 0h | Over-Voltage High Frequency Fault reported by comparator based monitoring. Details reported in INT_OVHF. Represents ORed value of all bits in INT_OVHF.<br>0 = No OVHF fault detected<br>1 = OVHF fault detected |

Product Folder Links: *TPS389C03-Q1*

**Table 8-4. INT_MONITOR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 1 | UVLF | R | 0h | Under-Voltage Low Frequency Fault reported by ADC based measurement. Details reported in INT_UVLF. Represents ORed value of all bits in INT_UVLF.<br>0 = No UVLF fault detected<br>1 = UVLF fault detected |
| 0 | UVHF | R | 0h | Under-Voltage High Frequency Fault reported by comparator based monitoring. Details reported in INT_UVHF. Represents ORed value of all bits in INT_UVHF.<br>0 = No UVHF fault detected<br>1 = UVHF fault detected |

### 8.1.1.3 INT_UVHF Register (Offset = 12h) [Reset = 00h]

INT_UVHF is shown in Table 8-5.

Return to the Summary Table.

High Frequency channel Under-Voltage Interrupt Status register.

**Table 8-5. INT_UVHF Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-4 | RSVD | R/W1C | 0h | RSVD |
| 3 | F_UVHF[4] | R/W1C | 0h | Under-Voltage High Frequency Fault for MON4. Trips if MON4 High Frequency signal goes below UVHF[4].<br>0 = MON4 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register)<br>1 = MON4 has UVHF fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the UVHF fault condition is also removed (MON4 High Frequency signal is above UVHF[4]). |
| 2 | F_UVHF[3] | R/W1C | 0h | Under-Voltage High Frequency Fault for MON3. Trips if MON3 High Frequency signal goes below UVHF[3].<br>0 = MON3 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register)<br>1 = MON3 has UVHF fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the UVHF fault condition is also removed (MON3 High Frequency signal is above UVHF[3]). |
| 1 | F_UVHF[2] | R/W1C | 0h | Under-Voltage High Frequency Fault for MON2. Trips if MON2 High Frequency signal goes below UVHF[2].<br>0 = MON2 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register)<br>1 = MON2 has UVHF fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the UVHF fault condition is also removed (MON2 High Frequency signal is above UVHF[2]). |
| 0 | RSVD | R/W1C | 0h | RSVD |

### 8.1.1.4 INT_UVLF Register (Offset = 14h) [Reset = 00h]

INT_UVLF is shown in Table 8-6.

Return to the Summary Table.

Low Frequency channel Under-Voltage Interrupt Status register.

Product Folder Links: TPS389C03-Q1

### Table 8-6. INT_UVLF Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RSVD | R/W1C | 0h | RSVD |
| 3 | F_UVLF[4] | R/W1C | 0h | Under-Voltage Low Frequency Fault for MON4 . Trips if MON4 Low Frequency signal goes below UVLF[4].<br>0 = MON4 has no UVLF fault detected (or interrupt disabled in IEN_UVLF register)<br>1 = MON4 has UVLF fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the UVLF fault condition is also removed (MON4 Low Frequency signal is above UVLF[4]). |
| 2 | F_UVLF[3] | R/W1C | 0h | Under-Voltage Low Frequency Fault for MON3. Trips if MON3 Low Frequency signal goes below UVLF[3].<br>0 = MON3 has no UVLF fault detected (or interrupt disabled in IEN_UVLF register)<br>1 = MON3 has UVLF fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the UVLF fault condition is also removed (MON3 Low Frequency signal is above UVLF[3]). |
| 1 | F_UVLF[2] | R/W1C | 0h | Under-Voltage Low Frequency Fault for MON2. Trips if MON2 Low Frequency signal goes below UVLF[2].<br>0 = MON2 has no UVLF fault detected (or interrupt disabled in IEN_UVLF register)<br>1 = MON2 has UVLF fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the UVLF fault condition is also removed (MON2 Low Frequency signal is above UVLF[2]). |
| 0 | RSVD | R/W1C | 0h | RSVD |

### 8.1.1.5 INT_OVHF Register (Offset = 16h) [Reset = 00h]

INT_OVHF is shown in Table 8-7.

Return to the Summary Table.

High Frequency channel Over-Voltage Interrupt Status register

### Table 8-7. INT_OVHF Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RSVD | R/W1C | 0h | RSVD |
| 3 | F_OVHF[4] | R/W1C | 0h | Over-Voltage High Frequency Fault for MON4. Trips if MON4 High Frequency signal goes above OVHF[4].<br>0 = MON4 has noOVHF fault detected (or interrupt disabled in IEN_OVHF register)<br>1 = MON4 has OVHF fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the OVHF fault condition is also removed (MON4 High Frequency signal is below OVHF[4]) |
| 2 | F_OVHF[3] | R/W1C | 0h | Over-Voltage High Frequency Fault for MON3. Trips if MON3 High Frequency signal goes above OVHF[3].<br>0 = MON3 has no OVHF fault detected (or interrupt disabled in IEN_OVHF register)<br>1 = MON3 has OVHF fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the OVHF fault condition is also removed (MON3 High Frequency signal is below OVHF[3]) |

Product Folder Links: *TPS389C03-Q1*

**Table 8-7. INT_OVHF Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 1 | F_OVHF[2] | R/W1C | 0h | Over-Voltage High Frequency Fault for MON2. Trips if MON2 High Frequency signal goes above OVHF[2].<br>0 = MON2 has no OVHF fault detected (or interrupt disabled in IEN_OVHF register)<br>1 = MON2 has OVHF fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the OVHF fault condition is also removed (MON2 High Frequency signal is below OVHF[2]) |
| 0 | RSVD | R/W1C | 0h | RSVD |

### 8.1.1.6 INT_OVLF Register (Offset = 18h) [Reset = 00h]

INT_OVLF is shown in Table 8-8.

Return to the Summary Table.

Low Frequency channel Over-Voltage Interrupt Status register

**Table 8-8. INT_OVLF Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RSVD | R/W1C | 0h | RSVD |
| 3 | F_OVLF[4] | R/W1C | 0h | Over-Voltage Low Frequency Fault for MON4. Trips if MON4 Low Frequency signal goes above OVLF[4].<br>0 = MON4 has no OVLF fault detected (or interrupt disabled in IEN_OVLF register)<br>1 = MON4 has OVLF fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the OVLF fault condition is also removed (MON4 Low Frequency signal is below OVLF[4]). |
| 2 | F_OVLF[3] | R/W1C | 0h | Over-Voltage Low Frequency Fault for MON3. Trips if MON3 Low Frequency signal goes above OVLF[3].<br>0 = MON3 has no OVLF fault detected (or interrupt disabled in IEN_OVLF register)<br>1 = MON3 has OVLF fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the OVLF fault condition is also removed (MON3 Low Frequency signal is below OVLF[3]). |
| 1 | F_OVLF[2] | R/W1C | 0h | Over-Voltage Low Frequency Fault for MON2. Trips if MON2 Low Frequency signal goes above OVLF[2].<br>0 = MON2 has no OVLF fault detected (or interrupt disabled in IEN_OVLF register)<br>1 = MON2 has OVLF fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the OVLF fault condition is also removed (MON2 Low Frequency signal is below OVLF[2]). |
| 0 | RSVD | R/W1C | 0h | RSVD |

### 8.1.1.7 INT_CONTROL Register (Offset = 22h) [Reset = 00h]

INT_CONTROL is shown in Table 8-9.

Return to the Summary Table.

Control and Communication Interrupt Status register.

**Table 8-9. INT_CONTROL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-5 | RSVD | R/W1C | 0h | RSVD |
| 4 | F_CRC | R/W1C | 0h | Runtime register CRC Fault:<br>0 = No fault detected (or IEN_CONTROL.RT_CRC is disabled)<br>1 = Register CRC fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit. The bit will be set again during next register CRC check if the same fault is detected |
| 3 | F_NIRQ | R/W1C | 0h | Interrupt pin fault (fault bit always enabled; no enable bit available):<br>0 = No fault detected on NIRQ pin<br>1 = Low resistance path to supply detected on NIRQ pin<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the NIRQ fault condition is also removed. |
| 2 | F_TSD | R/W1C | 0h | Thermal Shutdown fault:<br>0 = No TSD fault detected (or IEN_CONTROL.TSD is disabled)<br>1 = TSD fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the TSD fault condition is also removed |
| 1 | RSVD | R/W1C | 0h | RSVD |
| 0 | F_PEC | R/W1C | 0h | Packet Error Checking fault:<br>0 = PEC mismatch has not occurred (or IEN_CONTROL.PEC is disabled)<br>1 = PEC mismatch has occurred, or VMON_MISC.REQ_PEC=1 and PEC is missing in a write transaction<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit. The bit will be set again during next I2C transaction if the same fault is detected. |

### 8.1.1.8 INT_TEST Register (Offset = 23h) [Reset = 00h]

INT_TEST is shown in Table 8-10.

Return to the Summary Table.

Internal Test and Configuration Load Interrupt Status register.

**Table 8-10. INT_TEST Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-4 | RSVD | R/W1C | 0h | RSVD |
| 3 | ECC_SEC | R/W1C | 0h | ECC single-error corrected on OTP configuration load:<br>0 = No single-error corrected (or IEN_TEST.ECC_SEC is disabled)<br>1 = Single-error corrected<br>Write-1-to-clear will clear the bit. The bit will be set again during next OTP configuration load if the same fault is detected. |
| 2 | ECC_DED | R/W1C | 0h | ECC double-error detected on OTP configuration load:<br>0 = No double-error detected on OTP load<br>1 = Double-error detected on OTP load<br>The fault bit is always enabled (there is no associated interrupt enable bit). The device will move to failsafe mode on double error detection. |
| 1 | BIST_Complete_INT | R/W1C | 0h | Indication of Built-In Self-Test complete:<br>0 = BIST not complete (or IEN_TEST.BIST_C is disabled)<br>1 = BIST complete<br>Write-1-to-clear will clear the bit. The bit will be set again on completion of next BIST execution |

**Table 8-10. INT_TEST Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 0 | BIST_Fail_INT | R/W1C | 0h | Built-In Self-Test fault:<br>0 = No BIST fault detected (or IEN_TEST.BIST is disabled)<br>1 = BIST fault detected<br>Write-1-to-clear will clear the bit. The bit will be set again during next BIST execution if the fault is detected |

### 8.1.1.9 INT_VENDOR Register (Offset = 24h) [Reset = 00h]

INT_VENDOR is shown in Table 8-11.

Return to the Summary Table.

Vendor Specific Internal Interrupt Status register.

**Table 8-11. INT_VENDOR Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RSVD | R/W1C | 0h | RSVD |
| 6 | LDO_OV_Error | R/W1C | 0h | Internal LDO Overvoltage error.<br>0 = No internal LDO overvoltage fault detected<br>1 = Internal LDO overvoltage fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the LDO fault condition is also removed. |
| 5 | NRST_MISMATCH | R/W1C | 0h | Designates error due to drive state and read back. During an NRST toggle NRST mismatch will be active after 2μs, NRST must exceed 0.6*VDD to be considered in a logic high state.<br>0 = No fault detected on NRST pin<br>1 = Error due to drive state and read back.<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the NRST fault condition is also removed. |
| 4 | Freq_DEV_Error | R/W1C | 0h | Designates internal frequency errors.<br>0 = No internal frequency fault detected<br>1 = Internal frequency fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the frequency fault condition is also removed. |
| 3 | SHORT_DET | R/W1C | 0h | Address pin short detect.<br>0 = No address pin short fault detected<br>1 = Address pin short fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the address pin short fault condition is also removed. |
| 2 | OPEN_DET | R/W1C | 0h | Address pin open detect.<br>0 = No address pin open fault detected<br>1 = Address pin open fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the address pin open fault condition is also removed. |
| 1 | ESM_ERROR | R/W1C | 0h | Indication of ESM fault.<br>0 = No ESM fault detected<br>1 = ESM fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the ESM fault condition is also removed. |

**Table 8-11. INT_VENDOR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 0 | WDT_ERROR | R/W1C | 0h | Indication of Watchdog fault.<br>0 = No Watchdog fault detected<br>1 = Watchdog fault detected<br>The recovery of the fault condition does NOT clear the bit. It can only be cleared by the host with a write-1-to-clear. Write-1-to-clear will clear the bit only if the Watchdog fault condition is also removed. |

### 8.1.1.10 VMON_STAT Register (Offset = 30h) [Reset = 7Eh]

VMON_STAT is shown in Table 8-12.

Return to the Summary Table.

Status flags for internal operations and other non critical conditions.

**Table 8-12. VMON_STAT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | FAILSAFE | R | 0h | 1 = Device in FAILSAFE state |
| 6 | ST_BIST_C | R | 1h | Built-In Self-Test state:<br>0 = BIST not complete<br>1 = BIST complete |
| 5 | ST_VDD | R | 1h | Status VDD |
| 4 | ST_NIRQ | R | 1h | Status NIRQ pin |
| 3 | RSVD | R | 1h | RSVD |
| 2 | ACTIVE | R | 1h | 1 = Device in ACTIVE state |
| 1 | RSVD | R | 1h | RSVD |
| 0 | RSVD | R | 0h | RSVD |

### 8.1.1.11 TEST_INFO Register (Offset = 31h) [Reset = 00h]

TEST_INFO is shown in Table 8-13.

Return to the Summary Table.

Internal Self-Test and ECC information.

**Table 8-13. TEST_INFO Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RSVD | R | 0h | RSVD |
| 5 | ECC_SEC | R | 0h | Status of ECC single-error correction on OTP configuration load.<br>0 = no error correction applied<br>1 = single-error correction applied |
| 4 | ECC_DED | R | 0h | Status of ECC double-error detection on OTP configuration load.<br>0 = no double-error detected<br>1 = double-error detected |
| 3 | BIST_VM | R | 0h | Status of Volatile Memory test output from BIST.<br>0 = Volatile Memory test pass<br>1 = Volatile Memory test fail |
| 2 | BIST_NVM | R | 0h | Status of Non-Volatile Memory test output from BIST.<br>0 = Non-Volatile Memory test pass<br>1 = Non-Volatile Memory test fail |
| 1 | BIST_L | R | 0h | Status of Logic test output from BIST.<br>0 = Logic test pass<br>1 = Logic test fail |

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**Table 8-13. TEST_INFO Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 0 | BIST_A | R | 0h | Status of Analog test output from BIST.<br>0 = Analog test pass<br>1 = Analog test fail |

### 8.1.1.12 OFF_STAT Register (Offset = 32h) [Reset = 00h]

OFF_STAT is shown in Table 8-14.

Return to the Summary Table.

Channel OFF status.

**Table 8-14. OFF_STAT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RSVD | R | 0h | RSVD |
| 3 | MON[4] | R | 0h | Represents the OFF status of each channel:<br>0 = channel 4 is NOT OFF<br>1 = channel 4 is OFF (below OFF threshold) |
| 2 | MON[3] | R | 0h | Represents the OFF status of each channel:<br>0 = channel 3 is NOT OFF<br>1 = channel 3 is OFF (below OFF threshold) |
| 1 | MON[2] | R | 0h | Represents the OFF status of each channel:<br>0 = channel 2 is NOT OFF<br>1 = channel 2 is OFF (below OFF threshold) |
| 0 | RSVD | R | 0h | RSVD |

### 8.1.1.13 WDT_STAT Register (Offset = 37h) [Reset = 00h]

WDT_STAT is shown in Table 8-15.

Return to the Summary Table.

Watchdog Status

**Table 8-15. WDT_STAT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RSVD | R | 0h | RSVD |
| 5-3 | WD_STATE | R | 0h | Represents Watchdog state.<br>000 = WD Idle state<br>001 = WD Open state<br>010 = WD Close state<br>011 = WD Startup state<br>100 = WD suspend state |
| 2 | ST_WDEXP | R | 0h | Will flag if close window expires before writing 3 answers or if open window expires.<br>1 = close window or open window expired (bit clears when read) |
| 1 | RSVD | R | 0h | RSVD |
| 0 | ST_WDUV | R | 0h | Will flag if an extra answer in close window (4 answers in close window) OR a wrong answer in close window OR a wrong answer in open window.<br>1 = extra or wrong answer (bit clears when read) |

### 8.1.1.14 WD_STAT_QA Register (Offset = 38h) [Reset = 3Ch]

WD_STAT_QA is shown in Table 8-16.

Return to the Summary Table.

Watchdog Answer Count and Token

### Table 8-16. WD_STAT_QA Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | RSVD | R | 0h | RSVD |
| 5-4 | ANSW_CNT[1:0] | R | 3h | Represents Answer count in real time |
| 3-0 | TOKEN[3:0] | R | Ch | Represents Token in real time. Enabling the watchdog sets the Token value to 0. |

### 8.1.1.15 MON_LVL[2] Register (Offset = 41h) [Reset = 00h]

MON_LVL[2] is shown in Table 8-17.

Return to the Summary Table.

Channel 2 voltage level.

### Table 8-17. MON_LVL[2] Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | ADC[7:0] | R | 0h | Represents MON2 voltage telemetry value in hex |

### 8.1.1.16 MON_LVL[3] Register (Offset = 42h) [Reset = 00h]

MON_LVL[3] is shown in Table 8-18.

Return to the Summary Table.

Channel 3 voltage level.

### Table 8-18. MON_LVL[3] Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | ADC[7:0] | R | 0h | Represents MON3 voltage telemetry value in hex |

### 8.1.1.17 MON_LVL[4] Register (Offset = 43h) [Reset = 00h]

MON_LVL[4] is shown in Table 8-19.

Return to the Summary Table.

Channel 4 voltage level.

### Table 8-19. MON_LVL[4] Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | ADC[7:0] | R | 0h | Represents MON4 voltage telemetry value in hex |

### 8.1.1.18 BANK_SEL Register (Offset = F0h) [Reset = 00h]

BANK_SEL is shown in Table 8-20.

Return to the Summary Table.

Bank Select.

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**Table 8-20. BANK_SEL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-1 | RSVD | R/W | 0h | RSVD |
| 0 | BANK_Select | R/W | 0h | Represents bank selection.<br>0 = Bank 0<br>1 = Bank 1 |

### 8.1.1.19 PROT1 Register (Offset = F1h) [Reset = 00h]

PROT1 is shown in Table 8-21.

Return to the Summary Table.

Locks or unlocks register changes. Must match PROT2.

**Table 8-21. PROT1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | RSVD | R/W | 0h | RSVD |
| 5 | WRKC | R/W | 0h | Represents Protection from writes for WRKC group. Both PROT1 and PROT2 need to be set for protection.<br>0 = Changes to register are possible<br>1 = Changes to register are not possible |
| 4 | RSVD | R/W | 0h | RSVD |
| 3 | CFG | R/W | 0h | Represents Protection from writes for CFG group. Both PROT1 and PROT2 need to be set for protection.<br>0 = Changes to register are possible<br>1 = Changes to register are not possible |
| 2 | IEN | R/W | 0h | Represents Protection from writes for IEN group. Both PROT1 and PROT2 need to be set for protection.<br>0 = Changes to register are possible<br>1 = Changes to register are not possible |
| 1 | MON | R/W | 0h | Represents Protection from writes for MON group. Both PROT1 and PROT2 need to be set for protection.<br>0 = Changes to register are possible<br>1 = Changes to register are not possible |
| 0 | RSVD | R/W | 0h | RSVD |

### 8.1.1.20 PROT2 Register (Offset = F2h) [Reset = 00h]

PROT2 is shown in Table 8-22.

Return to the Summary Table.

Locks or unlocks register changes. Must match PROT1.

**Table 8-22. PROT2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | RSVD | R/W | 0h | RSVD |
| 5 | WRKC | R/W | 0h | Represents Protection from writes for CFG group. Both PROT1 and PROT2 need to be set for protection.<br>0 = Changes to register are possible<br>1 = Changes to register are not possible |
| 4 | RSVD | R/W | 0h | RSVD |
| 3 | CFG | R/W | 0h | Represents Protection from writes for CFG group. Both PROT1 and PROT2 need to be set for protection.<br>0 = Changes to register are possible<br>1 = Changes to register are not possible |

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**Table 8-22. PROT2 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 2 | IEN | R/W | 0h | Represents Protection from writes for IEN group. Both PROT1 and PROT2 need to be set for protection.<br>0 = Changes to register are possible<br>1 = Changes to register are not possible |
| 1 | MON | R/W | 0h | Represents Protection from writes for MON group. Both PROT1 and PROT2 need to be set for protection.<br>0 = Changes to register are possible<br>1 = Changes to register are not possible |
| 0 | RSVD | R/W | 0h | RSVD |

### 8.1.1.21 PROT_MON Register (Offset = F3h) [Reset = 1Fh]

PROT_MON is shown in Table 8-23.

Return to the Summary Table.

Locks MON registers in tandem with PROT1 and PROT2.

**Table 8-23. PROT_MON Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RSVD | R/W | 1h | RSVD |
| 3 | MON[4] | R/W | 1h | Protects MON4 from writes along with PROT1 and PROT2.<br>0= Changes are possible<br>1= Changes are not possible |
| 2 | MON[3] | R/W | 1h | Protects MON3 from writes along with PROT1 and PROT2.<br>0= Changes are possible<br>1= Changes are not possible |
| 1 | MON[2] | R/W | 1h | Protects MON2 from writes along with PROT1 and PROT2.<br>0= Changes are possible<br>1= Changes are not possible |
| 0 | RSVD | R/W | 1h | RSVD |

### 8.1.1.22 I2CADDR Register (Offset = F9h) [Reset = 30h]

I2CADDR is shown in Table 8-24.

Return to the Summary Table.

I2C Address

**Table 8-24. I2CADDR Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RSVD | R/W | 0h | RSVD |
| 6-3 | ADDR_NVM[3:0] | R | 6h | Represents I2C address from internal OTP. Default value of 30 hex. Also the default I2C address for fail safe mode if I2C communication fails |
| 2-0 | ADDR_STRAP[2:0] | R | 0h | Represents I2C address from resistor value on ADDR pin. |

### 8.1.1.23 DEV_CFG Register (Offset = FAh) [Reset = 00h]

DEV_CFG is shown in Table 8-25.

Return to the Summary Table.

Status of I2C interface voltage levels.

**Table 8-25. DEV_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | RSVD | R | 0h | RSVD |

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### 8.1.2 BANK1 Registers

Table 8-26 lists the memory-mapped registers for the BANK1 registers. All register offset addresses not listed in Table 8-26 should be considered as reserved locations and the register contents should not be modified.

**Table 8-26. BANK1 Registers**

| Offset | Acronym | Register Name | Section |
|---|---|---|---|
| 10h | VMON_CTL | VMON device control register. | Go |
| 11h | VMON_MISC | Miscellaneous VMON configurations. | Go |
| 12h | TEST_CFG | Built-In Self Test (BIST) execution configuration. | Go |
| 13h | IEN_UVHF | High Frequency channel Under-Voltage Interrupt Enable register | Go |
| 14h | IEN_UVLF | Low Frequency channel Under-Voltage Interrupt Enable register. | Go |
| 15h | IEN_OVHF | High Frequency channel Over-Voltage Interrupt Enable register. | Go |
| 16h | IEN_OVLF | Low Frequency channel Over-Voltage Interrupt Enable register. | Go |
| 1Bh | IEN_CONTROL | Control and Communication Fault Interrupt Enable register. | Go |
| 1Ch | IEN_TEST | Internal Test and Configuration Load Fault Interrupt Enable register | Go |
| 1Dh | IEN_VENDOR | Vendor Specific Internal Interrupt Enable register. | Go |
| 1Eh | MON_CH_EN | Channel Voltage Monitoring Enable. | Go |
| 1Fh | VRANGE_MULT | Channel Voltage Monitoring Range/Scaling. | Go |
| 30h | UV_HF[2] | Channel 2 High Frequency channel Under-Voltage threshold. | Go |
| 31h | OV_HF[2] | Channel 2 High Frequency channel Over-Voltage threshold. | Go |
| 32h | UV_LF[2] | Channel 2 Low Frequency channel Under-Voltage threshold. | Go |
| 33h | OV_LF[2] | Channel 2 Low Frequency channel Over-Voltage threshold. | Go |
| 34h | FLT_HF[2] | Channel 2 UV and OV debouncing for High Frequency thresholds comparator output. | Go |
| 35h | FC_LF[2] | Channel 2 Low Frequency Path G(s) Cutoff Frequency (-3 dB point). The register changes the filter properties of the programmable LPF such that the total frequency response G(s) meets these cutoff frequencies. | Go |
| 40h | UV_HF[3] | Channel 3 High Frequency channel Under-Voltage threshold. | Go |
| 41h | OV_HF[3] | Channel 3 High Frequency channel Over-Voltage threshold. | Go |
| 42h | UV_LF[3] | Channel 3 Low Frequency channel Under-Voltage threshold. | Go |
| 43h | OV_LF[3] | Channel 3 Low Frequency channel Over-Voltage threshold. | Go |
| 44h | FLT_HF[3] | Channel 3 UV and OV debouncing for High Frequency thresholds comparator output. | Go |

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**Table 8-26. BANK1 Registers (continued)**

| Offset | Acronym | Register Name | Section |
|--------|---------|---------------|---------|
| 45h | FC_LF[3] | Channel 3 Low Frequency Path G(s) Cutoff Frequency (-3 dB point). The register changes the filter properties of the programmable LPF such that the total frequency response G(s) meets these cutoff frequencies. | Go |
| 50h | UV_HF[4] | Channel 4 High Frequency channel Under-Voltage threshold. | Go |
| 51h | OV_HF[4] | Channel 4 High Frequency channel Over-Voltage threshold. | Go |
| 52h | UV_LF[4] | Channel 4 Low Frequency channel Under-Voltage threshold. | Go |
| 53h | OV_LF[4] | Channel 4 Low Frequency channel Over-Voltage threshold. | Go |
| 54h | FLT_HF[4] | Channel 4 UV and OV debouncing for High Frequency thresholds comparator output. | Go |
| 55h | FC_LF[4] | Channel 4 Low Frequency Path G(s) Cutoff Frequency (-3 dB point). The register changes the filter properties of the programmable LPF such that the total frequency response G(s) meets these cutoff frequencies. | Go |
| 9Eh | ESM | ESM threshold time for asserting a fault. | Go |
| 9Fh | TI_CONTROL | Manual BIST/WD EN/Manual Reset via I2C/ESM deglitch/Reset delay | Go |
| A1h | AMSK_ON | Auto-mask UVLF, UVHF, and OVHF interrupts on power up transitions. | Go |
| A2h | AMSK_OFF | Auto-mask UVLF, UVHF, and OVHF interrupts on power down transitions. | Go |
| A5h | SEQ_TOUT_MSB | Timeout for UV faults during powerup and power down. | Go |
| A6h | SEQ_TOUT_LSB | Timeout for UV faults during powerup and power down. | Go |
| A8h | SEQ_UP_THLD | Threshold at which AMSK is released (VMON considered on) for power up. | Go |
| A9h | SEQ_DN_THLD | Threshold at which AMSK is released (VMON considered off) for power down. | Go |
| AAh | WDT_CFG | Max violation count for WD and Delay multiplier for Start Up Window. | Go |
| ABh | WDT_CLOSE | Close Window Time. | Go |
| ACh | WDT_OPEN | Open Window Time. | Go |
| ADh | WDT_QA_CFG | Feedback/Poly/Seed for Watchdog. | Go |
| AEh | WDT_ANSWER | Answer for the Watchdog. | Go |
| F0h | BANK_SEL | Bank Select. | Go |

Complex bit access types are encoded to fit into small table cells. Table 8-27 shows the codes that are used for access types in this section.

**Table 8-27. BANK1 Access Type Codes**

| Access Type | Code | Description |
|-------------|------|-------------|
| **Read Type** | | |
| R | R | Read |
| **Write Type** | | |

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**Table 8-27. BANK1 Access Type Codes (continued)**

| Access Type | Code | Description |
|---|---|---|
| W | W | Write |
| **Reset or Default Value** | | |
| -n | | Value after reset or the default value |

### 8.1.2.1 VMON_CTL Register (Offset = 10h) [Default = 20h]

VMON_CTL is shown in Table 8-28.

Return to the Summary Table.

VMON device control register.

**Table 8-28. VMON_CTL Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-5 | RSVD | R/W | 1h | RSVD |
| 4 | FORCE_WDO_LOW | R/W | 0h | Force assertion of WDO |
| 3 | RESET_PROT | R/W | 0h | Reset_Prot = read 0, write 1 to clear Protection registers |
| 2-1 | RSVD | R/W | 0h | RSVD |
| 0 | FORCE_NIRQ_LOW | R/W | 0h | Force assertion of NIRQ |

### 8.1.2.2 VMON_MISC Register (Offset = 11h) [Default = X]

VMON_MISC is shown in Table 8-29.

Return to the Summary Table.

Miscellaneous VMON configurations.

**Table 8-29. VMON_MISC Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7 | RSVD | R/W | X | RSVD |
| 6-4 | WDO_DLY[2:0] | R/W | X | WDO_Delay (not applicable for latched WDO) |
| 3-2 | RSVD | R/W | X | RSVD |
| 1 | REQ_PEC | R/W | X | Require PEC.<br>0 = PEC not required<br>1 = PEC required |
| 0 | EN_PEC | R/W | X | Enable PEC.<br>0 = PEC not enabled<br>1 = PEC enabled |

### 8.1.2.3 TEST_CFG Register (Offset = 12h) [Default = X]

TEST_CFG is shown in Table 8-30.

Return to the Summary Table.

Built-In Self Test (BIST) execution configuration.

**Table 8-30. TEST_CFG Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-3 | RSVD | R/W | X | RSVD |
| 2 | AT_SHDN | R/W | X | Run BIST at SHDN |

**Table 8-30. TEST_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 1 | AT_POR[1] | R/W | X | Run BIST at POR, 2nd bit for redundancy |
| 0 | AT_POR[0] | R/W | X | Run BIST at POR |

### 8.1.2.4 IEN_UVHF Register (Offset = 13h) [Default = X]

IEN_UVHF is shown in Table 8-31.

Return to the Summary Table.

High Frequency channel Under-Voltage Interrupt Enable register

**Table 8-31. IEN_UVHF Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-4 | RSVD | R/W | X | RSVD |
| 3 | MON[4] | R/W | X | enabling uvhf for channel 4, Disable=0, Enable=1 |
| 2 | MON[3] | R/W | X | enabling uvhf for channel 3, Disable=0, Enable=1 |
| 1 | MON[2] | R/W | X | enabling uvhf for channel 2, Disable=0, Enable=1 |
| 0 | RSVD | R/W | X | RSVD |

### 8.1.2.5 IEN_UVLF Register (Offset = 14h) [Default = X]

IEN_UVLF is shown in Table 8-32.

Return to the Summary Table.

Low Frequency channel Under-Voltage Interrupt Enable register.

**Table 8-32. IEN_UVLF Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-4 | RSVD | R/W | X | RSVD |
| 3 | MON[4] | R/W | X | enabling uvlf for channel 4, Disable=0, Enable=1 |
| 2 | MON[3] | R/W | X | enabling uvlf for channel 3, Disable=0, Enable=1 |
| 1 | MON[2] | R/W | X | enabling uvlf for channel 2, Disable=0, Enable=1 |
| 0 | RSVD | R/W | X | RSVD |

### 8.1.2.6 IEN_OVHF Register (Offset = 15h) [Default = X]

IEN_OVHF is shown in Table 8-33.

Return to the Summary Table.

High Frequency channel Over-Voltage Interrupt Enable register.

**Table 8-33. IEN_OVHF Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-4 | RSVD | R/W | X | RSVD |
| 3 | MON[4] | R/W | X | enabling ovhf for channel 4, Disable=0, Enable=1 |
| 2 | MON[3] | R/W | X | enabling ovhf for channel 3, Disable=0, Enable=1 |
| 1 | MON[2] | R/W | X | enabling ovhf for channel 2, Disable=0, Enable=1 |
| 0 | RSVD | R/W | X | RSVD |

### 8.1.2.7 IEN_OVLF Register (Offset = 16h) [Default = X]

IEN_OVLF is shown in Table 8-34.

Return to the Summary Table.

Low Frequency channel Over-Voltage Interrupt Enable register.

**Table 8-34. IEN_OVLF Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-4 | RSVD | R/W | X | RSVD |
| 3 | MON[4] | R/W | X | enabling ovlf for channel 4, Disable=0, Enable=1 |
| 2 | MON[3] | R/W | X | enabling ovlf for channel 3, Disable=0, Enable=1 |
| 1 | MON[2] | R/W | X | enabling ovlf for channel 2, Disable=0, Enable=1 |
| 0 | RSVD | R/W | X | RSVD |

### 8.1.2.8 IEN_CONTROL Register (Offset = 1Bh) [Default = X]

IEN_CONTROL is shown in Table 8-35.

Return to the Summary Table.

Control and Communication Fault Interrupt Enable register.

**Table 8-35. IEN_CONTROL Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-5 | RSVD | R/W | X | RSVD |
| 4 | RT_CRC_Int | R/W | X | Register Run time CRC error Interrupt. Disable=0, Enable = 1 |
| 3 | RSVD | R/W | X | RSVD |
| 2 | TSD_INT | R/W | X | Thermal shutdown Interrupt. Disable=0, Enable = 1 |
| 1 | RSVD | R/W | X | RSVD |

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**Table 8-35. IEN_CONTROL Register Field Descriptions (continued)**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 0 | PEC_INT | R/W | X | PEC Error Interrupt.<br>Disable=0,<br>Enable = 1 |

### 8.1.2.9 IEN_TEST Register (Offset = 1Ch) [Default = X]

IEN_TEST is shown in Table 8-36.

Return to the Summary Table.

Internal Test and Configuration Load Fault Interrupt Enable register

**Table 8-36. IEN_TEST Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-4 | RSVD | R/W | X | RSVD |
| 3 | ECC_SEC | R/W | X | SEC Error Interrupt.<br>Disable=0,<br>Enable = 1 |
| 2 | RSVD | R/W | X | RSVD |
| 1 | BIST_Complete_INT | R/W | X | BIST complete Interrupt.<br>Disable=0,<br>Enable = 1 |
| 0 | BIST_Fail_INT | R/W | X | BIST Fail Interrupt.<br>Disable=0,<br>Enable = 1 |

### 8.1.2.10 IEN_VENDOR Register (Offset = 1Dh) [Default = X]

IEN_VENDOR is shown in Table 8-37.

Return to the Summary Table.

Vendor Specific Internal Interrupt Enable register.

**Table 8-37. IEN_VENDOR Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-6 | RSVD | R/W | X | RSVD |
| 5 | NRST_MISMATCH | R/W | X | NRST mismatch Interrupt.<br>Disable=0,<br>Enable = 1 |
| 4 | ESM_TO_WDO | R/W | X | Maps ESM fault to WDO.<br>Not mapped=0<br>Mapped = 1 |
| 3 | ESM_TO_NIRQ | R/W | X | Maps ESM fault to NIRQ.<br>Not mapped=0<br>Mapped = 1 |
| 2 | WDT_TO_NIRQ | R/W | X | Maps Watchdog fault to NIRQ.<br>Not mapped=0<br>Mapped = 1 |
| 1 | ESM_TO_NRST | R/W | X | Maps ESM fault to NRST.<br>Not mapped=0<br>Mapped = 1 |
| 0 | WDT_TO_NRST | R/W | X | Maps Watchdog fault to NRST.<br>Not mapped=0<br>Mapped = 1 |

### 8.1.2.11 MON_CH_EN Register (Offset = 1Eh) [Default = X]

MON_CH_EN is shown in Table 8-38.

Return to the Summary Table.

Channel Voltage Monitoring Enable.

**Table 8-38. MON_CH_EN Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-4 | RSVD | R/W | X | RSVD |
| 3 | MON[4] | R/W | X | Enables channel 4 monitoring. Enabled = 1, Disabled = 0 |
| 2 | MON[3] | R/W | X | Enables channel 3 monitoring. Enabled = 1, Disabled = 0 |
| 1 | MON[2] | R/W | X | Enables channel 2 monitoring. Enabled = 1, Disabled = 0 |
| 0 | RSVD | R/W | X | RSVD |

### 8.1.2.12 VRANGE_MULT Register (Offset = 1Fh) [Default = X]

VRANGE_MULT is shown in Table 8-39.

Return to the Summary Table.

Channel Voltage Monitoring Range/Scaling.

**Table 8-39. VRANGE_MULT Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-4 | RSVD | R/W | X | RSVD |
| 3 | MON[4] | R/W | X | Scalar for MON_4. 1x =0, 4x = 1 |
| 2 | MON[3] | R/W | X | Scalar for MON_3. 1x =0, 4x = 1 |
| 1 | MON[2] | R/W | X | Scalar for MON_2. 1x =0, 4x = 1 |
| 0 | RSVD | R/W | X | RSVD |

### 8.1.2.13 UV_HF[2] Register (Offset = 30h) [Default = X]

UV_HF[2] is shown in Table 8-40.

Return to the Summary Table.

Channel 2 High Frequency channel Under-Voltage threshold.

**Table 8-40. UV_HF[2] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-0 | THRESHOLD[7:0] | R/W | X | Undervoltage threshold for High Frequency component of monitored channel.<br>The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.<br>With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV.<br>With scaling = 4x, the 8-bit value represents the range 0.8 Vto 5.9 V with 1 LSB = 20 mV. |

### 8.1.2.14 OV_HF[2] Register (Offset = 31h) [Default = X]

OV_HF[2] is shown in Table 8-41.

Return to the Summary Table.

Channel 2 High Frequency channel Over-Voltage threshold.

**Table 8-41. OV_HF[2] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-0 | THRESHOLD[7:0] | R/W | X | Overvoltage threshold for High Frequency component of monitored channel.<br>The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.<br>With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV.<br>With scaling = 4x, the 8-bit value represents the range 0.8 Vto 5.9 V with 1 LSB = 20 mV. |

### 8.1.2.15 UV_LF[2] Register (Offset = 32h) [Default = X]

UV_LF[2] is shown in Table 8-42.

Return to the Summary Table.

Channel 2 Low Frequency channel Under-Voltage threshold.

**Table 8-42. UV_LF[2] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-0 | THRESHOLD[7:0] | R/W | X | Undervoltage threshold for Low Frequency component of monitored channel.<br>The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.<br>With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV.<br>With scaling = 4x, the 8-bit value represents the range 0.8 Vto 5.9 V with 1 LSB = 20 mV. |

### 8.1.2.16 OV_LF[2] Register (Offset = 33h) [Default = X]

OV_LF[2] is shown in Table 8-43.

Return to the Summary Table.

Channel 2 Low Frequency channel Over-Voltage threshold.

**Table 8-43. OV_LF[2] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-0 | THRESHOLD[7:0] | R/W | X | Overvoltage threshold for Low Frequency component of monitored channel.<br>The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.<br>With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV.<br>With scaling = 4x, the 8-bit value represents the range 0.8 Vto 5.9 V with 1 LSB = 20 mV. |

### 8.1.2.17 FLT_HF[2] Register (Offset = 34h) [Default = X]

FLT_HF[2] is shown in Table 8-44.

Return to the Summary Table.

Channel 2 UV and OV debouncing for High Frequency thresholds comparator output.

**Table 8-44. FLT_HF[2] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-4 | OV_DEB[3:0] | R/W | X | Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.<br>0000b = 0.1 µs 1000b = 25.6 µs<br>0001b = 0.2 µs 1001b = 51.2 µs<br>0010b = 0.4 µs 1010b = 102.4 µs<br>0011b = 0.8 µs 1011b = 102.4 µs<br>0100b = 1.6 µs 1100b = 102.4 µs<br>0101b = 3.2 µs 1101b = 102.4 µs<br>0110b = 6.4 µs 1110b = 102.4 µs<br>0111b = 12.8 µs 1111b = 102.4 µs |
| 3-0 | UV_DEB[3:0] | R/W | X | Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.<br>0000b = 0.1 µs 1000b = 25.6 µs<br>0001b = 0.2 µs 1001b = 51.2 µs<br>0010b = 0.4 µs 1010b = 102.4 µs<br>0011b = 0.8 µs 1011b = 102.4 µs<br>0100b = 1.6 µs 1100b = 102.4 µs<br>0101b = 3.2 µs 1101b = 102.4 µs<br>0110b = 6.4 µs 1110b = 102.4 µs<br>0111b = 12.8 µs 1111b = 102.4 µs |

### 8.1.2.18 FC_LF[2] Register (Offset = 35h) [Default = X]

FC_LF[2] is shown in Table 8-45.

Return to the Summary Table.

Channel 2 Low Frequency Path G(s) Cutoff Frequency (-3 dB point). The register changes the filter properties of the programmable LPF such that the total frequency response G(s) meets these cutoff frequencies.

**Table 8-45. FC_LF[2] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-5 | RSVD | R/W | X | RSVD |
| 4 | ovhf_to_nrst | R/W | X | Maps Channel 2 ovhf fault to NRST<br>Not mapped = 0,<br>Mapped = 1 |

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**Table 8-45. FC_LF[2] Register Field Descriptions (continued)**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 3 | uvhf_to_nrst | R/W | X | Maps Channel 2 uvhf fault to NRST<br>Not mapped = 0,<br>Mapped = 1 |
| 2-0 | Cut_off_Freq[2:0] | R/W | X | Channel 2 Cut of frequency for LF faults filter<br>000 =Invalid<br>001 =Invalid<br>010 =250Hz<br>011 = 500Hz<br>100 = 1kHz<br>101 = 2kHz<br>110 =4kHz<br>111 = Invalid |

### 8.1.2.19 UV_HF[3] Register (Offset = 40h) [Default = X]

UV_HF[3] is shown in Table 8-46.

Return to the Summary Table.

Channel 3 High Frequency channel Under-Voltage threshold.

**Table 8-46. UV_HF[3] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-0 | THRESHOLD[7:0] | R/W | X | Undervoltage threshold for High Frequency component of monitored channel.<br>The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.<br>With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV.<br>With scaling = 4x, the 8-bit value represents the range 0.8 Vto 5.9 V with 1 LSB = 20 mV. |

### 8.1.2.20 OV_HF[3] Register (Offset = 41h) [Default = X]

OV_HF[3] is shown in Table 8-47.

Return to the Summary Table.

Channel 3 High Frequency channel Over-Voltage threshold.

**Table 8-47. OV_HF[3] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-0 | THRESHOLD[7:0] | R/W | X | Overvoltage threshold for High Frequency component of monitored channel.<br>The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.<br>With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV.<br>With scaling = 4x, the 8-bit value represents the range 0.8 Vto 5.9 V with 1 LSB = 20 mV. |

### 8.1.2.21 UV_LF[3] Register (Offset = 42h) [Default = X]

UV_LF[3] is shown in Table 8-48.

Return to the Summary Table.

Channel 3 Low Frequency channel Under-Voltage threshold.

**Table 8-48. UV_LF[3] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-0 | THRESHOLD[7:0] | R/W | X | Undervoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 Vto 5.9 V with 1 LSB = 20 mV. |

### 8.1.2.22 OV_LF[3] Register (Offset = 43h) [Default = X]

OV_LF[3] is shown in Table 8-49.

Return to the Summary Table.

Channel 3 Low Frequency channel Over-Voltage threshold.

**Table 8-49. OV_LF[3] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-0 | THRESHOLD[7:0] | R/W | X | Overvoltage threshold for Low Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV. With scaling = 4x, the 8-bit value represents the range 0.8 Vto 5.9 V with 1 LSB = 20 mV. |

### 8.1.2.23 FLT_HF[3] Register (Offset = 44h) [Default = X]

FLT_HF[3] is shown in Table 8-50.

Return to the Summary Table.

Channel 3 UV and OV debouncing for High Frequency thresholds comparator output.

**Table 8-50. FLT_HF[3] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-4 | OV_DEB[3:0] | R/W | X | Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.<br>0000b = 0.1 µs 1000b = 25.6 µs<br>0001b = 0.2 µs 1001b = 51.2 µs<br>0010b = 0.4 µs 1010b = 102.4 µs<br>0011b = 0.8 µs 1011b = 102.4 µs<br>0100b = 1.6 µs 1100b = 102.4 µs<br>0101b = 3.2 µs 1101b = 102.4 µs<br>0110b = 6.4 µs 1110b = 102.4 µs<br>0111b = 12.8 µs 1111b = 102.4 µs |
| 3-0 | UV_DEB[3:0] | R/W | X | Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.<br>0000b = 0.1 µs 1000b = 25.6 µs<br>0001b = 0.2 µs 1001b = 51.2 µs<br>0010b = 0.4 µs 1010b = 102.4 µs<br>0011b = 0.8 µs 1011b = 102.4 µs<br>0100b = 1.6 µs 1100b = 102.4 µs<br>0101b = 3.2 µs 1101b = 102.4 µs<br>0110b = 6.4 µs 1110b = 102.4 µs<br>0111b = 12.8 µs 1111b = 102.4 µs |

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### 8.1.2.24 FC_LF[3] Register (Offset = 45h) [Default = X]

FC_LF[3] is shown in Table 8-51.

Return to the Summary Table.

Channel 3 Low Frequency Path G(s) Cutoff Frequency (-3 dB point). The register changes the filter properties of the programmable LPF such that the total frequency response G(s) meets these cutoff frequencies.

**Table 8-51. FC_LF[3] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-5 | RSVD | R/W | X | RSVD |
| 4 | ovhf_to_nrst | R/W | X | Maps Channel 3 ovhf fault to NRST<br>Not mapped = 0,<br>Mapped = 1 |
| 3 | uvhf_to_nrst | R/W | X | Maps Channel 3 uvhf fault to NRST<br>Not mapped = 0,<br>Mapped = 1 |
| 2-0 | Cut_off_Freq[2:0] | R/W | X | Channel 3 Cut of frequency for LF faults filter<br>000 =Invalid<br>001 =Invalid<br>010 =250Hz<br>011 = 500Hz<br>100 = 1kHz<br>101 = 2kHz<br>110 =4kHz<br>111 = Invalid |

### 8.1.2.25 UV_HF[4] Register (Offset = 50h) [Default = X]

UV_HF[4] is shown in Table 8-52.

Return to the Summary Table.

Channel 4 High Frequency channel Under-Voltage threshold.

**Table 8-52. UV_HF[4] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-0 | THRESHOLD[7:0] | R/W | X | Undervoltage threshold for High Frequency component of monitored channel.<br>The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.<br>With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV.<br>With scaling = 4x, the 8-bit value represents the range 0.8 Vto 5.9 V with 1 LSB = 20 mV. |

### 8.1.2.26 OV_HF[4] Register (Offset = 51h) [Default = X]

OV_HF[4] is shown in Table 8-53.

Return to the Summary Table.

Channel 4 High Frequency channel Over-Voltage threshold.

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**Table 8-53. OV_HF[4] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-0 | THRESHOLD[7:0] | R/W | X | Overvoltage threshold for High Frequency component of monitored channel.<br>The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.<br>With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV.<br>With scaling = 4x, the 8-bit value represents the range 0.8 Vto 5.9 V with 1 LSB = 20 mV. |

### 8.1.2.27 UV_LF[4] Register (Offset = 52h) [Default = X]

UV_LF[4] is shown in Table 8-54.

Return to the Summary Table.

Channel 4 Low Frequency channel Under-Voltage threshold.

**Table 8-54. UV_LF[4] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-0 | THRESHOLD[7:0] | R/W | X | Undervoltage threshold for Low Frequency component of monitored channel.<br>The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.<br>With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV.<br>With scaling = 4x, the 8-bit value represents the range 0.8 Vto 5.9 V with 1 LSB = 20 mV. |

### 8.1.2.28 OV_LF[4] Register (Offset = 53h) [Default = X]

OV_LF[4] is shown in Table 8-55.

Return to the Summary Table.

Channel 4 Low Frequency channel Over-Voltage threshold.

**Table 8-55. OV_LF[4] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-0 | THRESHOLD[7:0] | R/W | X | Overvoltage threshold for Low Frequency component of monitored channel.<br>The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.<br>With scaling = 1x, the 8-bit value represents the range 0.2 V to 1.475 V with 1 LSB = 5 mV.<br>With scaling = 4x, the 8-bit value represents the range 0.8 Vto 5.9 V with 1 LSB = 20 mV. |

### 8.1.2.29 FLT_HF[4] Register (Offset = 54h) [Default = X]

FLT_HF[4] is shown in Table 8-56.

Return to the Summary Table.

Channel 4 UV and OV debouncing for High Frequency thresholds comparator output.

**Table 8-56. FLT_HF[4] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-4 | OV_DEB[3:0] | R/W | X | Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.<br>0000b = 0.1 µs 1000b = 25.6 µs<br>0001b = 0.2 µs 1001b = 51.2 µs<br>0010b = 0.4 µs 1010b = 102.4 µs<br>0011b = 0.8 µs 1011b = 102.4 µs<br>0100b = 1.6 µs 1100b = 102.4 µs<br>0101b = 3.2 µs 1101b = 102.4 µs<br>0110b = 6.4 µs 1110b = 102.4 µs<br>0111b = 12.8 µs 1111b = 102.4 µs |
| 3-0 | UV_DEB[3:0] | R/W | X | Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.<br>0000b = 0.1 µs 1000b = 25.6 µs<br>0001b = 0.2 µs 1001b = 51.2 µs<br>0010b = 0.4 µs 1010b = 102.4 µs<br>0011b = 0.8 µs 1011b = 102.4 µs<br>0100b = 1.6 µs 1100b = 102.4 µs<br>0101b = 3.2 µs 1101b = 102.4 µs<br>0110b = 6.4 µs 1110b = 102.4 µs<br>0111b = 12.8 µs 1111b = 102.4 µs |

### 8.1.2.30 FC_LF[4] Register (Offset = 55h) [Default = X]

FC_LF[4] is shown in Table 8-57.

Return to the Summary Table.

Channel 4 Low Frequency Path G(s) Cutoff Frequency (-3 dB point). The register changes the filter properties of the programmable LPF such that the total frequency response G(s) meets these cutoff frequencies.

**Table 8-57. FC_LF[4] Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-5 | RSVD | R/W | X | RSVD |
| 4 | ovhf_to_nrst | R/W | X | Maps Channel 4 ovhf fault to NRST<br>Not mapped = 0,<br>Mapped = 1 |
| 3 | uvhf_to_nrst | R/W | X | Maps Channel 4 uvhf fault to NRST<br>Not mapped = 0,<br>Mapped = 1 |
| 2-0 | Cut_off_Freq[2:0] | R/W | X | Channel 4 Cut of frequency for LF faults filter<br>000 =Invalid<br>001 =Invalid<br>010 =250Hz<br>011 = 500Hz<br>100 = 1kHz<br>101 = 2kHz<br>110 =4kHz<br>111 = Invalid |

### 8.1.2.31 ESM Register (Offset = 9Eh) [Default = X]

ESM is shown in Table 8-58.

Return to the Summary Table.

ESM threshold time for asserting a fault.

**Table 8-58. ESM Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-0 | THRESHOLD[7:0] | R/W | X | Threshold value representing the ESM delay time (1ms to 864ms) |

### 8.1.2.32 TI_CONTROL Register (Offset = 9Fh) [Default = X]

TI_CONTROL is shown in Table 8-59.

Return to the Summary Table.

Manual BIST/WD EN/Manual Reset via I2C/ESM deglitch/Reset delay

**Table 8-59. TI_CONTROL Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7 | ENTER_BIST | R/W | X | Manual BIST.<br>1 = Enter BIST |
| 6 | WDT_EN | R/W | X | Watchdog EN to be used along with hardware WD_EN pin.<br>1 = Watchdog Enabled,<br>0 = Watchdog Disabled |
| 5 | I2C_MR | R/W | X | Manual Reset.<br>1 = Assert NRST low |
| 4-3 | ESM_DEB[1:0] | R/W | X | ESM debounce filter<br>00 = 10µs<br>01 = 25µs<br>10 =50µs<br>11 =100µs |
| 2-0 | RST_DLY[2:0] | R/W | X | Reset delay<br>000 =200µs<br>001 =1ms<br>010 =10ms<br>011 = 16ms<br>100 = 20ms<br>101 = 70ms<br>110 =100ms<br>111 = 200ms |

### 8.1.2.33 AMSK_ON Register (Offset = A1h) [Default = X]

AMSK_ON is shown in Table 8-60.

Return to the Summary Table.

Auto-mask UVLF, UVHF, and OVHF interrupts on power up transitions.

**Table 8-60. AMSK_ON Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-4 | RSVD | R/W | X | RSVD |
| 3 | MON[4] | R/W | X | Automask at power on for MON 4.<br>0 = Disabled<br>1 = Enabled |
| 2 | MON[3] | R/W | X | Automask at power on for MON 3.<br>0 = Disabled<br>1 = Enabled |
| 1 | MON[2] | R/W | X | Automask at power on for MON 2.<br>0 = Disabled<br>1 = Enabled |
| 0 | RSVD | R/W | X | RSVD |

Product Folder Links: TPS389C03-Q1

### 8.1.2.34 AMSK_OFF Register (Offset = A2h) [Default = X]

AMSK_OFF is shown in Table 8-61.

Return to the Summary Table.

Auto-mask UVLF, UVHF, and OVHF interrupts on power down transitions.

**Table 8-61. AMSK_OFF Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-4 | RSVD | R/W | X | RSVD |
| 3 | MON[4] | R/W | X | Automask at power off for MON 4.<br>0 = Disabled<br>1 = Enabled |
| 2 | MON[3] | R/W | X | Automask at power off for MON 3.<br>0 = Disabled<br>1 = Enabled |
| 1 | MON[2] | R/W | X | Automask at power off for MON 2.<br>0 = Disabled<br>1 = Enabled |
| 0 | RSVD | R/W | X | RSVD |

### 8.1.2.35 SEQ_TOUT_MSB Register (Offset = A5h) [Default = X]

SEQ_TOUT_MSB is shown in Table 8-62.

Return to the Summary Table.

Timeout for UV faults during powerup and power down.

**Table 8-62. SEQ_TOUT_MSB Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-0 | MILLISEC[15:8] | R/W | X | Sequence time out MSB |

### 8.1.2.36 SEQ_TOUT_LSB Register (Offset = A6h) [Default = X]

SEQ_TOUT_LSB is shown in Table 8-63.

Return to the Summary Table.

Timeout for UV faults during powerup and power down.

**Table 8-63. SEQ_TOUT_LSB Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-0 | MILLISEC[7:0] | R/W | X | Sequence time out LSB |

### 8.1.2.37 SEQ_UP_THLD Register (Offset = A8h) [Default = X]

SEQ_UP_THLD is shown in Table 8-64.

Return to the Summary Table.

Threshold at which AMSK is released (VMON considered on) for power up.

**Table 8-64. SEQ_UP_THLD Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-4 | RSVD | R/W | X | RSVD |

**Table 8-64. SEQ_UP_THLD Register Field Descriptions (continued)**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 3 | MON[4] | R/W | X | AMSK releases at UVLF or OFF threshold for MON_4.<br>0 = off threshold,<br>1 = UVLF threshold |
| 2 | MON[3] | R/W | X | AMSK releases at UVLF or OFF threshold for MON_3.<br>0 = off threshold,<br>1 = UVLF threshold |
| 1 | MON[2] | R/W | X | AMSK releases at UVLF or OFF threshold for MON_2.<br>0 = off threshold,<br>1 = UVLF threshold |
| 0 | RSVD | R/W | X | RSVD |

### 8.1.2.38 SEQ_DN_THLD Register (Offset = A9h) [Default = X]

SEQ_DN_THLD is shown in Table 8-65.

Return to the Summary Table.

Threshold at which AMSK is released (VMON considered off) for power down.

**Table 8-65. SEQ_DN_THLD Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-4 | RSVD | R/W | X | RSVD |
| 3 | MON[4] | R/W | X | AMSK releases at UVLF or OFF threshold for MON_4.<br>0 = off threshold,<br>1 = UVLF threshold |
| 2 | MON[3] | R/W | X | AMSK releases at UVLF or OFF threshold for MON_3.<br>0 = off threshold,<br>1 = UVLF threshold |
| 1 | MON[2] | R/W | X | AMSK releases at UVLF or OFF threshold for MON_2.<br>0 = off threshold,<br>1 = UVLF threshold |
| 0 | RSVD | R/W | X | RSVD |

### 8.1.2.39 WDT_CFG Register (Offset = AAh) [Default = X]

WDT_CFG is shown in Table 8-66.

Return to the Summary Table.

Max violation count for WD and Delay multiplier for Start Up Window.

**Table 8-66. WDT_CFG Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7 | RSVD | R/W | X | RSVD |
| 6-4 | MAX_VIOLATION_COUNT | R/W | X | Max violation count for Watchdog<br>000 =0<br>001 =1<br>010 =2<br>011 = 3<br>100 = 4<br>101 = 5<br>110 = 6<br>111 = 7 |
| 3 | RSVD | R/W | X | RSVD |

**Table 8-66. WDT_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 2-0 | WDT_Startup_DLY_MULTIPLIER[2:0] | R/W | X | Watchdog Startup delay multiplier<br>000 =0<br>001 =1<br>010 =2<br>011 = 3<br>100 = 4<br>101 = 5<br>110 = 6<br>111 = 7 |

### 8.1.2.40 WDT_CLOSE Register (Offset = ABh) [Default = X]

WDT_CLOSE is shown in Table 8-67.

Return to the Summary Table.

Close Window Time.

**Table 8-67. WDT_CLOSE Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-0 | CLOSE[7:0] | R/W | X | Close window time (1ms to 864ms) |

### 8.1.2.41 WDT_OPEN Register (Offset = ACh) [Default = X]

WDT_OPEN is shown in Table 8-68.

Return to the Summary Table.

Open Window Time.

**Table 8-68. WDT_OPEN Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-0 | OPEN[7:0] | R/W | X | Open window time (1ms to 864ms) |

### 8.1.2.42 WDT_QA_CFG Register (Offset = ADh) [Default = 00h]

WDT_QA_CFG is shown in Table 8-69.

Return to the Summary Table.

FeedbackPolt/Seed for Watchdog.

**Table 8-69. WDT_QA_CFG Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-6 | FDBK[1:0] | R/W | 0h | Feedback used for computing answer |
| 5-4 | POLY[1:0] | R/W | 0h | Poly used for computing answer |
| 3-0 | SEED[3:0] | R/W | 0h | Seed used for computing answer |

### 8.1.2.43 WDT_ANSWER Register (Offset = AEh) [Default = 00h]

WDT_ANSWER is shown in Table 8-70.

Return to the Summary Table.

Answer for the Watchdog.

Submit Document Feedback     75
Product Folder Links: *TPS389C03-Q1*

**Table 8-70. WDT_ANSWER Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-0 | ANSWER[7:0] | R/W | 0h | Answer |

### 8.1.2.44 BANK_SEL Register (Offset = F0h) [Default = 00h]

BANK_SEL is shown in Table 8-71.

Return to the Summary Table.

Bank Select.

**Table 8-71. BANK_SEL Register Field Descriptions**

| Bit | Field | Type | Default | Description |
|-----|-------|------|---------|-------------|
| 7-1 | RSVD | R/W | 0h | RSVD |
| 0 | BANK_Select | R/W | 0h | Represents bank selection.<br>0 = Bank 0<br>1 = Bank 1 |

Product Folder Links: *TPS389C03-Q1*

# 9 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

Modern SOC and FPGA devices typically have multiple power rails to provide power to the different blocks within the IC. Accurate voltage level and timing requirements are common and must be met to provide proper operation of these devices. By utilizing TPS389C03-Q1 along with a multichannel voltage sequencer, the power up and power down sequencing requirements as well as the core voltage requirements of the target SOC or FPGA device can be met. This design focuses on meeting the timing requirements for an SOC by using the TPS389C03-Q1.

## 9.2 Typical Application

### 9.2.1 Automotive Multichannel Sequencer and Monitor

A typical application for the TPS389C03-Q1 is shown in Figure 9-1. TPS389C03-Q1 is used to provide the proper voltage monitoring for the target SOC device. A mulitchannel voltage monitor TPS389C03-Q1 is used to monitor the voltage rails as these rails power up and power down to ensure that the correct sequence occurs in both occasions. A safety microcontroller is also used to provide ACT, NIRQ, and I²C commands to the TPS389C03-Q1 and sequencer. The ACT signal from the safety microcontroller determines when the TPS389C03-Q1enters into ACTIVE or SHDN states while the NIRQ pin of the TPS389C03-Q1 acts as an interrupt pin that is set when a fault has occurred. The host microcontroller can clear the fault by writing 1 to the affected register. The power rails for the safety microcontroller are not shown in Figure 9-1 for simplicity.
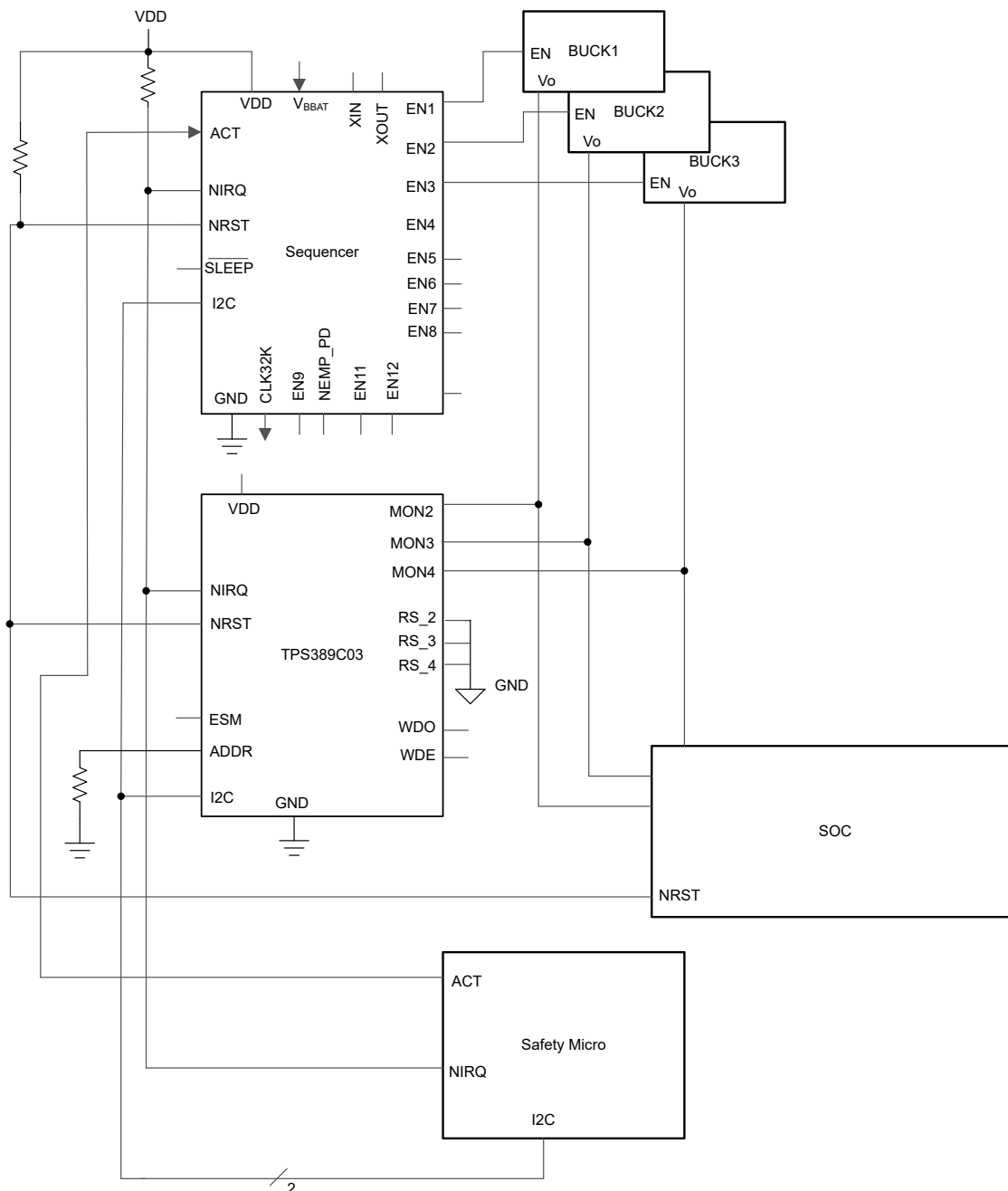


**Figure 9-1. TPS389C03-Q1 Voltage Monitor Design Block Diagram**

Product Folder Links: *TPS389C03-Q1*

### 9.2.2 Design Requirements

- Three different voltage rails supplied by DC/DC converters need to be properly monitored in this design.
- All detected failures in sequencing should be reported via an external hardware interrupt signal.
- All detected failures should be logged in internal registers and be accessible to an external processor via I²C.

### 9.2.3 Detailed Design Procedure

- TPS389C03-Q1 device option comes preprogrammed with default values for over voltage, under voltage.
- NIRQ pin requires a pull up resistor in the range of 1 kΩ to 100 kΩ.
- NRST pin requires a pull up resistor in the range of 1 kΩ to 100 kΩ.
- WDO pin requires a pull up resistor in the range of 1 kΩ to 100 kΩ.
- SDA and SCL lines require pull up resistors in the range of 10 kΩ.
- The safety microcontroller is used to clear fault interrupts reported through the NIRQ interrupt pin and the INT_SCR1 and INT_SCR2 registers. The interrupt flags can only be cleared by the host micrcontroller with a write-1-to-clear operation; interrupt flags are not automatically cleared if the fault condition is no longer present.

### 9.2.4 Application Curves
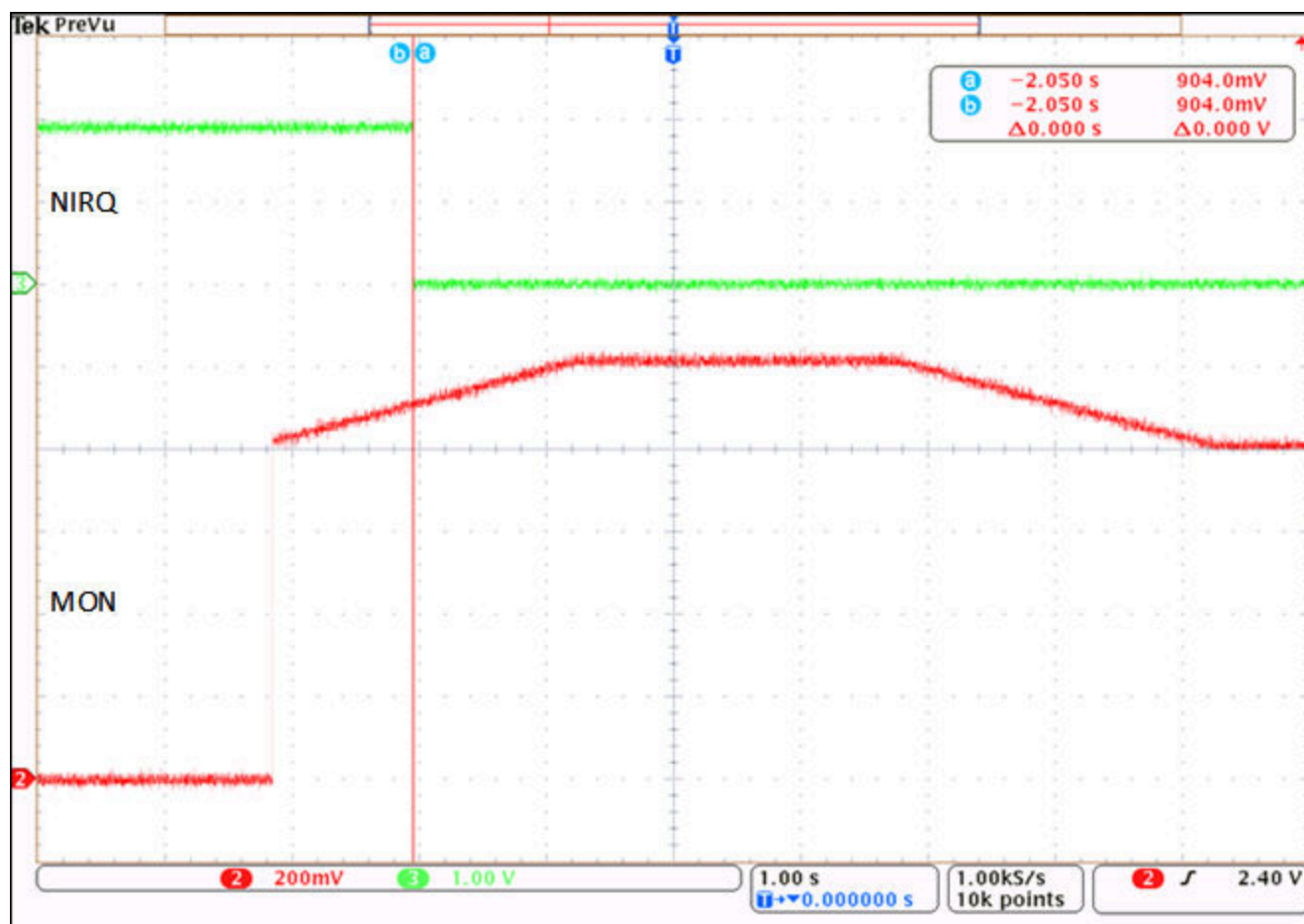


**Figure 9-2. NIRQ Triggered After an Overvoltage Fault**
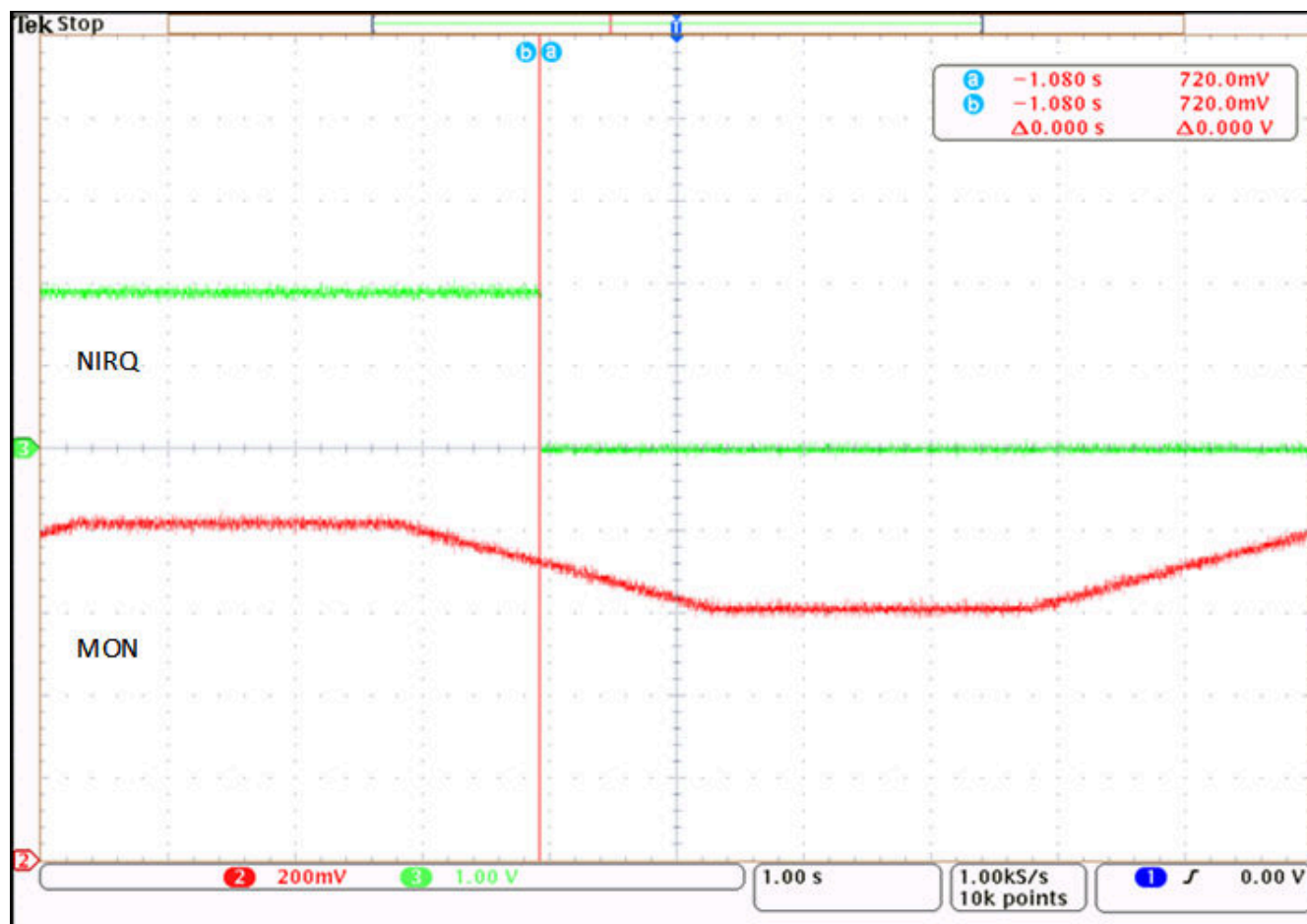
**Figure 9-3. NIRQ Triggered After an Undervoltage Fault**
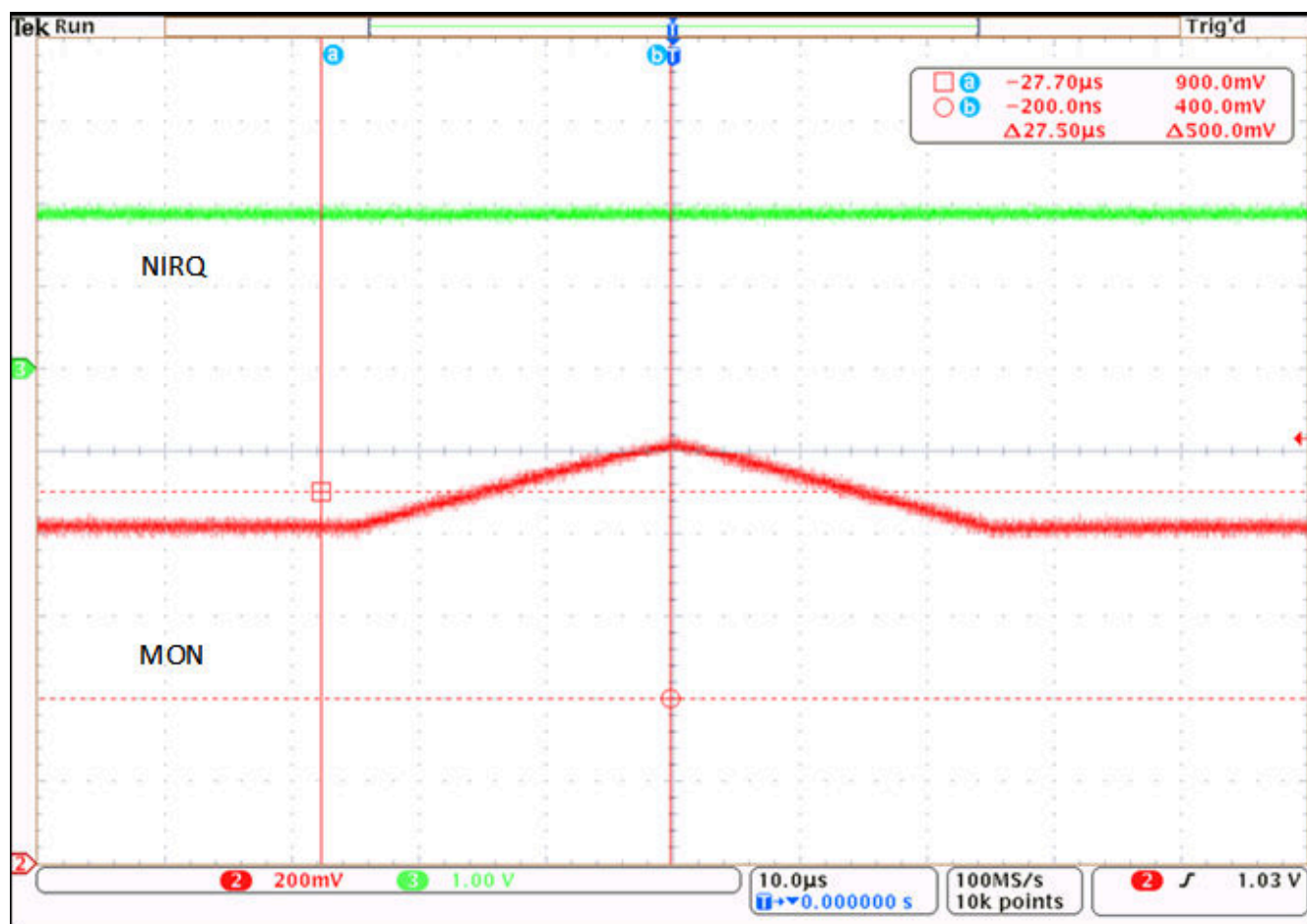
**Figure 9-4. NIRQ Not Triggered on Overvoltage Fault with 51.2 us OV Debounce Filter**
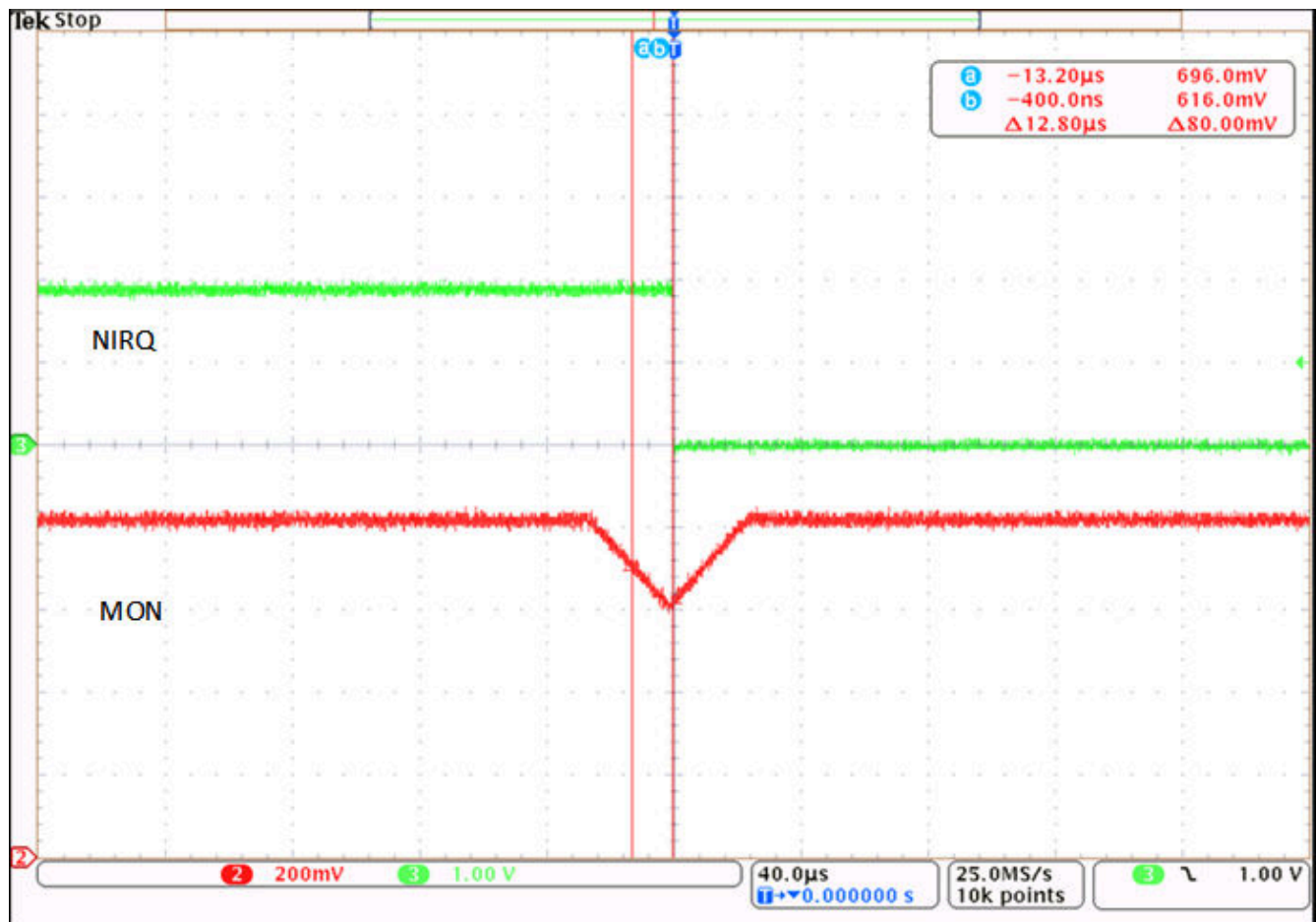
**Figure 9-5. NIRQ Triggered on Undervoltage Fault with 12.8 us UV Debounce Filter**
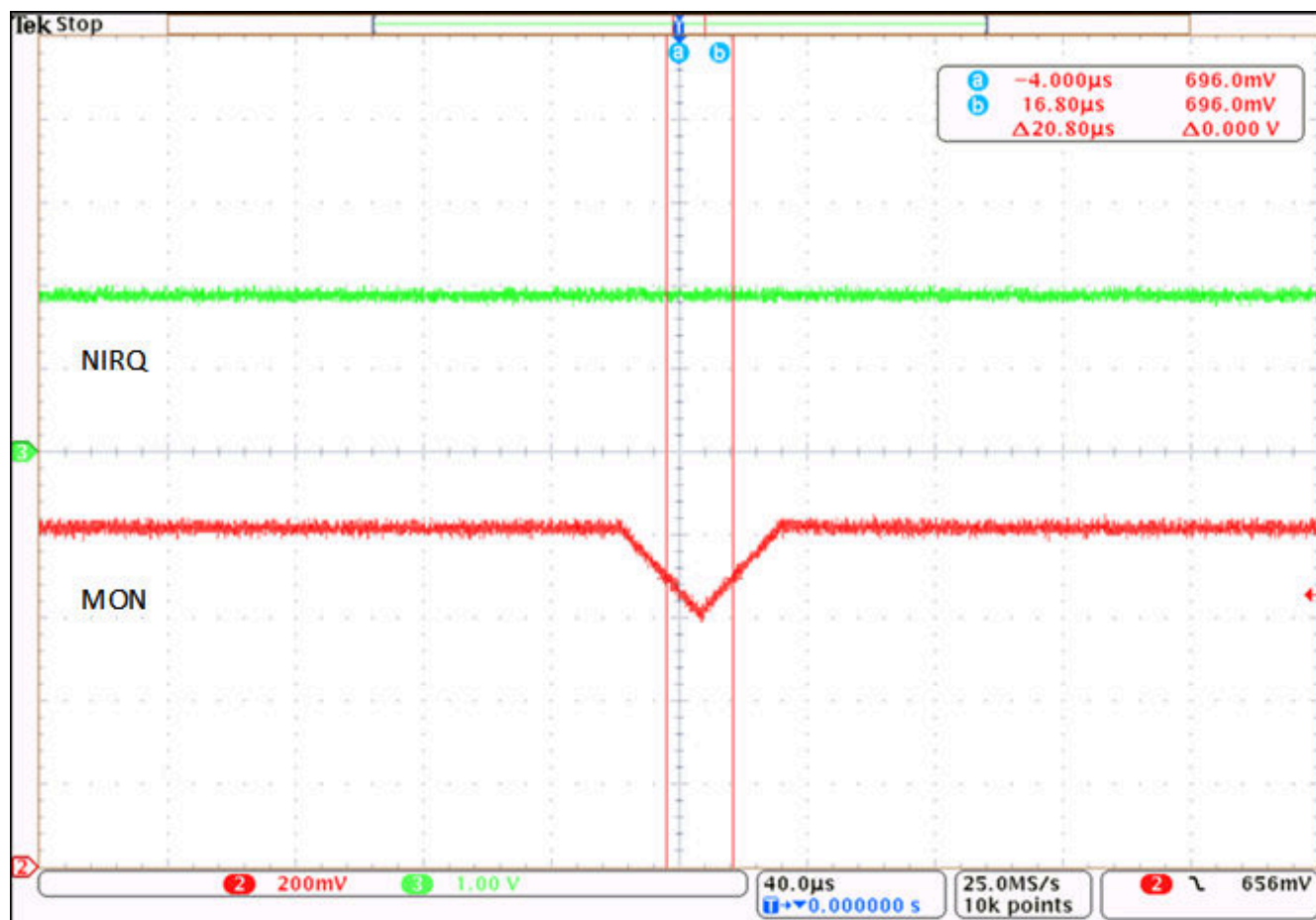
**Figure 9-6. NIRQ Not Triggered on Undervoltage Fault with 25 us UV Debounce Filter**
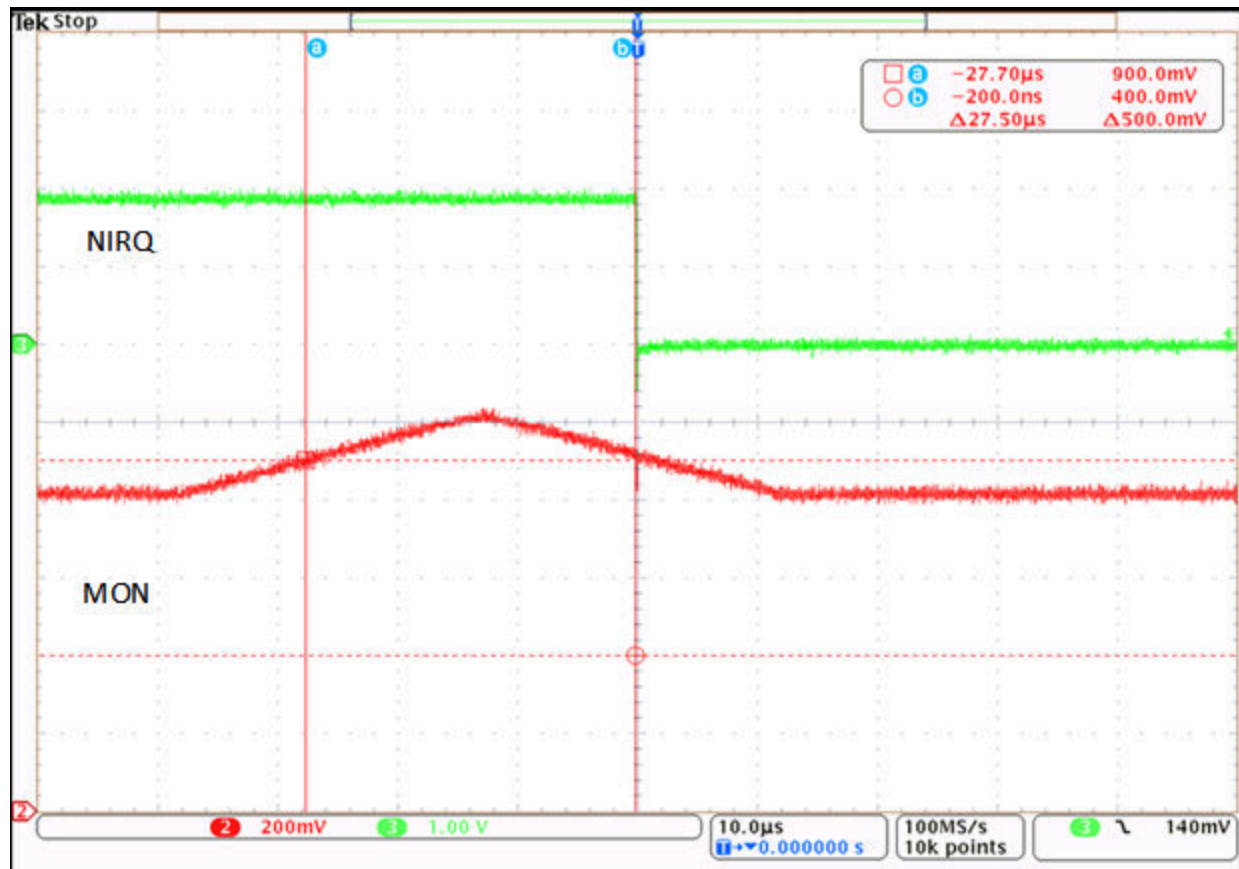
**Figure 9-7. NIRQ Triggered on Overvoltage Fault with 25 us OV Debounce Filter**
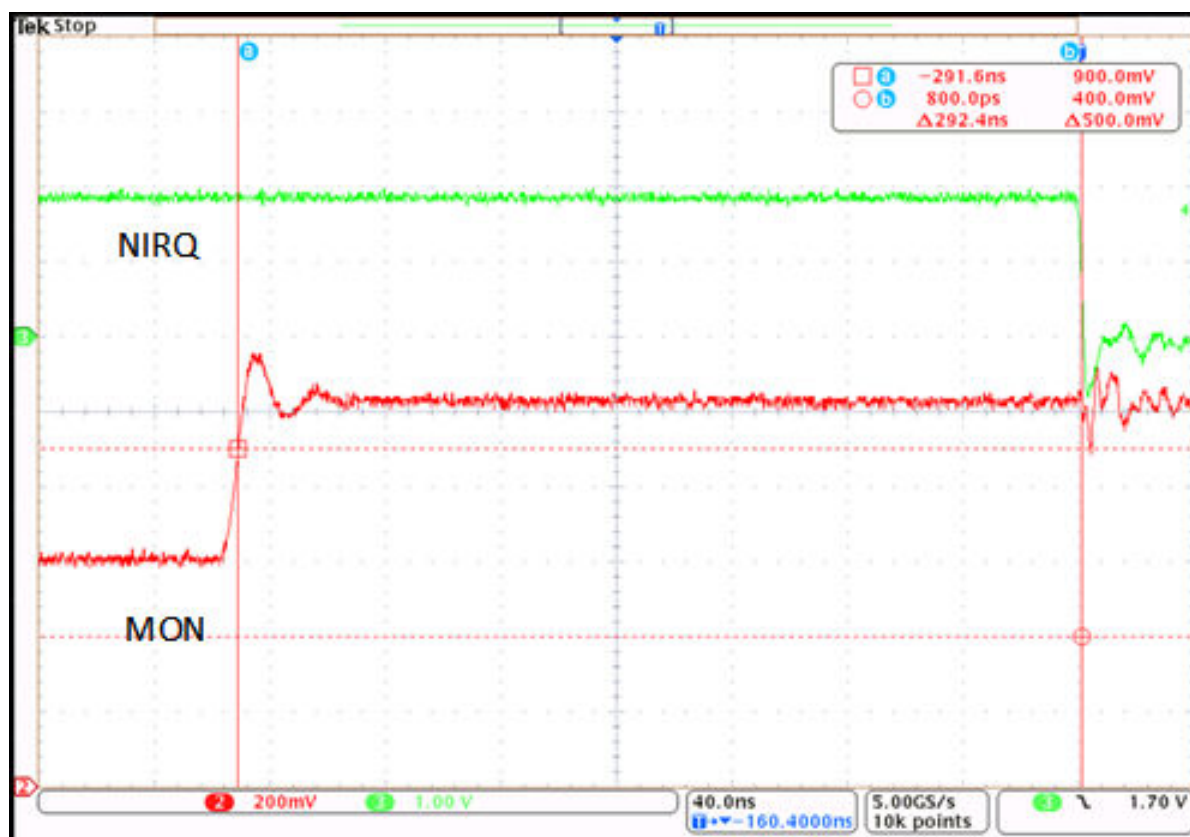
**Figure 9-8. NIRQ Propogation Delay Resulting from Overvoltage Fault**
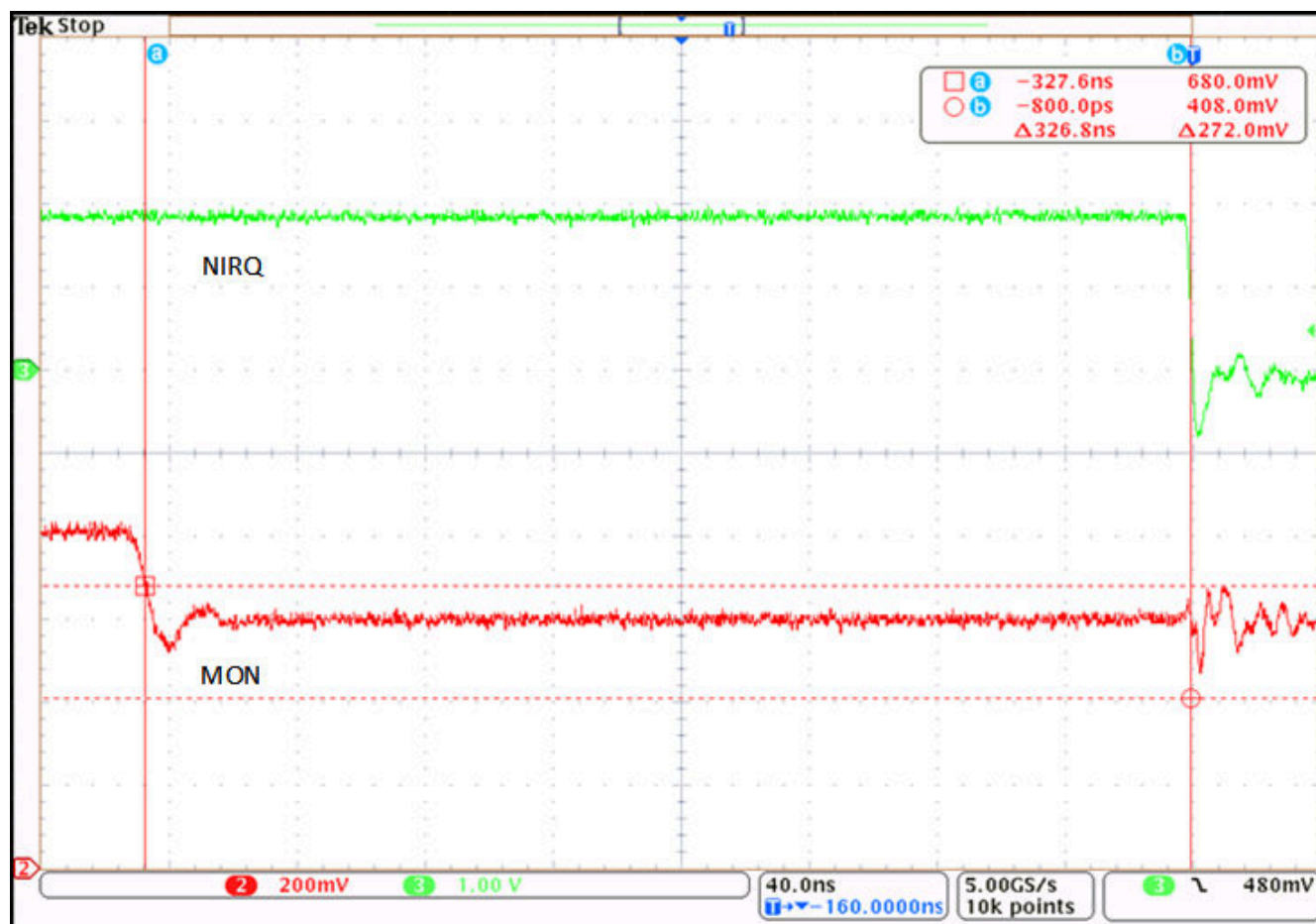
**Figure 9-9. NIRQ Propogation Delay Resulting from Undervoltage Fault**

Product Folder Links: *TPS389C03-Q1*
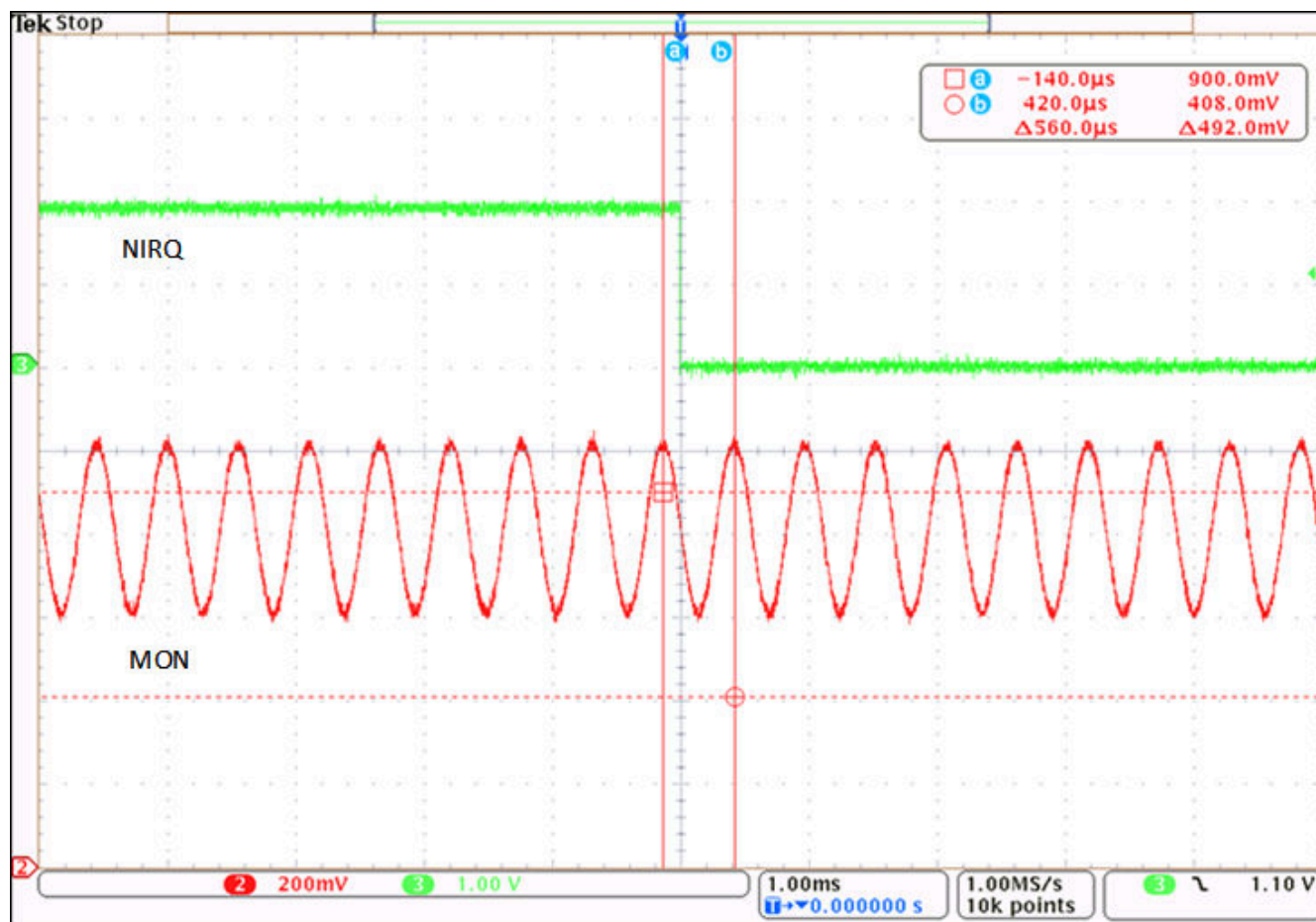
**Figure 9-10. 1 kHz Low Pass Filter Setting. NIRQ Triggered at 1.8 kHz Signal with a 0.8 V DC Component and 200 mVp-p AC Signal. OV and UV Thresholds Set to 0.9V and 0.7V. Reduced the Frequency From 2 kHz Until the NIRQ Pin Went Low.**

Product Folder Links: *TPS389C03-Q1*
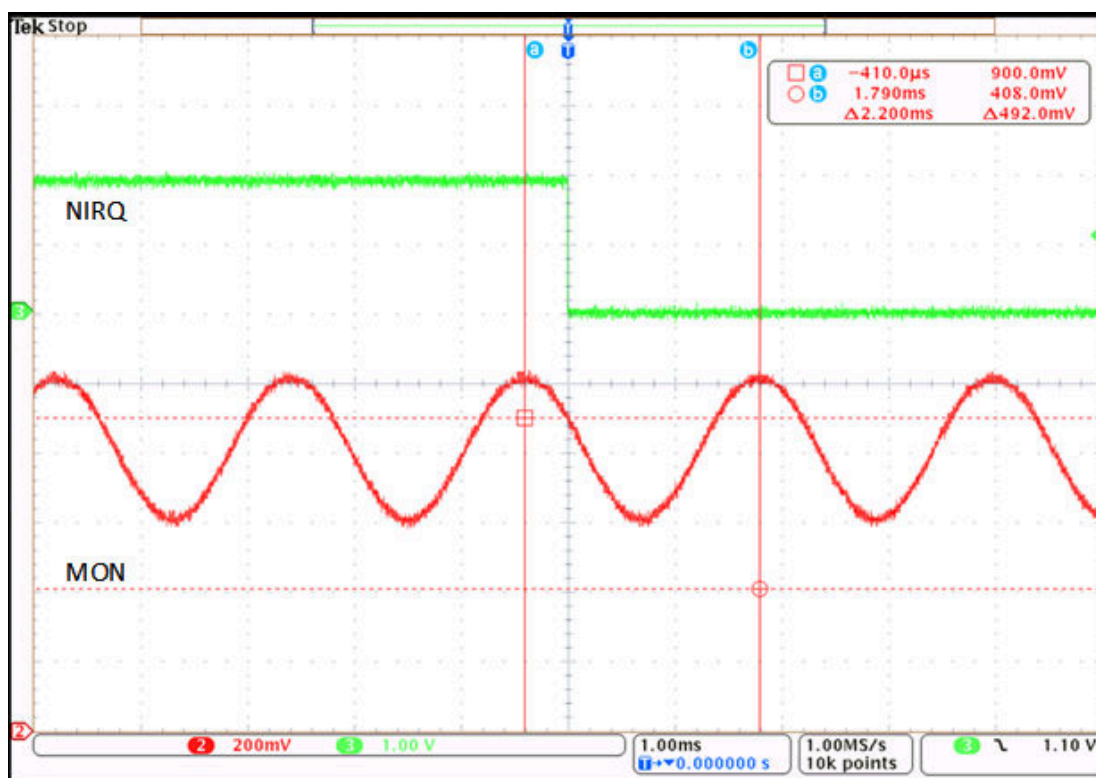
**Figure 9-11. 250 Hz Low Pass Filter setting. NIRQ Triggered at 455 Hz Signal With a 0.8 V DC Component and 200 mVp-p AC Signal. OV and UV Thresholds Set to 0.9V and 0.7V. Reduced the Frequency From 500 Hz Until the NIRQ Pin Went Low.**

Product Folder Links: *TPS389C03-Q1*
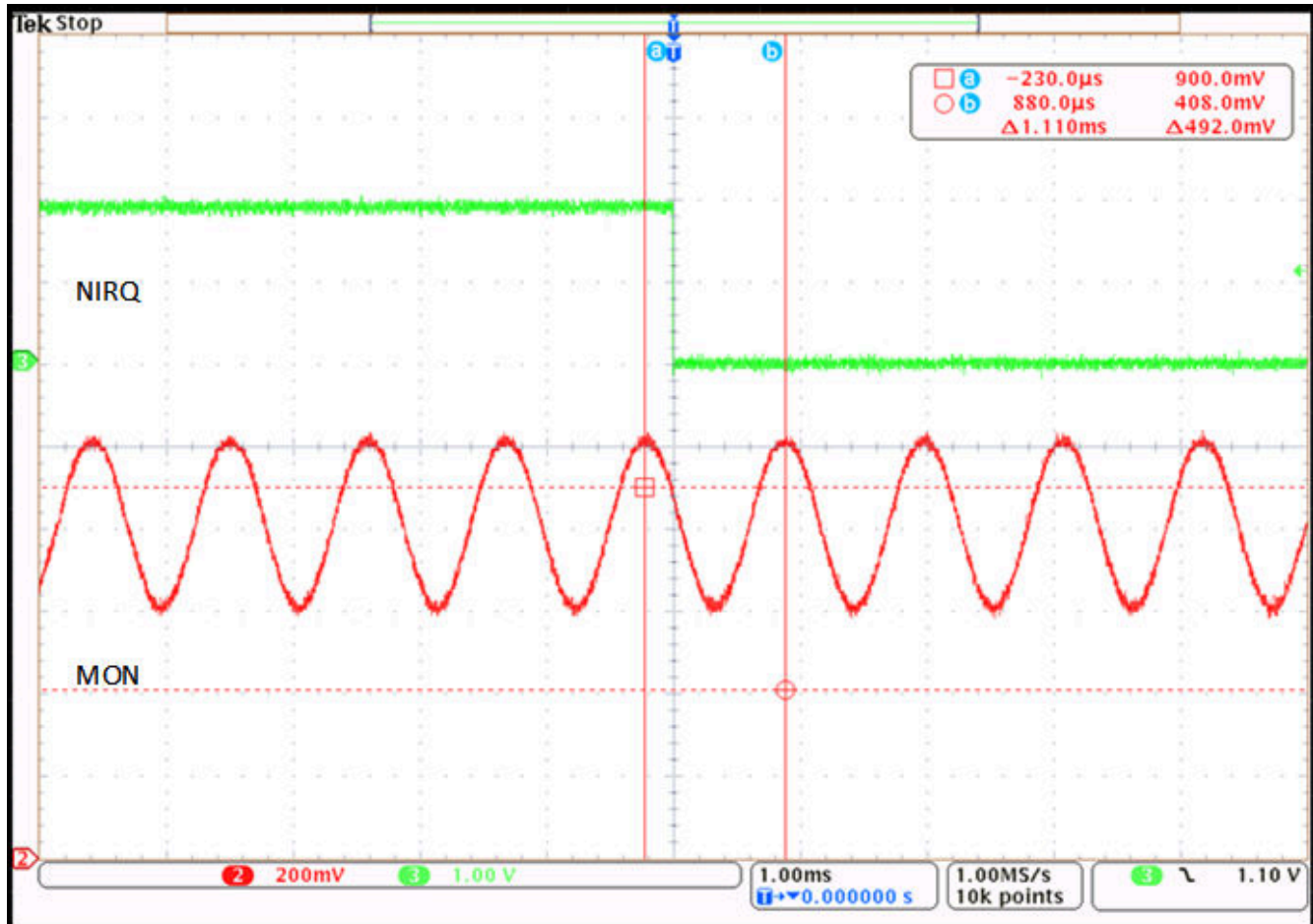
**Figure 9-12. 500 Hz Low Pass Filter Setting. NIRQ Triggered at 0.9 kHz Signal With a 0.8 V DC Component and 200 mVp-p AC Signal. OV and UV Thresholds Set to 0.9V and 0.7V. Reduced the Frequency From 1 kHz Until the NIRQ Pin Went Low.**

## 9.3 Power Supply Recommendations

### 9.3.1 Power Supply Guidelines

This device is designed to operate from an input supply with a voltage range between 2.6V to 5.5 V. It has a 6-V absolute maximum rating on the VDD pin. It is good analog practice to place a 0.1-µF to 1-µF capacitor between the VDD pin and the GND pin depending on the input voltage supply noise. If the voltage supply providing power to VDD is susceptible to any large voltage transient that exceed maximum specifications, additional precautions must be taken. See SNVA849 for more information.

## 9.4 Layout

### 9.4.1 Layout Guidelines

- Place the external components as close to the device as possible. This configuration prevents parasitic errors from occurring.
- Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC circuit and create ringing with peak voltages above the maximum VDD voltage.
- Avoid using long traces of voltage to the MON pin. Long traces increase parasitic inductance and cause inaccurate monitoring and diagnostics.

Product Folder Links: *TPS389C03-Q1*

- If differential voltage sensing is required for MON2 and/or MON3 and/or MON4 route RS_2,3,4 pin to the point of measurement. If RS_2,3,4 are not routed to the point of measurement, then route RS_2,3,4 to the GND pin of the device.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.
- For logic pins such as WD_EN and ESM, make sure the correct pull-up/down voltage is applied as per device logic levels for the associated functionality.
- For open-drain outputs like WDO, NIRQ, and NRST, select a pull-up resistor value such that the absolute maximum ratings of the device are not violated.

### 9.4.2 Layout Example
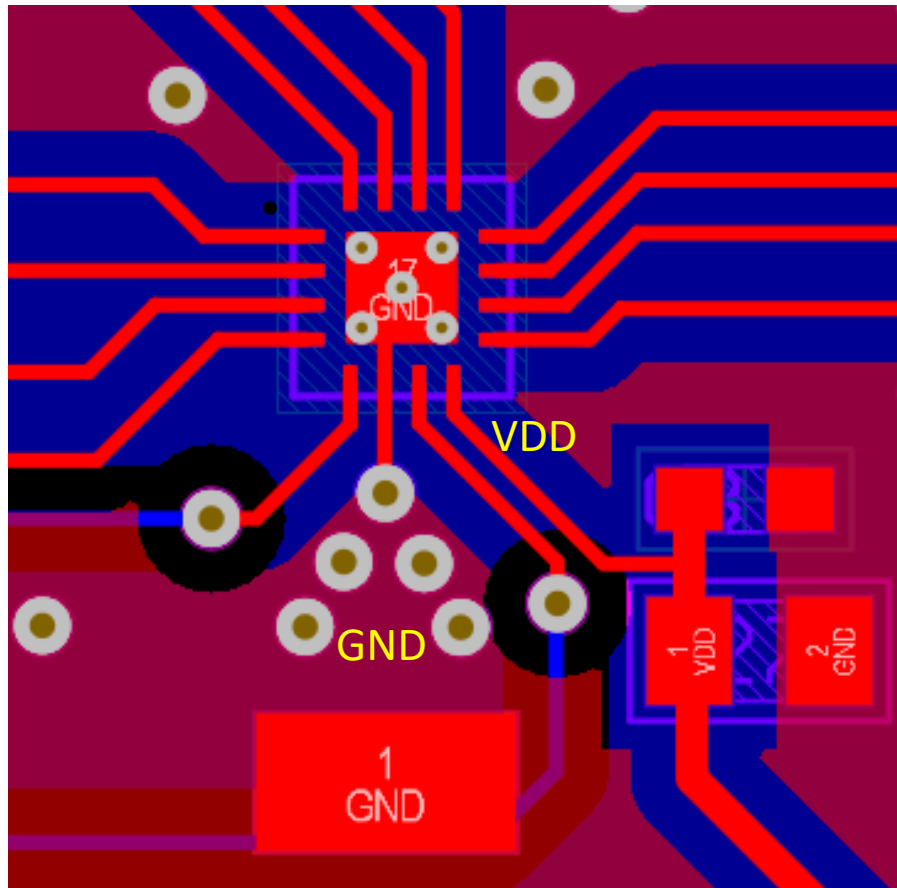


**Figure 9-13. Recommended Layout**

## 10 Device and Documentation Support

### 10.1 Device Nomenclature

Table 10-1 shows how to decode the function of the device based on the part number.

**Table 10-1. Device Thresholds**

| ORDERING CODE | Description |
|---|---|
| TPS389C0300CRTERQ1 | 3 Monitors, Q&A Watchdog, ESM |

**Table 10-2. TPS389C0300CRTERQ1 OTP Configuration**

| ADDR | DATA | Configuration Description |
|---|---|---|
| 0x00 | 0x28 | DEVICE_MODEL[7:3] and VENDOR_ID[2:0] |
| 0x01 | 0x43 | SILICON_REV[7:6] and OTP_REV[5:0] |
| 0x02 | 0xF1 | Channels disabled. MON2, 3, 4 enabled. |
| 0x11 | 0x0C | WDO_DLY not applicable for latched WDO configuration |
| 0x12 | 0x03 | BIST at POR |
| 0x13 | 0x06 | Enable UVHF Mon2,3 |
| 0x14 | 0x06 | Enable UVLF Mon2,3 |
| 0x15 | 0x06 | Enable OVHF Mon2,3 |
| 0x16 | 0x06 | Enable OVLF Mon2,3 |
| 0x1B | 0x04 | Thermal Shut Down Interrupt Enable |
| 0x1C | 0x01 | Bist Fail Interrupt |
| 0x1D | 0x25 | NRST MISMATCH, WDT → NIRQ, WDT → NRST |
| 0x1E | 0x06 | Enable Mon2,3 |
| 0x1F | 0x06 | Mon2,3 x4 Scaling |
| 0x30 | 0xBC | 4.56V UVHF Threshold Mon2 |
| 0x31 | 0xE8 | 5.44V OVHF Threshold Mon2 |
| 0x32 | 0xBC | 4.56V UVLF Threshold Mon2 |
| 0x33 | 0xE8 | 5.44V OVLF Threshold Mon2 |
| 0x34 | 0xAA | 102.4 µs De-Bounce |
| 0x35 | 0x1C | O VHF → NRST, UVHF → NRST, 1 kHz LF Cutoff |
| 0x40 | 0x6F | 3.02 V UVHF Threshold Mon3 |
| 0x41 | 0x8C | 3.6 V OVHF Threshold Mon3 |
| 0x42 | 0x6F | 3.02 V UVLF Threshold Mon3 |
| 0x43 | 0x8C | 3.6 V OVLF Threshold Mon3 |
| 0x44 | 0xAA | 102.4 µs De-bounce |
| 0x45 | 0x1C | O VHF → NRST, UVHF → NRST, 1 kHz LF Cutoff |
| 0X9E | 0x01 | ESM Threshold = 2 ms |
| 0X9F | 0x59 | Reset Delay 1 ms, WD EN |
| 0xA1 | 0x06 | AMSK ON MON2,3 |
| 0xA2 | 0x06 | AMSK OFF MON2,3 |
| 0xA5,6 | 0x00 | SEQ Timeout = 1 ms |
| 0xA8 | 0x06 | SEQ UP Mon2,3 UVLF |
| 0xA9 | 0x06 | SEQ DOWN Mon2,3 UVLF |
| 0xAA | 0x27 | WD Violation Count = 2, WD Delay = 7 |

Product Folder Links: *TPS389C03-Q1*

**Table 10-2. TPS389C0300CRTERQ1 OTP Configuration (continued)**

| ADDR | DATA | Configuration Description |
|------|------|---------------------------|
| 0xAB | 0x1D | WD Close = 30 ms |
| 0xAC | 0x1D | WD Open = 30 ms |
| 0xFA | 0x00 | 3.3V I2C interface |

## 10.2 Documentation Support

## 10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.7 Glossary

TI Glossary          This glossary lists and explains terms, acronyms, and definitions.

# 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
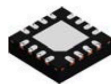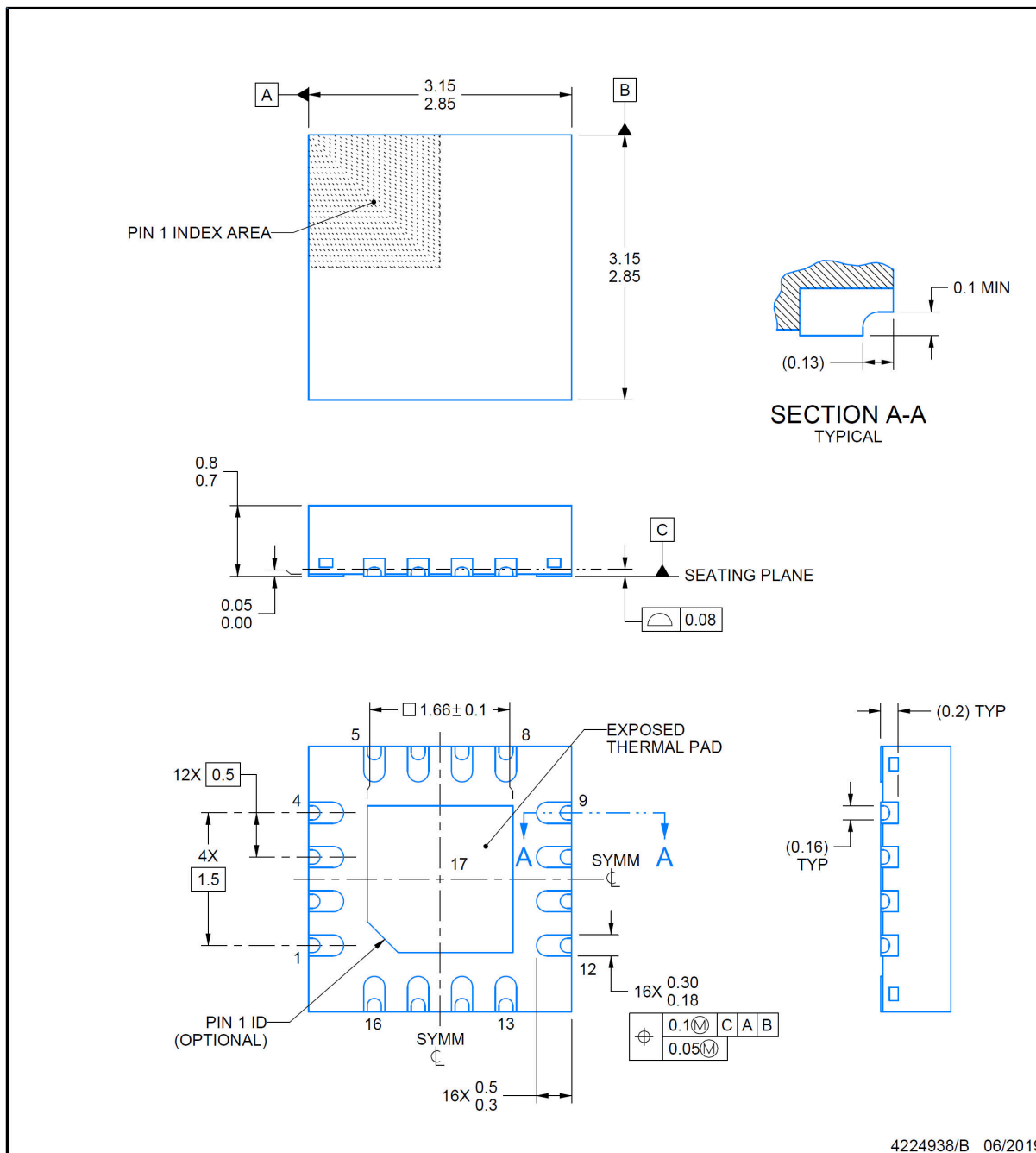
**RTE0016K**

**PACKAGE OUTLINE**

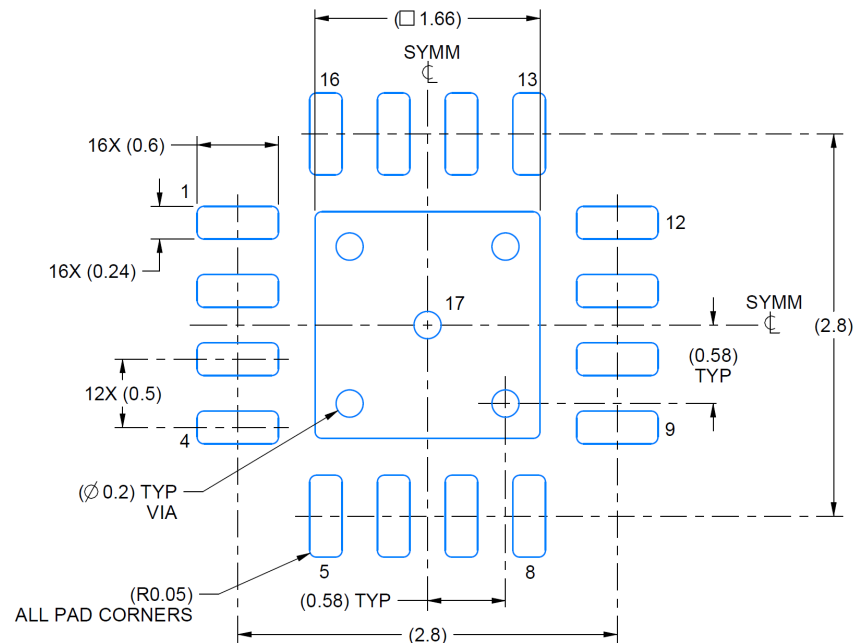**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



PIN 1 INDEX AREA

3.15
2.85

3.15
2.85

SECTION A-A
TYPICAL

0.1 MIN

(0.13)

0.8
0.7

0.05
0.00

SEATING PLANE

0.08

□ 1.66± 0.1

5          8

12X  0.5

4X
1.5

4

1

17

SYMM

PIN 1 ID
(OPTIONAL)

16        13

SYMM

EXPOSED
THERMAL PAD

9

A        SYMM        A

12

16X  0.30
     0.18

⊕  0.1Ⓜ  C A B
   0.05Ⓜ

16X  0.5
     0.3

(0.2) TYP

(0.16)
TYP

4224938/B   06/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

## RTE0016K

### WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

(□ 1.66)

SYMM

16X (0.6)

16X (0.24)

12X (0.5)

(⌀ 0.2) TYP
VIA

(R0.05)
ALL PAD CORNERS

(0.58) TYP

(0.58) TYP

SYMM

(2.8)

(2.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

0.07 MAX
ALL AROUND

METAL

EXPOSED
METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED
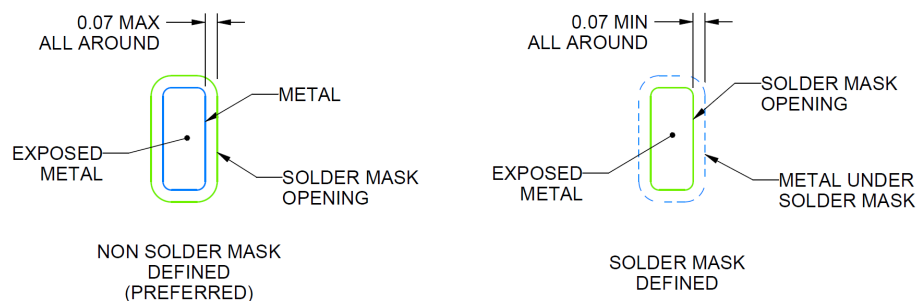
SOLDER MASK DETAILS

4224938/B   06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

Product Folder Links: TPS389C03-Q1

Texas Instruments
www.ti.com

# EXAMPLE STENCIL DESIGN

## RTE0016K

### WQFN - 0.8 mm max height
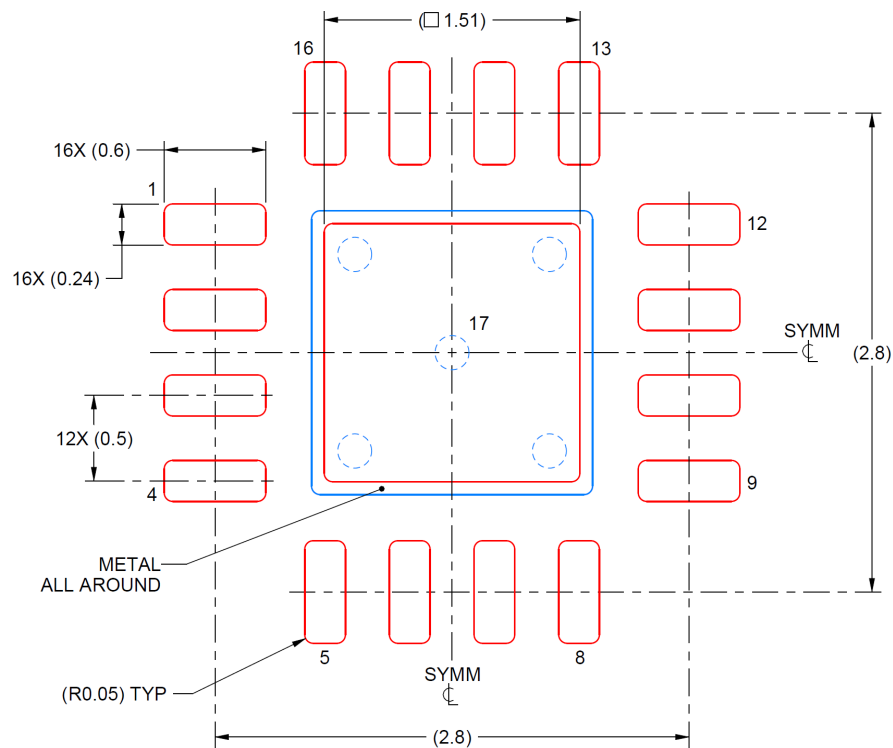
PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224938/B   06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS389C0300CRTERQ1 | ACTIVE | WQFN | RTE | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | C030Q | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**RTE 16**

**3 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
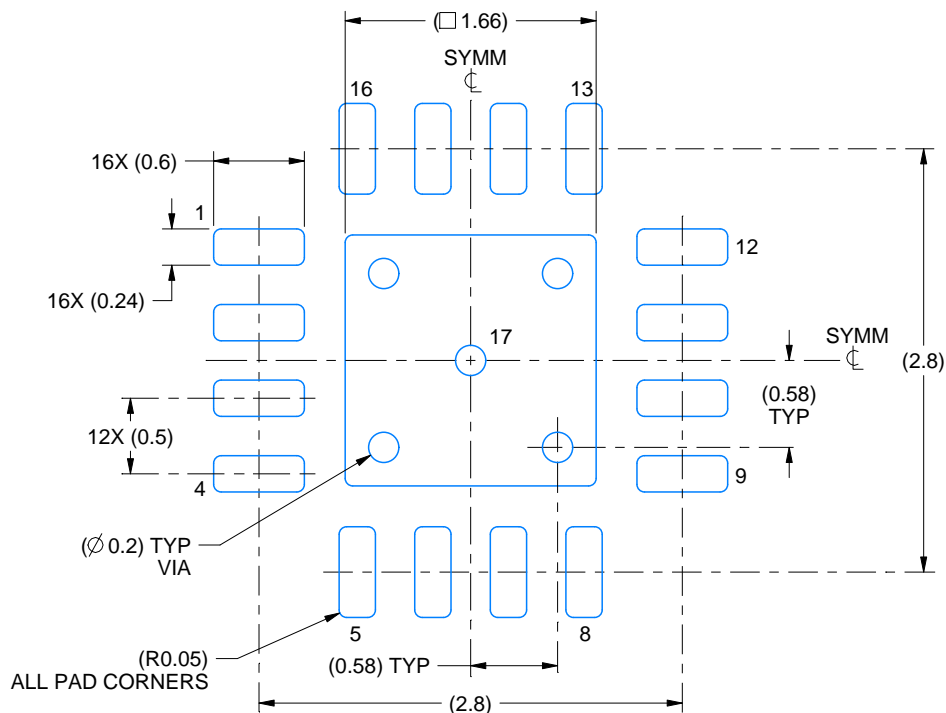Refer to the product data sheet for package details.



4225944/A

A | 3.1 / 2.9 | B

3.1 / 2.9

PIN 1 INDEX AREA

0.1 MIN

(0.13)

**SECTION A-A**
TYPICAL

0.8 / 0.7

0.05 / 0.00

C

SEATING PLANE

⌒ 0.08

□ 1.66 ± 0.1

EXPOSED THERMAL PAD

12X 0.5

4X 1.5

5    8

4

1

17

A — SYMM — A

16    13

SYMM

PIN 1 ID (OPTIONAL)

12

16X 0.30 / 0.18

⊕ 0.1 Ⓜ C A B
0.05 Ⓜ

16X 0.5 / 0.3

(0.2) TYP

(0.16) TYP

4224938/C   03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4224938/C   03/2022

NOTES: (continued)

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(□ 1.51)

16

13

16X (0.6)

1

16X (0.24)

12

17

SYMM

(2.8)

12X (0.5)

4

9

METAL
ALL AROUND

5

8

SYMM

(R0.05) TYP

(2.8)

## SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
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# IMPORTANT NOTICE AND DISCLAIMER