TPS40345 3-V to 20-V Input Synchronous Buck Controller

1 Features

- Input Voltage Range From 3 V to 20 V
- 600-kHz Switching Frequency
- High- and Low-Side FET $R_{DS(on)}$ Current Sensing
- Programmable Thermally Compensated OCP Levels
- Programmable Soft-Start
- 600-mV, 1.3% Reference Voltage
- Voltage Feed-Forward Compensation
- Supports Prebiased Output
- Frequency Spread Spectrum
- Thermal Shutdown Protection at 145°C
- 10-Pin 3-mm × 3-mm VSON Package With Ground Connection to Thermal Pad

2 Applications

- POL Modules
- Printers
- Digital TVs
- Telecom

3 Description

The TPS40345 is a synchronous buck controller that operates from 3-V to 20-V input and which can be used in cost-optimized applications. The controller implements a voltage-mode control architecture with input-voltage feed-forward compensation that responds instantly to a change in input voltage. The switching frequency is fixed at 600 kHz.

The frequency spread spectrum (FSS) feature adds to the switching frequency, significantly reducing the peak EMI noise and making it much easier to comply with EMI standards.

The TPS40345 offers design with a variety of user-programmable functions, including soft-start, overcurrent protection (OCP) levels, and loop compensation.

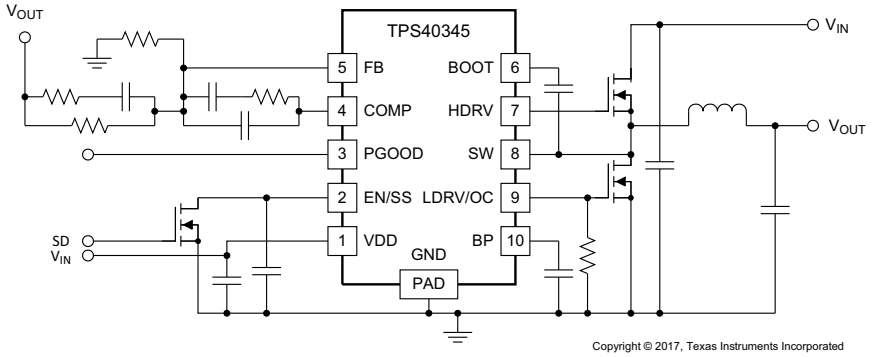
OCP level may be programmed by a single external resistor connected from the LDRV pin to circuit ground. During initial power on, the TPS40345 enters a calibration cycle, measures the voltage at the LDRV pin, and sets an internal OCP voltage level. During operation, the programmed OCP voltage level is compared to the voltage drop across the low-side FET when it is on to determine whether there is an overcurrent condition. The TPS40345 then enters a shutdown and restart cycle until the fault is removed.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS40345	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



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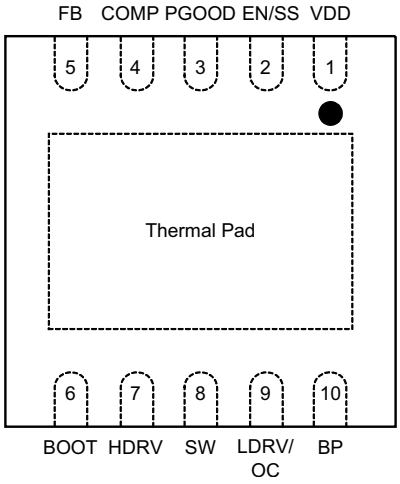
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2017	*	Initial release

5 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	6	I	Gate drive voltage for the high-side N-channel MOSFET. A 0.1-µF capacitor (typical) must be connected between this pin and SW. For low input voltage operation, an external Schottky diode from BP to BOOT is recommended to maximize the gate drive voltage for the high-side.
BP	10	O	Output bypass for the internal regulator. Connect a low ESR bypass ceramic capacitor of 1 µF or greater from this pin to GND.
COMP	4	O	Output of the error amplifier and connection node for loop feedback components.
EN/SS	2	I	Logic level input which starts or stops the controller via an external user command. Letting this pin float turns the controller on. Pulling this pin low disables the controller. This is also the soft-start programming pin. A capacitor connected from this pin to GND programs the soft-start time. The capacitor is charged with an internal current source of 10 µA. The resulting voltage ramp of this pin is also used as a second non-inverting input to the error amplifier after a 0.8 V (typical) level shift downwards. Output regulation is controlled by the internal level shifted voltage ramp until that voltage reaches the internal reference voltage of 600 mV – the voltage ramp of this pin reaches 1.4 V (typical). Optionally, a 267-kΩ resistor from this pin to BP enables the FSS feature.
FB	5	I	Inverting input to the error amplifier. In normal operation, the voltage on this pin is equal to the internal reference voltage.
PGOOD	3	O	Open-drain power good output.
HDRV	7	O	Bootstrapped gate drive output for the high-side N-channel MOSFET.
LDRV/OC	9	O	Gate drive output for the low-side synchronous rectifier N-channel MOSFET. A resistor from this pin to GND is also used to determine the voltage level for OCP. An internal current source of 10 µA flows through the resistor during initial calibration and that sets up the voltage trip point used for OCP.
VDD	1	I	Power input to the controller. Bypass VDD to GND with a low ESR ceramic capacitor of at least 1 µF close to the device.
SW	8	O	Sense line for the adaptive anti-cross conduction circuitry. Serves as common connection for the flying high-side FET driver.
GND	Thermal Pad	—	Ground connection to the controller. This is also the thermal pad used to conduct heat from the device. This connection serves a twofold purpose. The first is to provide an electrical ground connection for the device. The second is to provide a low thermal impedance path from the device die to the PCB. This pad should be tied externally to a ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VDD	–0.3	22	V
SW	–3	27	V
SW (< 100 ns pulse width, 10 µJ)		–5	V
BOOT	–0.3	30	V
HDRV	–5	30	V
BOOT-SW, HDRV-SW (differential from BOOT or HDRV to SW)	–0.3	7	V
COMP, PGOOD, FB, BP, LDRV, EN/SS	–0.3	7	V
Operating junction temperature, T_J	–40	145	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Input voltage, VDD	3		20	V
Operating junction temperature, T_J	–20		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS40345 DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = –20°C to 125°C, V_{VDD} = 12 V, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE						
V_{FB}	FB input voltage	T_J = 25°C, 3 V < V_{VDD} < 20 V	597	600	603	mV
		–20°C < T_J < 125°C, 3 V < V_{VDD} < 20 V	592	600	608	
INPUT SUPPLY						
V_{VDD}	Input supply voltage range		3		20	V
IDD_{SD}	Shutdown supply current	$V_{EN/SS}$ < 0.2 V		70	100	µA
IDD_Q	Quiescent, nonswitching	Let EN/SS float, V_{FB} = 1 V		2.5	3.5	mA
ENABLE/SOFT-START						
V_{IH}	High-level input voltage, EN/SS		0.55	0.7	1	V
V_{IL}	Low-level input voltage, EN/SS		0.27	0.3	0.33	V
I_{SS}	Soft-start source current		8	10	12	µA
V_{SS}	Soft-start voltage level		0.4	0.8	1.3	V
BP REGULATOR						
V_{BP}	Output voltage	I_{BP} = 10 mA	6.2	6.5	6.8	V
V_{DO}	Regulator dropout voltage, V_{VDD} – V_{BP}	I_{BP} = 25 mA, V_{VDD} = 3 V		70	110	mV
OSCILLATOR						
f_{SW}	PWM frequency		540	600	660	kHz
V_{RAMP} (1)	Ramp amplitude		V_{VDD}/6.6	V_{VDD}/6	V_{VDD}/5.4	V
f_{SWFSS}	Frequency spread-spectrum frequency deviation		12%			f_{SW}
f_{MOD}	Modulation frequency			25		kHz
PWM						
D_{MAX} (1)	Maximum duty cycle	V_{FB} = 0 V, 3 V < V_{VDD} < 20 V	90%			
$t_{ON(min)}$ (1)	Minimum controllable pulse width				70	ns
t_{DEAD}	Output driver dead time	HDRV off to LDRV on	5	25	35	ns
		LDRV off to HDRV on	5	25	30	
ERROR AMPLIFIER						
G_{BWP} (1)	Gain bandwidth product		10	24		MHz
A_{OL} (1)	Open loop gain		60			dB
I_{IB}	Input bias current (current out of FB pin)	V_{FB} = 0.6 V			75	nA
I_{EAOP}	Output source current	V_{FB} = 0 V	2			mA
I_{EAOM}	Output sink current	V_{FB} = 1 V	2			
PGOOD						
V_{OV}	Feedback upper voltage limit for PGOOD		655	675	700	mV
V_{UV}	Feedback lower voltage limit for PGOOD		500	525	550	
$V_{PGD-HYST}$	PGOOD hysteresis voltage at FB			25	40	
R_{PGD}	PGOOD pulldown resistance	V_{FB} = 0 V, I_{FB} = 5 mA		30	70	Ω
I_{PGDLK}	PGOOD leakage current	550 mV < V_{FB} < 655 mV, V_{PGOOD} = 5 V		10	20	µA

(1) Ensured by design. Not production tested.

Electrical Characteristics (continued)

T_J = –20°C to 125°C, V_{VDD} = 12 V, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVERS						
R_{HDHI}	High-side driver pullup resistance	$V_{BOOT} – V_{SW}$ = 5 V, I_{HDRV} = –100 mA	0.8	1.5	2.5	Ω
R_{HDLO}	High-side driver pulldown resistance	$V_{BOOT} – V_{SW}$ = 5 V, I_{HDRV} = 100 mA	0.5	1	2.2	Ω
R_{LDHI}	Low-side driver pullup resistance	I_{LDRV} = -100 mA	0.8	1.5	2.5	Ω
R_{LDLO}	Low-side driver pulldown resistance	I_{LDRV} = 100 mA	0.35	0.6	1.2	Ω
t_{HRISE} (1)	High-side driver rise time	C_{LOAD} = 5 nF		15		ns
t_{HFALL} (1)	High-side driver fall time			12		ns
t_{LRISE} (1)	Low-side driver rise time			15		ns
t_{LFALL} (1)	Low-side driver fall time			10		ns
OVERCURRENT PROTECTION						
$t_{PSSC(min)}$ (1)	Minimum pulse time during short circuit			250		ns
t_{BLNKH} (1)	Switch leading-edge blanking pulse time			150		ns
V_{OCH}	OC threshold for high-side FET	T_J = 25°C	360	450	580	mV
I_{OCSET}	OCSET current source	T_J = 25°C	9.5	10	10.5	µA
$V_{LD-CLAMP}$	Maximum clamp voltage at LDRV		260	340	400	mV
V_{OCLOS}	OC comparator offset voltage for low-side FET	T_J = 25°C	–8		8	mV
V_{OCLPRO} (1)	Programmable OC range for low-side FET	T_J = 25°C	12		300	mV
V_{THTC} (1)	OC threshold temperature coefficient (both high-side and low-side)			3000		ppm
t_{OFF}	OC retry cycles on EN/SS pin			4		Cycle
BOOT DIODE						
V_{DFWD}	Bootstrap diode forward voltage	I_{BOOT} = 5 mA		0.8		V
THERMAL SHUTDOWN						
T_{JSD} (1)	Junction shutdown temperature			145		°C
T_{JSDH} (1)	Hysteresis			20		°C

6.6 Typical Characteristics

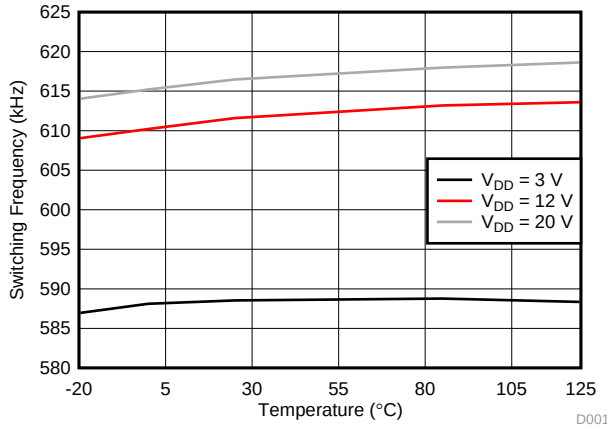


Figure 1. Switching Frequency vs Junction Temperature

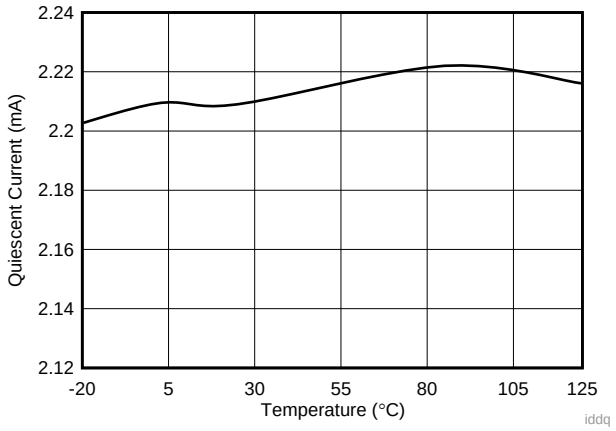


Figure 2. Quiescent Current vs Junction Temperature

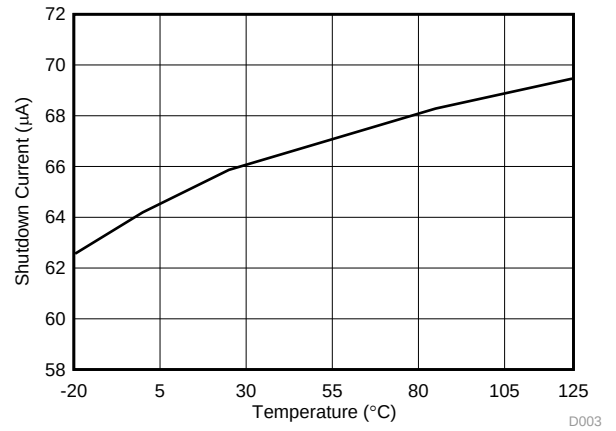


Figure 3. Shutdown Current vs Junction Temperature

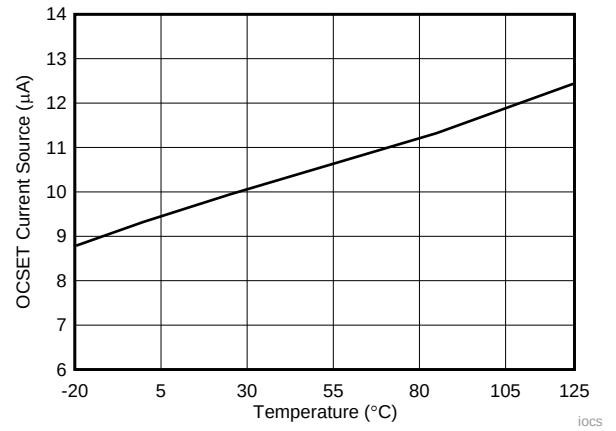


Figure 4. OCSET Current Source vs Junction Temperature

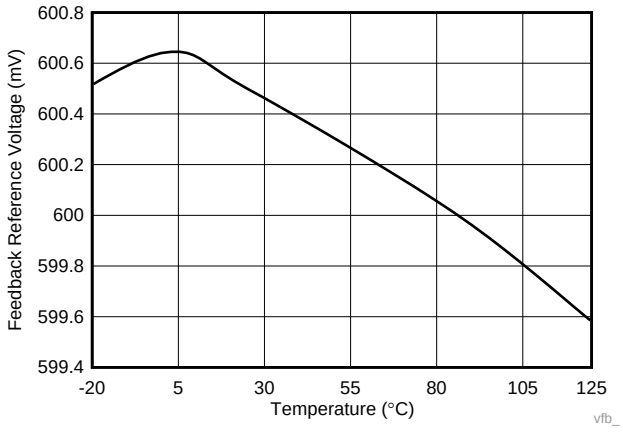


Figure 5. Feedback Reference Voltage vs Junction Temperature

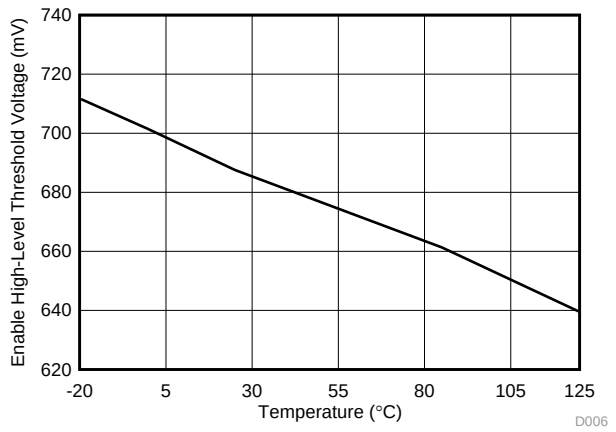


Figure 6. Enable High-Level Threshold Voltage vs Junction Temperature

Typical Characteristics (continued)

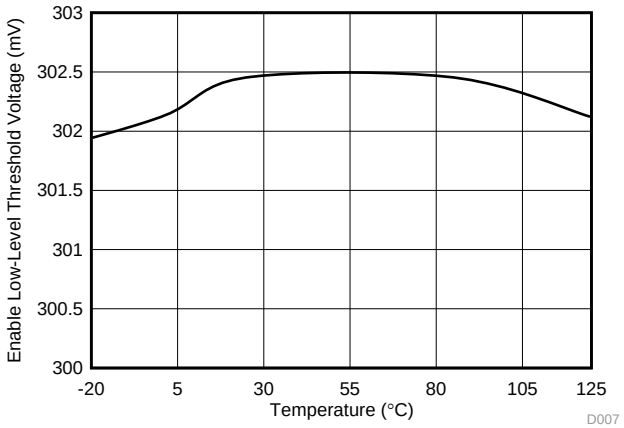


Figure 7. Enable Low-Level Threshold Voltage vs Junction Temperature

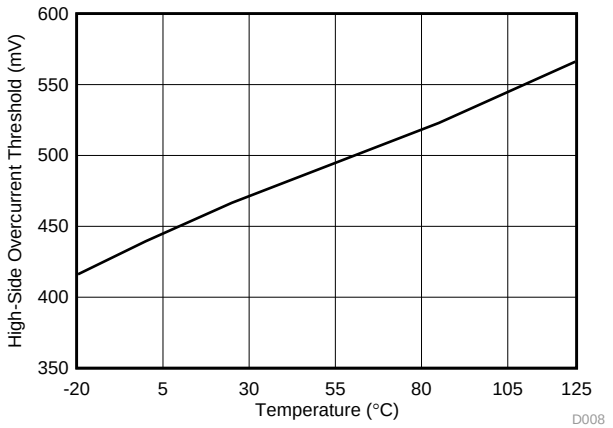


Figure 8. High-Side Overcurrent Threshold vs Junction Temperature

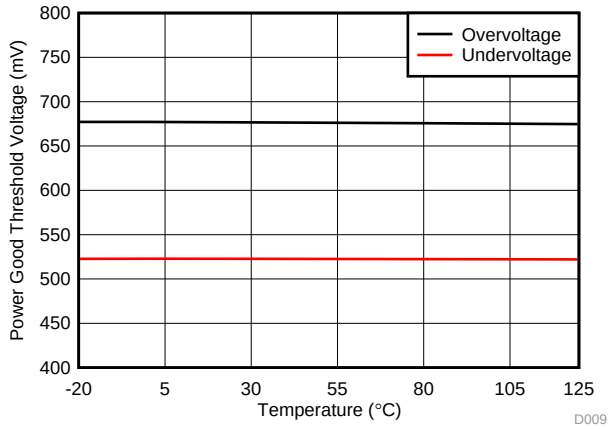


Figure 9. Power Good Threshold Voltage vs Junction Temperature

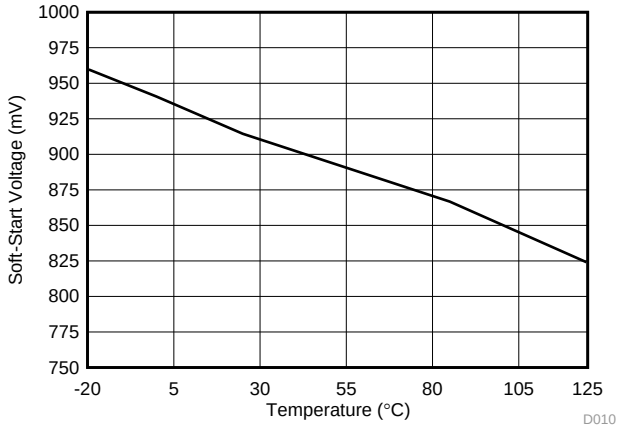


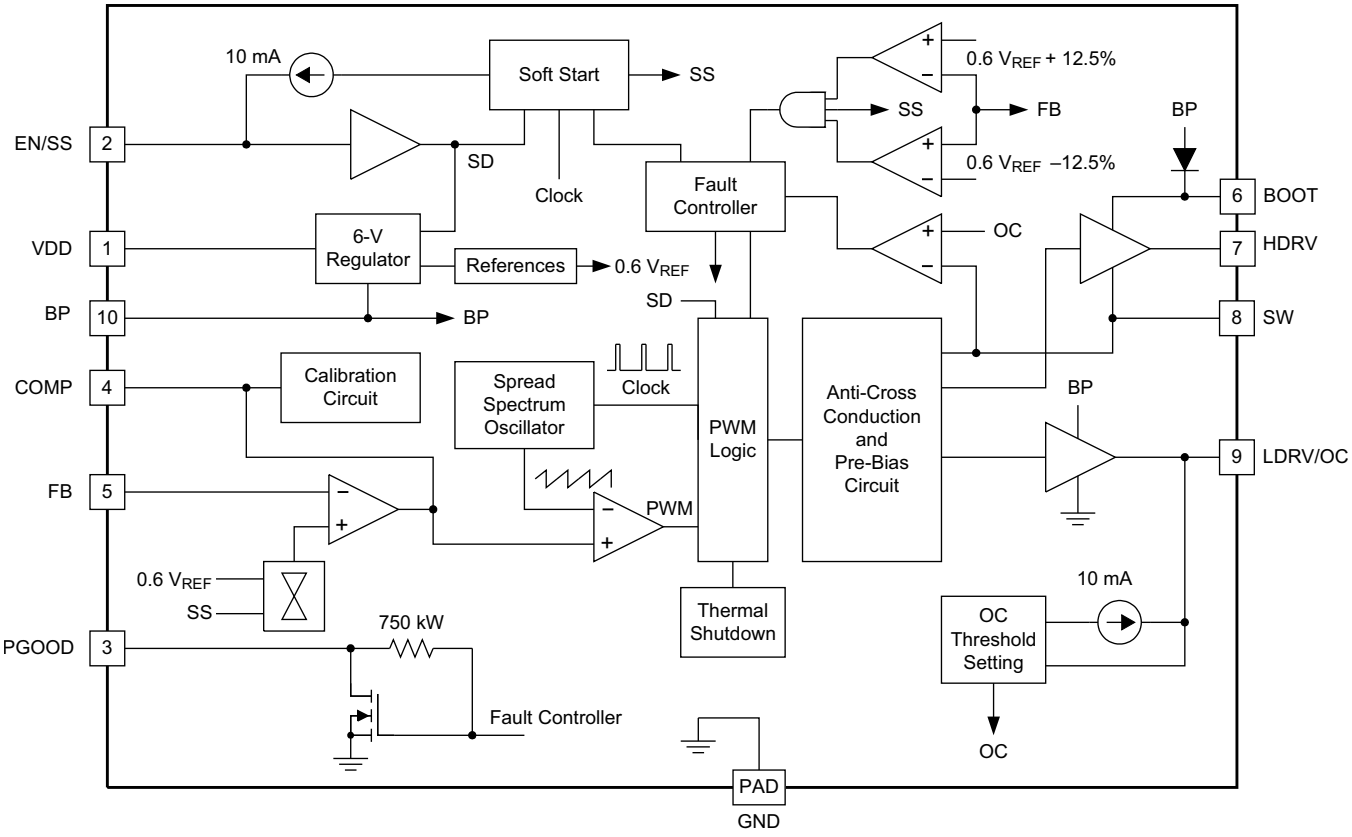
Figure 10. Soft-Start Voltage vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS40345 is a cost-optimized synchronous buck controller providing high-end features to construct high-performance DC–DC converters. Prebias capability eliminates concerns about damaging sensitive loads during start-up. Programmable overcurrent protection levels and hiccup overcurrent fault recovery maximize design flexibility and minimize power dissipation in the event of a prolonged output short. The frequency spread spectrum (FSS) feature reduces peak EMI noise by spreading the initial energy of each harmonic along a frequency band, thus giving a wider spectrum with lower amplitudes.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Voltage Reference

The 600-mV bandgap cell is internally connected to the noninverting input of the error amplifier. The reference voltage is trimmed with the error amplifier in a unity gain configuration to remove amplifier offset from the final regulation voltage. The 1.3% tolerance on the reference voltage allows the user to design a very accurate power supply.

Feature Description (continued)

7.3.2 Enable Functionality, Start-Up Sequence and Timing

After input power is applied, an internal current source of 40 µA starts to charge up the soft-start capacitor connected from EN/SS to GND. When the voltage across that capacitor increases to 0.7 V, it enables the internal BP regulator followed by a calibration. The total calibration time is about 1.9 ms. See Figure 11. During the calibration, the device performs in the following way. It disables the LDRV drive and injects an internal 10-µA current source to the resistor connected from LDRV to GND. The voltage developed across that resistor is then sampled and latched internally as the OCP trip level until one cycles the input or toggles the EN/SS.

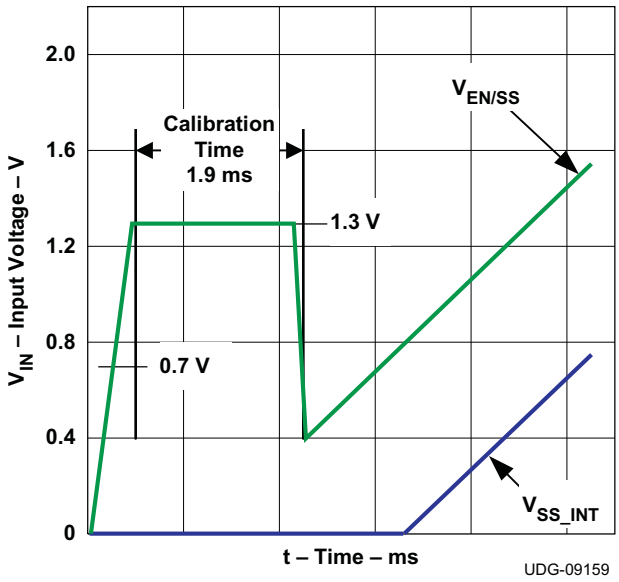


Figure 11. Start-Up Sequence and Timing

The voltage at EN/SS is internally clamped to 1.3 V before and/or during calibration to minimize the discharging time once calibration. The discharging current is from an internal current source of 140 µA and it pulls the voltage down to 0.4 V. The discharging current then initiates the soft-start by charging up the capacitor using an internal current source of 10 µA. The resulting voltage ramp on this pin is used as a second noninverting input to the error amplifier after an 800 mV (typical) downward level-shift; therefore, actual soft-start does not occur until the voltage at this pin reaches 800 mV.

If EN/SS is left floating, the controller starts automatically. EN/SS must be pulled down to less than 270 mV to ensure that the chip is in shutdown mode.

7.3.3 Soft-Start Time

The soft-start time of the TPS40345 is user programmable by selecting a single capacitor. The EN/SS pin sources 10 µA to charge this capacitor. The actual output ramp-up time is the amount of time that it takes for the 10 µA to charge the capacitor through a 600-mV range. There is some initial lag due to calibration and an offset (800 mV) from the actual EN/SS pin voltage to the voltage applied to the error amplifier.

The soft-start is done in a closed-loop fashion, meaning that the error amplifier controls the output voltage at all times during the soft-start period and the feedback loop is never open as occurs in duty cycle limit soft-start schemes. The error amplifier has two non-inverting inputs, one connected to the 600-mV reference voltage, and the other connected to the offset EN/SS pin voltage. The lower of these two voltages is what the error amplifier controls the FB pin. As the voltage on the EN/SS pin ramps up past approximately 1.4 V (800-mV offset voltage plus the 600 mV reference voltage), the 600-mV reference voltage becomes the dominant input and the converter has reached its final regulation voltage.

The capacitor required for a given soft-start ramp time for the output voltage is given by Equation 1.

$$C_{SS} = \left(\frac{I_{SS}}{V_{FB}} \right) \times t_{SS}$$

Feature Description (continued)

where

- C_{SS} is the required capacitance on the EN/SS pin. (F)
- I_{SS} is the soft-start source current (10 µA).
- V_{FB} is the feedback reference voltage (0.6 V).
- t_{SS} is the desired soft-start ramp time (s). (1)

7.3.4 Oscillator and Frequency Spread Spectrum (FSS)

The oscillator frequency is internally fixed. The TPS40345 operating frequency is 600 kHz.

Connecting a resistor with a value of 267 kΩ ±10% from BP to EN/SS enables the FSS feature. When the FSS is enabled, it spreads the internal oscillator frequency over a minimum 12% window using a 25-kHz modulation frequency with triangular profile. By modulating the switching frequency, side-bands are created. The emission power of the fundamental switching frequency and its harmonics is distributed into smaller pieces scattered around many sideband frequencies. The effect significantly reduces the peak EMI noise and makes it much easier for the resultant emission spectrum to pass EMI regulations.

7.3.5 Overcurrent Protection

Programmable OCP level at LDRV is from 6 mV to 150 mV at room temperature with 3000 ppm temperature coefficient to help compensate for changes in the low-side FET channel resistance as temperature increases. With a scale factor of 2, the actual trip point across the low-side FET is in the range of 12 mV to 300 mV. The accuracy of the internal current source is ±5%. Overall offset voltage, including the offset voltage of the internal comparator and the amplifier for scale factor of 2, is limited to ±8 mV.

Maximum clamp voltage at LDRV is 340 mV to avoid turning on the low-side FET during calibration and in a prebiased condition. The maximum clamp voltage is fixed and it does not change with temperature. If the voltage drop across R_{OCSET} reaches the 340-mV maximum clamp voltage during calibration (no R_{OCSET} resistor included), it disables OC protection. Once disabled, there is no low-side or high-side current sensing.

OCP level at HDRV is fixed at 450 mV with 3000-ppm temperature coefficient to help compensate for changes in the high-side FET channel resistance as temperature increases. OCP at HDRV provides pulse-by-pulse current limiting.

OCP sensing at LDRV is a true inductor valley current detection, using sample and hold. Equation 2 can be used to calculate R_{OCSET}:

$$R_{OCSET} = \left(\frac{\left(I_{OUT(max)} - \left(\frac{I_{P-P}}{2} \right) \right) \times R_{DS(on)} - V_{OCLOS}}{2 \times I_{OCSET}} \right)$$

where

- I_{OCSET} is the internal current source.
- V_{OCLOS} is the overall offset voltage.
- I_{P-P} is the peak-to-peak inductor current.
- $R_{DS(on)}$ is the drain to source ON-resistance of the low-side FET.
- $I_{OUT(max)}$ is the trip point for OCP.
- R_{OCSET} is the resistor used for setting the OCP level. (2)

To avoid overcurrent tripping in normal operating load range, calculate R_{OCSET} using Equation 2 with:

- The maximum $R_{DS(ON)}$ at room temperature
- The lower limit of V_{OCLOS} (–8 mV) and the lower limit of I_{OCSET} (9.5 µA) from the *Electrical Characteristics* table.
- The peak-to-peak inductor current I_{P-P} at minimum input voltage

Feature Description (continued)

Overcurrent is sensed across both the low-side FET and the high-side FET. If the voltage drop across either FET exceeds the OC threshold, a count increments one count. If no OC is detected on either FET, the fault counter decrements by one count. If three OC pulses are summed, a fault condition is declared which cycles the soft-start function in a hiccup mode. Hiccup mode consists of four dummy soft-start timeouts followed by a real one if overcurrent condition is encountered during normal operation, or five dummy soft-start timeouts followed by a real one if overcurrent condition occurs from the beginning during start. This cycle continues indefinitely until the fault condition is removed.

7.3.6 Drivers

The drivers for the external high-side and low-side MOSFETs can drive a gate-to-source voltage of V_{BP}. The LDRV driver for the low-side MOSFET switches between BP and GND, while the HDRV driver for the high-side MOSFET is referenced to SW and switches between BOOT and SW. The drivers have nonoverlapping timing that is governed by an adaptive delay circuit to minimize body diode conduction in the synchronous rectifier.

7.3.7 Prebias Start-Up

The TPS40345 contains a circuit to prevent current from being pulled from the output during start-up in the condition the output is prebiased. There are no PWM pulses until the internal soft-start voltage rises above the error amplifier input (FB pin), if the output is prebiased. Once the soft-start voltage exceeds the error amplifier input, the controller slowly initiates synchronous rectification by starting the synchronous rectifier with a narrow on time. The controller then increments that on time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This approach prevents the sinking of current from a prebiased output, and ensures the output voltage start-up and ramp to regulation is smooth and controlled.

7.3.8 Power Good

The TPS40345 provides an indication that output is good for the converter. This is an open-drain signal and pulls low when any condition exists that would indicate that the output of the supply might be out of regulation. These conditions include the following:

- V_{FB} is more than ±12.5% from nominal.
- Soft-start is active.
- A short-circuit condition has been detected.

NOTE

When there is no power to the device, PGOOD is not able to pull close to GND if an auxiliary supply is used for the power good indication. In this case, a built-in resistor connected from drain to gate on the PGOOD pulldown device makes the PGOOD pin look approximately like a diode to GND.

7.3.9 Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 145°C, the PWM and the oscillator are turned off and HDRV and LDRV are driven low. When the junction cools to the required level (125°C typical), the PWM initiates soft-start as during a normal power-up cycle.

7.4 Device Functional Modes

7.4.1 Modes of Operation

7.4.1.1 UVLO

In UVLO, VDD is less than UVLO_ON, the BP6 regulator is off, and the HDRV and LDRV are held low by internal passive discharge resistors.

7.4.1.2 Disable

Disable is forced by holding SS/EN below 0.4 V. In disable, the BP6 regulator is off, and both HDRV and LDRV are held low by passive discharge resistors.

Device Functional Modes (continued)

7.4.1.3 Calibration

Each enable of the TPS40345 device requires a calibration which lasts approximately 2 ms. During calibration the TPS40345 device LDRV and HDRV are held off by its pulldown drivers while the device configures as detailed in *Enable Functionality, Start-Up Sequence and Timing*.

7.4.1.4 Converting

When calibration completes, the TPS40345 ramps its reference voltage as described in *Soft-Start Time*, and the states of the LDRV and HDRV drivers are dictated by the COMP pin to regulate the FB pin equal to the internal reference.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS40345 a cost-optimized synchronous buck controllers providing high-end features to construct high-performance DC-DC converters. Prebias capability eliminates concerns about damaging sensitive loads during start-up. Programmable overcurrent protection levels and hiccup overcurrent fault recovery maximize design flexibility and minimize power dissipation in the event of a prolonged output short. frequency spread spectrum (FSS) feature reduces peak EMI noise by spreading the initial energy of each harmonic along a frequency band, thus giving a wider spectrum with lower amplitudes.

8.2 Typical Applications

For this 20-A, 12-V to 1.2-V design, the 600-kHz TPS40345 was selected for a balance between small size and high efficiency.

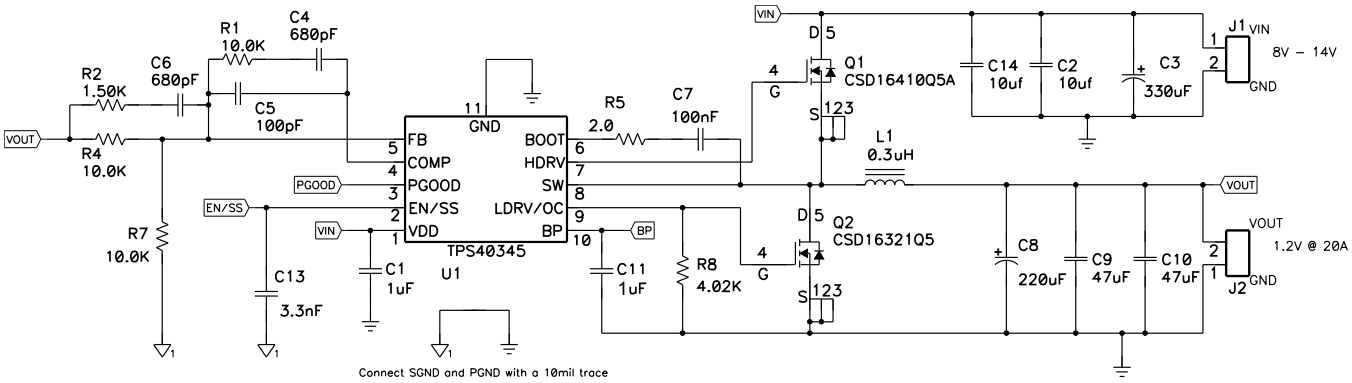


Figure 12. TPS40345 Design Example Schematic

Typical Applications (continued)

8.2.1 Design Requirements

For this example, follow the design parameters listed in Table 1.

Table 1. Design Example Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		8		14	V
$V_{INripple}$	Input ripple	I_{OUT} = 20 A			0.5	V
V_{OUT}	Output voltage	0 A ≤ I_{OUT} ≤ 20 A	1.164	1.2	1.236	V
	Line regulation	8 V ≤ V_{IN} ≤ 14 V			0.5%	
	Load regulation	0 A ≤ I_{OUT} ≤ 20 A			0.5%	
V_{RIPPLE}	Output ripple	I_{OUT} = 20 A			36	mV
V_{OVER}	Output overshoot	5 A ≤ I_{OUT} ≤ 15 A		100		mV
V_{UNDER}	Output undershoot	5 A ≤ I_{OUT} ≤ 15 A		100		mV
I_{OUT}	Output current	8 V ≤ V_{IN} ≤ 14 V	0		20	A
t_{SS}	Soft-start time	V_{IN} = 12 V		1.5		ms
I_{SCP}	Short-circuit current trip point		26			A
f_{SW}	Switching frequency			600		kHz
	Size				1.5	in^2

8.2.2 Detailed Design Procedure

8.2.2.1 Selecting the Switching Frequency

To achieve the small size for this design the TPS40345, with f_{SW} = 600 kHz, is selected for minimal external component size.

8.2.2.2 Inductor Selection (L1)

Synchronous buck power inductors are typically sized for approximately 30% peak-to-peak ripple current (I_{RIPPLE}).

Given this target ripple current, the required inductor size can be calculated in Equation 3.

$$L \approx \frac{V_{IN(max)} - V_{OUT}}{0.3 \times I_{OUT}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{F_{SW}} = \frac{14V - 1.2V}{0.3 \times 20A} \times \frac{1.2V}{14V} \times \frac{1}{600kHz} = 305nH \quad (3)$$

Selecting a standard 300-nH inductor value, solve for I_{RIPPLE} = 6 A

The RMS current through the inductor is approximated by Equation 4.

$$I_{Lrms} = \sqrt{I_{Lavg}^2 + \tfrac{1}{12} I_{RIPPLE}^2} = \sqrt{I_{OUT}^2 + \tfrac{1}{12} I_{RIPPLE}^2} = \sqrt{20^2 + \tfrac{1}{12} 6^2} = 20.07\ A \quad (4)$$

8.2.2.3 Output Capacitor Selection (C12)

The selection of the output capacitor is typically driven by the output transient response. Equation 5 and Equation 6 overestimate the voltage deviation to account for delays in the loop bandwidth and can be used to determine the required output capacitance.

$$V_{OVER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{OUT}} = \frac{I_{TRAN}^2 \times L}{V_{OUT} \times C_{OUT}} \quad (5)$$

$$V_{UNDER} < \frac{I_{TRAN}}{C_{OUT}} \times \Delta T = \frac{I_{TRAN}}{C_{OUT}} \times \frac{I_{TRAN} \times L}{V_{IN} - V_{OUT}} = \frac{I_{TRAN}^2 \times L}{(V_{IN} - V_{OUT}) \times C_{OUT}} \quad (6)$$

If $V_{IN(min)} > 2 \times V_{OUT}$, use overshoot (Equation 5) to calculate minimum output capacitance. If $V_{IN(min)} < 2 \times V_{OUT}$, use undershoot (Equation 6) to calculate minimum output capacitance.

$$C_{OUT(MIN)} = \frac{I_{TRAN(MAX)}^{2} \times L}{(V_{OUT}) \times V_{OVER}} = \frac{10^{2} \times 300nH}{1.2 \times 100mV} = 250\mu F \quad (7)$$

With a minimum capacitance, the maximum allowable ESR is determined by the maximum ripple voltage and is approximated by Equation 8.

$$ESR_{max} = \frac{V_{RIPPLE(Total)} - V_{RIPPLE(CAP)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(total)} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times F_{SW}}\right)}{I_{RIPPLE}} = \frac{36mV - \left(\frac{6A}{8 \times 250\mu F \times 600kHz}\right)}{6A} = 5.2m\Omega \quad (8)$$

Two 47-µF and one 220-µF capacitors are selected to provide more than 250 µF of minimum capacitance and 5.2 mΩ of ESR.

8.2.2.4 Peak Current Rating of Inductor

With output capacitance, it is possible to calculate the charge current during start-up and determine the minimum saturation current rating for the inductor. The start-up charging current is approximated by Equation 9.

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{T_{SS}} = \frac{1.2\ V(2 \times 47\ \mu F + 220\ \mu F)}{1.5\ ms} = 0.251\ A \quad (9)$$

$$I_{L\_PEAK} = I_{OUT(max)} + \tfrac{1}{2} I_{RIPPLE} + I_{CHARGE} = 20\ A + \tfrac{1}{2} \times 6\ A + 0.2512\ A = 23.25\ A \quad (10)$$

Table 2. Inductor Requirements

PARAMETER		VALUE	UNIT
L	Inductance	300	nH
$I_{L(rms)}$	RMS current (thermal rating)	20.07	A
$I_{L(peak)}$	Peak current (saturation rating)	23.25	A

8.2.2.5 Input Capacitor Selection (C8)

The input voltage ripple is divided between capacitance and ESR. For this design $V_{RIPPLE(cap)}$ = 150 mV and $V_{RIPPLE(esr)}$ = 150 mV. The minimum capacitance and maximum ESR are estimated by Equation 11.

$$C_{IN(min)} = \frac{I_{LOAD} \times V_{OUT}}{V_{RIPPLE(CAP)} \times V_{IN} \times F_{SW}} = \frac{20 \times 1.2V}{150mV \times 8V \times 600kHz} = 33.3uF \quad (11)$$

$$ESR_{MAX} = \frac{V_{RIPPLE(ESR)}}{I_{LOAD} + \frac{1}{2} I_{RIPPLE}} = \frac{150\ mV}{23A} = 6.5\ m\Omega \quad (12)$$

The RMS current in the input capacitors is estimated by Equation 13.

$$I_{RMS\_CIN} = I_{LOAD} \times \sqrt{D \times (1-D)} = 20\ A \times \sqrt{0.15 \times (1-0.15)} = 7.14\ Arms \quad (13)$$

Three 1210, 10-µF, 25-V, X5R ceramic capacitors are selected. Higher voltage capacitors are selected to minimize capacitance loss at the DC bias voltage to ensure the capacitors allow sufficient capacitance at the working voltage.

8.2.2.6 MOSFET Switch Selection (Q1 and Q2)

Reviewing available TI NexFET MOSFETs using the TI NexFET MOSFET selection tool, the CSD16410Q5A and CSD16321Q5 5-mm × 6-mm MOSFETs are selected.

These two FETs have maximum total gate charges of 5 nC and 10 nC, respectively.

8.2.2.7 Bootstrap Capacitor (C6)

To ensure proper charging of the high-side FET gate, limit the ripple voltage on the boost capacitor to less than 50 mV.

$$C_{Boost} = 20 \times Q_{G1} = 20 \times 5\ nC = 100\ nF \quad (14)$$

8.2.2.8 VDD Bypass Capacitor (C7)

Per this TPS40345 data sheet, select a 1-uF X5R or better ceramic bypass capacitor for VDD.

8.2.2.9 BP Bypass Capacitor (C5)

Per the TPS40345 data sheet, a minimum 1-uF ceramic capacitance is required to stabilize the BP regulator. To limit regulator noise to less than 10 mV, the value of the bypass capacitor is calculated in Equation 15.

$$C_{BP} = 100 \times MAX(Q_{G1}, Q_{G2}) \quad (15)$$

Because Q2 is larger than Q1, and the total gate charge of Q2 is 10 nC, a BP capacitor of 1 µF is calculated. A standard value of 1 µF is selected to limit noise on the BP regulator.

8.2.2.10 Short-Circuit Protection (R11)

The TPS40345 uses the negative drop across the low-side FET at the end of the OFF-time to measure the inductor current. Allowing for 30% over maximum load and 20% rise in $R_{DS(on)Q1}$ for self-heating, the voltage drop across the low-side FET at current limit is given by Equation 16.

$$V_{OC} = (1.3 \times I_{LOAD} - \frac{1}{2} I_{ripple}) \times 1.2 \times R_{DSONG2} = (1.3 \times 20\ A - \frac{1}{2}\ 6\ A) \times 1.2 \times 4.6\ m\Omega = 127\ mV \quad (16)$$

The TPS40345 internal temperature coefficient helps compensate for the MOSFET's $R_{DS(on)}$ temperature coefficient, so the current limit programming resistor is selected by Equation 17.

$$R_{CS} = \frac{V_{OC} - V_{OCLOS(min)}}{2 \times I_{OCSET(min)}} = \frac{127\ mV - (-8\ mV)}{2 \times 9.5\ \mu A} = 7.1\ k\Omega \quad (17)$$

8.2.2.11 Feedback Divider (R4, R5)

The TPS40345 controller uses a full operational amplifier with an internally fixed 0.6-V reference. R4 is selected between 10 kΩ and 50 kΩ for a balance of feedback current and noise immunity. With R4 set to 10 kΩ, The output voltage is programmed with a resistor divider given by Equation 18.

$$R7 = \frac{V_{FB} \times R4}{V_{OUT} - V_{FB}} = \frac{0.600\ V \times 10.0\ k\Omega}{1.2\ V - 0.600\ V} = 10\ k\Omega \quad (18)$$

8.2.2.12 Compensation: (C2, C3, C4, R3, R6)

Using the TPS40k Loop Stability Tool for 100-kHz bandwidth and 60° phase margin with a R4 value of 10.0 kΩ, the following values are returned.

- C4 = 680 pF
- C5 = 100 pF
- C6 = 680 pF
- R1 = 10 kΩ
- R2 = 1.5 kΩ

8.2.3 Application Curves

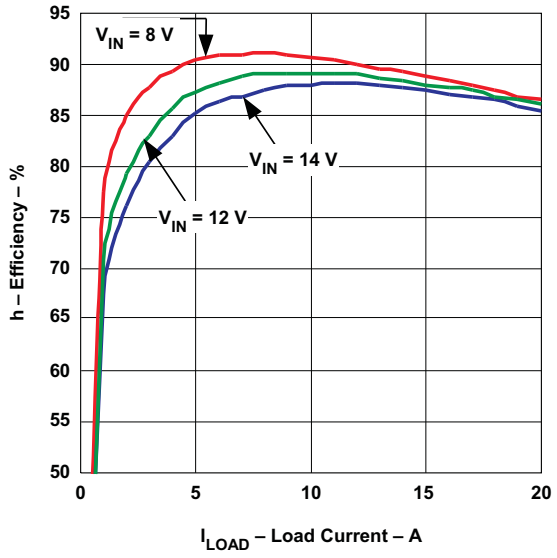


Figure 13. Efficiency vs Load Current

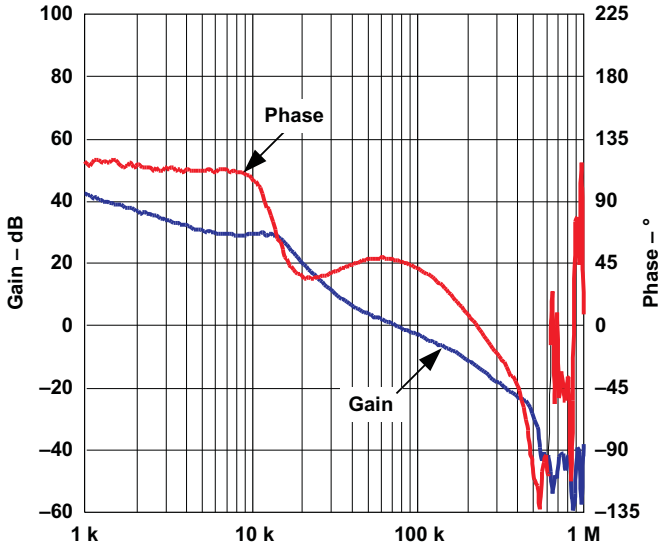


Figure 14. Gain and Phase vs Frequency

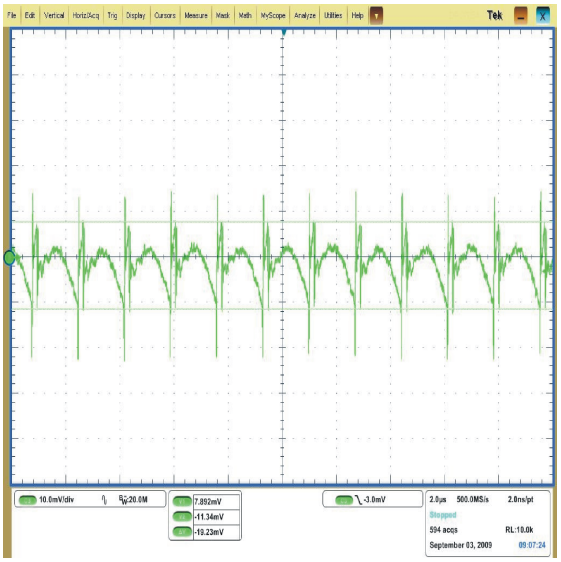


Figure 15. Output Ripple 10 mV/div, 2-µs/div, 20-MHz Bandwidth

9 Power Supply Recommendations

The TPS40345 device is designed to operate from an input voltage supply between 3 V and 20 V. This input supply must remain within the input voltage supply range. This supply must be well regulated.

10 Layout

10.1 Layout Guidelines

- For MOSFET or power block layout, follow the layout recommendations provided for the MOSFET or power block selected.
- Connect VDD to VIN as close as possible to the drain connection of the high-side FET to avoid introducing additional drop, which could trigger short-circuit protection.
- Place VDD and BP to GND capacitors within 2 mm of the device and connected to the thermal pad (GND).
- Connect the FB to GND resistor to the thermal tab (GND) with a minimum 10-mil wide trace.
- Place VOUT to FB resistor within 2 mm of the FB pin.
- Connect the EN/SS-to-GND capacitor to the thermal tab (GND) with a minimum 10-mil-wide trace. It may share this trace with FB to GND.
- If a BJT or MOSFET is used to disable EN/SS, place it within 5 mm of the device.
- If a COMP to GND resistor is used, place it within 5 mm of the device.
- All COMP and FB traces should be kept minimum line width and as short as possible to minimize noise coupling.
- EN/SS should not be routed more than 20 mm from the device.
- If multiple layers are used, extend GND under all components connected to FB, COMP and EN/SS to reduce noise sensitivity.
- HDRV and LDRV must provide short, low inductance paths of 5 mm or less to the gates of the MOSFETs or power block.
- Place no more than 1 Ω of resistance between HDRV or LDRV and their MOSFET or power block gate pins.
- LDRV / OC to GND current limit programming resistor may be placed on the far side of the MOSFET if necessary to ensure a short connection from LDRV to the gate of the low-side MOSFET.
- Place the BOOT to SW resistor and capacitor within 4 mm of the device using a minimum of 10-mil-wide trace. The full width of the component pads are preferred for trace widths if design rules allow.
- If via must be used between the HDRV, SW and LDRV pins and their respective MOSFET or power block connections, use a minimum of two vias to reduce parasitic inductance
- Refer to the land pattern data for the preferred layout of thermal vias within the thermal pad.
- TI recommends extending the top-layer copper area of the thermal pad (GND) beyond the package a minimum 3 mm between pins 1 and 10 and 5 and 6 to improve thermal resistance to ambient of the device.

10.2 Layout Example

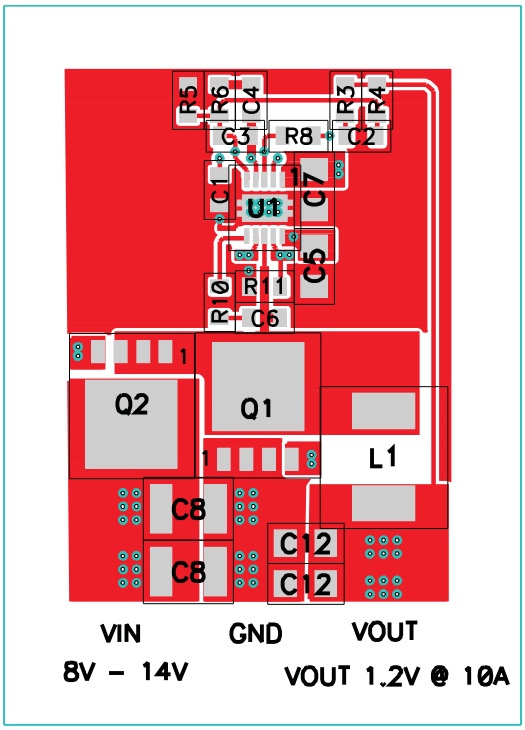


Figure 16. Top Copper With Components

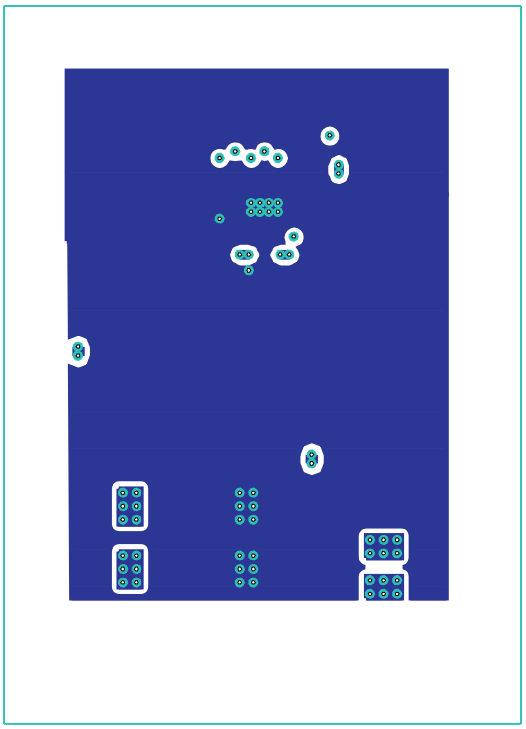


Figure 17. Top Internal Copper Layout

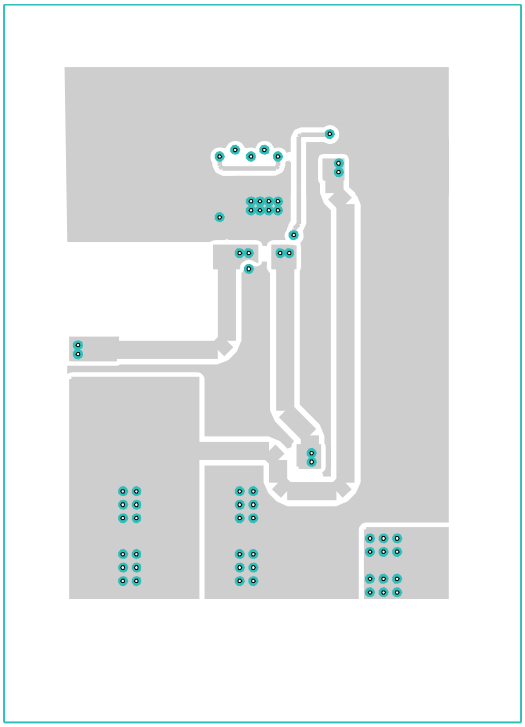


Figure 18. Bottom Internal Copper Layout

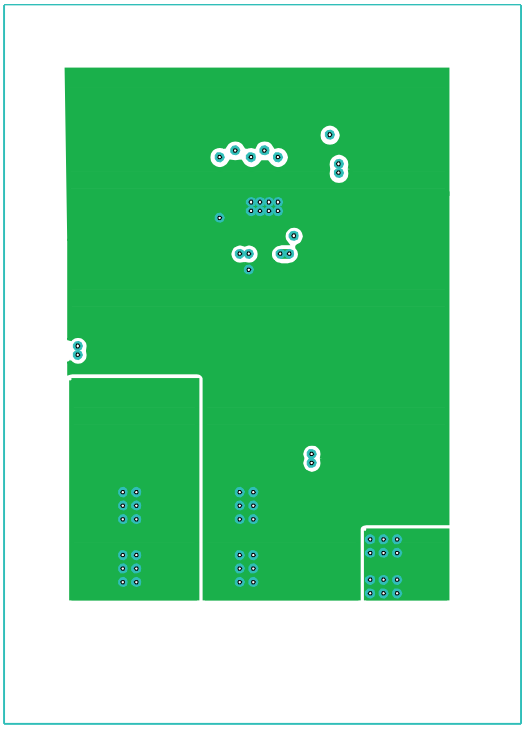


Figure 19. Bottom Copper Layer

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

These references, design tools and links to additional references, including design software, may be found at http://power.ti.com

1. Additional PowerPAD™ information may be found in Applications Briefs (SLMA002) and (SLMA004).
2. *Understanding Buck Power Stages in Switchmode Power Supplies*
3. *Under The Hood Of Low Voltage DC/DC Converters* – SEM1500 Topic 5 – 2002 Seminar Series
4. *Designing Stable Control Loops* – SEM 1400 – 2001 Seminar Series

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS40345DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-20 to 85	0345
TPS40345DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-20 to 85	0345
TPS40345DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-20 to 85	0345
TPS40345DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-20 to 85	0345

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

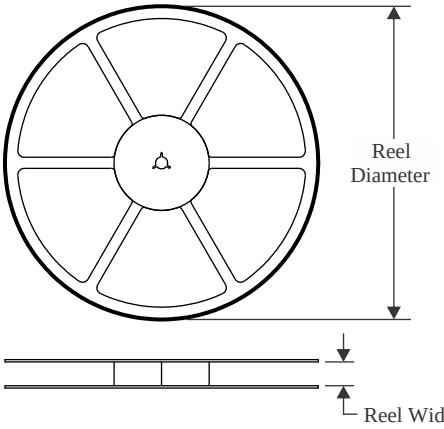
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

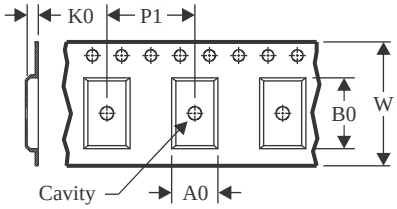
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

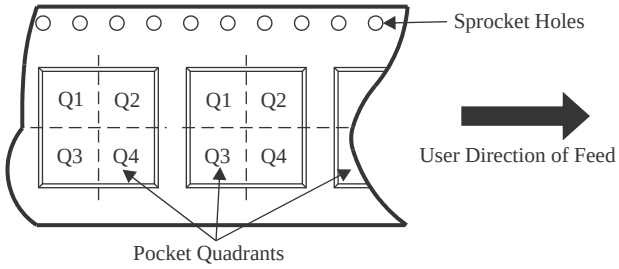


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

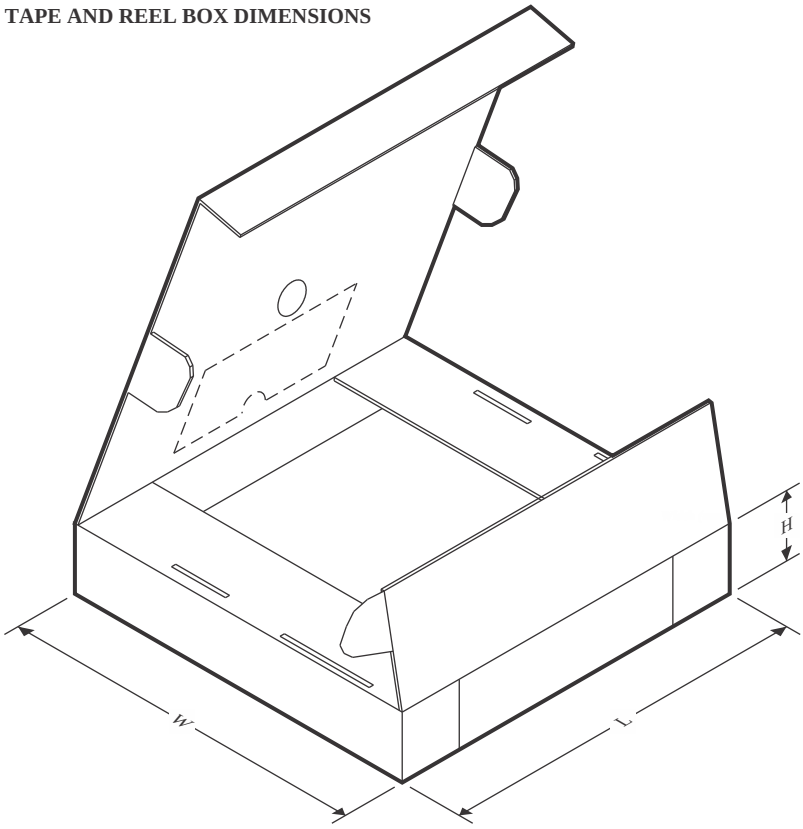
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40345DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40345DRCT	VSON	DRC	10	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40345DRCR	VSON	DRC	10	3000	338.0	355.0	35.0
TPS40345DRCT	VSON	DRC	10	250	205.0	200.0	33.0

GENERIC PACKAGE VIEW

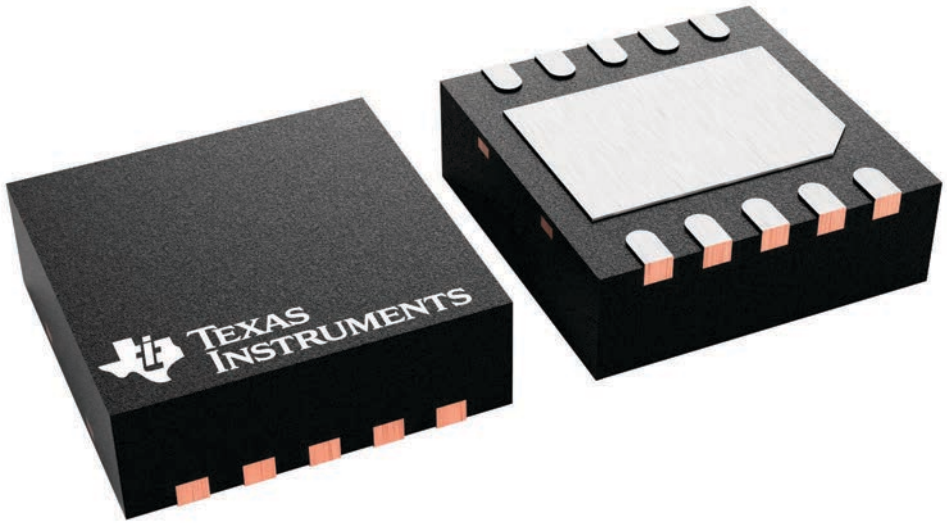
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



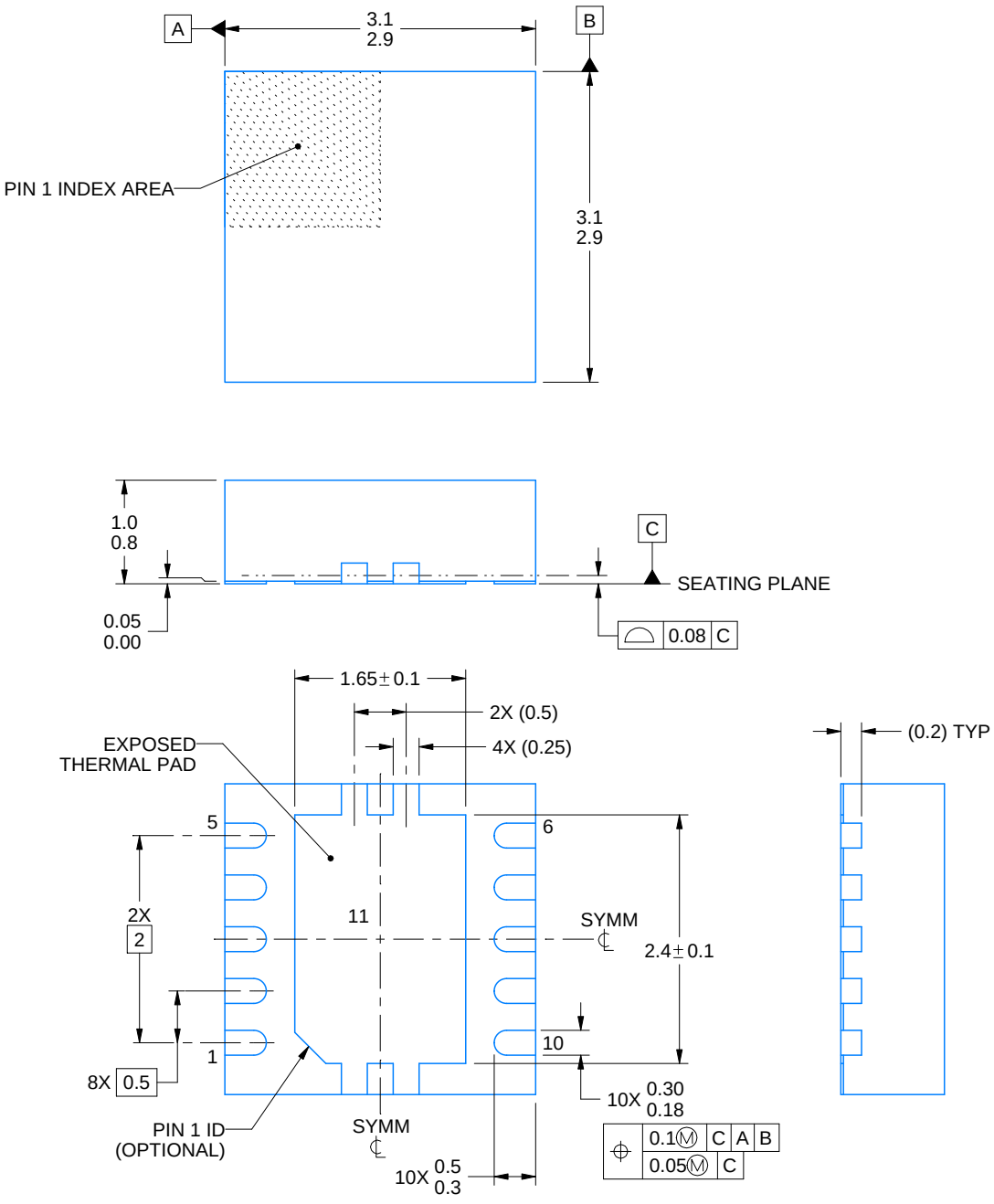
4226193/A

DRC0010J

PACKAGE OUTLINE

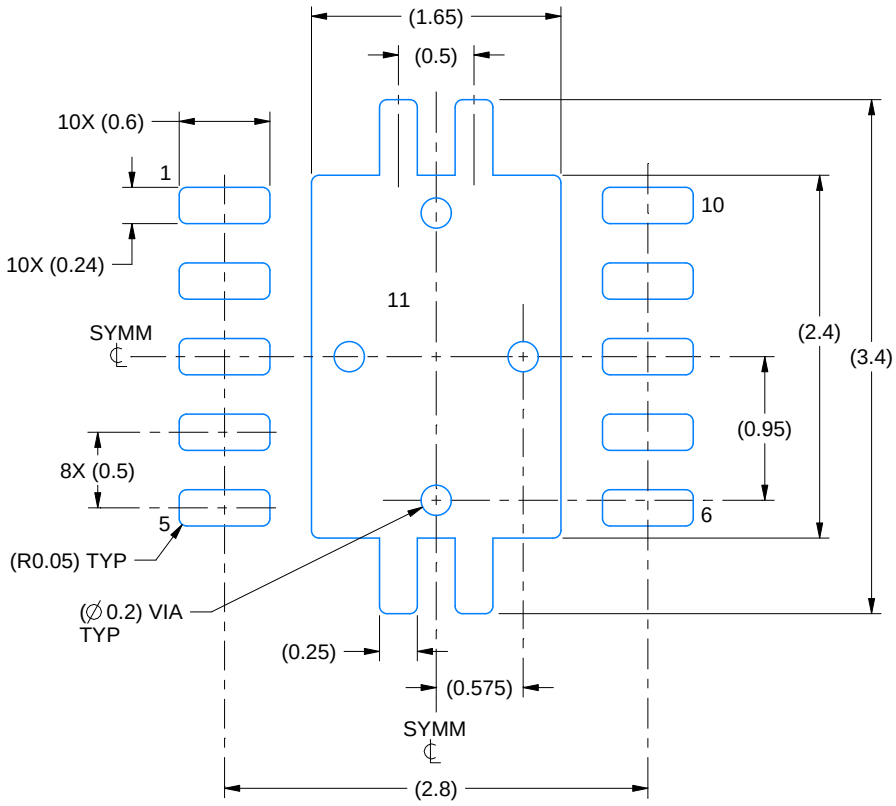
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

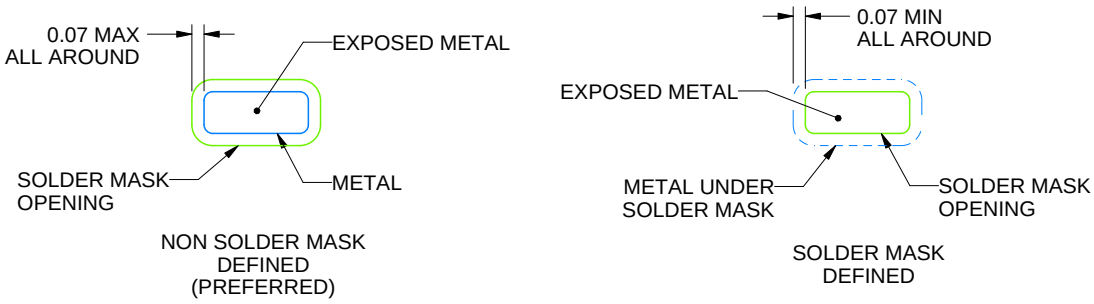


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

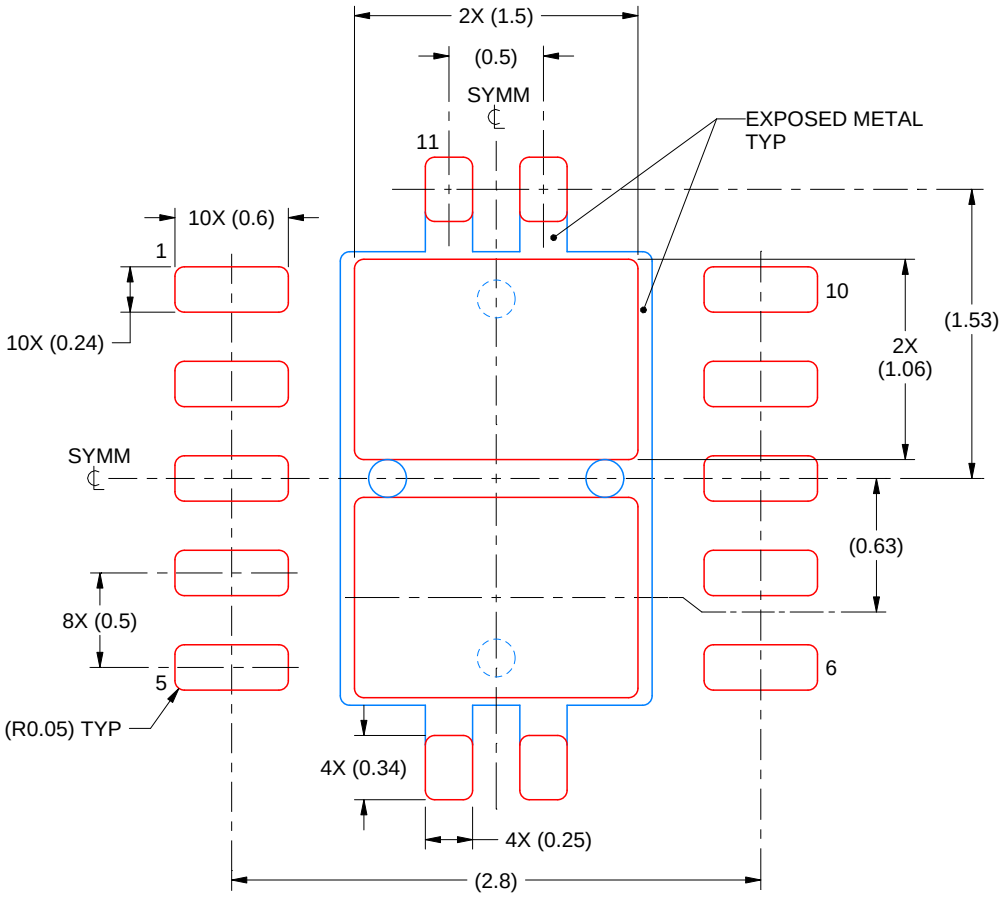
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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