

# TPS4811Q1 100V Automotive Smart High-Side Driver With Protection and Diagnostics

## 1 Features

- AEC-Q100 qualified with the following results
  - Device temperature grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ambient operating temperature range
- [Functional Safety-Capable](#)
  - [Documentation available to aid functional safety system design](#)
- 3.5V to 80V input range (100V absolute maximum)
- Output reverse polarity protection down to  $-30\text{V}$
- Integrated 12V charge pump with 100 $\mu\text{A}$  capacity
- Low 1.6 $\mu\text{A}$  shutdown current (EN/UVLO = Low)
- Strong pull up (3.7A) and pull down (4A) gate driver
- Drives external back-to-back N-channel MOSFETs
- Variant with integrated pre-charge switch driver (TPS48111Q1) to drive capacitive loads
- Two-level adjustable overcurrent protection (IWRN, ISCP) with adjustable circuit breaker timer (TMR) and fault flag output ( $\overline{\text{FLT\_I}}$ )
- Fast short-circuit protection: 1.2 $\mu\text{s}$  (TPS48111Q1), 4 $\mu\text{s}$  (TPS48110Q1)
- Accurate analog current monitor output (IMON):  $\pm 2\%$  at 30mV  $V_{\text{SNS}}$
- Accurate, adjustable undervoltage lockout (UVLO) and overvoltage protection (OV):  $< \pm 2\%$
- Remote overtemperature sensing (DIODE) and protection with fault flag output ( $\overline{\text{FLT\_T}}$ )

## 2 Applications

- [Power distribution box](#)
- [Body control module](#)
- [DC/DC converter](#)
- [Battery management system](#)

## 3 Description

The TPS4811x-Q1 family is a 100V smart high side driver with protection and diagnostics. With wide operating voltage range from 3.5V to 80V, the device is an excellent choice for 12V, 24V, and 48V system designs.

The device has a strong 3.7A peak source (PU) and 4A peak sink (PD) GATE driver that enables power switching using parallel FETs in high current system designs. Use INP as the gate driver control input.

The device has accurate current sensing ( $\pm 2\%$ ) output (IMON) enabling system designs for energy management. The device has integrated two-level overcurrent protection with  $\overline{\text{FLT\_I}}$  output with complete adjustability of thresholds and response times. Auto-retry and latch-off fault behavior can be configured. The device features remote overtemperature protection with  $\overline{\text{FLT\_T}}$  output.

The TPS48111Q1 integrates a pre-charge driver (G) with control input (INP\_G). This features enables designs that must drive large capacitive loads. In shutdown mode, the controller draws a total shutdown current of 1.6 $\mu\text{A}$  at 48V supply input.

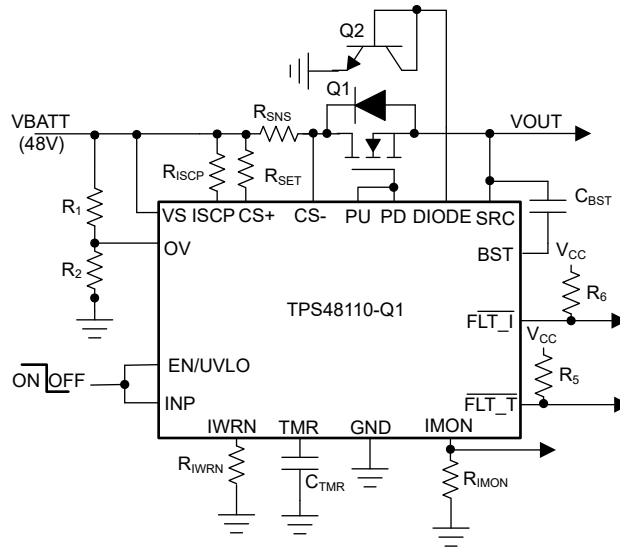
The TPS4811x-Q1 is available in a 19-pin VSSOP package with a pin removed between adjacent high voltage and low voltage pins, providing 0.8mm clearance.

### Package Information

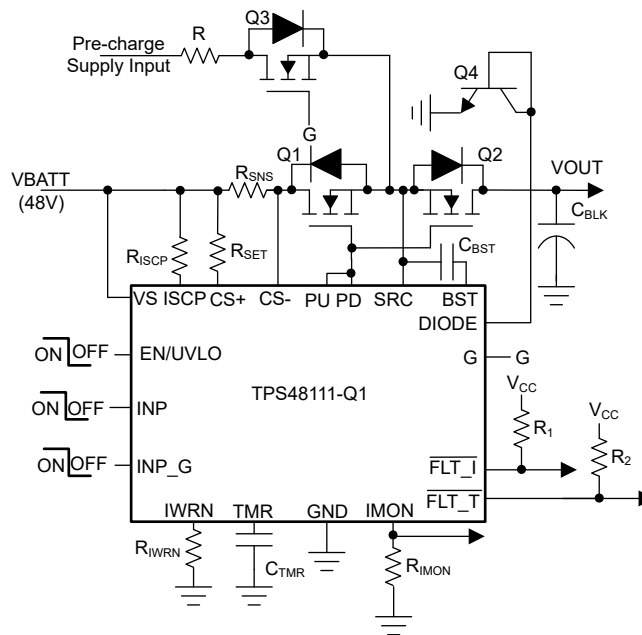
PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TPS48110Q1	DGX (VSSOP, 19)	5.10mm × 3.00mm
TPS48111Q1		

- (1) For all available packages, see the orderable addendum at the end of the datasheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.





**Smart High Side Driver for Heater Loads**



**Circuit Breaker for DC-DC Converter**

## Table of Contents

<b>1</b>	<b>Features</b> .....	<b>1</b>		<b>9</b>	<b>Application and Implementation</b> .....	<b>29</b>
<b>2</b>	<b>Applications</b> .....	<b>1</b>		9.1	Application Information.....	29
<b>3</b>	<b>Description</b> .....	<b>1</b>		9.2	Typical Application: Driving HVAC PTC Heater Load on KL40 Line in Power Distribution Unit.....	29
<b>4</b>	<b>Device Comparison Table</b> .....	<b>4</b>		9.3	Typical Application: Driving B2B FETs With Pre- Charging the Output Capacitance.....	35
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>5</b>		9.4	Typical Application: Designing for EMI.....	37
<b>6</b>	<b>Specifications</b> .....	<b>7</b>		9.5	Power Supply and EMI Recommendations.....	38
6.1	Absolute Maximum Ratings.....	7		9.6	Layout.....	39
6.2	Recommended Operating Conditions.....	7		<b>10</b>	<b>Device and Documentation Support</b> .....	<b>42</b>
6.3	ESD Ratings.....	7		10.1	Receiving Notification of Documentation Updates.....	42
6.4	Thermal Information.....	8		10.2	Support Resources.....	42
6.5	Electrical Characteristics.....	8		10.3	Trademarks.....	42
6.6	Switching Characteristics.....	10		10.4	Electrostatic Discharge Caution.....	42
6.7	Typical Characteristics.....	11		10.5	Glossary.....	42
<b>7</b>	<b>Parameter Measurement Information</b> .....	<b>14</b>		<b>11</b>	<b>Revision History</b> .....	<b>42</b>
<b>8</b>	<b>Detailed Description</b> .....	<b>16</b>		<b>12</b>	<b>Mechanical, Packaging, and Orderable Information</b> .....	<b>43</b>
8.1	Overview.....	16				
8.2	Functional Block Diagram.....	16				
8.3	Feature Description.....	17				
8.4	Device Functional Mode (Shutdown Mode).....	28				

## 4 Device Comparison Table

	TPS48110Q1	TPS48111Q1
Overvoltage protection	Yes	No
Pre-charge driver	No	Yes
Short-circuit protection response time	4 $\mu$ s	1.2 $\mu$ s
Overtemperature fault response	Auto-retry with fixed 512ms timer	Latch-off

## 5 Pin Configuration and Functions

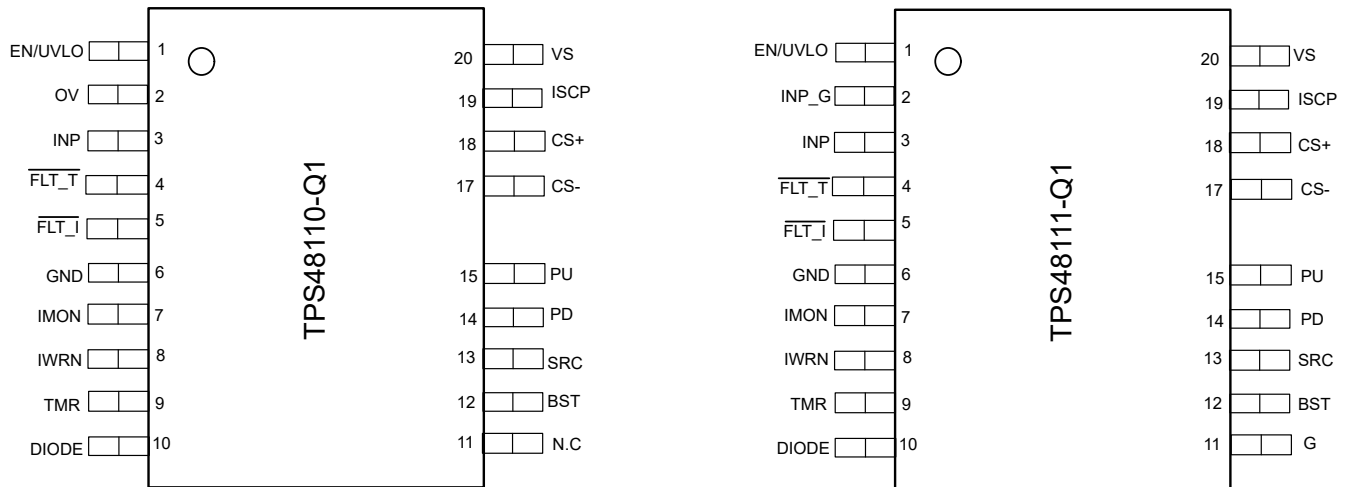


Figure 5-1. DGX Package, 19-Pin VSSOP (Top View)

Table 5-1. Pin Functions

NAME	PIN		TYPE <sup>(1)</sup>	DESCRIPTION
	TPS48110Q1	TPS48111Q1		
	DGX-19 (VSSOP)			
EN/UVLO	1	1	I	EN/UVLO input. A voltage on this pin above 1V enables normal operation. Forcing this pin below 0.3V shuts down the TPS4811x-Q1, reducing quiescent current to approximately 1.6µA (typical). Optionally connect to the input supply through a resistive divider to set the undervoltage lockout. When EN/UVLO is left floating an internal pull down of 60nA pulls EN/UVLO low and keeps the device in OFF state.
OV	2	—	I	Adjustable overvoltage threshold input. Connect a resistor ladder from input supply, OV to GND. When the voltage at OV exceeds the overvoltage cut-off threshold then the PD is pulled down to SRC turning OFF the external FET. When the voltage at OV goes below OV falling threshold then PU gets pulled up to BST, turning ON the external FET. OV must be connected to GND when not used. When OV is left floating an internal pull down of 60nA pulls OV low and keeps PU pulled up to BST.
INP_G	—	2	I	Input Signal. CMOS compatible input reference to GND that sets the state of G pin. INP_G has an internal pull-down to GND to keep G pulled to SRC when INP_G is left floating. Connect INP_G to GND if the G drive functionality is unused.
INP	3	3	I	Input Signal. CMOS compatible input reference to GND that sets the state of PD and PU pins. INP has an internal pull-down to GND to keep PD pulled to SRC when INP is left floating.
FLT_T	4	4	O	Open Drain Fault Output. This pin asserts low when overtemperature fault is detected.
FLT_I	5	5	O	Open Drain Fault Output. This pin asserts low after the voltage on the TMR pin has reached the fault threshold of 1.1V. This pin indicates the pass transistor is about to turn off due to an overcurrent condition. The FLT_I pin does not go to a high-impedance state until the overcurrent condition and the auto-retry time expire.
GND	6	6	G	Connect GND to system ground.

**Table 5-1. Pin Functions (continued)**

NAME	PIN		TYPE <sup>(1)</sup>	DESCRIPTION
	TPS48110Q1	TPS48111Q1		
	DGX-19 (VSSOP)			
IMON	7	7	O	Analog current monitor output. This pin sources a scaled down ratio of current through the external current sense resistor $R_{SNS}$ . A resistor from this pin to GND converts current proportional to voltage. If unused, connect the pin to GND.
IWRN	8	8	I	Overcurrent detection setting. A resistor across IWRN to GND sets the over current comparator threshold. Connect IWRN to GND if overcurrent protection feature is not desired.
TMR	9	9	I	Fault Timer Input. A capacitor across TMR pin to GND sets the time for fault warning, fault turn-off (FLT_I) and retry periods. Leave it open for fastest setting. Connect TMR to GND to disable overcurrent protection.
DIODE	10	10	I	Diode connection for temperature sensing. Connect this pin to base and collector of an MMBT3904 NPN BJT. Connect DIODE to GND, if remote overtemperature protection feature is not desired.
G	—	11	O	GATE of external pre-charge FET. Connect to the GATE of the external FET. Leave the G pin floating if the G drive functionality is unused.
N.C	11	—	—	No connect.
BST	12	12	O	High Side Bootstrapped Supply. An external capacitor with a minimum value of $> Q_{g(tot)}$ of the external FET must be connected between this pin and SRC.
SRC	13	13	O	Source connection of the external FET.
PD	14	14	O	High Current Gate Driver Pull-Down. This pin pulls down to SRC. For the fastest turn-off, tie this pin directly to the gate of the external high side MOSFET.
PU	15	15	O	High Current Gate Driver Pull-Up. This pin pulls up to BST. Connect this pin to PD for maximum gate drive transition speed. A resistor can be connected between this pin and the gate of the external MOSFET to control the in-rush current during turn-on.
CS-	17	17	I	Current sense negative input.
CS+	18	18	I	Current sense positive input. Connect a 50 - 100 $\Omega$ resistor across CS+ to the external current sense resistor.
ISCP	19	19	I	Short-circuit detection threshold setting. Connect ISCP to CS- if short-circuit protection is not desired.
VS	20	20	Power	Supply pin of the controller.

(1) I = input, O = output, I/O = input and output, P = power, G = Ground

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input Pins	VS, CS+, CS–, ISCP to GND	–1	100	V
	VS, CS+, CS– to SRC	–60	100	
	SRC to GND	–30	100	
	PU, PD, G, BST to SRC	–0.3	16	
	TMR, IWRN, DIODE to GND	–0.3	5.5	
	OV, EN/UVLO, INP, INP_G, FLT_I, FLT_T to GND	–1	20	
	CS+ to CS–	–0.3	0.3	
	$I_{(FLT\_I)}$ , $I_{(FLT\_T)}$		10	mA
	$I_{(CS+)}$ to $I_{(CS-)}$ , 1msec	–100	100	
	Voltage slew rate on drain side input pins (VS, CS+, CS–, ISCP)			60
Output Pins	PU, PD, G, BST to GND	–30	112	V
	IMON to GND	–1	7.5	
Operating junction temperature, $T_j$ <sup>(2)</sup>		–40	150	°C
Storage temperature, $T_{stg}$		–55	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

### 6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
Input Pins	VS, CS+, CS– to GND	0		80	V
	EN/UVLO, OV to GND	0		15	
Output Pins	FLT_I, FLT_T to GND	0		15	
	IMON to GND	0		5	
External Capacitor	VS to GND	22			nF
	BST to SRC	0.1			$\mu$ F
$T_j$	Operating Junction temperature <sup>(2)</sup>	–40		150	°C

- (1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

### 6.3 ESD Ratings

			VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	$\pm 2000$	V	
		Charged device model (CDM), per AEC Q100-011	Corner pins (EN/UVLO, DIODE, G, VS)		$\pm 750$
			Other pins		$\pm 500$

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS4811x-Q1		UNIT
		DGX		
		19 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87		°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.5		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.7		°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.5		°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	43.3		°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

## 6.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical values at  $T_J = 25^{\circ}\text{C}$ ,  $V_{(VS)} = V_{(CS+)} = V_{(CS-)} = 48\text{V}$ ,  $V_{(BST-SRC)} = 12\text{V}$ ,  $V_{(SRC)} = 0\text{V}$ ,  $V_{SNS} =$  Voltage across  $R_{SNS}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY VOLTAGE</b>						
$V_{(VS)}$	Operating input voltage		3.5		80	V
$V_{(VS\_PORR)}$	VS POR threshold, rising		2.75	3	3.2	V
$V_{(VS\_PORF)}$	VS POR threshold, falling		2.65	2.9	3.1	V
$I_{(Q)}$	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)} = 2\text{V}$		613	700	$\mu\text{A}$
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN/UVLO)} = 0\text{V}$ , $V_{(SRC)} = 0\text{V}$		1.6	5.36	$\mu\text{A}$
		$V_{(EN/UVLO)} = 0\text{V}$ , $V_{(SRC)} = 0\text{V}$ , $-40^{\circ}\text{C} < T_J < 85^{\circ}\text{C}$		1.6	2.65	$\mu\text{A}$
<b>ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT</b>						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.16	1.18	1.2	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		1.1	1.11	1.13	V
$V_{(ENF)}$	Enable threshold voltage for low IQ shutdown, falling		0.3	0.7	0.9	V
	Enable Hysteresis			43	60	mV
$I_{(EN/UVLO)}$	Enable input leakage current	$V_{(EN/UVLO)} = 12\text{V}$		61	320	nA
<b>OVER VOLTAGE PROTECTION (OV) INPUT - TPS48110-Q1 Only</b>						
$V_{(OVR)}$	Overvoltage threshold input, rising	TPS48110-Q1 Only	1.16	1.18	1.2	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.1	1.11	1.13	V
$I_{(OV)}$	OV Input leakage current	$0\text{V} < V_{(OV)} < 5\text{V}$		60	300	nA
<b>CHARGE PUMP (BST-SRC)</b>						
$I_{(BST)}$	Charge Pump Supply current	$V_{(BST-SRC)} = 10\text{V}$	80	100	126	$\mu\text{A}$
$V_{(BST-SRC)}$	Charge Pump Turn ON voltage		11	11.7	12.3	V
	Charge Pump Turn OFF voltage		11.6	12.3	13	V
$V_{(BST\_UVLOR)}$	$V_{(BST-SRC)}$ UVLO voltage threshold, rising		7	7.6	8.1	V
$V_{(BST\_UVLOF)}$	$V_{(BST-SRC)}$ UVLO voltage threshold, falling		6	6.5	6.9	V
$V_{(BST-SRC)}$	Charge Pump Voltage at $V_{(VS)} = 3.5\text{V}$		8.6			V
<b>GATE DRIVER OUTPUTS (PU, PD, G)</b>						
$R_{(PD)}$	Pull-Down Resistance			0.69	1.34	$\Omega$
$I_{(PU)}$	Peak Source Current			3.75		A
$I_{(PD)}$	Peak Sink Current			4		A

## 6.5 Electrical Characteristics (continued)

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical values at  $T_J = 25^{\circ}\text{C}$ ,  $V_{(VS)} = V_{(CS+)} = V_{(CS-)} = 48\text{V}$ ,  $V_{(BST-SRC)} = 12\text{V}$ ,  $V_{(SRC)} = 0\text{V}$ ,  $V_{SNS} =$  Voltage across  $R_{SNS}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(G)}$	Gate charge (sourcing) current, on state	TPS48111-Q1 Only	72	100	140	$\mu\text{A}$
	Gate discharge (sinking) current, off state		92	131	190	$\text{mA}$
<b>CURRENT SENSE AND OVER CURRENT PROTECTION (CS+, CS-, IMON, ISCP, IWRN)</b>						
$V_{(OS\_SET)}$	Input referred offset ( $V_{SNS}$ to $V_{(IMON)}$ scaling)	$R_{SET} = 100\ \Omega$ , $R_{IMON} = 5\text{k}\Omega$ , $10\text{k}\Omega$ (corresponds to $V_{SNS} = 6\text{mV}$ to $30\text{mV}$ ) Gain of 45 and 90 respectively.	-200		200	$\mu\text{V}$
$V_{(GE\_SET)}$	Gain error ( $V_{SNS}$ to $V_{(IMON)}$ scaling)		-1.27		1.27	%
$V_{(IMON\_Acc)}$	IMON accuracy	$V_{SNS} = 30\text{mV}$ , $R_{SET} = 100\ \Omega$ , $R_{IMON} = 10\text{k}\Omega$	-2		2	%
		$V_{SNS} = 6\text{mV}$ , $R_{SET} = 100\ \Omega$ , $R_{IMON} = 5\text{k}\Omega$	-5		5	%
$V_{(SNS\_WRN)}$	Overcurrent protection (OCP) voltage threshold	$R_{SET} = 100\ \Omega$ , $R_{IWRN} = 39.7\text{k}\Omega$	29.2	30.6	31.5	$\text{mV}$
		$R_{SET} = 100\ \Omega$ , $R_{IWRN} = 120\text{k}\Omega$	8	10	12	$\text{mV}$
$I_{(ISCP)}$	SCP Input Bias current		13.7	15.6	17.6	$\mu\text{A}$
$V_{(SNS\_SCP)}$	Short-circuit protection (SCP) voltage threshold	$R_{ISCP} = 2.1\text{k}\Omega$	35	40	45	$\text{mV}$
		$R_{ISCP} = 750\ \Omega$		19		$\text{mV}$
$I_{(CS-)}$	CS- Input Bias current		160	183	200	$\mu\text{A}$
<b>DELAY TIMER (TMR)</b>						
$I_{(TMR\_SRC\_CB)}$	TMR source current		73	82	91	$\mu\text{A}$
$I_{(TMR\_SRC\_FLT)}$	TMR source current		2.1	2.5	3.3	$\mu\text{A}$
$I_{(TMR\_SNK)}$	TMR sink current		2.1	2.5	3	$\mu\text{A}$
$V_{(TMR\_OC)}$	TMR voltage threshold for over current shutdown		1.112	1.2	1.3	$\text{V}$
$V_{(TMR\_FLT)}$	TMR voltage threshold for FLT_T assertion		1.03	1.1	1.2	$\text{V}$
$V_{(TMR\_LOW)}$	Voltage at TMR pin for AR counter falling threshold		0.15	0.2	0.22	$\text{V}$
<b>INPUT CONTROLS (INP, INP_G), FAULT FLAGS (FLT_I, FLT_T)</b>						
$R_{(FLT\_I)}$	FLT_I Pull-down resistance		54	70	90	$\Omega$
$R_{(FLT\_T)}$	FLT_T Pull-down resistance			70		$\Omega$
$I_{(FLT\_T)}$	FLT Input leakage current				400	$\text{nA}$
$V_{(INP\_H)}$				1.6	2	$\text{V}$
$V_{(INP\_L)}$			0.8	1.2		$\text{V}$
$V_{(INP\_Hys)}$				400		$\text{mV}$
$V_{(INP\_G\_H)}$				1.6	2	$\text{V}$
$V_{(INP\_G\_L)}$		TPS48111-Q1 Only	0.8	1.2		$\text{V}$
$V_{(INP\_G\_Hys)}$				400		$\text{mV}$
<b>TEMPERATURE SENSING AND PROTECTION (DIODE)</b>						
$I_{(DIODE)}$	External diode current source	High level		160		$\mu\text{A}$
		Low level		10		$\mu\text{A}$
	Diode current ratio		15.4	16	16.6	A/A
$T_{(DIODE\_TSD\_rising)}$	DIODE sense TSD rising threshold	With MMBT3904 BJT for sensing	140	150	160	$^{\circ}\text{C}$

## 6.6 Switching Characteristics

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical values at  $T_J = 25^{\circ}\text{C}$ ,  $V_{(VS)} = V_{(CS+)} = V_{(CS-)} = 48\text{V}$ ,  $V_{(BST-SRC)} = 12\text{V}$ ,  $V_{(SRC)} = 0\text{V}$ ,  $V_{SNS} =$  Voltage across  $R_{SNS}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PU(INP\_H)}$	INP Turn ON propagation Delay	INP $\uparrow$ to PU $\uparrow$ , $C_L = 47\text{nF}$		1	2	$\mu\text{s}$
$t_{PD(INP\_L)}$	INP Turn OFF propagation Delay	INP $\downarrow$ to PD $\downarrow$ , $C_L = 47\text{nF}$			1	$\mu\text{s}$
$t_{G(INP\_G\_H)}$	INP_G Turn ON propagation Delay	INP_G $\uparrow$ to G $\uparrow$ , $C_L = 1\text{nF}$		21		$\mu\text{s}$
$t_{G(INP\_G\_L)}$	INP_G Turn OFF propagation Delay	INP_G $\downarrow$ to G $\downarrow$ , $C_L = 1\text{nF}$		0.55	0.8	$\mu\text{s}$
$t_{PD(EN\_OFF)}$	EN Turn OFF Propagation Delay	EN $\downarrow$ to PD $\downarrow$ , $C_L = 47\text{nF}$		3.2	5	$\mu\text{s}$
$t_{PD(UVLO\_OFF)}$	UVLO Turn OFF Propagation Delay	UVLO $\downarrow$ to PD $\downarrow$ , $C_L = 47\text{nF}$		3.5	6	$\mu\text{s}$
$t_{PD(VS\_OFF)}$	PD Turn OFF delay during input supply (VS) interruption	VS $\downarrow$ $V_{(VS\_PORF)}$ to PD $\downarrow$ , $C_L = 47\text{nF}$ , INP = EN/UVLO = 2V		54		$\mu\text{s}$
$t_{PU(VS\_ON)}$	PU Turn ON delay during input supply (VS) recovery	VS $\uparrow$ $V_{(VS\_PORR)}$ to PU $\uparrow$ , $C_L = 47\text{nF}$ , INP = EN/UVLO = 2V, $V_{(BST-SRC)} >$ $V_{(BST\_UVLOR)}$		328	465	$\mu\text{s}$
$t_{PD(OV\_OFF)}$	OV Turn Off propagation Delay	OV $\uparrow$ to PD $\downarrow$ , $C_L = 47\text{nF}$		2.6	4	$\mu\text{s}$
$t_{SC}$	Short-circuit protection propagation Delay	$(V_{CS+} - V_{CS-}) \uparrow V_{(SNS\_SCP)}$ to PD $\downarrow$ , $C_L = 47\text{nF}$ , TPS48111-Q1 Only		1.16	1.6	$\mu\text{s}$
	Short-circuit protection propagation Delay	$(V_{CS+} - V_{CS-}) \uparrow V_{(SNS\_SCP)}$ to PD $\downarrow$ , $C_L = 47\text{nF}$ , TPS48110-Q1 Only		4	5	$\mu\text{s}$
$t_{OC}$	Over current protection delay	$(V_{CS+} - V_{CS-}) \uparrow V_{(SNS\_WRN)}$ to PD $\downarrow$ , $C_L = 47\text{nF}$ , $C_{TMR} = 0\text{nF}$		25	30	$\mu\text{s}$
	Over current protection delay	$(V_{CS+} - V_{CS-}) \uparrow V_{(SNS\_WRN)}$ to PD $\downarrow$ , $C_L = 47\text{nF}$ , $C_{TMR} = 22\text{nF}$		370		$\mu\text{s}$
$t_{(FLT\_I\_ASSERT)}$	FLT_I assertion delay	$C_{TMR} = 22\text{nF}$		340		$\mu\text{s}$
$t_{(FLT\_I\_DEASSERT)}$	FLT_I de-assertion delay			260		$\mu\text{s}$
$t_{(FLT\_T)AR}$	TSD Auto-retry	TPS48110-Q1 Only		512		msec

## 6.7 Typical Characteristics

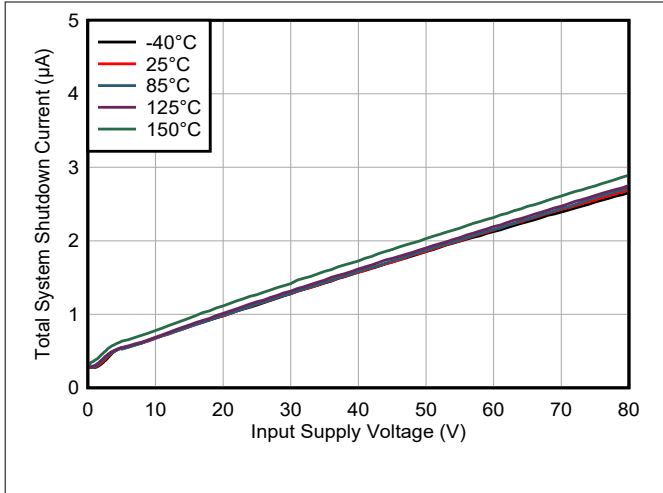


Figure 6-1. Shutdown Supply Current vs Supply Voltage

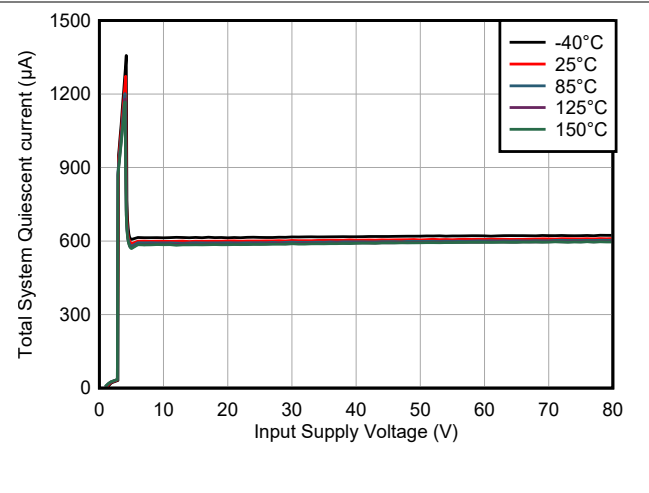


Figure 6-2. Operating Quiescent Current vs Supply Voltage

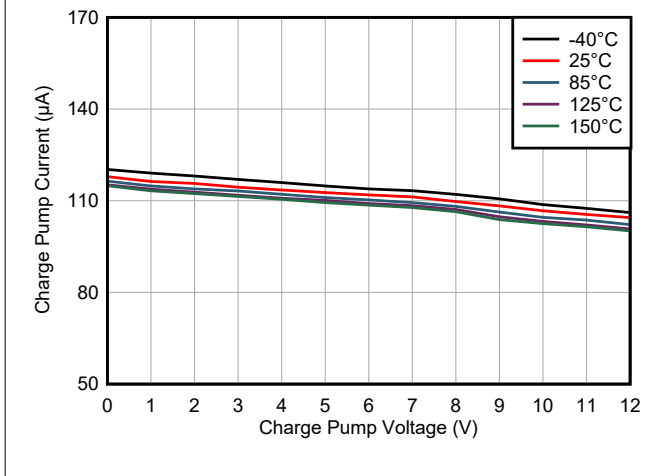


Figure 6-3. Charge Pump Current vs Charge Pump Voltage

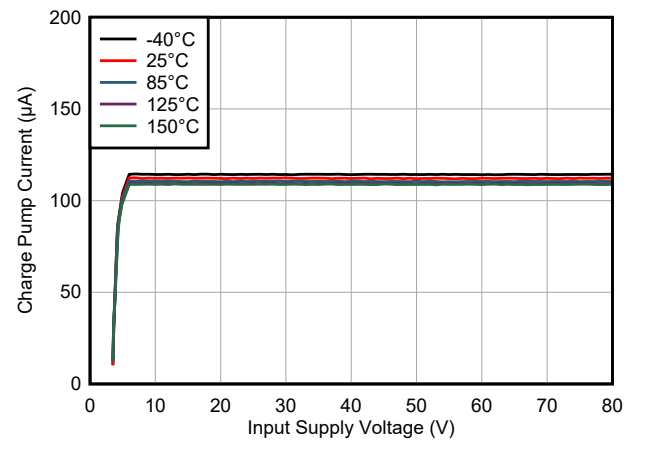


Figure 6-4. Charge Pump Current vs Input Supply Voltage

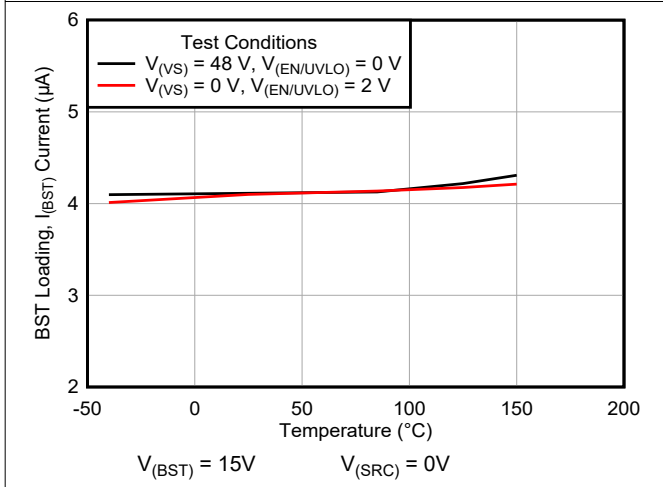


Figure 6-5. BST Loading Current ( $I_{BST}$ ) vs Temperature

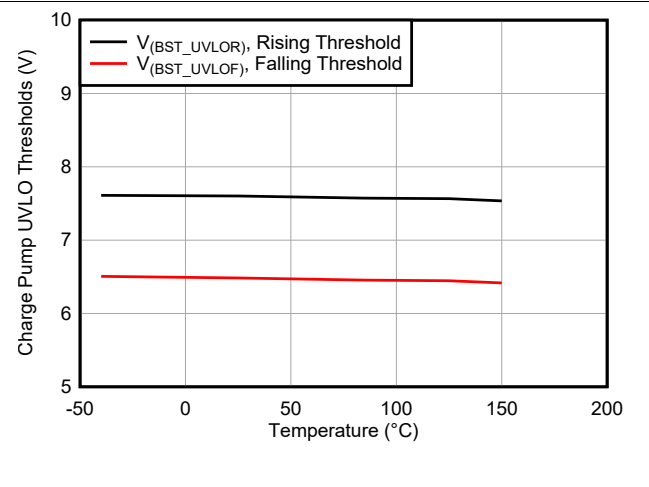


Figure 6-6. Charge Pump UVLO Thresholds vs Temperature

### 6.7 Typical Characteristics (continued)

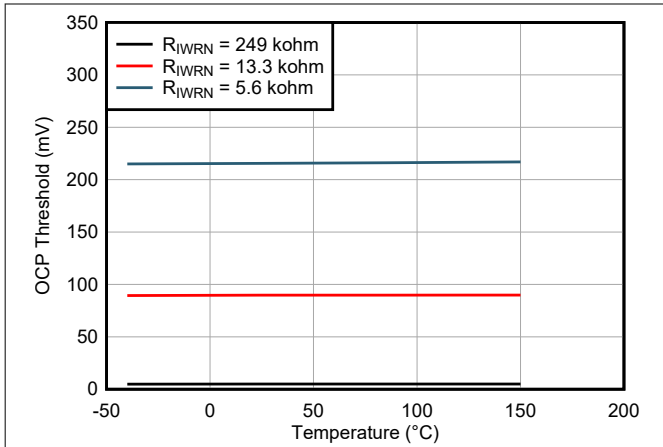


Figure 6-7. Overcurrent Threshold ( $V_{(SNS\_WRN)}$ ) vs Temperature

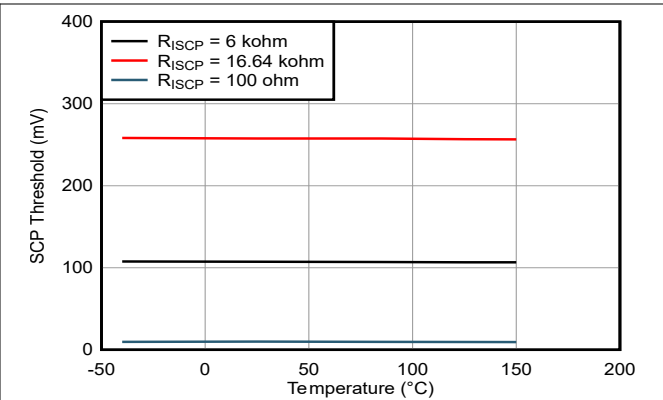


Figure 6-8. Short-Circuit Threshold ( $V_{(SNS\_SCP)}$ ) vs Temperature

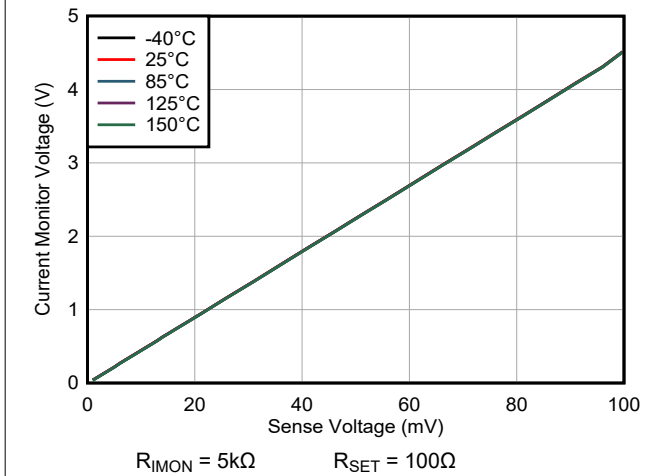


Figure 6-9. Current Monitor Output ( $V_{(IMON)}$ ) vs Sense Voltage ( $V_{(SNS)}$ )

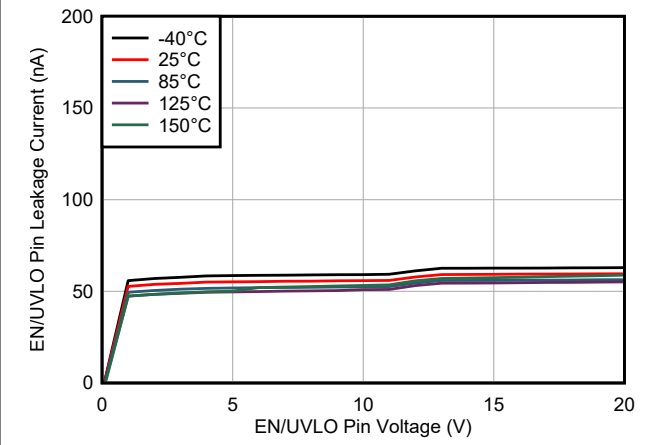


Figure 6-10. EN/UVLO Pin Voltage vs Current

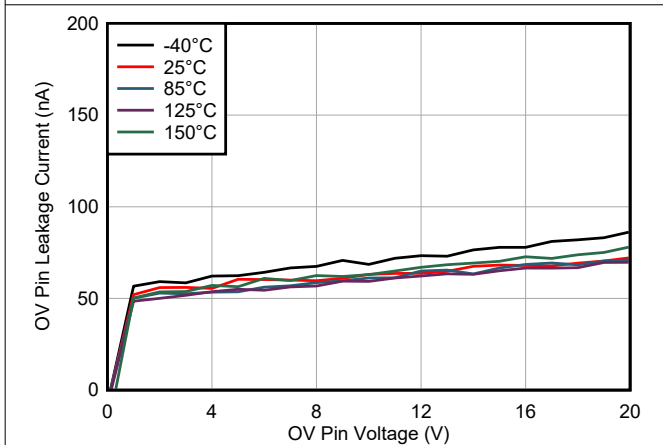


Figure 6-11. OV Pin Voltage vs Leakage Current

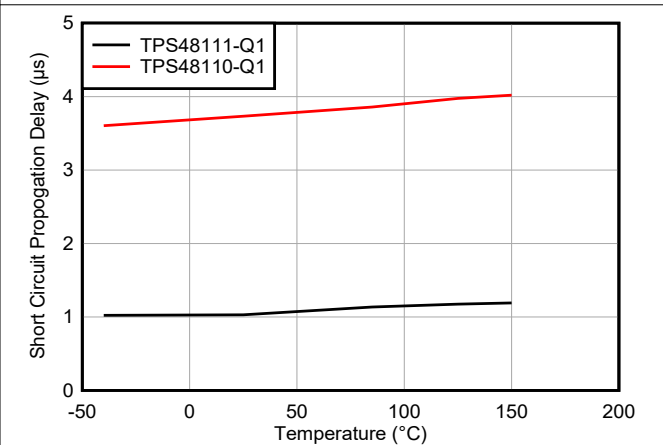
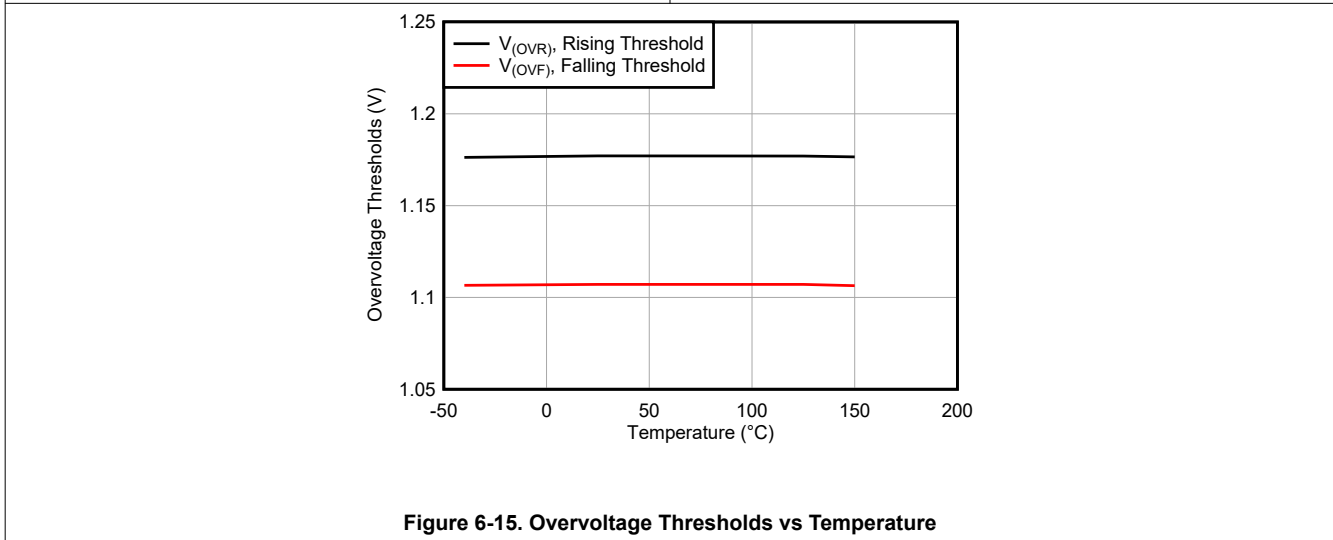
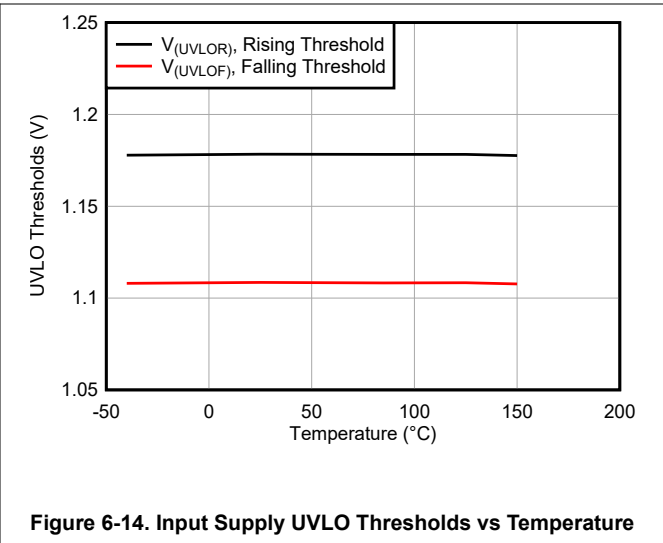
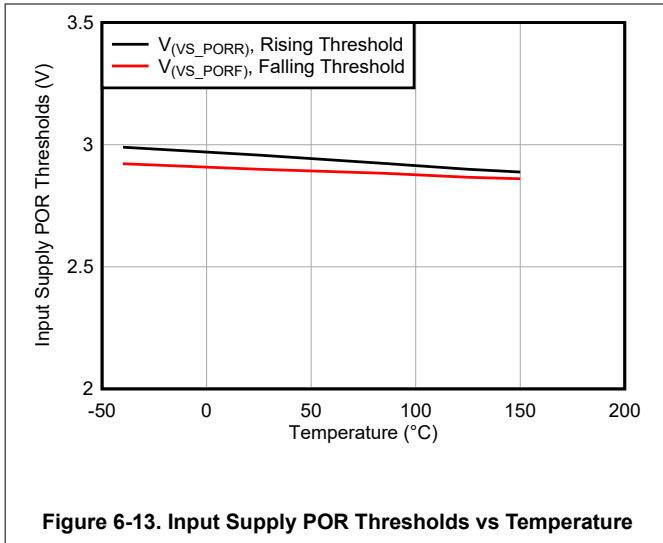
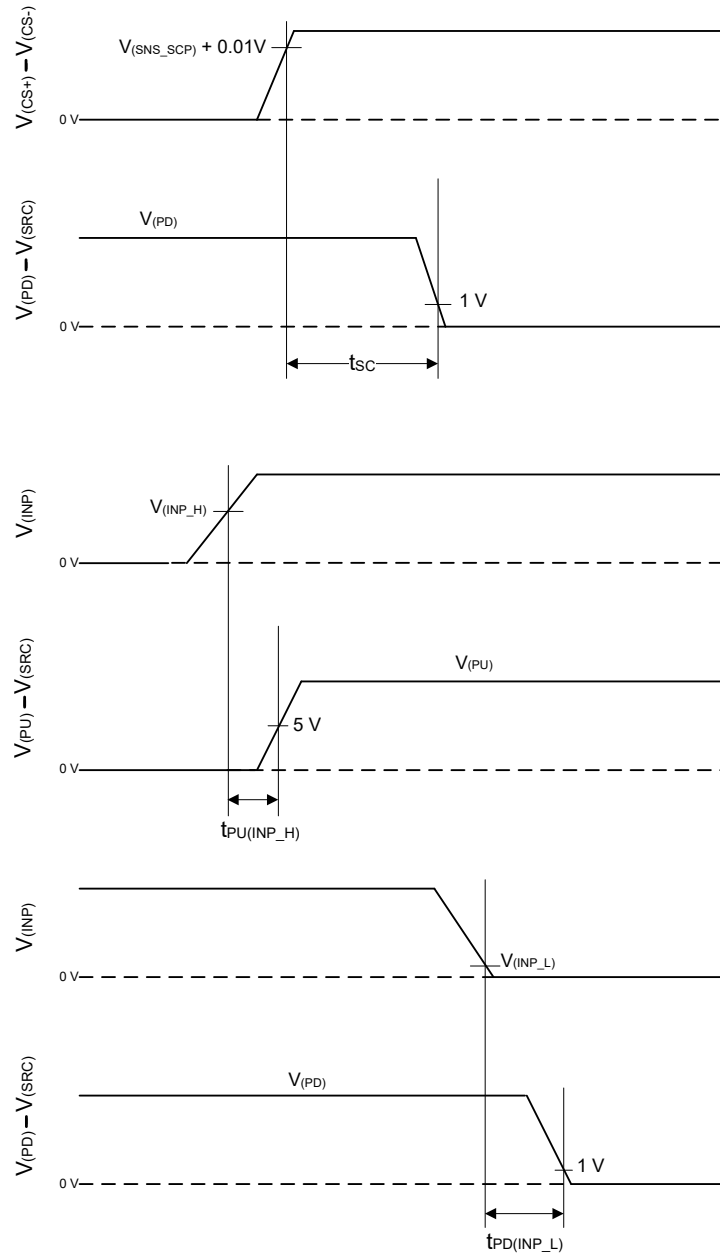


Figure 6-12. Short-Circuit Protection Response Time ( $t_{sc}$ ) vs Temperature

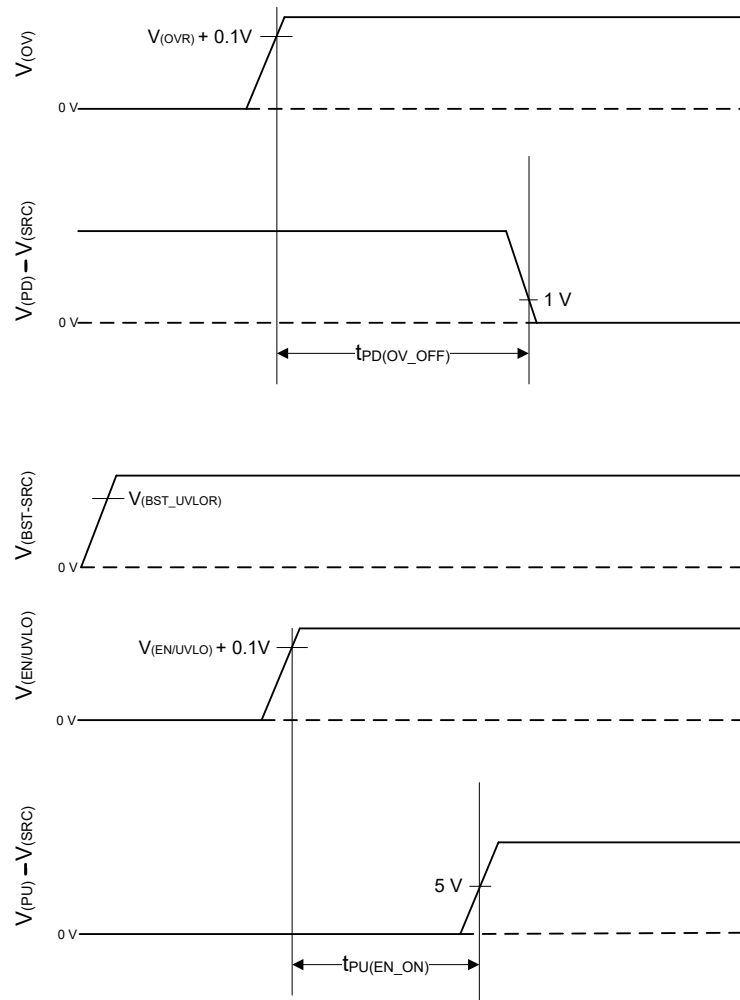
## 6.7 Typical Characteristics (continued)



## 7 Parameter Measurement Information



**Figure 7-1. Timing Waveforms**



**Figure 7-2. Timing Waveforms**

## 8 Detailed Description

### 8.1 Overview

The TPS4811x-Q1 family is a 100V smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5V – 80V, the device is an excellent choice for 12V, 24V, and 48V system designs.

The device has a strong 3.7A peak source (PU) and 4A peak sink (PD) GATE driver that enables power switching using parallel FETs in high current system designs. Use INP as the gate driver control input. MOSFET slew rate control (ON and OFF) is possible by placing external R-C components.

The device has accurate current sensing ( $\pm 2\%$  at 30mV  $V_{SNS}$ ) output (IMON) enabling systems for energy management. The device has integrated two-level overcurrent protection with  $\overline{FLT\_I}$  output with complete adjustability of thresholds and response time. Auto-retry and latch-off fault behavior can be configured.

The device features remote overtemperature protection with  $\overline{FLT\_T}$  output enabling robust system protection.

TPS48110Q1 has an accurate overvoltage protection ( $< \pm 2\%$ ), providing robust load protection.

The TPS48111Q1 integrates a pre-charge driver (G) with control input (INP\_G). This feature enables system designs that need to drive large capacitive loads by pre-charging first and then turning ON the main power FETs.

TPS4811x-Q1 has an accurate undervoltage protection ( $< \pm 2\%$ ) using EN/UVLO pin. Pull EN/UVLO low ( $< 0.3V$ ) to turn OFF the device and enter into shutdown state. In shutdown mode, the controller draws a total shutdown current of 1.6 $\mu A$  at 48V supply input.

### 8.2 Functional Block Diagram

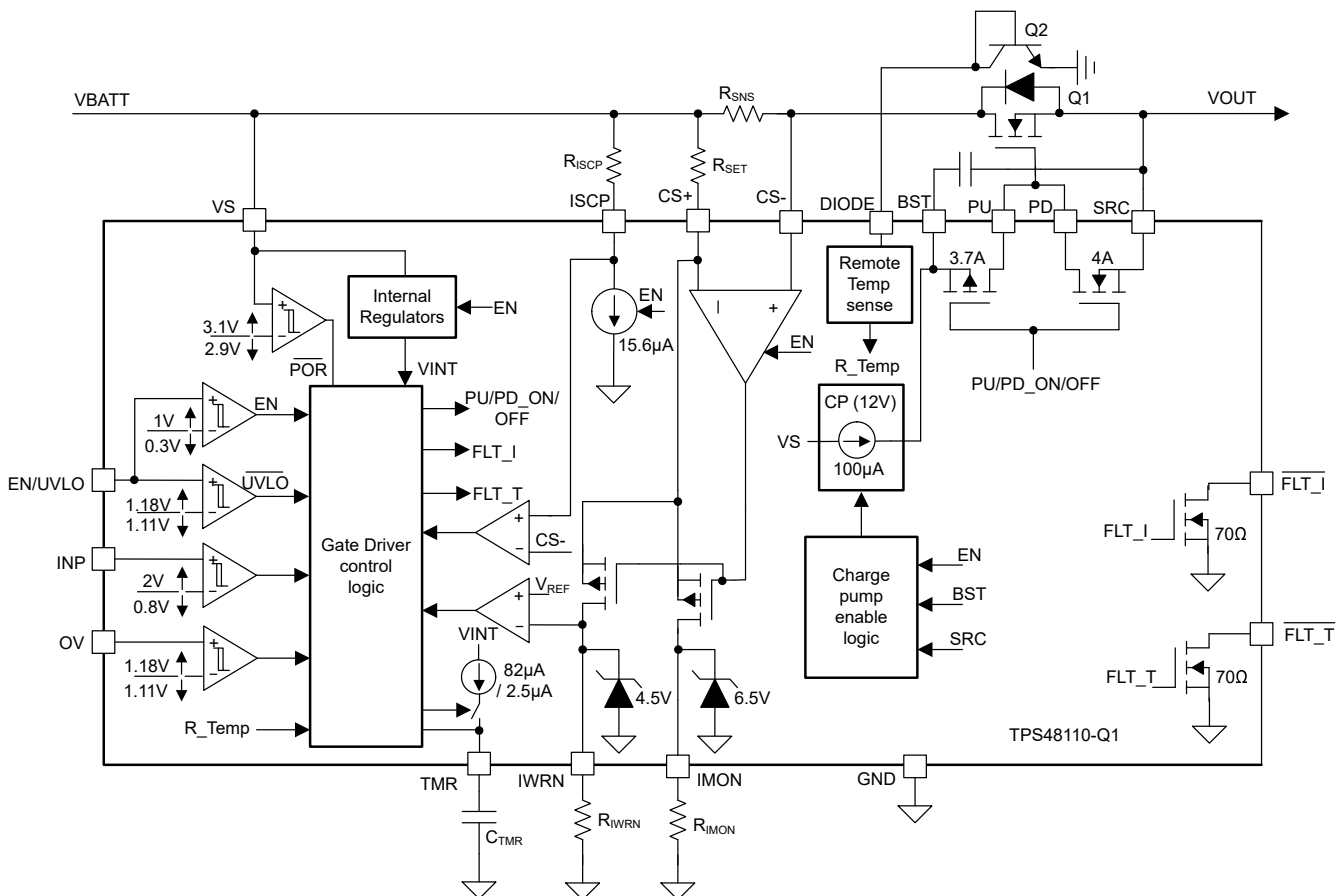


Figure 8-1. TPS48110Q1 Functional Block Diagram

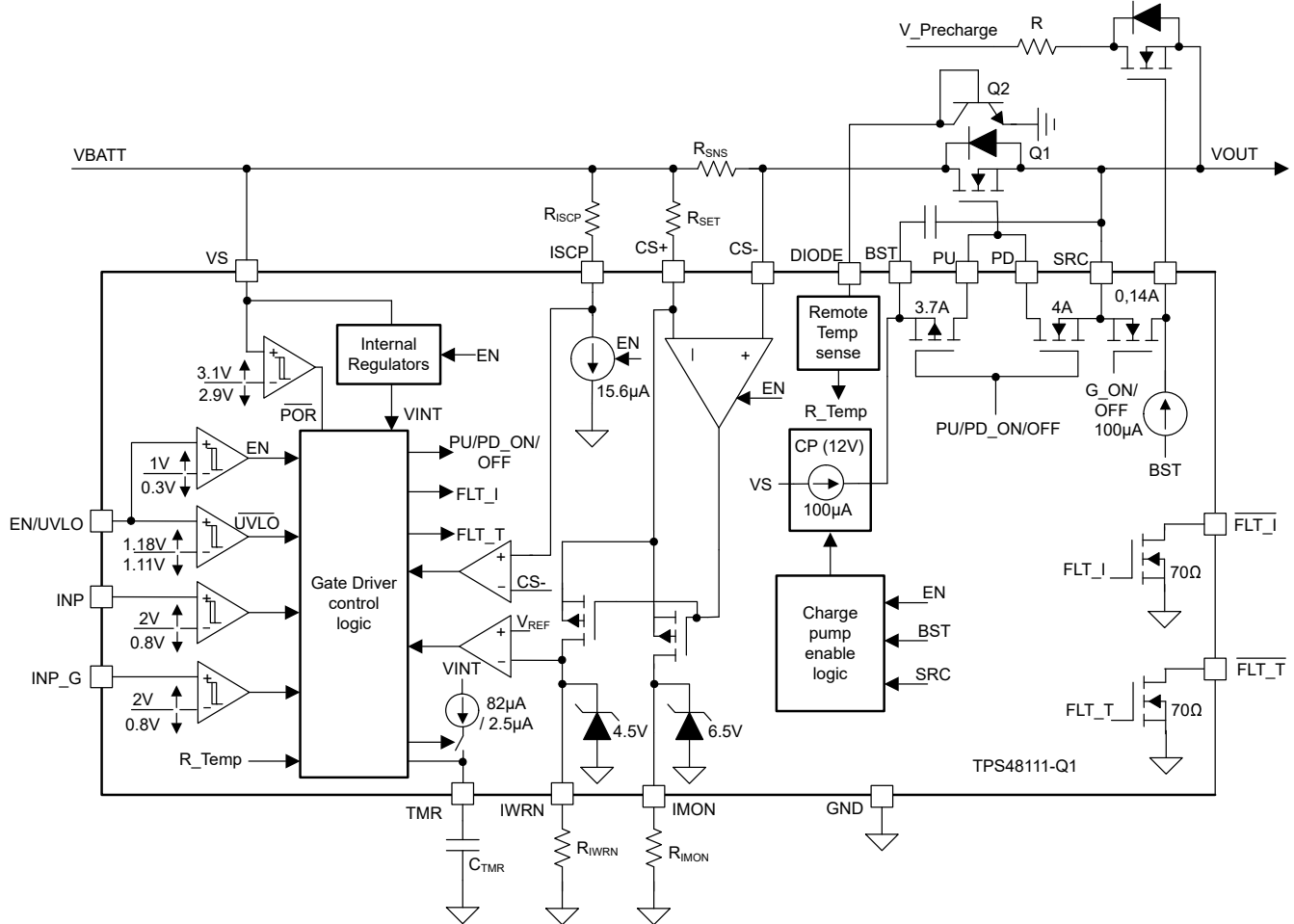


Figure 8-2. TPS4811Q1 Functional Block Diagram

## 8.3 Feature Description

### 8.3.1 Charge Pump and Gate Driver output (VS, PU, PD, BST, SRC)

Figure 8-3 shows simplified diagram of the charge pump and gate driver circuit implementation. The device houses a strong 3.7A peak source and 4A peak sink gate drivers. The strong gate drivers enable paralleling of FETs in high power system designs ensuring minimum transition time in saturation region. A 12V, 100µA charge pump is derived from VS terminal and charges the external boot-strap capacitor,  $C_{BST}$  that is placed across the GATE driver (BST and SRC).

In switching applications, if the charge pump supply demand is higher than 100µA, then supply BST externally using a low leakage diode and  $V_{AUX}$  supply as shown in the Figure 8-3.

VS is the supply pin to the controller. With VS applied and EN/UVLO pulled high, the charge pump turns ON and charges the  $C_{BST}$  capacitor. After the voltage across  $C_{BST}$  crosses  $V_{(BST\_UVLOR)}$ , the GATE driver section gets activated. The device has a 1V (typical) UVLO hysteresis to ensure chattering less performance during initial GATE turn ON. Select  $C_{BST}$  based on the external FET's  $Q_G$  and allowed dip during FET turn ON. The charge pump remains enabled until the BST to SRC voltage reaches 12.3V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the BST to SRC voltage discharges to 11.7V typically at which point the charge pump is enabled. The voltage between BST and SRC continue to charge and discharge from between 12.3V and 11.7V as shown in the Figure 8-3.

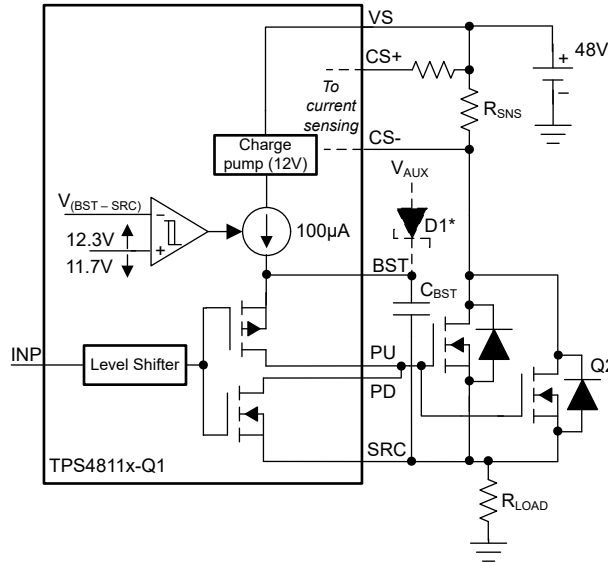


Figure 8-3. Gate Driver

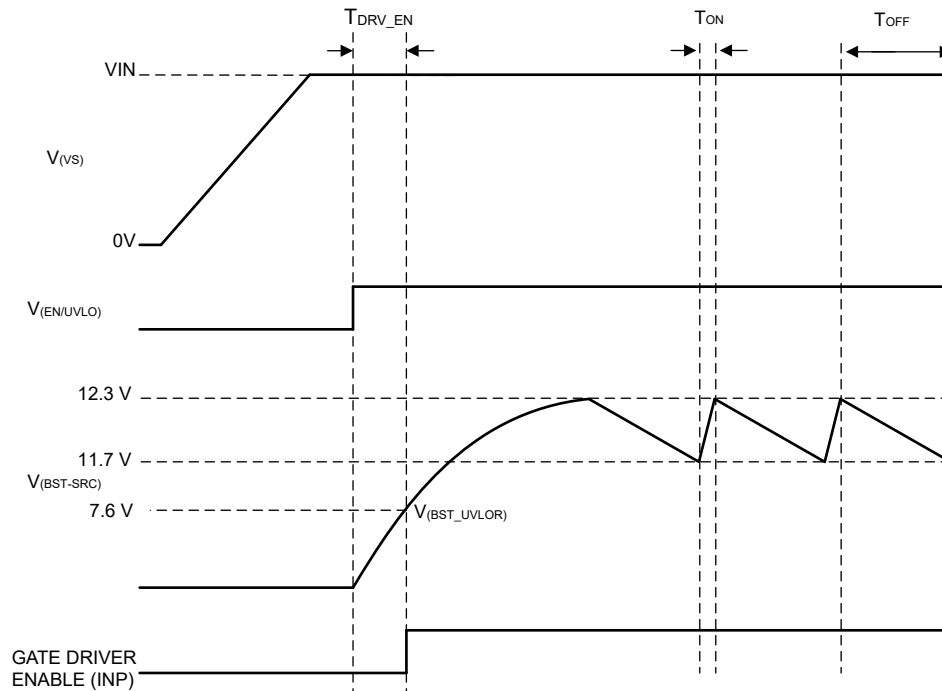


Figure 8-4. Charge Pump Operation

Use the following equation to calculate the initial gate driver enable delay.

$$T_{DRV\_EN} = \frac{C_{BST} \times V_{(BST\_UVLOR)}}{100\mu A} \quad (1)$$

Where:

- $C_{BST}$  is the charge pump capacitance connected across BST and SRC pins
- $V_{(BST\_UVLOR)} = 7.6V$  (typical)

If  $T_{DRV\_EN}$  needs to be reduced then pre-bias BST terminal externally using an external  $V_{AUX}$  supply through a low leakage diode D1 as shown in Figure 8-3. With this connection,  $T_{DRV\_EN}$  reduces to 350 $\mu$ s. TPS4811x-Q1 application circuit with external supply to BST is shown in Figure 8-5.

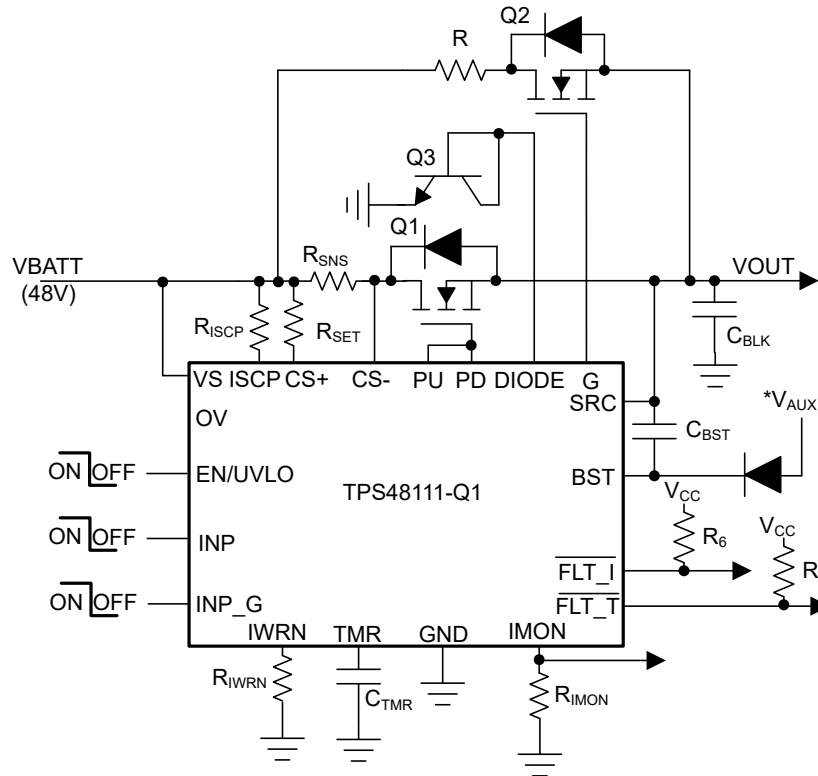


Figure 8-5. TPS4811Q1 Application Circuit With External Supply to BST

**Note**

$V_{AUX}$  can be supplied by external supply ranging from 8.1V and 15V.

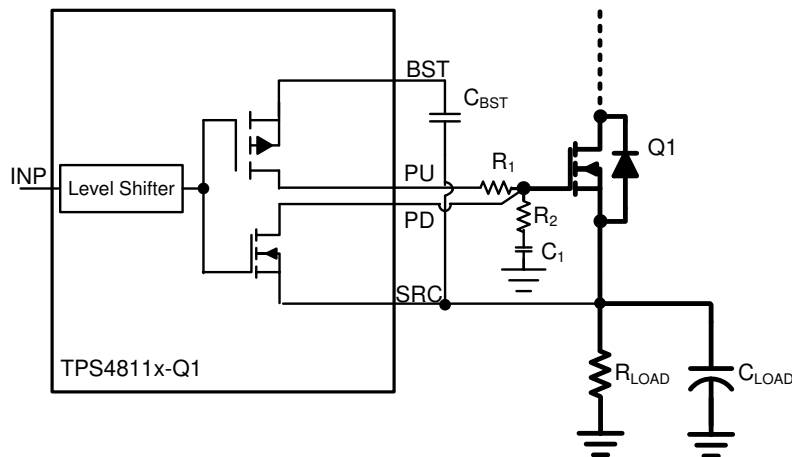
**8.3.2 Capacitive Load Driving**

Certain end equipments such as automotive power distribution unit power different loads, including other ECUs. ECUs can have large input capacitances. If power to the ECUs is switched on in uncontrolled way, large inrush currents can occur, potentially damaging the power FETs.

To limit the inrush current during capacitive load switching, use following system design techniques with TPS4811x-Q1 devices.

**8.3.2.1 FET Gate Slew Rate Control**

For limiting inrush current during turn ON of the FET with capacitive loads, use  $R_1$ ,  $R_2$ , and  $C_1$ , as shown in Figure 8-6. The  $R_1$  and  $C_1$  components slow down the voltage ramp rate at the gate of the FET. The FET source follows the gate voltage resulting in a controlled voltage ramp across the output capacitors.



**Figure 8-6. Inrush Current Limiting with FET Gate Slew Rate Control**

Use the [Equation 2](#) to calculate the inrush current during turn-ON of the FET.

$$I_{\text{INRUSH}} = C_{\text{LOAD}} \times \frac{V_{\text{BATT}}}{T_{\text{charge}}} \quad (2)$$

$$I_{\text{INRUSH}} = \frac{0.63 \times V_{(\text{BST} - \text{SRC})} \times C_{\text{LOAD}}}{R_1 \times C_1} \quad (3)$$

Where

- $C_{\text{LOAD}}$  is the load capacitance
- $V_{\text{BATT}}$  is the input voltage
- $T_{\text{charge}}$  is the charge time
- $V_{(\text{BST} - \text{SRC})}$  is the charge pump voltage (12V)

Use a damping resistor  $R_2$  ( $\cong 10\Omega$ ) in series with  $C_1$ . [Equation 3](#) can be used to compute required  $C_1$  value for a target inrush current. A 100k $\Omega$  resistor for  $R_1$  can be a good starting point for calculations.

Connecting PD pin of TPS4811x-Q1 directly to the gate of the external FET ensures fast turn OFF without any impact of  $R_1$  and  $C_1$  components.

$C_1$  results in an additional loading on  $C_{\text{BST}}$  to charge during turn ON. Use [Equation 4](#) to calculate the required  $C_{\text{BST}}$  value.

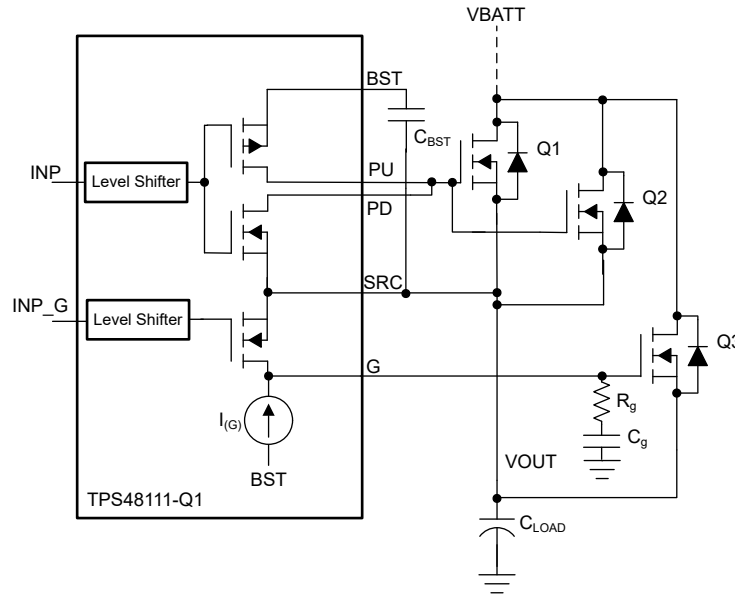
$$C_{\text{BST}} > Q_{\text{g}(\text{total})} + 10 \times C_1 \quad (4)$$

Where,  $Q_{\text{g}(\text{total})}$  is the total gate charge of the FET.

### 8.3.2.2 Using Precharge FET - (with TPS4811Q1 Only)

In high-current applications where several FETs are connected in parallel, the gate slew rate control for the main FETs is not recommended due to unequal distribution of inrush currents among the FETs. This action makes FET selection complex and results in over sizing of the FETs.

The TPS4811Q1 integrates precharge gate driver (G) with a dedicated control input (INP\_G). This feature can be used to drive a separate FET that can be used to precharge the capacitive load. [Figure 8-7](#) shows the precharge FET implementation for capacitive load charging using TPS4811Q1. An external capacitor  $C_{\text{g}}$  reduces the gate turn-ON slew rate and controls the inrush current.



**Figure 8-7. Capacitor Charging Using Gate Slew Rate Control of Precharge FET**

During power up with EN/UVLO high and  $C_{BST}$  voltage above  $V_{(BST\_UVLOR)}$  threshold, INP and INP\_G controls are active. For the precharge functionality, drive INP low to keep the main FETs OFF and drive INP\_G high. G output gets pulled up to BST with  $I_G$ . Use Equation 5 to calculate the required  $C_g$  value.

$$C_g = \frac{C_{LOAD} \times I_{(G)}}{I_{INRUSH}} \quad (5)$$

Where:

- $I_{(G)}$  is 100 $\mu$ A (typical)
- $C_{LOAD}$  is total load capacitance

Use Equation 2 to calculate the  $I_{INRUSH}$ . A series resistor  $R_g$  must be used in conjunction with  $C_g$  to limit the discharge current from  $C_g$  during turn-off. The recommended value for  $R_g$  is from 220 $\Omega$  to 470 $\Omega$ . After the output capacitor is charged, turn OFF the precharge FET by driving INP\_G low. G gets pulled low to SRC with an internal 135mA pulldown switch. The main FETs can be turned ON by driving INP high.

Figure 8-8 shows other system design approaches to charge large output capacitors in high current applications. The designs involve an additional power resistor in series in series with precharge FET. The back-to-back FET topology shown is typically used in bi-directional power control applications like battery management systems.



Where:

- $R_{SET}$  is the resistor connected across CS+ and VS
- $R_{SNS}$  is the current sense resistor
- $I_{OC}$  is the overcurrent level

---

**Note**

For short-circuit protection feature only, connect IWRN pin to GND and select  $R_{ISCP}$  resistor as per [Section 8.3.3.3](#).

For overcurrent protection feature only, connect ISCP pin to CS– pin directly and select  $R_{IWRN}$  resistor as per [Equation 6](#).

In case of overcurrent or short-circuit event, TPS4811Q1 controller turns off main FET by pulling PD low but state of pre-charge FET drive (G) is not changed.

---

### 8.3.3.1 Overcurrent Protection With Auto-Retry

The  $C_{TMR}$  programs the over current protection delay ( $t_{OC}$ ) and auto-retry time ( $t_{RETRY}$ ). Once the voltage across CS+ and CS– exceeds the set point, the  $C_{TMR}$  starts charging with 82µA pullup current. After the  $C_{TMR}$  charges up to  $V_{(TMR\_FLT)}$ ,  $\overline{FLT\_I}$  asserts low providing warning on impending FET turn OFF. After  $C_{TMR}$  charges to  $V_{(TMR\_OC)}$ , PD pulls low to SRC turning OFF the FET. Post this event, the auto-retry behavior starts. The  $C_{TMR}$  capacitor starts discharging with 2.5µA pulldown current. After the voltage reaches  $V_{(TMR\_LOW)}$  level, the capacitor starts charging with a 2.5µA pullup. After 32 charging, discharging cycles of  $C_{TMR}$  the FET turns ON back and  $\overline{FLT\_I}$  de-asserts after de-assertion delay of 260µs.

Use [Equation 7](#) to calculate the  $C_{TMR}$  capacitor to be connected between TMR and GND.

$$C_{TMR} = \frac{I_{TMR} \times t_{OC}}{1.2} \quad (7)$$

Where,  $I_{TMR}$  is internal pull-up current of 82µA,  $t_{OC}$  is desired overcurrent response time.

Use [Equation 8](#) to calculate the  $T_{FLT}$  duration.

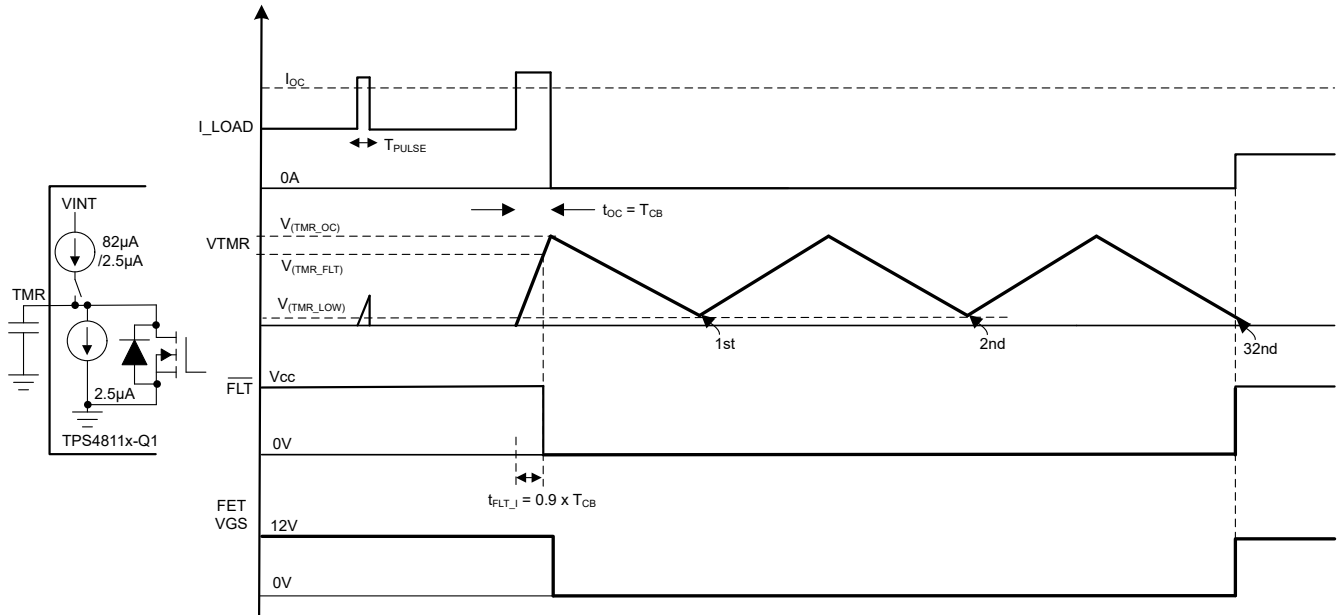
$$T_{FLT} = \frac{1.1 \times C_{TMR}}{82\mu} \quad (8)$$

Where,  $T_{FLT}$  is the  $\overline{FLT\_I}$  assertion delay.

The auto-retry time can be computed as:

$$t_{RETRY} = 22.7 \times 10^6 \times C_{TMR} \quad (9)$$

If the overcurrent pulse duration is below  $t_{OC}$ , then the FET remains ON and  $C_{TMR}$  is discharged using internal pulldown switch.



**Figure 8-10. Overcurrent Protection with Auto-Retry**

### 8.3.3.2 Overcurrent Protection With Latch-Off

Connect an approximately 100kΩ resistor across C<sub>TMR</sub> as shown in [Figure 8-11](#). With this resistor, during the charging cycle, the voltage across C<sub>TMR</sub> is clamped to a level below V<sub>(TMR\_OC)</sub>, resulting in a latch-off behavior.

Use [Equation 10](#) to calculate C<sub>TMR</sub> capacitor that connects between TMR and GND for R<sub>TMR</sub> = 100kΩ.

$$C_{TMR} = \frac{t_{OC}}{R_{TMR} \times \ln\left(\frac{1}{1 - \frac{1.2}{R_{TMR} \times I_{TMR}}}\right)} \quad (10)$$

Where:

- I<sub>TMR</sub> is internal pull-up current of 82μA
- t<sub>OC</sub> is desired overcurrent response time

Toggle INP or EN/UVLO (below ENF) or power cycle VS below V<sub>(VS\_PORF)</sub> to reset the latch. At low edge, the timer counter is reset and C<sub>TMR</sub> is discharged. PU pulls up to BST when INP is pulled high.

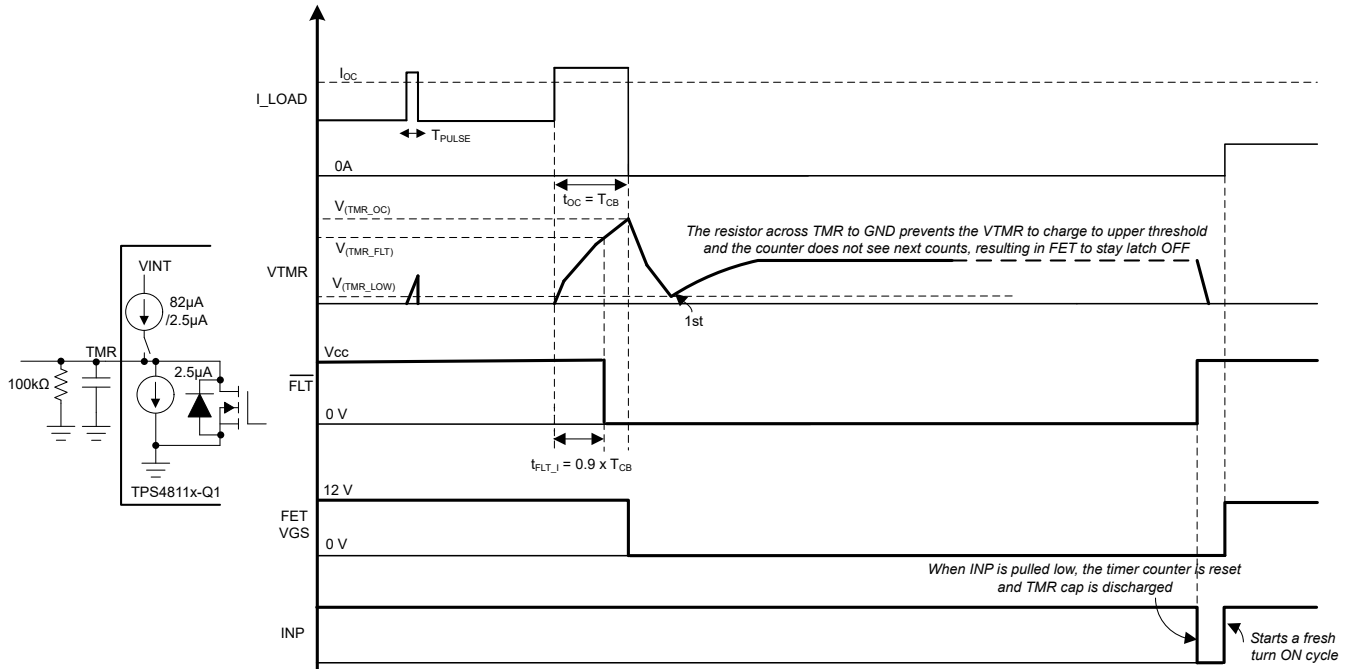


Figure 8-11. Overcurrent Protection With Latch-Off

### 8.3.3.3 Short-Circuit Protection

Connect a resistor,  $R_{ISCP}$ , as shown in Figure 8-12.

Use Equation 11 to calculate the required  $R_{ISCP}$  value.

$$R_{ISCP}(\Omega) = \frac{I_{SC} \times R_{SNS}}{15.6\mu} - 464 \quad (11)$$

Where:

- $R_{SNS}$  is the current sense resistor
- $I_{SC}$  is the desired short-circuit protection level

After the current exceeds the  $I_{SC}$  threshold, PD pulls low to SRC within 1.2μs in TPS4811Q1 and 4μs in TPS48110Q1, protecting the FET.  $\overline{FLT_1}$  asserts low at the same time. Subsequent to this event, the charge and discharge cycles of  $C_{TMR}$  start, similar to the behavior post FET OFF event in the over-current protection scheme.

Latch-off can also be achieved in the similar way as explained in the overcurrent protection scheme.

#### Note

Connect IWRN pin to GND if only short-circuit protection is required.  $R_{ISCP}$  resistor can be selected as per Section 8.3.3.3.

### 8.3.4 Analog Current Monitor Output (IMON)

TPS4811x-Q1 features an accurate analog load current monitor output (IMON) with adjustable gain. The current source at IMON terminal is configured to be proportional to the current flowing through the  $R_{SNS}$  current sense resistor. This current can be converted to a voltage using a resistor  $R_{IMON}$  from IMON terminal to GND terminal. This voltage, computed using Equation 12, can be used as a means of monitoring current flow through the system.

Use Equation 12 to calculate the  $V_{(IMON)}$ .



### 8.3.5 Overvoltage (OV) and Undervoltage Protection (UVLO)

TPS4811x-Q1 has an accurate undervoltage protection ( $< \pm 2\%$ ) using EN/UVLO pin.

TPS48110Q1 has an accurate overvoltage protection ( $< \pm 2\%$ ), providing robust load protection. Connect a resistor ladder as shown in Figure 8-13 for undervoltage and overvoltage protection threshold programming.

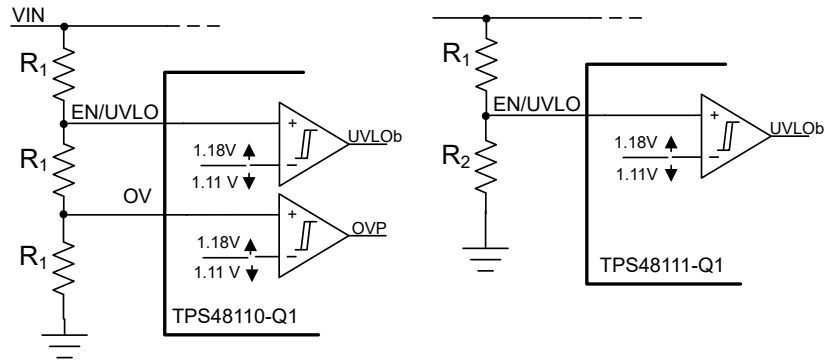


Figure 8-13. Programming Overvoltage and Undervoltage Protection Threshold

### 8.3.6 Remote Temperature sensing and Protection (DIODE)

The device features an integrated remote temperature sensing, protection and dedicated fault output. In TPS4811x-Q1, remote temperature measurement is done by using external transistor in diode configuration. Connect the DIODE pin of TPS4811x-Q1 to the collector and base of an MMBT3904 BJT. The temperature is calculated internally based on difference of measured diode voltages at two test currents.

In TPS48110Q1, after the sensed temperature reaches  $150^{\circ}\text{C}$ , the device pulls PD low to SRC, turning off the external FET and asserts  $\overline{\text{FLT\_T}}$  low. After the temperature reduces to  $130^{\circ}\text{C}$ , an internally fixed auto-retry cycle of 512ms commences.  $\overline{\text{FLT\_T}}$  de-asserts and the external FET turns ON after the retry duration of 512ms is lapsed.

In TPS48111Q1, after the sensed temperature crosses  $150^{\circ}\text{C}$ , PD and G get pulled low to SRC. After the TSD hysteresis, PU and G stays latched OFF. Latch gets reset by toggling EN/UVLO below  $V_{(\text{ENF})}$  or by power cycling VS below  $V_{(\text{VS\_PORF})}$ .

Figure 8-14 shows simplified block diagram of TPS4811x-Q1 DIODE based remote temperature sensing.

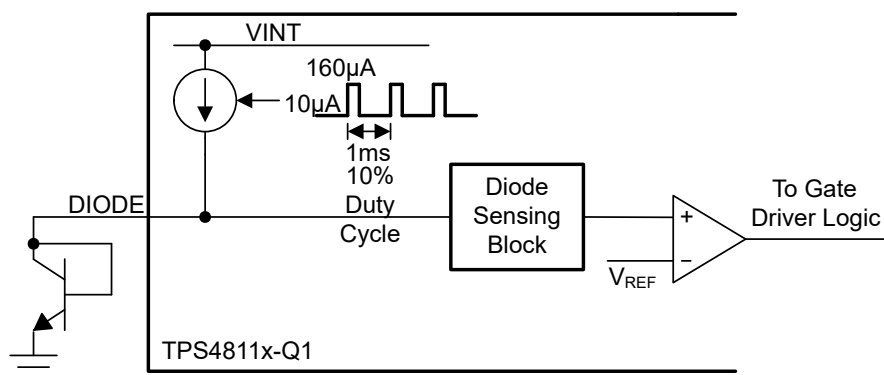


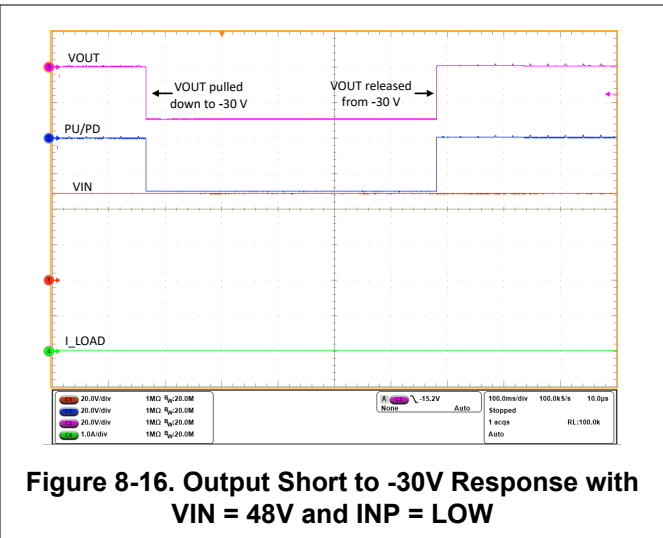
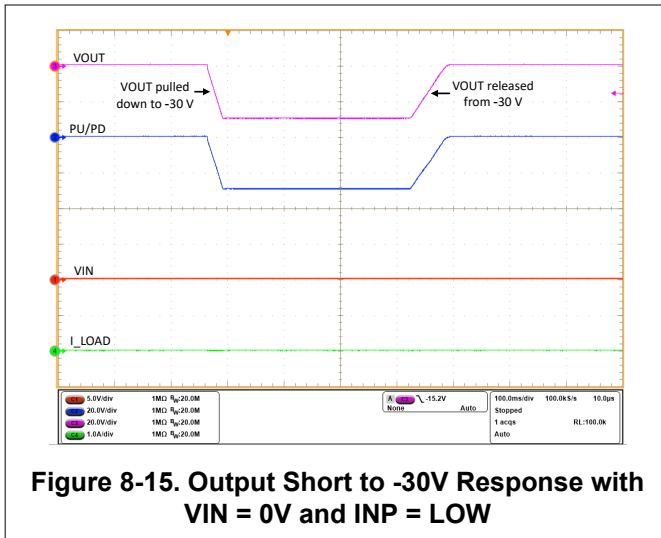
Figure 8-14. DIODE Based Remote Temperature Sensing Block Diagram

### 8.3.7 Output Reverse Polarity Protection

The TPS4811x-Q1 withstands output reverse voltages down to  $-30\text{V}$ . With INP low, PD is pulled low to SRC and keeps the external FET OFF even with output (SRC) voltage at negative levels preventing high current flow and protecting the main FET. Refer to Figure 8-15 and Figure 8-16 for test waveforms.

TPS4811-Q1

SLUSEE5E – JANUARY 2022 – REVISED APRIL 2026



8.3.8 TPS4811x-Q1 as a Simple Gate Driver

Figure 8-17 shows application schematics of TPS4811x-Q1 as a simple gate driver in load disconnect switch as well as back-to-back FETs driving topologies. The protection features such as two-level overcurrent protection, overvoltage protection, and overtemperature protection are disabled.

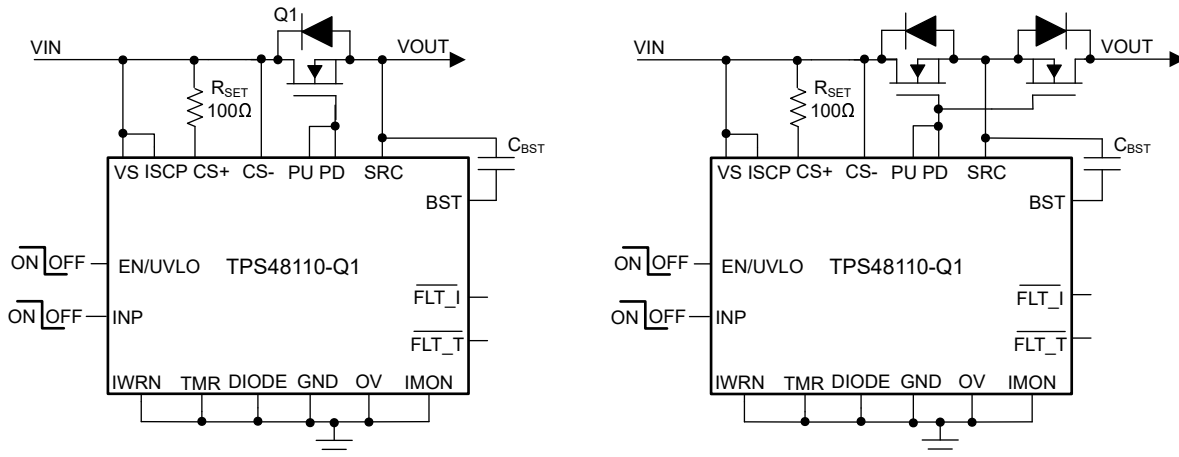


Figure 8-17. Connection Diagram of TPS4811Q1 for Simple Gate Driver Design

8.4 Device Functional Mode (Shutdown Mode)

The TPS4811x-Q1 has two modes of operation: active mode and low IQ shutdown mode. If the EN/UVLO pin voltage is greater than the rising threshold, then the device is in active mode. In active state the internal charge pump is enabled, gate drivers and all the protection and diagnostic features are enabled.

If the EN/UVLO voltage is pulled  $< V_{(ENF)}$ , the device enters into low IQ shutdown mode. In this mode, the charge pump, gate drivers and all the protection features are disabled. The external FETs turn OFF. The TPS4811x-Q1 consumes low IQ of 1.6 $\mu$ A (typical) in this mode.

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS4811x-Q1 family is a 100V smart high side driver with protection and diagnostics. The TPS4811x-Q1 device controls external N-channel MOSFETs and its drive architecture is suitable to drive back-to-back N-Channel MOSFETs. The strong gate 3.7A peak source and 4A peak sink capabilities enable switching parallel MOSFETs in high current applications such as circuit breaker in Powertrain (DC/DC converter), Battery Management System, Electric Power Steering, and driving PTC heater loads etc. The TPS4811x-Q1 device provides two-level adjustable overcurrent protection with adjustable circuit breaker timer, fast short-circuit protection, accurate analog current monitor output, and remote overtemperature protection.

The variant TPS48111Q1 features a separate pre-charge driver (G) with independent control input (INP\_G). This feature enables system designs that need to pre-charge the large output capacitance before turning ON the main power path.

The following design procedure can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool [TPS4811Q1 Design Calculator](#) is available in the web product folder.

### 9.2 Typical Application: Driving HVAC PTC Heater Load on KL40 Line in Power Distribution Unit

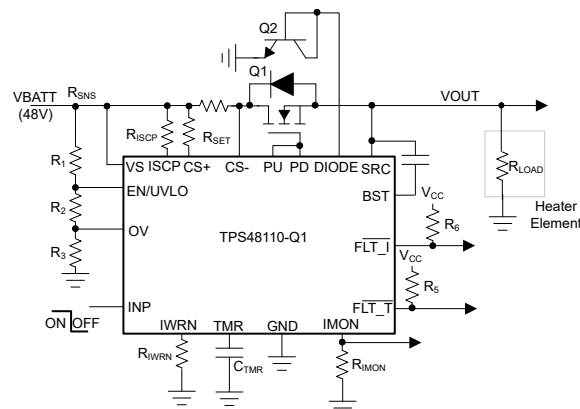


Figure 9-1. Typical Application Schematic: Driving HVAC PTC Heater

## 9.2.1 Design Requirements

Table 9-1 shows the design parameters for this application example.

**Table 9-1. Design Parameters**

PARAMETER	VALUE
Typical input voltage, $V_{IN}$	48V
Undervoltage lockout set point, $V_{INUVLO}$	24V
OV set point, $V_{INOVLP}$	58V
Maximum load current, $I_{OUT}$	12A
Overcurrent protection threshold, $I_{OC}$	15A
Short-circuit protection threshold, $I_{SC}$	20A
Fault timer period ( $t_{OC}$ )	1ms
Fault response	Auto-retry
Load resistance, $R_{LOAD}$	$4 \pm 0.2\Omega$
Load switching frequency, $F_{SW}$	100Hz

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Selection of Current Sense Resistor, $R_{SNS}$

The recommended range of the overcurrent protection threshold voltage,  $V_{(SNS\_WRN)}$ , extends from 10mV to 200mV. Values near the low threshold of 10mV can be affected by the system noise. Values near the upper threshold of 200mV can cause high power dissipation in the current sense resistor. To minimize both the concerns, 25mV is selected as the overcurrent protection threshold voltage. The current sense resistor,  $R_{SNS}$  can be calculated using Equation 15.

$$R_{SNS} = \frac{V_{(SNS - WRN)}}{I_{OC}} = \frac{25mV}{15A} = 1.66m\Omega \quad (15)$$

The next smaller available sense resistor 1.5m $\Omega$ , 1% is chosen.

### 9.2.2.2 Selection of Scaling Resistor, $R_{SET}$

$R_{SET}$  is the resistor connected between VS and CS+ pins. This resistor scales the overcurrent protection threshold voltage and coordinates with  $R_{IWRN}$  and  $R_{IMON}$  to determine the overcurrent protection threshold and current monitoring output. The recommended range of  $R_{SET}$  is 50 $\Omega$ –100 $\Omega$ .

$R_{SET}$  is selected as 100 $\Omega$ , 1% for this design example.

### 9.2.2.3 Programming the Overcurrent Protection Threshold - $R_{IWRN}$ Selection

The  $R_{IWRN}$  sets the overcurrent protection (circuit breaker detection) threshold, whose value can be calculated using Equation 16.

$$R_{IWRN}(\Omega) = \frac{11.9 \times R_{SET}}{(R_{SNS} \times I_{OC} + V_{(OS\_SET)})} \quad (16)$$

To set 15A as overcurrent protection threshold,  $R_{IWRN}$  value is calculated to be 52.88k $\Omega$ .

Select the closest available standard value: 54k $\Omega$ , 1%

### 9.2.2.4 Programming the Short-Circuit Protection Threshold - $R_{ISCP}$ Selection

The  $R_{ISCP}$  sets the short-circuit protection threshold, whose value can be calculated using Equation 17.

$$R_{ISCP}(\Omega) = \frac{I_{SC} \times R_{SNS}}{15.6\mu} - 464 \quad (17)$$

To set 20A as short-circuit protection threshold,  $R_{ISCP}$  value is calculated to be 1.46k $\Omega$ .

Select the closest available standard value: 1.3k $\Omega$ , 1%.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between ISCP and CS- pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI recommends to add filter capacitor of 1nF across ISCP and CS- pins close to the device. Because nuisance trips are dependent on the system and layout parasitics, TI recommends to test the design in a real system and tweaked as necessary.

#### 9.2.2.5 Programming the Fault Timer Period - $C_{TMR}$ Selection

For the design example under discussion, overcurrent transients are allowed for 1ms duration. This blanking interval,  $t_{OC}$  (or circuit breaker interval,  $T_{CB}$ ) can be set by selecting appropriate capacitor  $C_{TMR}$  from TMR pin to ground. The value of  $C_{TMR}$  to set 1ms for  $t_{OC}$  can be calculated using [Equation 18](#).

$$C_{TMR} = \frac{82\mu \times t_{OC}}{1.2} = 68.33\text{nF} \quad (18)$$

Select the closest available standard value: 68nF, 10%.

#### 9.2.2.6 Selection of MOSFET, $Q_1$

For selecting the MOSFET  $Q_1$ , important electrical parameters are the maximum continuous drain current  $I_D$ , the maximum drain-to-source voltage  $V_{DS(MAX)}$ , the maximum drain-to-source voltage  $V_{GS(MAX)}$ , and the drain-to-source ON resistance  $R_{DS(ON)}$ .

The maximum continuous drain current,  $I_D$ , rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage,  $V_{DS(MAX)}$ , must be high enough to withstand the highest voltage seen in the application. Considering 60V as the maximum application voltage, MOSFETs with  $V_{DS}$  voltage rating of 80V is suitable for this application.

The maximum  $V_{GS}$  TPS4811Q1 can drive is 13V, so a MOSFET with 15V minimum  $V_{GS}$  rating must be selected.

To reduce the MOSFET conduction losses, lowest possible  $R_{DS(ON)}$  is preferred.

Based on the design requirements, IPB160N08S4-03ATMA1 is selected and its ratings are:

- 80V  $V_{DS(MAX)}$  and  $\pm 20V$   $V_{GS(MAX)}$
- $R_{DS(ON)}$  is 2.6m $\Omega$  typical at 10V  $V_{GS}$
- MOSFET  $Q_{g(total)}$  is 86nC

#### 9.2.2.7 Selection of Bootstrap Capacitor, $C_{BST}$

The internal charge pump charges the external bootstrap capacitor (connected between BST and SRC pins) with approximately 100 $\mu$ A. In case of switching applications, the BST must be powered externally from  $V_{AUX}$  supply (ranging between 8.1V to 15V) through a low-leakage silicon diode such as CMHD3595 or BAT46WH,115 to avoid collapsing the BST-SRC supply. This need is determined by the value of the switching frequency and MOSFET gate charge.

The maximum possible frequency without external supply is given by [Equation 19](#).

$$f_{SW,max} = \frac{I_{(BST)}}{2 \times Q_{g(total)}} = 581\text{Hz} \quad (19)$$

As the present application is switched at 100Hz, external supply is not required. Use the following equation to calculate the minimum required value of the bootstrap capacitor for driving two parallel BUK7S0R5-40HJ MOSFETs.

$$C_{BST} = \frac{Q_{g(total)}}{1V} = 380\text{nF} \quad (20)$$

Select the closest available standard value: 470nF, 10%.

### 9.2.2.8 Setting the Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage set point are adjusted using an external voltage divider network of  $R_1$ ,  $R_2$  and  $R_3$  connected between VS, EN/UVLO, OVP, and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving [Equation 19](#) and [Equation 22](#).

$$V_{(OVR)} = \frac{R_3}{(R_1 + R_2 + R_3)} \times V_{IN_{OVP}} \quad (21)$$

$$V_{(UVLOR)} = \frac{R_2 + R_3}{(R_1 + R_2 + R_3)} \times V_{IN_{UVLO}} \quad (22)$$

For minimizing the input current drawn from the power supply, TI recommends to use higher values of resistance for  $R_1$ ,  $R_2$  and  $R_3$ . However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current,  $I(R_{123})$  must be selected to be 20 times greater than the leakage current of UVLO and OVP pins.

From the device electrical specifications,  $V_{(OVR)} = 1.18V$  and  $V_{(UVLOR)} = 1.18V$ . From the design requirements,  $V_{IN_{OVP}}$  is 58V and  $V_{IN_{UVLO}}$  is 24V. To solve the equation, first select the value of  $R_1 = 470k\Omega$  and use [Equation 22](#) to solve for  $(R_2 + R_3) = 24.3k\Omega$ . Use [Equation 21](#) and value of  $(R_2 + R_3)$  to solve for  $R_3 = 10.1k\Omega$  and finally  $R_2 = 14.2k\Omega$ . Select the closest standard 1% resistor values:  $R_1 = 470k\Omega$ ,  $R_2 = 14.3k\Omega$ , and  $R_3 = 10.2k\Omega$ .

### 9.2.2.9 Choosing the Current Monitoring Resistor, $R_{IMON}$

Voltage at IMON pin  $V_{(IMON)}$  is proportional to the output load current. This can be connected to an ADC of the downstream system for monitoring the operating condition and health of the system. The  $R_{IMON}$  must be selected based on the maximum load current and the input voltage range of the ADC used.  $R_{IMON}$  is set using [Equation 23](#).

$$V_{(IMON)} = \left( V_{SNS} + V_{(OS\_SET)} \right) \times \frac{0.9 \times R_{IMON}}{R_{SET}} \quad (23)$$

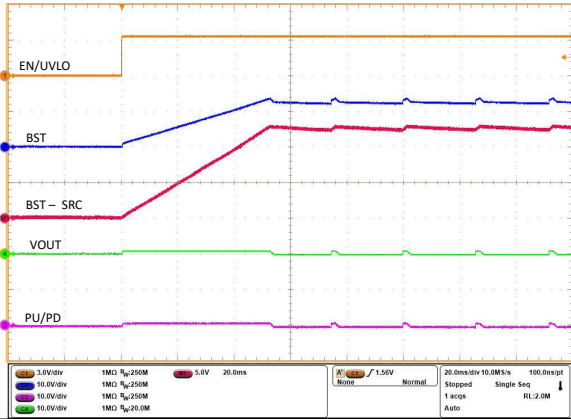
Where  $V_{SNS} = I_{OC} \times R_{SNS}$  and  $V_{(OS\_SET)}$  is the input referred offset ( $\pm 200\mu V$ ) of the current sense amplifier.

For  $I_{OC} = 15A$  and considering the operating range of ADC to be 0V to 3.3V (for example,  $V_{(IMON)} = 3.3V$ ),  $R_{IMON}$  can be calculated as:

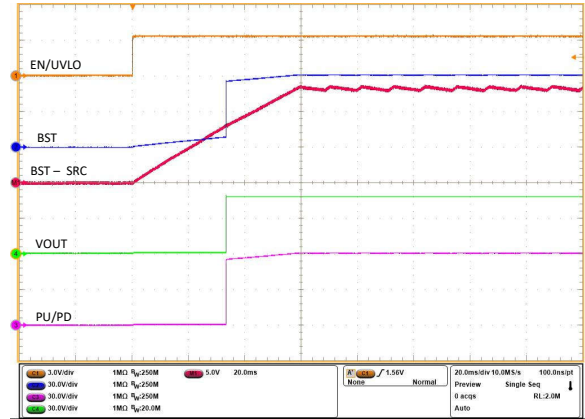
$$R_{IMON} = \frac{V_{(IMON)} \times R_{SET}}{[V_{SNS} + V_{(OS\_SET)}] \times 0.9} = 16.52k\Omega \quad (24)$$

Selecting an  $R_{IMON}$  value less than shown in [Equation 24](#) verifies that ADC limits are not exceeded for maximum value of load current. Choose the closest available standard value: 16.5k $\Omega$ , 1%.

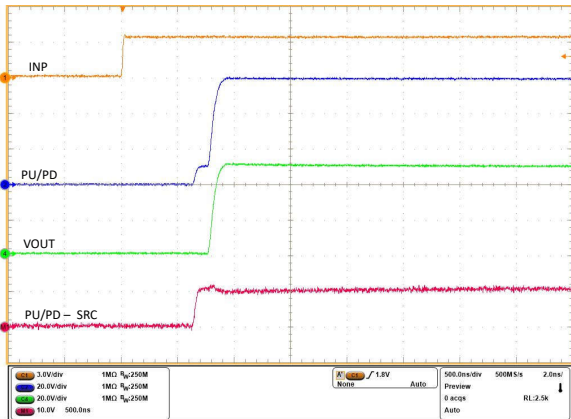
### 9.2.3 Application Curves



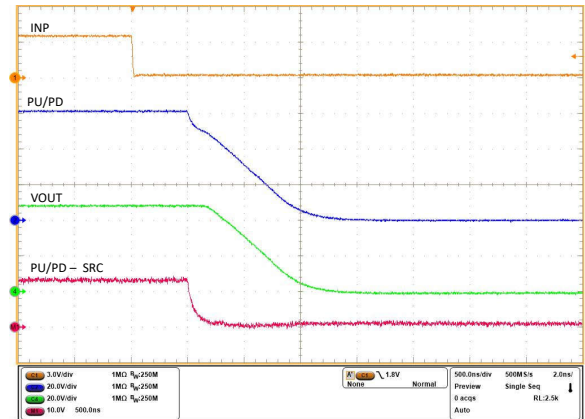
**Figure 9-2. Start-Up Profile of Bootstrap Voltage for INP = GND and  $C_{BST} = 470\text{nF}$**



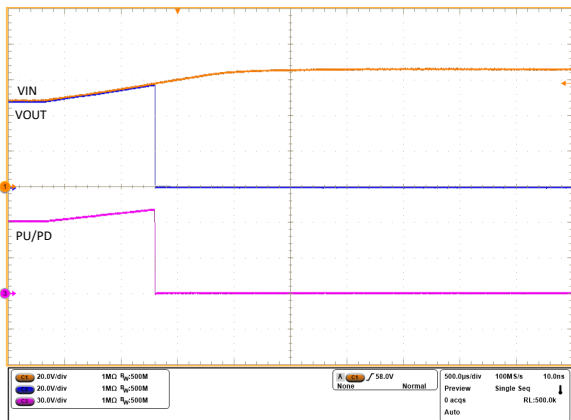
**Figure 9-3. Start-Up Profile of Bootstrap Voltage for INP = HIGH and  $C_{BST} = 470\text{nF}$**



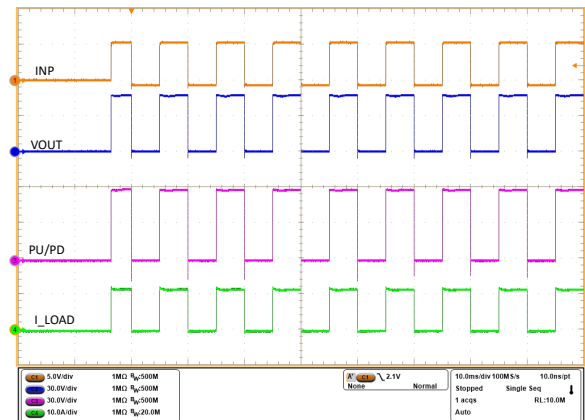
**Figure 9-4. Turn-ON Response of TPS4811Q1 for INP -> LOW to HIGH and  $C_{BST} = 470\text{nF}$**



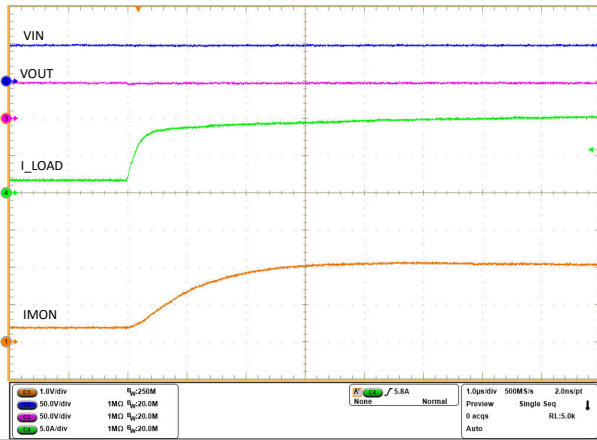
**Figure 9-5. Turn-OFF Response of TPS4811Q1 for INP -> HIGH to LOW and  $C_{BST} = 470\text{nF}$**



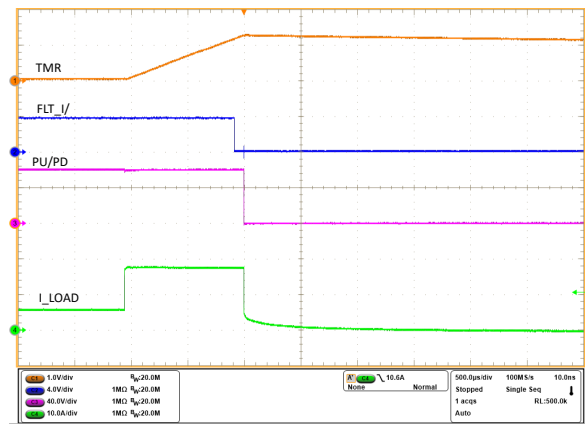
**Figure 9-6. Overvoltage Cut-off Response at 58V Level of TPS4811Q1**



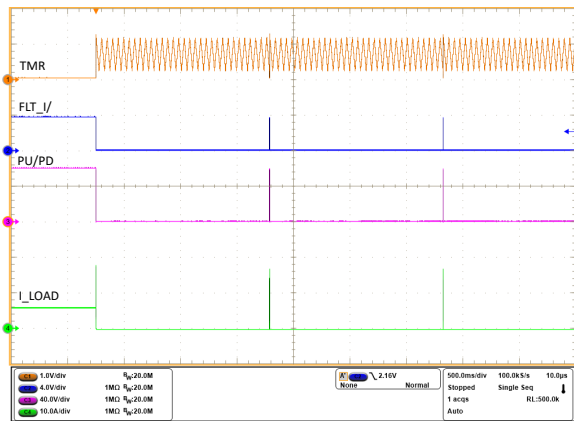
**Figure 9-7. Load Switching at 100Hz With TPS4811Q1**



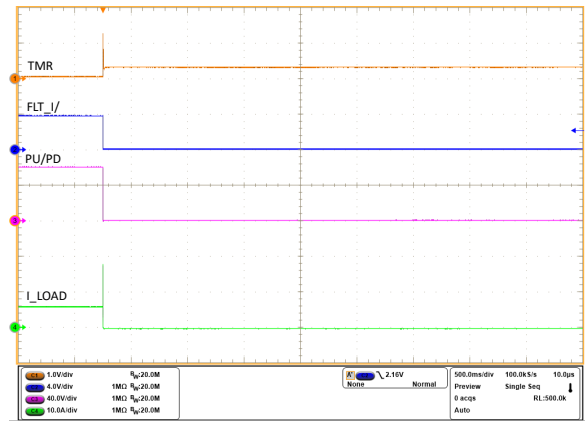
**Figure 9-8. IMON Response During 10A Load Step**



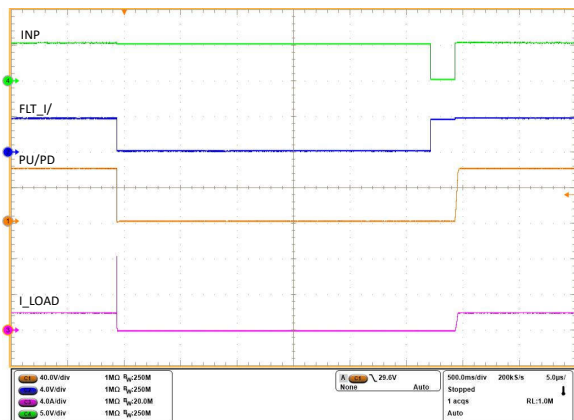
**Figure 9-9. Overcurrent Response of TPS4811Q1 for a Load Step from 5A to 18A With 15A Overcurrent Protection Setting**



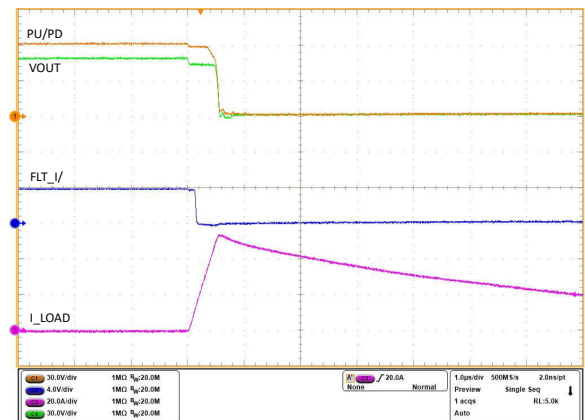
**Figure 9-10. Auto-Retry Response of TPS4811Q1 for an Overcurrent Fault**



**Figure 9-11. Latch-off Response of TPS4811Q1 for an Overcurrent Fault**



**Figure 9-12. Response During Coming Out of Overload Fault With INP Reset**



**Figure 9-13. Output Hot-Short Response of the TPS4811Q1 Device**

### 9.3 Typical Application: Driving B2B FETs With Pre-Charging the Output Capacitance

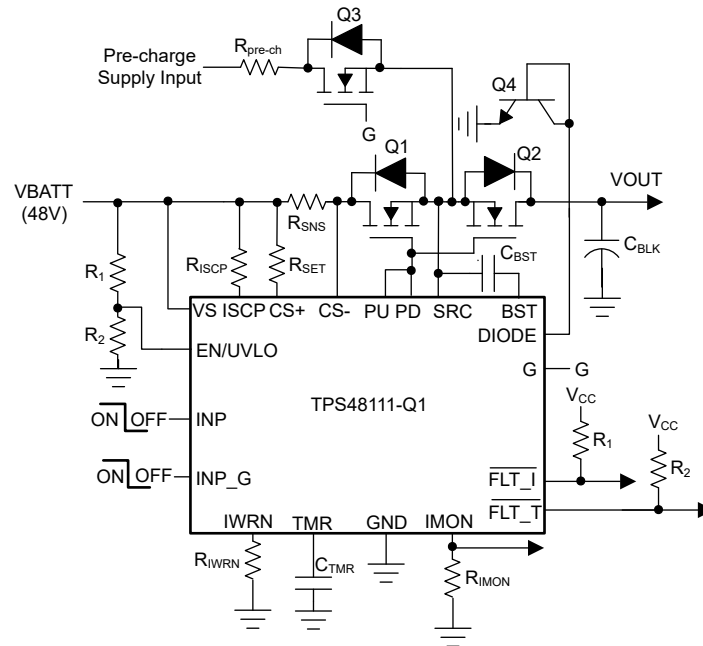


Figure 9-14. Typical Application Schematic: Driving DC-DC Converter Loads in PowerTrain™ Modules

#### 9.3.1 Design Requirements

Table 9-2 shows the design parameters for this application example.

Table 9-2. Design Parameters

PARAMETER	VALUE
Typical input voltage, $V_{IN}$	48V
Undervoltage lockout set point, $V_{INUVLO}$	24V
Maximum load current, $I_{OUT}$	40A
Overcurrent protection threshold, $I_{OC}$	50A
Short-circuit protection threshold, $I_{SC}$	60A
Fault timer period ( $t_{OC}$ )	1ms
Fault response	Latch-off
Load capacitance, $C_{OUT}$	400 $\mu$ F
Inrush current limit, $I_{inrush}$	500mA

#### 9.3.2 External Component Selection

By following similar design procedure as outlined in [Detailed Design Procedure](#), the external component values are calculated as below:

- $R_{SNS} = 500\mu\Omega$
- $R_{SET} = 100\Omega$
- $R_{IWRN} = 47k\Omega$  to set 50A as overcurrent protection threshold
- $R_{ISCP} = 1.46k\Omega$  to set 60A as short-circuit protection threshold
- $C_{TMR} = 68nF$  to set 1ms circuit breaker time
- $R_1$  and  $R_2$  are selected as 470k $\Omega$  and 24.9k $\Omega$  respectively to set  $V_{IN}$  undervoltage lockout threshold at 24V
- $R_{IMON} = 15k\Omega$  to limit maximum  $V_{(IMON)}$  voltage to 3.3V at full-load current of 50A

- To reduce conduction losses, IAUS300N08S5N012 MOSFET is selected. Two FETs are used in parallel for control and another two FETs are used in parallel for reverse current blocking
  - 80V  $V_{DS(MAX)}$  and  $\pm 20V$   $V_{GS(MAX)}$
  - $R_{DS(ON)}$  is 1m $\Omega$  typical at 10V  $V_{GS}$
  - $Q_g$  of each MOSFET is 231nC
- $C_{BST} = (4 \times Q_g) / 1V = 1\mu F$

### 9.3.2.1 Selection of Pre-Charge Resistor

The value of pre-charge resistor must be selected to limit the inrush current to  $I_{inrush}$  as per [Equation 25](#).

$$R_{pre - ch} = \frac{V_{IN}}{I_{inrush}} = 96\Omega \quad (25)$$

The power rating of the pre-charge resistor is decided by the average power dissipation given by [Equation 26](#).

$$P_{avg} = \frac{E_{pre - ch}}{T_{pre - ch}} = \frac{0.5 \times C_{OUT} \times V_{IN}^2}{5 \times R_{pre - ch} \times C_{OUT}} = 2.4W \quad (26)$$

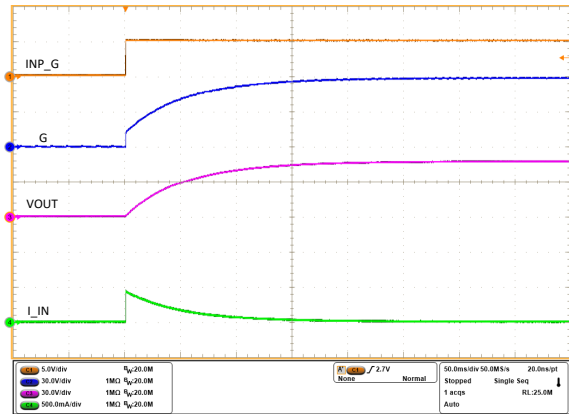
The peak power dissipation in the pre-charge resistor is given by [Equation 27](#).

$$P_{peak} = \frac{V_{IN}^2}{R_{pre - ch}} = 24W \quad (27)$$

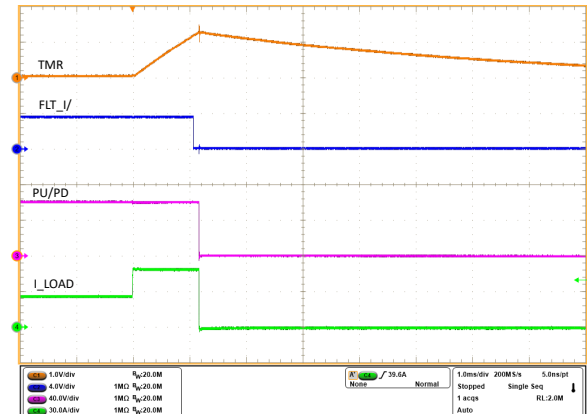
Two 220 $\Omega$ , 1.5W, 5% CRCW2512220RJNEGHP resistors are used in parallel to support both average and peak power dissipation.

TI suggests the designer to share the entire power dissipation profile of pre-charge resistor with the resistor manufacturer and get their recommendation.

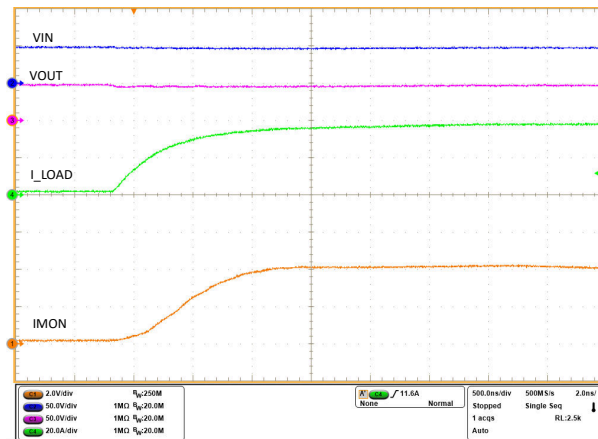
### 9.3.3 Application Curves



**Figure 9-15. Pre-charge Profile of the Output Capacitance (VIN = 48V, C<sub>OUT</sub> = 440μF, No Load)**



**Figure 9-16. Overcurrent Response of TPS4811Q1 for a Load Step from 24A to 54A With 50A Overcurrent Protection Setting**



**Figure 9-17. IMON Response During 40A Load Step**

## 9.4 Typical Application: Designing for EMI

The TPS4811Q1 device features a high accuracy current sense amplifier. Placing strategic EMI components on the current sense pins, CS+ and CS-, can mitigate noise coupling that impacts the current sense functionality of the device.

### 9.4.1 Common EMI Components

For differential pins, like the CS+ and CS- pins, X and Y capacitors are most effective in preventing EMI noise from impacting current sense functions. The X capacitor works to filter differential noise between the two pins and the Y capacitors placed on each pin filter the common mode noise.

General filtering capacitors placed on pins like IMON, IWRN, DIODE, and ISCP to CS- are good practice in most cases, but must be prioritized for EMI applications.

Lastly, ferrite beads can also be placed in series with sense pins to provide a high impedance path at specific low frequency ranges. Ferrite beads are often limited to ranges <1GHz and must be chosen with low DC resistance to mitigate the impact on current sense functions, which rely on the precise values of RSNS, RSET, and ILOAD.

### 9.4.2 Programming the Overcurrent Protection Threshold with Added DC Resistance - RIWRN

Consider an application that uses ferrite beads. The RIWRN equation can be modified to include the impact of additional DC resistance from the ferrite bead.

$$R_{IWRN}(\Omega) = \frac{11.9 \times (R_{SET} + R_{FB})}{(R_{SNS} \times I_{OC}) + V_{OS,SET} + (R_{FB} + I_{CS-})} \quad (28)$$

Where, RSET is the resistor connected across CS+ and VS, RSNS is the current sense resistor, IOC is the overcurrent level, V(OS,SET) is the comparator offset voltage, RFB is the DC resistance of the ferrite bead, and ICS- is the leakage current at the CS- pin.

### 9.4.3 Choosing the Current Monitoring Resistor with Added DC Resistance - RIMON

Additional DC resistance also impacts the RIMON selection.

$$V_{IMON}(V) = [V_{SNS} + V_{OS,SET} + (R_{FB} \times I_{CS-})] \times \frac{0.9 \times R_{IMON}}{R_{SET} + R_{FB}} \quad (29)$$

The IMON accuracy can also be recalculated:

$$\%V_{IMON} = \frac{V_{OS,SET} + (R_{FB} \times I_{CS-})}{V_{SNS}} \times 100 \quad (30)$$

### 9.4.4 Programming the Short Circuit Protection Threshold with Added DC Resistance - RISCP

Lastly, modify [Equation 31](#) because the SCP comparator uses the voltage at CS- pin to compare against voltage created at ISCP pin.

$$R_{ISCP}(\Omega) = \frac{(I_{sc} \times R_{SNS}) + (I_{CS-} \times R_{FB})}{15.6\mu A} - 464 \quad (31)$$

## 9.5 Power Supply and EMI Recommendations

When the external MOSFETs turn OFF during the conditions such as INP control, overvoltage cutoff, overcurrent protection causing an interruption of the current flow, the input parasitic line inductance generates a positive voltage spike on the input and output parasitic inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the [Absolute Maximum Ratings](#) of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Use of a TVS diode and input capacitor filter combination across input to and GND to absorb the energy and dampen the positive transients.
- Use of a diode or a TVS diode across the output and GND to absorb negative spikes.

The TPS4811Q1 gets powered from the VS pin. Voltage at this pin must be maintained above  $V_{(VS\_PORR)}$  level to ensure proper operation. If the input power supply source is noisy with transients, then TI recommends to place a  $R_{VS} - C_{VS}$  filter between the input supply line and VS pin to filter out the supply noise. TI recommends  $R_{VS}$  value around 100Ω.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between ISCP and CS- pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI recommends to add filter capacitor of 1nF ( $C_{SCP}$ ) across ISCP and CS- pins close to the device. Because nuisance trips are dependent on the system and layout parasitics, TI recommends to test the design in a real system and tweaked as necessary.

The following figure shows the circuit implementation with optional protection components.

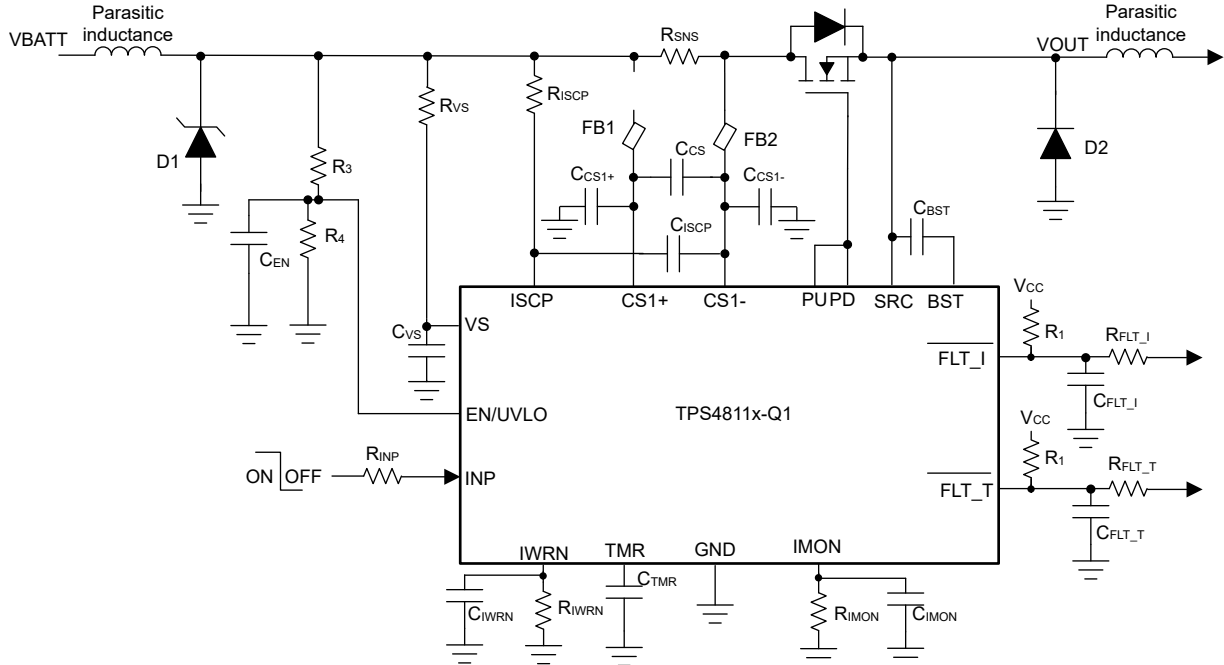


Figure 9-18. Circuit Implementation With Optional Protection Components for TPS4811Q1

Table 9-3. Power Supply and EMI Recommendation Components

Component Designator	Description	Recommended Value
$R_{VS}$ , $C_{VS}$	TPS4811Q1 gets powered from the VS pin. Voltage at this pin must be maintained above $V_{(VS\_PORR)}$ level to ensure proper operation during noisy line transients.	100Ω, 0.1-10μF
$C_{ISCP}$	In a case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between CS1+ and CS1- pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI suggests to add a placeholder for RC filter components across the sense resistor ( $R_{SNS}$ ) and tweak the values during test in the real system. Capacitor ( $C_{ISCP}$ ) across ISCP and DRN pins can also be placed to avoid false short-circuit protection (SCP) during inrush duration or startup.	0.001-1μF
FB1, FB2, $C_{CS}$ , $C_{CS1+}$ , $C_{CS1-}$ , $C_{IMON}$ , $C_{IWRN}$	Ferrite beads (FB1, FB2 ) can be required at CS1+ and CS1- pins for better immunity performance during EMI/EMC testing. Ferrite beads must be selected such that DC Resistance is very low on CS- pin to avoid significantly impacting IMON accuracy. Some other filtering can also be required based on type of immunity test and frequency band through $C_{CS}$ , $C_{CS1+}$ , $C_{CS1-}$ , $C_{IMON}$ , $C_{IWRN}$ to achieve robust immunity performance.	MMZ1608B102CTA00, 10pF for $C_{TMP}$ , $C_{IOC}$ and 10pF - 100nF for others
$R_{GATE\_PU}$ , $R_{GATE\_PD}$ , $D_3$	Resistors on GATE pins can be used for controlling rise and fall time of external FETs. Separate $R_{GATE\_PU}$ must be used for individual external FETs connected in parallel.	Any value
$C_{EN}$	If EN is derived from input supply then $C_{EN}$ can be used to filter supply line transients and avoid false UVLO trigger.	1 - 1000nF
$R_{INP}$ , $R_{FLT\_I}$ , $R_{FLT\_T}$	INP, FLT_I, FLT_T, pins needs to be connected to MCU or other HI/LO source through a resistor for protection especially for reverse polarity fault events.	1 - 10kΩ
$C_{FLT\_I}$ , $C_{FLT\_T}$	Capacitor on FLT_I, FLT_T pins can be used for masking faults	Any value

## 9.6 Layout

### 9.6.1 Layout Guidelines

- The sense resistor ( $R_{SNS}$ ) must be placed close to the TPS4811x-Q1 and then connect  $R_{SNS}$  using the Kelvin techniques. Refer to [Choosing the Right Sense Resistor Layout](#) for more information on the Kelvin techniques.

- For all the applications, TI recommends a 0.1 $\mu$ F or higher value ceramic decoupling capacitor between VS terminal and GND. Consider adding RC network at the supply pin (VS) of the controller to improve decoupling against the power line disturbances.
- The high current path from the board's input to the load, and the return path, must be parallel and close to each other to minimize loop inductance.
- The external MOSFETs must be placed close to the controller such that the GATE of the MOSFETs are close to PU/PD pins to form short GATE loop. Consider adding a place holder for a resistor in series with the Gate of each external MOSFET to damp high frequency oscillations if need arises.
- Place a TVS diode at the input to clamp the voltage transients during hot-plug and fast turn-off events.
- The external boot-strap capacitor must be placed close to BST and SRC pins to form very short loop.
- The ground connections for the various components around the TPS4811x-Q1 must be connected directly to each other, and to the TPS4811x-Q1's GND, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- The DIODE pin sources current to measure the temperature. TI recommends BJT MMBT3904 to use as a remote temperature sense element. Take care in the PCB layout to keep the parasitic resistance between the DIODE pin and the MMBT3904 low so as not to degrade the measurement. In addition, TI recommends to make a Kelvin connection from the emitter of the MMBT3904 to the GND of the part to ensure an accurate measurement. Additionally, a small 1000pF bypass capacitor must be placed in parallel with the MMBT3904 to reduce the effects of noise.

### 9.6.2 Layout Example

- Top Layer
- Inner Layer GND plane
- Inner Layer PGND plane
- Via to GND plane
- Via to PGND plane

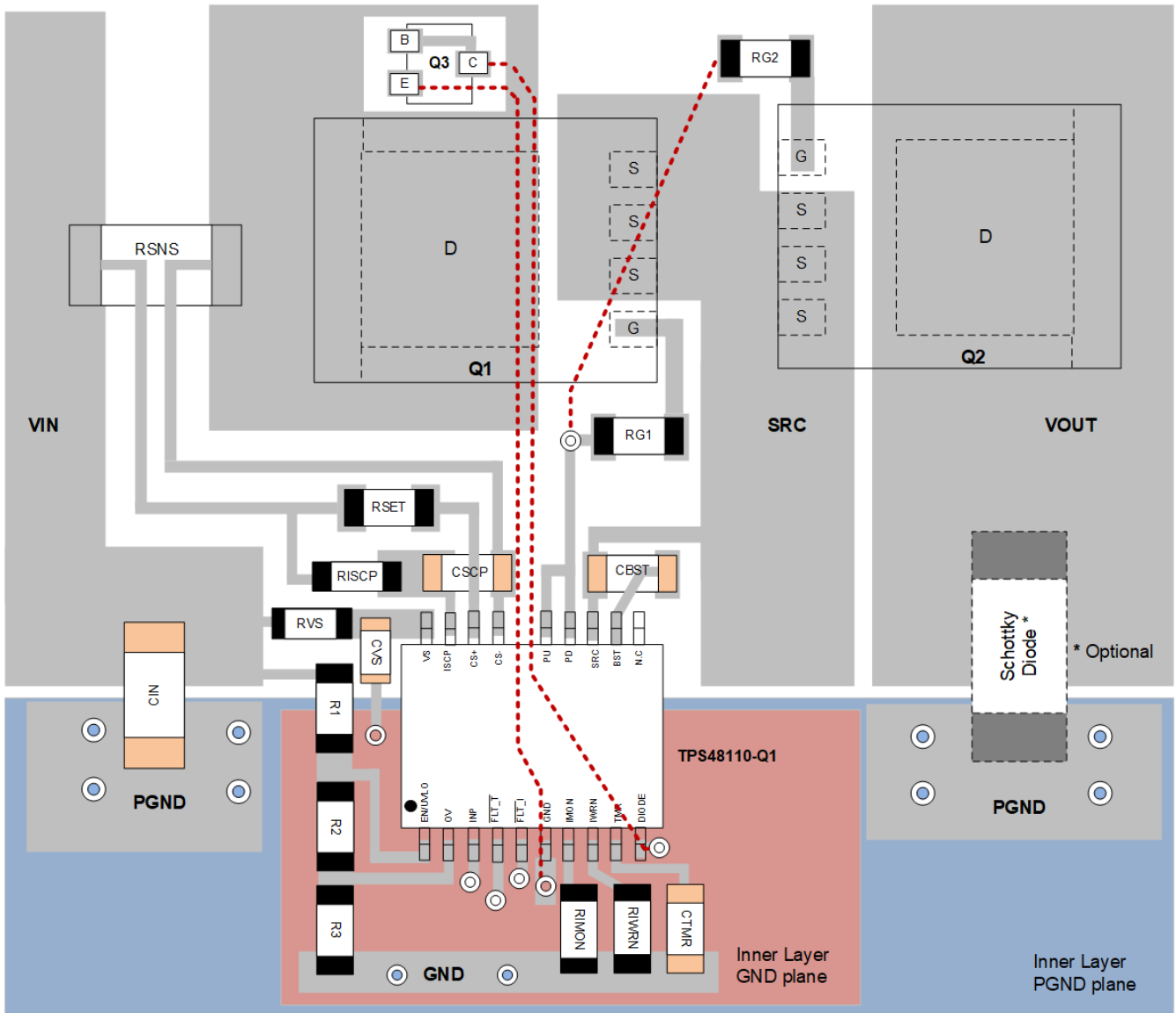


Figure 9-19. Typical PCB Layout Example of TPS4811Q1 With B2B MOSFETs

## 10 Device and Documentation Support

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.3 Trademarks

PowerTrain™ and TI E2E™ are trademarks of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2024) to Revision E (April 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed storage temperature minimum from: $-40^{\circ}\text{C}$ to: $-55^{\circ}\text{C}$ .....	7
• Added voltage slew rate on drain side input pins (VS, CS+, CS-, ISCP).....	7
• Added $I_{(\text{CS-})}$ input bias current.....	8
• Updated <a href="#">Figure 8-6</a> .....	19
• Changed charge pump voltage reference from: 11V to: 12V.....	19
• Added Overcurrent and Short-Circuit Protection section.....	22
• Moved <a href="#">Equation 6</a> from: Detailed Design Procedure to: Overcurrent and Short-Circuit Protection.....	22
• Updated <a href="#">Equation 6</a> to include comparator offset voltage.....	22
• Added <a href="#">Figure 8-9</a> .....	22
• Changed <a href="#">Equation 11</a> from: $-600$ to: $-464$ .....	25
• Moved Device Functional Mode (Shutdown Mode) after Feature Description.....	28
• Updated <a href="#">Equation 16</a> to include comparator offset voltage.....	30
• Changed <a href="#">Equation 17</a> from: $-600$ to: $-464$ .....	30
• Changed calculated $R_{\text{ISCP}}$ value from: $1.32\text{k}\Omega$ to: $1.46\text{k}\Omega$ .....	30
• Added Typical Application: Designing for EMI.....	37
• Changed from: Power Supply Recommendations to: Power Supply and EMI Recommendations.....	38
• Updated <a href="#">Figure 9-19</a> to include $R_{\text{SET}}$ and $R_{\text{ISCP}}$ connection.....	41

---

<b>Changes from Revision C (December 2022) to Revision D (April 2024)</b>	<b>Page</b>
• Updated the DIODE sense TSD rising threshold, $T_{(DIODE\_TSD\_rising)}$ , specification in the <i>Electrical Characteristics</i> section.....	<b>7</b>

---

## **12 Mechanical, Packaging, and Orderable Information**

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS48110AQDGXRQ1</a>	Active	Production	VSSOP (DGX)   19	5000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2UZS
TPS48110AQDGXRQ1.A	Active	Production	null (null)	5000   LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	See TPS48110AQDGXRQ1	2UZS
<a href="#">TPS48111LQDGXRQ1</a>	Active	Production	VSSOP (DGX)   19	5000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2XXS
TPS48111LQDGXRQ1.A	Active	Production	null (null)	5000   LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	See TPS48111LQDGXRQ1	2XXS

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

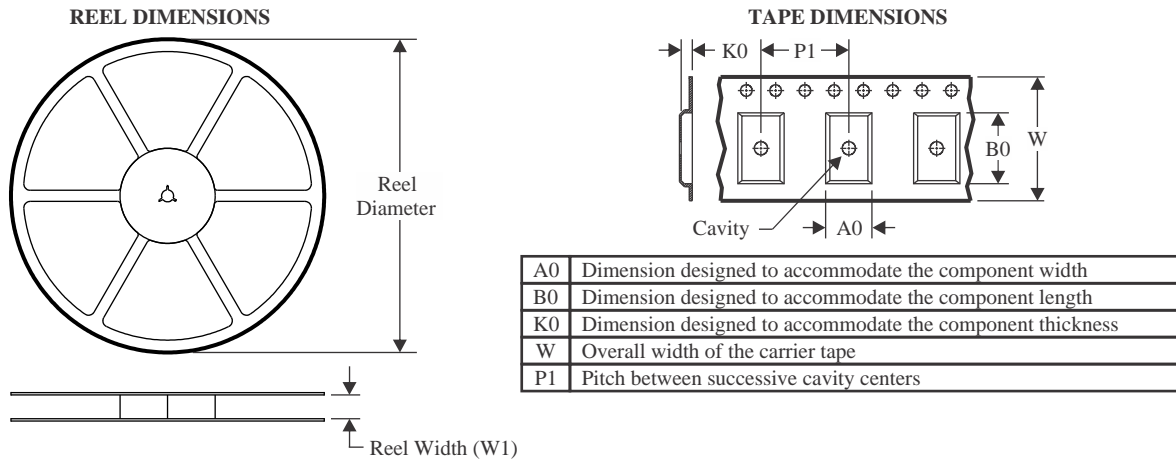
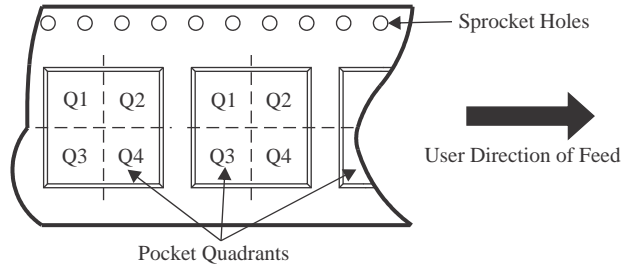
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS48110AQDGXRQ1	VSSOP	DGX	19	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
TPS48111LQDGXRQ1	VSSOP	DGX	19	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS48110AQDGXRQ1	VSSOP	DGX	19	5000	353.0	353.0	32.0
TPS48111LQDGXRQ1	VSSOP	DGX	19	5000	353.0	353.0	32.0

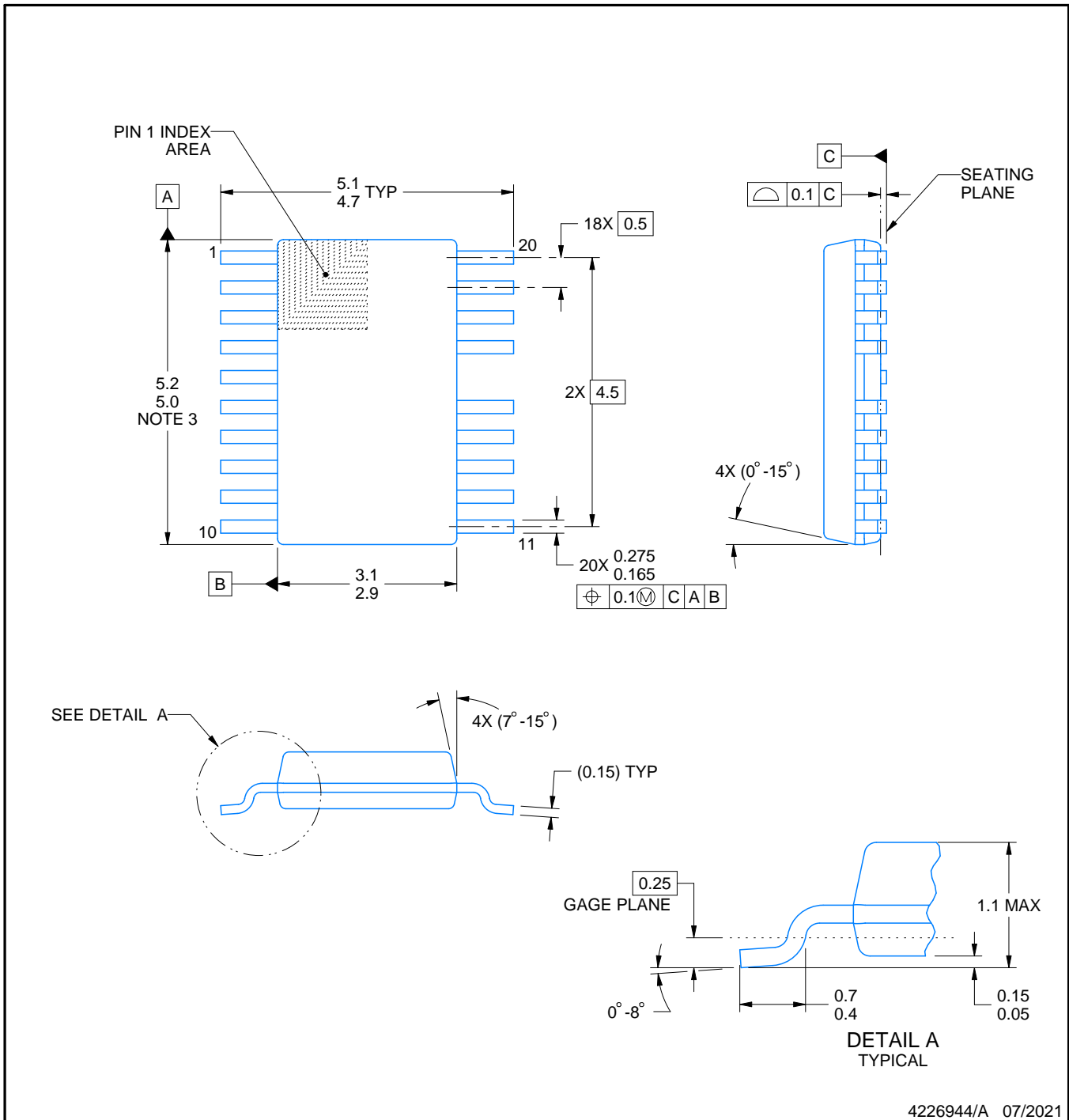
# DGX0019A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226944/A 07/2021

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of July 2021.
5. Features may differ or may not be present.

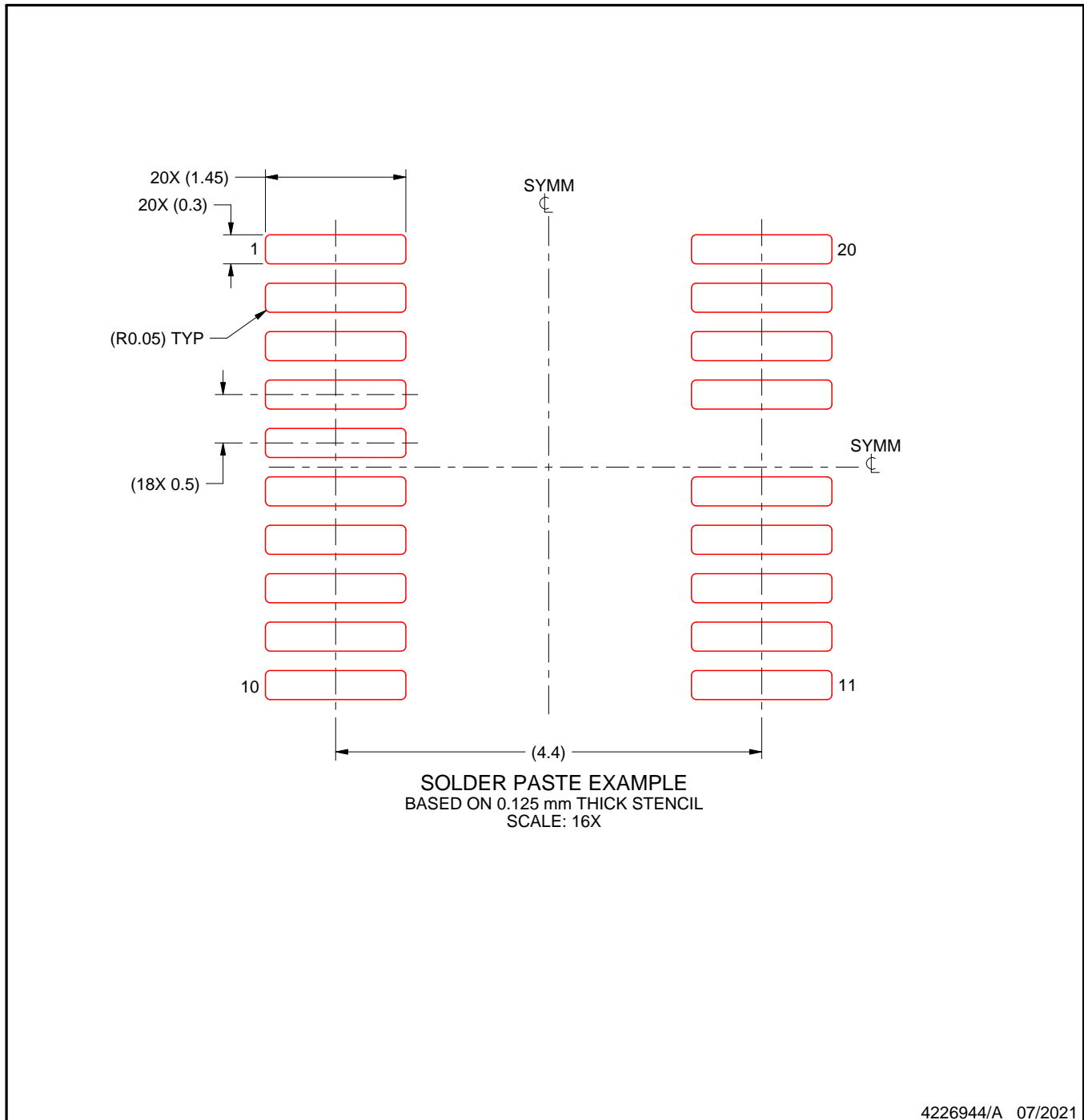


# EXAMPLE STENCIL DESIGN

DGX0019A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025