TPS53627 2-Phase, D-CAP+™ Step-Down Controller for VR13 CPU V_{CORE} and DDR Memory

1 Features

- Intel® VR13 Serial VID (SVID) Compliant
- 1- or 2-Phase Operation
- Supports Both Droop and Non-Droop Applications
- 8-Bit DAC with 10-mV Step
- 4.5-V to 28-V Conversion Voltage Range
- Output Range: 0.5 V to 2.3 V
- Optimized Efficiency at Light and Heavy Loads
- 8 Independent Levels of Overshoot Reduction (OSR) and Undershoot Reduction (USR)
- Driverless Configuration for Efficient High-Frequency Switching
- Supports Discrete, Power Block, Power Stage™ or DrMOS MOSFET Implementations
- Accurate, Adjustable Voltage Positioning
- 300-kHz to 1-MHz Frequency Selections
- Patented AutoBalance™ Phase Balancing
- Programmable ON-Pulse Extension for Load Transient Boost
- Programmable Auto DCM and CCM Operation
- Selectable 8-level Current Limit
- Small, 4 mm × 4 mm, 32-Pin, VQFN PowerPad™ Package

2 Applications

- VDDQ for DDR Memory
- SoC Processor V_{CORE} Power

3 Description

The TPS53627 device is a driverless, VR13 SVID compliant, synchronous buck controller. Advanced control features such as D-CAP+ ™architecture with overlapping pulse support undershoot reduction (USR) and overshoot reduction (OSR) to provide fast transient response, lowest output capacitance and high efficiency. The device also supports single-phase operation in CCM and DCM operation for light-load efficiency boost. The device integrates a full set of VR13 I/O features including VR_READY (PGOOD), ALERT and VR_HOT. The SVID interface address allows programming from 00h to 07h. Adjustable control of V_{OUT} slew rate can be programmed as high as 20mV/uS.

Paired with the TI NexFET™ Power Stage, this total solution delivers exceptionally high speed and low switching loss.

The TPS53627 device package is a space saving, thermally enhanced 32-pin VQFN package that operates from –40°C to +105°C.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS53627	VQFN (32)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the document.

Simplified Schematic

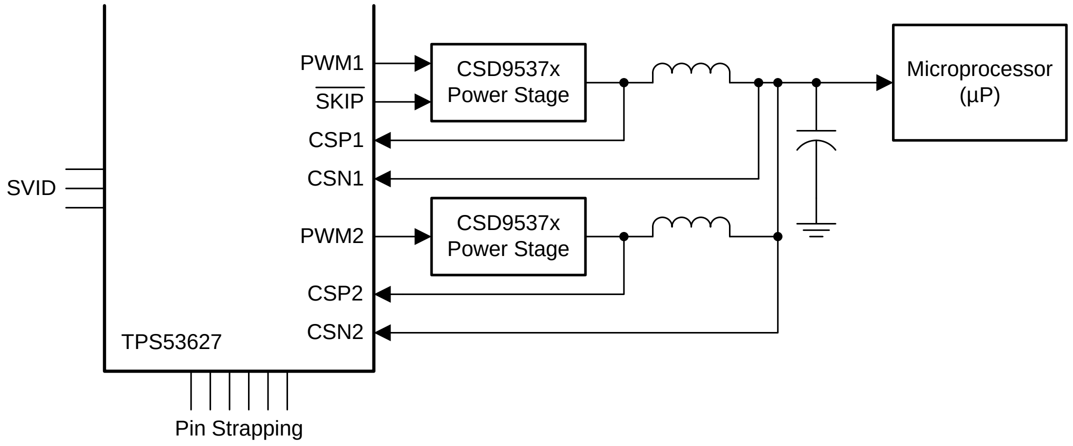

Table of Contents

4 Revision History

DATE	REVISION	NOTES
March 2017	*	Initial release.

5 Device and Documentation Support

5.1 Documentation Support

5.1.1 Related Documentation

For related documentation see the following:

TPS51604 Data Sheet

5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

5.4 Trademarks

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5.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

5.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS53627RSMR	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	TPS 53627
TPS53627RSMR.A	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	TPS 53627
TPS53627RSMR.B	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	TPS 53627
TPS53627RSMT	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	TPS 53627
TPS53627RSMT.A	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	TPS 53627
TPS53627RSMT.B	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	TPS 53627

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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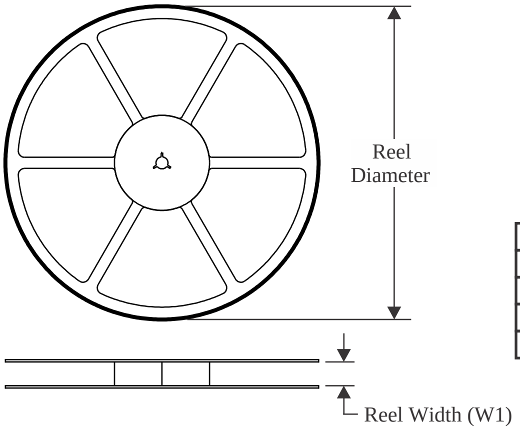
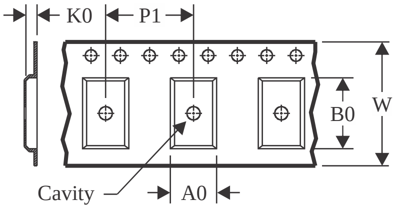
TAPE AND REEL INFORMATION

REEL DIMENSIONS

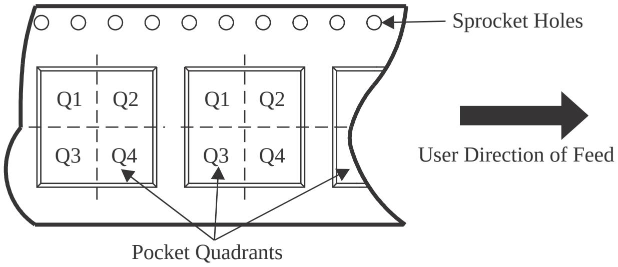


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

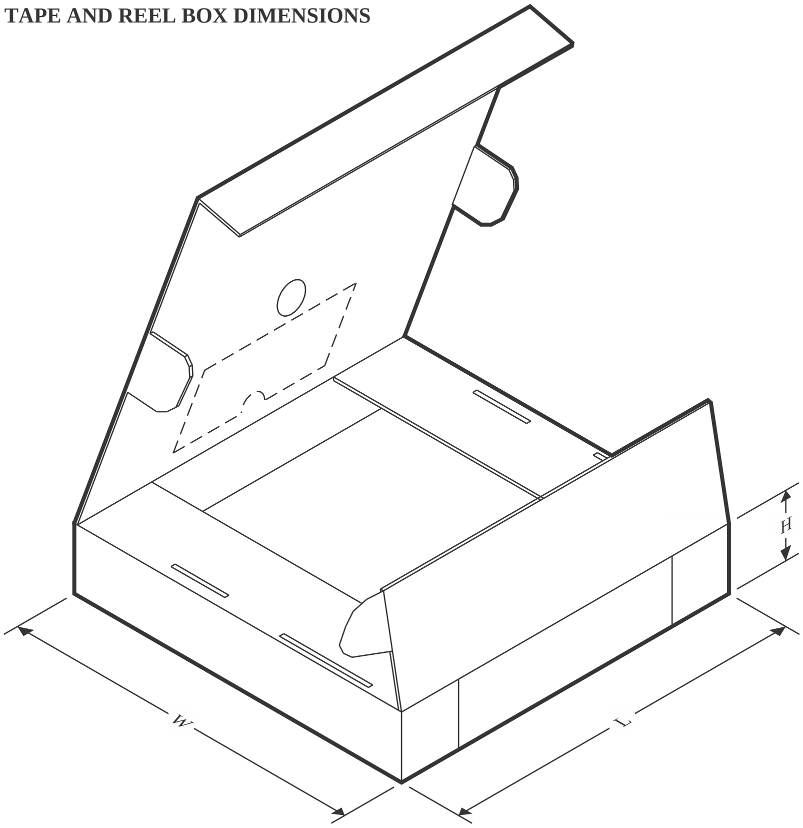
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53627RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS53627RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53627RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
TPS53627RSMT	VQFN	RSM	32	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

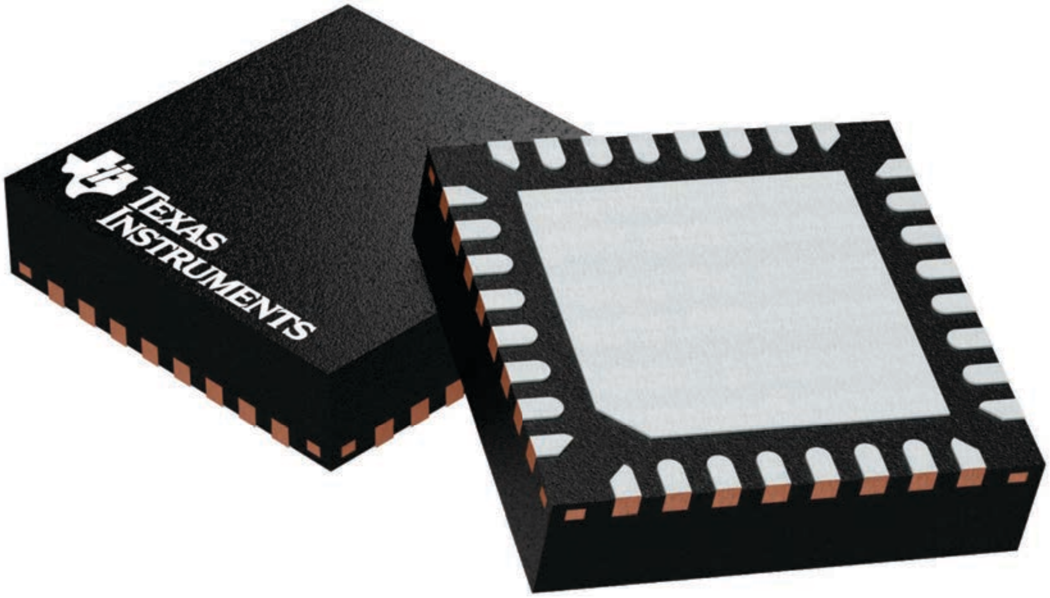
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

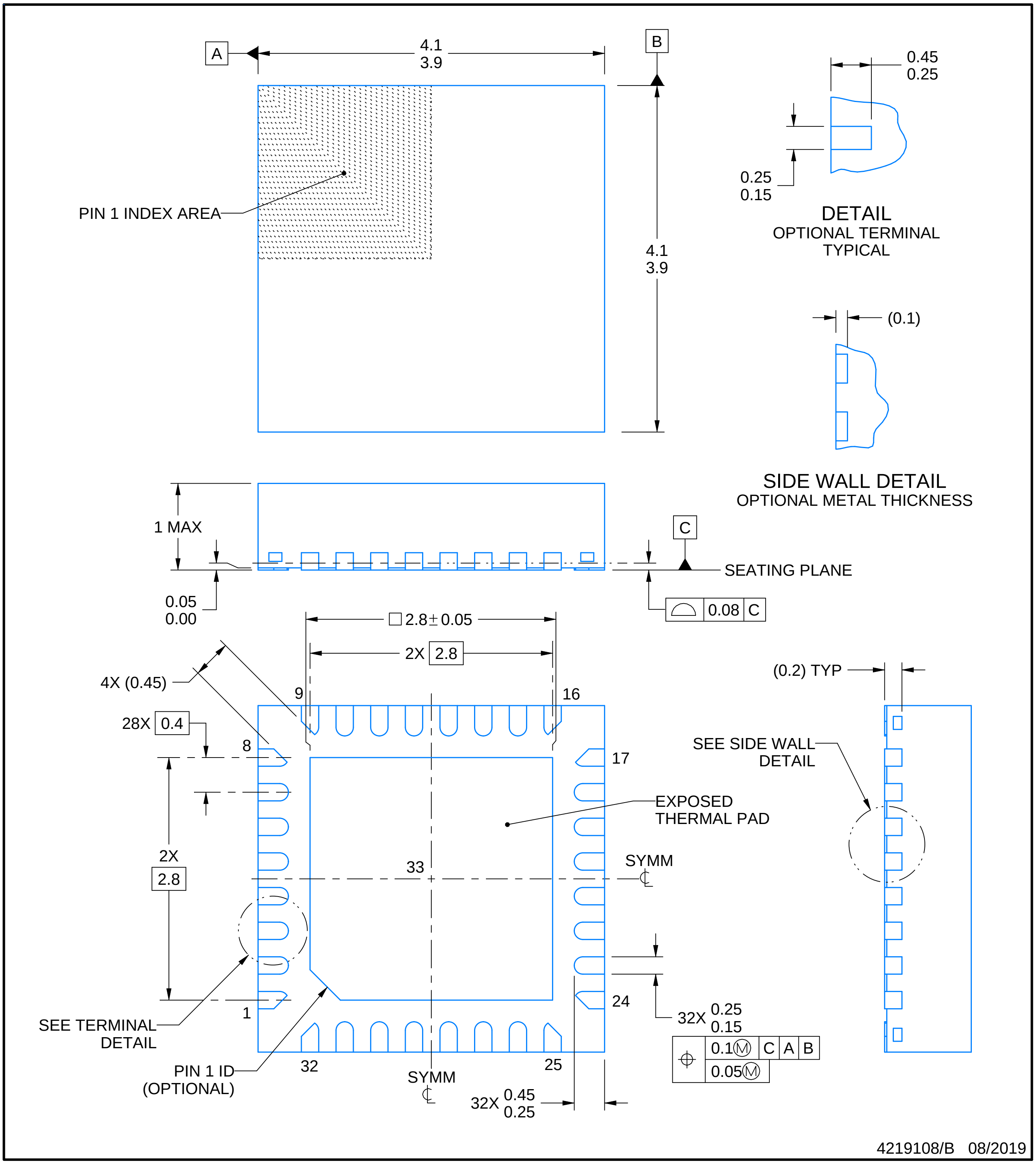


PACKAGE OUTLINE

RSM0032B

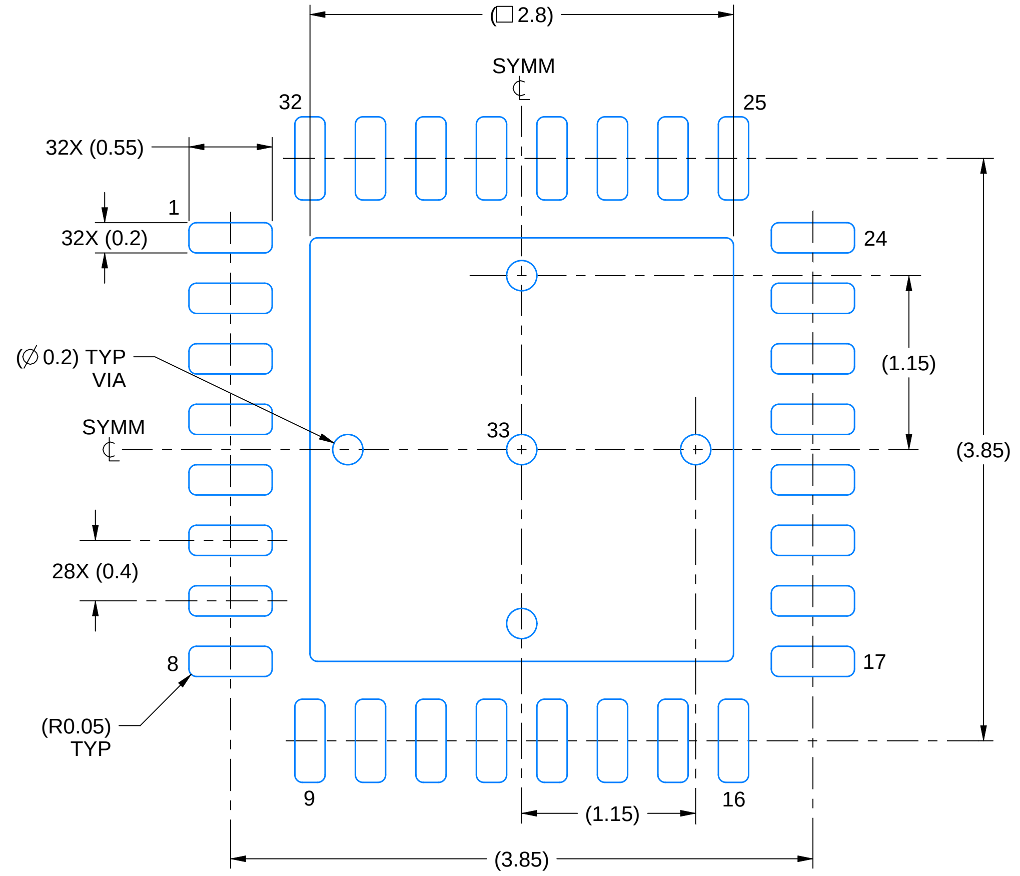
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

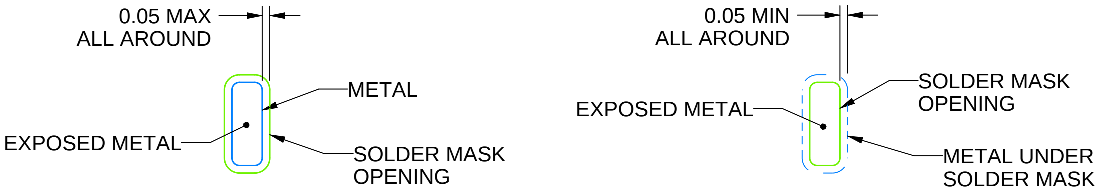


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

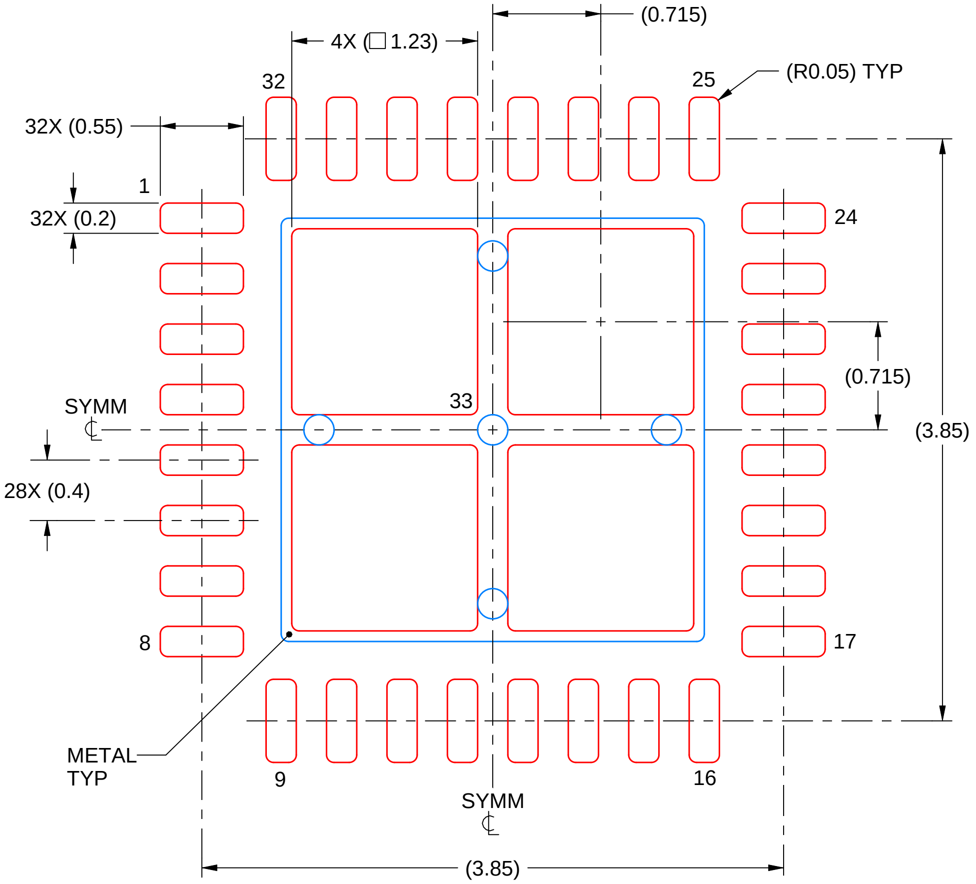
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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