2.2 – 4 -V, 14-A SYNCHRONOUS BUCK CONVERTER WITH DISABLED SINKING DURING START-UP

FEATURES

- **8-mΩ MOSFET Switches for High Efficiency at 14.5-A Peak Output Current**
- **Separate Low-Voltage Power Bus**
- **Disabled Current Sinking During Start-Up**
- **Adjustable Output Voltage Down to 0.9 V**
- **Wide PWM Frequency: Fixed 350 kHz, 550 kHz or Adjustable 280 kHz to 700 kHz**
- **Synchronizable to 700 kHz**
- **Load Protected by Peak Current Limit and Thermal Shutdown**
- **Integrated Solution Reduces Board Area and Total Cost**

APPLICATIONS

- **Low-Voltage, High-Density Distributed Power Systems**
- **Point of Load Regulation for High-Performance DSPs, FPGAs, ASICs, and Microprocessors**
- **Broadband, Networking, and Optical Communications Infrastructure**
- **Power PC Series Processors**

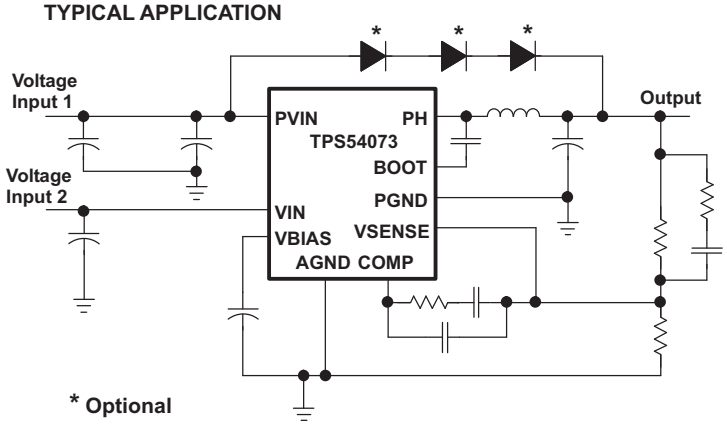
DESCRIPTION

As a member of the SWIFT™family of dc/dc regulators, the TPS54073 low-input voltage high-output current synchronous buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that enables maximum performance and flexibility in choosing the output filter L and C components; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally or externally set slow-start circuit to limit in-rush currents; and a power good output useful for processor/logic reset, fault signaling, and supply sequencing.

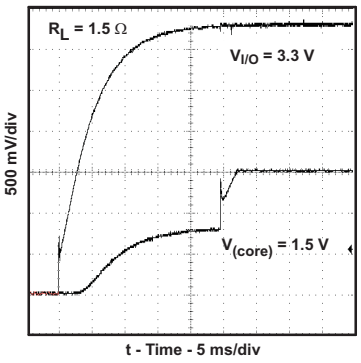
For reliable power up in output precharge applications, the TPS54073 is designed to only source current during start-up.

The TPS54073 is available in a thermally enhanced 28-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks. TI provides evaluation modules and the SWIFT™ designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles

TYPICAL APPLICATION



START-UP WAVEFORM WITH 3 PRECHARGE DIODES



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	OUTPUT VOLTAGE	PACKAGE	PART NUMBER
–40°C to 85°C	Adjustible down to 0.9 V	Plastic HTSSOP (PWP)(1)	TPS54073PWP

(1) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54073PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			TPS54073	UNIT
V_I	Input voltage range	SS/ENA, SYNC	–0.3 to 7	V
		RT	–0.3 to 6	
		VSENSE	–0.3 to 4	
		PVIN, VIN	–0.3 to 4.5	
		BOOT	–0.3 to 10	
V_O	Output voltage range	VBIAS, COMP, PWRGD	–0.3 to 7	V
		PH	–0.6 to 6	
V_O	Source current	PH	Internally limited	
		COMP, VBIAS	6	mA
I_S	Sink current	PH	25	A
		COMP	6	mA
		SS/ENA, PWRGD	10	
	Voltage differential	AGND to PGND	±0.3	V
T_J	Operating junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature range		–65 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage, VIN	3		4	V
	Power Input voltage, PVIN	2.2		4	V
T_J	Operating junction temperature	–40		125	C

DISSIPATION RATINGS(1)(2)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
28-Pin PWP with solder	14.87°C/W	6.72 W(3)	3.69 W	2.69 W
28-Pin PWP without solder(4)	27.9°C/W	3.58 W	1.97 W	1.43 W

(1) For more information on the PWP package, see TI technical brief, literature number SLMA002.
(2) Test board conditions:
  a. 3 inch × 3 inch, 4 layers, thickness = 0.062 inch
  b. 2-ounce copper traces located on die top of the PCB.
  c. 2-ounce copper mixed plane and traces on the bottom of the PCB.
  d. 2-ounce copper ground planes on the two internal layers of the PCB.
  e. 12 thermal vias (see the Figure 11 in the *Application Section* of this data sheet.
(3) Maximum power dissipation may be limited by over current protection.
(4) Estimated performance

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, VIN = 3 V to 4 V, PVIN = 2.2 V to 4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN							
V_I	Input voltage, VIN			3		4	V
	Supply voltage range, PVIN		Output = 1.8 V	2.2		4	V
I_Q	Quiescent current	VIN = 3.3 V	f_s = 350 kHz, RT open, PH pin open, SYNC = 0 V, PVIN = 2.5 V		6.3	10	mA
			f_s = 550 kHz, RT open, PH pin open, SYNC ≥ 2.5 V, PVIN = 2.5 V		8.6	13	mA
			SHUTDOWN, SS/ENA = 0 V, PVIN = 2.5 V		1	1.4	mA
		PVIN = 2.5 V	f_s = 350 kHz, RT open, PH pin open, SYNC = 0 V, VIN = 3.3 V		3.2	6	mA
			f_s = 550 kHz, RT open, PH pin open, SYNC ≥ 2.5 V, VIN = 3.3 V		4.4	7	mA
			SHUTDOWN, SS/ENA = 0 V, VIN = 3.3 V		< 140		µA
UNDERVOLTAGE LOCKOUT (VIN)							
	Start threshold voltage, UVLO				2.9	3	V
	Stop threshold voltage, UVLO			2.7	2.8		V
	Hysteresis voltage, UVLO				100		mV
	Rising and falling edge deglitch, UVLO(1)				2.5		µs
BIAS VOLTAGE							
	Output voltage, VBIAS		$I_{(VBIAS)}$ = 0	2.7	2.8	2.9	V
	Output current, VBIAS(2)					100	µA
CUMULATIVE REFERENCE							
V_{ref}	Accuracy			0.882	0.891	0.900	V
REGULATION							
	Line regulation(3)(4)		I_L = 7 A, f_s = 350 kHz, T_J = 85°C		0.05		%/V
	Load regulation(3)(4)		I_L = 0 A to 14 A, f_s = 350 kHz, T_J = 85°C PVIN = 2.5 V, VIN = 3.3 V		0.013		%/A
OSCILLATOR							
	Internally set—free running frequency		RT open(3), SYNC ≤ 0.8 V	280	350	420	kHz
			RT open(3), SYNC ≥ 2.5 V	440	550	660	
	Externally set—free running frequency range		RT = 180 kΩ (1% resistor to AGND)(3)	252	280	308	kHz
			RT = 100 kΩ (1% resistor to AGND)	460	500	540	
			RT = 68 kΩ (1% resistor to AGND)(3)	663	700	762	
	High-level threshold voltage, SYNC			2.5			V
	Low-level threshold voltage, SYNC					0.8	V
	Pulse duration, SYNC(3)			50			ns
	Frequency range, SYNC			300		700	kHz
	Ramp valley(3)				0.75		V
	Ramp amplitude (peak-to-peak)(3)				1		V
	Minimum controllable on time(3)					200	ns
	Maximum duty cycle(3)			90%			

(1) Specified by design
(2) Static resistive loads only
(3) Specified by design
(4) Specified by the circuit used in Figure 12

ELECTRICAL CHARACTERISTICS (continued)

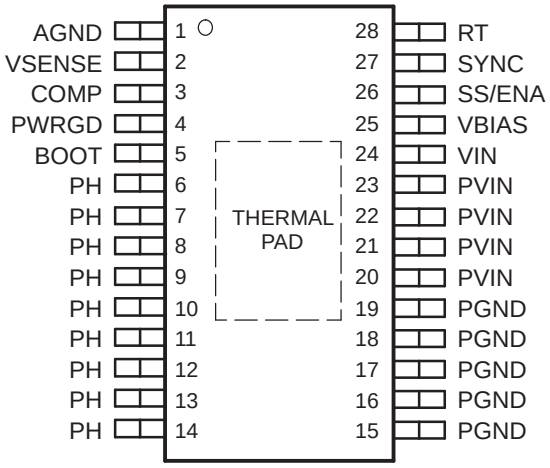
T_J = –40°C to 125°C, VIN = 3 V to 4 V, PVIN = 2.2 V to 4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
	Error amplifier open-loop voltage gain	1 kΩ COMP to AGND(5)	90	110		dB
	Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND(5)	3	5		MHz
	Error amplifier common mode input voltage range	Powered by internal LDO(5)	0		VBIAS	V
	Input bias current, VSENSE	VSENSE = V_{ref}		60	250	nA
	Output voltage slew rate (symmetric), COMP		1	1.4		V/µs
PWM COMPARATOR						
	PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime)	10-mV overdrive(5)		70	85	ns
SLOW-START/ENABLE						
	Enable threshold voltage, SS/ENA		0.82	1.2	1.4	V
	Enable hysteresis voltage, SS/ENA(5)			0.03		V
	Falling edge deglitch, SS/ENA(5)			2.5		µs
	Internal slow-start time		2.6	3.35	4.1	ms
	Charge current, SS/ENA	SS/ENA = 0 V	2	5	8	µA
	Discharge current, SS/ENA	SS/ENA = 0.2 V, VIN = 2.7 V, PVIN = 2.5 V	1.3	2.3	4	mA
POWER GOOD						
	Power-good threshold voltage	VSENSE falling		93		%V_{ref}
	Power-good hysteresis voltage(5)			3		%V_{ref}
	Power-good falling edge deglitch(5)			35		s
	Output saturation voltage, PWRGD	$I_{(sink)}$ = 2.5 mA		0.18	0.3	V
	Leakage current, PWRGD	VIN = 3.3 V, PVIN = 2.5 V			1	µA
CURRENT LIMIT						
	Current limit	VIN = 3.3 V, PVIN = 2.5 V (5), Output shorted	14.5	21		A
	Current limit leading edge blanking time(5)			100		ns
	Current limit total response time(5)			200		ns
THERMAL SHUTDOWN						
	Thermal shutdown trip point(5)		135	165		°C
	Thermal shutdown hysteresis(5)			10		°C
OUTPUT POWER MOSFETS						
$r_{DS(on)}$	Power MOSFET switches	VIN = 3 V, PVIN = 2.5 V		8	21	mΩ
		VIN = 3.6 V, PVIN = 2.5 V		8	18	

(5) Specified by design

DEVICE INFORMATION

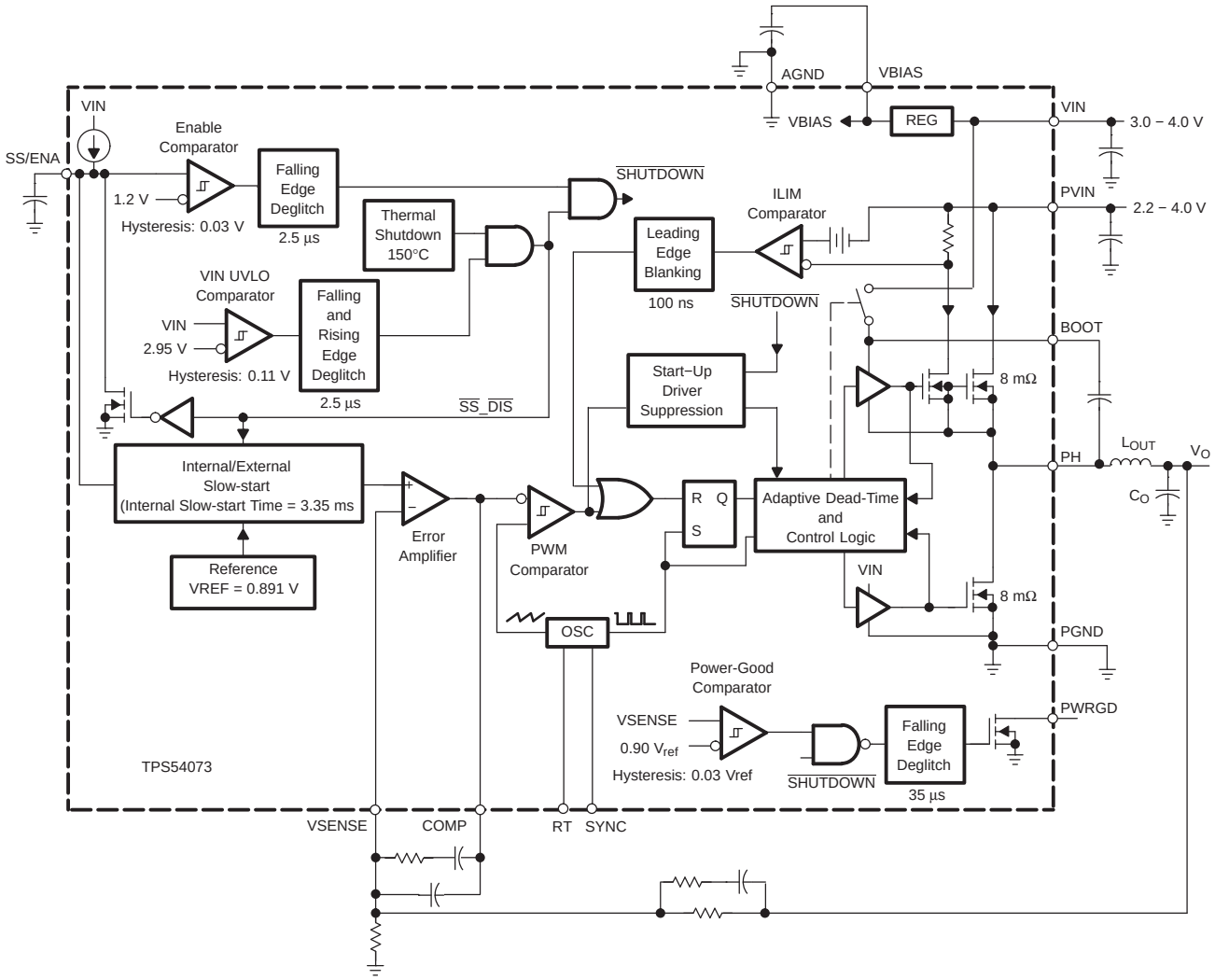
PWP PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

PIN NAME	PIN NUMBER	DESCRIPTION
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, and RT resistor. If using the PowerPAD, connect it to AGND. See the *Application Information* section for details.
BOOT	5	Bootstrap output. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE
PGND	15, 16, 17, 18, 19	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	6-14	Phase output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
PVIN	20, 21, 22, 23	Input supply for the power MOSFET switches and internal bias regulator. Bypass the PVIN pins to the PGND pins close to device package with a high-quality, low-ESR 10-µF ceramic capacitor.
PWRGD	4	Power-good open-drain output. High when VSENSE > 90% V_{ref}, otherwise PWRGD is low. Note that output is low when SS/ENA is low or the internal shutdown signal is active.
RT	28	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f_s.
SS/ENA	26	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
SYNC	27	Synchronization input. Dual function pin which provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin.
VBIAS	25	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high-quality, low-ESR 0.1-µF to 1.0-µF ceramic capacitor.
VIN	24	Input supply for the internal control circuits. Bypass the VIN pin to the PGND pins close to device package with a high-quality, low-ESR 1-µF ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect to output voltage compensation network/output divider.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE VS JUNCTION TEMPERATURE

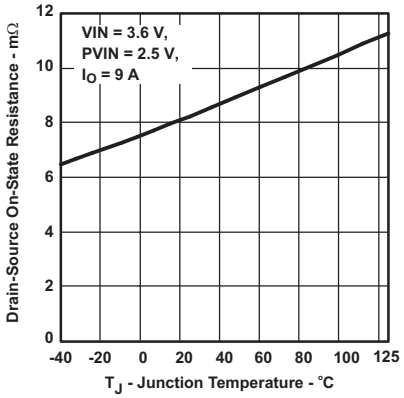


Figure 1.

DRAIN-SOURCE ON-STATE RESISTANCE VS JUNCTION TEMPERATURE

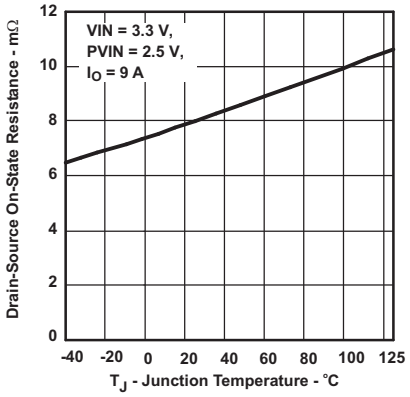


Figure 2.

INTERNALLY SET OSCILLATOR FREQUENCY VS JUNCTION TEMPERATURE

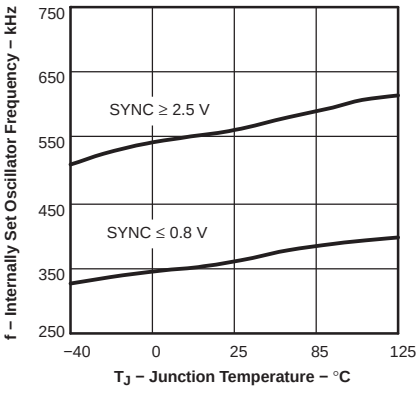


Figure 3.

TYPICAL CHARACTERISTICS (continued)

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

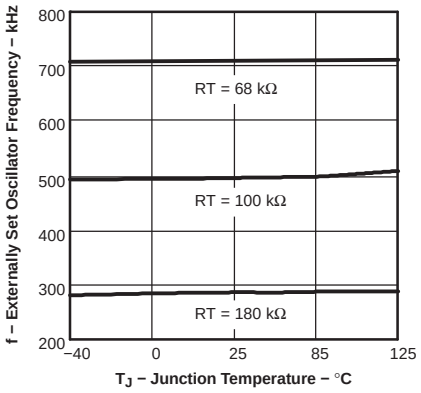


Figure 4.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

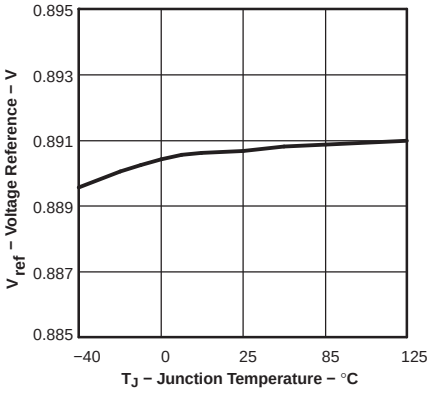


Figure 5.

DEVICE POWER DISSIPATION vs OUTPUT CURRENT

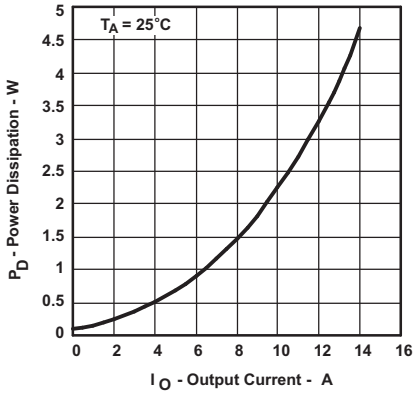


Figure 6.

REFERENCE VOLTAGE vs INPUT VOLTAGE

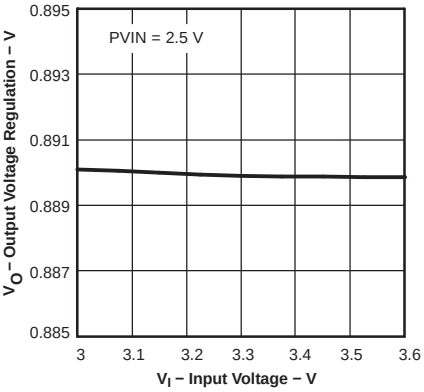


Figure 7.

ERROR AMPLIFIER OPEN-LOOP RESPONSE

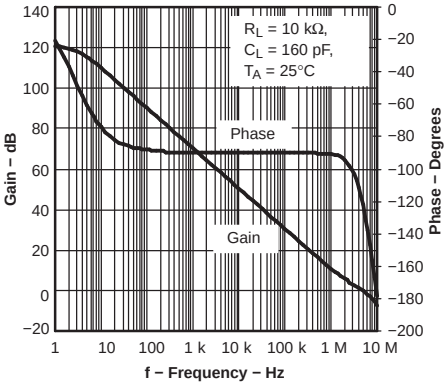


Figure 8.

INTERNAL SLOWS-START TIME vs JUNCTION TEMPERATURE

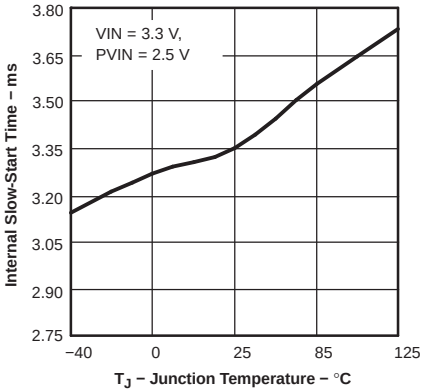


Figure 9.

APPLICATION INFORMATION

PCB LAYOUT

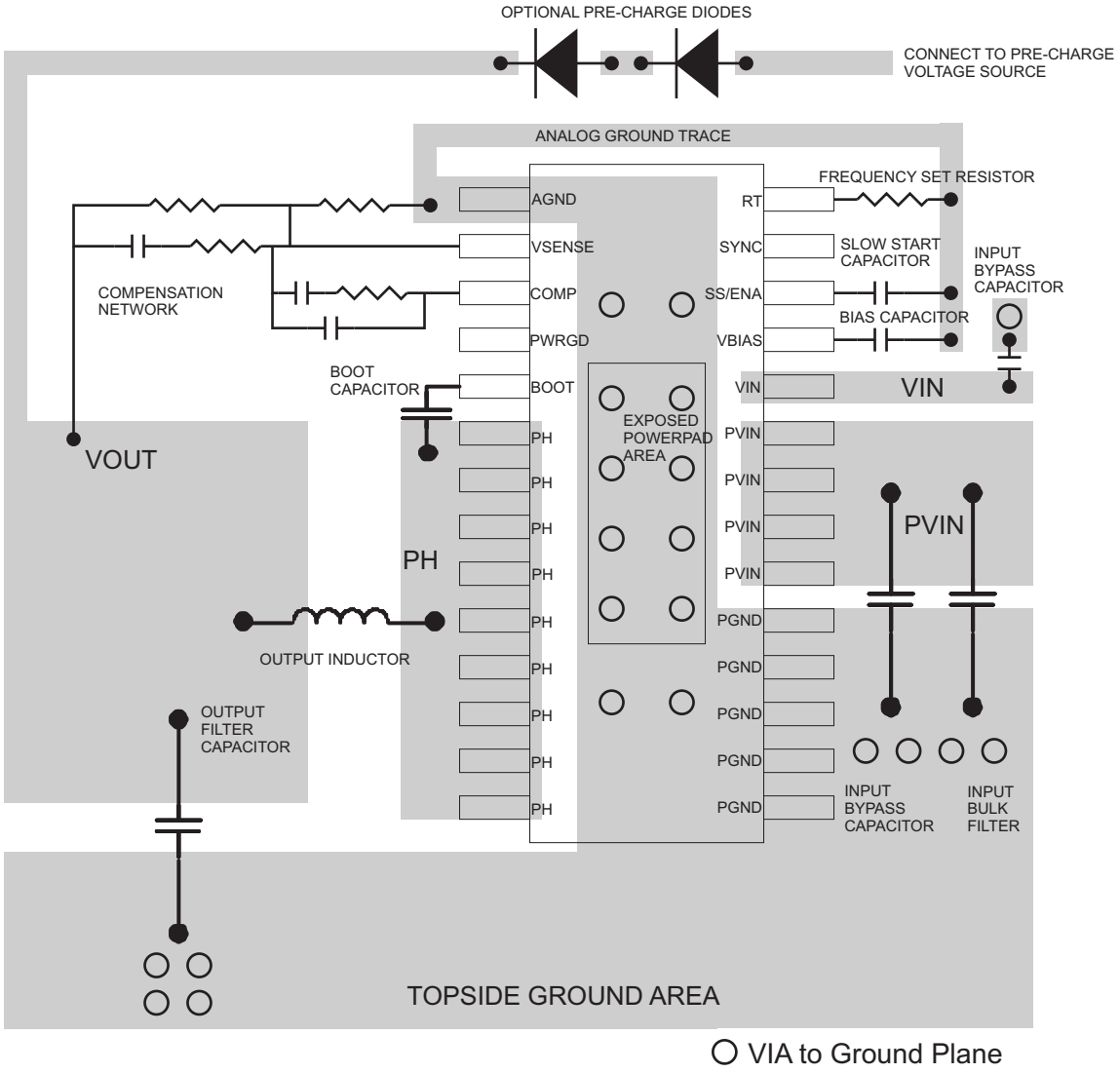


Figure 10. TPS54073 Layout

The PVIN pins are connected together on the printed-circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the TPS54073 ground pins. The minimum recommended bypass capacitance is a 10-µF ceramic capacitor with a X5R or X7R dielectric. The optimum placement is as close as possible to the PVIN pins, the AGND, and PGND pins. See Figure 10 for an example of a board layout. If the VIN is connected to a separate source supply, it is bypassed with its own capacitor. There is an area of ground on the top layer of the PCB, directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors. The AGND and PGND pins are tied to the PCB ground by connecting them to the ground area under the device as shown in Figure 10. Use a separate wide trace for the analog ground signal path. This analog ground is used for the voltage set point divider, timing resistor RT, slow-start capacitor, and bias capacitor grounds. The PH pins are tied together and routed to the output inductor. Because the PH connection is the switching node, an inductor is located close to the PH pins, and the area of the PCB conductor is minimized to prevent excessive capacitive coupling. Connect the boot capacitor between the phase node and the BOOT pin as shown in Figure 10. Keep the boot capacitor close to the IC, and minimize the conductor trace lengths.

Connect the output filter capacitor(s) between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins, Lout, Cout, and PGND as small as is practical. Place the compensation components from the VOUT trace to the VSENSE and COMP pins. Do not place these components too close to the PH trace. Due to the size of the IC package and the device pinout, they must be routed close, but maintain as much separation as possible while keeping the layout compact. Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace. If a slow-start capacitor or RT resistor is used, or if the SYNC pin is used to select 350-kHz operating frequency, connect them to this trace.

Optional prebias diodes should be connected between the output voltage trace and the prebias source. The source is VIN, PVIN, or some other voltage rail. This is dependent on the user's application circuit. In some cases, the diodes are not required if the prebias voltage is caused by an external load circuit leakage path.

For operation at full rated load current, the analog ground plane must provide an adequate heat-dissipating area. A 3-inch by 3-inch plane of 1-ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD must be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available must be used when 6-A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer must be made using 0.013-inch diameter vias to avoid solder wicking through the vias.

Eight vias must be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the twelve recommended that enhance thermal performance must be included in areas not under the device package.

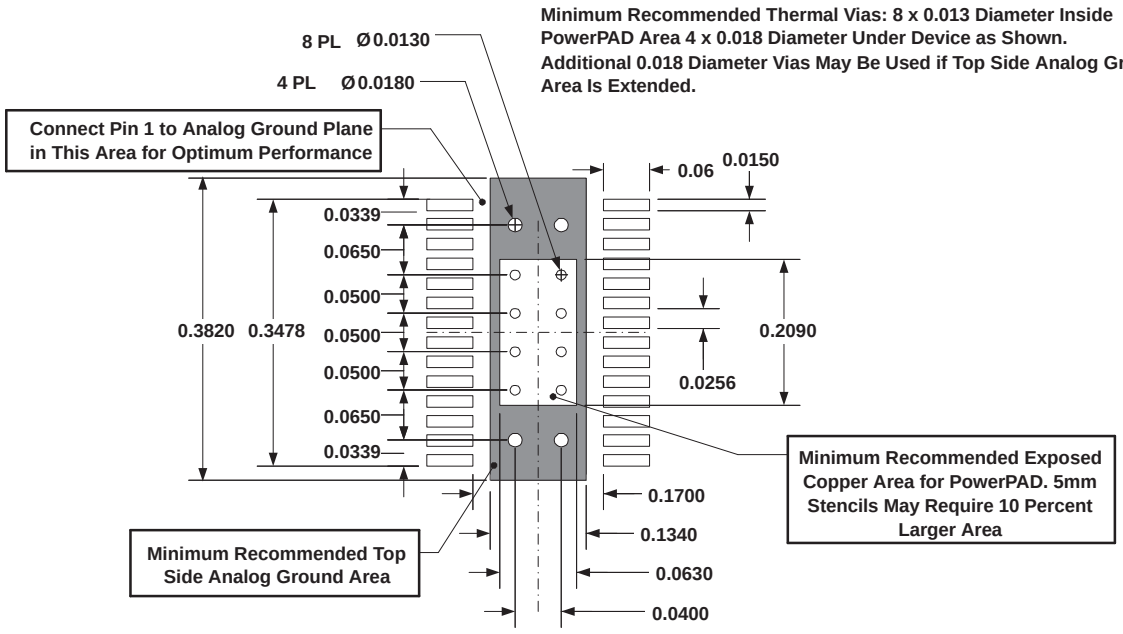


Figure 11. Recommended Land Pattern for 28-Pin PWP PowerPAD

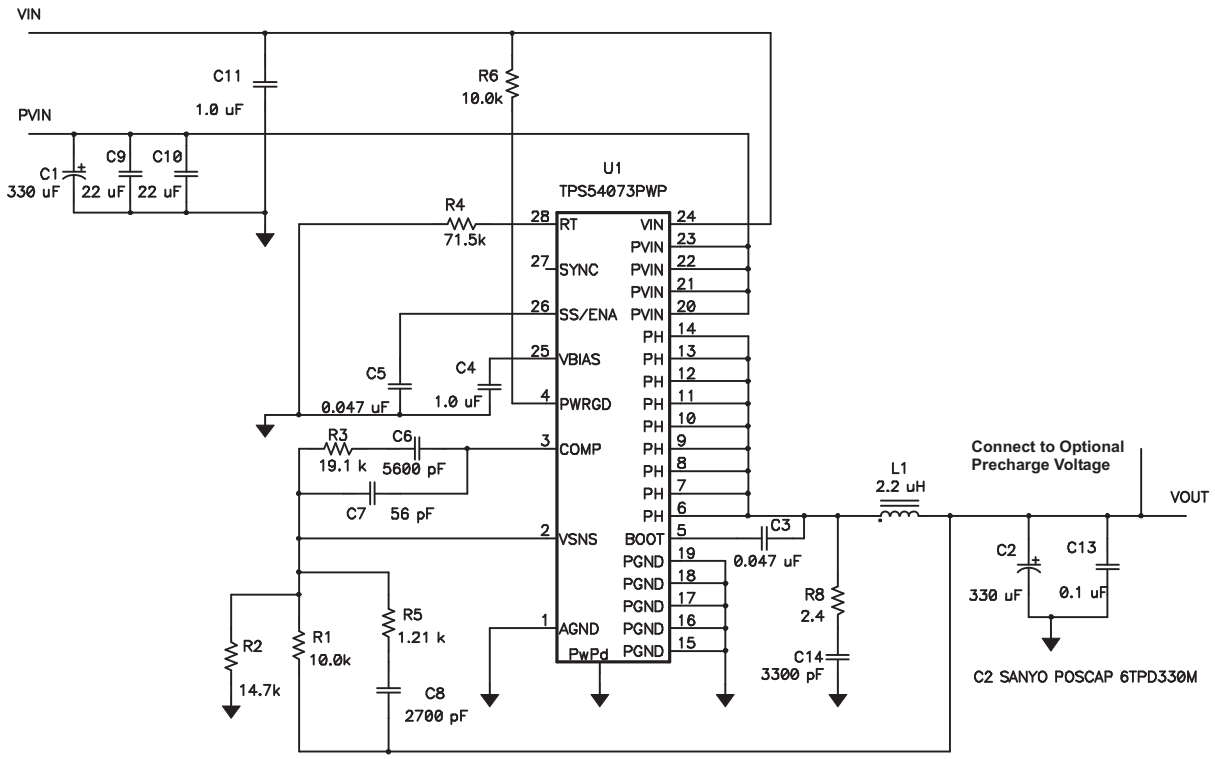


Figure 12. Application Circuit, 3.3 V to 1.5 V

Figure 12 shows the schematic for a typical TPS54073 application. The TPS54073 provides up to 14-A output current at a nominal output voltage of 1.5 V. Nominal input voltages are 3.3 V for PVIN, and 3.3 V for VIN. For proper thermal performance, the exposed PowerPAD underneath the device must be soldered to the printed-circuit board.

DESIGN PROCEDURE

The following design procedure is used to select component values for the TPS54073. Alternately, the SWIFT Designer Software is used to generate a complete design. The SWIFT Designer Software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

DESIGN PARAMETERS

To begin the design process, a few parameters must be decided. The designer needs to know:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

For this design example, use the following as the input parameters:

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage (VIN)	3.3 V
Input voltage range (PVIN)	2.2 to 3.5 V
Output voltage	1.5 V
Input ripple voltage	350 mV
Output ripple voltage	20 mV
Output current rating	14 A
Operating frequency	700 kHz

SWITCHING FREQUENCY

The switching frequency can be set to either one of two internally programmed frequencies or set to a externally programmed frequency. With the RT pin open, setting the SYNC pin at or above 2.5 V selects 550-kHz operation, while grounding or leaving the SYNC pin open selects 350-kHz operation. For this design, the switching frequency is externally programmed using the RT pin. By connecting a resistor (R4) from RT to AGND, any frequency in the range of 250 kHz to 700 kHz can be set. Use Equation 1 to determine the proper value of RT.

$$R4(k\Omega) = \frac{500\ kHz}{fs(kHz)} \times 100\ k\Omega \quad (1)$$

In this example circuit, R4 is calculated to be 71.5 kΩ and the switching frequency is set at 700 kHz.

INPUT CAPACITORS

The TPS54073 requires an input de-coupling capacitor and, depending on the application, a bulk input capacitor. The minimum value for the de-coupling capacitor, C9, is 10 µF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. Additionally, some bulk capacitance may be needed, especially if the TPS54073 circuit is not located within approximately 2 inches from the input voltage source. The value for this capacitor is not critical but it also should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable.

This input ripple voltage can be approximated by Equation 2:

$$\Delta V_{PVIN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum load current. f_{sw} is the switching frequency, $C_{(BULK)}$ is the bulk capacitor value and ESR_{MAX} is the maximum series resistance of the bulk capacitor.

The maximum RMS ripple current also needs to be checked. For worst-case conditions, this can be approximated by Equation 3:

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (3)$$

In this case, the input ripple voltage would be 329 mV and the RMS ripple current would be 7 A. The maximum voltage across the input capacitors would be Vin max plus delta Vin/2. The chosen bulk capacitor, a Sanyo POSCAP 6TPD330M is rated for 6.3 V and 4.4 A of ripple current; two bypass capacitors, TDK C3225X7R1C226KT are each rated for 16 V, and the ripple current capacity is greater than 3 A at the operating frequency of 700 kHz. Total ripple current handling is in excess of 10.4 A. It is important that the maximum ratings for voltage and current are not exceeded under any circumstance.

OUTPUT FILTER COMPONENTS

Two components need to be selected for the output filter, L1 and C2. Because the TPS54073 is an externally compensated device, a wide range of filter component types and values can be supported.

Inductor Selection

To calculate the minimum value of the output inductor, use Equation 4

$$L_{MIN} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW}\ x\ 0.8} \quad (4)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. For designs using low ESR output capacitors such as ceramics, use K_{IND} = 0.3. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results. If designing for high output currents, the minimum current limit trip point must also be taken into consideration when choosing the output inductor. The minimum current limit trip point for the TPS54073 is 14.5 A. The maximum inductor ripple current can be calculated using Equation 5:

$$I_{LMAX} \le 2 \times \left(I_{LIMIT(MIN)} - I_{(MAX)}\right) \quad (5)$$

For a 14 A maximum output current, the peak-to-peak inductor ripple current must be less than 1 A. This corresponds to a K_{IND} of 0.071 in Equation 4.

F_{SW} is the nominal switching frequency. Use 0.8 times the nominal switching frequency to account for internal variations from the set frequency.

The minimum inductor value is calculated to be 1.54 µH. A 2.2-µH inductor which is slightly larger than the minimum is selected.

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from Equation 6:

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left[V_{OUT} \times \frac{\left(V_{in(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{sw} \times 0.8}\right]^2} \quad (6)$$

and the peak inductor current can be found from Equation 7

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} \times V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{sw} \times 0.8} \quad (7)$$

For this design, the RMS inductor current is 14.001 A, and the peak inductor current is 14.43 A. The Vishay IHLP5050CZ-01 style output inductor with a value of 2.2 µH meets these current requirements. Increasing the inductor value decreases the ripple current and the corresponding output ripple voltage. The inductor value can be decreased if more margin in the RMS current is required. In general, inductor values for use with the TPS54073 falls in the range of 1 µH to 3.3 µH, depending on the maximum required output current.

Capacitor Requirements

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed-loop crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the closed-loop crossover frequency at less than 1/5 of the switching frequency. With high switching frequencies such as the 700 kHz frequency of this design, internal circuit limitations of the TPS54073 limit the practical maximum crossover frequency to about 70 kHz. To allow for adequate phase gain in the compensation network, the LC corner frequency should be about one decade or so below the closed-loop crossover frequency. This limits the minimum capacitor value for the output filter to:

$$C_{OUT(MIN)} = \frac{1}{L_{OUT}} \times \left(\frac{K}{2\pi f_{CO}}\right)^2 \quad (8)$$

Where K is the frequency multiplier for the spread between f_{LC} and f_{CO}. K should be between 5 and 15, typically 10 for one decade difference. For a desired crossover of 40-kHz and a 2.2-µH inductor, the minimum value for the output capacitor is 304 µF using a minimum K factor of 6.5. Increasing the K factor would require using a larger capacitance. The selected output capacitor must be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any de-rating amount must also be included. The maximum RMS ripple current in the output capacitors is given by Equation 9:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left[\frac{V_{OUT} \times \left(V_{PVIN(MAX)} - V_{OUT}\right)}{V_{PVIN(MAX)} \times L_{OUT} \times F_{SW}}\right] \quad (9)$$

The calculated RMS ripple current is 201 mA in the output capacitors.

The maximum ESR of the output capacitor is determined by the amount of allowable output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter; therefore, the maximum specified ESR as listed in the capacitor data is given by Equation 10 :

$$ESR_{MAX} = N_C \times \left[\frac{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}\right] \times \Delta V_{P-P(MAX)} \quad (10)$$

and the maximum ESR required is 29 mΩ. A capacitor that meets these requirements is a Cornell Sanyo POSCAP 6TPD33M rated at 6.3 V with a maximum ESR of 0.015 Ω and a ripple current rating of 2 A. An additional small 0.1-µF ceramic bypass capacitor C13 is a also used.

Other capacitor types work well with the TPS54073, depending on the needs of the application.

Compensation Components

The external compensation used with the TPS54073 allows for a wide range of output filter configurations. A large range of capacitor values and types of dielectric are supported. The design example uses Type-3 compensation consisting of R1, R3, R5, C6, C7, and C8. Additionally, R2 along with R1 forms a voltage divider network that sets the output voltage. These component reference designators are the same as those used in the SWIFT Designer Software. There are a number of different ways to design a compensation network. This procedure outlines a relatively simple procedure that produces good results with most output filter combinations. Use the SWIFT Designer Software for designs with unusually high closed-loop crossover frequencies, low value, low ESR output capacitors such as ceramics or if you are unsure about the design procedure.

When designing compensation networks for the TPS54073, a number of factors need to be considered. The gain of the compensated error amplifier should not be limited by the open-loop amplifier gain characteristics and should not produce excessive gain at the switching frequency. Also, the closed-loop crossover frequency should be set less than one-fifth of the switching frequency, and the

phase margin at crossover must be greater than 45 degrees. The general procedure outlined here produces results consistent with these requirements without going into great detail about the theory of loop compensation.

First, calculate the output filter LC corner frequency using Equation 11:

$$f_{LC} = \frac{1}{2\pi \sqrt{L_{OUT} C_{OUT}}} \quad (11)$$

For the design example, f_{LC} = 5.906 kHz.

The closed-loop crossover frequency should be chosen to be greater than f_{LC} and less than one-fifth of the switching frequency. Also, the crossover frequency should not exceed 100 kHz, as the error amplifier may not provide the desired gain. For this design, a crossover frequency of 40 kHz was chosen. This value is chosen for comparatively wide loop bandwidth while still allowing for adequate phase boost to insure stability.

Next, calculate the R2 resistor value for the output voltage of 1.5 V using Equation 12:

$$R2 = \frac{R1 \times 0.891}{V_{OUT} - 0.891} \quad (12)$$

For any TPS54073 design, start with an R1 value of 10 kΩ. R2 is 14.7 kΩ.

Now, the values for the compensation components that set the poles and zeros of the compensation network can be calculated. Assuming that R1 >> than R5 and C6 >> C7, the pole and zero locations are given by Equation 13 through Equation 20:

$$f_{Z1} = \frac{1}{2\pi R3 C6} \quad (13)$$

$$f_{Z2} = \frac{1}{2\pi R1 C8} \quad (14)$$

$$f_{P1} = \frac{1}{2\pi R5 C8} \quad (15)$$

$$f_{P2} = \frac{1}{2\pi R3 C7} \quad (16)$$

Additionally, there is a pole at the origin, which has unity gain at a frequency:

$$f_{INT} = \frac{1}{2\pi R1 C6} \quad (17)$$

This pole is used to set the overall gain of the compensated error amplifier and determines the closed-loop crossover frequency. Because R1 is given as 10 kΩ and the nominal crossover frequency is selected as 40 kHz, the desired f_{INT} can be calculated from Equation 18:

$$f_{INT} = \frac{f_{CO} \times f_{Z1} \times f_{Z2}}{V_{IN(NOM)} \times f_{LC}^{\,2}} \quad (18)$$

For this design, one zero is placed at f_{LC} and the other at one fourth f_{LC}, so Equation 18 simplifies to:

$$f_{INT} = \frac{f_{CO}}{V_{IN(NOM)} \times 4} \quad (19)$$

It is important to note that these equations are only valid for the pole and zero locations as specified

The value for C6 is given by Equation 20:

$$C6 = \frac{1}{2\pi R1 f_{INT}} \quad (20)$$

The first zero, f_{Z1} is located at one-half the output filter LC corner frequency; so, R3 can be calculated from:

$$R3 = \frac{1}{\pi C6 f_{LC}} \quad (21)$$

The second zero, f_{Z2} is located at the output filter LC corner frequency; so, C8 can be calculated from:

$$C8 = \frac{1}{2\pi R1 f_{LC}} \quad (22)$$

The first pole, f_{P1} is located to coincide with output filter ESR zero frequency. This frequency is given by:

$$f_{ESR0} = \frac{1}{2\pi R_{ESR} C_{OUT}} \quad (23)$$

where R_{ESR} is the equivalent series resistance of the output capacitor.

In this case, the ESR zero frequency is 48.2 kHz, and R5 can be calculated from:

$$R5 = \frac{1}{2\pi C8 f_{ESR}} \quad (24)$$

The final pole is placed at a frequency above the closed-loop crossover frequency high enough to not cause the phase to decrease too much at the crossover frequency while still providing enough attenuation so that there is little or no gain at the switching frequency. The f_{P2} pole location for this circuit is set to 150 kHz and the last compensation component value C7 can be derived:

$$C7 = \frac{1}{2\pi R3 \times 150000} \quad (25)$$

Note that capacitors are only available in a limited range of standard values, so the nearest standard value has been chosen for each capacitor. The measured closed-loop response for this design is shown in Figure 5.

BIAS AND BOOTSTRAP CAPACITORS

Every TPS54073 design requires a bootstrap capacitor, C3, and a bias capacitor, C4. The bootstrap capacitor must be a 0.1 µF. The bootstrap capacitor is located between the PH pins and BOOT. The bias capacitor is connected between the VBIAS pin and AGND. The value should be 1.0 µF. Both capacitors should be high-quality ceramic types with X7R or X5R grade dielectric for temperature stability. They should be placed as close to the device connection pins as possible.

POWER GOOD

The TPS54073 is provided with a power-good output pin PWRGD. This output is an open-drain output and is intended to be pulled up to a 3.3-V logic supply. A 10-kΩ pullup works well in this application. The absolute maximum voltage is 6 V, so care must be taken not to connect this pull up to Vin if the maximum input voltage exceeds 6 V.

SNUBBER CIRCUIT

R8 and C14 of the application schematic comprise a snubber circuit. The snubber is included to reduce over-shoot and ringing on the phase node when the internal high side FET turns on. Since the frequency and amplitude of the ringing depends to a large degree on parasitic effects, it is best to choose these component values based on actual measurements of any design layout. See literature number SLUP100 for more detailed information on snubber design

DESIGN WITH CERAMIC CAPACITORS

Figure 13 shows an application where all ceramic capacitors, including the main output filter capacitor, are used. The compensation network components were calculated using SWIFT Designer Software. See Figure 23 through Figure 26 for loop response, performance graphs, and switching waveforms for this circuit.

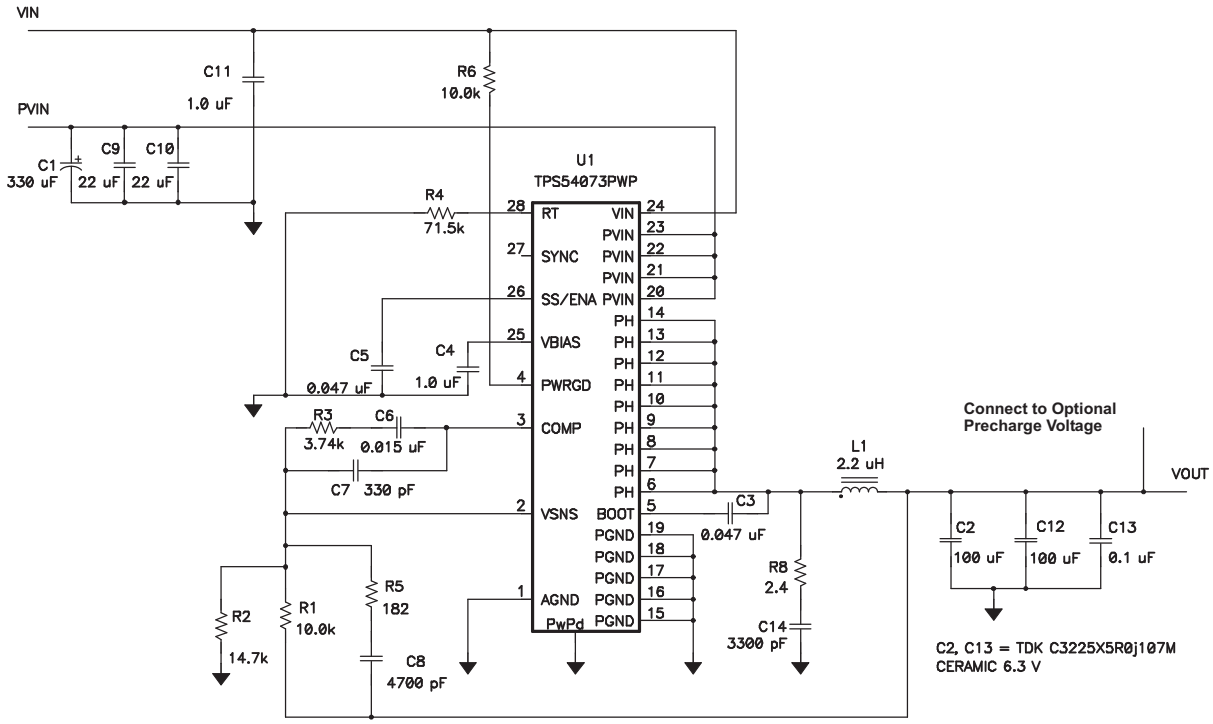


Figure 13. 1.5 V Power Supply With Ceramic Output Capacitors

PERFORMANCE GRAPHS

The performance data for Figure 14 through Figure 22 are for the circuit in Figure 12. Conditions are PVIN = 2.5 V, VIN = 3.3 V, V_O = 1.5 V, f_s = 700 kHz, and I_O = 7 A, T_A = 25°C, unless otherwise specified.

MEASURED LOOP RESPONSE VS FREQUENCY

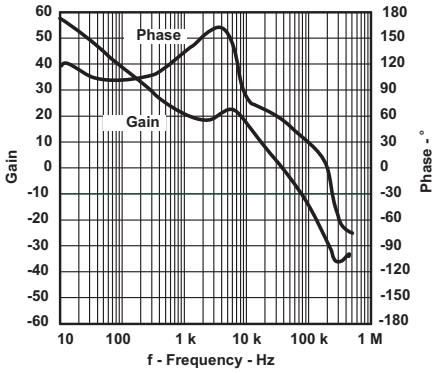


Figure 14.

LOAD REGULATION VS OUTPUT CURRENT

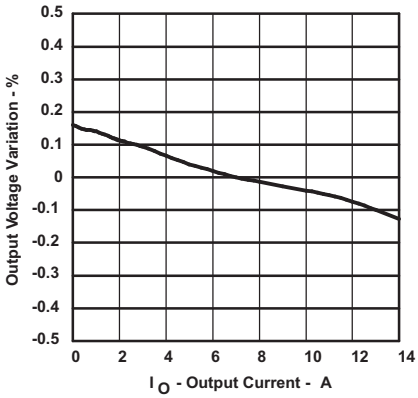


Figure 15.

LINE REGULATION VS INPUT VOLTAGE

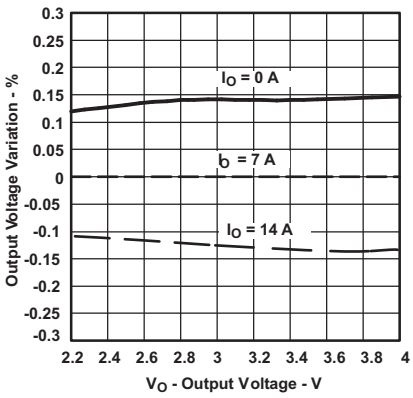


Figure 16.

EFFICIENCY VS OUTPUT CURRENT

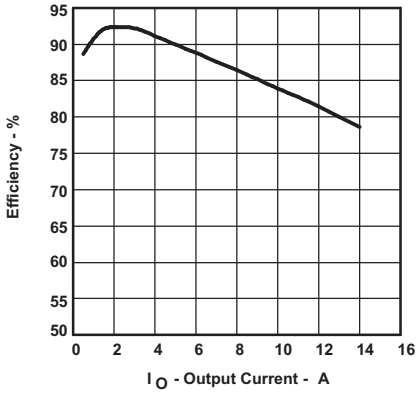


Figure 17.

INPUT RIPPLE VOLTAGE

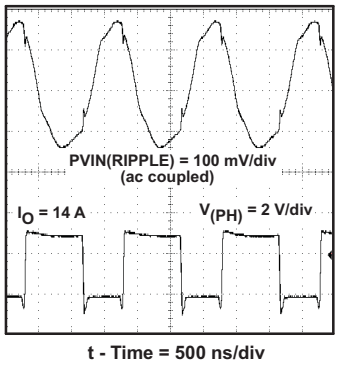


Figure 18.

OUTPUT VOLTAGE RIPPLE

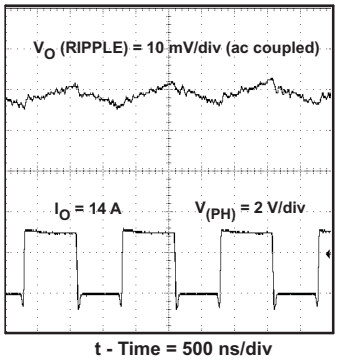


Figure 19.

LOAD TRANSIENT RESPONSE

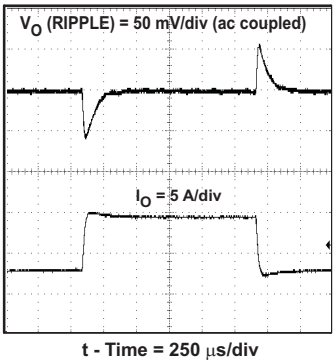


Figure 20.

START-UP WAVEFORM WITH PRECHARGE

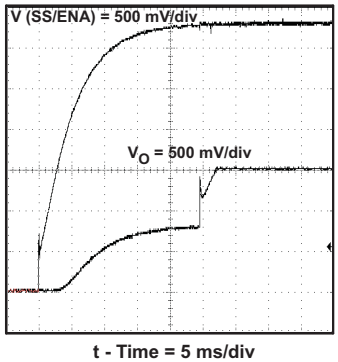


Figure 21.

OUTPUT INDUCTOR RIPPLE CURRENT

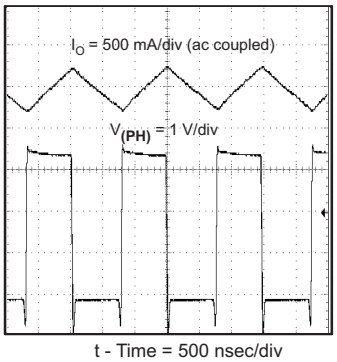


Figure 22.

PERFORMANCE GRAPHS (continued)

The performance data for Figure 23 through Figure 26 are for the circuit in Figure 13. Conditions are PVIN = VIN = 3.3 V, V_O = 1.5 V, f_s = 700 kHz, and I_O = 7 A, T_A = 25C, unless otherwise specified.

MEASURED LOOP RESPONSE VS FREQUENCY

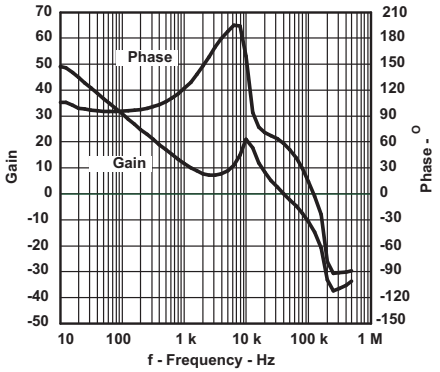


Figure 23.

OUTPUT VOLTAGE RIPPLE

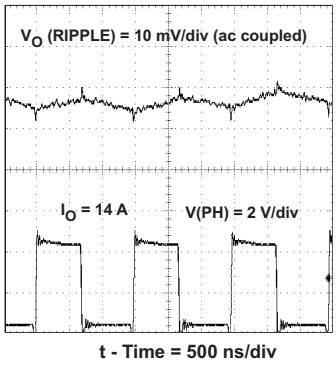


Figure 24.

LOAD TRANSIENT RESPONSE

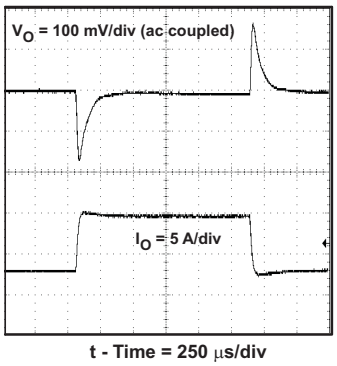


Figure 25.

FREE-AIR TEMPERATURE VS OUTPUT CURRENT

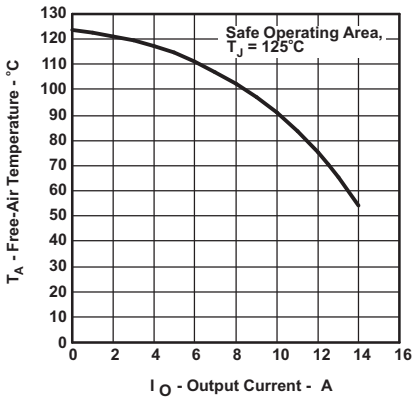


Figure 26.

DETAILED DESCRIPTION

OPERATING WITH SEPARATE PVIN

The TPS54073 is designed to operate with the power stage (high-side and low-side MOSFETs) and the PVIN input connected to a separate power source from VIN. The primary intended application has VIN connected to a 3.3-V bus and PVIN connected to a 2.5-V bus. The TPS54073 cannot be damaged by any sequencing of these voltages. However, the UVLO (see detailed description section) is referenced to the VIN input. Some conditions may cause undesirable operation.

If PVIN is absent when the VIN input is high, the slow-start is released, and the PWM circuit goes to maximum duty factor. When the PVIN input ramps up, the output of the TPS54073 follows the PVIN input until enough voltage is present to regulate to the proper output value.

NOTE:

If the PVIN input is controlled via a fast bus switch, it results in a hard-start condition and may damage the load (i.e., whatever is connected to the regulated output of the TPS54073). If a power-good signal is not available from the 2.5-V power supply, one can be generated using a comparator and hold the SS/ENA pin low until the 2.5-V bus power is good. An example of this is shown in Figure 27. This circuit can also be used to prevent the TPS54073 output from following the PVIN input while the PVIN power supply is ramping up.

DISABLED SINKING DURING START-UP (DSDS)

The DSDS feature enables minimal voltage drooping of output precharge capacitors at start-up. The TPS54073 is designed to disable the low-side MOSFET to prevent sinking current from a precharge output capacitor during start-up. Once the high-side MOSFET has been turned on to the maximum duty cycle limit, the low-side MOSFET is allowed to switch. Once the maximum duty cycle condition is met, the converter functions as a sourcing converter until the SS/ENA is pulled low.

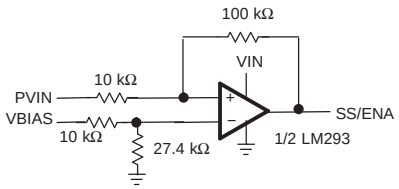


Figure 27. Undervoltage Lockout Circuit for PVIN Using Open-Collector or Open-Drain Comparator

PVIN and VIN can be tied together for 3.3-V bus operation.

MAXIMUM OUTPUT VOLTAGE

The maximum attainable output voltage is limited by the minimum voltage at the PVIN pin. Nominal maximum duty cycle is limited to 90% in the TPS54073; so, maximum output voltage is:

$$V_{O(max)} = PVIN_{(min)} \times 0.9 \quad (26)$$

Care must be taken while operating when nominal conditions cause duty cycles near 90%. Load transients can require momentary increases in duty cycle. If the required duty cycle exceeds 90%, the output may fall out of regulation.

GROUNDING AND PowerPAD LAYOUT

The TPS54073 has two internal grounds (analog and power). Inside the TPS54073, the analog ground ties to all of the noise-sensitive signals, whereas the power ground ties to the noisier power signals. The PowerPAD must be tied directly to AGND. Noise injected between the two grounds can degrade the performance of the TPS54073, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground planes are recommended. These two planes must tie together directly at the IC to reduce noise between the two grounds. The only components that must tie directly to the power ground plane are the input capacitor, the output capacitor, the input voltage de-coupling capacitor, and the PGND pins of the TPS54073.

UNDERVOLTAGE LOCKOUT (UVLO)

The TPS54073 incorporates an undervoltage-lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-µs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN. UVLO is with respect to VIN and not PVIN, see the *Application Information* section.

SLOW-START/ENABLE (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start-up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-µs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND.

Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ V}{5\ \mu A} \tag{27}$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ V}{5\ \mu A} \tag{28}$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

VBIAS REGULATOR (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high-quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor must be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.7 V, and external loads on VBIAS with ac or digital-switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits. VBIAS is derived from the VIN pin; see the functional block diagram of this data sheet.

VOLTAGE REFERENCE

The voltage reference system produces a precise V_{ref} signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high-precision regulation of the TPS54073, because it cancels offset errors in the scale and error amplifier circuits.

OSCILLATOR AND PWM RAMP

The oscillator frequency is set to an internally fixed value of 350 kHz. The oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor between the RT pin to ground. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100\ \text{k}\Omega}{\text{R}} \times 500\ [\text{kHz}] \tag{29}$$

ERROR AMPLIFIER

The high-performance, wide bandwidth, voltage error amplifier sets the TPS54073 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type-2 or Type-3 compensation can be employed using external compensation components.

PWM CONTROL

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control-logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp. During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54073 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

DEAD-TIME CONTROL AND MOSFET DRIVERS

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. While the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V.

The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, whereas the high-side driver is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

OVERCURRENT PROTECTION

The cycle-by-cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold. The high-side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading-edge blanking circuit prevents current limit false tripping. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

THERMAL SHUTDOWN

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the slow-start circuit, heating up due to the fault condition, and then shutting down on reaching the thermal shutdown trip point. This sequence repeats until the fault condition is removed.

POWER-GOOD (PWRGD)

The power-good circuit monitors for undervoltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or SS/ENA is low. When VIN, UVLO threshold, SS/ENA, enable threshold, and VSENSE > 90% of V_{ref}, the open-drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35-µs falling-edge deglitch circuit prevent tripping of the power-good comparator due to high-frequency noise.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54073PWP	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS54073
TPS54073PWP.A	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS54073
TPS54073PWPG4	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS54073

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

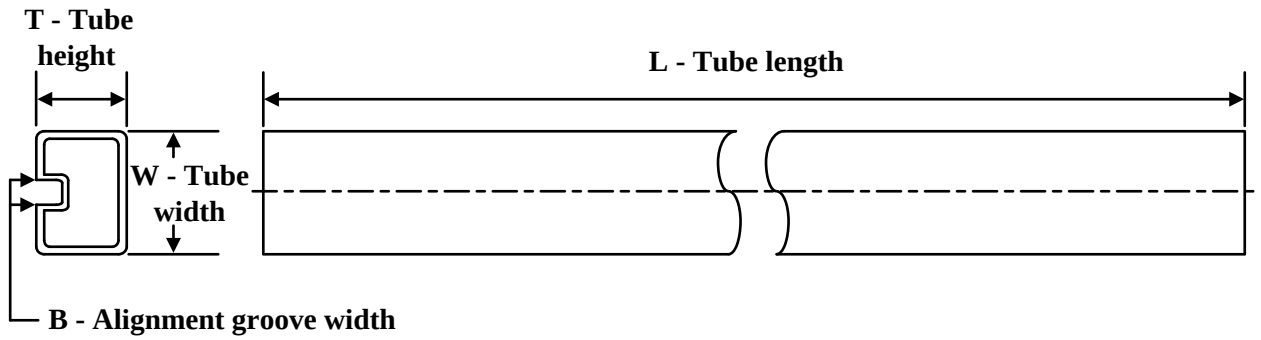
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54073PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPS54073PWP.A	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPS54073PWPG4	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

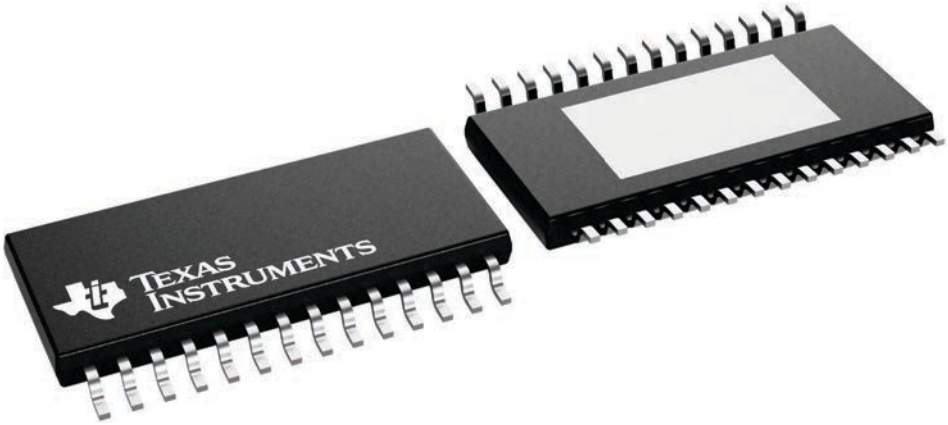
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

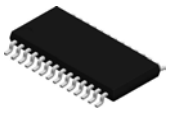
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

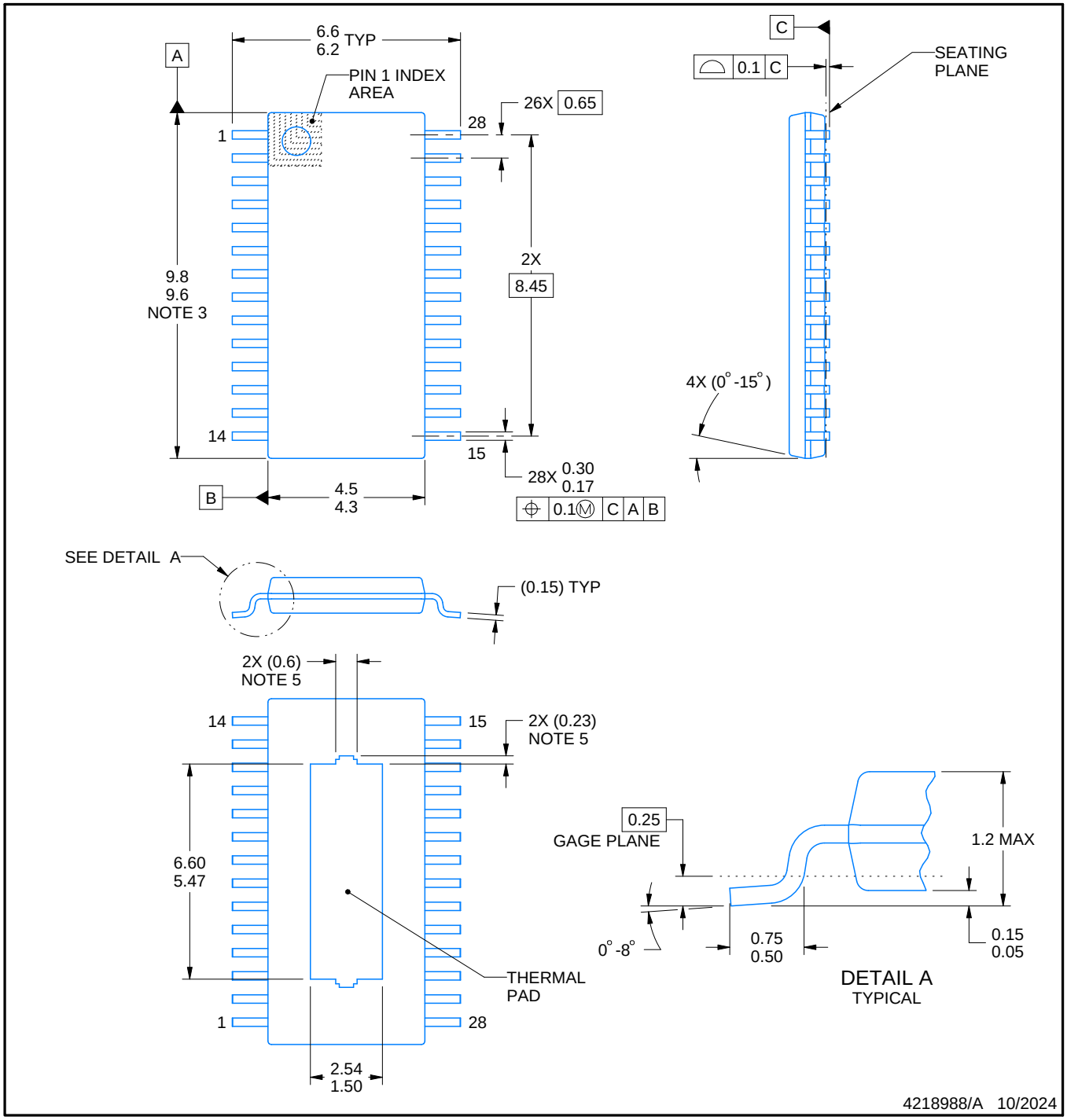
PACKAGE OUTLINE

PWP0028D



PowerPAD™ TSSOP - 1.2 mm max height

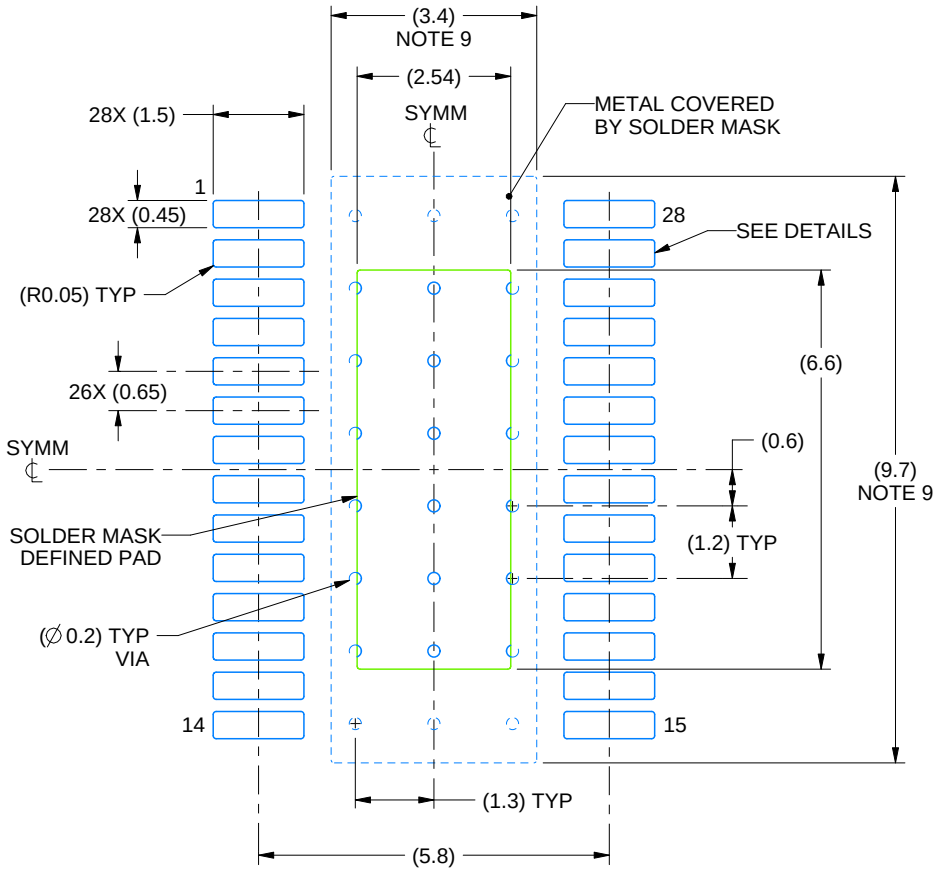
SMALL OUTLINE PACKAGE



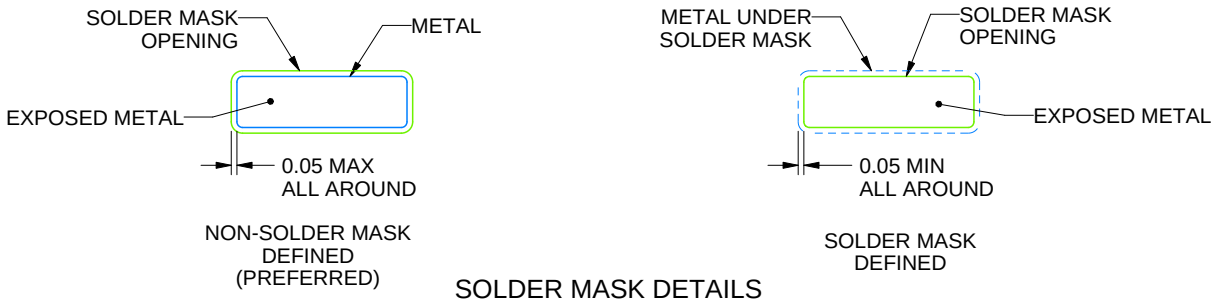
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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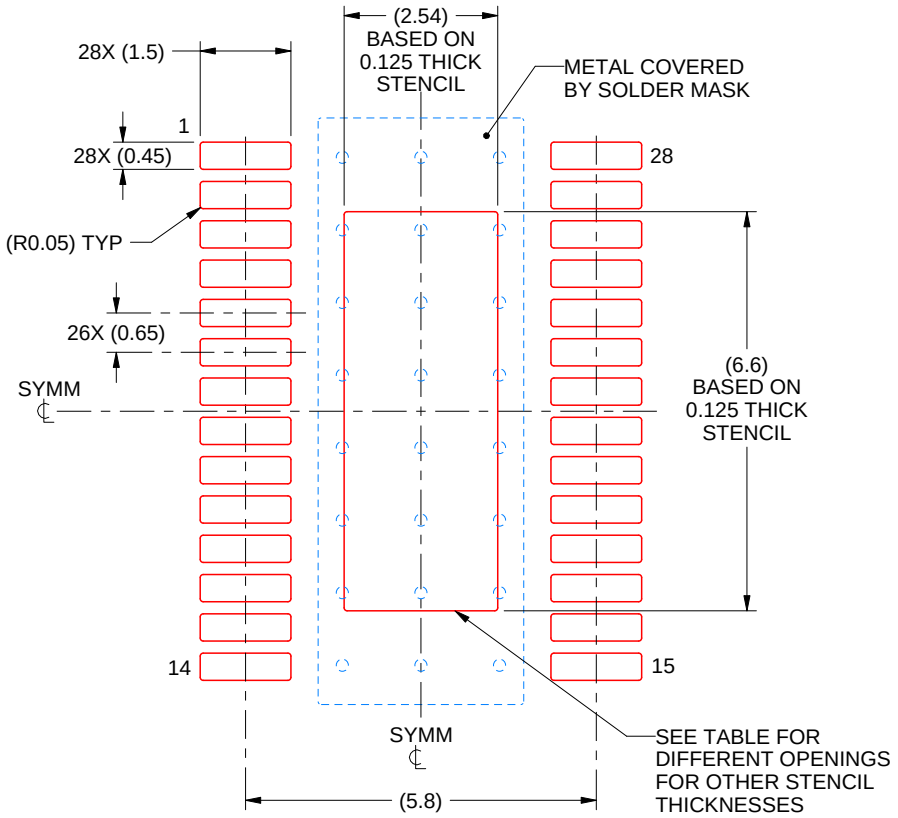
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.84 X 7.38
0.125	2.54 X 6.60 (SHOWN)
0.15	2.32 X 6.02
0.175	2.15 X 5.58

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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