TPS54620 4.5-V to 17-V Input, 6-A, Synchronous, Step-Down SWIFT™ Converter

1 Features

- Integrated 26 mΩ and 19 mΩ MOSFETs
- Split Power Rail: 1.6 V to 17 V on PVIN
- 200-kHz to 1.6-MHz Switching Frequency
- Synchronizes to External Clock
- 0.8 V ±1% Voltage Reference Overtemperature
- Low 2-µA Shutdown Quiescent Current
- Monotonic Start-Up into Prebiased Outputs
- –40°C to 150°C Operating Junction Temperature Range
- Adjustable Slow Start and Power Sequencing
- Power Good Output Monitor for Undervoltage and Overvoltage
- Adjustable Input Undervoltage Lockout
- For SWIFT™ Documentation, Visit http://www.ti.com/swift
- Create a Custom Design Using the TPS54620 With the WEBENCH Power Designer

2 Applications

- High Density Distributed Power Systems
- High Performance Point of Load Regulation
- Broadband, Networking and Optical Communications Infrastructure

3 Description

The TPS54620 in thermally enhanced 3.50 mm × 3.50 mm QFN package is a full featured 17-V, 6-A, synchronous, step-down converter which is optimized for small designs through high efficiency and integrating the high-side and low-side MOSFETs. Further space savings are achieved through current mode control, which reduces component count, and by selecting a high switching frequency, reducing the footprint of the inductor.

The output voltage start-up ramp is controlled by the SS/TR pin which allows operation as either a stand-alone power supply or in tracking situations. Power sequencing is also possible by correctly configuring the enable and the open-drain power good pins.

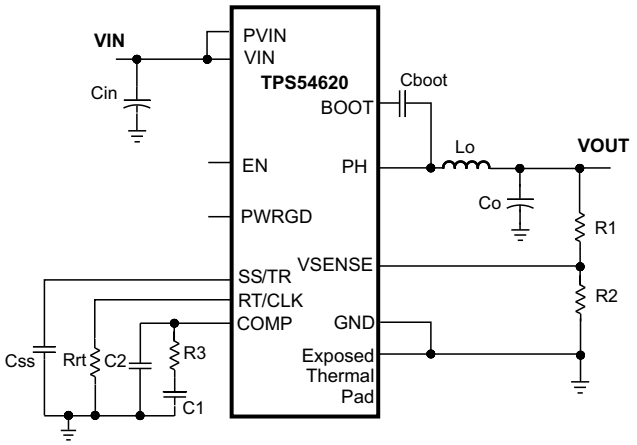
Cycle-by-cycle current limiting on the high-side FET protects the device in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. There is also a low-side sinking current limit that turns off the low-side MOSFET to prevent excessive reverse current. Thermal shutdown disables the part when die temperature exceeds thermal shutdown temperature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54620	VQFN (14)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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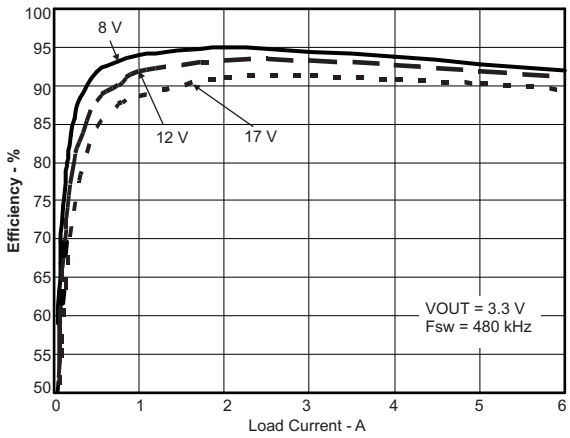
Efficiency vs Load Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2016) to Revision F	Page
• Updated data sheet text to our latest documentation and translations standards	1
• Removed all references to the SwitcherPro™ Software Tool because it is no longer available for this part	1
• Moved storage temperature ratings to the *Absolute Maximum Ratings* table	5
• Changed *Handling Ratings* table to *ESD Ratings*	5
• Changed RHY package to RHL in the *Thermal Information* table	6
• Changed RGY values in the *Thermal Information* table	6
• Updated packages in the last bullet point of *Layout Guidelines*	34
• Added information to the last list item in *Layout Guidelines*	34

Changes from Revision D (October 2014) to Revision E	Page
• Added recommended layout guide lines for sensitive components and the output sensing trace to the *Layout Guidelines* section.	34
• Added *Receiving Notification of Documentation Updates* and Community Resources sections.	37

Changes from Revision C (April 2011) to Revision D	Page
• Added the Device Information table, Handling Ratings table, the Recommended Operating Conditions table, and the Thermal Information table	1
• Changed the Absolute Maximum Ratings for BOOT-PH, MAX value From: 7 V To: 7.7 V	5
• Changed Equation 28 From: C7(nF) To: C5(nF)	27

Changes from Revision B (October 2010) to Revision C	Page
• Changed From separate RHL and RGY packages To a combined RHL and RGY package	4

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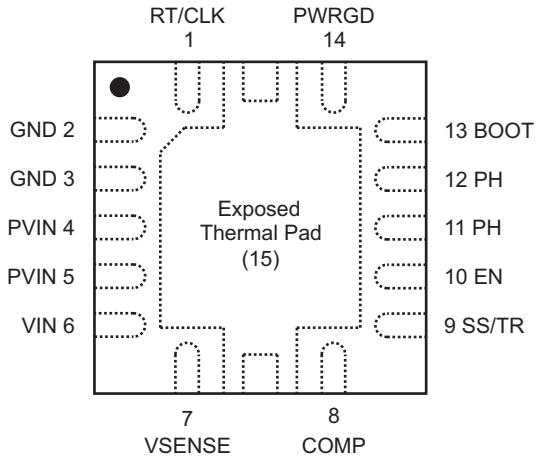
Changes from Revision A (January 2010) to Revision B	Page
• Changed Small Signal Model for Frequency Compensation section	18

Changes from Original (May 2009) to Revision A	Page
• Changed title from 17 V Input, 6 A Output, Synchronous Step Down Switcher with Integrated FET (SWIFT)	1
• Changed PowerPAD to Exposed Thermal Pad	4
• Changed Changed the Absolute Maximum Ratings for EN, MAX value From: 3 V To: 6 V	5
• Changed minimum switching frequency min value from 180 to 160	7
• Changed minimum switching frequency max value from 220 to 240	7
• Added "Type 3" block around C11	19
• Changed PCB Layout graphic	35

5 Pin Configurations and Functions

RHL and RGY Packages
14-Pin VQFN
(Top View)



Pin Functions

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
RT/CLK	1	I	Automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device; in CLK mode, the device synchronizes to an external clock.
GND	2, 3	G	Return for control circuitry and low-side power MOSFET.
PVIN	4, 5	P	Power input. Supplies the power switches of the power converter.
VIN	6	P	Supplies the control circuitry of the power converter.
VSENSE	7	I	Inverting input of the gm error amplifier.
COMP	8	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation to this pin.
SS/TR	9	O	Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
EN	10	I	Enable pin. Float to enable. Adjust the input undervoltage lockout with two resistors.
PH	11, 12	O	Switch node.
BOOT	13	I	A bootstrap cap is required between BOOT and PH. The voltage on this cap carries the gate drive voltage for the high-side MOSFET.
PWRGD	14	G	Power Good fault pin. Asserts low if output voltage is low because of thermal shutdown, dropout, over-voltage, EN shutdown, or during slow start.
Exposed Thermal PAD	15	G	Thermal pad of the package and signal ground and it must be soldered down for proper operation.

(1) I = input, O = output, G = GND, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	20	V
	PVIN	–0.3	20	V
	EN	–0.3	6	V
	BOOT	–0.3	27	V
	VSENSE	–0.3	3	V
	COMP	–0.3	3	V
	PWRGD	–0.3	6	V
	SS/TR	–0.3	3	V
	RT/CLK	–0.3	6	V
Output voltage	BOOT-PH	0	7.7	V
	PH	–1	20	V
	PH 10ns Transient	–3	20	V
Vdiff (GND to exposed thermal pad)		–0.2	0.2	V
Source current	RT/CLK		±100	µA
	PH		Current Limit	A
Sink current	PH		Current Limit	A
	PVIN		Current Limit	A
	COMP		±200	µA
	PWRGD	–0.1	5	mA
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input voltage	4.5		17	V
PVIN	Power stage input voltage	1.6		17	V
	Output current	0		6	A
T_J	Operating junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS54620		UNIT
		RGY (VQFN)	RHL (VQFN)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.1	40.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	34.4	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.4	11.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.4	11.4	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	1.8	1.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 4.5 V to 17 V, PVIN = 1.6 V to 17 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN AND PVIN PINS)					
PVIN operating input voltage		1.6		17	V
VIN operating input voltage		4.5		17	V
VIN internal UVLO threshold	VIN rising		4	4.5	V
VIN internal UVLO hysteresis			150		mV
VIN shutdown supply Current	EN = 0 V		2	5	µA
VIN operating—nonswitching supply current	VSENSE = 810 mV		600	800	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.21	1.26	V
Enable threshold	Falling	1.10	1.17		V
Input current	EN = 1.1 V		1.15		µA
Hysteresis current	EN = 1.3 V		3.4		µA
VOLTAGE REFERENCE					
Voltage reference	0 A ≤ I_{OUT} ≤ 6 A	0.792	0.8	0.808	V
MOSFET					
High-side switch resistance	BOOT-PH = 3 V		32	60	mΩ
High-side switch resistance[1]	BOOT-PH = 6 V		26	40	mΩ
Low-side Switch Resistance[1]	VIN = 12 V		19	30	mΩ
ERROR AMPLIFIER					
Error amplifier Transconductance (gm)	–2 µA < I_{COMP} < 2 µA, $V_{(COMP)}$ = 1 V		1300		µMhos
Error amplifier DC gain	VSENSE = 0.8 V	1000	3100		V/V
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100-mV input overdrive		±110		µA
Start switching threshold			0.25		V
COMP to Iswitch gm			16		A/V
CURRENT LIMIT					
High-side switch current limit threshold		8	11		A
Low-side switch sourcing current limit		7	10		A
Low-side switch sinking current limit			2.3		A

(1) Measured at pins

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Electrical Characteristics (continued)

T_J = –40°C to 150°C, VIN = 4.5 V to 17 V, PVIN = 1.6 V to 17 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN					
Thermal shutdown		160	175		°C
Thermal shutdown hysteresis			10		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
Minimum switching frequency	Rrt = 240 kΩ (1%)	160	200	240	kHz
Switching frequency	Rrt = 100 kΩ (1%)	400	480	560	kHz
Maximum switching frequency	Rrt = 29 kΩ (1%)	1440	1600	1760	kHz
Minimum pulse width			20		ns
RT/CLK high threshold				2	V
RT/CLK low threshold		0.8			V
RT/CLK falling edge to PH rising edge delay	Measured at 500 kHz with RT resistor in series		66		ns
Switching frequency range (RT mode set point and PLL mode)		200		1600	kHz
PH (PH PIN)					
Minimum on-time	Measured at 90% to 90% of VIN, 25°C, I_{PH} = 2 A		94	135	ns
Minimum off-time	BOOT-PH ≥ 3 V		0		ns
BOOT (BOOT PIN)					
BOOT-PH UVLO			2.1	3	V
SLOW START AND TRACKING (SS/TR PIN)					
SS charge current			2.3		μA
SS/TR to VSENSE matching	$V_{(SS/TR)}$ = 0.4 V		29	60	mV
POWER GOOD (PWRGD PIN)					
VSENSE threshold	VSENSE falling (Fault)		91		% Vref
	VSENSE rising (Good)		94		% Vref
	VSENSE rising (Fault)		109		% Vref
	VSENSE falling (Good)		106		% Vref
Output high leakage	VSENSE = Vref, $V_{(PWRGD)}$ = 5.5 V		30	100	nA
Output low	$I_{(PWRGD)}$ = 2 mA			0.3	V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 μA		0.6	1	V
Minimum SS/TR voltage for PWRGD				1.4	V

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6.6 Typical Characteristics

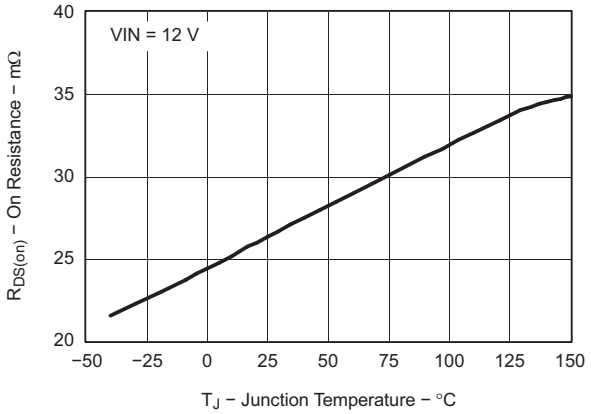

Figure 1. High-Side $R_{DS(on)}$ vs Temperature

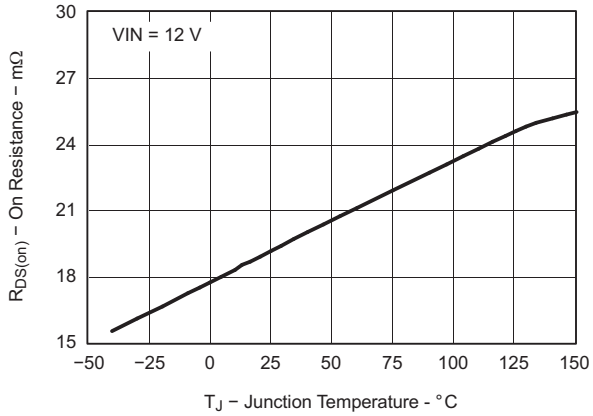

Figure 2. Low-Side $R_{DS(on)}$ vs Temperature

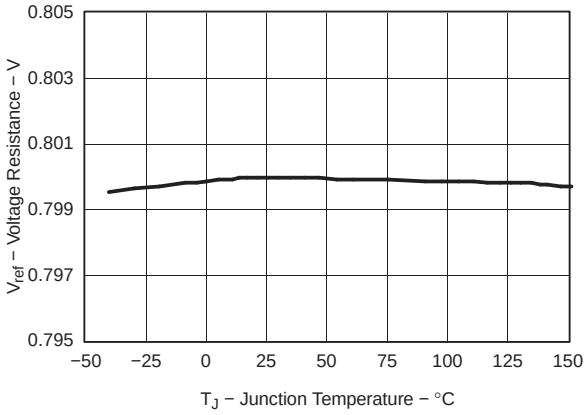

Figure 3. Voltage Reference vs Temperature

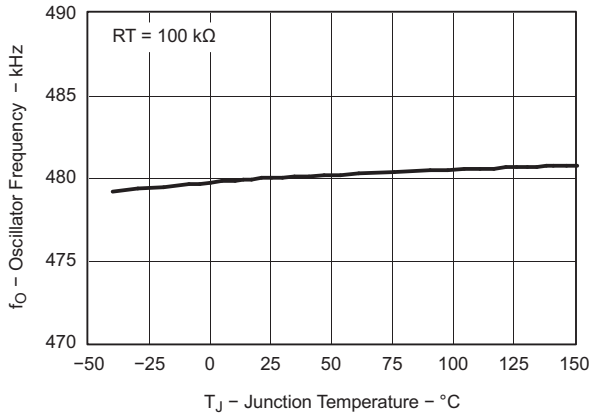

Figure 4. Oscillator Frequency vs Temperature

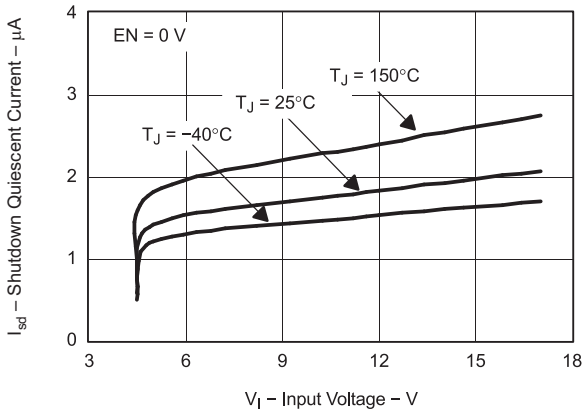

Figure 5. Shutdown Quiescent Current vs Input Voltage

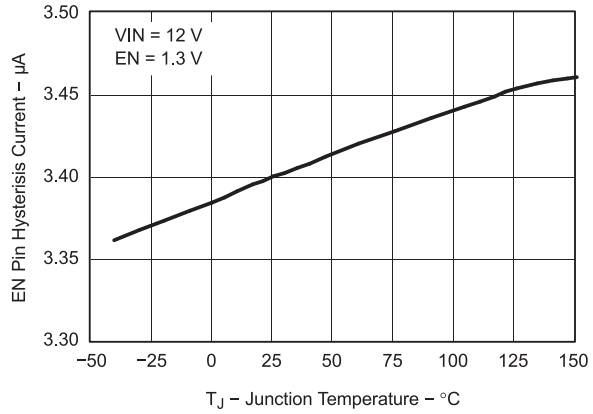

Figure 6. EN Pin Hysteresis Current vs Temperature

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Typical Characteristics (continued)

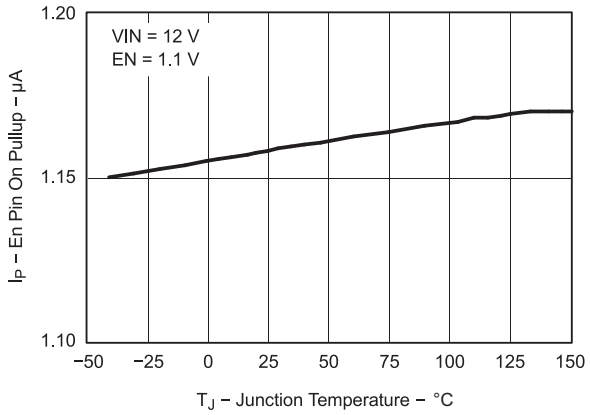

Figure 7. Pin Pullup Current vs Temperature

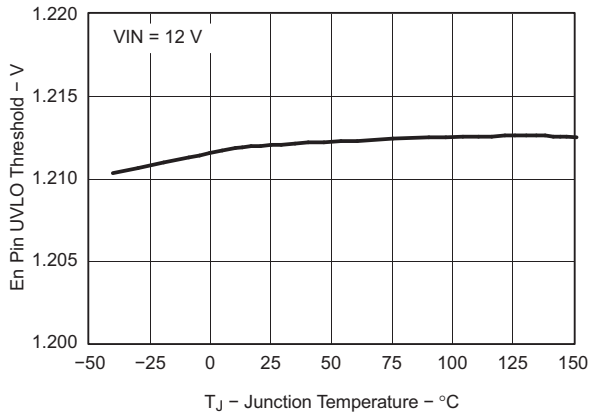

Figure 8. Pin UVLO Threshold vs Temperature

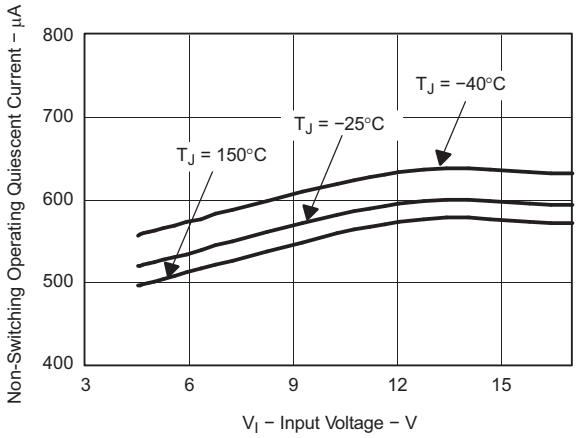

Figure 9. Non-Switching Operating Quiescent Current (VIN) vs Input Voltage

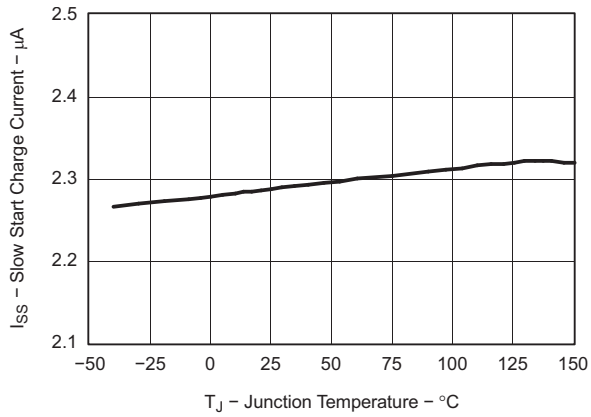

Figure 10. Slow Start Charge Current vs Temperature

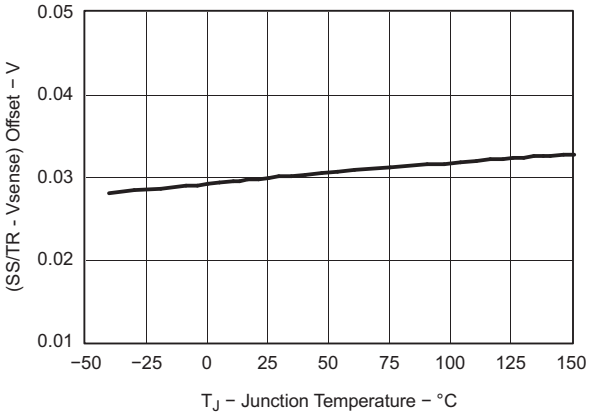

Figure 11. (SS/TR - VSENSE) Offset vs Temperature

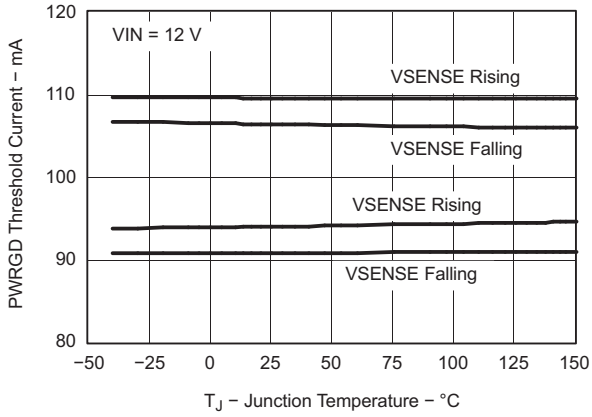

Figure 12. PWRGD Threshold vs Temperature

Typical Characteristics (continued)

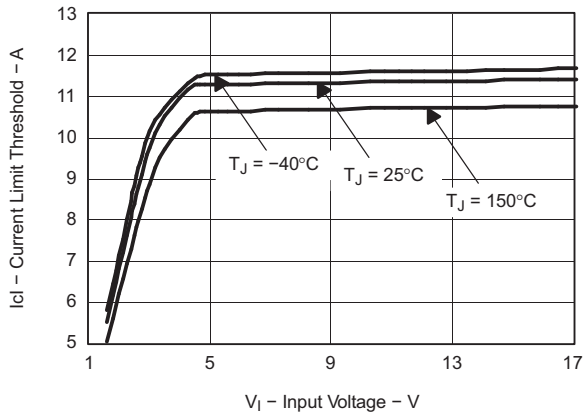

Figure 13. High-Side Current Limit Threshold vs Input Voltage

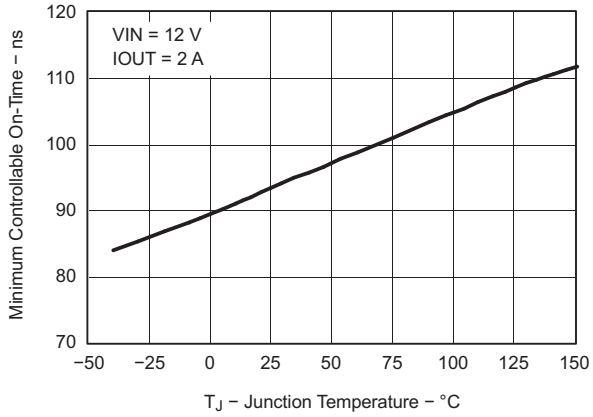

Figure 14. Minimum Controllable On-Time vs Temperature

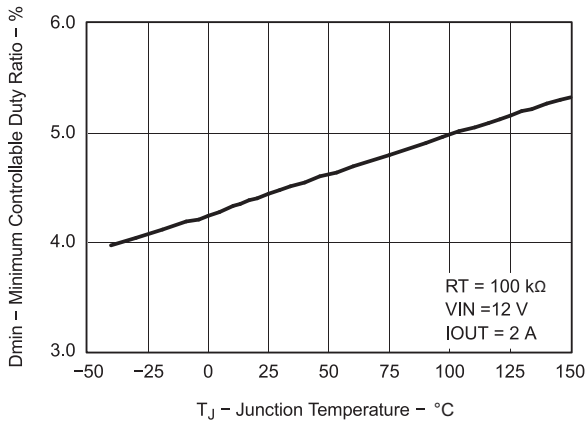

Figure 15. Minimum Controllable Duty Ratio vs Junction Temperature

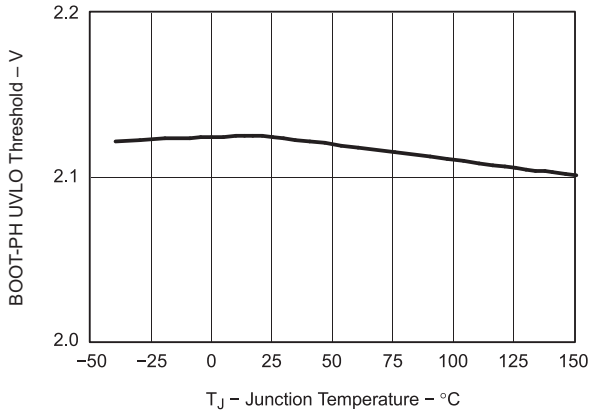

Figure 16. BOOT-PH UVLO Threshold vs Temperature

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7 Detailed Description

7.1 Overview

The device is a 17-V, 6-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients, the device implements a constant frequency peak current mode control that also simplifies external frequency compensation. The wide switching frequency of 200 kHz to 1600 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor-to-ground on the RT/CLK pin. The device also has an internal phase lock loop (PLL) controlled by the RT/CLK pin that can be used to synchronize the switching cycle to the falling edge of an external system clock.

The device has been designed for safe monotonic start-up into prebiased loads. The default start-up is when VIN is typically 4.0 V. The EN pin has an internal pullup current source that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pullup current. The total operating current for the device is approximately 600 μA when not switching and under no load. When the device is disabled, the supply current is typically less than 2 μA.

The integrated MOSFETs allow for high efficiency power supply designs with continuous output currents up to 6 amperes. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

The device reduces the external component count by integrating the boot recharge circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and PH pins. The boot capacitor voltage is monitored by a BOOT to PH UVLO (BOOT-PH UVLO) circuit allowing PH pin to be pulled low to recharge the boot capacitor. The device can operate at 100% duty cycle as long as the boot capacitor voltage is higher than the preset BOOT-PH UVLO threshold which is typically 2.1 V. The output voltage can be stepped down to as low as the 0.8-V voltage reference (Vref).

The device has a power good comparator (PWRGD) with hysteresis which monitors the output voltage through the VSENSE pin. The PWRGD pin is an open-drain MOSFET which is pulled low when the VSENSE pin voltage is less than 91% or greater than 109% of the reference voltage Vref and asserts high when the VSENSE pin voltage is 94% to 106% of the Vref.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor or resistor divider should be coupled to the pin for slow start or critical power supply sequencing requirements.

The device is protected from output overvoltage, overload, and thermal fault conditions. The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage circuit power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the VSENSE pin voltage is lower than 106% of the Vref. The device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections which help control the inductor current and avoid current runaway. The device also shuts down if the junction temperature is higher than thermal shutdown trip point. The device is restarted under control of the slow-start circuit automatically when the junction temperature drops 10°C typically below the thermal shutdown trip point.

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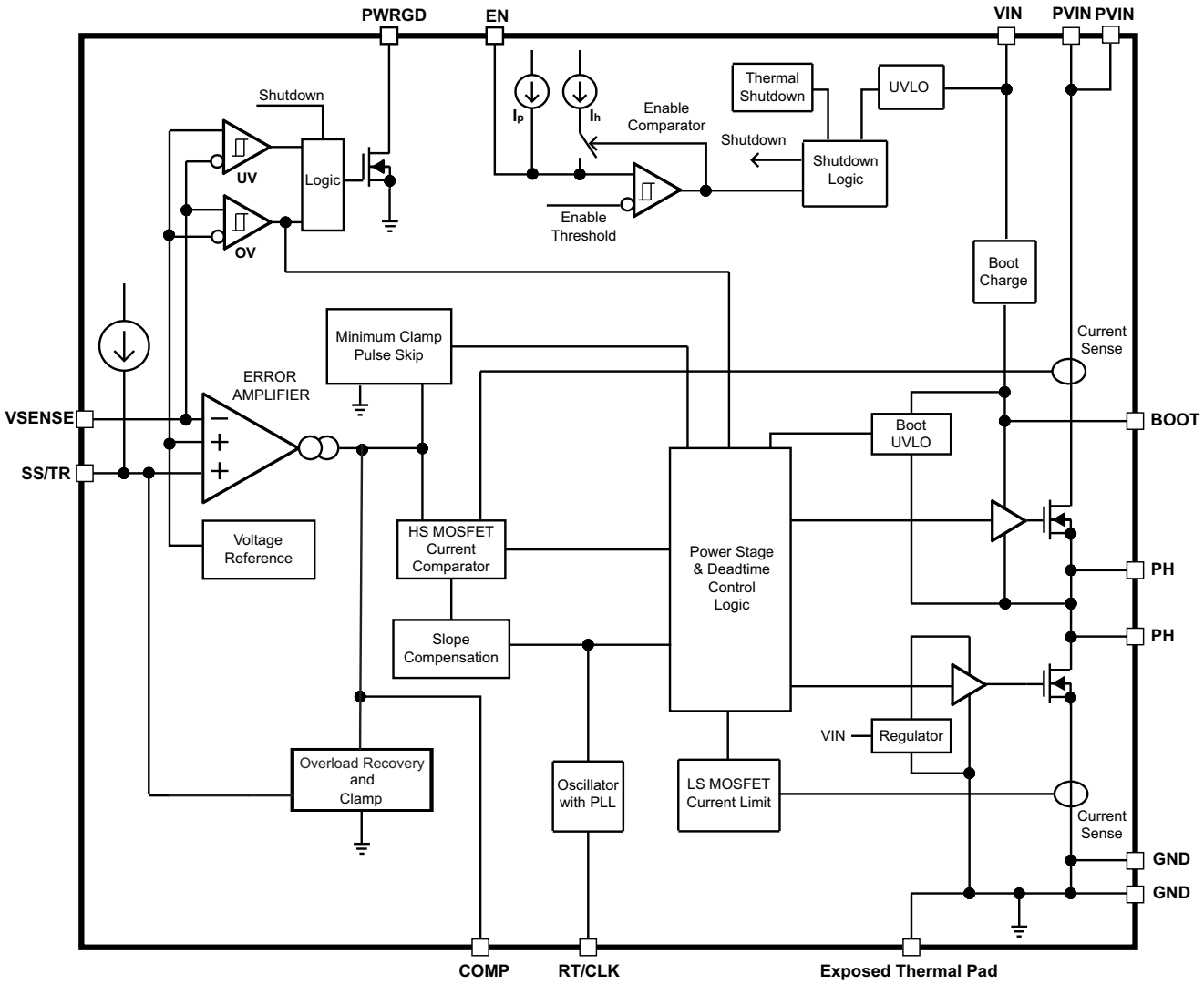
7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The device uses a adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turnon of the high-side power switch. The error amplifier output is converted into a current reference which compares to the high-side power switch current. When the power switch current reaches current reference generated by the COMP voltage level the high-side power switch is turned off and the low-side power switch is turned on.

7.3.2 Continuous Current Mode Operation (CCM)

As a synchronous buck converter, the device normally works in CCM (Continuous Conduction Mode) under all load conditions.

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Feature Description (continued)

7.3.3 VIN and Power VIN Pins (VIN and PVIN)

The device allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN pin voltage supplies the internal control circuits of the device. The PVIN pin voltage provides the input voltage to the power converter system.

If tied together, the input voltage for VIN and PVIN can range from 4.5 V to 17 V. If using the VIN separately from PVIN, the VIN pin must be between 4.5 V and 17 V, and the PVIN pin can range from as low as 1.6 V to 17 V. A voltage divider connected to the EN pin can adjust the either input voltage UVLO appropriately. Adjusting the input voltage UVLO on the PVIN pin helps to provide consistent power up behavior.

7.3.4 Voltage Reference

The voltage reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit.

7.3.5 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output (VOUT) to the VSENSE pin. TI recommends using 1% tolerance or better divider resistors. Referring to the application schematic of Figure 34, start with a 10 kΩ for R6 and use Equation 1 to calculate R5. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R5 = \frac{Vo - Vref}{Vref} R6$$

where

- Vref = 0.8V (1)

The minimum output voltage and maximum output voltage can be limited by the minimum on time of the high-side MOSFET and bootstrap voltage (BOOT-PH voltage) respectively. More discussions are located in *Minimum Output Voltage* and *Bootstrap Voltage (BOOT) and Low Dropout Operation*.

7.3.6 Safe Start-Up into Prebiased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a prebiased output. During monotonic prebiased start-up, the low-side MOSFET is not allowed to sink current until the SS/TR pin voltage is higher than 1.4 V.

7.3.7 Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the VSENSE pin voltage to the lower of the SS/TR pin voltage or the internal 0.8-V voltage reference. The transconductance of the error amplifier is 1300 μA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground.

7.3.8 Slope Compensation

The device adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty cycle range.

7.3.9 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on/off control of the device. When the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state.

The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use either open-drain or open-collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 150 mV.

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Feature Description (continued)

If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVIN in split-rail applications, then the EN pin can be configured as shown in Figure 17, Figure 18, and Figure 19. When using the external UVLO function, TI recommends setting the hysteresis to be greater than 500 mV.

The EN pin has a small pullup current Ip which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h when the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 2 and Equation 3.

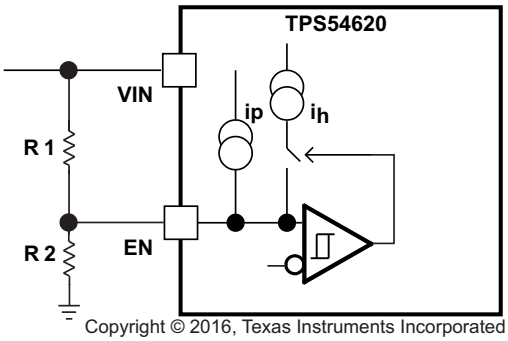

Figure 17. Adjustable VIN Undervoltage Lockout

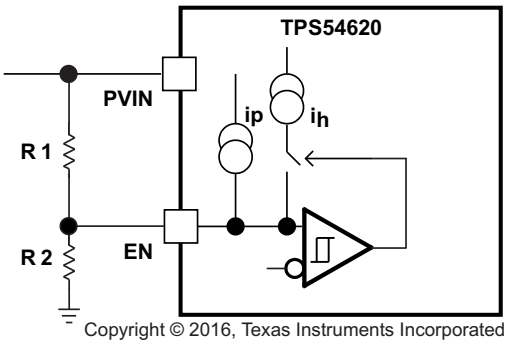

Figure 18. Adjustable PVIN Undervoltage Lockout, VIN ≥ 4.5 V

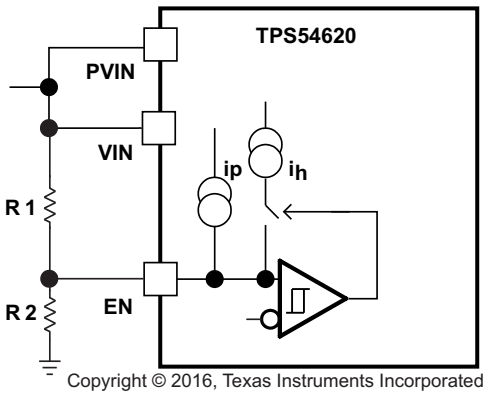

Figure 19. Adjustable VIN and PVIN Undervoltage Lockout

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Feature Description (continued)

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h}$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \quad (2)$$

where

- I_h = 3.4 μA
- I_p = 1.15 μA
- $V_{ENRISING}$ = 1.21 V
- $V_{ENFALLING}$ = 1.17 V (3)

7.3.10 Adjustable Switching Frequency and Synchronization (RT/CLK)

The RT/CLK pin can be used to set the switching frequency of the device in two modes.

In RT mode, a resistor (RT resistor) is connected between the RT/CLK pin and GND. The switching frequency of the device is adjustable from 200 kHz to 1600 kHz by placing a maximum of 240 kΩ and minimum of 29 kΩ, respectively. In CLK mode, an external clock is connected directly to the RT/CLK pin. The device is synchronized to the external clock frequency with PLL.

The CLK mode overrides the RT mode. The device is able to detect the proper mode automatically and switch from the RT mode to CLK mode.

7.3.11 Slow Start (SS/TR)

The device uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow-start time. The device has an internal pullup current source of 2.3 μA that charges the external slow-start capacitor. The calculations for the slow-start time (Tss, 10% to 90%) and slow-start capacitor (Css) are shown in Equation 4. The voltage reference (Vref) is 0.8 V and the slow-start charge current (Iss) is 2.3 μA.

$$t_{SS}\ (ms) = \frac{Css\ (nF) \times Vref\ (V)}{Iss\ (\mu A)} \quad (4)$$

When the input UVLO is triggered, the EN pin is pulled below 1.21 V, or a thermal shutdown event occurs, the device stops switching and enters low current operation. At the subsequent power up when the shutdown condition is removed, the device does not start switching until it has discharged its SS/TR pin to ground ensuring proper soft-start behavior.

7.3.12 Power Good (PWRGD)

The PWRGD pin is an open-drain output. When the VSENSE pin is between 94% and 106% of the internal voltage reference the PWRGD pin pulldown is deasserted and the pin floats. TI recommends using a pullup resistor between the values of 10 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD is in a defined state when the VIN input voltage is greater than 1 V but with reduced current sinking capability. The PWRGD achieves full current sinking capability when the VIN input voltage is above 4.5 V.

The PWRGD pin is pulled low when VSENSE is lower than 91% or greater than 109% of the nominal internal reference voltage. Also, if the PWRGD is pulled low and the input UVLO or thermal shutdown are asserted, the EN pin is pulled low or the SS/TR pin is set below 1.4 V.

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Feature Description (continued)

7.3.13 Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. When the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

7.3.14 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

7.3.14.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference the high-side switch is turned off.

7.3.14.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

7.3.15 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 165°C typically.

7.3.16 Small Signal Model for Loop Response

Figure 20 shows an equivalent model for the device control loop which can be modeled in a circuit simulation program to check frequency response and transient responses. The error amplifier is a transconductance amplifier with a gm of 1300 μA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor Roea (2.38 MΩ) and capacitor Coea (20.7 pF) model the open-loop gain and frequency response of the error amplifier. The 1-mV AC voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c and c/b show the small signal responses of the power stage and frequency compensation respectively. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

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Feature Description (continued)

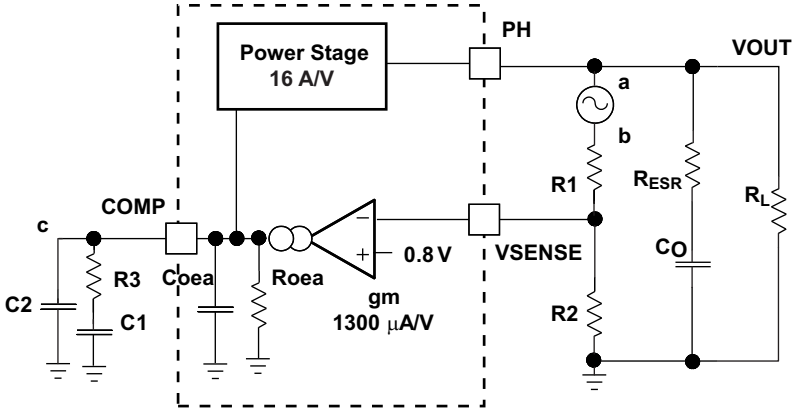

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Figure 20. Small Signal Model for Loop Response

7.3.17 Simple Small Signal Model for Peak Current Mode Control

Figure 21 is a simple small signal model that can be used to understand how to design the frequency compensation. The device power stage can be approximated to a voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control-to-output transfer function is shown in Equation 5 and consists of a DC gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 20) is the power stage transconductance (gm_{ps}), which is 16 A/V for the device. The DC gain of the power stage is the product of gm_{ps}, and the load resistance (R_L) as shown in Equation 6 with resistive loads. As the load current increases, the DC gain decreases. This variation with load may seem problematic at first glance, but fortunately the dominant pole moves with load current (see Equation 7). The combined effect is highlighted by the dashed line in Figure 22. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions, making it easier to design the frequency compensation.

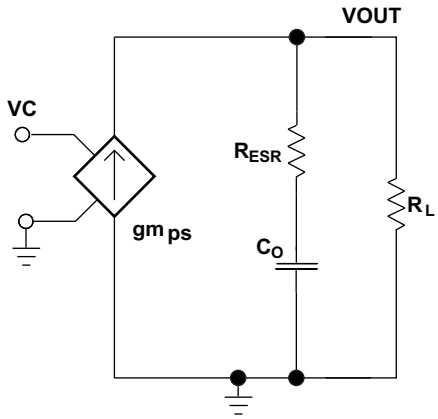

Figure 21. Simplified Small Signal Model for Peak Current Mode Control

Feature Description (continued)

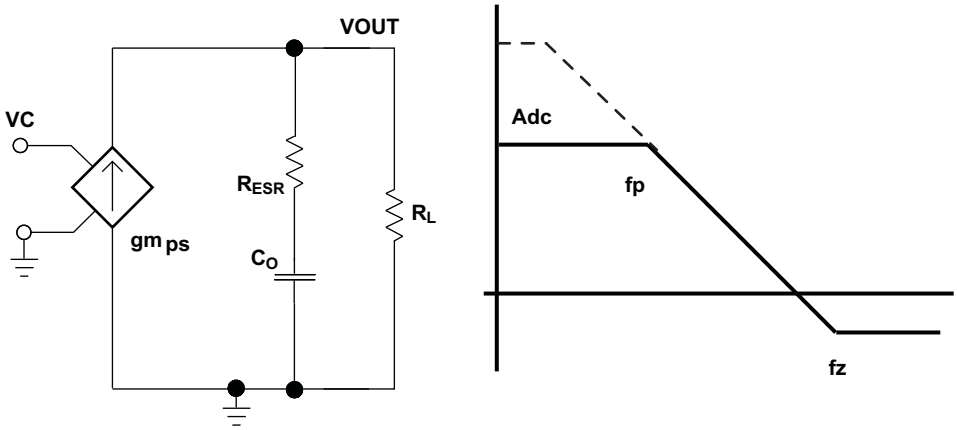

Figure 22. Simplified Frequency Response for Peak Current Mode Control

$$\frac{VOUT}{VC} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times fz}\right)}{\left(1 + \frac{s}{2\pi \times fp}\right)} \tag{5}$$

$$Adc = gm_{ps} \times R_L$$

where

- gm_{ps} is the power stage gain (16 A/V).
- R_L is the load resistance (6)

$$fp = \frac{1}{C_O \times R_L \times 2\pi}$$

where

- C_O is the output capacitance.
- R_L is the load resistance (7)

$$fz = \frac{1}{C_O \times R_{ESR} \times 2\pi}$$

where

- C_O is the output capacitance.
- R_{ESR} is the equivalent series resistance of the output capacitor. (8)

7.3.18 Small Signal Model for Frequency Compensation

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used Type II compensation circuits and a Type III frequency compensation circuit, as shown in Figure 23. In Type 2A, one additional high frequency pole, C6, is added to attenuate high-frequency noise. In Type III, one additional capacitor, C11, is added to provide a phase boost at the crossover frequency. See *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352) for a complete explanation of Type III compensation.

The design guidelines below are provided for advanced users who prefer to compensate using the general method. The below equations only apply to designs whose ESR zero is above the bandwidth of the control loop. This is usually true with ceramic output capacitors. See the *Application Information* section for a step-by-step design procedure using higher ESR output capacitors with lower ESR zero frequencies.

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Feature Description (continued)

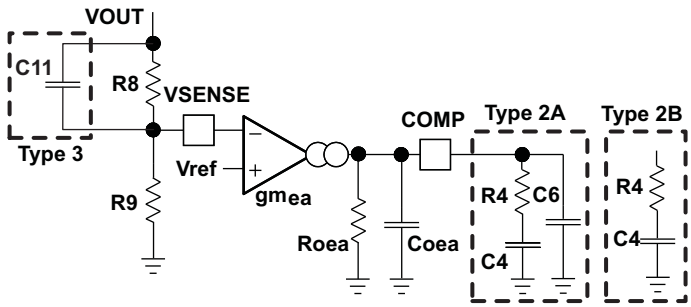

Figure 23. Types of Frequency Compensation

The general design guidelines for device loop compensation are as follows:

1. Determine the crossover frequency, fc. A good starting point is 1/10th of the switching frequency, fsw.
2. R4 can be determined by:

$$R4 = \frac{2\pi \times fc \times VOUT \times Co}{gm_{ea} \times Vref \times gm_{ps}}$$

where

- gm_{ea} is the GM amplifier gain (1300 μA/V)
- gm_{ps} is the power stage gain (12 A/V)
- Vref is the reference voltage (0.8 V) (9)

3. Place a compensation zero at the dominant pole: $\left(fp = \frac{1}{C_O \times R_L \times 2\pi}\right)$

C4 can be determined by:

$$C4 = \frac{R_L \times Co}{R4} \quad (10)$$

4. C6 is optional. It can be used to cancel the zero from the ESR (Equivalent Series Resistance) of the output capacitor Co.

$$C6 = \frac{R_{ESR} \times Co}{R4} \quad (11)$$

5. Type III compensation can be implemented with the addition of one capacitor, C11. This allows for slightly higher loop bandwidths and higher phase margins. If used, C11 is calculated from Equation 12.

$$C11 = \frac{1}{(2 \cdot \pi \cdot R8 \cdot fc)} \quad (12)$$

7.4 Device Functional Modes

7.4.1 Adjustable Switching Frequency (RT Mode)

To determine the RT resistance for a given switching frequency, use Equation 13 or the curve in Figure 24. To reduce the solution size, one would set the switching frequency as high as possible, but tradeoffs of the supply efficiency and minimum controllable on-time must be considered.

$$Rrt(k\Omega) = 48000 \cdot Fsw\,(kHz)^{-0.997} - 2 \quad (13)$$

Device Functional Modes (continued)

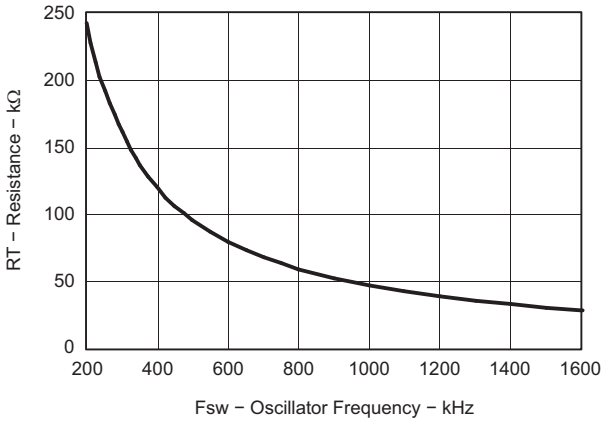

Figure 24. RT Set Resistor vs Switching Frequency

7.4.2 Synchronization (CLK Mode)

An internal Phase Locked Loop (PLL) has been implemented to allow synchronization between 200 kHz and 1600 kHz, and to easily switch from RT mode to CLK mode.

To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin.

In applications where both RT mode and CLK mode are needed, the device can be configured as shown in Figure 25. Before the external clock is present, the device works in RT mode and the switching frequency is set by RT resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the SYNC pin is pulled above the RT/CLK high threshold (2.0 V), the device switches from the RT mode to the CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. TI does not recommend switching from the CLK mode back to the RT mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by RT resistor.

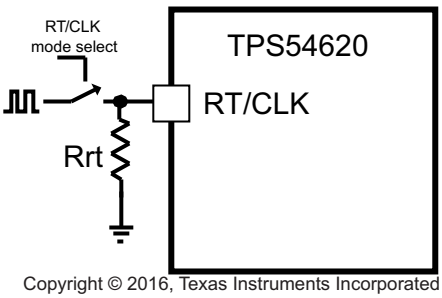

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Figure 25. Works With Both RT Mode and CLK Mode

7.4.3 Bootstrap Voltage (BOOT) and Low-Dropout Operation

The device has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than VIN and BOOT-PH voltage is below regulation. The value of this ceramic capacitor should be 0.1 μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

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Device Functional Modes (continued)

To improve dropout, the device is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than the BOOT-PH UVLO threshold which is typically 2.1 V. When the voltage between BOOT and PH drops below the BOOT-PH UVLO threshold the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged. In applications with split input voltage rails, 100% duty cycle operation can be achieved as long as (VIN – PVIN) > 4 V.

7.4.4 Sequencing (SS/TR)

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN and PWRGD pins.

The sequential method is illustrated in Figure 26 using two TPS54620 devices. The power good of the first device is coupled to the EN pin of the second device which enables the second power supply when the primary supply reaches regulation. Figure 27 shows the results of Figure 26.

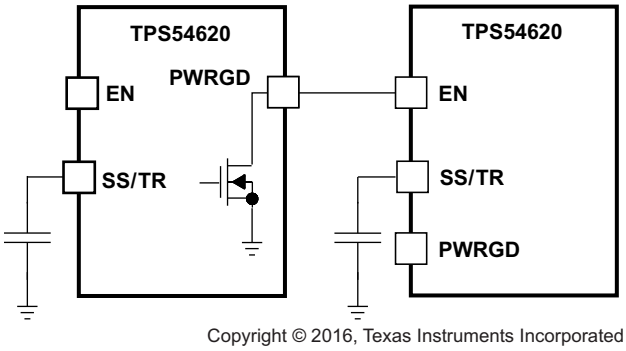

Figure 26. Sequential Start-Up Sequence

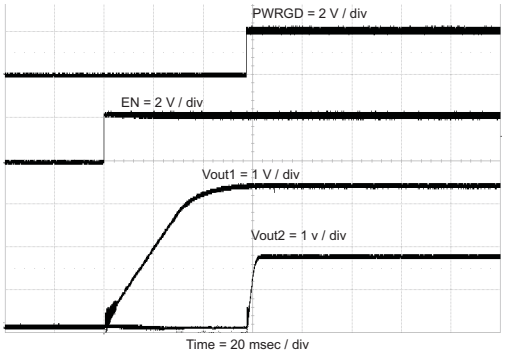

Figure 27. Sequential Start-Up Using EN and PWRGD

Figure 28 shows the method implementing ratiometric sequencing by connecting the SS/TR pins of two devices together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow start time the pullup current source must be doubled in Equation 4. Figure 29 shows the results of Figure 28.

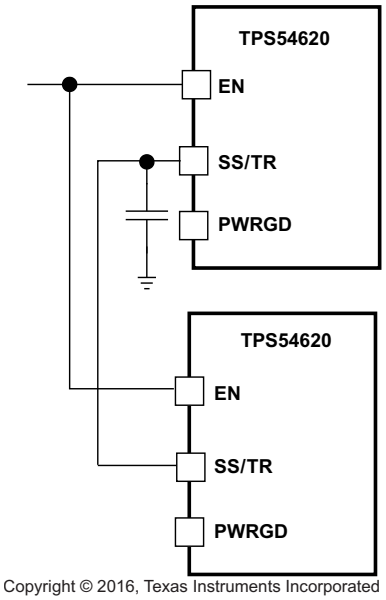

Figure 28. Ratiometric Start-Up Sequence

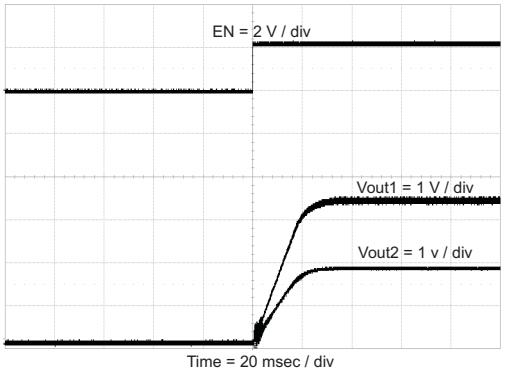

Figure 29. Ratiometric Start-Up Using Coupled SS/TR Pins

Device Functional Modes (continued)

Ratiometric and simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 30 to the output of the power supply that must be tracked or another voltage reference source. Using Equation 14 and Equation 15, the tracking resistors can be calculated to initiate the Vout2 slightly before, after or at the same time as Vout1. Equation 16 is the voltage difference between Vout1 and Vout2.

To design a ratiometric start-up in which the Vout2 voltage is slightly greater than the Vout1 voltage when Vout2 reaches regulation, use a negative number in Equation 14 and Equation 15 for ΔV. Equation 16 results in a positive number for applications where the Vout2 is slightly lower than Vout1 when Vout2 regulation is achieved. Figure 31 and Figure 32 show the results for positive ΔV and negative ΔV, respectively.

The ΔV variable is zero volt for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset (Vssoffset, 29 mV) in the slow-start circuit and the offset created by the pullup current source (Iss, 2.3 μA) and tracking resistors, the Vssoffset and Iss are included as variables in the equations. Figure 33 shows the result when ΔV = 0 V.

To ensure proper operation of the device, the calculated R1 value from Equation 14 must be greater than the value calculated in Equation 17.

$$R1 = \frac{Vout2 + \Delta V}{Vref} \times \frac{Vssoffset}{Iss} \tag{14}$$

$$R2 = \frac{Vref \times R1}{Vout2 + \Delta V - Vref} \tag{15}$$

$$\Delta V = Vout1 - Vout2 \tag{16}$$

$$R1 > 2800 \times Vout1 - 180 \times \Delta V \tag{17}$$

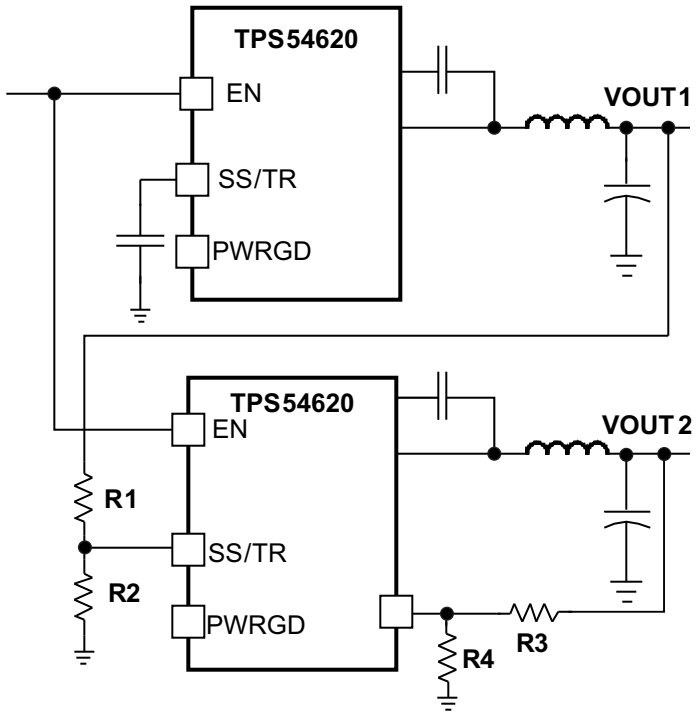

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Figure 30. Ratiometric and Simultaneous Start-Up Sequence

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Device Functional Modes (continued)

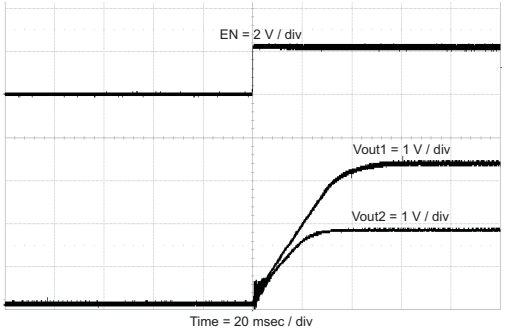

Figure 31. Ratiometric Start-Up With Vout1 Leading Vout2

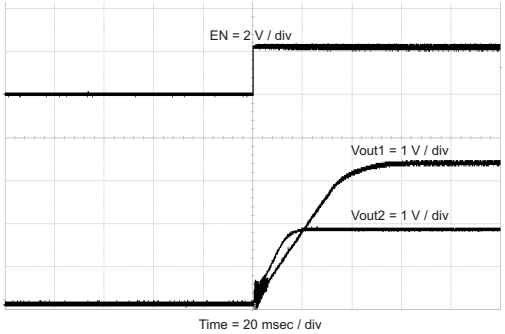

Figure 32. Ratiometric Start-Up With Vout2 Leading Vout1

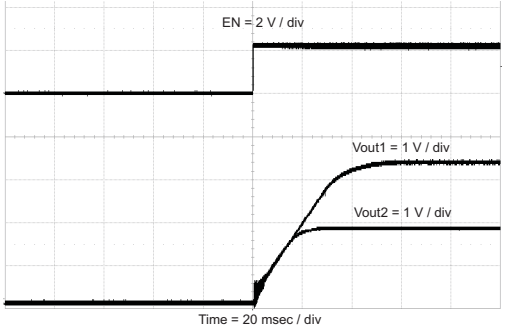

Figure 33. Simultaneous Start-Up

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54620 device is a highly-integrated, synchronous, step-down, DC-DC converter. This device is used to convert a higher DC input voltage to a lower DC output voltage, with a maximum output current of 6 A.

8.2 Typical Application

The application schematic of Figure 34 was developed to meet the requirements of the device. This circuit is available as the TPS54620EVM-374 evaluation module. The design procedure is given in this section.

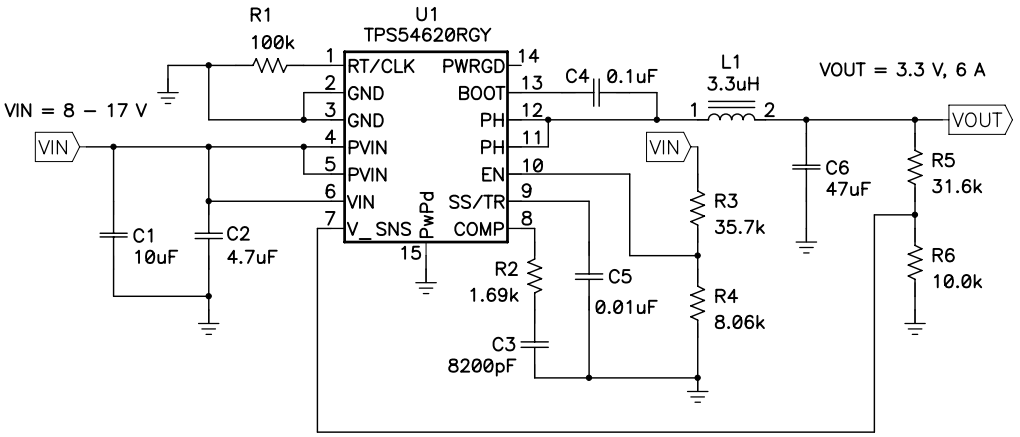

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Figure 34. Typical Application Circuit

8.2.1 Design Requirements

This example details the design of a high frequency switching regulator design using ceramic output capacitors. A few parameters must be known to start the design process. These parameters are typically determined at the system level. For this example, the known parameters in Table 1 are used.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Output Voltage	3.3 V
Output Current	6 A
Transient Response 1A load step	ΔVout = 5 %
Input Voltage	12 V nominal, 8 V to 17 V
Output Voltage Ripple	33 mV p-p
Start Input Voltage (Rising Vin)	6.528 V
Stop Input Voltage (Falling Vin)	6.190 V
Switching Frequency	480 kHz

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8.2.2 Detailed Design Procedures

8.2.2.1 Custom Design With WEBENCH Tools

Click here to create a custom design using the TPS54620 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

8.2.2.2 Operating Frequency

The first step is to decide on a switching frequency for the regulator. There is a trade-off between higher and lower switching frequencies. Higher switching frequencies may produce a smaller solution size using lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which hurt the efficiency and thermal performance of the converter. In this design, a moderate switching frequency of 480 kHz is selected to achieve both a small solution size and a high-efficiency operation.

8.2.2.3 Output Inductor Selection

To calculate the value of the output inductor, use Equation 18. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, KIND is normally from 0.1 to 0.3 for the majority of applications.

$$L1 = \frac{Vinmax - Vout}{Io \cdot Kind} \cdot \frac{Vout}{Vinmax \cdot f sw} \tag{18}$$

For this design example, use KIND = 0.3 and the inductor value is calculated to be 3.08 µH. For this design, a nearest standard value was chosen: 3.3 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 20 and Equation 21.

$$Iripple = \frac{Vinmax - Vout}{L1} \cdot \frac{Vout}{Vinmax \cdot f sw} \tag{19}$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \cdot \left(\frac{V_o \cdot (Vinmax - Vo)}{Vinmax \cdot L1 \cdot f sw} \right)^2} \tag{20}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{21}$$

For this design, the RMS inductor current is 6.02 A and the peak inductor current is 6.84 A. The chosen inductor is a Coilcraft MSS1048 series 3.3 µH. It has a saturation current rating of 7.38 A and a RMS current rating of 7.22 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

8.2.2.4 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these three criteria

The desired response to a large change in the load current is the first criteria. The output capacitor must supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 22 shows the minimum output capacitance necessary to accomplish this.

$$Co > \frac{2 \cdot \Delta Iout}{f sw \cdot \Delta Vout}$$

where

- ΔIout is the change in output current,
- fsw is the regulators switching frequency,
- and ΔVout is the allowable change in the output voltage (22)

For this example, the transient load response is specified as a 5% change in Vout for a load step of 1 A. For this example, ΔIout = 1.0 A and ΔVout = 0.05 × 3.3 = 0.165 V. Using these numbers gives a minimum capacitance of 25 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 23 calculates the minimum output capacitance needed to meet the output voltage ripple specification. In this case, the maximum output voltage ripple is 33 mV. Under this requirement, Equation 23 yields 13.2 µF.

$$Co > \frac{1}{8 \cdot f sw} \cdot \frac{1}{\frac{Voripple}{Iripple}}$$

where

- Vripple is the maximum allowable output voltage ripple,
- and Iripple is the inductor ripple current (23)

Equation 24 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 24 indicates the ESR should be less than 19.7 mΩ. In this case, the ESR of the ceramic capacitors is much smaller than 19.7 mΩ.

$$Resr < \frac{Voripple}{Iripple} \tag{24}$$

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases this minimum value. For this example, a 47-µF, 6.3-V X5R ceramic capacitor with 3 mΩ of ESR is be used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation 25 can be used to calculate the RMS ripple current the output capacitor is required to support. For this application, Equation 25 yields 485 mA.

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$$Icorms = \frac{Vout \cdot (Vinmax - Vout)}{\sqrt{12} \cdot Vinmax \cdot L1 \cdot fsw} \tag{25}$$

8.2.2.5 Input Capacitor Selection

The TPS54620 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 4.7 µF of effective capacitance on the PVIN input voltage pins and 4.7 µF on the Vin input voltage pin. In some applications additional bulk capacitance may also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54620. The input ripple current can be calculated using Equation 26.

$$Icirms = Iout \cdot \sqrt{\frac{Vout}{Vinmin} \cdot \frac{(Vinmin - Vout)}{Vinmin}} \tag{26}$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. For this example, one 10-µF and one 4.7-µF, 25-V capacitors in parallel have been selected as the VIN and PVIN inputs are tied together so the TPS54620 may operate from a single supply. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 27. Using the design example values, Ioutmax = 6 A, Cin = 14.7 µF, Fsw = 480 kHz, yields an input voltage ripple of 213 mV and a RMS input ripple current of 2.95 A.

$$\Delta Vin = \frac{Ioutmax \cdot 0.25}{Cin \cdot fsw} \tag{27}$$

8.2.2.6 Slow-Start Capacitor Selection

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54620 reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft-start capacitor value can be calculated using Equation 28. For the example circuit, the soft-start time is not too critical because the output capacitor value is 47 µF, which does not require much current to charge to 3.3 V. The example circuit has the soft-start time set to an arbitrary value of 3.5 ms which requires a 10-nF capacitor. In TPS54620, Iss is 2.3 µA and Vref is 0.8 V.

$$C5(nF) = \frac{Tss(ms) \text{ x } Iss(\mu A)}{Vref(V)} \tag{28}$$

8.2.2.7 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT-PH pin for proper operation. TI recommends using a ceramic capacitor with X5R or better grade dielectric. The capacitor must have a 10-V or higher voltage rating.

8.2.2.8 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) can be adjusted using the external voltage divider network of R3 and R4. R3 is connected between VIN and the EN pin of the TPS54620 and R4 is connected between EN and GND . The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. For the example design, the supply should turn on and start switching when the input voltage increases above 6.528 V (UVLO start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 6.190 V (UVLO stop or disable). Equation 2 and Equation 3 can be used to calculate the values for the upper and lower resistor values. For the stop voltages specified the nearest standard resistor value for R3 is 35.7 kΩ and for R4 is 8.06 kΩ.

8.2.2.9 Output Voltage Feedback Resistor Selection

The resistor divider network R5 and R6 is used to set the output voltage. For the example design, 10 kΩ was selected for R6. Using Equation 29, R5 is calculated as 31.25 kΩ. The nearest standard 1% resistor is 31.6 kΩ.

$$R5 = \frac{Vo - Vref}{Vref} R6 \tag{29}$$

8.2.2.9.1 Minimum Output Voltage

Due to the internal design of the TPS54620, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.8 V. Above 0.8 V, the output voltage may be limited by the minimum controllable on time. The minimum output voltage in this case is given by Equation 30

$$V_{OUT}min = Ontimemin \times fsmax\ (V_{IN}max + I_{OUT}min\ (R_{DS2}min - R_{DS1}min)) - I_{OUT}min\ (R_L + R_{DS2}min)$$

where

- $V_{OUT}min$ = minimum achievable output voltage
- Ontimemin = minimum controllable on-time (135 ns maximum)
- $fsmax$ = maximum switching frequency including tolerance
- $V_{IN}max$ = maximum input voltage
- $I_{OUT}min$ = minimum load current
- $R_{DS1}min$ = minimum high-side MOSFET on-resistance (36 to 32 mΩ typical)
- $R_{DS2}min$ = minimum low-side MOSFET on-resistance (19 mΩ typical)
- R_L = series resistance of output inductor (30)

8.2.2.10 Compensation Component Selection

There are several industry techniques used to compensate DC-DC regulators. The method presented here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60 and 90 degrees. The method presented here ignores the effects of the slope compensation that is internal to the TPS54620. Because the slope compensation is ignored, the actual cross over frequency is usually lower than the crossover frequency used in the calculations. Use WEBENCH software for a more accurate design.

First, the modulator pole, $fpmod$, and the esr zero, $fzmod$ must be calculated using Equation 31 and Equation 32. For Cout, use a derated value of 22.4 µF. use Equation 33 and Equation 34 to estimate a starting point for the closed-loop crossover frequency fco. Then the required compensation components may be derived. For this design example, $fpmod$ is 12.9 kHz and $fzmod$ is 2730 kHz. Equation 33 is the geometric mean of the modulator pole and the ESR zero and Equation 34 is the geometric mean of the modulator pole and one half the switching frequency. Use a frequency near the lower of these two values as the intended crossover frequency fco. In this case Equation 33 yields 175 kHz and Equation 34 yields 55.7 kHz. The lower value is 55.7 kHz. A slightly higher frequency of 60.5 kHz is chosen as the intended crossover frequency.

$$fpmod = \frac{Iout}{2 \cdot \pi \cdot Vout \cdot Cout} \tag{31}$$

$$fzmod = \frac{1}{2 \cdot \pi \cdot RESR \cdot Cout} \tag{32}$$

$$fco = \sqrt{fpmod \cdot fzmod} \tag{33}$$

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$$f\text{co} = \sqrt{f\text{pmod} \cdot \frac{f\text{sw}}{2}} \tag{34}$$

Now the compensation components can be calculated. First calculate the value for R2 which sets the gain of the compensated network at the crossover frequency. Use Equation 35 to determine the value of R2.

$$\text{R2} = \frac{2\pi \cdot f\text{c} \cdot \text{Vout} \cdot \text{Cout}}{\text{gm}_{\text{ea}} \cdot \text{Vref} \cdot \text{gm}_{\text{ps}}} \tag{35}$$

Next calculate the value of C3. Together with R2, C3 places a compensation zero at the modulator pole frequency. Equation 36 to determine the value of C3.

$$\text{C3} = \frac{\text{Vout} \cdot \text{Cout}}{\text{Iout} \cdot \text{R2}} \tag{36}$$

Using Equation 35 and Equation 36 the standard values for R2 and C3 are 1.69 kΩ and 8200 pF.

An additional high frequency pole can be used if necessary by adding a capacitor in parallel with the series combination of R2 and C3. The pole frequency is given by Equation 37. This pole is not used in this design.

$$f\text{p} = \frac{1}{2 \cdot \pi \cdot \text{R2} \cdot \text{Cp}} \tag{37}$$

8.2.2.11 Fast Transient Considerations

In applications where fast transient responses are important, the application circuit in Figure 34 can be modified as shown in Figure 35, which is a customized reference design (PMP4854-2, REV.B).

The frequency responses of Figure 35 is shown in Figure 36. The crossover frequency is pushed much higher to 118 kHz and the phase margin is about 57 degrees.

For more information about Type II and Type III frequency compensation circuits, refer to the *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352) and *TPS54620 & TPS54XXX Current-Mode Step-Down Converter Design Calculator* (SLVC219) data sheet.

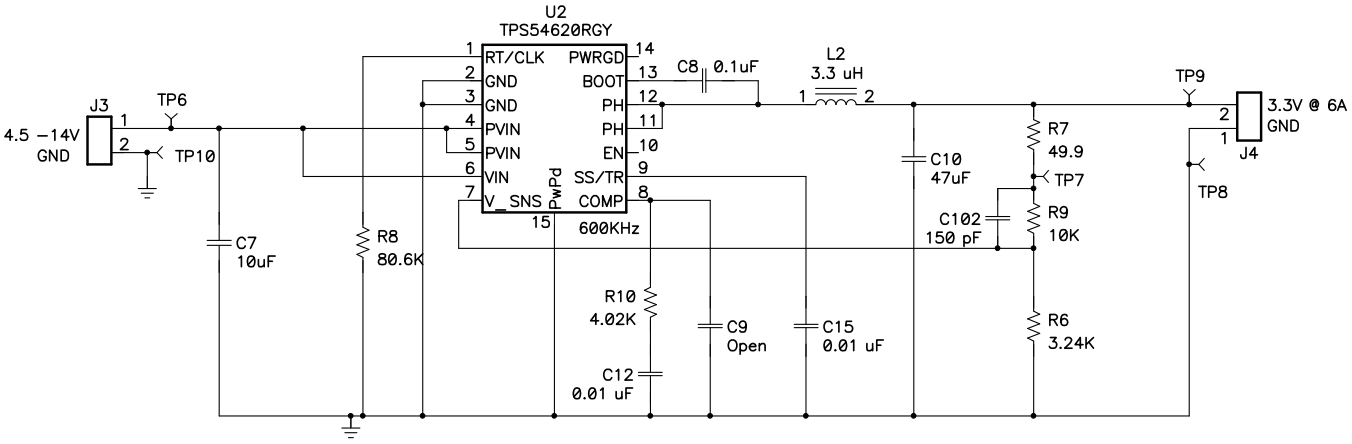

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Figure 35. 3.3-V Output Power Supply Design (PMP4854-2) With Fast Transients

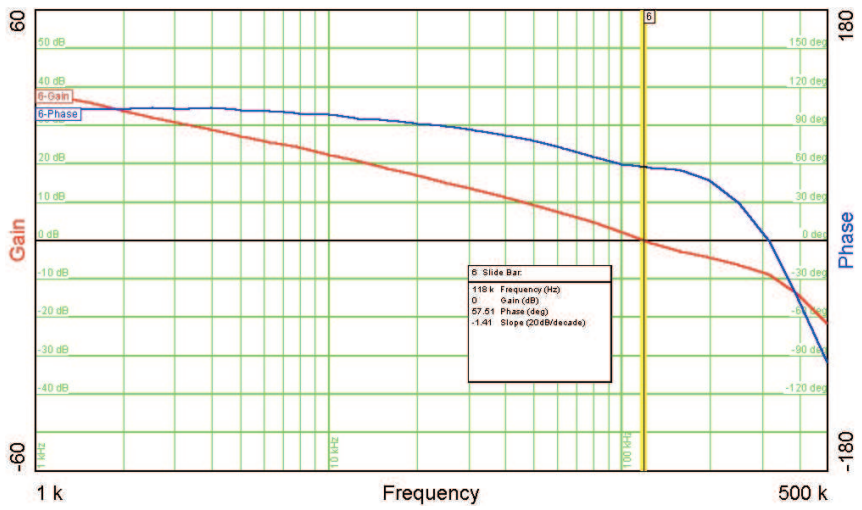

Figure 36. Closed-Loop Response for PMP4854-2

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8.2.3 Application Curves

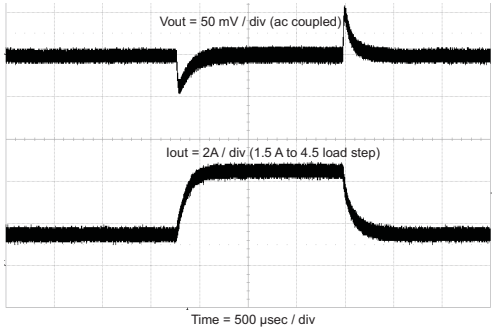

Figure 37. Load Transient

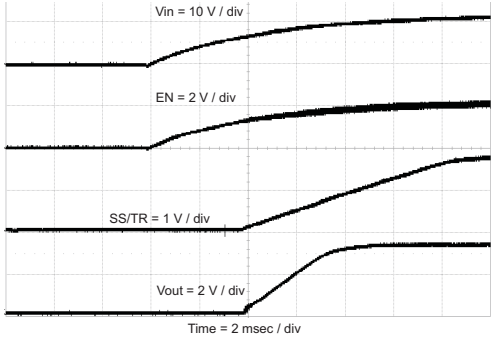

Figure 38. Start-Up With VIN

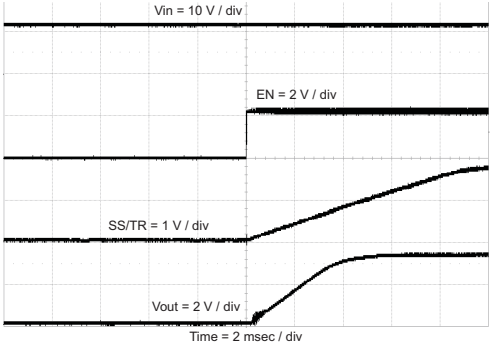

Figure 39. Start-Up With EN

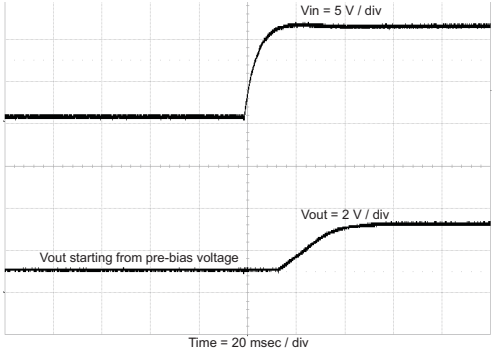

Figure 40. Start-Up With Prebias

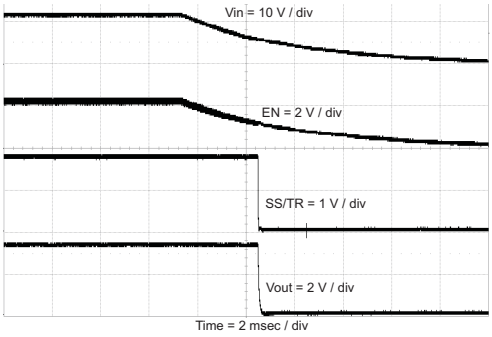

Figure 41. Shutdown With VIN

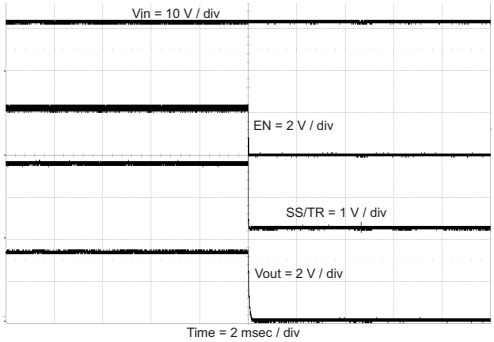

Figure 42. Shutdown With EN

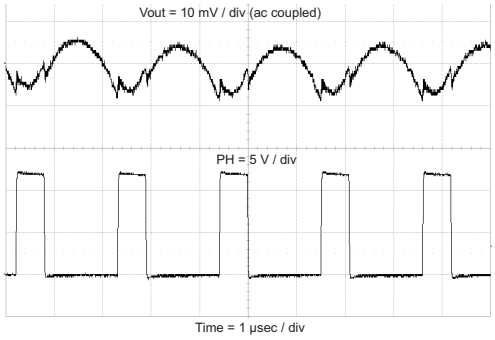

Figure 43. Output Voltage Ripple With No Load

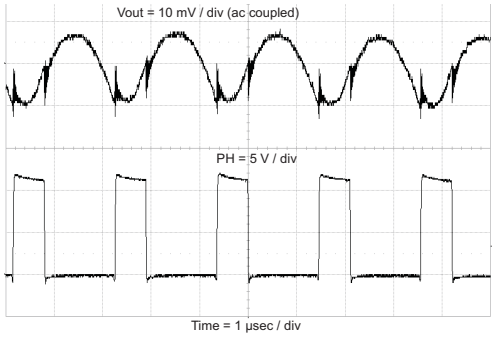

Figure 44. Output Voltage Ripple With Full Load

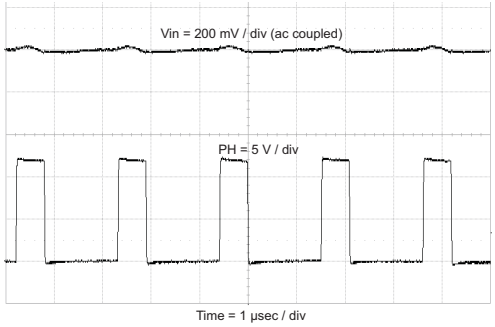

Figure 45. Input Voltage Ripple With No Load

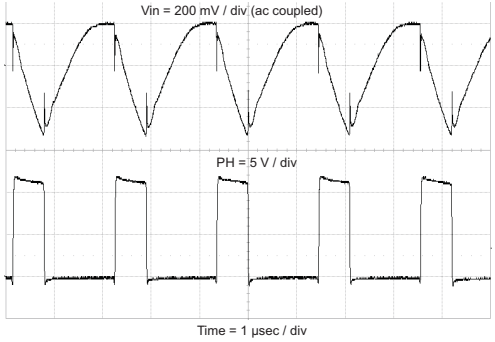

Figure 46. Input Voltage Ripple With Full Load

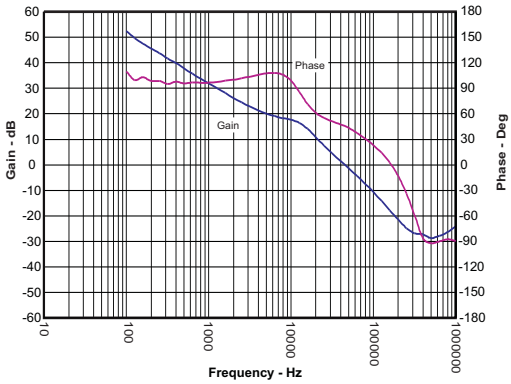

Figure 47. Closed-Loop Response

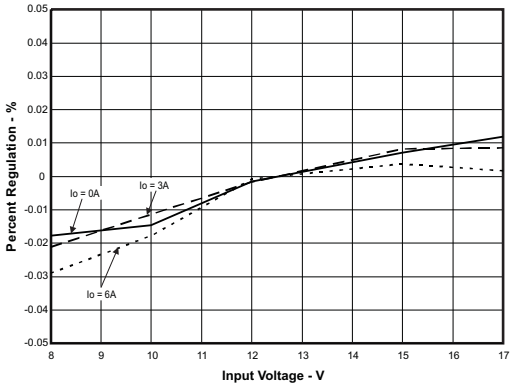

Figure 48. Line Regulation

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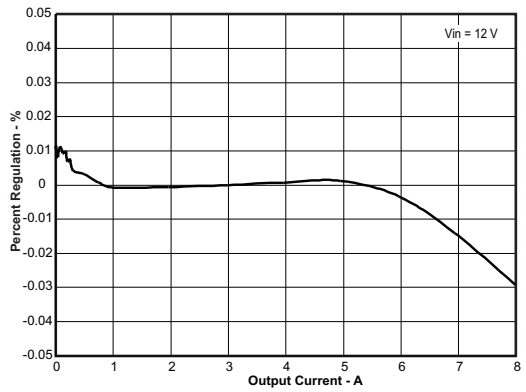

Figure 49. Load Regulation

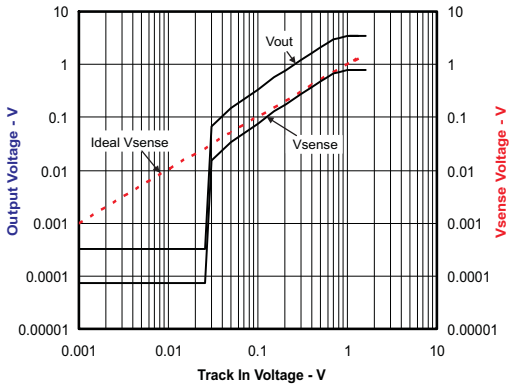

Figure 50. Tracking Performance

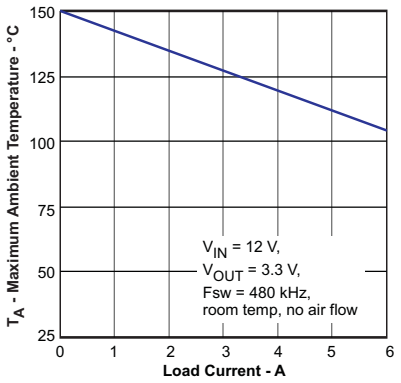

Figure 51. Maximum Ambient Temperature vs Load Current

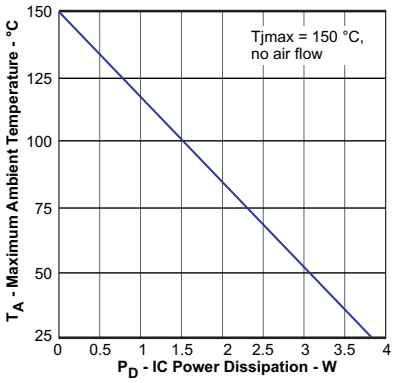

Figure 52. Maximum Ambient Temperature vs IC Power Dissipation

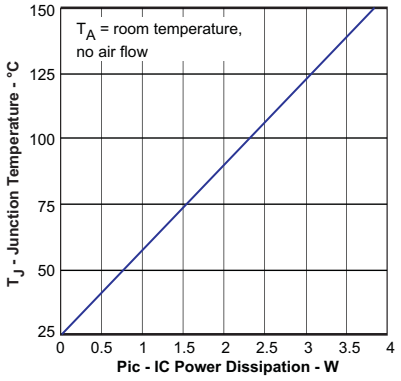

Figure 53. Junction Temperature vs IC Power Dissipation

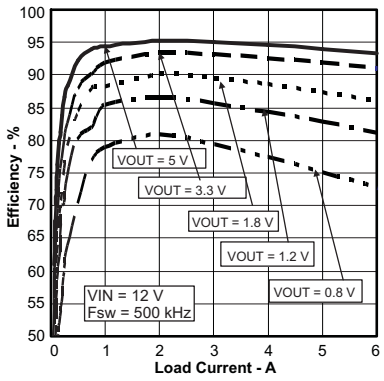

Figure 54. Efficiency vs Load Current

9 Power Supply Recommendations

The TPS54620 is designed to operate from an input voltage supply range between 4.5 V and 17 V. This supply voltage must be well regulated. Power supplies must be well bypassed for proper electrical performance. This includes a minimum of one 4.7-µF (after de-rating) ceramic capacitor, type X5R or better from PVIN to GND, and from VIN to GND. Additional local ceramic bypass capacitance may be required in systems with small input ripple specifications, in addition to bulk capacitance if the TPS54620 device is located more than a few inches away from its input power supply. In systems with an auxiliary power rail available, the power stage input, PVIN, and the analog power input, VIN, may operate from separate input supplies. See Figure 55 (layout recommendation) for recommended bypass capacitor placement.

10 Layout

10.1 Layout Guidelines

- Layout is a critical portion of good power supply design. See Figure 55 for a PCB layout example.
- The top layer contains the main power traces for VIN, VOUT, and VPHASE. Also, on the top layer are connections for the remaining pins of the TPS54620 and a large top-side area filled with ground.
- The top layer ground area must be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS54620 device to provide a thermal path from the exposed thermal pad land to ground.
- The GND pin must be tied directly to the power pad under the IC and the power pad.
- For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance.
- To help eliminate these problems, the PVIN pin must be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric.
- Take care to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections.
- The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric.
- Make sure to connect this capacitor to the quite analog ground trace rather than the power ground trace of the PVIn bypass capacitor.
- Since the PH connection is the switching node, the output inductor must be placed close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground must use the same power ground trace as the PVIN input bypass capacitor.
- Try to minimize this conductor length while maintaining adequate width.
- The small signal components must be grounded to the analog ground path as shown.
- All sensitive analog traces and components such as VSENSE, RT/CLK and COMP must be placed away from high-voltage switching nodes such as PH, BOOT and the output inductor to avoid noise coupling.
- The output voltage sense trace must be connected to the positive terminal of one output capacitor in the design, with the best high frequency characteristics. The output voltage will be most tightly regulated at the voltage sense point.
- The RT/CLK pin is sensitive to noise so the RT resistor must be placed as close as possible to the IC and routed with minimal lengths of trace.
- The additional external components can be placed approximately as shown.
- It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.
- Land pattern and stencil information is provided in the data sheet addendum.
- The dimension and outline information is for the standard RHL (S-PVQFN-N14) package.
- There may be slight differences between the provided data and actual lead frame used on the TPS54620RGY package. The RGY package is identical to the RHL package. The RHL footprint should be used for both packages.

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10.2 Layout Example

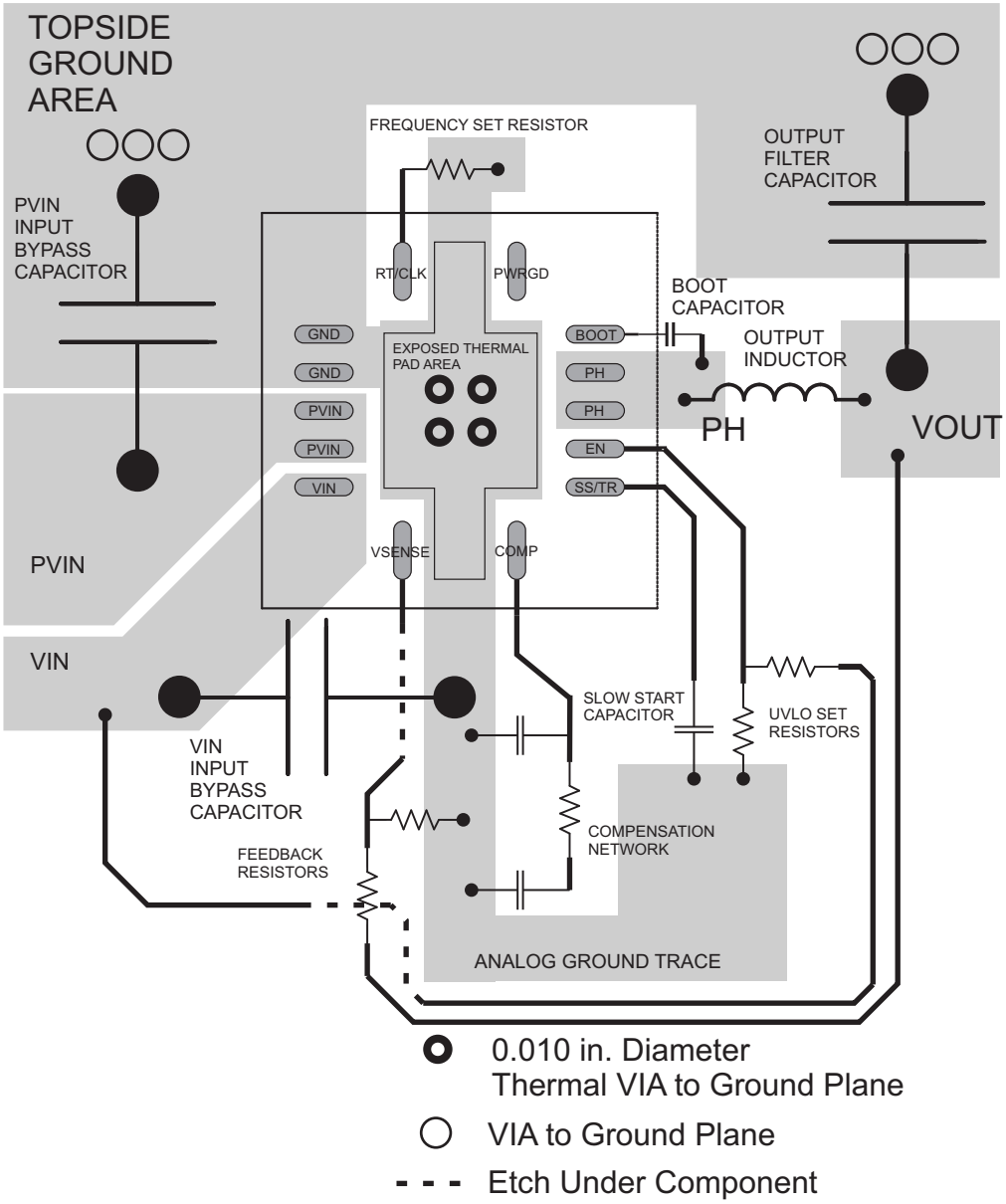

Figure 55. PCB Layout

Layout Example (continued)

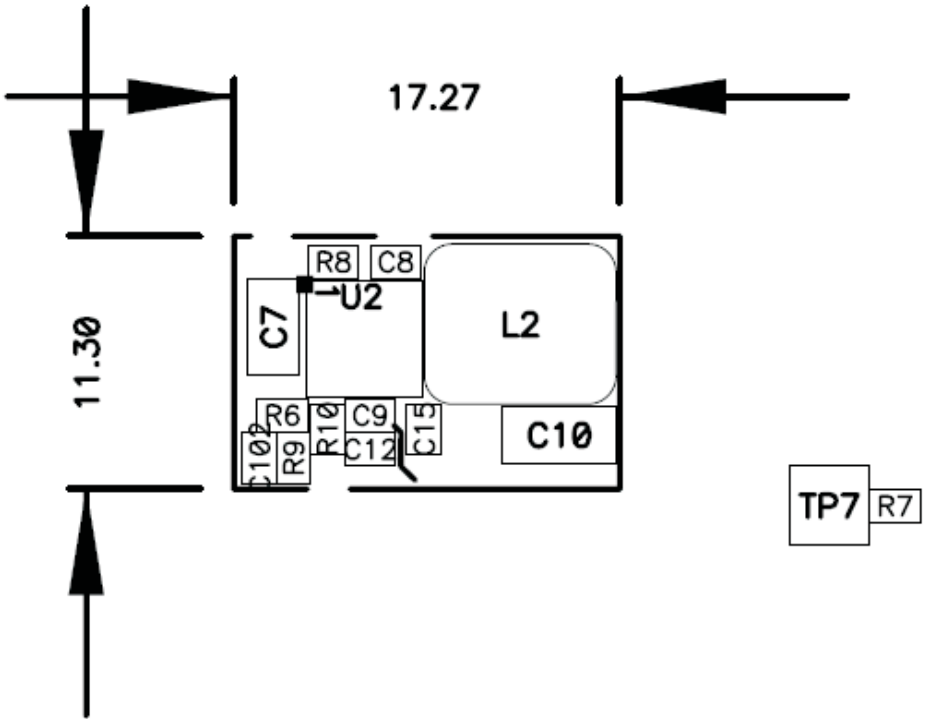

Figure 56. Ultra-Small PCB Layout Using TPS54620 (PMP4854-2)

10.3 Estimated Circuit Area

The estimated printed-circuit board area for the components used in the design of Figure 34 is 0.58. in^2 (374 mm^2). This area does not include test points or connectors.

The board area can be further reduced if size is a big concern in an application. Figure 56 shows the printed circuit board layout for PMP4854-2 as shown in Figure 35 whose board area is as small as 17.27 mm × 11.30 mm.

10.4 Thermal Consideration

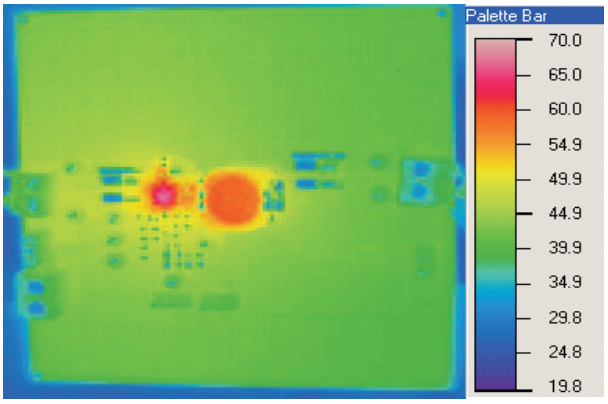

Figure 57. Thermal Signature of TPS54620EVM-374 Operating at V_{IN} = 12 V, V_{OUT} = 3.3 V, 6 A, T_A = Room Temperature

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH Tools

Click here to create a custom design using the TPS54620 device with the WEBENCH® Power Designer.

1. Start by entering the V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize the design for key parameters like efficiency, footprint, and cost by using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides a customized schematic and a list of materials with real-time pricing and component availability.
4. In most cases, users will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share the design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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WEBENCH is a registered trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
905-5462001	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RGYR.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RGYR.B	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RGYRG4	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RGYRG4.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RGYRG4.B	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RGYT	Active	Production	VQFN (RGY) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RGYT.A	Active	Production	VQFN (RGY) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RGYT.B	Active	Production	VQFN (RGY) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RHLR	Active	Production	VQFN (RHL) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RHLR.A	Active	Production	VQFN (RHL) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RHLR.B	Active	Production	VQFN (RHL) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RHLRG4	Active	Production	VQFN (RHL) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RHLRG4.A	Active	Production	VQFN (RHL) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RHLRG4.B	Active	Production	VQFN (RHL) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RHLT	Active	Production	VQFN (RHL) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RHLT.A	Active	Production	VQFN (RHL) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620
TPS54620RHLT.B	Active	Production	VQFN (RHL) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54620

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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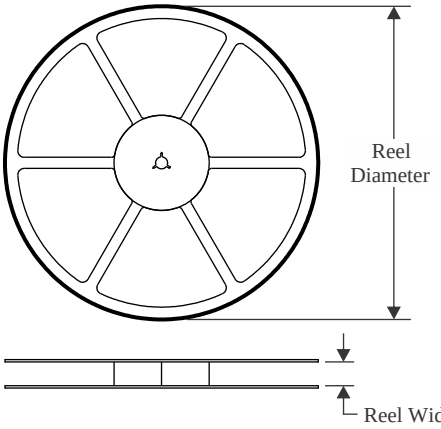
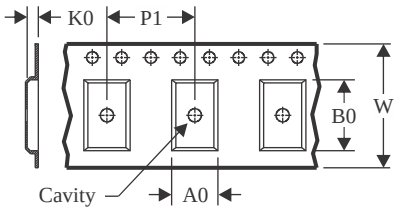
TAPE AND REEL INFORMATION

REEL DIMENSIONS

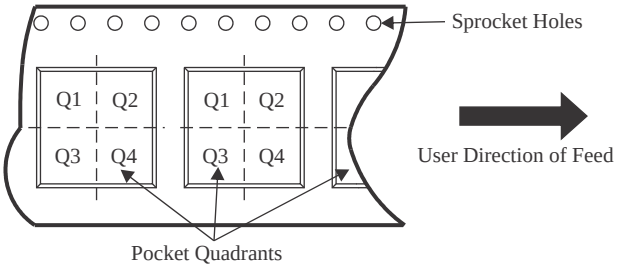


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

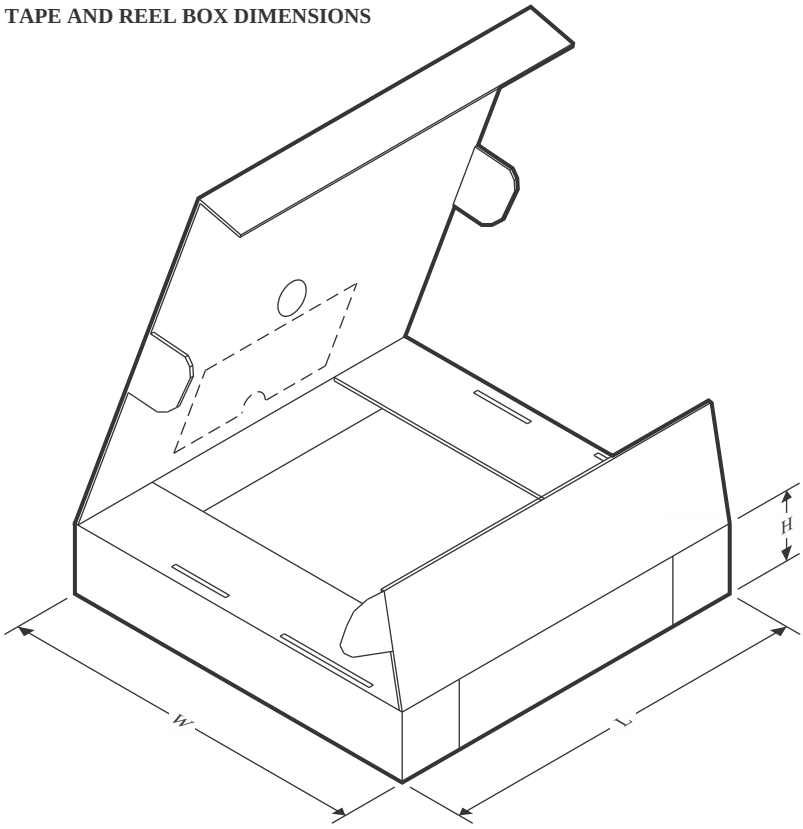
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54620RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS54620RGYRG4	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS54620RGYT	VQFN	RGY	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS54620RGYT	VQFN	RGY	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS54620RHLR	VQFN	RHL	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS54620RHLRG4	VQFN	RHL	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS54620RHLT	VQFN	RHL	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS54620RHLT	VQFN	RHL	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54620RGYR	VQFN	RGY	14	3000	346.0	346.0	33.0
TPS54620RGYRG4	VQFN	RGY	14	3000	346.0	346.0	33.0
TPS54620RGYT	VQFN	RGY	14	250	210.0	185.0	35.0
TPS54620RGYT	VQFN	RGY	14	250	213.0	191.0	35.0
TPS54620RHLR	VQFN	RHL	14	3000	346.0	346.0	33.0
TPS54620RHLRG4	VQFN	RHL	14	3000	346.0	346.0	33.0
TPS54620RHLT	VQFN	RHL	14	250	210.0	185.0	35.0
TPS54620RHLT	VQFN	RHL	14	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

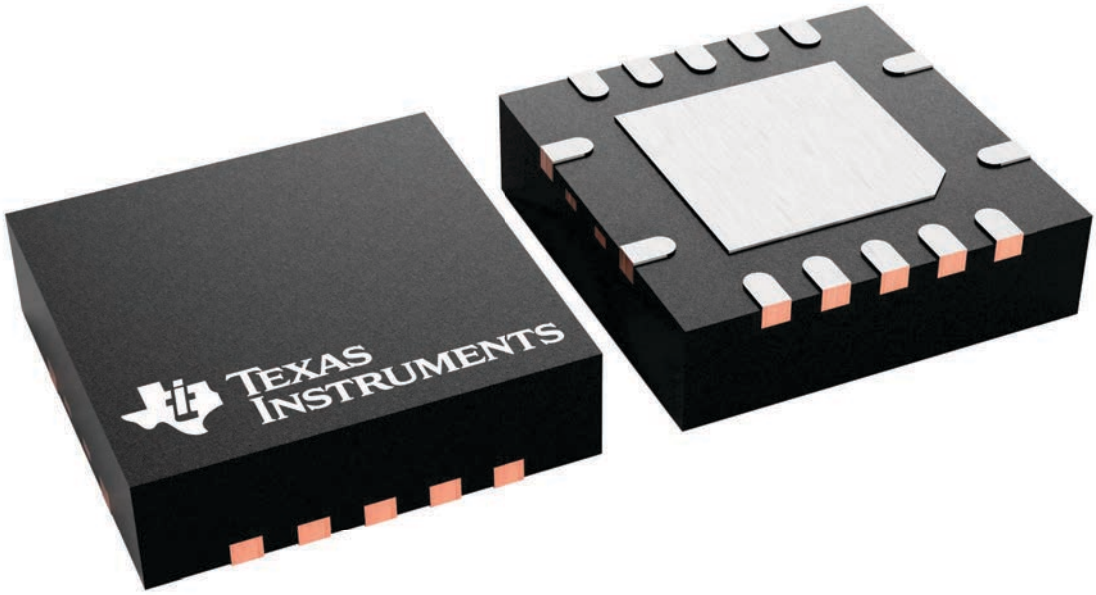
RGY 14

VQFN - 1 mm max height

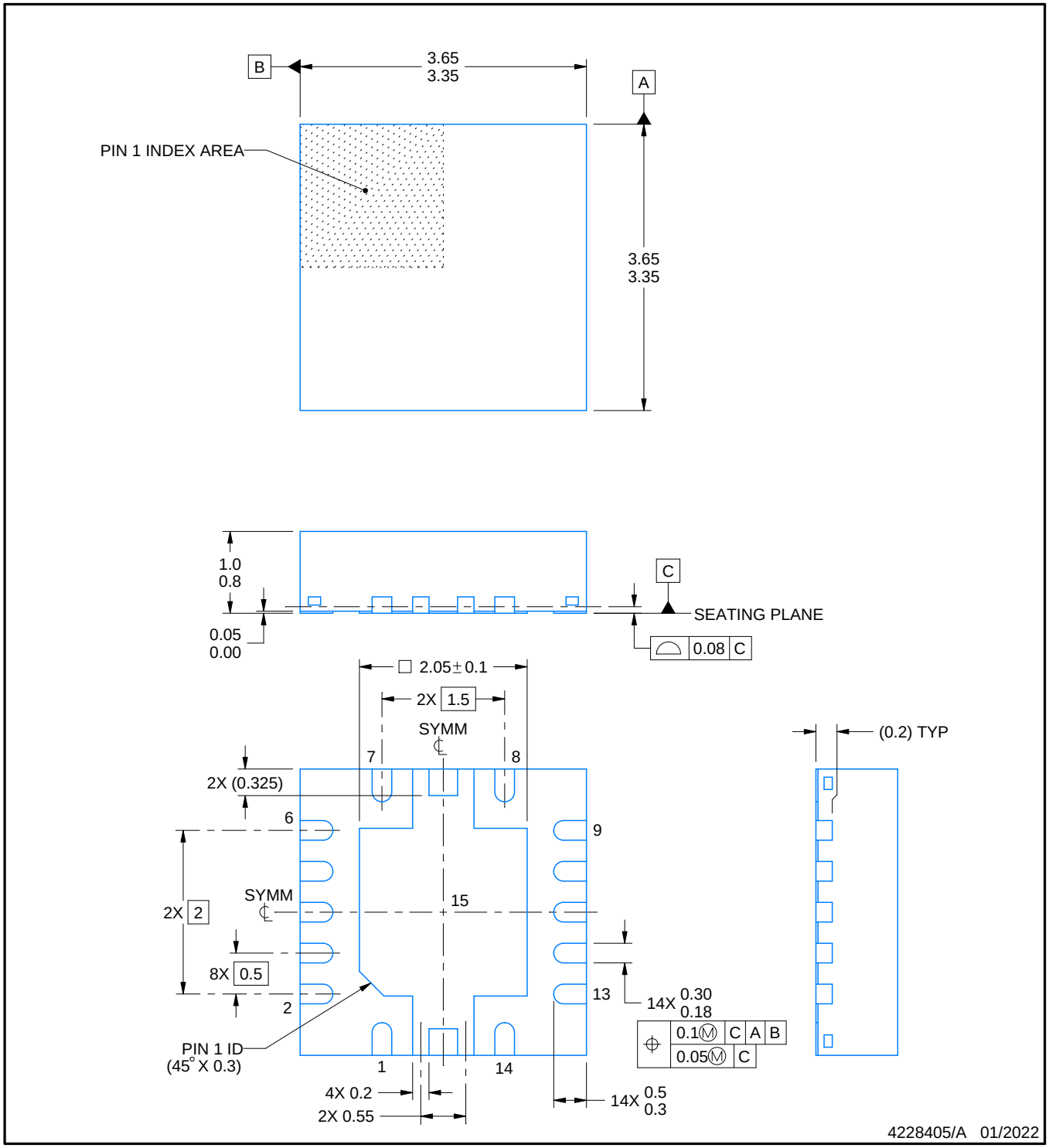
3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

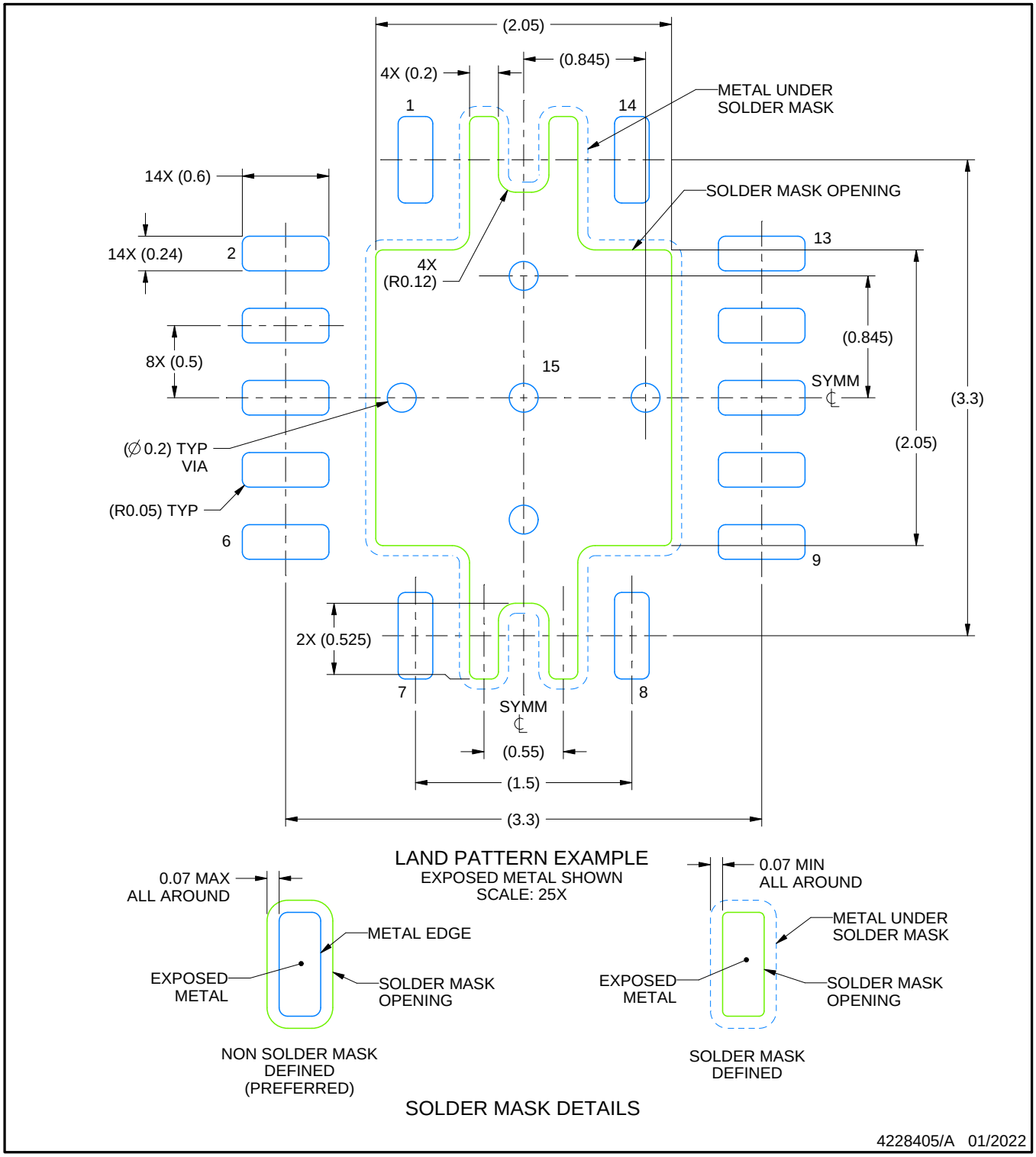


4231541/A



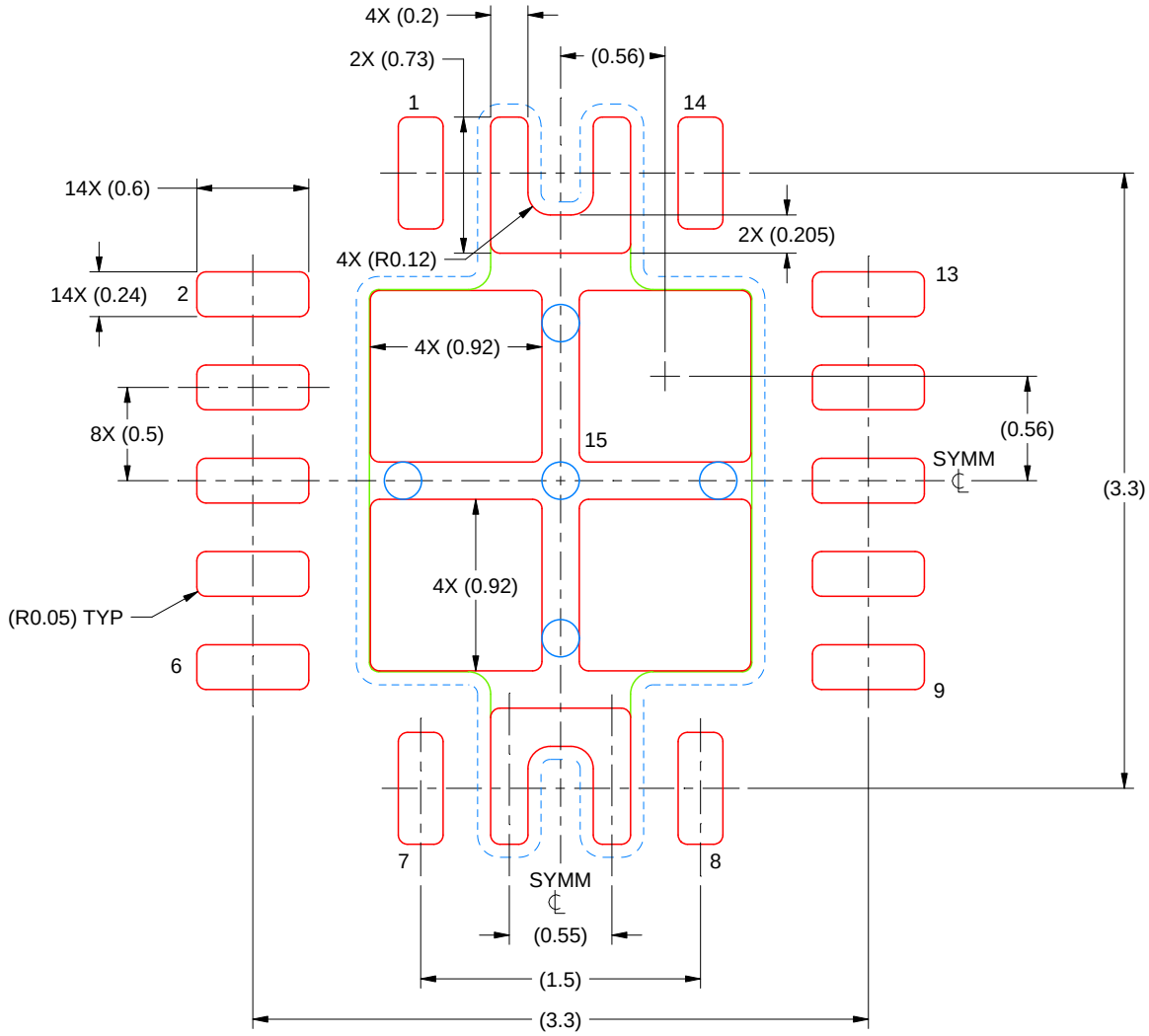
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
79% PRINTED COVERAGE BY AREA
SCALE: 25X

4228405/A 01/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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