TPS546E25 4V to 18V Input, 50A, 4 × Stackable, Synchronous Buck Converter With PMBus® and Telemetry

1 Features

- 2.7V to 18V input voltage with external bias
- 4V to 18V input voltage without external bias
- 0.4V to 5.5V output voltage
- Supports 50A single-phase or 2 ×, 3 ×, or 4 × stacked configurations
- Rds_{on_HS} = 2.6mΩ, Rds_{on_LS} = 1mΩ
- 400kHz to 2MHz operating frequency (four discrete settings through pin-strap, additional settings through PMBus®)
- PMBus programmable
  - Revision 1.5 compliant with PASSKEY security feature
  - Input voltage, output voltage, output current, temperature telemetry
  - Programmable overcurrent, overvoltage, undervoltage, overtemperature protections
  - Includes single command write function in stacked configuration
  - Extended write protection feature
  - Non-volatile memory to store configuration settings
- Two methods for programming the output voltage
  - Internal resistor divider (discrete settings) with boot-up voltage selected by pin-strapping
  - External resistor divider (continuous settings) with boot-up voltage selected by VBOOT
- Precision voltage reference and differential remote sense for high output accuracy
  - ± 0.5% DAC accuracy from 0°C to 85°C junction
  - ± 0.85% VOUT tolerance from –40°C to 125°C junction
- Selectable FCCM/DCM in single phase only
- Start-up without PMBus communication through pin-strapping
- Safe start-up into prebiased output
- 0.5ms to 16ms programmable soft-start time
- D-CAP4 control topology with fast transient response, supporting all ceramic output capacitors
- Programmable internal loop compensation
- Selectable cycle-by-cycle valley current limit
- Open-drain power-good output

2 Applications

- Server and cloud-computing POLs
- Hardware accelerator
- Network interface card (NIC)

3 Description

The TPS546E25 device is a highly integrated, buck converter with D-CAP4 control topology for fast transient response. All programmable parameters can be configured by the PMBus interface and stored in NVM as the new default values to minimize the external component count. Pin-strap options allow for configuration as primary or secondary, stack position and stack number, DCM (single phase only) or FCCM, overcurrent limit, fault response, internal or external feedback resistor, output voltage selection or range, switching frequency, and compensation.

The PMBus interface with 1MHz clock support gives a convenient, standardized digital interface for configuration as well as telemetry of key parameters including output voltage, output current, and internal die temperature. Response to fault conditions can be set to restart, latch off, or ignore, depending on system requirements. Two, three, and four TPS546E25 devices can be interconnected to provide up to 200A on a single output.

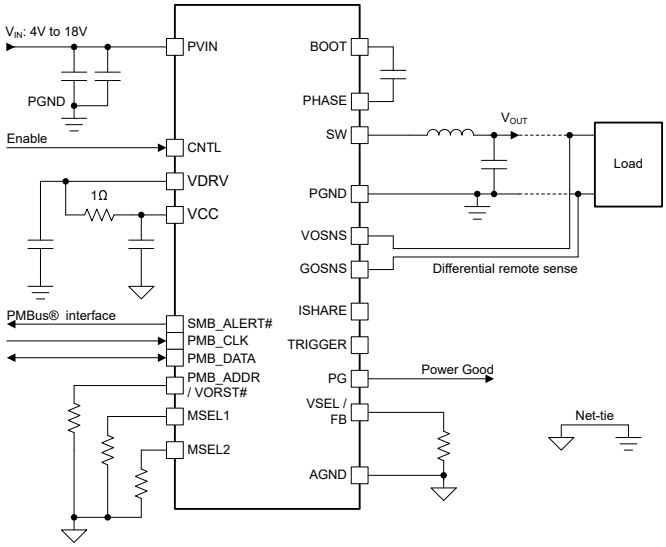
The TPS546E25 has an option to overdrive the internal 4.5V LDO with an external 5V supply through the VDRV and VCC pins to improve efficiency, reduce power dissipation, and enable start-up with a lower input voltage.

The TPS546E25 is a lead-free device and is RoHS compliant without exemption.

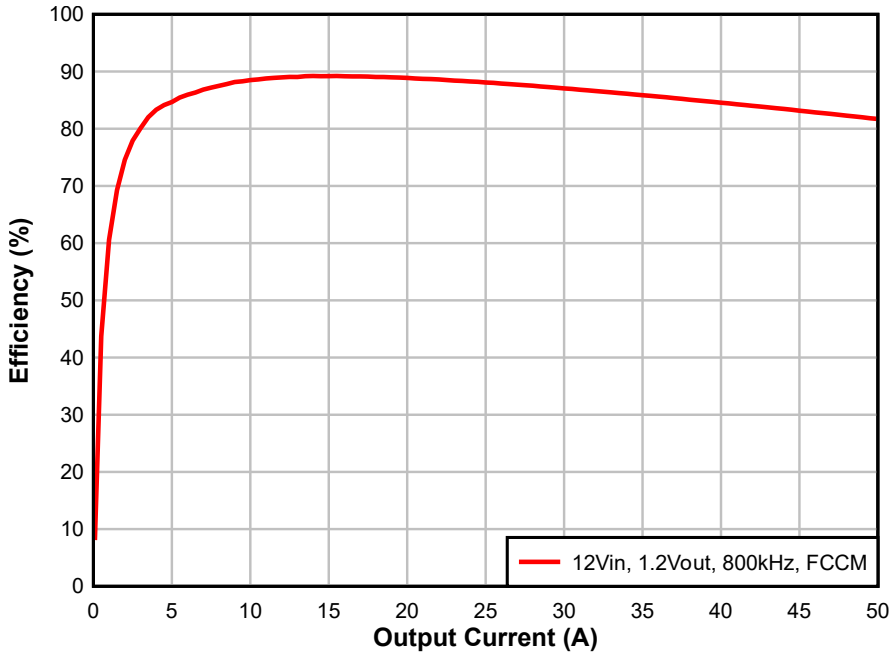
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS546E25	RXX (WQFN-FCRLF, 37)	6mm × 5mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic



Typical Efficiency

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4 Pin Configuration and Functions

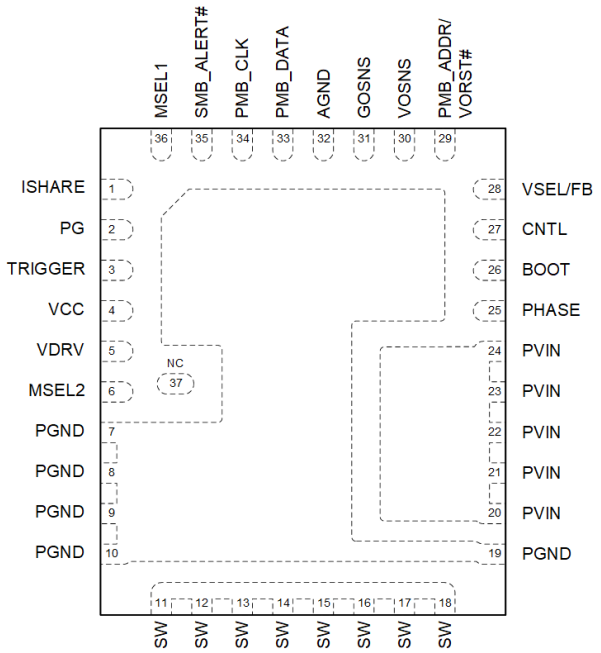


Figure 4-1. RXX 37-Pin WQFN-FCRLF Package (Top View)

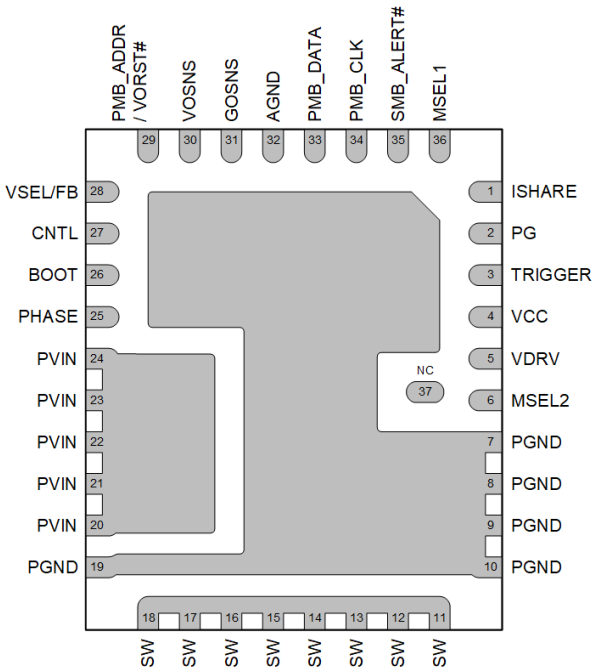


Figure 4-2. RXX 37-Pin WQFN-FCRLF Package (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	32	G	Analog ground pin, reference point for internal control circuitry
BOOT	26	P	Supply rail for the high-side gate driver (boost terminal). Connect the bootstrap capacitor from this pin to PHASE pin. TI recommends a 10V, X7R or better, 0.1µF or greater value ceramic capacitor. The capacitor must have at least 50nF of capacitance after DC bias derating at 5V.
CNTL	27	I	CTRL pin, an active-high input pin that, when asserted high, causes the converter to begin the soft-start sequence for the output voltage rail.
GOSNS	31	I	Negative input of the differential remote sense circuit, connect to the ground sense point on the load side.
ISHARE	1	I/O	ISHARE pin for stackable configuration. Tie this pin to other ISHARE pins in the stack. Do not connect (float) in standalone configuration.
MSEL1	36	I	Use a resistor to AGND to select primary, secondary device, internal, external feedback, current limit, and fault response options. See *Pin-Strapping*.
MSEL2	6	I	Use a resistor to AGND to select switching frequency, ramp, and gain compensation options for the device. See *Pin-Strapping*.
NC	37		Not connected. This pin is floating internally.
PG	2	O	Open-drain power-good indicator
PGND	7, 8, 9, 10, 19	G	Power ground for the internal power stage
PHASE	25	I/O	Return for high-side MOSFET driver. Shorted to SW internally. Connect the bootstrap capacitor from BOOT pin to PHASE pin.
PMB_ADDR/ VORST#	29	I	Use a resistor to AGND to select the PMBus address light load operating mode, DCM or FCCM, and multiphase stacking options. See Pin-Strapping.
PMB_CLK	34	I	PMBus clock pin, open drain
PMB_DATA	33	I/O	PMBus bi-directional data pin, open drain

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
PVIN	20, 21, 22, 23, 24	P	Power input for both the power stage and the input of the internal VCC LDO
SMB_ALERT_#	35	O	SMBALERT# as described in the SMBus specification. The pin is open-drain. The SMBALERT# indicator is used in conjunction with the Alert Response Address (ARA). During nominal operation, the SMBALERT# is held high.
SW	11 – 18	O	Output switching terminal of the power converter. Connect these pins to the output inductor.
TRIGGER	3	I/O	TRIGGER pin for stackable configuration. Tie this pin to other TRIGGER pins in the stack. Do not connect (float) in standalone configuration.
VCC	4	P	Output of internal 4.5V LDO from PVIN and Supply for analog control circuitry. Bypass with a 10V rated X5R or better 2.2µF capacitor to AGND and connect to VDRV with a 1Ω resistor. Check layout guidelines for more details.
VDRV	5	—	5V supply for gate drivers. Bypass to PGND with a 10V rated X5R or better 2.2µF and connect to VCC with a 1Ω resistor. An external 5V bias can be connected to this pin to reduce power losses on the internal LDO or to allow operation with a lower PVIN voltage. Check layout guidelines for more details.
VOSNS	30	I	Output voltage sense pin and positive input of the differential remote sense circuit. For both internal and external feedback, connect VOSNS to the Vout sense point with no more than 100Ω of resistance.
VSEL/FB	28	I	When the device is configured to use the internal FB divider, this pin is VSEL. Use a resistor to AGND to select the output voltage. See *Programming MSEL1* and *Programming VSEL\FB*. When the device is configured for an external resister divider, this pin is the feedback pin of the device. Connect this pin to VOSNS and GOSNS with a resistor divider to set the output voltage. See *Layout Guidelines*

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	PVIN - PGND	–0.3	19	V
Pin voltage	SW – PGND, DC	–0.3	19	V
Pin voltage	SW – PGND, transient < 10ns	–3.0	21	V
Pin voltage	PVIN – SW, DC	–0.3	20	V
Pin voltage	PVIN – SW, transient < 10ns	–3.0	24	V
Pin voltage	BOOT – PGND	–0.3	25	V
Pin voltage	BOOT – SW, BOOT - PHASE	–0.3	5.5	V
Pin voltage	VDRV – PGND, VCC - AGND	–0.3	5.5	
Pin voltage	GOSNS – AGND	–0.3	0.3	
Pin voltage	AGND – PGND	–0.3	0.3	V
Pin voltage	MSEL1, MSEL2, PMB_ADDR/VORST#, VSEL/FB, VOSNS	–0.3	5.5	V
Pin voltage	PG, TRIGGER	–0.3	5.5	
Pin voltage	ISHARE	–0.3	1.98	V
Pin voltage	PMB_CLK, PMB_DATA, SMB_ALERT, CNTL	–0.3	5.5	V
Sink current	PG		10	mA
Sink current	PMB_CLK, PMB_DATA, SMB_ALERT		22	mA
T_{stg}	Storage temperature	–55	150	°C
T_J	Operating junction temperature	–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{PVIN}	Pin voltage	PVIN - PGND voltage range	4		18	V
V_{VCC}	Internal LDO pin voltage	Internal LDO		4.5		V
V_{VCC}	External bias pin voltage	External bias voltage allowed	4.7		5.3	V
V_{PVIN}	Pin voltage	VCC biased with 4.7V to 5.3V	2.7		18	V
	Pin voltage with respect to PGND	VDRV		4.5		V
	Pin voltage with respect to AGND	CNTL	1.1	1.2		V
	Pin voltage with respect to AGND	PMB_CLK, PMB_DATA, SMB_ALERT	–0.1	1.8	5.25	V
	Pin voltage	AGND - PGND		0		V
	Pin voltage	AGND - GOSNS	–100		100	mV
I_{OUT}	Output current range		0		50	A
I_{PMB}	PMBus pin sink current	PMB_CLK, PMB_DATA, SMB_ALERT			20	mA

5.3 Recommended Operating Conditions (continued)

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
I_{PG}	Power-good sink current capability		0		5	mA
T_J	Operating junction temperature		–40		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPS546E25		UNIT
		RXX 37-pin QFN		
		JEDEC 51-7 PCB	TPS546E25EVM-1PH	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26	14	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.4	n/a[2]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.6	n/a[2]	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.15	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.6	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application note*.
(2) The thermal simulation setup is not applicable to a TI EVM layout.

5.5 Electrical Characteristics

T_J = –40°C to +125°C. PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
$I_{Q(PVIN)}$	PVIN quiescent current	Non-switching, PVIN = 12V, V_{CTRL} = 0V, no external bias on VCC/VDRV pin			10		mA
$I_{SD(PVIN)}$	PVIN shutdown supply current	PVIN = 12V, V_{EN} = 0V, no bias on VCC and VDRV pins			20		µA
I_{VCC}	VCC external bias current	5V external bias on VCC+VDRV, regular switching. T_J = 25°C, PVIN = 12V, V_{OUT} = 1.1V, V_{EN} = 2V, f_{SW} = 1MHz	f_{SW} = 1MHz		10		mA
I_{VDRV}	VDRV external bias current	5V external bias on VCC+VDRV, regular switching. T_J = 25°C, PVIN = 12V, V_{OUT} = 1.1V, V_{EN} = 2V, f_{SW} = 1MHz	f_{SW} = 1MHz		40		mA
$I_{Q(VDRV)}$	VCC+VDRV quiescent current	5V external bias on VCC+VDRV, non-switching. PVIN = 12V, V_{EN} = 0V			8.5		mA
INPUT UVLO AND OV							
$PVIN_{OV}$	PVIN overvoltage threshold (55h) VIN_OV_FAULT_LIMIT	(55h) VIN_OV_FAULT_LIMIT = 16.5V		15.9	16.5		V
		(55h) VIN_OV_FAULT_LIMIT = 18.5V		18.9	19.5		V
$PVIN_{OV}$	PVIN overvoltage falling threshold to clear the PVIN_OVF status bit once set.	PVIN falling			13.5		V
VIN_ON	PVIN turn-on voltage (35h) VIN_ON	PVIN rising (See Supported PMBus Commands for Default)	(35h) VIN_ON = 10V		10		V
			(35h) VIN_ON = 9V		9		V
			(35h) VIN_ON = 8V		8		V
VIN_ON			(35h) VIN_ON = 7V		7		V
			(35h) VIN_ON = 6V		6		V
			(35h) VIN_ON = 5V		5		V
			(35h) VIN_ON = 3.8V		3.8		V
			(35h) VIN_ON = 2.5V		2.5		V

5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C. PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VIN_OFF	PVIN turn-off voltage (36h) VIN_OFF	PVIN falling (See Supported PMBus Commands for Default)	(36h) VIN_OFF = 9.5V		9.5		V
			(36h) VIN_OFF = 8.5V		8.5		V
			(36h) VIN_OFF = 7.5V		7.5		V
			(36h) VIN_OFF = 6.5V		6.5		V
			(36h) VIN_OFF = 5.5V		5.5		V
			(36h) VIN_OFF = 4.2V		4.2		V
			(36h) VIN_OFF = 3.6V		3.6		V
			(36h) VIN_OFF = 2.3V		2.3		V
$T_{DGLTCH(ON)}$	VIN_ON deglitch time				50		µs
$T_{DGLTCH(OFF)}$	VIN_OFF deglitch time				5		µs
ENABLE							
$V_{EN(R)}$	CTRL voltage rising threshold	CTRL rising, enable switching			1.2	1.3	V
$V_{EN(F)}$	CTRL voltage falling threshold	CTRL falling, disable switching		0.9	1.0		V
$V_{EN(H)}$	CTRL voltage hysteresis				0.2		V
$t_{EN(DGLTCH)}$	CTRL deglitch time (1)			0.2			µs
$R_{EN(PD)}$	CTRL internal pulldown resistor (CTRL to AGND)	VEN = 2V, CTRL pin to AGND		110	125	140	kΩ
INTERNAL VCC LDO							
$V_{VCC(LDO)}$	Internal VCC LDO output voltage	PVIN = 4V, $I_{VCC(load)}$ = 5mA	PVIN = 4V, $I_{VCC(load)}$ = 5mA	3.925	3.97	4.0	V
$V_{VCC(LDO)}$	Internal VCC LDO output voltage	PVIN = 5V to 18V, $I_{VCC(load)}$ = 5mA		4.28	4.44	4.55	V
$V_{VCC(ON)}$	VCC UVLO rising threshold	VCC rising		3.70	3.80	3.86	V
$V_{VCC(OFF)}$	VCC UVLO falling threshold	VCC falling		3.50	3.60	3.65	V
$V_{VCC(DO)}$	VCC LDO dropout voltage	PVIN – V_{VCC}, PVIN = 4V, $I_{VCC(load)}$ = 45mA		90	144	226	mV
$I_{VCC(SC)}$	VCC LDO short-circuit current limit	PVIN = 12V		150	200		mA
VOUT VOLTAGE							
$V_{OUT(ACC)}$	Output voltage regulation accuracy	T_J = 0°C to 85°C	V_{OUT} = 0.5V, VOSL = 1, V_{VOSNS} – V_{GOSNS}	0.496	0.5	0.504	V
			V_{OUT} = 1V, VOSL = 0.5, V_{VOSNS} – V_{GOSNS}	0.995	1	1.005	V
			V_{OUT} = 1.8V, VOSL = 0.25, V_{VOSNS} – V_{GOSNS}	1.791	1.8	1.809	V
			V_{OUT} = 3.3V, VOSL = 0.125, V_{VOSNS} – V_{GOSNS}	3.284	3.3	3.316	V
		T_J = –40°C to 125°C	V_{OUT} = 0.5V, VOSL = 1, V_{VOSNS} – V_{GOSNS}	0.494	0.5	0.506	V
			V_{OUT} = 1V, VOSL = 0.5, V_{VOSNS} – V_{GOSNS}	0.9915	1	1.0085	V
			V_{OUT} = 1.8V, VOSL = 0.25, V_{VOSNS} – V_{GOSNS}	1.784	1.8	1.816	V
			V_{OUT} = 3.3V, VOSL = 0.125, V_{VOSNS} – V_{GOSNS}	3.271	3.3	3.329	V
I_{VOS}	VOSNS input current	V_{VOSNS} = 1.8V, VOSL = 0.25			60	100	µA
V_{OUTRES}		Resolution of VOUT_COMMAND and VOUT_TRIM			1.953		mV
VOSL	VOUT_SCALE_LOOP. Internal feedback loop scaling factor.	Programmable range, 4 discrete settings		0.125		1	
VOUT_TRIM	Programmable range			-125		123	mV
VOUT_TR	Output voltage transition rate accuracy	VOUT_TRANSITION_RATE = 10mV/µs		8.8	9.77	10.7	mV/µs
SWITCHING FREQUENCY							

5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C. PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{SW(FCCM)}$	Switching frequency (33h) FREQUENCY_SWITCH	PVIN = 12V, FCCM, V_{OUT} = 1.1V, no load	(33h) FREQUENCY_SWITCH = 000b		400	440	kHz
			(33h) FREQUENCY_SWITCH = 001b	510	600	660	kHz
			(33h) FREQUENCY_SWITCH = 010b	680	800	920	kHz
			(33h) FREQUENCY_SWITCH = 011b	850	1000	1150	kHz
			(33h) FREQUENCY_SWITCH = 100b	1020	1200	1440	kHz
			(33h) FREQUENCY_SWITCH = 101b		1400		kHz
			(33h) FREQUENCY_SWITCH = 110b		1800		kHz
			(33h) FREQUENCY_SWITCH = 111b		2000		kHz
STARTUP AND SHUTDOWN TIMING							
$t_{ON(DLY)}$	Power on sequence delay, (60h) TON_DELAY (See Supported PMBus Commands for Default)	V_{VCC} = 4.5V	TON_DELAY = 0ms		0.05	0.1	ms
			TON_DELAY = 0.5ms		0.5	0.55	ms
			TON_DELAY = 1.0ms		1.0	1.1	ms
			TON_DELAY = 2.0ms		2.0	2.2	ms
$t_{ON(Rise)}$	Soft-start time, (61h) TON_RISE (See Supported PMBus Commands for Default)	V_{VCC} = 4.5V	TON_RISE = 0.5ms		0.5	0.55	ms
			TON_RISE = 1.0ms		1.0	1.1	ms
			TON_RISE = 2.0ms		2.0	2.2	ms
			TON_RISE = 4.0ms		4.0	4.4	ms
			TON_RISE = 8.0ms		8.0	8.8	ms
			TON_RISE = 16.0ms		16.0	17.6	ms
$t_{OFF(DLY)}$	Power off sequence delay, (64h) TOFF_DELAY (See Supported PMBus Commands for Default)	V_{VCC} = 4.5V	TOFF_DELAY = 0ms		0	0.05	ms
			TOFF_DELAY = 1.0ms		1.0	1.1	ms
			TOFF_DELAY = 1.5ms		1.5	1.65	ms
			TOFF_DELAY = 2.0ms		2.0	2.2	ms
$SR_{(Fall)}$	Soft-stop slew rate, (65h) TOFF_FALL(See Supported PMBus Commands for Default)	V_{VCC} = 4.5V, VOSL = 0.5 VDACBOOT = 0.55V	TOFF_FALL = 0.5ms		-2.22		mV/µs
			TOFF_FALL = 1ms		-1.11		mV/µs
			TOFF_FALL = 2ms		-0.56		mV/µs
			TOFF_FALL = 4ms		-0.28		mV/µs
		V_{VCC} = 4.5V, VOSL = 0.25 VDACBOOT = 0.45V	TOFF_FALL = 0.5ms		-3.64		mV/µs
			TOFF_FALL = 1ms		-1.82		mV/µs
			TOFF_FALL = 2ms		-0.91		mV/µs
			TOFF_FALL = 4ms		-0.46		mV/µs
POWER STAGE							
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C, PVIN = 12V, $V_{BOOT-PHASE}$ = 4.5V			2.55		mΩ
		T_J = 25°C, PVIN = 12V, $V_{BOOT-PHASE}$ = 5V			2.47		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C, PVIN = 12V, $V_{VCC/VDRV}$ = 4.5V			0.97		mΩ
		T_J = 25°C, PVIN = 12V, $V_{VCC/VDRV}$ = 5V			0.94		mΩ
$t_{ON(min)}$	Minimum ON pulse width	$V_{VCC/VDRV}$ = 4.5V			30		ns
$t_{OFF(min)}$	Minimum OFF pulse width	$V_{VCC/VDRV}$ = 4.5V, I_O =1.5A, V_{OUT} = $V_{OUT(set)}$ – 20mV, SW falling edge to rising edge			210		ns
BOOTSTRAP CIRCUIT							
$I_{BOOT(LKG)}$	BOOT leakage current	V_{EN} = 2V, $V_{BOOT-PHASE}$ = 5V				150	µA
$V_{BT-PH(UV\_F)}$	BOOT-PHASE UVLO falling threshold				3		V
OVERCURRENT PROTECTION							

5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C. PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{LS(OC)}$	Low-side MOSFET valley overcurrent limit, (46h) IOUT_OC_FAULT_LIMIT (See Supported PMBus Commands for Default)	IOUT_OC_FAULT_LIMIT = 12A		11	12.5	14	A
		IOUT_OC_FAULT_LIMIT = 15A(1)		13.5	15	16.5	A
		IOUT_OC_FAULT_LIMIT = 18A(1)		16.5	18.75	21	A
		IOUT_OC_FAULT_LIMIT = 24A(1)		21	23.75	26	A
		IOUT_OC_FAULT_LIMIT = 26A(1)		23.5	26.25	29	A
		IOUT_OC_FAULT_LIMIT = 30A		27	30	33	A
		IOUT_OC_FAULT_LIMIT = 35A(1)		31	35	38.5	A
		IOUT_OC_FAULT_LIMIT = 37A(1)		33.5	37.5	41.5	A
		IOUT_OC_FAULT_LIMIT = 40A		36	40	44	A
		IOUT_OC_FAULT_LIMIT = 44A(1)		39	43.75	48	A
		IOUT_OC_FAULT_LIMIT = 49A(1)		43.5	48.75	54	A
		IOUT_OC_FAULT_LIMIT = 50A		45	50	55	A
		IOUT_OC_FAULT_LIMIT = 55A(1)		49	55	60.5	A
		IOUT_OC_FAULT_LIMIT = 60A(1)		54	60	66	A
$I_{(OCW)}$	Average output current warning, (4Ah) IOUT_OC_WARN_LIMIT (See Supported PMBus Commands for Default)	IOUT_OC_WARN_LIMIT = 5A(1)			5		A
		IOUT_OC_WARN_LIMIT = 10A(1)			10		A
		IOUT_OC_WARN_LIMIT = 15A(1)			15		A
		IOUT_OC_WARN_LIMIT = 20A(1)			20		A
		IOUT_OC_WARN_LIMIT = 25A(1)			25		A
		IOUT_OC_WARN_LIMIT = 30A(1)			30		A
		IOUT_OC_WARN_LIMIT = 35A(1)			35		A
		IOUT_OC_WARN_LIMIT = 40A(1)			40		A
		IOUT_OC_WARN_LIMIT = 45A(1)			45		A
		IOUT_OC_WARN_LIMIT = 50A(1)			50		A
		IOUT_OC_WARN_LIMIT = 55A(1)			55		A
$I_{LS(NOC)}$	Low-side MOSFET negative overcurrent limit, (See Supported PMBus Commands for Default)		SEL_UCF = 00b(1)		–30		A
			SEL_UCF = 01b(1)		–25		A
			SEL_UCF = 01b(1)		–20		A
			SEL_UCF = 01b(1)		–10		A
STACKING INTERFACE							
$V_{IH(TRIG)}$	High-level Primary detection input voltage	Secondary device TRIG input to determine rimary device synchronization		2.5	3.2		V
$V_{IL(sync)}$	Low-level input voltage triggering	Secondaty device TRIG input to determine triggering			1.85	2.3	V
$V_{OHH(TRIG)}$	TRIGGER output high voltage for Primary synchronization			2.5	3.2		V
	Minimum pulse width detection of TRIGGER pulse	Secondary device input		10			ns
	Minimum pulse width of TRIGGER pulse	Primary device output		25			ns
CURRENT SHARING							
$I_{SHARE(acc)}$	Output current sharing accuracy of two devices defined as the ratio of the current difference between two devices to the sum of the two	I_{OUT} ≥ 20A per device (1)		–10%		+10%	%
	V_{ISHARE} fault trip threshold				200mV		V
$I_{SHARE(acc)}$	Output current sharing accuracy of two devices defined as the current difference between each device and the average of all devices	I_{OUT} < 20A per device (1)		–2		2	A
	V_{ISHARE} fault release threshold						V
OUTPUT OVF/UVF							
V_{OVF}	Vout overvoltage fault (OVF) threshold, (40h) VOUT_OV_FAULT_LIMIT (See Supported PMBus Commands for Default)	(VOSNS – GOSNS) rising	VOUT_OV_FAULT_LIMIT = 573d		112%		VOC
			VOUT_OV_FAULT_LIMIT = 594d		116%		VOC
			VOUT_OV_FAULT_LIMIT = 614d		120%		VOC
			VOUT_OV_FAULT_LIMIT = 717d		150%		VOC

5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C. PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OVF(acc)}$	Vout OVF accuracy	(VOSNS – GOSNS) rising		–3%		3%	VOC
V_{UVF}	Vout undervoltage fault (UVF) threshold, (44h) VOUT_UV_FAULT_LIMIT (See Supported PMBus Commands for Default)	(VOSNS – GOSNS) falling	VOUT_UV_FAULT_LIMIT = 430d		84%		VOC
			VOUT_UV_FAULT_LIMIT = 389d		76%		VOC
			VOUT_UV_FAULT_LIMIT = 348d		68%		VOC
			VOUT_UV_FAULT_LIMIT = 307d		60%		VOC
$V_{OVF(acc)}$	Vout UVF accuracy	(VOSNS – GOSNS) falling		–3%		3%	VOC
	Vout UVF and UVW delay time (See Supported PMBus Commands for Default)	(45h) VOUT_UV_FAULT_RESPONSE<2:0> = x00b			2		µs
		(45h) VOUT_UV_FAULT_RESPONSE<2:0> = x01b			16		µs
		(45h) VOUT_UV_FAULT_RESPONSE<2:0> = x10b			64		µs
		(45h) VOUT_UV_FAULT_RESPONSE<2:0> = x11b			256		µs
T_{HICCUP}	Hiccup sleep time before a restart. Applicable to all faults with hiccup response option.	(45h) VOUT_UV_FAULT_RESPONSE<5:3> = 111b			52		ms
$V_{OVF(FIX)}$	V_{OUT} fixed OVF protection threshold (See Supported PMBus Commands for Default)	VOUT_SCALE_LOOP = 1	OVF_FIXED = 0b		0.75		V
			OVF_FIXED = 1b		0.9		V
		VOUT_SCALE_LOOP = 0.5	OVF_FIXED = 0b	1.425	1.5	1.575	V
			OVF_FIXED = 1b	1.71	1.8	1.89	V
		VOUT_SCALE_LOOP = 0.25	OVF_FIXED = 0b	2.93	3.0	3.07	V
			OVF_FIXED = 1b		3.6		V
		VOUT_SCALE_LOOP = 0.125	OVF_FIXED = 0b		4.8		V
			OVF_FIXED = 1b		6.0		V
OUTPUT OVW/UVW							
V_{OVW}	Overvoltage warning (OVW) threshold, (42h) VOUT_OV_WARN_LIMIT (See Supported PMBus Commands for Default)	(VOSNS – GOSNS) rising	VOUT_OV_WARN_LIMIT = 553d	105%	108%	111%	VOC
			VOUT_OV_WARN_LIMIT = 573d		112%		VOC
			VOUT_OV_WARN_LIMIT = 594d		116%		VOC
			VOUT_OV_WARN_LIMIT = 655d		128%		VOC
$t_{OVW(DLY)}$	OVW delay time	(VOSNS – GOSNS) > V_{OVW}			2		µs
$V_{UVW(range)}$	Undervoltage warning (UVW) threshold, (43h) VOUT_UV_WARN_LIMIT programmable range	(VOSNS – GOSNS) falling		68%		96%	VOC
$V_{UVW(res)}$	Undervoltage warning (UVW) threshold resolution				4%		VOC
V_{UVW}	Undervoltage warning (UVW) threshold, (43h) VOUT_UV_WARN_LIMIT (See Supported PMBus Commands for Default)	(VOSNS – GOSNS) falling	VOUT_UV_WARN_LIMIT = 492d		96%		VOC
			VOUT_UV_WARN_LIMIT = 471d	89%	92%	95%	VOC
			VOUT_UV_WARN_LIMIT = 451d		88%		VOC
			VOUT_UV_WARN_LIMIT = 430d		84%		VOC
POWER GOOD							
$t_{PG(DLY\_RISE)}$	PG rising edge delay (soft-start done to high delay time, only occurs during startup - See Supported PMBus Commands for Default)	PGD_DEL = 00b			0		ms
		PGD_DEL = 01b			0.5		ms
		PGD_DEL = 10b			1.0		ms
		PGD_DEL = 11b			2.0		ms
$t_{PG(DLY\_UVF)}$	PG falling edge UVF delay				1		µs
$I_{PG(sink)}$	PG sink current	V_{PG} = 0.3V, V_{VCC} = 4.5V		10			mA
$I_{PG(LKG)}$	Pin leakage current when open drain output is high	V_{PG} = 5V				5	µA
$V_{OL(PG)}$	Pin output low-level voltage	I_{PG} = 10mA, V_{IN} = 12V, V_{VCC} = 4.5V				300	mV
	Minimum VCC for valid PG output	V_{EN} = 0V, R_{pullup} = 10kΩ V_{PG} ≤ 0.3V				1.2	V
RESET (VORST#)							
$V_{TH\_H(reset)}$	High-level voltage threshold (1.8V logic)	VORST# pin	SEL_VORST_TH = 1		1.1	1.35	V
$V_{TH\_L(reset)}$	Low-level voltage threshold (1.8V logic)	VORST# pin	SEL_VORST_TH = 1	0.8	0.9		V
$V_{HYS(reset)}$	Input voltage hysteresis (1.8V logic)	VORST# pin	SEL_VORST_TH = 1		125		mV
$V_{TH\_H(reset)}$	High-level voltage threshold (1.2V logic)	VORST# pin	SEL_VORST_TH = 0		0.6	0.65	V
$V_{TH\_L(reset)}$	Low-level voltage threshold (1.2V logic)	VORST# pin	SEL_VORST_TH = 0	0.45	0.5		V
$V_{HYS(reset)}$	Input voltage hysteresis (1.2V logic)	VORST# pin	SEL_VORST_TH = 0		150		mV
$V_{IH(reset)}$	Input logic low (1.8V logic)	VORST# pin	SEL_VORST_TH = 1			0.8	V

5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C. PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IL(reset)}$	Input logic high (1.8V logic)	VORST# pin	SEL_VORST_TH = 1	1.35			V
$V_{IH(reset)}$	Input logic low (1.2V logic)	VORST# pin	SEL_VORST_TH = 0			0.4	V
$V_{IL(reset)}$	Input logic high (1.2V logic)	VORST# pin	SEL_VORST_TH = 0	0.9			V
$t_{PW(reset)}$	Minimum VORST# pulse-width (1)					0.2	µs
THERMAL SHUTDOWN AND TEMPERATURE PROTECTION							
$T_{J(SD)}$	Thermal shutdown threshold (1)	Junction temperature rising		153	166		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis (1)				30		
$T_{OT(FAULT)}$	Over temperature fault threshold, (4Fh) OT_FAULT_LIMIT (See Supported PMBus Commands for Default)	Programmable range		115		165	
		Resolution			5		
$T_{OT(WARN)}$	Over temperature warning threshold, (51h) OT_WARN_LIMIT (See Supported PMBus Commands for Default)	Programmable range		95		130	
		Resolution			5		
TELEMETRY (PMBUS)							
$M_{IOUT(rng)}$	Output current measurement range			0		57.125	A
$M_{IOUT(acc)}$	Output current measurement accuracy datapoints	T_J = 0-125°C	I_{OUT} = 2.5A	1.25	2.5	3.75	A
			I_{OUT} = 15A(2)	13.5	15	16.5	A
			I_{OUT} = 30A(2)	27.6	30	32.4	A
			I_{OUT} = 50A(2)	46	50	54	A
	Output current measurement accuracy		0A ≤ I_{OUT} ≤ 10A	−1.25		1.25	A
			I_{OUT} = 15A(1)	−10%		10%	
			30A < I_{OUT} ≤ 50A(2)	−8%		8%	
$M_{VOUT(rng)}$	Output voltage measurement range			0		6	V
$M_{VOUT(acc)}$	Output voltage measurement accuracy datapoint	VOUT_SCALE_LOOP = 1	V_{OUT} = 0.5V	0.4925	0.5	0.5075	V
		VOUT_SCALE_LOOP = 0.5	V_{OUT} = 0.75V	0.735	0.75	0.765	V
		VOUT_SCALE_LOOP = 0.5	V_{OUT} = 1.1V	1.089	1.1	1.11	V
		VOUT_SCALE_LOOP = 0.25	V_{OUT} = 1.5V	1.47	1.5	1.53	V
		VOUT_SCALE_LOOP = 0.25	V_{OUT} = 1.8V	1.773	1.8	1.827	V
		VOUT_SCALE_LOOP = 0.125	V_{OUT} = 3.3V	3.234	3.3	3.366	V
$M_{PVIN(rng)}$	Input voltage measurement range			4		18	V
$M_{PVIN(acc)}$	Input voltage measurement accuracy datapoint	T_J = 25°C	VIN = 8V		8		V
			VIN = 12V	11.9	12	12.1	V
			VIN = 16V		16		V
$M_{TSNS(rng)}$	Internal temperature sense range			−40		150	°C
$M_{TSNS(acc)}$	Internal temperature sense accuracy	–40°C ≤ T_J ≤ 150°C		−4		4	°C
PMBUS INTERFACE							
$V_{IH(PMBUS)}$	High-level input voltage on PMB_CLK, PMB_DATA			1.35			V
$V_{IL(PMBUS)}$	Low-level input voltage on PMB_CLK, PMB_DATA					0.8	
$I_{IH(PMBUS)}$	Input high level current into PMB_CLK, PMB_DATA			–10		10	µA
$V_{OL(PMBUS)}$	Output low level voltage on PMB_DATA SMB_ALERT	VCC ≥ 4.5V, I_{pin} = 20mA				0.4	V
$I_{OH(PMBUS)}$	Output high level open drain leakage current into PMB_CLK, PMB_DATA, SMB_ALERT	V_{pin} = 5.5V				10	µA
$I_{OL(PMBUS)}$	Output low level open drain sinking current on PMB_DATA, SMB_ALERT	V_{pin} = 0.4V		20			mA
C_{PIN_PMB}	PMB_CLK and PMB_DATA pin input capacitance (1)	V_{pin} = 0.1V to 1.35V				5	pF
f_{PMBUS_CLK}	PMBus operating frequency range			10		1000	kHz
t_{BUF}	Bus free time between a STOP and START condition			0.5			µs

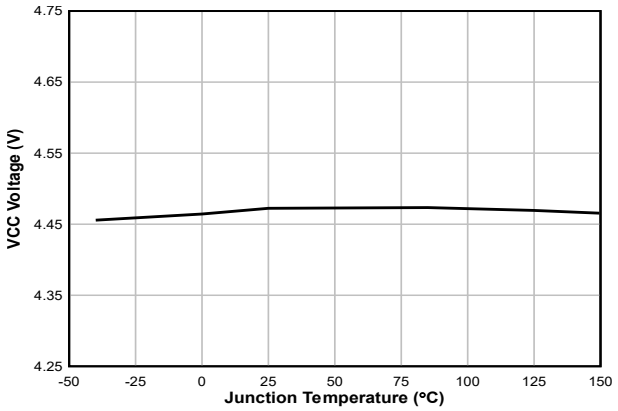
5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C. PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{HD_STA}	Hold time for a (repeated) START condition		0.26			µs
t_{SU_STA}	Setup time for a repeated START condition		0.26			µs
t_{SU_STO}	Setup time for a STOP condition		0.26			µs
t_{HD_PMB}	PMB_DATA hold time		0			µs
t_{SU_PMB}	PMB_DATA setup time		50			ns
$t_{TIMEOUT}$	Detect clock low timeout		25	30	35	ms
t_{LOW}	Low period of PMB_CLK		0.5			µs
t_{HIGH}	High period of PMB_CLK		0.26			µs
t_{R_PMB}	PMB_CLK and PMB_DATA rise time (1)	1000kHz class; $V_{IL(MAX)}$ –150mV to $V_{IH(MIN)}$ + 150mV			120	ns
t_{F_PMB}	PMB_CLK and PMB_DATA fall time (1)	1000kHz class; $V_{IH(MIN)}$ + 150mV to $V_{IL(MAX)}$ –150mV			120	ns
N_{WR_NVM}	Number of NVM writeable cycles (1)	–40°C ≤ T_J ≤ 125°C	1000			cycle

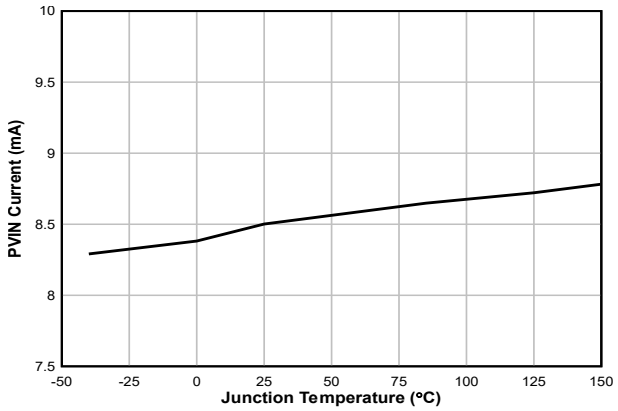
(1) Specified by design
(2) Specified by correlation

5.6 Typical Characteristics



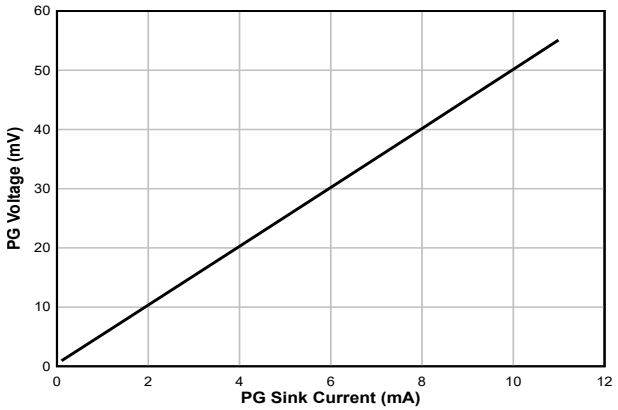
V_{PVIN} = 12V CNTL = 0V (Non Switching) VCC = Internal, 5mA load

Figure 5-1. VCC LDO vs Junction Temperature



V_{PVIN} = 12V CNTL = 0V (Non Switching) VCC = Internal

Figure 5-2. VIN Iq vs Junction Temperature



V_{PVIN} = 12V CNTL = 0V (Non Switching) VCC = Internal

Figure 5-3. I-V Curve for PGOOD

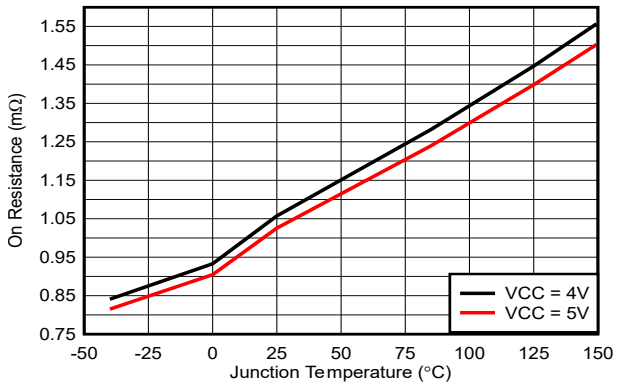


Figure 5-4. Low-Side MOSFET On-Resistance ($R_{DSO(on)}$) vs Junction Temperature

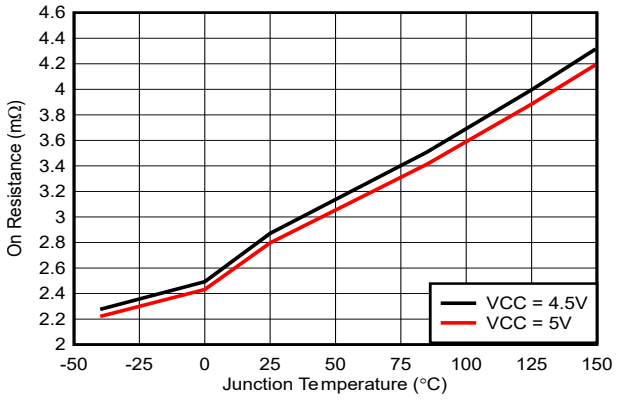
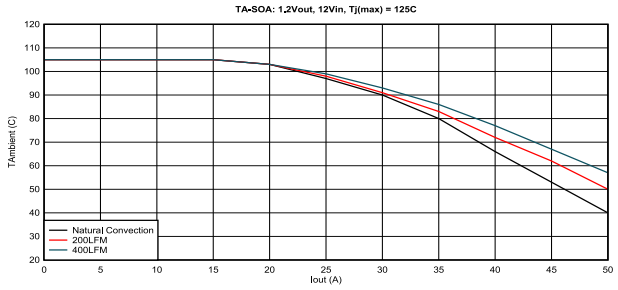


Figure 5-5. High-Side MOSFET On-Resistance ($R_{DSO(on)}$) vs Junction Temperature



PVIN = 12V FSW = 800kHz VCC = Internal
MODE = FCCM V_{OUT} = 1.2V Tj(max) = 125C

Figure 5-6. Safe Operating Area Ambient Temperature versus Loading Current

6 Detailed Description

6.1 Overview

The TPS546E25 is a highly-integrated, buck converter with D-CAP4 control topology for fast transient response and reduced output capacitance. All programmable parameters can be configured by the PMBus interface and many can be stored in NVM as the new default values to minimize the external component count. These features make the device well-designed for space-constrained applications.

Overcurrent, overvoltage, undervoltage, and overtemperature protections are provided internally in the device. TPS546E25 is a lead-free device and is RoHS compliant without exemption.

6.2 Functional Block Diagram

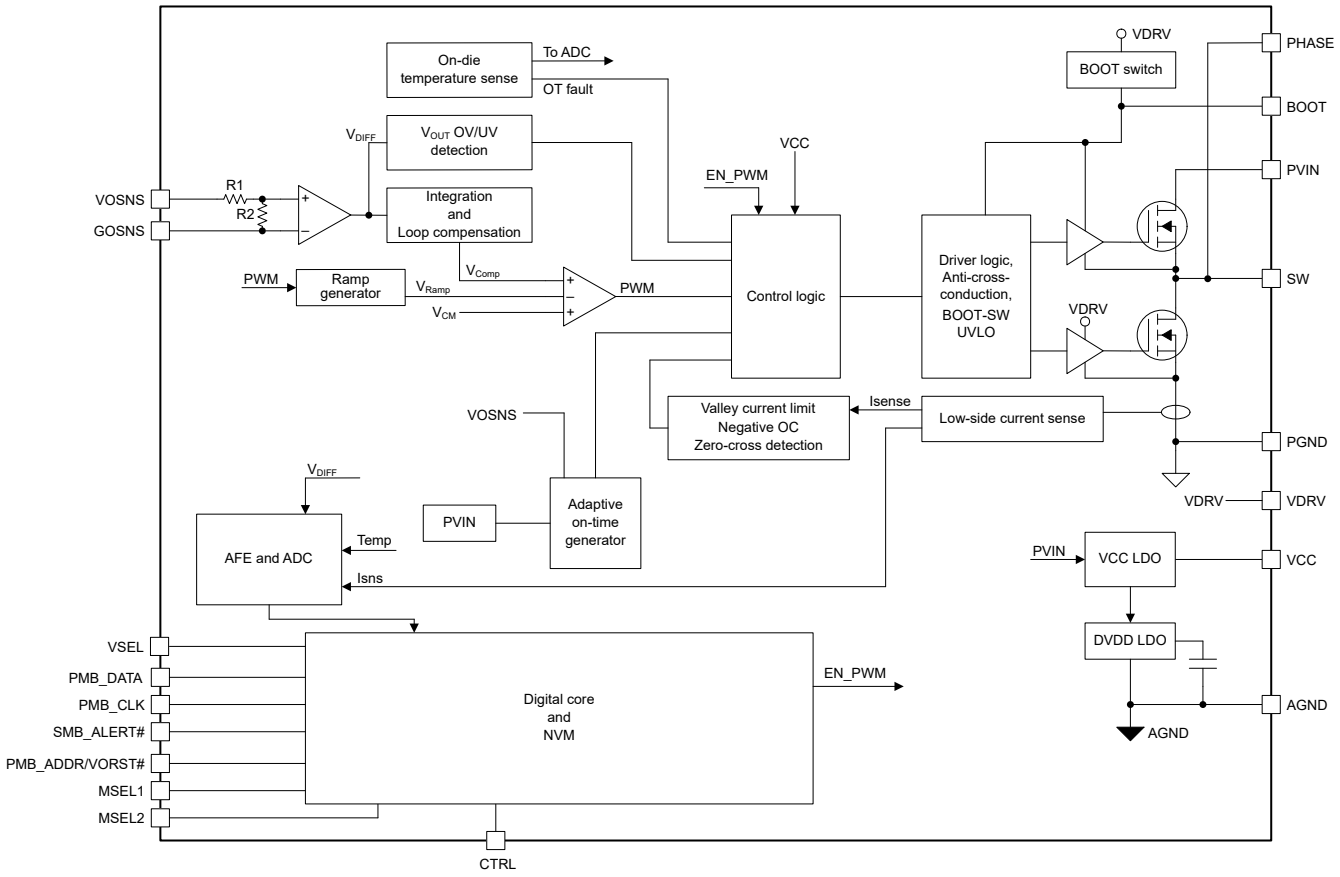


Figure 6-1. Block Diagram when Internal Feedback is Selected

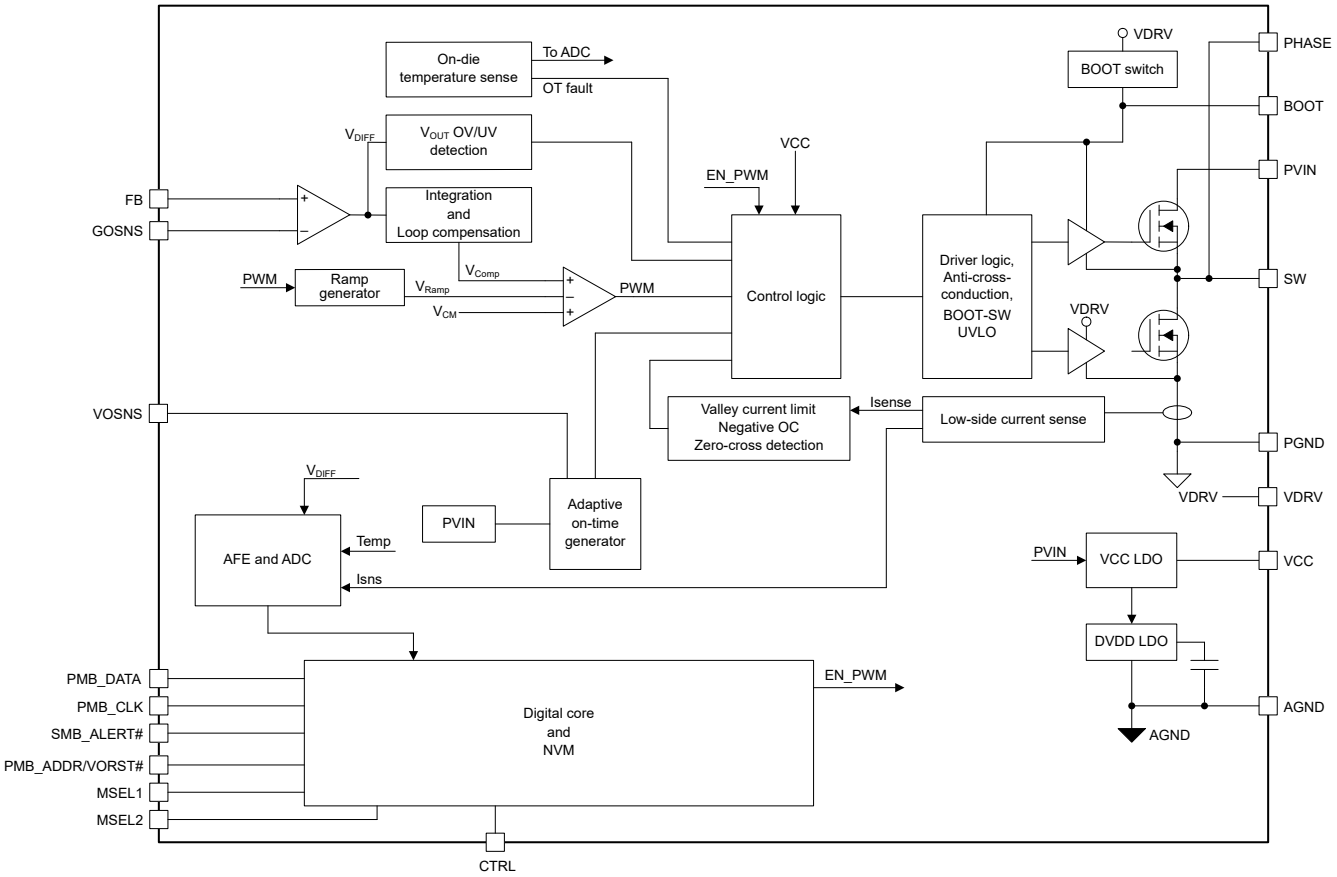


Figure 6-2. Block Diagram when External Feedback is Selected

6.3 Feature Description

6.3.1 D-CAP4 Control

The device uses D-CAP4 control to achieve a fast load transient response while maintaining ease-of-use. The D-CAP4 control architecture includes an internal ripple generation network enabling the use of very lowESR output capacitors such as multi-layered ceramic capacitors (MLCC) and low ESR polymer capacitors. No external current sensing, ripple injection or voltage compensation networks are required with D-CAP4 control architecture. The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine with the voltage feedback signal to regulate the loop operation, allowing the use of ultra-low ESR polymer and multi-layer ceramic capacitors (MLCCs).

D-CAP4 control architecture reduces loop gain variation across VOUT, enabling a fast load transient response across the entire output voltage range with one ramp setting. Unlike earlier D-CAP2 and D-CAP3 architectures, D-CAP4 uses a fixed ramp amplitude each switching cycle and a forward GAIN path to improve transient response and pulse frequency jitter while an error integrator provides high DC set-point accuracy.

The Ramp amplitude per switching cycle is

$$\frac{V_{ramp} \times N_{phase}}{GAIN} \times \left(1 - \frac{V_{out}}{V_{in}}\right) \quad (1)$$

Due to the limited number of pin-programmable Ramp and GAIN options, and the dependance of the control loop performance on the output inductor, TI recommends that designs using pin programming compensation consider the available loop options when selecting the inductor and the minimum and maximum capacitance that the compensation options support when selecting the capacitor.

When using PMBus programmed compensation through (D4h) COMP, the range and resolution of available Ramp voltages and GAIN options is generally broad enough that designs can follow a more traditional design flow where the inductor is selected based on switching frequency and ripple current, and then capacitors are selected to meet ripple and transient requirements, then finally Ramp and GAIN is selected to make sure of stability with the inductor and capacitor, however many designers can find following the compensation first design flow to narrow the choice of inductors easier, and then selecting a more optimized ramp / GAIN option after the inductor has been selected.

Evaluate the maximum inductor value, which can be used with each compensation option while still meeting the application transient requirements. To do this action, calculate the maximum dynamic output impedance needed to meet the transient requirements for the application.

$$Z_{out(dynamic)} < \frac{V_{OUT(transient)}}{I_{OUT(transient)}} \quad (2)$$

For each of the six pin programmable V_{ramp} / GAIN options, calculate the maximum inductance that can be used with that ramp to achieve the required output impedance

$$L_{(max)} = Z_{out(dynamic)} \times \frac{V_{sense} \times GAIN}{Fsw \times V_{ramp}} \quad (3)$$

With the maximum inductor value, estimate the peak to peak inductor ripple current for each available V_{ramp} / GAIN compensation option and select an inductor whose peak to peak ripple current is between 10% and 40% of the expected full load current.

$$I_{L(pk-pk)} = (V_{IN} - V_{OUT}) \times \left(\frac{V_{OUT}}{V_{IN} \times L \times Fsw}\right) \quad (4)$$

Selecting an inductor close to the maximum inductor meeting the dynamic impedance requirements minimizes over design and reduces the minimum amount of capacitance required to maintain stability while picking a smaller inductor reduces the amount of capacitance required to meet large-signal overshoot requirements, especially at low input voltages.

After an inductor has been selected, calculate the closed loop, mid-band dynamic output impedance by arranging the maximum inductance equation

$$Z_{out(dynamic)} = \frac{L_{(max)} \times V_{ramp} \times Fsw}{V_{sense} \times GAIN} \quad (5)$$

Note

When using the internal feedback divider, V_{sense} is the output voltage at the VOSNS pin. When using an external feedback divider, V_{sense} is the reference voltage at the VSEL/FB pin.

To estimate the linear transient performance

$$V_{OUT(Transient)} = Z_{OUT(Dynamic)} \times I_{OUT(Transient)} \quad (6)$$

The minimum capacitance for stability is

$$C_{OUT(min)} = \frac{2}{\pi \times Z_{OUT(Dynamic)} \times Fsw} \quad (7)$$

The minimum capacitance to meet large signal overshoot is

$$C_{OUT(min)} = \frac{I_{OUT(Transient)}^{2} \times L}{V_{OUT} \times V_{OUT(Transient)}} \quad (8)$$

The maximum recommended capacitance places the L-C resonant frequency no less than ½ the integrator zero frequency, which can be estimated by

$$F_{Res} > 1/2 \times \frac{1}{2 \times \pi \times INT\_TIME \times GAIN} \quad (9)$$

6.3.1.1 Loop Compensation

The TPS546E25 provides several options for tuning the output voltage feedback and response to transients. The PMBus command Section 7.67 includes all the GAIN and RAMP settings, a subset of the GAIN and RAMP settings are also selectable through Pin-Strapping through Programming MSEL2.

- RAMP: sets the internal inner-loop full cycle RAMP amplitude. Smaller ramp settings result in faster response to load transient events, but also lead to increased off-time jitter. Likewise, large ramp settings result in reduced frequency jitter, but become slower to respond to an output voltage deviation. The ramp setting, along with GAIN, inductor and output capacitance also affects the small-signal bandwidth of the converter. There are two settings available through Programming MSEL2, and four options through PMBus command COMP.
- GAIN sets the proportional gain from the sensed output voltage – VOSNS when using the internal feedback divider, or VSEL/FB when using an external feedback divider. GAIN, along with RAMP, and inductor, sets the forward transconductance from the sensed output voltage to the inductor current as the inverse of Equation 5. There are three settings available through Programming MSEL2 and twelve though PMBus command COMP.
- INT_TIME is the integration time constant. The integration time constant affects the settling and response time following an input or output transient. The default is for the INT_TIME is set automatically based on the switching frequency and can be overridden through the COMP register.

6.3.2 Internal VCC LDO and Using an External Bias on the VCC Pin and VDRV Pin

TPS546E25 has an internal 4.5V LDO featuring input from PVIN and output to the VCC pin. When the PVIN voltage rises, the internal LDO is enabled automatically and starts regulating LDO output voltage on the VCC pin. The VCC voltage provides the bias voltage for the internal analog circuitry in controller side and the VDRV voltage provides the supply voltage for the power stage side.

Both the VCC pin and the VDRV pin must be bypassed with a 2.2µF, at least 6.3V rating ceramic capacitor. The VCC pin decoupling capacitor is required to refer to AGND to provide a clean ground for the analog circuitry in controller. The VDRV pin decoupling capacitor is required to refer to PGND to minimize the parasitic loop inductance for the driver circuitry in the power stage. TI highly recommends placing a 1Ω resistor between the VCC pin and VDRV pin to form an RC filter, thus the noise impact from power stage is reduced.

An external bias ranging 4.75V to 5.30V can be connected to the VDRV pin and VCC pin and power the IC. This connection enhances the efficiency of the converter because the VDRV and VCC power supply current now runs off this external bias instead of the internal linear regulator.

A VDRV UVLO circuit monitors the VDRV pin voltage and disables the switching when VDRV falls below the VDRV UVLO falling threshold. Maintaining a stable and clean VCC voltage is required for a smooth operation of the device.

Considerations when using an external bias on the VDRV and VCC pin are shown below:

- Connect the external bias to VDRV pin directly. Place a 1Ω resistor between the VCC pin and VDRV pin, then VCC is powered through the 1Ω filtering resistor.
- A good power-up sequence is the external 5V bias is applied to VDRV pin first (VCC pin is also powered by the external bias through the 1Ω filtering resistor), then the 12V bus applied on PVIN pin, and then CTRL signal goes high.

6.3.3 Input Undervoltage Lockout (UVLO)

The TPS546E25 provides four independent UVLO functions for the broadest range of flexibility in start-up control. While only the fixed VCC UVLO is required to enable PMBus connectivity as well as PIN/IOUT/VOUT/TEMPERATURE monitoring, all four UVLO functions must be met before switching can be enabled.

6.3.3.1 Fixed VCC_OK UVLO

The TPS546E25 has an internally fixed UVLO of 3.15V (typical) on VCC to enable the digital core and initiate power-on reset, including pin-strap detection. The off-threshold on VCC is 3.1V (typical). After VCC level rises above 3.15V (typical) and stays above 3.1V (typical), the PMBus communication is enabled.

6.3.3.2 Fixed VDRV UVLO

The TPS546E25 device has an internally fixed UVLO of 3.6V (typical) on VDRV to enable drivers for power FETs and output voltage conversion. The off-threshold on VDRV is 3.4V (typical).

6.3.3.3 Programmable PVIN UVLO

Two PMBus commands (VIN_ON and VIN_OFF) allow the user to set PVIN voltage turn-on and turn-off thresholds independently.

The register uses multiple UVLO circuitries (VCC, VDRV, and PVIN UVLO) to enable or disable the power conversion. If VIN_OFF is programmed higher than VIN_ON, the TPS546E25 rapidly switches between enabled and disabled while PVIN remains below VIN_OFF. Please set VIN_ON threshold always greater than VIN_OFF threshold.

6.3.3.4 Control (CNTL) Enable

The TPS546E25 offers precise enable, disable threshold on the CNTL pin. The power stage switching is held off until the CNTL pin voltage rises above the logic high threshold (typically 1.2V). The power stage switching is turned off after CNTL pin voltage drops below the logic low threshold (typically 1V).

CNTL pin has an internal filter to avoid unexpected ON or OFF due to short glitches. The deglitch time is set to 0.2µs.

The recommended operating condition for CNTL pin is up to 5.3V and the absolute maximum rating is 5.5V. *Do not* connect the CNTL pin to PVIN pin directly.

The TPS546E25 remains in disabled state when the CNTL pin floats. The CNTL pin is internally pulled down to AGND through a 125kΩ resistor.

6.3.4 Differential Remote Sense and Internal, External Feedback Divider

The TPS546E25 offers true differential remote sense function which is implemented between the VOSNS pin and GOSNS pin. The output of the differential remote sense amplifier is internally fed into the control loop and doe not come out to a package pin.

Differential remote sense function compensates a potential voltage drop on the PCB traces thus helps maintain VOUT accuracy under steady state operation and load transient event. Connecting the VOSNS pin and GOSNS pin to the remote location allows sensing the output voltage at a remote location. The connections from VOSNS pin and GOSNS pin to the remote location must be a pair of PCB traces with at least 12 mil trace width, and must implement Kelvin sensing across a high bypass capacitor of 0.1µF or higher. The ground connection of the remote sensing signal must be connected to GOSNS pin. The VOUT connection of the remote sensing signal must be connected to VOSNS pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW node, or high frequency clock lines. TI recommends to shield the pair of remote sensing lines with ground planes above and below.

The recommended GOSNS operating range (refer to AGND pin) is −300mV to +300mV. In case of local sense (no remote sensing), short GOSNS pin to AGND.

The TPS546E25 offers two methods for determining the converter output voltage: a fully integrated, internal, precision feedback divider or an external feedback divider. The method used is determined by the selection made on the MSEL1 pin (see Pin-Strapping for details). Using the external feedback divider, the output voltage is programmed with an external resistor divider from the output (VOSNS connection) to ground return (GOSNS) with the center point connected to the FB/VSEL pin. TI recommends to use 1% tolerance or better divider resistors. Starting with a fixed value for the bottom resistor, typically 10kΩ, use the equation to calculate the top resistor in the divider.

Where VREF is the internal reference DAC voltage programmed in VBOOT_NVM by default, which is 0.4V.

If MSEL1 is set to use the internal feedback divider, a resistor from VSEL/FB to AGND selects the output voltage setting (see *Set Output Voltage* for more details).

6.3.5 Set the Output Voltage and VORST#

The TPS546E25 offers both internal feedback divider (discrete) and external feedback divider (continuous) output voltage setting options.

With the continuous output voltage setting method, the reference DAC default is set to 0.4V (VBOOT_1 in VBOOT_OFFSET_1) and the external resistor divider is the equivalent to VOUT_SCALE_LOOP = 1. The divider gain is now determined by the external voltage setting resistors as described in Loop Compensation.

With the discrete output voltage setting method, the output voltage is determined by two settings: VOUT_COMMAND and VOUT_SCALE_LOOP. Together, these two parameters determine the converter output voltage. VOUT_COMMAND is used to adjust the reference DAC input to the Error Amplifier and can be in the range of 0.25V to 0.75V. VOUT_SCALE_LOOP selects a voltage divider gain of 1, 0.5, 0.25, or 0.125.

When PMBus or Pin-Strapping is used to set the regulated voltage, the commanded output voltage in volts is determined by a combination of VOUT_COMMAND, VOUT_TRIM, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, and OPERATION commands, as below. As stated in the description of the VOUT_MODE command, the VOUT step size is 1.953mV. The programmed VOUT is computed as:

VOUT = (VOUT_COMMAND + VOUT_TRIM + (VOUT_MARGIN_HIGH – 1) * VOUT_COMMAND × OPERATIONS[5] – (1–m VOUT_MARGIN_LOW) * VOUT_COMMAND × OPERATIONS[4])

The output voltage is related to:

- VOUT_MAX
- VOUT_MIN
- VOUT_OV_FAULT_LIMIT
- VOUT_OV_WARN_LIMIT
- VOUT_UV_FAULT_LIMIT
- VOUT_UV_WARN_LIMIT

The TPS546E25 defaults to the relative format for the following per bit 7 in VOUT_MODE:

- VOUT_MARGIN_HIGH
- VOUT_MARGIN_LOW
- VOUT_OV_FAULT_LIMIT
- VOUT_OV_WARN_LIMIT
- VOUT_UV_FAULT_LIMIT
- VOUT_UV_WARN_LIMIT

Refer to the detailed description of VOUT_MODE for details.

The range of recommended VOUT_COMMAND values is dependent upon the configured VOUT_SCALE_LOOP. The design does not limit the VOUT_COMMAND value to be within this recommended range. The VOUT_COMMAND value is limited only by VOUT_MAX and VOUT_MIN. The VOUT LSB is 1.953mV, the minimum VOUT is 0.25V, and the maximum VOUT is 5.5V.

Table 6-1. VOUT_COMMAND Recommended Range

VOUT_SCALE_LOOP (V/V)	VOUT RANGE (V)	VOUT_COMMAND RECOMMENDED RANGE (dec)
1	0.244 – 0.75	125 – 384
0.5	0.244 – 1.5	125 – 768
0.25	0.488 – 3	250 – 1536
0.125	0.976 – 5.504	500 – 2818

The TPS546E25 offers a VOUT reset (VORST#) function on the PMB_ADDR/VORST# pin. If PMB_ADDR/VORST# is low and EN_VORST in SYS_CFG_USER1[2] = 1, then VOUT_COMMAND is set to VBOOT at the setting in VOUT_TRANSITION_RATE.

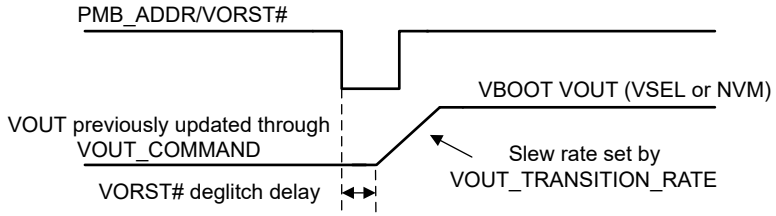


Figure 6-3. VOUT Reset by VORST#

6.3.6 Start-Up and Shutdown

The start-up and shutdown of the device is controlled by several PMBus programmable values including:

- (01h) OPERATION
- (02h) ON_OFF_CONFIG
- (60h) TON_DELAY
- (61h) TON_RISE
- (64h) TOFF_DELAY
- (65h) TOFF_FALL

The t_{ON_RISE} time is selectable by pin-strapping through MSEL1, PMBus programming, or both.

With the default ON_OFF_CONFIG settings, the timing is as shown. See the *Supported PMBus® commands* for full details on the implementation and use.

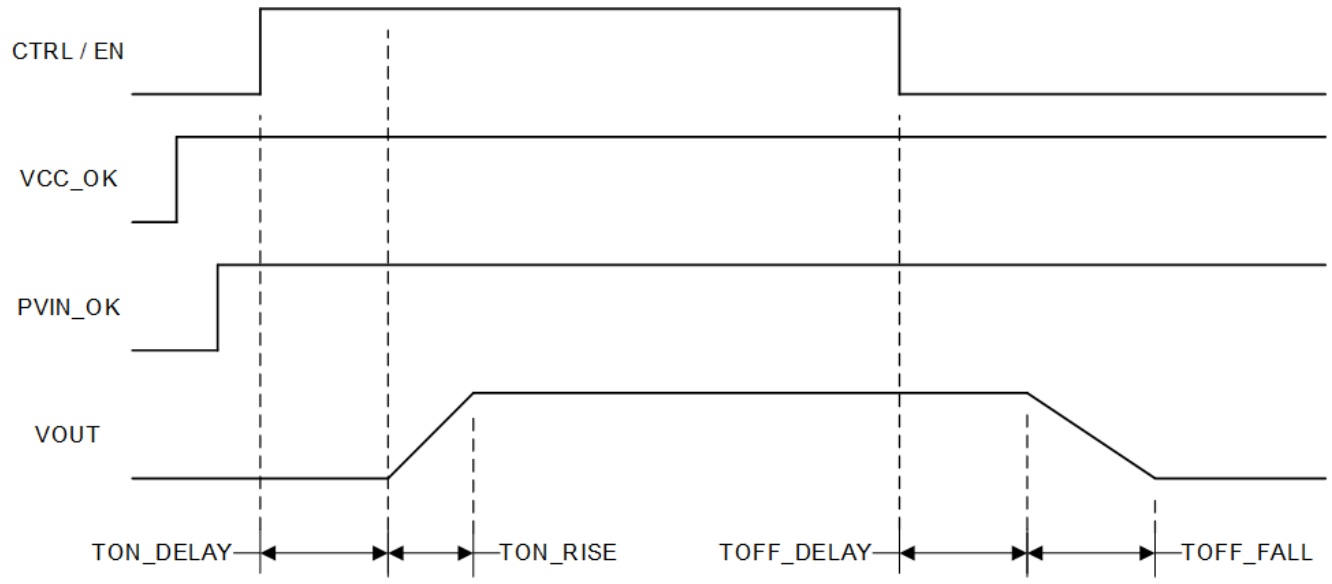


Figure 6-4. TPS546E25 Start-Up and Shutdown

Start-Up

The start-up sequence includes three sequential periods. During the first period, the device does initialization, which includes building up internal LDOs and references, register value initialization, pin-strap detection, enabling digital interface, and so forth. The initialization, which is not gated by the CTRL pin voltage, starts as long as VCC pin voltage is above the VCC_OK UVLO rising threshold (3.15V typical). The length of this period is about 200µs for TPS546E25. The PMBus communication including both read and write operations is allowed after finishing the initialization.

After the CTRL pin voltage crosses above CTRL high threshold (typically 1.2V) the device moves to the second period, power-on delay. The power-on delay is programmable in TPS546E25 through register TON_DELAY with minimum 0.05ms delay and maximum 2ms delay.

The V_{OUT} soft start is the third period. A soft-start ramp, which is an internal signal, starts when the chosen power-on delay finishes. The soft-start time can be selected in register TON_RISE with options of 1ms, 2ms, 4ms, 8ms, and 16ms. When starting up without prebias on the output, the VOUT ramps up from 0V to either the selected Vboot value or the programmable VOUT_COMMAND value to avoid the inrush current by the output capacitor charging, and also minimize VOUT overshoot.

For the start-up with a prebiased output, the device limits current from being discharged from the prebiased output voltage by preventing the low-side FET from forcing the SW node low until after the first PWM pulse turns on the high-side FET. After the increasing reference voltage exceeds the feedback voltage, which is internally divided down from (VOSNS−GOSNS) level, the high-side SW pulses start. This action enables a smooth start-up with a prebiased output.

Shutdown

The TPS546E25 also offers a programmable soft-stop feature through the PMBus register TOFF_FALL with 0.5ms, 1ms, 2ms, and 4ms options. The soft-stop feature forces a controlled decrease of the output voltage from regulation to 200mV. After Vout is discharged to 200mV level, the power stage stops switching and goes to tri-state. There can be negative inductor current forced during the TOFF_FALL time to discharge the output voltage.

After a stop condition is received and the selected TOFF_DELAY delay expires, the TPS546E25 device enters the soft-stop operation during which the control loop actively controls the discharge slew rate of the output voltage. The power stage continues switching while the internal reference ramps down linearly. The discharge

slew rate during this phase is determined by the selected boot up voltage (not the current output voltage) and the selected TOFF_FALL time. After Vout is discharged to 200mV level the power stage stops switching and goes to tri-state. The Vout discharge continues but the discharge slew rate is controlled by the load current. With this discharge operation, the TPS546E25 device controls the soft-stop slew rate rather the total soft-stop time, thus the total VOUT discharge time (also known as, soft-stop time) can vary from the register TOFF_FALL value. The TOFF_FALL time is used to set the internal reference DAC ramp-down time from the regulation level to 0mV. For example, under heavy load condition, the total soft-stop time from VOUT regulation level to zero volt is likely shorter than the programmed TOFF_FALL value. Under light load, the total soft-stop time likely becomes longer than the programmed TOFF_FALL value.

6.3.7 Dynamic Voltage Slew Rate

The TPS546E25 offers VOUT_TRANSITION_RATE register to set slew rate when changing the output voltage levels.

During the output voltage transition, due to the quick charge or discharge to output capacitors, the power stage sees extra inrush current. This inrush current plus load current can trigger overcurrent protection when there is no sufficient room from OCL or NOC setting. For example, the positive inductor current during VOUT step-up transition goes higher than nominal operation. If the LS valley OCL threshold is set relatively low and does not allow the extra inrush current, the inductor current is potentially limited by the cycle-by-cycle overcurrent limit feature, thus the actual step-up slew rate is lower than the desired value. Similar situations can happen to VOUT step-down transitions with no load condition. The negative inductor current during VOUT step-down transition goes more negative than nominal operation. However, the inductor current is not allowed to go more negative than the negative OC threshold. Thus, triggering NOC operation during VOUT step-down transition results that the actual step-down slew rate is lower than the desired value.

6.3.8 Set Switching Frequency

The TPS546E25 allows users to select the switching frequency through pin-strapping on MSEL2 or FREQUENCY_SWITCH register and operation mode through FCCM bit in SYS_CFG_USER1.

When setting the switching frequency above 1.4MHz, a separate VCC bias must be used.

6.3.9 Switching Node (SW)

The SW pins connect to the switching node of the power conversion stage. The SW pins act as the return path for the high-side gate driver. During nominal operation, the voltage swing on SW normally traverses from below ground to above the input voltage. Parasitic inductance in the PVIN to PGND loop (including the component from the PCB layout and also the component inside the package) and the output capacitance (COSS) of both power FETs form a resonant circuit that can produce high frequency (> 100MHz) ringing on this node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. TPS546E25 high-side gate driver is fine tuned to minimize the peak ringing amplitude so that an RC snubber on SW node is usually not needed. However, TI highly recommends for the user to measure the voltage stress across either the high-side or low-side FET and make sure that the peak ringing amplitude does not exceed the absolute maximum rating limit listed in the *Absolute Maximum Ratings* table.

6.3.10 Overcurrent Limit and Low-side Current Sense

For a synchronous buck converter, the inductor current increases at a linear rate determined by the input voltage, the output voltage, and the output inductor value during the high-side MOSFET on-time (ON time). During the low-side MOSFET on-time (OFF time), this inductor current decreases linearly per slew rate determined by the output voltage and the output inductor value. The inductor during the OFF time, even with a negative slew rate, usually flows from the device SW node to the load the device which is said to be sourcing current and the output current is declared to be positive. This section describes the overcurrent limit feature based on the positive low-side current. The next section describes the overcurrent limit feature based on the negative low-side current.

The positive overcurrent limit (OCL) feature in the TPS546E25 device is implemented to clamp low-side *valley current* on a cycle-by-cycle basis. The inductor current is monitored during the OFF time by sensing the

current flowing through the low-side MOSFET. When the sensed low-side MOSFET current remains above the selected OCL threshold, the low-side MOSFET stays ON until the sensed current level becomes lower than the selected OCL threshold. This operation extends the OFF time and pushes the next ON time (where the high-side MOSFET turns on) out. As a result, the OCL bit in STATUS_IOUT is set, also the average output current sourced by the device is reduced. As long as the load pulls a heavy load where the sensed low-side *valley current* exceeds the selected OCL threshold, the device continuously operates in this clamping mode which extends the current OFF time and pushes the next ON time out. The device does not implement a fault response circuit directly tied to the overcurrent limit circuit, instead, the VOUT Tracking UVF function is used to shuts the device down under an overcurrent fault. During an overcurrent event, the current sunk by the load (I_{OUT}) exceeds the current sourced by the device to the output capacitors, thus, the output voltage tends to decrease. Eventually, when the output voltage falls below the selected undervoltage fault threshold, the VOUT Tracking UVF comparator detects and shuts down the device after the UVF Response Delay (programmable in VOUT_UV_FAULT_RESPONSE register). The device then responds to the Tracking UVF trigger per bit[3] *RESTART* selection in VOUT_UV_FAULT_RESPONSE register. With the *RESTART* bit unset (value "0"), the device latches OFF both high-side and low-side drivers. The latch is cleared with a reset of VCC or by toggling the EN pin. With the *RESTART* bit set (value "1"), the device enters hiccup mode and re-starts automatically after a hiccup sleep time of 56ms, without limitation on the number of restart attempts. In other words, the response to an overcurrent fault is set by the programmed UVF response.

If an OCL condition happens during a soft-start ramp the device still operates with the cycle-by-cycle current limit based on the sensed low-side valley current. This operation can limit the energy charged into the output capacitors thus the output voltage likely ramps up slower than the desired soft-start slew rate. During the soft start, the VOUT Tracking UVF comparator is disabled thus the device does not respond to a UVF event. Upon the completion of the soft start, the VOUT Tracking UVF comparator is enabled, then the device starts responding to the UVF event.

The OCL feature in the device is implemented by detecting the low-side valley current through analog circuitries and has no relationship with the integrated Analog-to-Digital converter (ADC). The telemetry analog-front-end gets an input from the low-side current sense circuit and average low-side MOSFET current from the start to the end of each low-side MOSFET on time. By this method, the telemetry sub-system reports the load current (IOUT) which is the average value of the inductor current but not peak or valley values.

6.3.11 Negative Overcurrent Limit

The TPS546E25 device is a synchronous buck converter, thus the current can flow from the device to the load or from the load into the device through SW node. When current is flowing from the device SW node to the load the device is said to be sourcing current and the output current declared to be positive. When current is flowing into the device SW node from the load, the device is said to be sinking current and the current is declared to be negative.

The device offers a programmable, cycle-by-cycle negative overcurrent (NOC) limit through the SEL_UCF bit in the SYS_CFG_USER1 register. Similar with the positive overcurrent limit, the inductor current is monitored during the low-side MOSFET ON period. To prevent too large negative current and a damage of low-side MOSFET, the device turns off the low-side MOSFET after the detected on the low-side MOSFET exceeds the selected NOC limit.

The NOC operation usually happens after an overvoltage event but can also happen during VOUT step-down transition with fast slew rate.

6.3.12 Zero-Crossing Detection

TPS546E25 device uses a zero-crossing (ZC) circuit to perform the zero inductor current detection during skip-mode operation. The ZC threshold is set to a small negative value before the low-side MOSFET is turned off, entering discontinuous conduction mode (DCM) operation. After entering DCM, the ZC threshold hysteresis increases the threshold to a small positive value after entering DCM. As a result, the device delivers better light-load efficiency.

When the load current increases enough such that the device exits DCM, the ZC circuit must detect 16 consecutive cycles of negative inductor current below the ZC threshold before returning to DCM. Only one cycle without ZC detection is required to exit DCM.

During Soft-start (61h) TON_RISE the ZC circuit is always disabled and the

TPS546E25 starts up in FCCM operation. If 16 consecutive cycles of negative inductor current are detected after (61h) TON_RISE completes, the TPS546E25 can enter DCM operation if FCCM mode is not selected by pin-programming or (D1h) SYS_CFG_USER1 programming

6.3.13 Input Overvoltage Protection

The TPS546E25 device actively monitors the PVIN input voltage. When the PVIN voltage level is above the overvoltage threshold, TPS546E25 stops switching and pulls PG signal low. Two options are provided for PVIN OV rising threshold in VIN_OV_FAULT_LIMIT register while the PVIN OV falling threshold is always 13.5V.

After the PVIN overvoltage fault is triggered, the device latches off until EN pin is toggled or PVIN is reset.

6.3.14 Output Overvoltage and Undervoltage Protection

The TPS546E25 device monitors the output voltage (VOSNS − GOSNS) to provide overvoltage (OV) and undervoltage (UV) protection. The Tracking OVF and Tracking UVF thresholds both track to the VOUT setting but can be selected independently.

VOUT Tracking UVF

When the output voltage (VOSNS − GOSNS) drops below the VOUT setting by the value configured in VOUT_UV_FAULT_LIMIT register, the tracking UVF comparator detects and an internal UVF Response Delay counter selected in VOUT_UV_FAULT_RESPONSE register begins. At the same time, the UVF bit in STATUS_VOUT register is set.

The tracking UVF function is enabled only after the soft-start period completes.

During the UVF Response Delay, if the output voltage (VOSNS − GOSNS) rises above the UVF threshold, thus not qualified for a UVF event, the UVF response delay timer resets to zero. When the VOUT drops below the UVF threshold again, the UVF response delay timer re-starts from zero.

The TPS546E25 device also offers tracking UV Warning (UVW) function. The VOUT_UV_WARN_LIMIT shows the available tracking UVW thresholds. When the output voltage (VOSNS − GOSNS) drops lower than the VOUT setting by the value configured in VOUT_UV_WARN_LIMIT register, the tracking UVW comparator detects and the UVW bit in STATUS_VOUT register is set. There is no purpose delay for UVW event.

VOUT Tracking OVF

When the output voltage (VOSNS − GOSNS) rises higher than the VOUT setting by the value configured in VOUT_OV_FAULT_LIMIT register, the tracking OVF comparator detects and the device responds to the OV fault immediately per the selection inVOUT_OV_FAULT_RESPONSE register. At the same time, the OVF bit in STATUS_VOUT register is set.

The tracking OVF function is enabled only after the soft-start period completes.

The TPS546E25 device also offers tracking OV Warning (OVW) function. When the output voltage (VOSNS − GOSNS) rises higher than the VOUT setting by the value configured in VOUT_OV_WARN_LIMIT register, the tracking OVW comparator detects and the OVW bit in STATUS_VOUT register is set. There is no purpose delay for the OVW event.

6.3.15 Overtemperature Protection

To have full coverage for a potential overtemperature event, the TPS546E25 device implements three overtemperature protection circuitries: two on the controller die and one on the Power Stage (PS) die.

Programmable OTP by Monitoring the Controller Die Temperature

The on-die temperature sense circuit senses the controller die temperature. The sensed signal is fed into an internal ADC and converted to the Controller die temperature which is reported as (8Dh) READ_TEMP1 through the Telemetry sub-system. This feature utilizes a digital comparator that compares the output of the IC TEMPERATURE telemetry to the fault threshold selected in OT_FAULT_LIMIT register. The device stops the SW switching when the sensed IC temperature goes beyond the selected threshold. The device response to a Programmable OTP event is described in OT_FAULT_RESPONSE.

Analog OTP by Monitoring the Controller Die Temperature

The sensed temperature signal is fed into an analog OTP circuit on the controller die as well. An analog comparator is used to compare the output of the controller die temperature sensing circuit to a fixed threshold (rising 166°C typical). The device stops the SW switching when the sensed IC temperature goes beyond the fixed threshold. The device response to an Analog OTP event is always the same as the Programmable OTP.

Given the fixed threshold (166°C typical) for the analog OTP is higher than the highest setting (150°C typical) in programmable OTP, the analog OTP is unlikely to trigger during the nominal operation.

Analog OTP by Monitoring the Power Stage Die Temperature

A temperature sensing circuit is implemented in the Power Stage (PS) die. This sensed is fed into an analog OTP circuit on the PS die. An analog comparator is used to compare the output of the PS die temperature sensing circuit to a fixed threshold (rising 166°C typical). The device stops the SW switching when the sensed IC temperature goes beyond the fixed threshold. After the PS die temperature falls 30°C below the rising threshold, the device automatically restarts with an initiated soft start. This analog OTP is a non-latch protection.

6.3.16 Telemetry

The telemetry sub-system in the controller core supports the following measurements:

- Input voltage (direct measurement)
- Output voltage (direct measurement)
- Output current (direct measurement)
- Controller die temperature (direct measurement)

The ADC output is a single conversion of each measurement without rolling window averaging for fast refresh rate of these key system parameter. All above parameters are measured sequentially while the output current is measured more often than the others. This sequence design allows each IOUT telemetry value to be updated within 95µs, while each of the rest of telemetry value to be updated within 190µs.

VOUT Telemetry

The output voltage sense telemetry senses the differential voltage across VOSNS to GOSNS pin. The minimum READ_VOUT value is clamped at 0V. When the internal voltage divider is selected, the READ_VOUT value is scaled based on the VOUT_SCALE_LOOP value selected when setting the output voltage.

When the external voltage divider is selected, the VOUT at the ADC input is internally scaled by the VOUT_SCALE_MONITOR value selected, and the VOUT_SCALE_LOOP is always set to 1. The user can maximize the dynamic range of the sensed signal based the expected VOUT setting as described in the table in VOUT_SCALE_MONITOR. If the VOUT_SCALE_MONITOR value is chosen such that the maximum allowed VO

IOUT Telemetry

The output current sense telemetry senses the average of low-side FET current from the start to the end of each low-side FET on time which provides the average inductor current. To achieve high accuracy and wide report range, the device automatically sets the current sense gain. The value for READ_IOUT is

$$READ\_IOUT = I_{SWavg} \times IMON\_GAIN\_CAL + IOUT\_CAL\_OFFSET \quad (10)$$

Where

- I_{SWavg} is the average current flowing out of the SW pin during the low-side FET on-time

IC Temperature Telemetry

The die temperature sense telemetry senses the controller die temperature. The power stage (PS) die implements overtemperature protection and the PS die temperature is not reported through telemetry sub-system. READ_TEMP1 is the PMBus READ_TEMP1 register value in decimal.

6.4 Device Functional Modes

6.4.1 Forced Continuous-Conduction Mode

When the operation mode is set to FCCM, the controller operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency maintained to an almost constant level over the entire load range which is designed for applications requiring tight control of the switching frequency at the cost of lower efficiency.

When FCCM is selected, the TPS546E25 device operates at CCM during the whole soft-start period as well as the nominal operation.

6.4.2 DCM Light Load Operation

When the operation mode is set to DCM, the device automatically reduces the switching frequency at light-load conditions to maintain high efficiency. This section describes the operation in detail.

As the output current decreases from heavy load condition, the inductor current also decreases until the rippled valley of the inductor current touches zero level. Zero level is the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM). The on-time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. The transition point to the light-load operation $I_{OUT(LL)}$ (for example: the threshold between continuous- and discontinuous-conduction mode) is calculated as shown in below equation.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times Fsw} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (11)$$

Where

- Fsw is the nominal continuous conduction switching frequency

The reduced switching frequency at load currents less than $I_{OUT(LL)}$ when in DCM are given by:

$$Fsw_{LL} = Fsw \times \frac{I_{OUT}}{I_{OUT(LL)}} \quad (12)$$

The output voltage peak to peak ripple increases in load operation, reaching up to 4 × the continuous conduction ripple voltage at no load.

TI recommends using low ESR capacitors (such as ceramic capacitor) for skip-mode.

6.4.3 Powering the Device From a 12V Bus

The device works well when powering from a 12V bus with a single V_{IN} configuration. As a single V_{IN} configuration, the internal LDO is powered by the 12V bus and generates 4.5V output to bias the internal analog circuitry and also powers up the gate drives. The V_{IN} input range under this configuration is 4V to 18V. Figure 6-5 shows an example for this single V_{IN} configuration.

V_{IN} and CNTL are the two signals to enable the part. For start-up sequence, any sequence between the V_{IN} and CNTL signals can power the device up correctly.

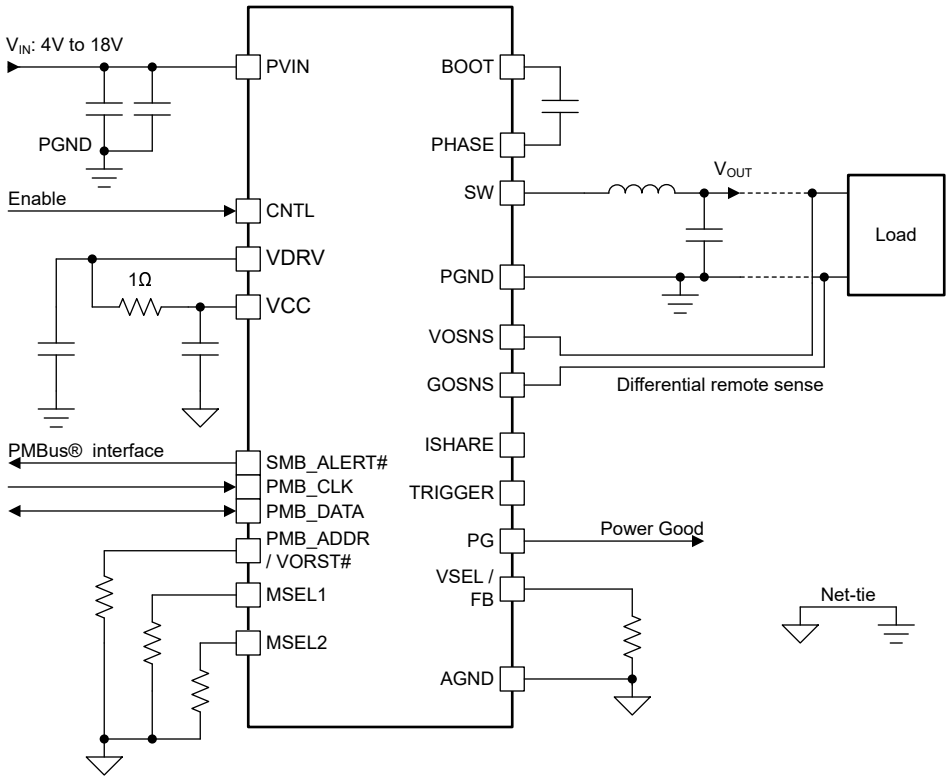


Figure 6-5. Single V_{IN} Configuration With 12V Bus

6.4.4 Powering the Device From a Split-rail Configuration

When an external bias that is at a different level from the main V_{IN} bus is applied to the VCC/VDRV pin, the device can be configured to split rail by using both the main V_{IN} bus and the VCC bias. Connecting a valid bias rail to the VCC/VDRV pin overrides the internal VCC LDO, saving power loss on that linear regulator. This configuration helps improve overall system-level efficiency but requires a valid VCC bias. A 5.0V rail is the common choice for VCC bias. With a stable VCC bias, the V_{IN} input range under this configuration can be as low as 2.7V and up to 18V.

The noise of the external bias affects the internal analog circuitry. To make sure of a proper operation, a clean, low-noise external bias, and a local decoupling capacitor from the VCC pin to PGND pin are required. Figure 6-6 shows an example for this split rail configuration.

The VCC external bias current during nominal operation varies with the bias voltage level and the switching frequency. For example, by setting the device to skip mode, the VCC pin draws less and less current from the external bias when the switching frequency decreases under light load conditions. The typical VCC external bias current under FCCM operation is listed in the *Electrical Characteristics* table to help the user prepare the capacity of the external bias.

Under split rail configuration, PVIN, VCC bias, and CTRL are the signals to enable the part. For the start-up sequence, TI recommends that the external bias is applied on the VCC/VDRV pin earlier than PVIN rail. A practical start-up sequence example is the external 5V bias is applied first, then the 12V bus is applied on PVIN, and then CTRL signal goes high.

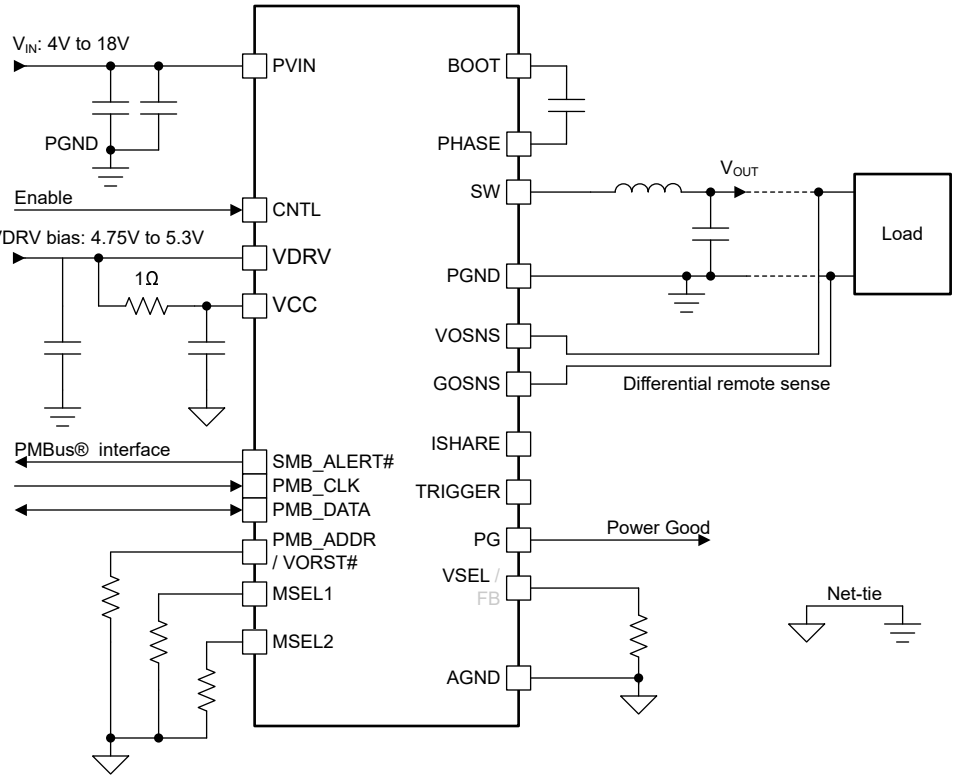


Figure 6-6. Split Rail Configuration With External VCC Bias

6.4.5 Pin-Strapping

The TPS546E25 provides four IC pins that allow the initial PMBus programming value on critical PMBus commands to be selected by the resistors connected to that pin without requiring PMBus communication. Whether a specific PMBus command is initialized to the value selected by the detected resistance or stored NVM memory is determined by the commands bit in the PIN_DETECT_OVERRIDE Command.

Check PIN_DETECT_OVERRIDE default value in Supported PMBus® Commands for which functions are using pin detection or NVM by default.

Table 6-2. Pin-Strapping Functions and Decode Order

FUNCTION	PIN USED FOR PIN-STRAP	PIN-STRAP ORDER
Primary / secondary Internal or external feedback divider Overcurrent limit (OCL) Soft start Fault response	MSEL1	1
Primary: Phase quantity Mode (FCCM/DCM) Primary (Common) PMBus address	PMB_ADDR	2
Secondary: Phase location Unique PMBus address		

Table 6-2. Pin-Strapping Functions and Decode Order (continued)

FUNCTION	PIN USED FOR PIN-STRAP	PIN-STRAP ORDER
Primary: Switching frequency (FSW) RAMP GAIN	MSEL2	3
Switching frequency (FSW) Overcurrent limit (OCL)		
Primary when internal feedback divider is used: VOUT VOSL NRSA VOUT_MAX VOUT_MIN Note: pin-strap is not used when external feedback divider is selected with MSEL1, and the pin becomes FB	VSEL/FB	4
Secondary uses VSEL to set VOSL and VOSM		

Note

The high precision pin-detection programming can be sensitive to PCB contamination from flux, moisture, and debris. As such, users must consider committing pin programmed values to user non-volatile memory and disable future use of pin-strapped values as part of the product flow. The programming sequence to commit pin programmed PMBus register values to NVM and disable future use of pin-strapped programming is:

- Select MSEL1, MSEL2, VSEL, and PMB_ADDR programming resistors to program the desired PMBus register values.
- Power VIN and VCC and VDRV above the UVLOs to initiate pin-detection and enable PMBus communication.
- Update any PMBus register values not programmed to the final value by pin-detection.
- Read the full PMBus registers.
- Perform a STORE/RESTORE.
- Allow a minimum 100ms for the device to complete a burn of NVM User Store. Loss of AVIN or VCC power during this 100ms can compromise the integrity of the NVM. Failure to complete the NVM burn can result in a corruption of NVM and a POR fault on subsequent power on resets.
- Perform a power reset by lowering VCC below the UVLO off threshold, then raising VCC above the UVLO on threshold.

6.4.5.1 Programming MSEL1

The pin-strapping table for MSEL1 is as shown below. Programming of PMBus commands at power-on depends on the value in PIN_DETECT_OVERRIDE . The default value for PIN_DETECT_OVERRIDE is 8E7Dh See PIN_DETECT_OVERRIDE to determine which commands are programmed by MSEL1 The Fault Response column applies to all three types of faults: overtemperature, overvoltage, and undervoltage.

Table 6-3. MSEL1 Resistor for Programming

RESISTOR (kΩ)	PRIMARY/ SECONDARY	FB DIVIDER	OVERCURRENT LIMIT (OCL) (A)	SOFT START (ms)	FAULT RESPONSE
< 1.78	Primary	Internal	50	0.5	Latch-Off
2.21				2	
2.74				0.5	Hiccup
3.32				2	
4.02			40	0.5	Latch-Off
4.87				2	
5.9				0.5	Hiccup
7.32				2	
9.09			30	0.5	Latch-Off
11.3				2	
14.3				0.5	Hiccup
18.2				2	
22.1		External	50	0.5	Hiccup
26.7				2	
33.2				4	
40.2				8	
49.9			40	0.5	Hiccup
60.4				2	
76.8				4	
102				8	
137			30	0.5	Hiccup
174				2	
243				8	
> 412	Secondary	N/A	See MSEL2 Secondary Device	N/A	Hiccup

6.4.5.2 Programming PMB_ADDR

The pin-strapping table for PMB_ADDR is shown below. The PMBus address used can be sourced from PMBus register PMBus_ADDR instead of pin-strapping, depending on the state of the OVRD_PMB_ADDR bit in the PIN_DETECT_OVERRIDE register. When pin-strapping is used as the source of PMBus address, the contents of PMBus_ADDR indicating PMBus address (bits [14:8]) are updated with the pin-strapped values.

The table below shows the valid PMBus address configurations for primary and secondary devices through pin-strap.

Table 6-4. Allowed Combinations of PMB_ADDR

SINGLE PHASE	TWO PHASE	THREE PHASE	FOUR PHASE
All Resistor Values between 0Ω and 18.2kΩ	Primary: 22.1kΩ Secondary: 0Ω	Primary: 49.9kΩ First Secondary: 4.02kΩ Second Secondary: 9.09kΩ	Primary: 137kΩ First Secondary: 22.1kΩ Second Secondary: 49.9kΩ Third Secondary: 137kΩ
	Primary: 26.7kΩ Secondary: 2.21kΩ	Primary: 60.4kΩ First Secondary: 4.87kΩ Second Secondary: 11.3kΩ	Primary: 174kΩ First Secondary: 26.7kΩ Second Secondary: 60.4kΩ Third Secondary: 174kΩ
	Primary: 33.2kΩ Secondary: 2.74kΩ	Primary: 76.8kΩ First Secondary: 5.9kΩ Second Secondary:14.3kΩ	Primary: 243kΩ First Secondary: 33.2kΩ Second Secondary: 76.8kΩ Third Secondary: 243kΩ
	Primary: 40.2kΩ Secondary: 3.32kΩ	Primary: 102kΩ First Secondary: 7.32kΩ Second Secondary Secondary:18.2kΩ	Primary: > 412kΩ First Secondary: 40.2kΩ Second Secondary: 102kΩ Third Secondary: > 412kΩ

Table 6-5. Resistor for Programming When MSEL1 Selects Primary = 1 (Primary Device)

RESISTOR (kΩ)	PRIMARY STACK NUMBER	MODE	COMMON ADDRESS
< 1.78	Primary Device - 1 Phase Stack	FCCM	11h
2.21			12h
2.74			13h
3.32		DCM	14h
4.02			15h
4.87			16h
5.9		FCCM	17h
7.32			18h
9.09			19h
11.3		DCM	1Ah
14.3			1Bh
18.2			1Ch
22.1	Primary Device - 2 Phase Stack	FCCM	0Dh
26.7			0Eh
33.2			0Fh
40.2			10h
49.9	Primary Device - 3 Phase Stack		0Dh
60.4			0Eh
76.8			0Fh
102			10h
137	Primary Device - 4 Phase Stack		0Dh
174			0Eh
243			0Fh
> 412			10h

Table 6-6. Resistor for Programming When MSEL1 Selects Secondary Device

RESISTOR (kΩ)	PRIMARY STACK NUMBER	MODE	COMMON ADDRESS	UNIQUE ADDRESS
< 1.78	First Secondary Device - 2 Phase Stack	FCCM	0Dh	1Dh
2.21			0Eh	1Eh
2.74			0Fh	1Fh
3.32			10h	20h
4.02	First Secondary Device - 3 Phase Stack		0Dh	1Dh
4.87			0Eh	1Eh
5.9			0Fh	1Fh
7.32			10h	20h
9.09	Second Secondary Device - 3 Phase Stack		0Dh	3Dh
11.3			0Eh	3Eh
14.3			0Fh	3Fh
18.2			10h	30h
22.1	First Secondary - 4 Phase Stack		0Dh	1Dh
26.7			0Eh	1Eh
33.2			0Fh	1Fh
40.2			10h	20h
49.9	Second Secondary - 4 Phase Stack		0Dh	3Dh
60.4			0Eh	3Eh
76.8			0Fh	3Fh
102			10h	30h
137	Third Secondary - 4 Phase Stack		0Dh	5Dh
174			0Eh	5Eh
243			0Fh	5Fh
> 412			10h	50h

6.4.5.3 Programming MSEL2

The pin-strapping table for MSEL2 is shown below. Programming of PMBus commands at power-on depends on the value in PIN_DETECT_OVERRIDE . The default value for PIN_DETECT_OVERRIDE is 8E7Dh See PIN_DETECT_OVERRIDE to determine which commands are programmed by MSEL2 and which are programmed by NVM default values

The defaults for the GAIN and RAMP values are:

- GAIN1 = 3V/V (user programmable by (D4h) COMP)
- GAIN2 = 10V/V
- GAIN3 = 30V/V
- RAMP1 = 60mV (user programmable by (D4h) COMP)
- RAMP2 = 120mV

Table 6-7. MSEL2 Resistor for Programming When MSEL1 Selects Primary = 1 (Primary Device)

RESISTOR (kΩ)	SWITCHING FREQUENCY (FSW) (kHz)	GAIN	RAMP
< 1.78	600	3V/V	60mV
2.21			120mV
2.74		10V/V	60mV
3.32			120mV
4.02		30V/V	60mV
4.87			120mV
5.9	800	3V/V	60mV
7.32			120mV
9.09		10V/V	60mV
11.3			120mV
14.3		30V/V	60mV
18.2			120mV
22.1	1000	3V/V	60mV
26.7			120mV
33.2		10V/V	60mV
40.2			120mV
49.9		30V/V	60mV
60.4			120mV
76.8	1400	3V/V	60mV
102			120mV
137		10V/V	60mV
174			120mV
243		30V/V	60mV
> 412			120mV

Table 6-8. MSEL2 Resistor for Programming When MSEL1 selects Primary = 0 (Secondary Device)

RESISTOR (kΩ)	SWITCHING FREQUENCY (FSW) (kHz)	OVERCURRENT LIMIT
< 1.78	600	50
2.21		
2.74		40
3.32		
4.02		30
4.87		
5.9	800	50
7.32		
9.09		40
11.3		
14.3		30
18.2		

Table 6-8. MSEL2 Resistor for Programming When MSEL1 selects Primary = 0 (Secondary Device) (continued)

RESISTOR (kΩ)	SWITCHING FREQUENCY (FSW) (kHz)	OVERCURRENT LIMIT
22.1	1000	50
26.7		
33.2		40
40.2		
49.9		30
60.4		
76.8	1400	50
102		
137		40
174		
243		30
> 412		

Table 6-9. MSEL2 Resistor for Programming When MSEL1 selects Primary = 0 (Secondary Device)

RESISTOR (kΩ)	SWITCHING FREQUENCY (FSW) (kHz)	OVERCURRNT LIMIT(OCL) (A)
< 1.78	600	50
2.21		
2.74		40
3.32		
4.02		30
4.87		
5.9	1000	50
7.32		
9.09		40
11.3		
14.3		30
18.2		
22.1	1400	50
26.7		
33.2		40
40.2		
49.9		30
60.4		
76.8	2000	50
102		
137		40
174		
243		30
> 412		

6.4.5.4 Programming VSEL\FB

When MSEL1 selects internal divider, the VSEL\FB pin behaves as VSEL. The resistor for VSEL programs the VOUT, VOSL, NRSA, VOUT_MIN, and VOUT_MAX as in the table below. VBOOT is VBOOT_OFFSET_1 and VOSL is VOUT_SCALE_LOOP. NRSA is derived from VOSL (NRSA = 1/VOSL). The value from VSEL can be overridden with the OVRD_VSEL bit in PIN_DETECT_OVERRIDE .

When MSEL1 selects external divider, the VSEL\FB pin behaves as FB, where the VBOOT is the NVM value with a default of 0.4V and VOSL of 1.0.

The VOUT and VFB voltages listed in this table do not include any offset programmed by (22h) VOUT_TRIM. Check the default value of (22h) VOUT_TRIM in *Supported PMBus® Commands* for any offset applied to VOUT.

In a multi-device stack, followers must use a VSEL resistor to select the appropriate VOUT_SCALE_LOOP value for the output voltage. If the primary device is using an internal divider, selecting the same VSEL resistor as the primary. If the primary device is using an external divider, select the VSEL resistor with the lowest VOUT_MAX greater than the maximum expected output voltage

Table 6-10. VSEL Resistor for Programming for Primary Device

RESISTOR (kΩ)	VOUT (V)	VBOOT_1 (b)	VOSL	NRSA	VOUT_MIN (V)	VOUT_MAX (V)
< 1.78	0.3	00001	1	1	0.25	0.75
2.21	0.5	10001				
2.74	0.55	10101				
3.32	0.6	11001				
4.02	0.65	11011				
4.87	0.7	00101	0.5	2	0.5	1.5
5.9	0.75	00111				
7.32	0.8	01001				
9.09	0.85	01011				
11.3	0.9	01101				
14.3	0.95	01111				
18.2	1	10001				
22.1	1.05	10011				
26.7	1.1	10101				
33.2	1.2	11001				
40.2	1.3	00011	0.25	4	1	3
49.9	1.5	00111				
60.4	1.8	01101				
76.8	2	10001				
102	2.5	00010	0.125	8	2	5.75
137	3	00111				
174	3.3	01010				
243	5	11010				
> 412	VBOOT NVM (0.4V default)	VBOOT_NVM	VOSL NVM (1.0 default)	1 (default)	VOUT_MIN NVM (0.25V default)	VOUT_MAX NVM (0.75V default)

Table 6-11. VSEL Resistor for Programming for Secondary Devices

RESISTOR (kΩ)	VOSL	NRSA	VOUT_MIN (V)	VOUT_MAX (V)
< 1.78	1	1	0.25	0.75
2.21				
2.74				
3.32				
4.02				
4.87	0.5	2	0.5	1.5
5.9				
7.32				
9.09				
11.3				
14.3				
18.2				
22.1				
26.7				
33.2				
40.2	0.25	4	1	3
49.9				
60.4				
76.8				
102	0.125	8	2	5.75
137				
174				
243				
> 412	VOSL NVM (1 default)	1 (default)	VOUT_MIN NVM (0.25V default)	VOUT_MAX NVM (0.75V default)

6.5 Programming

6.5.1 Supported PMBus® Commands

The following table lists the implemented registers and also the default for the bit behavior and register values.

Table 6-12. Supported PMBus® Commands and Default Values

COMMAND CODE	COMMAND NAME	R/W	NVM	DEFAULT VALUE (Hex)	DEFAULT BEHAVIOR
01h	OPERATION	R/W	NO	04h	Defines the operation of the device.
02h	ON_OFF_CONFIG	R/W	YES	16h	Turn ON/OFF by CNTL pin, Use TOFF_DELAY
03h	CLEAR_FAULTS	W	NO	N/A	Clear all faults.
04h	PHASE	R	NO	N/A	STACK_POSITION set by pin-strap selection.
09h	P2_PLUS_WRITE	W	NO	N/A	Page Plus Write function to send a command to a specific page and phase or all phases.
0Ah	P2_PLUS_READ	R	NO	N/A	Page Plus Read function to read data in a specific page and phase or all phases.
0Eh	PASSKEY	R/W	YES	00h	Passkey to lock access to (DDh) EXT_WRITE_PROTECTION
10h	WRITE_PROTECT	R/W	YES	00h	All Commands are writable
15h	STORE_USER_ALL	W	NO	N/A	Stores all current storable register settings into NVM.
16h	RESTORE_USER_ALL	W	NO	N/A	Restores all storable register settings from NVM.
19h	CAPABILITY	R	NO	D0h	The device has an SMB_ALERT# pin.
1Bh	SMBALERT_MASK	R/W	YES	N/A	Sets ability to mask events that trigger SMB_ALERT#.

Table 6-12. Supported PMBus® Commands and Default Values (continued)

COMMAND CODE	COMMAND NAME	R/W	NVM	DEFAULT VALUE (Hex)	DEFAULT BEHAVIOR
20h	VOUT_MODE	R	NO	97h	Indicates the device is relative format with an exponent value of -9 for an equivalent LSB of 1.953mV.
21h	VOUT_COMMAND	R/W	NO	VSEL	Set the output voltage through PMBus.
22h	VOUT_TRIM	R/W	YES	0000h	Apply a fixed offset voltage to the output voltage command value.
24h	VOUT_MAX	R/W	YES	VSEL	Maximum output voltage, initially set by pin-strap and settable by PMBus.
25h	VOUT_MARGIN_HIGH	R/W	YES	0210h	Sets the margin high percentage when selected in OPERATION register.
26h	VOUT_MARGIN_LOW	R/W	YES	01F0h	Sets the margin low percentage when selected in OPERATION register.
27h	VOUT_TRANSITION_RATE	R/W	YES	E850h	Sets the rate in mV/µs the output changes voltage.
29h	VOUT_SCALE_LOOP	R/W	YES	VSEL	Sets the feedback resistor ratio.
2Ah	VOUT_SCALE_MONITOR	R/W	YES	VSEL	Sets the feedback resistor ratio when external feedback divider is used for telemetry purposes.
2Bh	VOUT_MIN	R/W	YES	VSEL	Minimum output voltage, initially set by pin-strap and settable by PMBus.
33h	FREQUENCY_SWITCH	R/W	YES	MSEL2	Sets the switching frequency with default set by MSEL2 resistor
35h	VIN_ON	R/W	YES	0002h	PVIN ON threshold
36h	VIN_OFF	R/W	YES	0002h	PVIN OFF threshold
39h	IOUT_CAL_OFFSET	R/W	YES	F000h	Used to add or subtract a fixed offset from READ_IOUT with default of 0A.
40h	VOUT_OV_FAULT_LIMIT	R/W	YES	024Dh	VOUT Tracking OV Fault threshold = +12%
41h	VOUT_OV_FAULT_RESPONSE	R/W	YES	MSEL1	Fault Response from MSEL1
42h	VOUT_OV_WARN_LIMIT	R/W	YES	0229h	VOUT Tracking OV Warn threshold = +8%
43h	VOUT_UV_WARN_LIMIT	R/W	YES	01D7h	VOUT Tracking UV Fault threshold = -8%
44h	VOUT_UV_FAULT_LIMIT	R/W	YES	0185Dh	VOUT Tracking UV Fault threshold = -24%
45h	VOUT_UV_FAULT_RESPONSE	R/W	YES	MSEL1	Fault Response from MSEL1
46h	IOUT_OC_FAULT_LIMIT	R/W	YES	MSEL1	Valley Current Limit set by MSEL1
48h	IOUT_OC_LV_FAULT_LIMIT	R	NO	VOUT_UV	Same as VOUT_UV_FAULT_LIMIT
49h	IOUT_OC_LV_FAULT_RESPONSE	R	NO	VOUT_UV	Fault Response from VOUT_UV_FAULT_LIMIT
4Ah	IOUT_OC_WARN_LIMIT	R/W	YES	0030h	Output Overcurrent Warning Level 48A
4Fh	OT_FAULT_LIMIT	R/W	YES	1024h	Programmable OT fault limit = 145° C
50h	OT_FAULT_RESPONSE	R/W	YES	MSEL1	Fault Response from MSEL1
51h	OT_WARN_LIMIT	R/W	YES	101Fh	Programmable OT fault limit = 125° C
55h	VIN_OV_FAULT_LIMIT	R/W	YES	0809h	PVIN OV Fault Threshold = 18.5V
60h	TON_DELAY	R/W	YES	F800h	50µs turn-on delay
61h	TON_RISE	R/W	YES	MSEL1	Set by MSEL1
64h	TOFF_DELAY	R/W	YES	F800h	0ms turn-off delay
65h	TOFF_FALL	R/W	YES	F800h	0.5ms from the end of Toff Delay
78h	STATUS_BYTE	R	NO	41h	Status is device is OFF, and OTH is 1b.
79h	STATUS_WORD	R	NO	2841h	VIN is off and PGOOD_Z is 1b.
7Ah	STATUS_VOUT	R/W	YES	00h	Current status
7Bh	STATUS_IOUT	R/W	YES	00h	Current status
7Ch	STATUS_INPUT	R/W	YES	00h	Current status
7Dh	STATUS_TEMPERATURE	R/W	YES	00h	Current status
7Eh	STATUS_CML	R/W	NO	00h	Current status
7Fh	STATUS_OTHER	R/W	NO	00h	Current status
80h	STATUS_MFR_SPECIFIC	R/W	YES	00h	Current status
88h	READ_VIN	R	NO	N/A	Measured input voltage.
8Bh	READ_VOUT	R	NO	N/A	Measured output voltage.

Table 6-12. Supported PMBus® Commands and Default Values (continued)

COMMAND CODE	COMMAND NAME	R/W	NVM	DEFAULT VALUE (Hex)	DEFAULT BEHAVIOR
8Ch	READ_IOUT	R	NO	N/A	Measured output current.
8Dh	READ_TEMP_1	R	NO	N/A	Measured Controller die temperature
98h	PMBUS_REVISION	R	NO	55h	PMBus 1.5
99h	MFR_ID	R	NO	4954h	ASCII for "TI"
9Ah	MFR_MODEL	R	YES	0000h	Blank Manufacturer Model
9Bh	MFR_REVISION	R/W	YES	00h	Device revision
ADh	IC_DEVICE_ID	R	NO	5449546E2500h	IC part number
AEh	IC_DEVICE_REV	R	NO	00h	IC revision
D1h	SYS_CFG_USER1	R/W	YES	0000h	User Configuration Options
D3h	PMBUS_ADDR	R/W	YES	PMBUS ADDR	PMBus Address set by PMBUS_ADDR pin
D4h	COMP	R/W	YES	MSEL2	COMP set by MSEL2 pin detection
D5h	VBOOT_OFFSET_1	R/W	YES	VSEL	VBOOT set by VSEL
D6h	STACK_CONFIG	R	NO	N/A	Set by PMBUS_ADDR pin programming
D8h	PIN_DETECT_OVERRIDE	R/W	YES	8E7Dh	All Pin Detection Used
D9h	NVM_CHECKSUM	R	NO	DE7Eh	NVM Checksum excluding Passkey
DAh	READ_TELEMETRY	R	NO	N/A	Read VOUT, IOUT, and TEMP with a block read.
DBh	STATUS_ALL	R	NO	N/A	Read all STATUS with a block read.
DDh	EXT_WRITE_PROTECTION	RW	YES	0000h	All Pin Detection Used
DEh	IMON_CAL	R/W	YES	07h	READ_IOUT calibration adjustment 0%
FCh	FUSION_ID0	R	NO	02C0h	Device Identification used by FUSION
FDh	FUSION_ID1	R	NO	4B434F4Ch	Device Identification used by FUSION

7 Register Maps

7.1 Conventions for Documenting Block Commands

According to the SMBus specification, block commands are transmitted across the PMBus interface in ascending order. The description below shows the convention this document follows for documenting block commands.

When block values are listed as register map tables, block values are listed in byte order from top to bottom starting with Byte N and ending with Byte 1.

- Byte 1 (first byte sent) corresponds to bits 7:0.
- Byte 2 (second byte sent) corresponds to bits 15:8.
- Byte 3 (third byte sent) corresponds to bits 23:16.
- … and so on

When block values are listed as text in hexadecimal, block values are listed in byte order, from left to right, starting with Byte N and ending with Byte 1 with a space between each byte of the value. For example, in block 00 28 4C 54 49 54h, the byte order returned in response to a Block Read is:

- Byte 1, bits 7:0 = 54h
- Byte 2, bits 15:8 = 49h
- Byte 3, bits 23:16 = 54h
- Byte 4, bits 31:24 = 4Ch
- Byte 5, bits 39:32 = 28h
- Byte 6, bits 47:40 = 00h

Figure 7-1. Block Command Byte Ordering

47	46	45	44	43	42	41	40
RW	RW	RW	RW	RW	RW	RW	RW
Byte N							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
Byte …							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
Byte 4							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
Byte 3							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
Byte 2							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
Byte 1							

LEGEND: R/W = Read/Write; R = Read only

7.2 (01h) OPERATION

Register Address	01h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	No
Updates:	On-the-fly

The OPERATION command is used to enable or disable power conversion, in conjunction input from the enable pin, according to the configuration of the OPERATION command. It is also used to set the output voltage to the upper or lower MARGIN levels, and select soft-stop.

Return to Supported PMBus Commands.

Figure 7-2. (01h) OPERATION Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R	R
ON	OFF	MARGIN				0	0

LEGEND: R/W = Read/Write; R = Read only

Table 7-1. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	ON	R/W	0b	Enable/disable power conversion when the command is configured to require input from the CMD bit for output control. Note that there can be several other requirements that must be satisfied before the power conversion can begin (for example, input voltages above UVLO thresholds, enable pins high if required by (02h) ON_OFF_CONFIG and so forth). 0b: Disable power conversion. 1b: Enable power conversion if VIN is greater than the VIN_UVLO threshold, the CMD bit is high, and the SPR in the (02h) ON_OFF_CONFIG register is low, or the CPR is high and the CNTL pin is enabled.When the device is configured as a secondary device, this bit is always set to 1b.
6	OFF	R/W	0b	This bit controls the turnoff profile when (02h) ON_OFF_CONFIG is configured to require input from the CMD bit for output voltage control and OPERATION bit 7 transitions from 1b to 0b 0b: Immediate Off. Power conversion stops immediately and the power stage is forced to a high-Z state. 1b: Soft Off. Power conversion continues for the TOFF_ DELAY time, then the output voltage is ramped down at a slew rate according to TOFF_ FALL. Once the output voltage finishes ramping down, power conversions stops.
5:2	MARGIN	R/W	0001b	Sets the margin state. 0000b, 0001b, 0010b: Margin OFF. Output voltage target is (21h) VOUT_COMMAND, OV/UV faults behave normally per their respective fault response settings. 0101b: Margin Low (Ignore Fault if bit 7 is 1b). Output voltage target is Section 7.19. OV/UV faults are ignored and do not trigger shut-down or STATUS updates. 0110b: Margin Low (Act on Fault). Output voltage target is Section 7.19. OV/UV faults trigger per their respective fault response settings. 1001b: Margin High (Ignore Fault). Output voltage target is Section 7.18. OV/UV trigger are ignored and do not trigger shut-down or STATUS update. 1010b: Margin High (Act on Fault). Output voltage target is Section 7.18. OV/UV trigger per their respective fault response settings. Other: Invalid/Unsupported data
1	Reserved	R	0b	Not used and always set to 0.
0	Reserved	R	0b	Not used and always set to 0.

Attempts to write OPERATION to any value other than those listed above will be considered invalid/unsupported data and cause the device to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification, section 10.9.3.

7.3 (02h) ON_OFF_CONFIG

CMD Address	02h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
NVM Back-up:	EEPROM
Updates:	On-the-fly

The ON_OFF_CONFIG command configures the combination of enable pin input and PMBus commands needed to enable/disable power conversion. This includes how the unit responds when power is applied to PVIN. For the purposes of ON_OFF_CONFIG, the device pin CNTL is the CONTROL pin.

If the device is configured as a secondary device, the device will respond as bit 4 (PU) = 0b regardless of the state of the ON_OFF_CONFIG bits, the CNTL pin, and the PMBus ON bit, and any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT. The recommendation is to connect all CNTL pins together when in a stacked configuration.

Return to Supported PMBus Commands.

Figure 7-3. (02h) ON_OFF_CONFIG Register Map

7	6	5	4	3	2	1	0
R	R	R	R/W	R/W	R/W	R	R/W
0	0	0	PU	CMD	CPR	POL	CPA

LEGEND: R/W = Read/Write; R = Read only

Table 7-2. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:5	Reserved	R	000b	Not used and always set to 0.
4	PU	R/W	NVM	0b: Device starts power conversion any time the input power is present regardless of the state of the CONTROL(1) pin. 1b: Act on CONTROL pin and/or (01h) OPERATION command to start/stop power conversion as programmed in bits [3:0] in ON_OFF_CONFIG.
3	CMD	R/W	NVM	0b: Ignore (01h) OPERATION command to start/stop power conversion. 1b: Act on (01h) OPERATION command (and CONTROL pin if configured by CP) to start/stop power conversion.
2	CPR	R/W	NVM	0b: Ignore CONTROL pin to start/stop power conversion. 1b: Act on CONTROL pin (and (01h) OPERATION command if configured by bit [3]) to start/stop power conversion.
1	POL	R	1b	1b: CONTROL pin has active high polarity.
0	CPA	RW	NVM	0b: When power conversion is commanded OFF by the CONTROL pin (must be configured to respect the CONTROL pin as above), continue regulating for the time Section 7.44, then ramp the output voltage down in the time defined by Section 7.45. 1b: When power conversion is commanded OFF by the CONTROL pin (must be configured to respect the CONTROL pin as above), stop power conversion immediately.

(1) For the purposes of ON_OFF_CONFIG, the device pin CNTL is the CONTROL pin.

Attempts to write ON_OFF_CONFIG to any value other than those explicitly listed above will be considered invalid/unsupported data and cause the device to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification, section 10.9.3.

7.4 (03h) CLEAR_FAULTS

CMD Address	03h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
NVM Back-up:	No
Updates:	On-the-fly

CLEAR_FAULTS is a command used to clear any fault bits that have been set. This command clears all bits in all status registers. At the same time, the device releases its SMB_ALERT# signal output if SMB_ALERT# is asserted. CLEAR_FAULTS is a write-only command with no data.

The CLEAR_FAULTS command does not cause a unit that has shutdown due to a fault with a "Do Not Restart" fault response to restart. If the fault is still present when the bit is cleared, the fault bit is immediately set again and the host is notified by the usual means.

If the device successfully responds to an Alert Response Address (ARA) with its PMBus Address, it will clear SMB_ALERT# but not the status bit or bits (as it has successfully notified the host and then expects the host to handle the interrupt appropriately). The original fault (and any faults that occur between the initial assertion of SMB_ALERT# and the successful response of the device to the ARA) must be cleared (through CLEAR_FAULTS, turning on the output through the mechanism programmed into ON_OFF_CONFIG, writing 1b to the status bits set, or power reset) before any of these sources are allowed to re-trigger SMB_ALERT#. However, fault sources which become active after the device response to the ARA trigger SMB_ALERT#.

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7.5 (04h) PHASE

CMD Address	04h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Byte
NVM Back-up:	No
Updates:	On-the-fly

The PHASE command provides the ability to read the PHASE value for a device in a multi-phase stack so the device can be accessed by the common PMBus address for the stack using the (09h) P2_PLUS_WRITE and (0Ah) P2_PLUS_READ command. The value reflects the stack position STACK_POSITION<1:0> as stored in (D6h) STACK_CONFIG - reflecting the effect of PMBus updates or setting the OVRD_STACK_POS bit in PIN_DETECT_OVERRIDE.

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Figure 7-4. (04h) PHASE Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	STACK_POSITION	

LEGEND: R/W = Read/Write; R = Read only

Table 7-3. Register Field Descriptions

Bit	Field	Access	Reset	Description
1:0	STACK_POSITION	R	0b	See STACK_CONFIG, STACK_POSITION

7.6 (09h) P2_PLUS_WRITE

CMD Address	09h
Write Transaction:	Write Block
Read Transaction:	N/A
Format:	Varies (Target Command + 3 bytes)
Phased:	No
NVM Back-up:	No
Updates:	On-the-fly

The P2_PLUS_WRITE command is used to send a command and its associated data to:

- A specific page and phase (valid phases are 00h – 03h),
- All phases (PHASE = FFh) in specific page,
- A specific phase in all pages (PAGE = FFh),
- Or all phases in all pages (PAGE = FFh and PHASE = FFh)

within the addressed device without altering the value of the PAGE or PHASE command after the P2_PLUS_WRITE command is completed.

The only valid PAGE settings are 00h and FFh, which are treated the same. For any PAGE settings outside the valid range, the primary device will set the IVC bit and assert SMBALERT#. The PHASE setting can be set to the unique phase determined by STACK_POSITION in STACK_CONFIG or all phases (PHASE = FFh). For any PHASE settings outside the valid range, the primary device will set the IVC bit and assert SMBALERT#.

P2_PLUS_WRITE uses a Block Write format with 3 additional bytes byond the data of the base command. 1 byte for PAGE, 1 byte for PHASE, and 1 byte for the target command to be written.

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Figure 7-5. (09h) P2_PLUS_WRITE Register Map

23	22	21	20	19	18	17	16
W	W	W	W	W	W	W	W
P2_PLUS_WR_CMD							
15	14	13	12	11	10	9	8
W	W	W	W	W	W	W	W
P2_PLUS_WR_PHASE_NUM							
7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
P2_PLUS_WR_PAGE_NUM							

LEGEND: R/W = Read/Write; R = Read only

Table 7-4. Register Field Descriptions

Bit	Field	Access	Reset	Description
23:16	P2_PLUS_WR_CMD	W	00000000b	
15:8	P2_PLUS_WR_PHASE_NUM	W	00000000b	
7:0	P2_PLUS_WR_PAGE_NUM	W	00000000b	

7.7 (0Ah) P2_PLUS_READ

CMD Address	0Ah
Write Transaction:	N/A
Read Transaction:	Block Write - Block Read Process Call
Format:	Varies - As Target Command + 3 bytes
Phased:	Yes
NVM Back-up:	No
Updates:	On-the-fly

Description: The P2_PLUS_READ command is used to read the data associated with a command from:

- A specific page and phase,
- All phases (PHASE = FFh) in specific page,
- A specific phase in all pages (PAGE = FFh), or
- All phases in all pages (PAGE = FFh and PHASE = FFh)

within the addressed device without altering the value of the PAGE or PHASE command after the P2_PLUS_READ command is completed.

The only valid PAGE settings are 00h and FFh, which are treated the same. For any PAGE settings outside the valid range, the primary device will set the IVC bit and assert SMBALERT#. The PHASE setting can be to the unique phase determined by STACK_POSITION in STACK_CONFIG or all phases (PHASE = FFh). For any PHASE settings outside the valid range, the primary device will set the IVC bit and assert SMBALERT#.

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Figure 7-6. (09h) P2_PLUS_READ Register Map

23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
P2_PLUS_RD_CMD							
15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
P2_PLUS_RD_PHASE_NUM							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
P2_PLUS_RD_PAGE_NUM							

LEGEND: R/W = Read/Write; R = Read only

Table 7-5. Register Field Descriptions

Bit	Field	Access	Reset	Description
23:16	P2_PLUS_RD_CMD	RW	00000000b	
15:8	P2_PLUS_RD_PHASE_NUM	RW	00000000b	
7:0	P2_PLUS_RD_PAGE_NUM	RW	00000000b	

7.8 (0Eh) PASSKEY

CMD Address	0Eh
Write Transaction:	Write Block (4 Bytes)
Read Transaction:	Read (3 Bytes)
Format:	Unsigned Binary (4 bytes or 3 bytes)
Phased:	Yes
NVM Back-up:	EEPROM
Updates:	On-the-fly

The PMBus 1.5 standard command PASSKEY provides a customer with the ability to lock access to EXT_WRITE_PROTECTION with a User Programmed up to 32-bit passkey[KJ1] . The PASSKEY will accept fewer or more bytes on a write without NACKing.

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Figure 7-7. (0Eh) PASSKEY Register Map

15	14	13	12	11	10	9	8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PASSKEY_3				PASSKEY_2			
7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PASSKEY_1				PASSKEY_0			

LEGEND: R/W = Read/Write; R = Read only

Writing a non-zero value using PASSKEY will lock write access to EXT_WRITE_PROTECT (and STORE_USER_ALL if SNVML (EXT_WP[0]) is set) only after sending a STORE_USER_ALL command and performing a POWER_ON_RESET, or sending the PMBus command RESTORE_USER_ALL.

As a user option the NVM_CHECKSUM is read back as the next two bytes after the PASSKEY data.

When PASSKEY = 0000h, EXT_WRITE_PROTECT is unlocked and writable unless write protected by WRITE_PROTECT or EXT_WRITE_PROTECT . Non-Volatile memory is Unlocked. STORE commands function normally unless write protected by WRITE_PROTECT or EXT_WRITE_PROTECT . A READ on PASSKEY that has not yet been written will return 0000h. A WRITE on PASSKEY will set PASSKEY to be stored to NVM via STORE_USER_ALL.

When PASSKEY =! 0000h, Non-Volatile memory is locked. STORE_USER_ALL and EXT_WRITE_PROTECT is NACKED as “UNSUPPORTED or INVALID DATA”

A READ on PASSKEY will report a value of:

- 10h if no invalid attempts have been made to unlock PASSKEY
- 11h if One invalid attempt has been made to unlock PASSKEY
- 12h if Two invalid attempts have been made to unlock PASSKEY
- 1Fh if Three or more invalid attempts have been made to unlock PASSKEY

If a WRITE on PASSKEY does not match the value of PASSKEY in PASSKEY at Power On Reset or RESTORE_USER_ALL, the PASSKEY invalid access attempt counter is incremented. If the Counter reaches 3, all further WRITE attempts are considered invalid and the device will NACK and set IVD_DATA bit in STATUS_CML

If the WRITE data matches the Passkey used to PASSKEY access and less than 3 invalid attempts have been made, PASSKEY is allowed to be overwritten with a new PASSKEY value, including 0000h and the Invalid Attempts counter is reset to 0.

7.9 (10h) WRITE_PROTECT

CMD Address	10h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly

The WRITE_PROTECT command controls writing to the PMBus device. The intent of this command is to provide protection against accidental changes; it has one data byte that is described below. This command does NOT provide protection against deliberate or malicious changes to a configuration or operation of the device. All supported commands can have their parameters read, regardless of the WRITE_PROTECT settings.

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Figure 7-8. (10h) WRITE_PROTECT Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
WRITE_PROTECT							

LEGEND: R/W = Read/Write; R = Read only

Table 7-6. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:5	WRITE_ PROTECT	R/W	NVM	00h: Enable writes to all commands. 20h: Disables all write access except to the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG, STORE_USER_ALL, and VOUT_COMMAND commands. 40h: Disables all writes except to the WRITE_PROTECT, OPERATION, and STORE_USER_ALL commands. 80h: Disables all writes except to the WRITE_PROTECT and STORE_USER_ALL commands. 02h: Disables writes to all PMBus commands except VOUT_COMMAND (requires power-cycle to restore write access) 03h: Disables writes to all PMBus commands (requires power-cycle to restore write access) Other: Invalid/Unsupported data
4:0		R/W	00000b	

Attempts to write WRITE_PROTECT to any invalid value as specified above will be considered invalid/ unsupported data and cause the device to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification, section 10.9.3.

7.10 (15h) STORE_USER_ALL

CMD Address	15h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
NVM Back-up:	No
Updates:	Not recommended for on-the-fly-use, but not explicitly blocked

The STORE_USER_ALL command instructs the PMBus device to copy the entire contents of the Operating Memory to the matching locations in the non-volatile User Store Memory. Any items in Operating Memory that do not have matching locations in the User Store Memory are ignored.

The NVM values for command which are derived from Pin Programming on power-up are not updated in NVM unless written to since the last power-on and prior to the use of STORE_USER_ALL. If the bit for a command is updated in

NVM store operations are not recommended while the output is enabled, although the user is not explicitly prevented from doing so, as interruption can result in a corrupted NVM. PMBus commands issued during this time will be ignored. Following issuance of NVM store operations, TI recommends disabling regulation and waiting a minimum of 125ms before continuing.

EEPROM programming faults will cause the device to respond by flagging bit [1] in STATUS_CML.

Return to Supported PMBus Commands.

Figure 7-9. (15h) STORE_USER_ALL Register Map

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
STORE_USER_ALL							

LEGEND: R/W = Read/Write; R = Read only

7.11 (16h) RESTORE_USER_ALL

CMD Address	16h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
NVM Back-up:	No
Updates:	Not recommended for on-the-fly-use, but not explicitly blocked

The RESTORE_USER_ALL command instructs the PMBus device to copy the entire contents of the non-volatile User Store Memory to the matching locations in the Operating Memory. Then any values set through a Pin Detection after the last power-cycle overwrite the values in Operating Memory, unless otherwise specified in the particular register. The values in the Operating Memory are overwritten by the value retrieved from the User Store and Pin Detection. If the corresponding override bit is set in PIN_DETECT_OVERRIDE , the value from User Store Memory is not overwritten with the value set through Pin Detection.

Note

It is permitted to use the RESTORE_USER_ALL command while the output is enabled. However, PMBus commands will be ignored during the copy operation and there can be unpredictable, undesirable or even catastrophic results if done while the output is enabled. TI recommends to turn the device output off before issuing this command through the method programmed into ON_OFF_CONFIG.

Return to Supported PMBus Commands.

Figure 7-10. (16h) RESTORE_USER_ALL Register Map

7	6	5	4	3	2	1	0
W	W	W	W	W	W	W	W
RESTORE_USER_ALL							

LEGEND: R/W = Read/Write; R = Read only

7.12 (19h) CAPABILITY

CMD Address	19h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	No
Updates:	N/A

This command provides a way for the host to determine the capabilities of this PMBus device. This command is read-only and has one data byte formatted as below.

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Figure 7-11. (19h) CAPABILITY Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
PEC	SPEED		ALERT	FORMAT	AVSBUS	0	0

LEGEND: R/W = Read/Write; R = Read only

Table 7-7. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	PEC	R	1b	1b: Packet Error Checking is supported.
6:5	SPEED	R	10b	10b: Maximum supported bus speed is 1MHz.
4	ALERT	R	1b	1b: The device has an SMB_ALERT# pin and supports the SMBus Alert Response Protocol.
3	FORMAT	R	0b	0b: Numeric format is LINEAR or DIRECT.
2	AVSBUS	R	0b	0b: AVSBus is NOT supported.
1:0	Reserved	R	00b	Reserved and always set to 0.

7.13 (1Bh) SMBALERT_MASK

CMD Address:	1Bh
Write Transaction:	Write Word
Read Transaction:	Block Write-Block Read Process Call
Format:	Write: Unsigned Binary (2 bytes) Read: Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly

The SMBALERT_MASK command can be used to prevent a warning or fault condition from asserting the SMB_ALERT# signal. Setting a MASK bit does not prevent the associated bit in the STATUS_x command from being set, but prevents the associated bit in the STATUS_x command from asserting SMB_ALERT#. The following register descriptions describe the individual mask bits available.

SMBALERT_MASK write transaction is Write Word with the following:

- CMD Address = 1Bh
- Write Data Byte Low = STATUS_x COMMAND CODE
- Write Data Byte High = STATUS_x MASK

SMBALERT_MASK read transaction is a Block Write-Block Read Process Call with the following:

- CMD Address = 1Bh
- Byte Count = 1
- Write Data Byte = STATUS_x COMMAND CODE
- Byte Count = 1
- Read Data Byte = STATUS_x MASK

Please refer to the PMBus 1.3.1 Part II specification, section 15.38 SMBALERT_MASK Command for further details on this command, and the SMBus 3.1 specification, section 6.5.8 Block Write-Block Read Process Call for further details on the process call transaction.

STATUS_BYTE added and STATUS_WORD extended per new requirement in PMBus 1.4 Section 15.38.

Writing to a mask bit marked with an X with either a 0 or 1 will not cause an IVD error in (7Eh) STATUS_CML. A bit marked with ‘X’ will default to a mask value of ‘1’ and is incapable of ever asserting SMBALERT# (most commonly these are un-supported read-only logic 0 status bit positions. Attempting to read or write a mask byte for any STATUS_X command code other than this list shall be considered as invalid data or unsupported data (IVD) error in (7Eh) STATUS_CML

For all registers, a 0b indicates that SMB_ALERT# will be asserted when the condition happens, and a 1b indicates that SMB_ALERT# will not be asserted when the condition happens.

Return to Supported PMBus Commands.

Figure 7-12. (1Bh) SMBALERT_MASK_BYTE Register Map

7	6	5	4	3	2	1	0
R	R	R/W	R/W	R	R/W	R/W	R/W
0	MASK_OFF	MASK_OVF	MASK_OCF	0	MASK_OTFW	MASK_CML	MASK_OTH

Note

Mask for (78h) STATUS_BYTE (default = XX00 X000b) (lower byte)

Figure 7-13. (1Bh) SMBALERT_MASK_WORD Register Map

15	14	13	12	11	10	9	8
R/W	R/W	R/W	R/W	R	R	R/W	R

Figure 7-13. (1Bh) SMBALERT_MASK_WORD Register Map (continued)

MASK_VFW	MASK_OCFW	MASK_INPUT	MASK_MFR	MASK_PGOOD_Z	0	MASK_OTHER	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
STATUS_BYTE							

Note

Mask for (79h) STATUS_WORD (default = 0000 XX0Xb) (upper byte)

Figure 7-14. (1Bh) SMBALERT_MASK_VOUT Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R	R	R
MASK_OVF	MASK_OVW	MASK_UVW	MASK_UVF	MASK_VO_MAX_MIN_W	0	0	0

Note

Mask for (7Ah) STATUS_VOUT (default = 0000 0XXXb)

Figure 7-15. (1Bh) SMBALERT_MASK_IOUT Register Map

7	6	5	4	3	2	1	0
R/W	R	R/W	R/W	R	R	R	R
MASK_OCF	MASK_OCUV	MASK_OCW	MASK_UCF	0	0	0	0

Note

Mask for (7Bh) STATUS_IOUT (default = 0X00 XXXXb)

Figure 7-16. (1Bh) SMBALERT_MASK_INPUT Register Map

7	6	5	4	3	2	1	0
R/W	R	R	R	R/W	R	R	R
PVIN_OVF	0	0	0	LOW_VIN	0	0	0

Note

Mask for (7Ch) STATUS_INPUT (default = 0XXX 0XXXb)

Figure 7-17. (1Bh) STATUS_TEMPERATURE Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R	R	R	R	R	R
OTF_PROG	OTW_PROG	0	0	0	0	0	0

Note

Mask for (7Dh) STATUS_TEMPERATURE (default = 00XX XXXXb)

Figure 7-18. (1Bh) SMBALERT_MASK_CML Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R	R	R/W	R
MASK_IVC	MASK_IVD	MASK_PEC	MASK_MEM	0	0	MASK_OTHER	0

Note

Mask for (7Eh) STATUS_CML (default = 0000 XX0Xb)

Figure 7-19. (1Bh) SMBALERT_MASK_OTHER Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R/W
0	0	0	0	0	0	0	MASK_FRST_2_ALRT

Note

Mask for (7Fh) STATUS_OTHER (default = XXXX XXX0b)

Figure 7-20. (1Bh) SMBALERT_MASK_MFR_SPECIFIC Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R	R	R/W	R/W
MASK_DCM	MASK_OTF_BG	MASK_PS_FLT	MASK_PS_COMM_WRN	0	0	MASK_PS_OT	MASK_PS_UV

Note

Mask for (80h) STATUS_MFR_SPECIFIC (default = 0000 XX00b)

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7.14 (20h) VOUT_MODE

CMD Address	20h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	No
Updates:	N/A

The data byte for the VOUT_MODE command is one byte that consists of a one bit absolute/relative selection (always set to 1 for relative), two bit MODE, and five bit EXPONENT as shown in Figure 7-21. The two bit MODE sets whether the device uses the ULINEAR16, Half-precision IEEE 754 floating point, VID or DIRECT modes for output voltage related commands. The five bit PARAMETER provides more information about the selected mode, such as the ULINEAR16 exponent or which manufacturer's VID codes are being used.

Return to Supported PMBus Commands.

Figure 7-21. (20h) VOUT_MODE Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
REL	VOUT_MODE		VOUT_EXPONENT				

LEGEND: R/W = Read/Write; R = Read only

Table 7-8. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	REL	R	1b	1b: Relative data format
6:5	MODE	R	00b	00b: Linear format (ULINEAR16, SLINEAR16)
4:0	VOUT_EXPONENT	R	10111b	Specifies the exponent “N” to use with output voltage related commands, in two’s complement format. Value is fixed at -9 (1.953mV/LSB).

Attempts to write VOUT_MODE to any value will be considered invalid/unsupported data and cause the device to respond by flagging the appropriate status bits and notifying the host according to the PMBus 1.3.1 Part II specification, section 10.9.3.

7.15 (21h) VOUT_COMMAND

CMD Address	21h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16 per (20h) VOUT_MODE
NVM Back-up:	No (VBOOT_OFFSET_1) / VOUT_SCALE_LOOP
Updates:	on-the-fly

The regulated output can be set by PMBus or by the result of pin-strapping on pin VSEL. When PMBus or pin-strapping is used to set the regulated voltage, the commanded output voltage in volts is determined by a combination of VOUT_COMMAND, VOUT_TRIM, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, and OPERATION commands, as below. As stated in the description of the VOUT_MODE command, the VOUT step size is 1.953mV.

This register can be changed during soft-start or soft-stop. However, the rail will continue to ramp up/down to the original target (VBOOT) at the rate programmed into TON_RISE/TOFF_FALL. After soft-start completes (and if VOUT_COMMAND is different from the VBOOT value), the device will immediately transition from the VBOOT value to the latest written VOUT_COMMAND at the programmed VOUT_TRANSITION_RATE. Writes to VOUT_COMMAND during soft-stop will be acknowledged, however, no transition will occur and VOUT_COMMAND will get automatically updated back to VBOOT at the conclusion of soft-stop. After soft-start has completed, writes to VOUT_COMMAND are also allowed even if the output voltage is still transitioning to a previously programmed VOUT_COMMAND. The output voltage will immediately begin transitioning to the newly programmed VOUT_COMMAND at the rate specified by VOUT_TRANSITION_RATE. The device does not wait for the prior transition to complete.

Return to Supported PMBus Commands.

Figure 7-22. (21h) VOUT_COMMAND Register Map

15	14	13	12	11	10	9	8
R	R	R	R/W	R/W	R/W	R/W	R/W
VOUT_COMMAND (High Byte)							
7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VOUT_COMMAND (Low Byte)							

The programmed Vout is computed as:

default*: XXX0 0000 0000 0000 (binary) (X means writes will be ignored and reads will be 0)

VOUT = (VOUT_COMMAND + VOUT_TRIM + (VOUT_MARGIN_HIGH – 1) * VOUT_COMMAND * OPERATION[5] – (1 – VOUT_MARGIN_LOW) * VOUT_COMMAND * OPERATION[4]) * VOUT_MODE

LEGEND: R/W = Read/Write; R = Read only

Table 7-9. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:13	VOUT_COMMAND	R	000b	Not used and always set to 0.
12:0	VOUT_COMMAND	R/W	VBOOT_OFFSET_1 (see below)	Sets the output voltage target via the PMBus interface.

VBOOT Voltage

At power up, the reset value of VOUT_COMMAND is derived from VBOOT_OFFSET_1 / VOUT_SCALE_LOOP . When the rail is disabled by the mechanism programmed to ON_OFF_CONFIG or due to a fault, the value in VOUT_COMMAND is updated to VBOOT.

When the PMB_ADDR/VORST# pin is configured as a RESET# pin in SYS_CONFIG_USER1 (EN_VORST), assertion of the PMB_ADDR/VORST# pin causes the output voltage to return to the VBOOT value in VBOOT_OFFSET_1 (VBOOT_1), and causes the VOUT_COMMAND value to be updated accordingly.

Data Validity

Writes to VOUT_COMMAND for which the resulting value, including any offset from VOUT_TRIM, is greater than the current (24h) VOUT_MAX or less than the current (2Bh) VOUT_MIN, causes the VOUT_COMMAND to move to the value specified by (2Bh) VOUT_MIN or (24h) VOUT_MAX respectively. The VOUT_MAX_MIN warning bit is set in STATUS_VOUT, which sets the appropriate bit in STATUS_WORD, and the host is notified per the PMBus 1.3.1 Part II specification, section 10.2.

7.16 (22h) VOUT_TRIM

CMD Address	22h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR16 per (20h) VOUT_MODE
NVM Back-up:	EEPROM
Updates:	on-the-fly

VOUT_TRIM is used to apply a fixed offset voltage to the output voltage command value. Output voltage changes due to VOUT_TRIM occur at the rate specified by (27h) VOUT_TRANSITION_RATE.

Return to Supported PMBus Commands.

Figure 7-23. (22h) VOUT_TRIM Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
VOUT_TRIM (High Byte)							
7	6	5	4	3	2	1	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VOUT_TRIM (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 7-10. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:7	VOUT_TRIM_SIG_EXT	R	NVM	The 9 MSBs are read only limiting the range of VOUT_TRIM that can be programmed. Their value is set through sign extension of bit 6.
6:0	VOUT_ TRIM	RW	NVM	Output voltage offset. SLINEAR16 With the exponent of -9, the values will be limited to +123mV to -125mV.

Data Validity

The output voltage value (including any offset from VOUT_TRIM, (21h) VOUT_COMMAND, VOUT_MARGIN_HIGH, …) may not exceed the values supported by the DAC hardware.

Programming a VOUT_COMMAND + VOUT_TRIM value greater than the maximum value supported by the DAC hardware but less than (24h) VOUT_MAX will result in the regulated output voltage clamping at the maximum value supported by the DAC hardware and setting the VOUT_MAX_MIN warning bit in STATUS_VOUT.

Attempts to write VOUT_TRIM to any value outside those specified as valid, will be considered invalid/ unsupported data and cause the device to respond by flagging the appropriate status bits, and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

7.17 (24h) VOUT_MAX

CMD Address	24h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16, Absolute Only per VOUT_MODE
Phased:	No
NVM Back-up:	EEPROM or Pin Detection
Updates:	On-the-fly

The VOUT_MAX command sets an upper limit on the output voltage the unit and can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level.

Return to Supported PMBus Commands.

Figure 7-24. (24h) VOUT_MAX Register Map

15	14	13	12	11	10	9	8
R	R	R	R	RW	RW	RW	RW
0	0	0	0	VOUT_MAX			
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MAX							

LEGEND: R/W = Read/Write; R = Read only

Table 7-11. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:12	0	R	0b	Not supported and always 0.
11:0	VOUT_MAX	RW	NVM	Maximum output voltage. LINEAR16 absolute per the setting of (20h) VOUT_MODE. Refer to the following description for data validity.

The recommended data range for VOUT_MAX depends on the VOUT_SCALE_LOOP according to the table below:

VOUT_SCALE_LOOP mantissa	VOUT_MAX (V)	Data (d)
8d	0.34 - 0.75	175-384
4d	0.34 - 1.5	175 - 768
2d	0.68 - 3	350 - 1536
1d	1.36 - 5.75	700 - 2944

While conversion is enabled, any output voltage change (including VOUT_COMMAND, (22h) VOUT_TRIM, margin operations) that causes the new target voltage to be greater than the currenet value of VOUT_MAX will cause the VOUT_MAX_MIN_WARNING condition. This result causes the device to:

- Set to the output voltage to current value of VOUT_MAX at the slew rate defined by (27h) VOUT_TRANSITION_RATE.
- Set the NONE OF THE ABOVE bit in the (78h) STATUS_BYTE.
- Set the VOUT bit in the (79h) STATUS_WORD.
- Set the VOUT_MIN_MAX warning bit in (7Ah) STATUS_VOUT.
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2.

Although the scenario is uncommon, note that the same response results if the user attempted to program VOUT_MAX less than the current output voltage target.

In the event VOUT_MAX < (2Bh) VOUT_MIN, VOUT_MAX will dominate.

Data Validity

Attempts to write VOUT_MAX to any value outside those specified as valid will be considered invalid/ unsupported data and cause the device to respond by flagging the appropriate status bits and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

7.18 (25h) VOUT_MARGIN_HIGH

CMD Address	25h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16, relative, per VOUT_MODE
Phased:	No
NVM Back-up:	EEPROM
Updates:	On-the-fly

The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”. Because the Vout format is set to *relative* in the (20h) VOUT_MODE register – bit [7], the commanded Vout will increase by the multiplicative factor indicated in this command. This command also uses the LSB specified by (20h) VOUT_MODE. Output voltage transitions during margin operation occur at the slew rate defined by VOUT_TRANSITION_RATE.

When the MARGIN bits in the OPERATION command indicate “Margin High,” the output voltage is updated to the value of VOUT_MARGIN_HIGH + VOUT_TRIM.

Return to Supported PMBus Commands.

Figure 7-25. (25h) VOUT_MARGIN_HIGH Register Map

15	14	13	12	11	10	9	8
R	W	W	W	W	RW	RW	RW
VOUT_MARGIN_HIGH (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MARGIN_HIGH (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 7-12. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	Reserved	R	0b	
10:0	VOUT_ MARGIN_HI GH	RW	NVM	Margin High output voltage. ULINEAR16 relative per the setting of VOUT_ MODE

To optimize the number of EEPROM bits needed for this command, the bits in the above register do not have direct backup, but instead are correlated to an NVM backed bit called MRGN_HI_DFLT, that is used as below during EEPROM restore:

MARGIN_HI_DFLT	VOUT_MARGIN_HIGH[10:0]	% Margin
0b	528d	3.125
1b	536d	4.6875

The effect of this command is determined by the settings of the VOUT_MODE command. The table below also shows how the MRGN_HI_DFLT is determined for NVM storage.

VOUT_MARGIN_HIGH[10:0]		% Margin	MRGN_HI_DFLT
Greater than or equal to (decimal)	Less than (decimal)		
	524	1.5625	0
524	532	3.125	
532	540	4.6875	1
540	548	6.25	
548	556	7.8125	
556	564	9.375	
564	572	10.9375	
572	2048	12.5	

The minimum and maximum valid data values for VOUT_MARGIN_HIGH follow the description in VOUT_COMMAND. That is, the total combined output voltage, including VOUT_MARGIN_HIGH and VOUT_TRIM, follow the values allowed by the current VOUT_MAX setting.

Attempts to write (25h) VOUT_MARGIN_HIGH to any value outside those specified as valid will be considered invalid/unsupported data and cause the device to respond by flagging the appropriate status bits and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

7.19 (26h) VOUT_MARGIN_LOW

CMD Address	26h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16, Relative, per VOUT_MODE
Phased:	No
NVM Back-up:	EEPROM

The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”. Because the Vout format is set to *relative* in the VOUT_MODE register – bit [7], the commanded Vout will decrease by the multiplicative factor indicated in this command. This command also uses the LSB specified by VOUT_MODE. Output voltage transitions during margin operation occur at the slew rate defined by VOUT_TRANSITION_RATE.

When the MARGIN bits in the OPERATION command indicate “Margin Low,” the output voltage is updated to the value of VOUT_MARGIN_LOW + VOUT_TRIM.

Return to Supported PMBus Commands.

Figure 7-26. (26h) VOUT_MARGIN_LOW Register Map

15	14	13	12	11	10	9	8
W	W	W	W	W	W	RW	RW
VOUT_MARGIN_LOW (High Byte)							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MARGIN_LOW (Low Byte)							

LEGEND: R/W = Read/Write; R = Read only

Table 7-13. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:10	Reserved	R	0b	
9:0	VOUT_ MARGIN_L OW	RW	NVM	Margin Low output voltage. LINEAR16 relative per the setting of VOUT_ MODE

To optimize the number of EEPROM bits needed for this command, the bits in the above register do not have direct backup, but instead are correlated to an NVM backed bit called MRGN_LO_DFLT, that is used as below during EEPROM restore:

MARGIN_HI_DFLT	VOUT_MARGIN_HIGH[10:0]	% Margin
0b	496d	-3.125
1b	488d	-4.6875

The effect of this command is determined by the settings of the VOUT_MODE command. The table below also shows how the MRGN_LO_DFLT is determined for NVM storage.

VOUT_MARGIN_LOW[9:0]		% Margin	MRGN_LO_DFLT
> (d)	< (d)		
500	1024	-1.5625	0
492	500	-3.125	

VOUT_MARGIN_LOW[9:0]		% Margin	MRGN_LO_DFLT
> (d)	< (d)		
484	492	-4.6875	1
476	484	-6.25	
468	476	-7.8125	
460	468	-9.375	
452	460	-10.9375	
	452	-12.5	

The minimum and maximum valid data values for VOUT_MARGIN_LOW follow the description in VOUT_COMMAND. Attempts to write (26h) VOUT_MARGIN_LOW to any value outside those specified as valid will be considered invalid/unsupported data and cause the device to respond by flagging the appropriate status bits and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

7.20 (27h) VOUT_TRANSITION_RATE

CMD Address	27h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	LINEAR11
NVM Back-up:	EEPROM
Updates:	On-the-fly

The VOUT_TRANSITION_RATE sets the slew rate at which any output voltage changes during normal power conversion occur. This commanded rate of change does not apply when the unit is commanded to turn on or to turn off. The units are mV/µs.

Return to Supported PMBus Commands.

Figure 7-27. (27h) VOUT_TRANSITION_RATE Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
EXPONENT					VOUT_TRANSITION_RATE		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_TRANSITION_RATE							

LEGEND: R/W = Read/Write; R = Read only

Table 7-14. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	1 1101b	Linear format two's complement exponent. Fixed exponent of -3 resulting in 0.125mV/µs LSB.
10:8	VOUT_TRANSITION_RATE	R	0	Not used and always set to 0.
7:0		R/W	NVM	Linear format two's complement mantissa.

Data Validity

Writes to the read-only bits in the exponent and mantissa will be ignored and their value will not be updated. Every binary combination in the read/write mantissa bits is writeable and readable. However, the actual output voltage slew rate is set to the nearest supported setting. Additionally, the mantissa value restored from EEPROM is fixed for each supported setting. Refer to Table 7-15.

Table 7-15. Supported VOUT_TRANSITION_RATE settings and EEPROM restore values

VOUT_TRANSITION_RATE mantissa (decimal)		VOUT_TRANSITION_RATE (mV/µs)
Greater than or equal to	Less than	
0	8	0.625
8	15	1.26
15	30	2.44
30	42	4.88
42	62	6.51
62	84	9.77
84	144	13
144	256	19.53

7.21 (29h) VOUT_SCALE_LOOP

CMD Address	29h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	SLINEAR11
Updates:	Output disabled: see below. Output enabled: read-only.
NVM Back-up:	EEPROM

VOUT_SCALE_LOOP allows PMBus devices to map between the commanded voltage and the voltage at the control circuit input. The VOUT_SCALE_LOOP also programs an internal precision resistor divider so no external divider is required.

If MSEL1 pin-strap results in external resistor divider (VSEL/FB pin configured as a FB pin with external resistor divider), VOUT_SCALE_LOOP mantissa is set to 8.

The VOUT_SCALE_LOOP data can be written over PMBus only if:

- MSEL1 pin-strap results in internal resistor divider (VSLE/FB pin is configured as VSEL function), AND
- The rail is disabled by any of the ON_OFF_CONFIG mechanisms (in the DISABLE state).

Return to Supported PMBus Commands.

Figure 7-28. Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					VOUT_SCALE_LOOP		
7	6	5	4	3	2	1	0
R	R	R	R	R/W	R/W	R/W	R/W
VOUT_SCALE_LOOP							

LEGEND: R/W = Read/Write; R = Read-only

Table 7-16. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	1 1101b	Linear format two's complement exponent. Fixed exponent of -3 resulting in 0.125 LSB.
10:4	VOUT_SCALE_LOOP	R	0	Not used and always set to 0.
3:0	VOUT_SCALE_LOOP	R/W	NVM or VSEL resistor	Linear format two's complement mantissa. If the OVRD_VSEL bit in PIN_DETECT_OVERRIDE is set to 0, this value is set by the resistance detected from the VSEL pin to ground. To program this to a different value through PMBus, the OVRD_VSEL bit must be set to 1 and stored to NVM, then the device's VCC reset.

Data Validity

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware. Refer to Table 7-17.

Table 7-17. VOUT_SCALE_LOOP supported values and EEPROM restore values

VOUT_SCALE_LOOP mantissa (decimal)		Internal divider gain	VOUT_SCALE_LOOP mantissa EEPROM restore value (decimal)
Greater than or equal to	Less than		
0	2	0.125	1

Table 7-17. VOUT_SCALE_LOOP supported values and EEPROM restore values (continued)

VOUT_SCALE_LOOP mantissa (decimal)		Internal divider gain	VOUT_SCALE_LOOP mantissa EEPROM restore value (decimal)
Greater than or equal to	Less than		
2	4	0.25	2
4	8	0.5	4
8	16	1.0	8

7.22 (2Ah) VOUT_SCALE_MONITOR

CMD Address	2Ah
Write Transaction:	Write Word (if external feedback resistor is selected via MSEL1 pin-strap)
Read Transaction:	Read Word
Format:	LINEAR11
Updates:	On-the-fly when writable
NVM Back-up:	EEPROM or VSEL resistor

VOUT_SCALE_MONITOR indicates how VOUT scaling should be done if the external feedback resistor option is selected via MSEL1 pin-strap. VOUT_SCALE_MONITOR is set to VOUT_SCALE_LOOP when an internal feedback resistor is used and this command is then read only. If an external feedback resistor divider is selected, the user must select a value for VOUT_SCAL_MONITOR, which will then be used internal in place of the VOUT_SCALE_LOOP value.

Return to Supported PMBus Commands.

Figure 7-29. Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					VOUT_SCALE_MONITOR		
7	6	5	4	3	2	1	0
R	R	R	R	R/W	R/W	R/W	R/W
VOUT_SCALE_MONITOR							

LEGEND: R/W = Read/Write; R = Read-only

Table 7-18. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	1 1101b	Linear format two's complement exponent. Fixed exponent of -3 resulting in 0.125 LSB.
10:4	VOUT_SCALE_MONITOR	R	0	Not used and always set to 0.
3:0	VOUT_SCALE_MONITOR	R/W	NVM or VSEL resistor	Linear format two's complement mantissa. If the OVRD_VSEL bit in PIN_DETECT_OVERRIDE is set to 0, this value is set by the resistance detected from the VSEL pin to ground. To program this to a different value through PMBus, the OVRD_VSEL bit must be set to 1 and stored to NVM, then the device's VCC reset.

Data Validity

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware. Refer to Table 7-19. If the VOUT_SCALE_MONITOR value is chosen such that the maximum allowed VOSNS-GOSNS from the table is violated, then the reported READ_VOUT will not be accurate.

Table 7-19. VOUT_SCALE_MONITOR supported values and EEPROM restore values

VOUT_SCALE_MONITOR mantissa (decimal)		Internal divider gain	VOUT_SCALE_MONITOR mantissa EEPROM restore value (decimal)	Maximum allowed VOUT (VOSNS-GOSNS) (V)
Greater than or equal to	Less than			
0	2	0.125	1	5.5
2	4	0.25	2	3
4	8	0.5	4	1.5

Table 7-19. VOUT_SCALE_MONITOR supported values and EEPROM restore values (continued)

VOUT_SCALE_MONITOR mantissa (decimal)		Internal divider gain	VOUT_SCALE_MONITOR mantissa EEPROM restore value (decimal)	Maximum allowed VOUT (VOSNS-GOSNS) (V)
Greater than or equal to	Less than			
8	16	1.0	8	0.75

7.23 (2Bh) VOUT_MIN

CMD Address	2Bh
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	LINEAR16, Absolute Only per VOUT_MODE
Phased:	No
Updates:	on-the-fly
NVM Back-up:	EEPROM or Pin Detection

The VOUT_MIN command sets a lower limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a level which will render the load inoperable.

Return to Supported PMBus Commands.

Figure 7-30. (2Bh) VOUT_MIN Register Map

15	14	13	12	11	10	9	8
R	R	R	R	RW	RW	RW	RW
0	0	0	0	VOUT_MIN			
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MIN							

LEGEND: R/W = Read/Write; R = Read only

Table 7-20. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:12	VOUT_MIN	R	0000b	Not used and always set to 0.
11:0	VOUT_ MIN	RW	NVM	Minimum output voltage. LINEAR16 absolute per the setting of VOUT_ MODE.

During power conversion, any output voltage change (including VOUT_COMMAND, VOUT_TRIM, margin operations) that causes the new target voltage to be less than the current value of VOUT_MIN will cause the VOUT_MAX_MIN_WARNING fault condition. These results cause the device to:

- Set to the output voltage to current value of VOUT_MIN at the slew rate defined by VOUT_TRANSITION_RATE.
- Set the NONE OF THE ABOVE in the STATUS_BYTE.
- Set the VOUT bit in the STATUS_WORD.
- Set the VOUT_MIN_MAX warning bit in STATUS_VOUT.
- Notify the host per PMBus 1.3.1 Part II specification, section 10.2.

Although the scenario is uncommon, note that the same response results if the user attempted to program VOUT_MIN greater than the current output voltage target.

Data Validity

The minimum and maximum valid data values for VOUT_MIN follow those of VOUT_MAX. Attempts to write VOUT_MIN to any value outside those specified as valid will be considered invalid/unsupported data and cause the device to respond by flagging the appropriate status bits and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

7.24 (33h) FREQUENCY_SWITCH

CMD Address	33h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	SLINEAR11
NVM Backup:	EEPROM
Updates:	On-the-fly

FREQUENCY_SWITCH sets the switching frequency of the active device.

Return to Supported PMBus Commands.

Figure 7-31. (33h) FREQUENCY_SWITCH Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					FREQUENCY_SWITCH		
7	6	5	4	3	2	1	0
R	R	R	R	RW	RW	RW	RW
FREQUENCY_SWITCH							

LEGEND: R/W = Read/Write; R = Read only

Table 7-21. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	0 0111b	Linear format two's complement exponent. Fixed exponent of 7 resulting in 128kHz LSB.
10:4	FREQUENCY_SWITCH	R	000 0000b	Not used and always set to 0.
3:0	FREQUENCY_SWITCH	RW	NVM	Linear format two's complement mantissa.

The default initial value for FREQUENCY_SWITCH can be derived from either NVM or MSEL2 pin-strap.

Table 7-22. FREQUENCY_SWITCH supported values and EEPROM restore values

FREQUENCY_SWITCH [3:0]		SW Frequency (MHz)
Greater than or equal to	Less than	
	0100b (4d)	0.4
0100b (4d)	0110b (6d)	0.6
0110b (6d)	0111b (7d)	0.8
0111b (7d)	1001b (9d)	1.0
1001b (9d)	1010b (10d)	1.2
1010b (10d)	1101b (13d)	1.4
1101b (13d)	1111b (15d)	1.8
1111b (15d)	16d	2.0

Table 7-23. FREQUENCY_SWITCH pin-strap values - see MSEL2 for details

FREQUENCY_SWITCH [3:0]		SW Frequency (MHz)
Greater than or equal to	Less than	
0100b (4d)	0110b (6d)	0.6
0110b (6d)	0111b (7d)	0.8
0111b (7d)	1001b (9d)	1.0

Table 7-23. FREQUENCY_SWITCH pin-strap values - see MSEL2 for details (continued)

FREQUENCY_SWITCH [3:0]		SW Frequency (MHz)
Greater than or equal to	Less than	
1010b (10d)	1101b (13d)	1.4

Data Validity

Attempts to write FREQUENCY_SWITCH to any value outside those specified as valid will be considered invalid/unsupported data and cause the device to respond by flagging the appropriate status bits and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

7.25 (35h) VIN_ON

CMD Address	35h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	LINEAR11
NVM Backup:	EEPROM
Updates:	On-the-fly

The VIN_ON command sets the value of the PVIN input voltage, in Volts, at which the unit starts power conversion.

Return to Supported PMBus Commands.

Figure 7-32. (35h) VIN_ON Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					VIN_ON		
7	6	5	4	3	2	1	0
R	R	R	R	RW	RW	RW	RW
VIN_ON							

LEGEND: R/W = Read/Write; R = Read only

Table 7-24. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	0 0000b	Linear format two's complement exponent. Fixed exponent of 0 resulting in 1V LSB.
10:4	VIN_ON	R	000 0000b	Not used and always set to 0.
3:0	VIN_ON	RW	NVM	Linear format two's complement mantissa.

Note that the PVIN_UVF condition in STATUS_INPUT register is masked until the sensed input voltage exceeds the VIN_ON threshold for the first time following a power-on reset. The EN pin toggles and NVM store or restore operations do not reset this masking.

Table 7-25. VIN_ON supported values and EEPROM restore values

VIN_ON [3:0]		VIN_ON (V)
Greater than or equal to	Less than	
10d	16d	10
9d	10d	9
8d	9d	8
7d	8d	7
6d	7d	6
5d	6d	5
3d	5d	3.8
0d	3d	2.5

7.26 (36h) VIN_OFF

CMD Address	36h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	LINEAR11
NVM Backup:	EEPROM
Updates:	On-the-fly

The VIN_OFF command sets the value of the PVIN input voltage, in Volts, at which the unit must stop power conversion. If the power conversion enable conditions as defined by ON_OFF_CONFIG are met and PVIN is less than the selected VIN_OFF threshold, the power conversion turns off and the PVIN_UVF bit in STATUS_INPUT is set.

Return to Supported PMBus Commands.

Figure 7-33. (35h) VIN_OFF Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					VIN_OFF		
7	6	5	4	3	2	1	0
R	R	R	R	RW	RW	RW	RW
VIN_OFF							

LEGEND: R/W = Read/Write; R = Read only

Table 7-26. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	0 0000b	Linear format two's complement exponent. Fixed exponent of 0 resulting in 1V LSB.
10:4	VIN_ON	R	000 0000b	Not used and always set to 0.
3:0	VIN_ON	RW	NVM	Linear format two's complement mantissa.

While it is possible to set (36h) VIN_OFF threshold greater than (35h) VIN_ON threshold, it is not advisable and can produce rapid enabling and disabling of conversion and undesirable operation. Please set VIN_ON threshold always greater than VIN_OFF threshold.

Table 7-27. VIN_OFF supported values and EEPROM restore values

VIN_OFF [3:0]		VIN_OFF (V)
Greater than or equal to	Less than	
10d	16d	9.5
9d	10d	8.5
8d	9d	7.5
7d	8d	6.5
6d	7d	5.5
5d	6d	4.2
3d	5d	3.6
0d	3d	2.3

7.27 (39h) IOUT_CAL_OFFSET

CMD Address	39h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	LINEAR11
NVM Backup:	EEPROM
Updates:	On-the-fly

The IOUT_CAL_OFFSET is used to add or subtract (if negative) an offset current before reporting in READ_IOUT, for user calibration purposes. The minimum READ_IOUT is clamped to 0 even if negative offset is selected in IOUT_CAL_OFFSET and results in a negative number.

Return to Supported PMBus Commands.

Figure 7-34. (39h) IOUT_CAL_OFFSET

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					IOUT_CAL_OFFSET_SIG_EXT		
7	6	5	4	3	2	1	0
R	R	R	R	R/W	R/W	R/W	R/W
IOUT_CAL_OFFSET_SIG_EXT				IOUT_CAL_OFFSET_MAN			

LEGEND: R/W = Read/Write; R = Read only

Table 7-28. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	1 1110	Linear format two's complement exponent. Fixed exponent of -2 resulting in 0.25A LSB.
10:4	IOUT_CAL_OFFSET_SIG_EXT	R	000 0000b if bit 3 is 0 or 111 1111b if bit 3 is 1	These bits are used to extend the sign of bit 3 in IOUT_CAL_OFFSET_MAN through the rest of the mantissa.
3:0	IOUT_CAL_OFFSET_MAN	RW	NVM	The manitssa of IOUT_CAL_OFFSET_MAN Maximum +7d (0111b) is + 1.75A offset Minimum -8d (1000b) is -2A offset

7.28 (40h) VOUT_OV_FAULT_LIMIT

CMD Address	40h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	ULINEAR16, Relative per (20h) VOUT_MODE
NVM Backup:	EEPROM
Updates:	On-the-fly

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage sensed at the (VOSNS − GOSNS) pins that causes an output overvoltage fault. VOUT_OV_FAULT_LIMIT bits set an overvoltage fault threshold relative to the current VOUT setting that is commanded by VOUT_COMMAND. The VOUT Tracking OVF function is activated after the soft-start ramp completes.

Following an overvoltage fault condition, the device responds according to VOUT_OV_FAULT_RESP.

Return to Supported PMBus Commands.

Figure 7-35. (40h) VOUT_OV_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
Reserved					VOUT_OV_FAULT_LIMIT		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_OV_FAULT_LIMIT							

LEGEND: R/W = Read/Write; R = Read only

Table 7-29. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	Reserved	R	000000b	Not used and always set to 0.
10:0	VOUT_OV_FAULT_LIMIT	R/W	NVM	Sets the overvoltage fault threshold.

Table 7-30. VOUT_OV_FAULT_LIMIT supported values and EEPROM restore values

VOUT_OV_FAULT_LIMIT [10:0]		VOUT_OVF (V)
Greater than or equal to	Less than	
	584d	12%
584d	604d	16%
604d	666d	20%
666d	2048d	50%

7.29 (41h) VOUT_OV_FAULT_RESPONSE

CMD Address	41h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output over-voltage fault. This includes both the fault limit programmed into VOUT_OV_FAULT_LIMIT and the SEL_FIX_OVF selected in SYS_CFG_USER1. The device also:

- Sets the OVF bit in STATUS_BYTE
- Sets the VFW bit in STATUS_WORD
- Sets the OVF bit in STATUS_VOUT, and
- Notifies the host via the SMB_ALERT# pin.

Return to Supported PMBus Commands.

Figure 7-36. (41h) VOUT_OV_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
RW	R	RW	RW	RW	R	R	R
IGNRZ_OV	0	RS_OV			TD_OV		

LEGEND: R/W = Read/Write; R = Read only

Table 7-31. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	IGNRZ_OV	RW	1b	Output overvoltage response setting 0b: The device continues operation (i.e., ignores the fault) without interruption (note that the bit[7] IGNRZ_OV is **active low** so that when IGNRZ_OV=0, the fault is ignored). 1b: The device shuts down (disables the output) and responds according to the retry setting in bits RS_OV. Note that if an OV fault occurred while IGNRZ_OV is set to ignore the fault (0b) and if the fault status was not cleared through CLEAR_FAULTS, and if IGNRZ_OV is changed to 1b, the device will respond to the previous fault as programmed in RS_OV and TD_OV.
6		R	0b	Not used and always set to 0.
5:3	RS_OV	RW	NVM	Output voltage over voltage retry setting. 000b: Latch-off after the fault. A VCC power cycle or EN toggle can restart the power conversion. 111b: Automatically restart after a 52ms delay, without limitation on the number of restart attempts. Any value other than 000b or 111b will not be accepted and such an attempt shall be considered as invalid data or usupported data (ivd) and the device will respond as described in ivd. Because all 3 bits must be the same, only one bit (bit 5) is stored in EEPROM.

Table 7-31. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
2:0	TD_OV	R	000b	Output over voltage retry time delay setting. 000b: The device does not delay a restart, and is only supported with RS_OV = 000b. The output remains disabled until the fault is cleared. 111b: The device waits 52ms before it goes through a normal startup. This is only supported whel RS_OV = 111b. These bits are direct reflections of the RS_OV values. Any values written to these read only bits will be ignored.

7.30 (42h) VOUT_OV_WARN_LIMIT

Data Validity

CMD Address	42h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16, Relative per (20h) VOUT_MODE
NVM Backup:	EEPROM
Updates:	On-the-fly

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage sensed at the (VOSNS − GOSNS) pins that causes an output voltage high warning. This value is typically less than the output overvoltage fault threshold.

When the sensed output voltage exceeds the VOUT_OV_WARN_LIMIT threshold, the OVW bit in the STATUS_VOUT register is set.

Return to Supported PMBus Commands.

Figure 7-37. (42h) VOUT_OV_WARN_LIMIT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
Reserved					VOUT_OV_WARN_LIMIT		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_OV_WARN_LIMIT							

LEGEND: R/W = Read/Write; R = Read only

Table 7-32. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	Reserved	R	000000b	Not used and always set to 0.
10:0	VOUT_OV_WARN_LIMIT	R/W	NVM	Sets the overvoltage warn threshold.

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware.

Table 7-33. VOUT_OV_WARN_LIMIT supported values and EEPROM restore values

VOUT_OV_WARN_LIMIT [10:0]		VOUT_OVW (V)
Greater than or equal to	Less than	
	560d	8%
560d	584d	12%
584d	624d	16%
624d	2048d	28%

Data Validity

Attempts to write VOUT_OV_WARN_LIMIT to any value outside those specified as valid will be considered invalid/unsupported data and cause the device to respond by flagging the appropriate status bits and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

7.31 (43h) VOUT_UV_WARN_LIMIT

Data Validity

CMD Address	43h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16, Relative, per (20h) VOUT_MODE
NVM Backup:	EEPROM
Updates:	On-the-fly

The VOUT_UV_WARN_LIMIT command sets the value of the output voltage sensed at the (VOSNS − GOSNS) pins that causes an output voltage low warning. This value is typically less negative than the output undervoltage fault threshold.

When the sensed output voltage falls below the VOUT Tracking UVW threshold, the UVW bit in the STATUS_VOUT register is set.

Return to Supported PMBus Commands.

Figure 7-38. (43h) VOUT_UV_WARN_LIMIT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	RW	RW
Reserved						VOUT_UV_WARN_LIMIT	
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_UV_WARN_LIMIT							

LEGEND: R/W = Read/Write; R = Read only

Table 7-34. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:10	Reserved	R	000000b	Not used and always set to 0.
10:0	VOUT_OV_WARN_LIMIT	R/W	NVM	Sets the undervoltage warn threshold.

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware.

Table 7-35. VOUT_UV_WARN_LIMIT supported values and EEPROM restore values

VOUT_UV_WARN_LIMIT [10:0]		VOUT_UVW (V)
Greater than or equal to	Less than	
480d	1024d	-4%
464d	480d	-8%
440d	464d	-12%
416d	440d	-16%
400d	416d	-20%
384d	400d	-24%
360d	384d	-28%
	360d	-32%

7.32 (44h) VOUT_UV_FAULT_LIMIT

Data Validity

CMD Address	44h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	ULINEAR16, Relative, per (20h) VOUT_MODE
NVM Backup:	EEPROM
Updates:	On-the-fly

The VOUT_UV_FAULT_LIMIT command sets the value of the output voltage sensed at the (VOSNS − GOSNS) pins that causes an output undervoltage fault. The SEL_UVF bits set an undervoltage fault threshold relative to the current VOUT setting that is commanded by VOUT_COMMAND. The VOUT Tracking UVF function is activated after the soft-start ramp completes.

When the undervoltage fault condition is triggered, the device responds according to VOUT_UV_FAULT_RESPONSE.

Return to Supported PMBus Commands.

Figure 7-39. (44h) VOUT_UV_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	RW	RW
Reserved						VOUT_UV_FAULT_LIMIT	
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_UV_FAULT_LIMIT							

LEGEND: R/W = Read/Write; R = Read only

Table 7-36. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:10	Reserved	R	000000b	Not used and always set to 0.
9:0	VOUT_UV_FAULT_LIMIT	R/W	NVM	Sets the undervoltage fault threshold.

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware.

Attempts to write VOUT_UV_FAULT_LIMIT to any value outside those specified as valid will be considered invalid/unsupported data and cause the device to respond by flagging the appropriate status bits and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Table 7-37. VOUT_UV_FAULT_LIMIT supported values and EEPROM restore values

VOUT_UV_FAULT_LIMIT [10:0]		VOUT_UVF (V)
Greater than or equal to	Less than	
410d	1024d	-16%
369d	410d	-24%
328d	369d	-32%
	328d	-50%

7.33 (45h) VOUT_UV_FAULT_RESPONSE

CMD Address	45h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	EEPROM
Updates:	On-the-fly

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output under-voltage fault. The fault limit is programmed into VOUT_UV_FAULT_LIMIT. The device also:

- Sets the UVF bit in STATUS_BYTE
- Sets the VFW bit in STATUS_WORD
- Sets the UVF bit in STATUS_VOUT, and
- Notifies the host via the SMB_ALERT# pin.

Return to Supported PMBus Commands.

Figure 7-40. (45h) VOUT_UV_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
RW	R	R/W	R/W	R/W	R	R/W	R/W
0	IGNRZ_UV	RS_UV			TD_UV		

LEGEND: R/W = Read/Write; R = Read only

Table 7-38. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	0	R	0b	Not used and always set to 0. A write of 1 to this bit will result in an NACk and ivd.
6	IGNRZ_UV	RW	1b	Output undervoltage response setting 0b: The device continues operation (i.e., ignores the fault) without interruption (note that the bit[6] IGNRZ_UV is **active low** so that when IGNRZ_OV=0, the fault is ignored). 1b: The device continues to operate for the delay time specified by TD_UV. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting. Note that if an UV fault occurred while IGNRZ_UV is set to ignore the fault (0b) and if the fault status was not cleared through CLEAR_FAULTS, and if IGNRZ_UV is changed to 1b, the device will respond to the previous fault as programmed in RS_UV and TD_UV.
5:3	RS_UV	RW	NVM	Output voltage undervoltage retry setting. 000b: Latch-off after the fault. The device remains disabled until the fault is cleared. A VCC power cycle or EN toggle can restart the power conversion. 111b: Automatically restart after a 52ms delay, without limitation on the number of restart attempts, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown. Any value other than 000b or 111b will not be accepted and such an attempt shall be considered as invalid data or usupported data (ivd) and the device will respond as described in ivd. Because all 3 bits must be the same, only one bit (bit 5) is stored in EEPROM.

Table 7-38. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
2:0	TD_UV	R	000b	Output under voltage retry response time delay setting. The hiccup time is always 52ms, but the response can be delayed with the following settings in bits [1:0]. If the fault condition goes away before the delay counter expires, then the delay counter is reset to 0, and the output is not disabled. Bit 2 is read only and always 0. Writing a 1 to bit 2 will be ignored. 000b: 2 us 001b: 16 us 010b: 64 us 011b: 256 us

7.34 (46h) IOUT_OC_FAULT_LIMIT

CMD Address	46h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	LINEAR11
Phased:	Yes
NVM Backup:	EEPROM or Pin Detection
Updates:	On-the-fly

The IOUT_OC_FAULT_LIMIT command sets the value of the output current that causes the overcurrent detector to indicate an overcurrent fault condition. The thresholds selected here are compared to the sensed low-side valley current. See Overcurrent Limit and Low-side Current Sense for more details.

Return to Supported PMBus Commands.

Figure 7-41. (46h) IOUT_OC_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					IOUT_OC_FAULT_LIMIT		
7	6	5	4	3	2	1	0
R* or R/W**	R* or R/W**	R/W	R/W	R/W	R/W	R/W	R/W
IOUT_OC_FAULT_LIMIT							

LEGEND: R/W = Read/Write; R = Read only

Table 7-39. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	00000b	Linear format two's complement exponent. The exponent is configured automatically through other settings, with a result of 1b: 0.5A LSB 0b: 1A LSB
10:8	Reserved	R	00000b	Not used and always set to 0.
7	IOUT_OC_FAULT_LIMIT	R* or R/W**	0b	* When STACK_NUMBER[1:0] = 1b, bit 7 is read only. ** When STACK_NUMBER[1:0] is >2b, bit 7 is readable and writeable as described in P2_PLUS_WRITE Commands and Response to P2_PLUS_READ Commands descriptions.
6	IOUT_OC_FAULT_LIMIT	R* or R/W***	0b	* When STACK_NUMBER[1:0] = 1b, bit 6 is read only. ** When STACK_NUMBER[1:0] is >1b, bit 6 is readable and writeable as described in P2_PLUS_WRITE Commands and Response to P2_PLUS_READ Commands descriptions.
5:0	IOUT_OC_FAULT_LIMIT	R/W	NVM	These bits select the I_{OUT} valley current limiting threshold.

Data Validity

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware.

* Attempts to change the read-only bits (IOUT_OC_FAULT_LIMIT[15:8]) will be considered invalid/unsupported data when STACK_NUMBER[1:0] is = 1b. The device will NACK the unsupported data and the received value will be ignored. The 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the STATUS_CML registers will be set.

** Attempts to change the read-write bit (IOUT_OC_FAULT_LIMIT[7]) will only be considered valid data if STACK_NUMBER[1:0] is > 2b.

*** Attempts to change the read-write bit (IOUT_OC_FAULT_LIMIT[6]) will only be considered valid data if STACK_NUMBER[1:0] is > 1b.

Table 7-40. IOUT_OC_FAULT_LIMIT supported values and EEPROM restore values

IOUT_OC_FAULT_LIMIT [5:0]		IOUT_OC (A)
Greater than or equal to	Less than	
	14d	12.5
14d	17d	15
17d	22d	18.75
22d	25d	23.75
25d	28d	26.25
28d	33d	30 (60%)
33d	37d	35
37d	39d	37.5
39d	42d	40 (80%)
42d	47d	43.75
47d	50d	48.75
50d	53d	50 (100%)
53d	58d	55
58d		60

Response to P2_PLUS_WRITE Commands

When the PMBus host attempts to execute a P2+ write to IOUT_OC_FAULT_LIMIT **with the PHASE data in the command set to FFh**, the expectation is to equally divide the commanded net "Stack OC" level among the phases as their individual "Phase OC" settings. In order to achieve that, the device does the following:

- If STACK_NUMBER[1:0] is 2 (i.e., 2-phase operation), then the incoming commanded Stack OC level is converted to the individual Phase OC level by adding 1, followed by right-shift of 1 bit (i.e., dividing by 2, rounded **up**). The resulting Phase OC level is then binned into the appropriate IOUT_OC value based on the IOUT__OC_FAULT_LIMIT tables above.
- If STACK_NUMBER[1:0] is 4 (i.e., 4-phase operation), then the incoming commanded Stack OC level is converted to the individual Phase OC level by adding 2, followed by right-shift of 2 bits (i.e., dividing by 4, rounded **up**). The resulting Phase OC level is then binned into the appropriate IOUT_OC value based on the IOUT_OC_FAULT_LIMIT tables above.
- If STACK_NUMBER[1:0] is 3 (i.e., 3-phase operation), then the incoming commanded Stack OC level is directly converted to the PHASE IOUT_OC value using the table below:

Table 7-41. 3-ph STACK OC IOUT_OC_FAULT_LIMIT supported values and EEPROM restore values

3-ph STACK OC commanded[5:0]		PHASE IOUT_OC (A)
Greater than or equal to	Less than	
	42d	12.5
42d	51d	15
51d	64d	18.75
64d	75d	23.75
75d	85d	26.25

Table 7-41. 3-ph STACK OC IOUT_OC_FAULT_LIMIT supported values and EEPROM restore values (continued)

3-ph STACK OC commanded[5:0]		PHASE IOUT_OC (A)
Greater than or equal to	Less than	
85d	98d	30 (60%)
98d	109d	35
109d	117d	37.5
117d	126d	40 (80%)
126d	139d	43.75
139d	148d	48.75
148d	158d	50 (100%)
158d	173d	55
173d		60

Response to P2_PLUS_READ Commands

When the PMBus host attempts to execute a P2+ read on IOUT_OC_FAULT_LIMIT **with the PHASE data in the command set to FFh**, only the primary device will respond to P2+ read commands with incoming data for PHASE=FFh. The primary device multiplies the IOUT_OC level by the STACK_NUMBER and reports the product back on the PMBus. For example, if the IOUT_OC is 24A for the primary phase in a 3-phase rail, then a P2+ read with PHASE=FFh will yield 24 x 3 = 72A as the read-back value.

7.35 (48h) IOUT_OC_LV_FAULT_LIMIT

CMD Address	48h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	ULINEAR16, Relative, per (20h) VOUT_MODE
NVM Backup:	No, Set by (44h) VOUT_UV_FAULT_LIMIT
Updates:	On-the-fly

The IOUT_OC_FAULT_LIMIT defines the voltage threshold for UV fault declaration when the part is operating in current-limit conditions. When operating under OC limit conditions, these bits select the tracking VOUT UV fault threshold options which the part shuts down and are specified in the relative format based on LSB specified by VOUT_MODE. The design does not differentiate between these settings and those set by (44h) VOUT_UV_FAULT_LIMIT, so the contents of this register are directly copied from (44h) VOUT_UV_FAULT_LIMIT and have read-only access.

Return to Supported PMBus Commands.

Figure 7-42. (44h) IOUT_OC_LV_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
Reserved					IOUT_OC_LV_FAULT_LIMIT		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
IOUT_OC_LV_FAULT_LIMIT							

7.36 (49h) IOUT_OC_LV_FAULT_RESPONSE

CMD Address	49h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (2 bytes)
NVM Backup:	No
Updates:	On-the-fly

The IOUT_OC_LV_FAULT_RESPONSE register defines the response to a UV fault declaration when the part is operating in current-limit conditions. Upon detecting a fault, the device:

- Sets the IOUT_OC_FAULT bit in STATUS_BYTE
- Sets the IOUT bit in STATUS_WORD
- Sets the OCUV bit in STATUS_IOUT, and
- Notifies the host via the SMB_ALERT# pin.

Return to Supported PMBus Commands.

Figure 7-43. (49h) IOUT_OC_LV_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
0	IGNRZ_OC_LV	RS_OC_LV			TD__OC_LV		

LEGEND: R/W = Read/Write; R = Read only

Table 7-42. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	0	R	0b	Not used and always set to 0.
6	IGNRZ_OC_LV	R	1b	Output overvoltage response setting during OC. These bits are copied directly from VOUT_UV_FAULT_RESPONSE and have read only access in this register. 0b: The device continues operation (i.e., ignores the fault) without interruption (note that the bit[6] IGNRZ_UV is **active low** so that when IGNRZ_OV=0, the fault is ignored). 1b: The device continues to operate for the delay time specified by TD_OC_LV. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting.
5:3	RS_OC_LV	R	NVM	Output voltage under voltage retry setting. These bits are copied directly from VOUT_UV_FAULT_RESPONSE and have read only access in this register. 000b: Latch-off after the fault. The device remains disabled until the fault is cleared. A VCC power cycle or EN toggle can restart the power conversion. 111b: Automatically restart after a 52ms delay, without limitation on the number of restart attempts, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown. Any value other than 000b or 111b will not be accepted and such an attempt shall be considered as invalid data or usupported data (ivd) and the device will respond as described in ivd. Because all 3 bits must be the same, only one bit (bit 5) is stored in EEPROM.

Table 7-42. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
2:0	TD_OC_LV	R	000b	Output under voltage retry response time delay setting. These bits are copied directly from VOUT_UV_FAULT_RESPONSE and have read only access in this register. The hiccup time is always 52ms, but the response can be delayed with the following settings in bits [1:0]. If the fault condition goes away before the delay counter expires, then the delay counter is reset to 0, and the output is not disabled. Bit 2 is read only and always 0. 000b: 2 us 001b: 16 us 010b: 64 us 011b: 256 us

7.37 (4Ah) IOUT_OC_WARN_LIMIT

CMD Address	46h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	LINEAR11
Phased:	Yes
NVM Backup:	EEPROM
Updates:	On-the-fly

The IOUT_OC_WARN_LIMIT command sets the average value of the output current that causes the overcurrent detector to indicate an overcurrent warn condition.

Return to Supported PMBus Commands.

Figure 7-44. (46h) IOUT_OC_WARN_LIMIT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					IOUT_OC_WARN_LIMIT		
7	6	5	4	3	2	1	0
R	R	RW	RW	RW	RW	RW	RW
IOUT_OC_WARN_LIMIT							

LEGEND: R/W = Read/Write; R = Read only

Table 7-43. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	00000b	Linear format two's complement exponent. The exponent is configured automatically through other settings, with a result of 0b: 1A LSB
10:6	Reserved	R	00000b	Not used and always set to 0.
5:0	IOUT_OC_WARN_LIMIT	R/W	NVM	These bits select the average I_{OUT} warning threshold.

Data Validity

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware.

Attempts to change the read-only bits (IOUT_OC_WARN_LIMIT[15:6]) will be considered invalid/unsupported data. The device will NACK the unsupported data and the received value will be ignored. The 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the (7Eh) STATUS_CML registers will be set.

Table 7-44. IOUT_OC_WARN_LIMIT supported values and EEPROM restore values

IOUT_OC_WARN_LIMIT [5:0]		IOUT_OCW (A)
Greater than or equal to	Less than	
	8d	5
8d	13d	10
13d	18d	15
18d	23d	20
23d	28d	25

Table 7-44. IOUT_OC_WARN_LIMIT supported values and EEPROM restore values (continued)

IOUT_OC_WARN_LIMIT [5:0]		IOUT_OCW (A)
Greater than or equal to	Less than	
28d	33d	30
33d	38d	35
38d	43d	40
43d	48d	45
48d	53d	50
53d		55

Response to P2_PLUS_WRITE Commands

When the PMBus host attempts to execute a P2+ write to IOUT_OC_WARN_LIMIT **with the PHASE data in the command set to FFh**, the expectation is to equally divide the commanded net “Stack OCW” level among the phases as their individual “Phase OCW” settings. In order to achieve that, the device does the following:

- If STACK_NUMBER[1:0] is 2 (i.e., 2-phase operation), then the incoming commanded Stack OCW level is converted to the individual Phase OCW level by adding 1, followed by right-shift of 1 bit (i.e., dividing by 2, rounded **up**). The resulting Phase OCW level is then binned into the appropriate IOUT_OCW value based on the IOUT_OC_WARN_LIMIT tables above.
- If STACK_NUMBER<1:0> is 4 (i.e., 4-phase operation), then the incoming commanded Stack OCW level is converted to the individual Phase OCW level by adding 2, followed by right-shift of 2 bits (i.e., dividing by 4, rounded **up**). The resulting Phase OCW level is then binned into the appropriate IOUT_OCW value based on the IOUT_OC_WARN_LIMIT tables above.
- If STACK_NUMBER<1:0> is 3 (i.e., 3-phase operation), then the incoming commanded Stack OCW level is directly converted to the PHASE IOUT_OCW value using the table below:

Table 7-45. 3-ph STACK OCW IOUT_OC_WARN_LIMIT supported values and EEPROM restore values

3-ph STACK OCW commanded[5:0]		PHASE IOUT_OC (A)
Greater than or equal to	Less than	
	23d	5
33d	38d	10
41d	53d	15
51d	68d	20
60d	83d	25
68d	98d	30
78d	113d	35
87d	128d	40
93d	143d	45
101d	158d	50
111d	159d	55

Response to P2_PLUS_READ Commands

When the PMBus host attempts to execute a P2+ read on IOUT_OC_WARN_LIMIT **with the PHASE data in the command set to FFh**, only the primary device will respond to P2+ read commands with incoming data for PHASE=FFh. The primary device multiplies the IOUT_OCW level by the STACK_NUMBER and reports the product back on the PMBus. For example, if the IOUT_OCW is 25A for the primary phase in a 3-phase rail, then a P2+ read with PHASE=FFh will yield 25 x 3 = 75A as the read-back value.

7.38 (4Fh) OT_FAULT_LIMIT

CMD Address	4Fh
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	LINEAR11
Phased:	Yes
NVM Backup:	EEPROM
Updates:	On-the-fly

The OT_FAULT_LIMIT command sets the temperature of the unit at which it indicates an overtemperature fault condition. The unit of this command is degrees Celsius. This feature utilizes a digital comparator that compares the output of the IC TEMPERATURE telemetry to the fault threshold selected in this register.

The device response to an overtemperature event is described in (50h) OT_FAULT_RESPONSE.

Return to Supported PMBus Commands.

Figure 7-45. (4Fh) OT_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
Reserved					OT_FAULT_LIMIT		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OT_FAULT_LIMIT							

Figure 7-46.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
Reserved					OT_FAULT_LIMIT		

Figure 7-46.

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OT_FAULT_LIMIT							

LEGEND: R/W = Read/Write; R = Read only

Table 7-46. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	00010b	Linear format two's complement exponent with a result of 4 degrees Celcius LSB.
10:6	Reserved	R	00000b	Not used and always set to 0.
5:0	OT_FAULT_LIMIT	R/W	NVM (default 10 0010b (145 degrees C)	These bits select the over-temperature fault threshold in the controller die, based on the precision temperature sensor in the telemetry system.

Data Validity

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware.

Attempts to change the read-only bits (OT_FAULT_LIMIT[15:6]) will be considered invalid/unsupported data. The device will NACK the unsupported data and the received value will be ignored. The 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the (7Eh) STATUS_CML registers will be set.

Table 7-47. OT_FAULT_LIMIT supported values and EEPROM restore values

OT_FAULT_LIMIT [5:0]		OTF (deg C)
Greater than or equal to	Less than	
	30d	115
30d	31d	120
31d	32d	125
32d	34d	130
34d	35d	135
35d	36d	140
36d	37d	145
37d		150

7.39 (50h) OT_FAULT_RESPONSE

CMD Address	50h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	LINEAR11
Phased:	No
NVM Backup:	EEPROM
Updates:	On-the-fly

The (50) OT_FAULT_RESPONSE command instructs the device on what action to take in response to an overtemperature fault. Upon triggering the overtemperature fault, the device responds per the RS_OT bit in this register, sets the OTF_PROG bit in the STATUS_TEMPERATURE register, and notifies the host via the SMB_ALERT# pin.

Return to Supported PMBus Commands.

Figure 7-47. (50h) OT_FAULT_RESPONSE Register Map

7	6	5	4	3	2	1	0
R	R	RW	RW	RW	R	R	R
1	0	RS_OT			TD_OT		

LEGEND: R/W = Read/Write; R = Read only

Table 7-48. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	1	R	1b	Over-temperature response setting. Read only, and always set to 1b. The device shuts down and disables the output and responds according to the retry setting in bits RS_OT.
6	0	R	0b	Not used and always set to 0b.
5:3	RS_OT	RW	NVM	Over-temperature retry setting. 000b: Latch-off after the fault. The device remains disabled until the fault is cleared. A VCC power cycle or EN toggle can restart the power conversion. 111b: Automatically restart after a 52ms delay, without limitation on the number of restart attempts, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown. Any value other than 000b or 111b will not be accepted and such an attempt shall be considered as invalid data or usupported data (ivd) and the device will respond as described in ivd. Because all 3 bits must be the same, only one bit (bit 5) is stored in EEPROM.
2:0	TD_OT	R	000b	Over-temperature retry time delay setting. These bits are the same as the RS_OT setting. 000b: The device does not delay a restart. This is only supported with restart is deisabled by RS_OT = 000b. The device remains disabled until the fault is cleared. A VCC power cycle or EN toggle can restart the power conversion. 111b: Automatically restart after a 52ms delay, without limitation on the number of restart attempts, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown. This is only supported when RS_OT = 111b.

7.40 (51h) OT_WARN_LIMIT

CMD Address	51h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	LINEAR11
Phased:	Yes
NVM Backup:	EEPROM
Updates:	On-the-fly

The OT_WARN_LIMIT command sets the temperature of the unit at which it indicates an overtemperature warning alarm. The unit of this command is degrees Celsius. This feature utilizes a digital comparator that compares the output of the IC TEMPERATURE telemetry to the warning threshold selected in this register.

Upon triggering the overtemperature fault, the device sets the OTW_PROG bit in the STATUS_TEMPERATURE register and notifies the host via the SMB_ALERT# pin.

Return to Supported PMBus Commands.

Figure 7-48. (4Fh) OT_WARN_LIMIT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
Reserved					OT_WARN_LIMIT		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OT_WARN_LIMIT							

LEGEND: R/W = Read/Write; R = Read only

Table 7-49. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	00010b	Linear format two's complement exponent with a result of 4 degrees Celcius LSB.
10:6	Reserved	R	00000b	Not used and always set to 0.
5:0	OT_FAULT_LIMIT	R/W	NVM (default 10 0010b (125 degrees C)	These bits select the over-temperature warn threshold in the controller die, based on the precision temperature sensor in the telemetry system.

Data Validity

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware.

Attempts to change the read-only bits (OT_WARN_LIMIT[15:6]) will be considered invalid/unsupported data. The device will NACK the unsupported data and the received value will be ignored. The 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the (7Eh) STATUS_CML registers will be set.

Table 7-50. OT_WARN_LIMIT supported values and EEPROM restore values

OT_WARN_LIMIT [5:0]		OTW (deg C)
Greater than or equal to	Less than	
	25d	95
25d	26d	100
26d	27d	105

Table 7-50. OT_WARN_LIMIT supported values and EEPROM restore values (continued)

OT_WARN_LIMIT [5:0]		OTW (deg C)
Greater than or equal to	Less than	
27d	29d	110
29d	30d	115
30d	31d	120
31d	32d	125
32d	64d	130

7.41 (55h) VIN_OV_FAULT_LIMIT

CMD Address	55h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	LINEAR11
Phased:	No
NVM Backup:	EEPROM
Updates:	On-the-fly

The VIN_OV_FAULT_LIMIT command sets the PVIN voltage, in volts, when a VIN_OV_FAULT is declared. The response to a detected VIN_OV_FAULT is latch-off always. VIN_OV_FAULT_LIMIT is typically used to stop switching in the event of excessive input voltage, which can result in over-stress damage to the power FETs due to ringing on the SW node. Upon triggering the PVIN overvoltage fault, the device sets the PVIN_OVF bit in the STATUS_INPUT register and notifies the host via the SMB_ALERT# pin..

Return to Supported PMBus Commands.

Figure 7-49. (55h) VIN_OV_FAULT_LIMIT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					VIN_OV_FAULT_LIMIT		
7	6	5	4	3	2	1	0
R	R	R	R	RW	RW	RW	RW
VIN_OV_FAULT_LIMIT							

LEGEND: R/W = Read/Write; R = Read only

Table 7-51. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	00001b	Linear format two's complement exponent. The exponent is configured automatically through other settings, with a result of 2V LSB.
10:4	Reserved	R	00000b	Not used and always set to 0.
3:0	VIN_OV_FAULT_LIMIT	R/W	NVM (default 1001b (>18.5V)	These bits select the VIN over-voltage threshold.

Data Validity

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware.

Attempts to change the read-only bits (VIN_OV_FAULT_LIMIT[15:4]) will be considered invalid/unsupported data. The device will NACK the unsupported data and the received value will be ignored. The 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the (7Eh) STATUS_CML registers will be set.

Table 7-52. VIN_OV_FAULT_LIMIT supported values and EEPROM restore values

VIN_OV_FAULT_LIMIT [3:0]		PVIN_OVF (deg C)
Greater than or equal to	Less than	
	9d	16.5
9d	16d	18.5

7.42 (60h) TON_DELAY

CMD Address	60h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	LINEAR11
Phased:	No
NVM Backup:	EEPROM
Updates:	On-the-fly

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise.

Return to Supported PMBus Commands.

Figure 7-50. (60h) TON_DELAY Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					TON_DELAY		
7	6	5	4	3	2	1	0
R	R	R	R	R	RW	RW	RW
TON_DELAY							

LEGEND: R/W = Read/Write; R = Read only

Table 7-53. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	11111b	Linear format two's complement exponent. The exponent is not programmable, with a result of 0.5ms LSB.
10:3	Reserved	R	00000b	Not used and always set to 0.
2:0	TON_DELAY	R/W	000b	These bits select the TON_DELAY time. When 000b is selected, a minimum 50us delay is enforced.

Data Validity

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware.

Attempts to change the read-only bits (TON_DELAY[15:3]) will be considered invalid/unsupported data. The device will NACK the unsupported data and the received value will be ignored. The 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the (7Eh) STATUS_CML registers will be set.

Table 7-54. TON_DELAY supported values and EEPROM restore values

TON_DELAY [2:0]		TON_DELAY (ms)
Greater than or equal to	Less than	
	1d	0.05
1d	2d	0.5
2d	3d	1
3d	8d	2

7.43 (61h) TON_RISE

CMD Address	61h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	LINEAR11
NVM Backup:	EEPROM or Pin Detection
Updates:	On-the-fly

The TON_RISE command sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band, which effectively sets the slew rate of the reference DAC during the soft-start period. The soft-start time varies from the TON_RISE selection when VOUT_COMMAND is used for boot up. See section Start-Up and Shutdown for more details.

Return to Supported PMBus Commands.

Figure 7-51. (61h) TON_RISE Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					TON_RISE		
7	6	5	4	3	2	1	0
R	R	RW	RW	RW	RW	RW	RW
TON_RISE							

LEGEND: R/W = Read/Write; R = Read only

Table 7-55. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	11111b	Linear format two's complement exponent. The exponent is not programmable, with a result of 0.5ms LSB.
10:6	Reserved	R	00000b	Not used and always set to 0.
5:0	TON_RISE	R/W	000000b	These bits select the TON_RISE time.

Data Validity

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware.

Attempts to change the read-only bits (TON_RISE[15:6]) will be considered invalid/unsupported data. The device will NACK the unsupported data and the received value will be ignored. The 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the (7Eh) STATUS_CML registers will be set.

Table 7-56. TON_RISE supported values and EEPROM restore values

TON_RISE [5:0]		TON_RISE (ms)
Greater than or equal to	Less than	
	2d	0.5
2d	4d	1
4d	8d	2
8d	16d	4
16d	32d	8
32d	64d	16

7.44 (64h) TOFF_DELAY

CMD Address	64h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	LINEAR11
NVM Backup:	EEPROM
Updates:	On-the-fly

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the device starts the soft-stop operation.

Return to Supported PMBus Commands.

Figure 7-52. (64h) TOFF_DELAY Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					TOFF_DELAY		
7	6	5	4	3	2	1	0
R	R	R	R	R	RW	RW	RW
TOFF_DELAY							

LEGEND: R/W = Read/Write; R = Read only

Table 7-57. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	11111b	Linear format two's complement exponent. The exponent is not programmable, with a result of 0.5ms LSB.
10:3	Reserved	R	00000b	Not used and always set to 0.
2:0	TOFF_DELAY	R/W	000b	These bits select the TOFF_DELAY time.

Data Validity

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware.

Attempts to change the read-only bits (TOFF_DELAY[15:3]) will be considered invalid/unsupported data. The device will NACK the unsupported data and the received value will be ignored. The 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the (7Eh) STATUS_CML registers will be set.

Table 7-58. TOFF_DELAY supported values and EEPROM restore values

TOFF_DELAY [2:0]		TOFF_DELAY (ms)
Greater than or equal to	Less than	
	1d	0
1d	3d	1
3d	4d	1.5
3d	8d	2

7.45 (65h) TOFF_FALL

CMD Address	65h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	LINEAR11
NVM Backup:	EEPROM
Updates:	On-the-fly

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-off delay time until the reference DAC is commanded to 0mV. This command is used to cause the output voltage to decrease at a controlled rate, which effectively sets the slew rate of the reference DAC during the soft-off period. In the implementation of TOFF_FALL, the VREF DAC slew rate is adjusted for each of the supported 32 VBOOT levels to obtain a slew rate to have a soft-stop time close to (but not always exactly equal to) the target value. The selected slew rate for the 0.5ms TOFF_FALL is the same as shown in TON_RISE but with a negative slope. TOFF_FALL is scaled in the same manner as TON_RISE with the different settings.

The VOUT fall time is actually not equal to TOFF_FALL value since the device stops SW switching once the output voltage is discharged to 200mV, and the fall time is more for setting the reference DAC slew rate. See Shutdown for more details.

Return to Supported PMBus Commands.

Figure 7-53. (65h) TOFF_FALL Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					TOFF_FALL		
7	6	5	4	3	2	1	0
R	R	R	R	RW	RW	RW	RW
TOFF_FALL							

LEGEND: R/W = Read/Write; R = Read only

Table 7-59. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	11111b	Linear format two's complement exponent. The exponent is not programmable, with a result of 0.5ms LSB.
10:4	Reserved	R	0000000b	Not used and always set to 0.
3:0	TON_RISE	R/W	0000b	These bits select the TOFF_FALL time.

Data Validity

Every mantissa binary value in the writable bits is writeable and readable. However, the actual divider is set to the nearest supported value. Additionally, that mantissa value restored from EEPROM is fixed for each setting supported in hardware.

Attempts to change the read-only bits (TOFF_FALL[15:4]) will be considered invalid/unsupported data. The device will NACK the unsupported data and the received value will be ignored. The 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the STATUS_CML registers will be set.

Table 7-60. TOFF_FALL supported values and EEPROM restore values

TOFF_FALL [5:0]		TOFF_FALL (ms)
Greater than or equal to	Less than	
	2d	0.5

Table 7-60. TOFF_FALL supported values and EEPROM restore values (continued)

TOFF_FALL [5:0]		TOFF_FALL (ms)
Greater than or equal to	Less than	
2d	4d	1
4d	8d	2
8d	16d	4

7.46 (78h) STATUS_BYTE

CMD Address:	78h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	No
Updates:	On-the-fly

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults, such as overvoltage, overcurrent, overtemperature, and so forth. The supported STATUS_BYTE message content is described in the following table. The STATUS_BYTE is equal the low byte of STATUS_WORD. The conditions in the STATUS_BYTE are summary information only. They are asserted to inform the host as to which other STATUS registers should be checked in the event of a fault. Setting and clearing of these bits must be done in the individual status registers. For example, clearing VOUT_OVF in STATUS_VOUT also clears VOUT_OVF in STATUS_BYTE.

Attempts to write STATUS_BYTE will be considered invalid/unsupported data and cause the device to respond by flagging the appropriate status bits and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Secondary devices will set all bits to 0b.

Return to Supported PMBus Commands.

Figure 7-54. (78h) STATUS_BYTE Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
0	OFF	OVF	OCF	0	OTFW	CML	OTH

LEGEND: R/W = Read/Write; R = Read only

Table 7-61. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	Not supported	R	0b	Not supported and always set to 0b.
6	OFF	R	1b	LIVE (unlatched) status bit. 0b: The the device is enabled and converting power. 1b: The device is NOT converting power for any reason including simply not being enabled.
5	OVF	R	0b	An output overvoltage fault has occurred. This bit directly reflect the state of (7Ah) STATUS_VOUT[7] – OVF. If the user wants this fault sourced to be masked and not trigger SMBALERT, they must do it by masking (7Ah) STATUS_VOUT[7]. Note that secondary devices will set bit OVF to 0. 0b: An output overvoltage fault has NOT occurred. 1b: An output overvoltage fault has occurred.
4	OCF	R	0b	An output overcurrent fault has occurred. Per the PMBus spec, this bit can be set by either (7Bh) STATUS_IOUT[7] OCF or (7Bh) STATUS_IOUT[6] OCUV. (7Bh) STATUS_IOUT[6] OCUV is not a source of SMBALERT, so, if the user wants this fault source to be masked and not trigger SMBALERT, they must do so by masking the source bit in (7Bh) STATUS_IOUT 0b: An output overcurrent fault has NOT occurred. 1b: An output overcurrent fault has occurred.
3	Not supported	R	0b	Not supported and always set to 0b.

Table 7-61. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
2	OTFW	R	0b	OTF or OTW input has been asserted by the programmable temperature limit. 0b: A temperature fault or warning has NOT occurred. 1b: A temperature fault or warning has occurred, the host should check (7Dh) STATUS_TEMPERATURE for more information.
1	CML	R	0b	Communications, memory or logic fault has occurred in (7Eh) STATUS_CML. 0b: A communication, memory, logic fault has NOT occurred. 1b: A communication, memory, logic fault has occurred, the host should check (7Eh) STATUS_CML for more information.
0	OTH	R	0b	This bit is used to flag faults not covered with the other bit faults in STATUS_BYTE. In this case, VOUT_MAX_MIN_W, OTF_BG , LOW_VIN, UVF, OCW, OVW, UVW, PVIN_OVF, or FRST_2_ALRT. 0b: A fault other than those listed above has NOT occurred. 1b: A fault other than those listed above has occurred. The host should check (79h) STATUS_WORD for more information.

7.47 (79h) STATUS_WORD

CMD Address:	79h
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
NVM Back-up:	No
Updates:	On-the-fly

The STATUS_WORD command returns two bytes of information with a summary of the most critical faults, such as overvoltage, overcurrent, overtemperature, and so forth. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE. The supported STATUS_WORD message content is described in the following table. The conditions in the STATUS_BYTE are summary information only.

All of these bits can trigger SMB_ALERT# and have a corresponding bit in SMBALERT_MASK.

Attempts to write STATUS_WORD will be considered invalid/unsupported data and cause the device to respond by flagging the appropriate status bits and notifying the host according to the PMBus 1.3.1 Part II specification section 10.9.3.

Secondary devices will set bits PGOOD_Z and OVF to 0b.

Return to Supported PMBus Commands.

Figure 7-55. (79h) STATUS_WORD Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
VFW	OCFW	INPUT	MFR	PGOOD_Z	0	OTHER	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
STATUS_BYTE							

LEGEND: R/W = Read/Write; R = Read only

Table 7-62. Register Field Descriptions

Bit	Field	Access	Reset	Description
15	VFW	R	0b	Output Voltage Fault or Warning. A fault or warning in (7Ah) STATUS_VOUT is present (OVF + OVW + UVF + UVW + VOUT_MAX_Warning). 0b: An output voltage related fault has NOT occurred. 1b: An output voltage fault has occurred. The host should check STATUS_VOUT for more information.
14	OCFW	R	0b	Output Current Fault or Warning. A fault or warning in (7Bh) STATUS_IOUT is present (OCF + OCW). 0b: An output current related fault has NOT occurred. 1b: An output current fault has occurred. The host should check STATUS_IOUT for more information
13	INPUT	R	0b	INPUT fault or warning in (7Ch) STATUS_INPUT is present. Depends on LOW_VIN that may come up as a 1, if initially VIN<VIN_ON. 0b: An input related fault has NOT occurred. 1b: An input fault has occurred. The host should check (7Ch) STATUS_INPUT for more information.

Table 7-62. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
12	MFR	R	0b	Manufacturer specific fault/warning condition. A fault or warning in STATUS_MFR_SPECIFIC is present, with the exception of bit 7 DCM. 0b: A Manufacturer-defined fault has NOT occurred. 1b: A Manufacturer-defined fault has occurred. The host should check STATUS_MFR_SPECIFIC for more information.
11	PGOOD_Z	R	0b	Power Good Inverted. The Power Not Good is used to flag when the converter output voltage drops below the FAULT_LIMIT as defined by VOUT_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT. The signal is unlatched and always represents the current state of the device. 0b: The output voltage is within the regulation window. PG pin is floating. 1b: The output voltage is NOT within the regulation window. PG pin is pulled low. Note: Per PMBus spec v1.4 10.2.5.3, PGOOD_Z cannot be cleared by a PMBus write. It always reflects the current state of the device. Please reference the SMBALERT_MASK command for specific details regarding access to the PGOOD_Z mask bit. In secondary devices PGOOD_Z will always be set to 0 and the primary device will communicate the POWER_GOOD status of the stack.
10	Not Supported	R	0b	Not supported and always set to 0.
9	OTHER	R	0b	STATUS_OTHER fault/warning condition. A fault or warning (FRST_2_ALRT) in STATUS_OTHER is present. 0b: A STATUS_OTHER fault or warning has not occured. 1b: A STATUS_OTHER fault or warning has occured.
8	Not Supported	R	0b	Not supported and always set to 0.
7:0	STATUS_BYTE	R	00h	Always equal to the STATUS_BYTE value.

7.48 (7Ah) STATUS_VOUT

CMD Address:	7Ah
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte), read + writable clear
NVM Back-up:	Yes
Updates:	On-the-fly

The STATUS_VOUT command returns one data byte with contents regarding output voltage warnings and faults as follows. None of these bits is affected by the state of SMBALERT_MASK. However, if the corresponding fault/warning disable bits in the FAULT_CTRL register is set, then the corresponding status bits will also be blocked in addition to blocking the response from that fault. The status bits remain latched after the fault condition is no longer present (as conveyed by digital input fault/warning signal). They can be cleared by power-cycle, issuing the CLEAR_FAULTS command, or by toggling the on-off mechanism of the rail (as configured in the (02h) ON_OFF_CONFIG register.

All supported bits may be cleared either by CLEAR_FAULTS, turning on the output through the mechanism programmed into ON_OFF_CONFIG, or individually by writing 1b to the STATUS_VOUT register in their position, per the PMBus 1.3.1 Part II specification section 10.2.3.

Return to Supported PMBus Commands.

Figure 7-56. (7Ah) STATUS_VOUT Register Map

7	6	5	4	3	2	1	0
RW1C	RW1C	RW1C	RW1C	RW1C	R	R	R
OVF	OVW	UVW	UVF	VO_MAX_MIN_W	0	0	0

LEGEND: R/W1C = Read/Write 1 to clear; R = Read only

Table 7-63. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	OVF	RW1C	0b	0b: Latched flag indicating an output overvoltage fault has NOT occured. 1b: Latched flag indicating an output overvoltage fault has occured.
6	OVW	RW1C	0b	0b: Latched flag indicating an output overvoltage warning has NOT occured. 1b: Latched flag indicating an output overvoltage warning has occured. Note: OVW status bit will set automatically in the event of an OVF after soft start. If OVF is tripped before completion of soft start (fixed OVF), then the OVW status is not set.
5	UVW	RW1C	0b	0b: Latched flag indicating an output undervoltage fault has NOT occured. 1b: Latched flag indicating an output undervoltage fault has occured. Note: UVW status bit will also set automatically in the event of an UVF.
4	UVF	RW1C	0b	0b: Latched flag indicating an output undervoltage warning has NOT occured. 1b: Latched flag indicating an output undervoltage warning has occured.
3	VOUT_MAX_MIN_W	RW1C	0b	0b: Latched flag indicating a VOUT_MAX_MIN warning as described in VOUT_COMMAND has NOT occurred. 1b: Latched flag indicating a VOUT_MAX_MIN warning as described in VOUT_COMMAND has occurred.
2:0	Not supported	R	000b	Not supported and always set to 0.

7.49 (7Bh) STATUS_IOUT

CMD Address:	7Bh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	Yes
Updates:	On-the-fly

The STATUS_IOUT command returns one data byte with contents as follows. None of these bits is affected by the state of SMBALERT_MASK. However, if the corresponding fault/warning disable bits in the FAULT_CTRL register is set, then the corresponding status bits will also be blocked in addition to blocking the response from that fault. All supported bits may be cleared either by CLEAR_FAULTS, turning on the output through the mechanism programmed into ON_OFF_CONFIG, or individually by writing 1b to the STATUS_IOUT register in their position, per the PMBus 1.3.1 Part II specification section 10.2.3.

OCF[7] and OCW[5] share a single NVM bit for changing the shared default NVM masking capability. Thus, overcurrent fault and warning SMBALERT masking default can be set and stored to NVM by the user; however, since they share a single NVM bit, the default ability or inability (masking) to set SMBALERT is always common/same after a restore from NVM or power-cycle. In contrast, dynamically setting the two smb_alert mask bits different/independently is allowed and is the only way the two mask settings can be different. Upon power-cycle/NVM-restore the two SMB_ALERT mask settings will revert to the same setting. The initial default is that both will trigger SMBALERT (as noted in the SMBALERT_MASK command default definition). The actual NVM bit is associated with OCW [5] – so, the value in this bit position's SMBALERT_MASK bit is what is stored/restored to/from NVM.

Return to Supported PMBus Commands.

Figure 7-57. (7Bh) STATUS_IOUT Register Map

7	6	5	4	3	2	1	0
RW1C	R	RW1C	RW1C	R	R	R	R
OCF	OCUV	OCW	UCF	0	0	0	0

LEGEND: R/W1C = Read/Write 1 to clear; R = Read only

Table 7-64. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	OCF Supported	RW1C	0b	This latched bit is set to 1 upon detection of an IOUT OCF event as configured by the IOUT_OC_FAULT_LIMIT. Not supported and always set to 0.
6	OCUV	R	0b	VOUT UV caused by OCL. 0b: Latched flag indicating the IOUT_OC_LV_FAULT has NOT occurred. 1b: Latched flag indicating IOUT_OC_LV_FAULT has occurred. This bit is set when the output voltage is below the IOUT_OC_LV_FAULT_LIMIT AND the output current exceeds the IOUT_OC_FAULT_LIMIT. This bit cannot be cleared by writing to 1b to it. It is cleared by writing 1b to VOUT_UVF in STATUS_VOUT.
5	OCW	RW1C	0b	0b: Latched flag indicating an output overcurrent warning has NOT occured. 1b: Latched flag indicating an output overcurrent warning has occured.
4	UCF	RW1C	0b	This latched bit is set to 1 upon detection of IOUT UC fault. 0b: Latched flag indicating an output undercurrent fault has NOT occured. 1b: Latched flag indicating an output undercurrent fault has occured.
3:0	Not supported	R	0000b	Not supported and always set to 0.

7.50 (7Ch) STATUS_INPUT

CMD Address:	7Ch
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	Yes
Updates:	On-the-fly

The STATUS_INPUT command returns one data byte with contents as follows. The status bits remain latched after the fault condition is no longer present (as conveyed by digital input fault/warning signal). All supported bits may be cleared either by CLEAR_FAULTS, turning on the output through the mechanism programmed into ON_OFF_CONFIG, or individually by writing 1b to the STATUS_INPUT register in their position, per the PMBus 1.3.1 Part II specification section 10.2.3.

None of these bits is affected by the state of SMBALERT_MASK. However, if the corresponding fault/warning disable bits in the FAULT_CTRL register is set, then the corresponding status bits will also be blocked in addition to blocking the response from that fault.

Return to Supported PMBus Commands.

Figure 7-58. (7Ch) STATUS_INPUT Register Map

7	6	5	4	3	2	1	0
RW1C	R	R	R	RW1C	R	R	R
PVIN_OVF	0	0	0	LOW_VIN	0	0	0

LEGEND: R/W1C = Read/Write 1 to clear; R = Read only

Table 7-65. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	PVIN_OVF	R/W1C	0b	0b: Latched flag indicating an input overvoltage fault has NOT occured. 1b: Latched flag indicating an input overvoltage fault has occured.
6:4	Not Supported	R	000b	Not supported and always set to 0.
3	LOW_VIN	R/W1C	0b	This bit indicates the status of the PVIN voltage relative to VIN_ON and VIN_OFF. During the initial power up, LOW_VIN is not latched and does not assert SMB_ALERT#. Once PVIN exceeds VIN_ON for the first time, any subsequent PVIN < VIN_OFF events will be latched and assert SMB_ALERT#. 0b: PVIN is greater than VIN_ON. 1b: PVIN is less than VIN_OFF.
2:0	Not Supported	R	000b	Not supported and always set to 0.

7.51 (7Dh) STATUS_TEMPERATURE

CMD Address:	7Dh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	Yes
Updates:	On-the-fly

The STATUS_TEMPERATURE command returns one data byte with contents as follows. All supported bits may be cleared either by CLEAR_FAULTS, turning on the output through the mechanism programmed into ON_OFF_CONFIG, or individually by writing 1b to the STATUS_TEMPERATURE register in their position, per the PMBus 1.3.1 Part II specification section 10.2.3.

None of these bits is affected by the state of SMBALERT_MASK. However, if the corresponding fault/warning disable bits in the FAULT_CTRL register is set, then the corresponding status bits will also be blocked in addition to blocking the response from that fault.

Return to Supported PMBus Commands.

Figure 7-59. (7Dh) STATUS_TEMPERATURE Register Map

7	6	5	4	3	2	1	0
R/W1C	R/W1C	R	R	R	R	R	R
OTF_PROG	OTW_PROG	0	0	0	0	0	0

LEGEND: R/W1C = Read/Write 1 to clear; R = Read only

Table 7-66. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	OTF_PROG	R/W1C	0b	Programmable over-temperature fault. 0b: Latched flag indicating an overtemperature fault has NOT occured. 1b: Latched flag indicating an overtemperature fault has occured.
6	OTW_PROG	R/W1C	0b	Programmable over-temperature warning. 0b: Latched flag indicating an overtemperature warning has NOT occured. 1b: Latched flag indicating an overtemperature warning has occured.
5:0	Not supported	R	00h	Not supported and always set to 0.

7.52 (7Eh) STATUS_CML

CMD Address:	7Eh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	Yes
Updates:	On-the-fly

The STATUS_CML command returns one data byte with contents relating to communications, logic, and memory as follows. All supported bits may be cleared either by (03h) CLEAR_FAULTS, turning on the output through the mechanism programmed into (02h) ON_OFF_CONFIG, or individually by writing 1b to the STATUS_CML register in their position, per the PMBus 1.3.1 Part II specification section 10.2.3.

Return to Supported PMBus® Commands.

Figure 7-60. (7Eh) STATUS_CML Register Map

7	6	5	4	3	2	1	0
R/W1C	R/W1C	R/W1C	R/W1C	R	R	R/W1C	R
IVC	IVD	PEC	MEM	0	0	OTHER	0

LEGEND: R/W1C = Read/Write 1 to clear; R = Read only

Table 7-67. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	IVC	R/W1C	0b	0b: Latched flag indicating an invalid or unsupported command was NOT received. 1b: Latched flag indicating an invalid or unsupported command was received.
6	IVD	R/W1C	0b	0b: Latched flag indicating an invalid or unsupported data was NOT received. 1b: Latched flag indicating an invalid or unsupported data was received.
5	PEC	R/W1C	0b	0b: Latched flag indicating NO packet error check has failed. 1b: Latched flag indicating a packet error check has failed.
4	MEM	R/W1C	0b	0b: Latched flag indicating NO memory error was detected. 1b: Latched flag indicating a memory error was detected. The source of the fault could be one of the following sources internally: • Failure parity check during/after STORE_USER_ALL • During reset RESTORE (i.e., EEPROM restore at boot-up), either a mismatch between the EEPROM contents and the register contents; OR a failure to pass parity checks • When the user issues a RESTORE_USER_ALL command, a failure to pass parity checks • Failure during the NVM programming sequence. This bit cannot be cleared by any clearing mechanism until the underlying issue is resolved and the memory is updated.
3:2	Not supported	R	00b	Not supported and always set to 0.
1	OTHER	R/W1C	0b	0b: Latched flag indicating NO communication error detected. 1b: Latched flag indicating communication error detected.
0	Not supported	R	0b	Not supported and always set to 0.

The corresponding bit (78h) STATUS_BYTE is an OR'ing of the supported bits in this command. When any of the events in this command occurs and the bit representative of the events is set, the corresponding bit in (78h) STATUS_BYTE is updated. Likewise, if this byte is individually cleared (for example, by a write of 1b to a latched condition), it will clear the corresponding bit in (78h) STATUS_BYTE.

7.53 (7Fh) STATUS_OTHER

CMD Address:	7Eh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	No
Updates:	On-the-fly

The STATUS_OTHER command returns one data byte containing PMBus First to Alert status. First to Alert does not assert SMB_ALERT on its own. It is informational only – regarding the state of SMB_ALERT if/when the device asserts SMB_ALERT by means of any other fault condition.

All supported bits may be cleared either by CLEAR_FAULTS, turning on the output through the mechanism programmed into ON_OFF_CONFIG, or individually by writing 1b to the STATUS_OTHER register in their position, per the PMBus 1.3.1 Part II specification section 10.2.3.

Return to Supported PMBus Commands.

Figure 7-61. (7Fh) STATUS_OTHER Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	RW1C
0	0	0	0	0	0	0	FRST_2_ALRT

LEGEND: R/W1C = Read/Write 1 to clear; R = Read only

Table 7-68. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:1	Not supported	R	0000000b	Not supported and always set to 0.
0	FRST_2_ALRT	RW1C	0b	0b: Latched flag indicating that the device has not asserted SMBALERT or SMBALERT was asserted low before this device asserted SMBALERT. 1b: Latched flag indicating that the device has asserted SMBALERT and SMBALERT was not asserted low before this device asserted SMBALERT.

The corresponding bit STATUS_BYTE is an OR'ing of the supported bits in this command. When any of the events in this command occurs and the bit representative of the events is set, the corresponding bit in STATUS_BYTE is updated. Likewise, if this byte is individually cleared (for example, by a write of 1b to a latched condition), it will clear the corresponding bit in STATUS_BYTE.

7.54 (80h) STATUS_MFR_SPECIFIC

CMD Address	80h
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	Yes
Updates:	On-the-fly

The STATUS_MFR_SPECIFIC command returns one data byte with contents regarding manufacturer defined status as follows. All supported bits may be cleared either by (03h) CLEAR_FAULTS, turning on the output through the mechanism programmed into (02h) ON_OFF_CONFIG, or individually by writing 1b to the STATUS_MFR_SPECIFIC register in their position, per the PMBus 1.3.1 Part II specification section 10.2.3.

None of these bits is affected by the state of SMBALERT_MASK. However, if the corresponding fault/warning disable bits in the FAULT_CTRL register is set, then the corresponding status bits will also be blocked in addition to blocking the response from that fault..

Return to Supported PMBus Commands.

Figure 7-62. (80h) STATUS_MFR_SPECIFIC Register Map

7	6	5	4	3	2	1	0
R	R/W1C	R/W1C	R/W1C	R	R	R/W1C	R/W1C
DCM	OTF_BG	PS_FLT	PS_COMM_WRN	0	0	PS_OT	PS_UV

LEGEND: R/W1C = Read/Write 1 to clear; R = Read only

Table 7-69. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	DCM	R	0b	LIVE (unlatched) status bit. This bit is set upon detection of DCM operation. This bit does not trigger SMB_ALERT# and does not assert the MFR bit in STATUS_WORD or the OTH bit in STATUS_BYTE. 0b: The device is NOT operating in DCM. 1b: The device is operating in DCM.
6	OTF_BG	R/W1C	0b	0b: Latched flag indicating the controller fixed thermal shutdown has NOT occurred. 1b: Latched flag indicating the controller fixed thermal shutdown has occurred.
5	PS_FLT	R/W1C	0b	0b: Latched flag indicating a power-stage fault has NOT occured. 1b: Latched flag indicating a power-stage fault has occured. The faults which can set this bit are: 1. VDRV voltage at the power stage is insufficient (VDRV_UV). 2. Power-stage temperature exceeds the power-stage's fixed thermal shutdown (PS_OT). 3. PVIN voltage is less than the fixed $PVIN_{UVLO}$ threshold.
4	PS_COMM_WRN	R/W1C	0b	0b: Latched flag indicating a power-stage communication error has NOT occured. 1b: Latched flag indicating a power-stage communication error has occured.
3:2	Not supported	R	00b	Not supported and always set to 0.
1	PS_OT	R/W1C	0b	0b: Latched flag indicating the power-stage fixed thermal shutdown has NOT occurred. 1b: Latched flag indicating the power-stage fixed thermal shutdown has occurred.
0	PS_UV	R/W1C	0b	0b: Live flag indicating a power-stage undervoltage fault has NOT occurred. 1b: Live flag indicating a power-stage undervoltage fault has occurred.

7.55 (88h) READ_VIN

CMD Address	88h
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	LINEAR11
Phased:	Yes
NVM Backup:	No
Update Rate:	190µs
Supported Range:	4V – 20V

The READ_VIN command returns input voltage in Volts. READ_VIN is clamped to 4V. When the sensed voltage at PVIN is less than 4V, READ_VIN will report 4.0V See Telemetry for more details.

Return to Supported PMBus Commands.

Figure 7-63. (88h) READ_VIN Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					READ_VIN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_VIN							

LEGEND: R/W = Read/Write; R = Read only

Table 7-70. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	11011b	LINEAR11 format two's complement exponent. Fixed exponent of 7 resulting in 0.03125V LSB.
10:0	READ_VIN	R/W	000 0000 0000b	Input voltage telemetry data. Clamped at 128d (4V) minimum and 640d (20V) maximum.

7.56 (8Bh) READ_VOUT

CMD Address	8Bh
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	LINEAR16, Absolute per Section 7.14
NVM Backup:	No
Update Rate:	190 µs
Supported Range	VOUT 1.953mV step: up to 6V

The READ_VOUT command returns the actual, measured output voltage (VOSNS−GOSNS) in Volts. See Telemetry for more details. The format and LSB is set by (20h) VOUT_MODE.

Return to Supported PMBus Commands.

Figure 7-64. (8Bh) READ_VOUT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	READ_VOUT				
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_VOUT							

LEGEND: R/W = Read/Write; R = Read only

Table 7-71. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:13	0	R	000b	Not supported and always set to 0.
12:0	READ_VOUT	R/W	000 0000 0000b	Output voltage telemetry data. Clamped at 0V minimum.

The maximum valid value of READ_VOUT when an external feedback resistor is selected is shown in the table below. Any value above the maximum indicates an incorrect VOUT_SCALE_MONITOR setting.

Table 7-72. READ_VOUT supported values with external feedback resistor divider

VOUT_SCALE_MONITOR [3:0]		Max Valid READ_VOUT (V)
Greater than or equal to	Less than	
	2d	6.0
2d	4d	3.0
3.04d	8d	1.5
8d	16d	0.75

7.57 (8Ch) READ_IOUT

CMD Address	8Ch
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	LINEAR11
Phased:	YES
NVM Backup:	No
Update Rate:	70 µs

The READ_IOUT command returns the measured SW output current in Amperes. See Telemetry for more details.

Return to Supported PMBus Commands.

Figure 7-65. (8Ch) READ_IOUT Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					READ_IOUT		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_IOUT							

LEGEND: R/W = Read/Write; R = Read only

Table 7-73. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	11100b	Linear format two's complement exponent. Fixed exponent of -4 resulting in 0.0625A LSB for single stack and variable for multi-stack
10:0	READ_IOUT	R	Current Status	Output current reading. Max current capability of CSA telemetry is 57.125A See Telemetry for more details.

Response to P2_PLUS_READ Commands

When the PMBus host attempts to execute a P2+ read on READ_IOUT **with the PHASE data in the command set to FFh**, only the primary device will respond to P2+ read commands with incoming data for PHASE=FFh. The primary device multiplies the READ_IOUT level by the STACK_NUMBER and reports the product back on the PMBus. For example, if the READ_IOUT is 24A for the primary phase in a 3-phase rail, then a P2+ read with PHASE=FFh will yield 24 x 3 = 72A as the read-back value.

7.58 (8Dh) READ_TEMPERATURE_1

CMD Address	8Dh
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	LINEAR11
Phased:	Yes
NVM Backup:	No
Update Rate:	190 µs
Supported Range:	–40°C to 150°C

The READ_TEMP1 command returns the Controller die temperature in degrees Celsius. See Telemetry for more details.

Return to Supported PMBus Commands.

Figure 7-66. (8Dh) READ_TEMPERATURE_1 Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
EXPONENT					READ_TEMP1		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_TEMP1							

LEGEND: R/W = Read/Write; R = Read only

Table 7-74. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:11	EXPONENT	R	1 1110b	LINEAR11 format two's complement exponent. Fixed exponent of -2 resulting in 0.25 degrees Celsius LSB.
10:0	READ_TEMP1	R/W	000 0000 0000b	Temperature of the controller die.

7.59 (98h) PMBUS_REVISION

CMD Address	98h
Write Transaction:	N/A
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Backup:	No

The PMBUS_REVISION command returns the revision of the PMBus.

Return to Supported PMBus Commands.

Figure 7-67. (98h) PMBUS_REVISION Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
PMBUS_REVISION							

LEGEND: R/W = Read/Write; R = Read only

Table 7-75. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:0	PMBUS_REVISION	R	0101 0101b	PMBus revision, compliant to revision 1.5 of the PMBus specification (Part I and II).

7.60 (99h) MFR_ID

CMD Address	99h
Write Transaction:	N/A
Read Transaction:	Block Read
Format:	Unsigned Binary (2 bytes)
NVM Backup:	No
Update Rate:	95 µs
Supported Range:	0 W to 510 W (if PIN_OPW = 510 W)

This Read-only Block Read command returns a single word (16 bits) with the manufacturer's ID (name, abbreviation or symbol that identifies the unit's manufacturer). The BYTE_COUNT field in the Block Read command will be 2 (indicating 2 bytes will follow).

Return to Supported PMBus Commands.

Figure 7-68. (2Bh) VOUT_MIN Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
4				9			
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
5				4			

Note

54 is ASCII for T and 49 is ASCII for I

LEGEND: R/W = Read/Write; R = Read only

7.61 (9Ah) MFR_MODEL

CMD Address	9Ah
Write Transaction:	N/A
Read Transaction:	Block Read
Format:	Unsigned Binary (4 bytes)
NVM Backup:	No

This Read-only Block Read command returns 4 bytes (32 bits) with the manufacturer's model number. The BYTE_COUNT field in the Block Read command will be 4 (indicating 4 bytes will follow).

Return to Supported PMBus Commands.

Figure 7-69. (9Ah) MFR_MODEL Register Map

31	30	29	28	27	26	25	24
R	R	R	R	R	R	R	R
Part Number Extension							
23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R
Part Number Fifth Digit				Part Number Sixth Digit			
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
Part Number Third Digit				Part Number Fourth Digit			
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
Part Number First Digit				Part Number Second Digit			

LEGEND: R/W = Read/Write; R = Read only

7.62 (9Bh) MFR_REVISION

CMD Address	9Bh
Write Transaction:	Block Write
Read Transaction:	Block Read
Format:	Unsigned Binary (1 byte)
NVM Backup:	Yes

This single byte Block command is used to either set or read the manufacturer's revision number. It is writeable and includes NVM backup.

Return to Supported PMBus Commands.

Figure 7-70. (9Bh) MFR_REVISION

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
MFR_REVISION							

LEGEND: R/W = Read/Write; R = Read only

7.63 (ADh) IC_DEVICE_ID

CMD Address	ADh
Write Transaction:	N/A
Read Transaction:	Block Read
Format:	Unsigned Binary (6 bytes)
NVM Backup:	EEPROM
Updates:	On-the-fly

The block read-only IC_DEVICE_ID command is used to read the type or part number of an IC embedded within a PMBus that is used for the PMBus interface. IC_DEVICE_ID uses 6-byte block format. The first two byte shall be 0x5449h for “TI” in ASCII text format. The Third through Fifth byte shall be a direct readable Hex Part Number representing the 6-digit part-number. The Sixth byte shall be a Part Number Extention code

Return to Supported PMBus Commands.

Figure 7-71. (ADh) IC_DEVICE_ID Register Map

47	46	45	44	43	42	41	40
R	R	R	R	R	R	R	R
Part Number Extension							
39	38	37	36	35	34	33	32
R	R	R	R	R	R	R	R
Part Number Fifth Digit				Part Number Sixth Digit			
31	30	29	28	27	26	25	24
R	R	R	R	R	R	R	R
Part Number Third Digit				Part Number Fourth Digit			
23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R
Part Number First Digit				Part Number Second Digit			
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
4				9			
ASCII for "I"= 49h							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
5				4			
ASCII for "T"= 54h							

LEGEND: R/W = Read/Write; R = Read only

7.64 (AEh) IC_DEVICE_REV

CMD Address	AEh
Write Transaction:	N/A
Read Transaction:	Read Block
Format:	Unsigned Binary (1 byte)
NVM Backup:	No

The block read-only IC_DEVICE_REV command returns a single byte with the unique Device revision identifier. The DEVICE_REV starts at 0 with the first silicon and is incremented with each subsequent silicon revision. The BYTE_COUNT field in the Block Read command will be 01h (indicating 1 byte will follow).

Return to Supported PMBus Commands.

Figure 7-72. (AEh) IC_DEV)CE_REVC Register Map

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
Reserved	PS_IC			DEVICE_REVISION			

LEGEND: R/W = Read/Write; R = Read only

Table 7-76. Register Field Descriptions

Bit	Field	Access	Reset	Description
7	Reserved	R	0b	Not used and always set to 0.
6:4	PS_IC	R	111b	Power stage verision. These bits are mapped from the powerstage die-id.
3:0	DEVICE_REVISION	R	0	Device Revision.

7.65 (D1h) SYS_CFG_USER1

CMD Address	D1h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
NVM Back-up:	EEPROM
Updates:	On-the-fly

This command contains miscellaneious bits for system configuration.

Return to Supported PMBus Commands.

Figure 7-73. Register Map

15	14	13	12	11	10	9	8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
FCCM	0		EN_SS_DCM	PGD_DEL		SEL_UCF	
7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PEC_REQ	0	0	EXT_DIV	SEL_HI_VORST_TH	EN_VORST	SEL_FIX_OVF	EN_FIX_OVF

LEGEND: R/W = Read/Write; R = Read only

Table 7-77. Register Field Descriptions

Bit	Field	Access	Reset	Description
15	FCCM	R/W	NVM	Forced CCM operation. 1b: Forces continuous conduction in the switching converter. 0b: DCM operation is enabled and automatically entered/exited based on zero-crossing detection of the LFET sensed current. The bit is updated when disabled. PMBus writes are always accepted and the data is updated; however, in order for this bit to take effect, the rail must be disabled. When in stacked configuration, FCCM is always set to 1b.
14:13	0	R/W	00b	Not supported and always 0.
12	EN__SS_DCM	R/W	NVM	Enable DCM during SS (soft start). 1b: DCM operation is enabled during soft start. This will override the setting in the FCCM bit during soft start. 0b: DCM operation is disabled during soft start.
11:10	PGD_DEL	R/W	NVM	PG delay. These bits indicate the rising edge deglitch time from SS_DONE going high to PGOOD pin going high. As a result, this deglitch time is included only once per startup of the rail. PMBus writes are always accepted and the data is updated; however, in order for this bit to take effect, the rail must be disabled. 00b: 0.0015ms delay. 01b: 0.5ms delay. 10b: 1ms delay. 11b: 2ms delay.
9:8	SEL_UCF	R/W	NVM	These bits select the UCF threshold.
7	PEC_REQ	R/W	NVM	Require Packet Error Check (PEC) on all transactions. If not primary, this bit will be ignored. 0b: Respond to PEC per normal. Accept commands when no PEC is provided. Process PEC when additional PEC byte provided 1b: Reject any command transaction received without PEC. Respond as though an invalid PEC byte had been received.
6:5	0	R/W	00b	Not supported and always 0.

Table 7-77. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
4	EXT_DIV	R/W	NVM	Select external divider resistor. This bit is used to provide status on the selection of an external divider resistor versus an internal divider. This bit is set via pin-strap. Writes are accepted but are not stored. Reads will return pin-strapped value.
3	SEL_HI_VORST_TH	R/W	NVM	Select high threshold for VORST. 0b: VORST threshold is VH=0.6V, VL=0.5V 1b:VORST threshold is VH=1.1V, VL=0.9V
2	EN_VORST	R/W	NVM	Enable VOUT reset (VORST). 0b: Pulling down on (PMB_ADDR/VORST) has no effect on regulated output voltage; Vout remains unchanged 1b:Pulling down on (PMB_ADDR/VORST) has the effect of changing the regulated output voltage to VBOOT at a slew-rate specified by (27h) VOUT_TRANSITION_RATE. The transition to VBOOT will occur if the VORST# pin is low at the time of setting EN_VORST to 1.
1	SEL_FIX_OVF	R/W	NVM	Fixed OVF threshold selection. 0b: OVF threhold is 0.75V when (29h) VOUT_SCALE_LOOP mantissa is 8 0b: OVF threhold is 1.5V when (29h) VOUT_SCALE_LOOP mantissa is 4 0b: OVF threhold is 3.0V when (29h) VOUT_SCALE_LOOP mantissa is 2 0b: OVF threhold is 4.8V when (29h) VOUT_SCALE_LOOP mantissa is 1 1b: OVF threhold is 0.9V when (29h) VOUT_SCALE_LOOP mantissa is 8 1b: OVF threhold is 1.8V when (29h) VOUT_SCALE_LOOP mantissa is 4 1b: OVF threhold is 3.6V when (29h) VOUT_SCALE_LOOP mantissa is 2 1b: OVF threhold is 6.0V when (29h) VOUT_SCALE_LOOP mantissa is 1
0	EN_FIX_OVF	R/W	NVM	Fixed OV fault. 0b: Fixed OVF enabled. 1b: Fixed OVF disabled.

7.66 (D3h) PMBUS_ADDR

CMD Address	D3h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
NVM Back-up:	EEPROM
Updates:	On-the-fly. (15h) STORE_USER_ALL then VCC reset required for device to respond to a new PMBus address.

This command contains bits for setting the PMBus address for the device and other configuration settings for the PMB_ADDR pin. Storing changes to this command value to NVM will change the PMBus Address of the device on future power-on cycles even if the PMB_ADDR bit in (D8h) PIN_DETECT_OVERRIDE is set to use Programming PMB_ADDR pin detection. All pin programmable addresses will be shifted by the change applied to the current pin-programmed PMBus addesss.

For example, if a device powers on with PMB_ADDR/VORST# connected to AGND with >1.78kΩ, selecting PMBus Address 11h and PMBUS_ADDR is changed to 15h and then stored to NVM, all PMBUS_ADDR values in Programming PMB_ADDR will be shifted by the same +04h shift in address. If the resistor from PMB_ADDR/VORST# to AGND is not changed, the part will operate at the programmed PMBus address, even if (D8h) PIN_DETECT_OVERRIDE was not changed to select PMB_ADDR based on NVM programming.

Care must be taken when making changes to this value and leaving pin detection of PMBus Address enabled as it can result in selecting reserved PMBus addresses that my conflict with the operation of the device.

Care must also be taken when setting this command value above 70h. If the updated PMBus Address would push the highest pin programmable PMBus address above address 7Fh, the pin programmable addresses will be clamped to limit the pin programmable address range to 70h - 7Fh.

Return to Supported PMBus Commands.

Figure 7-74. (D2h) MFR_SPECIFIC_D2 (PMBUS_ADDR) Register Map

15	14	13	12	11	10	9	8
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reserved	COMMON_ADDR						
7	6	5	4	3	2	1	0
R	R	R	R/W	R	R	R	R/W
Reserved	UNIQUE_ADDR						

LEGEND: R/W = Read/Write; R = Read only

Table 7-78. Register Field Descriptions

Bit	Field	Access	Reset	Description
15	Reserved	R	0b	Not used and always set to 0.
14:8	COMMON_ADDR	R/W	NVM	The primary PMBus address of the part. After power-up restore, the value readback from this field shall be the address the device responds to. Refer to Programming PMB_ADDR for details on how pin-strapping affects this field.
7	Reserved	R	0b	Not used and always set to 0.
6:0	UNIQUE_ADDR	R/W	NVM	The secondary (UNIQUE) PMBus address of the part. Primary devices do not support a unique address, and the field is set to the same value as the COMMON_ADDR.

7.67 (D4h) COMP

CMD Address	D4h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
NVM Back-up:	EEPROM
Updates:	On-the-fly

This command contains feedback compensation settings for the regulated rail.

GAIN 1 and RAMP 1 options in Programming MSEL2 use the values for Ramp and Gain from this command, so changes to COMP stored to NVM will change the pin programmed values for GAIN1 and RAMP1 even if the ramp or gain bits in (D8h) PIN_DETECT_OVERRIDE are set to select pin-programmed values

Return to Supported PMBus Commands.

Figure 7-75. Register Map

15	14	13	12	11	10	9	8
R/W	R/W	R/W	R/W	R	R	R	R
GAIN				0			
7	6	5	4	3	2	1	0
R/W	R	R/W	R/W	R/W	R	R/W	R/W
FRC_IN_TIME	0	INT_TIME			0	SEL_RAMP	

LEGEND: R/W = Read/Write; R = Read only

Table 7-79. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:12	GAIN	R/W	NVM	These bits determine the AC Gain setting. 0000b: Gain of 3V/V 0001b: Gain of 5V/V 0010b: Gain of 10V/V 0011b: Gain of 15V/V 0100b: Gain of 20V/V 0101b: Gain of 25V/V 0110b: Gain of 30V/V 0111b: Gain of 35V/V 1000b: Gain of 40V/V 1001b: Gain of 50V/V 1010b: Gain of 60V/V 1011b: Gain of 70V/V
11:8	0	R	0000b	Not supported and always 0.

Table 7-79. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
7	FRC_INT_TIME	R/W	NVM	Force integrator time constant from NVM settings. 0b: Makes the INT_TIME[2:0] bits in this register read-only and are populated based on the existing live data in the (33h) FREQUENCY_SWITCH register, as specified by the look-up table INT_TIME below: • Fsw 400kHz, INT_TIME = 111b • Fsw 600kHz, INT_TIME = 110b • Fsw 800kHz or 1MHz, INT_TIME = 100b • Fsw 1.2MHz or 1.4MHz, INT_TIME = 011b • Fsw 1.8MHz or 2MHz, INT_TIME = 010b 1b: Makes the INT_TIME [2:0] bits in this register writable and initialized from the associated NVM backup
6	0	R	0b	Not supported and always 0.
5:3	INT_TIME	R/W	NVM	Integrator time constand setting. 000b = 0.25µs 001b = 1µs 010b = 3µs 011b = 4.5µs 100b = 6.25µs 101b = 8µs 110b = 10µs 111b = 20µs
2	0	R	0b	Not supported and always 0.
1:0	SEL_RAMP	R/W	NVM	Ramp amplitude/slope setting. These bits determine the ramp amplitude/slope. 00b = 60mV 01b = 120mV 10b = 180mV 11b = 240mV

Data Validity

Attempts to write to a read only bit in COMP will be ignored.

7.68 (D5h) VBOOT_OFFSET_1

CMD Address	D5h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
NVM Back-up:	EEPROM
Updates:	On-the-fly

This command contains bits for setting the boot-up voltage VBOOT.

Return to Supported PMBus Commands.

Figure 7-76. Register Map

15	14	13	12	11	10	9	8
R/W	R/W	R	R	R	R	R	R
SPARE_NVM		0	0	0	0	0	0
7	6	5	4	3	2	1	0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	VBOOT_1				

LEGEND: R/W = Read/Write; R = Read only

Table 7-80. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:14	SPARE_NVM	R/W	NVM	Spare NVM.
13:5	0	R	0b	Not supported and always 0.
4:0	VBOOT_1	R/W	NVM	These bits contains VBOOT setting that is used for the the VREF DAC target code for soft-start purposes (as against directly specifying the initial VOUT voltage). The user must choose the appropriate VOUT_SCALE_LOOP to achieve the desired output voltage VOUT. Setting the DAC target code directly multiplies the number of available VBOOT voltages by the number of internal gain options settings. Note: The effective boot-up voltage is determined by a combination of VBOOT, VOUT_SCALE_LOOP, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, and VOUT_TRIM, as described in the tables under the description of VOUT_COMMAND. The appropriate VOUT is from pin-strap or from NVM of VOUT_SCALE_LOOP. There is nothing preventing the VBOOT value from being updated in any state. If the active VBOOT is updated while in the SoftStart state, the output voltage will slew to the updated VBOOT setting. The VBOOT values are programmed through VBOOT_1.

Data Validity

Attempts to change the read-only bits [13:5] will be considered invalid/unsupported data. The device will NACK the unsupported data and the received value will be ignored. The 'cml' bit in the STATUS_BYTE and the 'ivd' bit in the STATUS_CML registers will be set.

Table 7-81. VBOOT_1 supported values and EEPROM restore values

VBOOT_1 [4:0] (b)	VDAC_BOOT (V)
00000	0
00001	0.299804688
00010	0.3125

Table 7-81. VBOOT_1 supported values and EEPROM restore values (continued)

VBOOT_1 [4:0] (b)	VDAC_BOOT (V)
00011	0.325195313
00100	0.337890625
00101	0.3501
00110	0.362304688
00111	0.375
01000	0.387695313
01001	0.3999
01010	0.412597656
01011	0.424804688
01100	0.4375
01101	0.450195313
01110	0.462890625
01111	0.4751
10000	0.487304688
10001	0.5
10010	0.512695313
10011	0.5249
10100	0.537109375
10101	0.549804688
10110	0.5625
10111	0.575195313
11000	0.587890625
11001	0.599609375
11010	0.625
11011	0.6499
11100	0.674804688
11101	0.700195313
11110	0.724609375
11111	0.75

7.69 (D6h) STACK_CONFIG

CMD Address	D6h
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly

STACK_CONFIG describes the number of devices in the system, where the device is in the stack, and its role in the system. While the bits [7:4] are read-only, the bits [3:2] and [1:0] are populated from pinstrap results.

Return to Supported PMBus Commands.

Figure 7-77. Register Map

7	6	5	4	3	2	1	0
R	R	R	R	RW	RW	RW	RW
PSTR_STACK				STACK_NUMBER		STACK_POSITION	

LEGEND: R/W = Read/Write; R = Read only

Table 7-82. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	PSTR_STACK	R	0000b	Stack number and stack position from pinstrap. Gives pinstrap value is STACK_NUMBER or STACK_POSITION are overwritten. The format is {STACK_NUMBER[1:0],STACK_POSITION[1:0]}.
3:2	STACK_POSITION	R/W	NVM	Device position in system stack. Indicates whether the part is a primary or secondary device. These bits are set by pinstrap. Reads will return pinstrapped values. 00b: Stack Controller / Primary Device 01b: First Secondary Device 10b: Second Secondary Device 11b: Third Secondary Device
1:0	STACK_NUMBER	R/W	NVM	Number of devices in system stack. Indicates the total number of devices in the stack including the controller/primary device. These bits are set by pinstrap. Reads will return pinstrapped values. 00b: Single Phase 01b: 2-Phase 10b: 3-Phase 11b: 4-Phase

7.70 (D8h) PIN_DETECT_OVERRIDE

CMD Address	D8h
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
NVM Back-up:	EEPROM
Updates:	On-the-fly

This register contains bits for overriding selected functions that can be set through NVM or Pinstrapping. When a bit is set to 0b, NVM values from the DEFAULT or USER stores override pin programmmed values according to the PMBus priority of command sources. When the bit is set to 1b, Pin programmed values override NVM values (DEFAULT or USER STORE).

PMBus command values populated from Pin Detection at Power On will not update their NVM values unless those commands are written prior to storing. When changing a bit from 1b to 0b, it is necessary to write the desired value to that command or commands before storing to NVM.

In order for an override bit to take effect (become activated), the user has to write the bit, store to EEPROM, and power-cycle the part.

Return to Supported PMBus Commands.

Figure 7-78. Register Map

15	14	13	12	11	10	9	8
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
OVRD_STACK	0	0	0	OVRD_SS	OVRD_FLT_R_ESP	OVRD_PMB_ADDR	0
7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	OVRD_MODE	OVRD_FSW	OVRD_RAMP	OVRD_GAIN	OVRD_OCL	0	OVRD_VSEL

LEGEND: R/W = Read/Write; R = Read only

Table 7-83. Register Field Descriptions

Bit	Field	Access	Reset	Description
15	OVRD_STACK	R/W	NVM	0b: Pinstrap results for (D6h) STACK_CONFIG are ignored. The device operates as a Primary, Single Phase device. 1b: Pinstrap results determine the Primary / Secondary configuration and (D6h) STACK_CONFIG value.
14:12	0	R	0b	Not supported and always set to 0. Attempts to write to this bit will be ignored.
13:12	0	R/W	00b	Not supported and always set to 0.
11	OVRD_SS	R/W	NVM	Override soft-start pinstrap value. 0b: Pinstrap results for TON_RISE are ignored. The values from NVM remain in effect until values are written to the TON_RISE register. 1b: Pinstrap results determine the soft-start value.
10	OVRD_FLT_RESP	R/W	NVM	Override fault response pinstrap value. 0b: PinStrap results for FAULT_RESPONSE are ignored. The values from NVM remain in effect until values are written to the VOUT_OV_FAULT_RESPONSE, VOUT_UV_FAULT_RESPONSE, or OT_FAULT_RESPONSE registers. 1b: Pinstrap results determine the fault response.

Table 7-83. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
9	OVRD_PMB_ADDR	R/W	NVM	Override PMBus Address pinstrap value. 0b: PinStrap results for PMBus_ADDR are ignored. The values from NVM remain in effect until values are written to the PMBus_ADDR register. 1b: Pinstrap results determine the PMBus Address value.
8:7	0	R/W	00b	Not supported and always set to 0.
6	OVRD_MODE	R/W	NVM	Override Mode pinstrap value. 0b: PinStrap results or FCCM/DCM light load operation are ignored. The values from NVM remain in effect until values are written to the SYS_CFG_USER1 register. 1b: Pinstrap results determine the Mode value.
5	OVRD_FSW	R/W	NVM	Override Frequency Switch pinstrap value. 0b: PinStrap results for FREQUENCY_SWITCH are ignored. The values from NVM remain in effect until values are written to the FREQUENCY_SWITCH register. 1b: Pinstrap results determine the Frequency Switch value.
4	OVRD_RAMP	R/W	NVM	Override RAMP pinstrap value. 0b: PinStrap results for COMP are ignored. The values from NVM remain in effect until values are written to the COMP register. 1b: Pinstrap results determine the RAMP value.
3	OVRD_GAIN	R/W	NVM	Override GAIN pinstrap value. 0b: PinStrap results obtained from Pin pinstrapping operation are ignored. The values from NVM remain in effect until values are written to the COMP register. 1b: Pinstrap results determine the RAMP and GAIN values.
2	OVRD_OCL	R/W	NVM	Override Overcurrent Limit (OCL) pinstrap value. 0b: PinStrap results IOUT_OC_FAULT_LIMIT are ignored. The values from NVM remain in effect until values are written to the IOUT_OC_FAULT_LIMIT register. 1b: Pinstrap results determine the OCL value.
1	0	R/W	NVM	Not supported and always set to 0.
0	OVRD_VSEL	R/W	NVM	Override VSEL pinstrap value. 0b: PinStrap results for VSEL are ignored. The values from NVM remain in effect until values are written to the VBOOT_1, VOUT_SCALE_LOOP, VOUT_COMMAND, VOUT_MAX, or VOUT_MIN registers. 1b: Pinstrap results determine the VSEL value. Ignored if external resistor divider is chosen.

7.71 (D9h) NVM_CHECKSUM

CMD Address	D1h
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
NVM Back-up:	No
Updates:	On-the-fly

This command contains CRC value from reading contents of the non-volatile memory (NVM). The value of the checksum will be calculated as CRC-16 (polynomial 0x8005). The checksum will be calculated in 8 parallel slices. Any padding needed to make the last word of the input 8 bits will be 0s. The checksum value will be stored in NVM to ensure the integrity of the STORE function. Any corrupted data that happens during a STORE operation will be detected on RESTORE when the user compares the calculated NVM_CHECKSUM with a known good value that is expected.

Return to Supported PMBus Commands.

Figure 7-79. (D9h) NVM_CHECKSUM Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
NVM_CHECKSUM							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
NVM_CHECKSUM							

LEGEND: R/W = Read/Write; R = Read only

Table 7-84. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	NVM_CHECKSUM	R		Responds with the Check Sum results of the last stored NVM. The 32-bit (0Eh) PASSKEY NVM bits are excluded from the NVM_CHECKSUM determination to prevent a malicious actor from reading the device configuration and repeatedly setting PASSKEY values in an attempt to discover the PASSKEY value.

7.72 (DAh) READ_TELEMETRY

CMD Address	DAh
Write Transaction:	N/A
Read Transaction:	Read Block
Format:	Unsigned Binary (6 bytes)
NVM Back-up:	No
Updates:	On-the-fly

This command provides for a 6-byte BLOCK read of Telemetry values to improve bus utilization for poling by combining multiple READ functions into a single command, eliminating the need for multiple address and command code bytes.

Each Byte-pair within the READ_TELEMETRY block is ordered as a READ WORD pair with the low-byte first and high-byte second. The bytes are order as (Byte 0 through Byte 5):

Byte 0, Byte 1: READ_VOUT Low-Byte, READ_VOUT High-Byte

Byte 2, Byte 3: READ_IOUT Low-Byte, READ_IOUT High-Byte

Byte 4, Byte 5: READ_TEMP1 Low-Byte, READ_TEMP1 High-Byte

Return to Supported PMBus Commands.

Figure 7-80. (DAh) READ_TELEMETRY Block Map

0	1	2	3	4	5
R	R	R	R	R	R
READ_VOUT		READ_IOUT		READ_TEMP1	

LEGEND: R/W = Read/Write; R = Read only

Table 7-85. Block Field Descriptions

Block	Field	Access	Reset	Description
0:1	READ_VOUT	R		For the contents of each byte-pair in the block, refer to the specifics of each command.
2:3	READ_IOUT	R		
4:5	READ_TEMP1	R		

7.73 (DBh) STATUS_ALL

CMD Address:	DBh
Write Transaction:	N/A
Read Transaction:	Read Block
Format:	Unsigned Binary (6 bytes)
NVM Back-up:	No
Updates:	On-the-fly

STATUS_ALL provides for a 6-byte block BLOCK READ of all 6 standard STATUS command codes. This can reduce bus utilization to read multiple faults.

Return to Supported PMBus Commands.

Figure 7-81. (DBh) STATUS_ALL Block Map

0	1	2	3	4	5
R	R	R	R	R	R
STATUS_VOUT	STATUS_IOUT	STATUS_INPUT	STATUS_TEMPERATURE	STATUS_CML	STATUS_MFR

LEGEND: R/W = Read/Write; R = Read only

Table 7-86. Block Field Descriptions

Block	Field	Access	Reset	Description
0	STATUS_VOUT	R		For the contents of each byte in the block, refer to the specifics of each command.
1	STATUS_IOUT	R		
2	STATUS_INPUT	R		
3	STATUS_TEMPERATURE	R		
4	STATUS_CML	R		
5	STATUS_MFR	R		

7.74 (DDh) EXT_WRITE_PROTECTION

CMD Address	DDh
Write Transaction:	Write Word
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
NVM Back-up:	EEPROM
Updates:	On-the-fly

This command configures additional register write protection beyond the standard PMBus write protection (10h) WRITE_PROTECT.

Return to Supported PMBus Commands.

Figure 7-82. (DDh) EXT_WRITE_PROTECTION Register Map

15	14	13	12	11	10	9	8
R	RW	RW	RW	RW	RW	RW	RW
0	WPL	TRIML	VOCL	VOFCL	WRNL	IO_TEMPL	MRGNL
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OPL	DFGL	VIFCL	SQNCL	MFRDL	PSKYL	RNVML	SNVML

LEGEND: R/W = Read/Write; R = Read only

Table 7-87. Register Field Descriptions

Bit	Field	Access	Reset	Description
15	0	R	0b	Not used and always set to 0. Attempts to read this bit will be ignored.
14	WPL	R/W	NVM	**W**rite **P**rotect **L**ock. Blocks writes to the standard (10h) WRITE_PROTECT and EXTENDED_WRITE_PROTECT commands. Once set, it is not removable. 0b: (10h) WRITE_PROTECT and EXTENDED_WRITE_PROTECT commands are writeable. 1b:(10h) WRITE_PROTECT and EXTENDED_WRITE_PROTECT commands are read only.
13	TRIML	R/W	NVM	Blocks writes to trim related commands (VOUT_TRIM, IMON_CAL, VOUT_SCALE_LOOP, VOUT_SCALE_MONITOR, VBOOT_OFFSET_1), including commands which set the base output voltage and are typically set to a fixed value for the devices configuration. 0b: Commands are writable unless write protected by (10h) WRITE_PROTECT. 1b:Commands are read only.
12	VOCL	R/W	NVM	**Vo**ut **C**ommand **L**ock. Blocks writes to commands related to setting the base output voltage (VOUT_MODE, VOUT_COMMAND) and may be changed dynamically in the application. 0b: Commands are writable unless write protected by (10h) WRITE_PROTECT. 1b:Commands are read only.
11	VOFCL	R/W	NVM	**Vo**ut **F**ault **C**onfiguration **L**ock. Blocks writes to commands related to configuration of output voltage faults (VOUT_MAX, VOUT_OV_FAULT_LIMIT, VOUT_OV_FAULT_RESPONSE, VOUT_UV_FAULT_LIMIT, VOUT_UV_FAULT_RESPONSE, VOUT_MIN). 0b: Commands are writable unless write protected by (10h) WRITE_PROTECT. 1b:Commands are read only.

Table 7-87. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
10	WRNL	R/W	NVM	**Warn**ings **L**ock. Blocks writes to commands related to configuration of warnings (SMBALERT_MASK, VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT, IOUT_OC_WARN_LIMIT, OT_WARN_LIMIT), including masking which faults or warnings can assert SMB_ALERT#. 0b: Commands are writable unless write protected by (10h) WRITE_PROTECT. 1b:Commands are read only.
9	IO_TEMPL	R/W	NVM	**Io**utand **Temp**erature **L**ock. Blocks writes to commands related to configuration of output current and temperature faults (IOUT_OC_FAULT_LIMIT, IOUT_OC_FAULT_RESPONSE, OT_FAULT_LIMIT, OT_FAULT_RESPONSE). 0b: Commands are writable unless write protected by (10h) WRITE_PROTECT. 1b:Commands are read only.
8	MRGNL	R/W	NVM	**Margin L**ock. Blocks writes to commands related to margining the output voltage (VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, VOUT_TRANSITION_RATE). 0b: Commands are writable unless write protected by (10h) WRITE_PROTECT. 1b:Commands are read only.
7	OPL	R/W	NVM	**Op**eration **L**ock. Blocks writes to the OPERATION command. 0b: Commands are writable unless write protected by (10h) WRITE_PROTECT. 1b:Commands are read only.
6	CFGL	R/W	NVM	**Con**fig**L**ock. Blocks writes to commands related to setting the device's configuration (FREQUENCY_SWITCH, SYS_CFG_USER1, PMB_ADDR, COMP , STACK_CONFIG). 0b: Commands are writable unless write protected by (10h) WRITE_PROTECT. 1b:Commands are read only.
5	VIFCL	R/W	NVM	**Vin F**ault **C**onfiguration **L**ock. Blocks writes to commands related to configuration of input voltage faults (VIN_OV_FAULT_LIMIT). 0b: Commands are writable unless write protected by (10h) WRITE_PROTECT. 1b:Commands are read only.
4	SQNL	R/W	NVM	**Sequence L**ock. Blocks writes to commands related to configuration of sequencing (TON_DELAY, TON_RISE, TOFF_DELAY, TOFF_FALL, ON_OFF_CONFIG, VIN_ON, and VIN_OFF). 0b: Commands are writable unless write protected by (10h) WRITE_PROTECT. 1b:Commands are read only.
3	MFRDL	R/W	NVM	**Manufacturer D**ata **L**ock. Blocks writes to manufacturer data commands (MFR_ID, MFR_MODEL, MFR_REVISION). 0b: Commands are writable unless write protected by (10h) WRITE_PROTECT. 1b:Commands are read only.
2	PSKYL	R/W	NVM	**Passkey L**ock**.** Blocks writes to the PASSKEY command. This is meant to prevent accidental or malicious attempts to set a PASSKEY on a device without one. Setting this bit will also prevent unlocking the device through the PASSKEY command. 0b: Commands are writable unless write protected by (10h) WRITE_PROTECT. 1b:Commands are read only.
1	RNVML	R/W	NVM	**R**estore **NVM L**ock. Blocks writes to the RESTORE_USER_ALL command. When RESTORE_USER_ALL is blocked, restore after power-up must still be allowed. 0b: Commands are writable unless write protected by (10h) WRITE_PROTECT. 1b:Commands are read only.
0	SNVML	R/W	NVM	**S**tore **NVM L**ock. Blocks writes to the STORE_USER_ALL command. 0b: Commands are Writable unless Read Only from (10h) WRITE_PROTECT. 1b at Power on Reset or RESTORE: Commands are read only. 1b at all other times: No change until STORE, then a reset or RESTORE.

7.75 (DEh) IMON_CAL

CMD Address	DEh
Write Transaction:	Write Byte
Read Transaction:	Read Byte
Format:	Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly

The IMON_CAL command contains bits for READ_IOUT calibration.

Return to Supported PMBus Commands.

Figure 7-83. (DEh) IMON_CAL Register Map

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0				IMON_OFS_CAL			

LEGEND: R/W = Read/Write; R = Read only

Table 7-88. Register Field Descriptions

Bit	Field	Access	Reset	Description
7:4	0	R	0000b	Not supported and always 0.
3:0	IMON_OFS_CAL	R/W	NVM	These bits contains the READ_IOUT gain calibration. This field gives flexibility to change the gain of nominal reporting by −3.52% to +3.91%. 0000b: IMON Gain Adjustment = −3.52% 0001b: IMON Gain Adjustment = −3.13% 0010b: IMON Gain Adjustment = −2.34% 0011b: IMON Gain Adjustment = −1.95% 0100b: IMON Gain Adjustment = −1.56% 0101b: IMON Gain Adjustment = −1.17% 0110b: IMON Gain Adjustment = −0.39% 0111b: IMON Gain Adjustment = −0% 1000b: IMON Gain Adjustment = +0.39% 1001b: IMON Gain Adjustment = +1.17% 1010b: IMON Gain Adjustment = +1.56% 1011b: IMON Gain Adjustment = +1.95% 1100b: IMON Gain Adjustment = +2.34% 1101b: IMON Gain Adjustment = +3.13% 1110b: IMON Gain Adjustment = +3.52% 1111b: IMON Gain Adjustment = +3.91%

7.76 (FCh) FUSION_ID0

CMD Address	FCh
Write Transaction:	N/A
Read Transaction:	Read Word
Format:	Unsigned Binary (2 bytes)
Phased:	No
NVM Back-up:	No

FUSION_ID0 provides a platform level Identification code to be used by Texas Instruments Digital Power Designer for identifying a TI device.

Writes to this command will be accepted, but ignored otherwise (the readback value of this command does not change following a write attempt). This command is writeable for some TI devices, so to maintain cross-compatibility, the device accepts write transactions to this command as well. No STATUS_CML bits are set as a result of the receipt of a write attempt to this command.

Return to Supported PMBus Commands.

Figure 7-84. (FCh) FUSION_ID0 Register Map

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
FUSION_ID0							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
FUSION_ID0							

LEGEND: R/W = Read/Write; R = Read only

Table 7-89. Register Field Descriptions

Bit	Field	Access	Reset	Description
15:0	FUSION_ID0	R	02C0h	Hard Coded to 02C0h

7.77 (FDh) FUSION_ID1

CMD Address	FDh
Write Transaction:	N/A
Read Transaction:	Block Read
Format:	Unsigned Binary (6 bytes)
Phased:	No
NVM Back-up:	No

FUSION_ID1 provides a platform level Identification code to be used by Texas Instruments Digital Power Designer for identifying a TI device.

Writes to this command will be accepted, but ignored otherwise (the readback value of this command does not change following a write attempt). This command is writeable for some TI devices, so to maintain cross-compatibility, the device accepts write transactions to this command as well. No STATUS_CML bits are set as a result of the receipt of a write attempt to this command.

Return to Supported PMBus Commands.

Figure 7-85. (FDh) FUSION_ID1 Register Map

47	46	45	44	43	42	41	40
R	R	R	R	R	R	R	R
FUSION_ID1							
39	38	37	36	35	34	33	32
R	R	R	R	R	R	R	R
FUSION_ID1							
31	30	29	28	27	26	25	24
FUSION_ID1							
23	22	21	20	19	18	17	16
R	R	R	R	R	R	R	R
FUSION_ID1							
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
FUSION_ID1							
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
FUSION_ID1							

LEGEND: R/W = Read/Write; R = Read only

Table 7-90. Register Field Descriptions

Bit	Field	Access	Reset	Description
47:40	FUSION_ID1	R	4Bh	Hard coded to 4Bh
39:32	FUSION_ID1	R	43h	Hard coded to 43h
31:24	FUSION_ID1	R	4Fh	Hard coded to 4Fh
23:16	FUSION_ID1	R	4Ch	Hard coded to 4Ch

Table 7-90. Register Field Descriptions (continued)

Bit	Field	Access	Reset	Description
15:8	FUSION_ ID1	R	49h	Hard coded to 49h
7:0	FUSION_ ID1	R	54h	Hard coded to 54h

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS546E25 device is a highly-integrated, synchronous, step-down DC/DC converter. The TPS546E25 has a simple design procedure where programmable parameters can be configured by pin-strapping or PMBus and stored to nonvolatile memory (NVM) to minimize external component count.

8.2 Typical Application

8.2.1 Application

This design describes a 1.2V, 50A application.

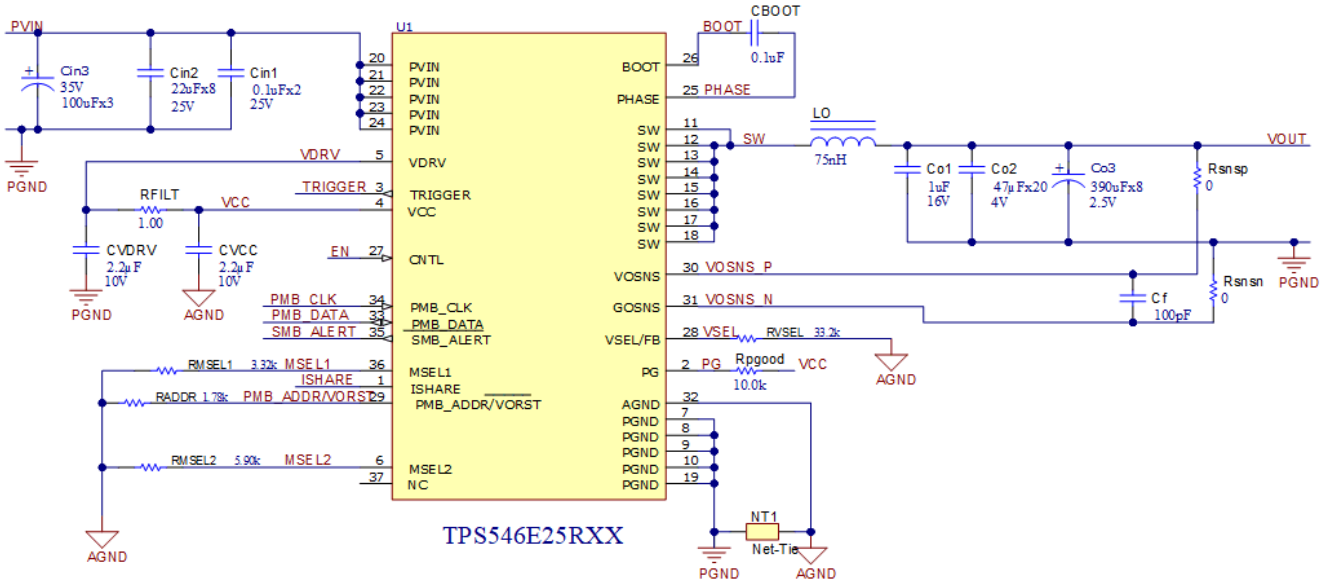


Figure 8-1. 1.2V, 50A Output Application

8.2.2 Design Requirements

This design uses the parameters listed in the following table.

Table 8-1. Design Parameters

PARAMETER	VALUE
Input voltage	10.8V – 13.2V
Output voltage	1.2V
Output current	50A
Switching frequency	800kHz
PMBus address	11h

8.2.3 Detailed Design Procedure

The following steps illustrate how to select key components, pin-strapping, and other considerations to use the device.

8.2.3.1 Input Capacitor Selection

Input capacitors must be selected to provide reduction in input voltage ripple and high-frequency bypassing, which in return reduces switching stress on the power stage MOSFETs internal to the device. In this example, a 0.1µF, 25V, 0402 must be placed as close as possible to the PVIN pins of the device on the same layer as the IC on the PCB. In addition, 8 × 22µF ceramic capacitors are used and a 100µF bulk capacitor is used on the input.

8.2.3.2 Inductor Selection

The inductor must be selected such that the transient performance and ripple requirements are balanced for a particular design. In general, a smaller inductance increases loop bandwidth leading to better transient response at the expense of higher current and voltage ripple.

Determine the amount of inductor ripple current desired for the converter. 25% to 40% of the maximum DC output current results in a good compromise between RMS losses (in the MOSFETs and inductor) and good load transient response.

$$L = ((vin\text{-}vout) \times duty\text{-}cycle \times Ts) / (delta\text{-}I) \quad (13)$$

Now select an inductor capable of withstanding the DC current. A good selection:

- Has inductance *droop* of less than 20% of initial value at full load
- Not saturate under overload conditions
- Has low DC and core losses at the frequency of operation
- Has a temperature rise within the bounds of the operating environment

In this example, a 75nH, 0.228mΩ inductor is used.

8.2.3.3 Output Capacitor Selection

Selecting the output capacitance for the converter involves a number of considerations. Closed loop stability and load transient response are the two main goals. From the perspective of loop stability, the impedance of the output capacitance must take into account not only the value of the capacitor, but the ESR and ESL as well. The ESR provides a *zero* to the filter transfer function at

$$Fz = 1 / (2pi \times ESR \times C) \quad (14)$$

and the ESL provides a second zero at

$$Fz2 = 1 / (2pi \times sqrt (ESL \times C)) \quad (15)$$

In selecting the output capacitance of the output filter, often two or three types of capacitors are used.

The selection of output capacitance to support load transient response is the next consideration. The capacitance to minimize an output voltage overshoot is calculated as

$$Cout > (L \times Idrop\text{^}2) / (vout\_overshoot\text{^}2\text{-}vout\_nominal\text{^}2) \quad (16)$$

This is the energy in the inductor being transferred to the energy difference between the nominal output voltage and the peak overshoot output voltage.

In many cases, with a 3% output voltage overshoot requirement, the resulting LC corner frequency is on the order of 1% to 1.5% of the switching frequency.

The fast load transient response of D-CAP4 largely addresses the case where there is a load increase and a voltage undershoot. However, there are cases where, during a load step increase, the minimum OFF time

of the converter limits the ability of the converter to increase the switching frequency fast enough to maintain regulation. This case can be true for higher output voltages and higher nominal switching frequencies.

In this design, 8 × 390µF SP caps and 20 × 47µF ceramic caps are used to support a 50A load step with 100A/µs slew rate with a +/–3% output voltage regulation.

8.2.3.4 Compensation Selection

The internal compensation of the device covers a wide range of applications. Some settings are adjusted automatically, such as the zero frequency of the error amplifier, which is adjusted with frequency selection. Other settings are determined by pin-strapping selection of MSEL2 or setting through PMBus.

FB_ZERO_TAU is the setting for the error amplifier zero setting:

$$Fz = (10^6) / (2\pi \times FB\_ZERO\_TAU) \quad (17)$$

The RAMP sets the internal inner-loop RAMP amplitude. See *Programming MSEL2* and COMP for a full description of the RAMP settings available through pin-strapping and PMBus. Start with the 120mv setting. This selection must give the best compromise between jitter and transient response. A larger RAMP can improve jitter at the expense of lower phase margin, necessitating the need for a feed-forward capacitor (across an upper voltage setting divider resistor).

When using the internal divider to set the output voltage, GAIN is used to make sure the feedback loop has enough loop gain to provide stability and good load transient performance. Select the GAIN setting according to the VOUT_SCALE_LOOP parameter setting.

GAIN	VOSL
3	0.125
10	0.25
15	0.5
30	1

For converters with external voltage setting resistors, begin with the GAIN setting as in C above, and divide by the voltage setting resistor ratio.

$$GAIN\_External\_R = GAIN\_From\_C\_above / (R\_BOT / (R\_TOP+R\_BOT)) \quad (18)$$

The device uses D-CAP4 control to achieve a fast load transient response while maintaining ease-of-use. The D-CAP4 control architecture includes an internal ripple generation network enabling the use of very low ESR output capacitors such as multi-layered ceramic capacitors (MLCC) and low ESR polymer capacitors. No external current sensing network or voltage compensators are required with D-CAP4 control architecture.

The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine with the voltage feedback signal to regulate the loop operation. D-CAP4 control architecture reduces loop gain variation across VOUT, enabling a fast load transient response across the entire output voltage range with one ramp setting. The R-C time-constant of the internal ramp circuit sets the zero frequency of the ramp, similar to other R-C based internal ramp generation architectures. The reduced variation in loop gain also mitigates the need for a feedforward capacitor to optimize the transient response. The ramp amplitude varies with VIN to minimize variation in loop gain across input voltage, commonly referred to as input voltage feedforward.

The device uses internal circuitry to correct for the DC offset caused by the injected ramp, and significantly reduces the DC offset caused by the output ripple voltage, especially with light load current. For any control topologies supporting no external compensation, there is a minimum range, maximum range, or both, for the output filter to support. The output filter used for a typical buck converter is a low-pass L-C circuit. This L-C filter has double pole. At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency L-C double pole has a 180-degree drop in phase. At the

output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and increases the phase by 90 degrees per decade above the zero frequency.

The inductor and capacitor selected for the output filter must be such that the double pole is located no higher than 1/30th of the steady-state operating frequency.

The compensation and output filter must be considered together. Choosing very small output capacitance leads to a high frequency L-C double pole which causes the overall loop gain to stay high until the L-C double frequency. Given the zero from the internal ripple generation network is a relatively high frequency as well, the loop with very small output capacitance can have too high of a crossover frequency which can cause instability.

In general, where reasonable (or smaller) output capacitance is desired, output ripple requirement and load transient requirement can be used to determine the necessary output capacitance for stable operation. For the maximum output capacitance recommendation, select the inductor and capacitor values so that the L-C double pole frequency is no less than 1/100th of the operating frequency. With this starting point, verify the small signal response on the board using the following criteria: the phase margin at the loop crossover is greater than 50 degrees. The actual maximum output capacitance can go higher as long as phase margin is greater than 50 degrees. However, small signal measurement (bode plot) must be done to confirm the design.

If MLCCs are used, consider the derating characteristics to determine the final output capacitance for the design. For example, when using an MLCC with specifications of 10µF, X5R and 6.3V, the derating by DC bias and AC bias are 80% and 50%, respectively. The effective derating is the product of these two factors, which in this case is 40% and 4µF. Consult with capacitor manufacturers for specific characteristics of the capacitors to be used in the application.

For large output filters with an L-C double pole near 1/100th of the operating frequency, additional phase boost can be required. A feedforward capacitor placed in parallel with RFB_HS can boost the phase. Refer to *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* application note for details. Besides boosting the phase, a feedforward capacitor feeds more VOUT node information into the FB node through AC coupling. This feedforward during load transient event enables faster response of the control loop to a VOUT deviation. However, this feedforward during steady state operation also feeds more VOUT ripple and noise into FB. High ripple and noise on FB usually leads to more jitter, or even double-pulse behavior. To determine the final feedforward capacitor value impacts to phase margin, load transient performance, ripple, and noise on FB must all be considered.

8.2.3.5 VCC and VRDV Bypass Capacitors

Use a minimum of 2.2µF to 4.7µF, 10V rated capacitor for bypassing of the VCC and VDRV pins, with a 1Ω connecting the two pins. The VCC bypass capacitor must refer to AGND, and the VDRB bypass capacitor must refer to PGND.

8.2.3.6 BOOT Capacitor Selection

Use a minimum of a 0.1µF capacitor connected from PHASE to BOOT. An optional series boot resistor of 0Ω or 2.2Ω can be added.

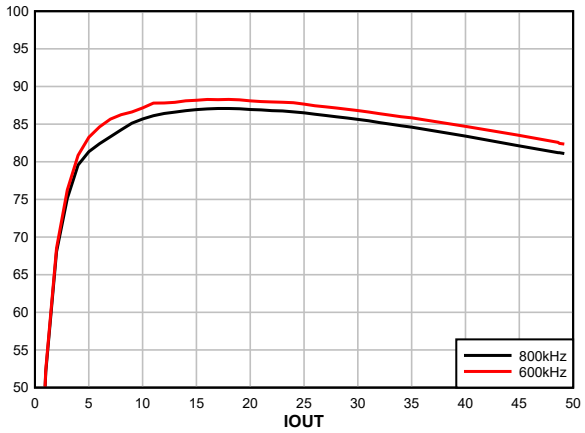
8.2.3.7 VOSNS and GOSNS Capacitor Selection

Use a 100pF ceramic capacitor between VOSNS and GOSNS, with RSNSP and RSNSN resistors to VOUT and PGND respectively. The decoupling capacitor minimizes the impact from switching noise and enables better VOUT and remote PGND sensing at the load.

8.2.3.8 PMBus® Address Resistor Selection

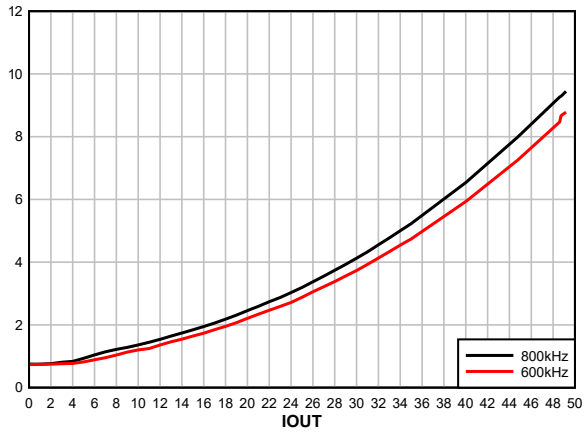
Refer to *Programming PMB_ADDR/VORST#* for the list of PMBus addresses selectable by an external resistor. A resistor between the PMB_ADDR/VORST# pin and AGND sets the preconfigured PMBus address in the memory map. In this application, the 1.78kΩ resistor selects a PMBus address of 11h.

8.2.4 Application Curves



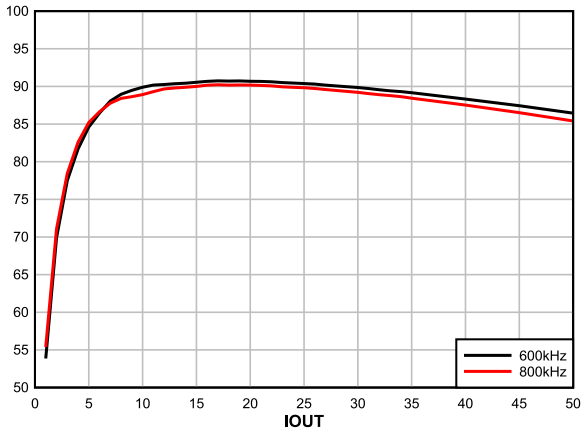
PVIN = 12V V_{OUT} = 0.75V

Figure 8-2. Efficiency, FCCM, Internal LDO



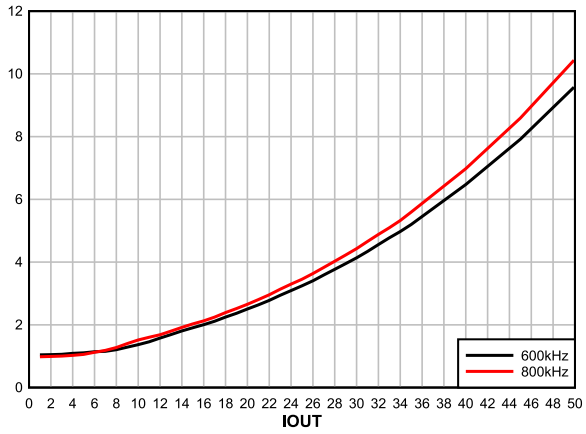
PVIN = 12V V_{OUT} = 0.75V

Figure 8-3. Power Dissipation, FCCM, Internal LDO



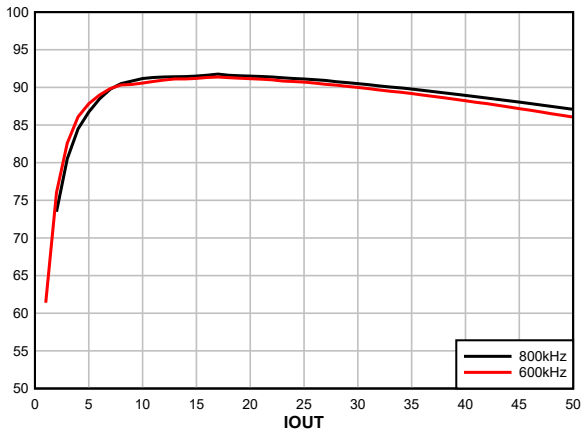
PVIN = 12V V_{OUT} = 1.2V

Figure 8-4. Efficiency, FCCM, Internal LDO



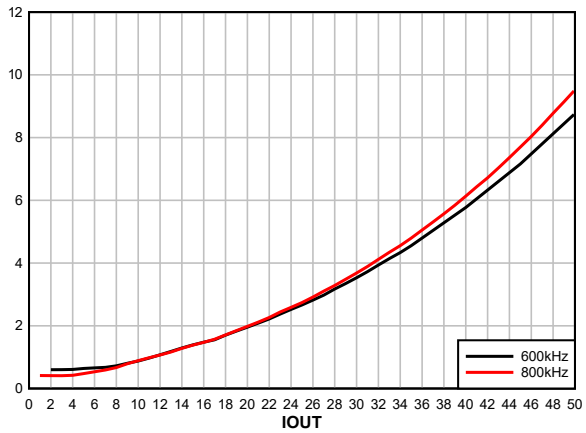
PVIN = 12V V_{OUT} = 1.2V

Figure 8-5. Power Dissipation, FCCM, Internal LDO



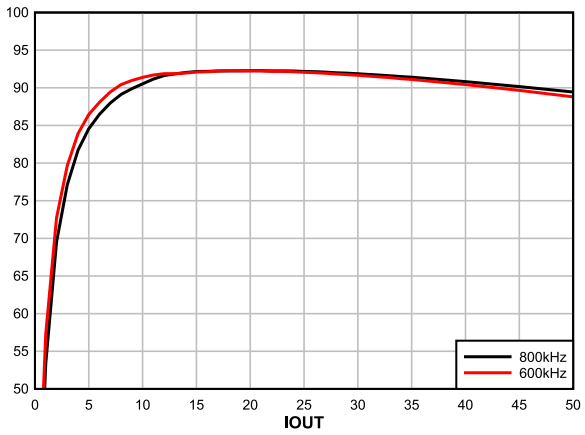
PVIN = 12V V_{OUT} = 1.2V

Figure 8-6. Efficiency, FCCM, External 5V Bias



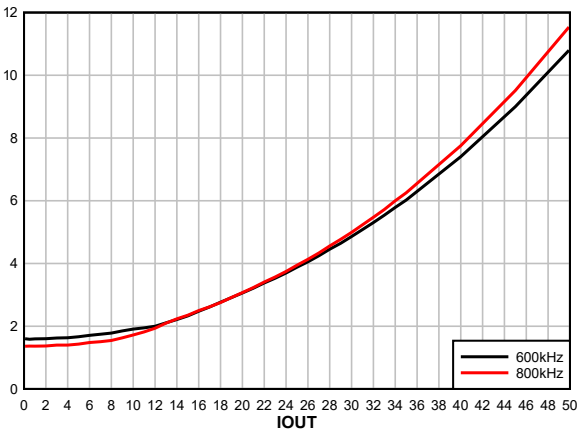
PVIN = 12V V_{OUT} = 1.2V

Figure 8-7. Power Dissipation, FCCM, External 5V Bias



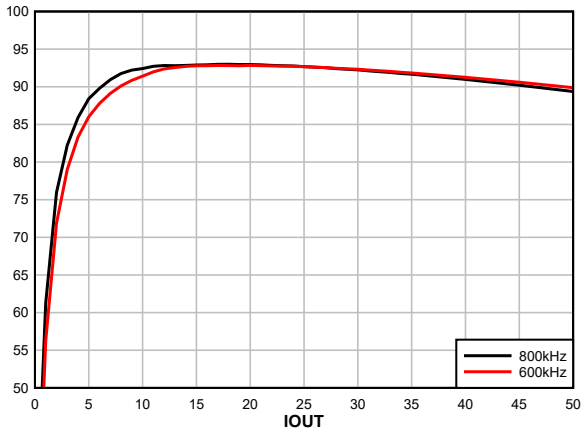
PVIN = 12V V_{OUT} = 1.8V

Figure 8-8. Efficiency, FCCM, Internal LDO



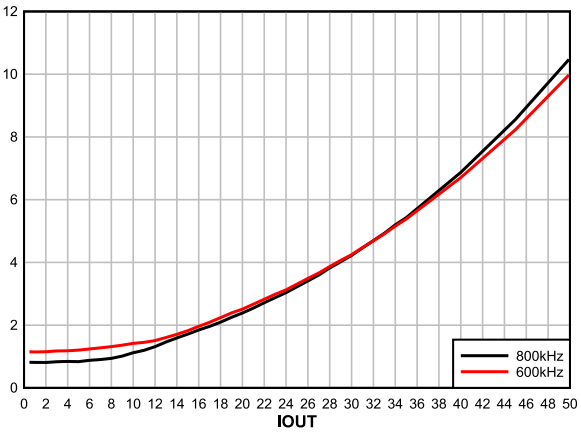
PVIN = 12V V_{OUT} = 1.8V

Figure 8-9. Power Dissipation, FCCM, Internal LDO



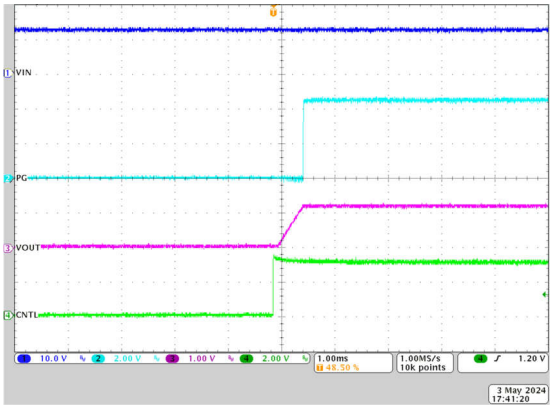
PVIN = 12V V_{OUT} = 1.8V

Figure 8-10. Efficiency, FCCM, External 5V Bias



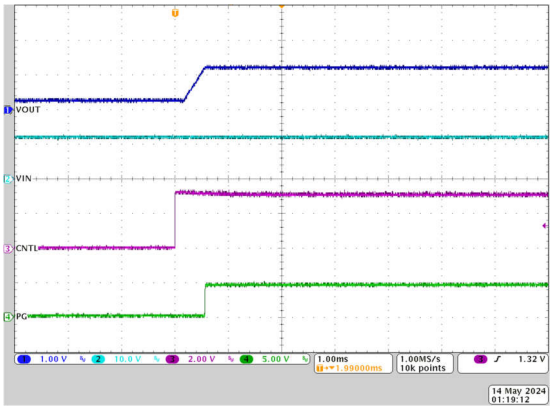
PVIN = 12V V_{OUT} = 1.8V

Figure 8-11. Power Dissipation, FCCM, External 5V Bias



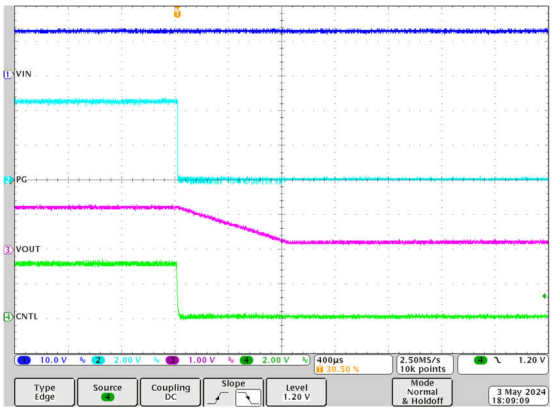
CH1 = VIN CH3 = VOUT
CH2 = PG CH4 = CNTL

Figure 8-12. CNTL Start-Up Waveform



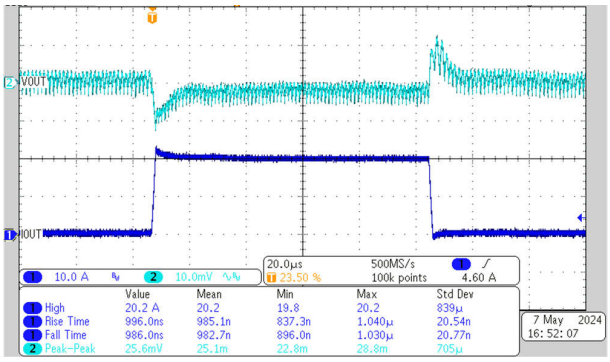
CH1 = VOUT CH3 = CNTL
CH2 = VIN CH4 = PG

Figure 8-13. CNTL Prebiased Start-Up, 300mV Applied



CH1 = VIN
CH2 = PG
CH3 = VOUT
CH4 = CNTL

Figure 8-14. CNTL Shutdown Waveform, 1.2 Vout, 800kHz FCCM



CH1 = IOUT
CH2 = VOUT
20A/us Slew Rate

Figure 8-15. Load Transient 0A to 20A

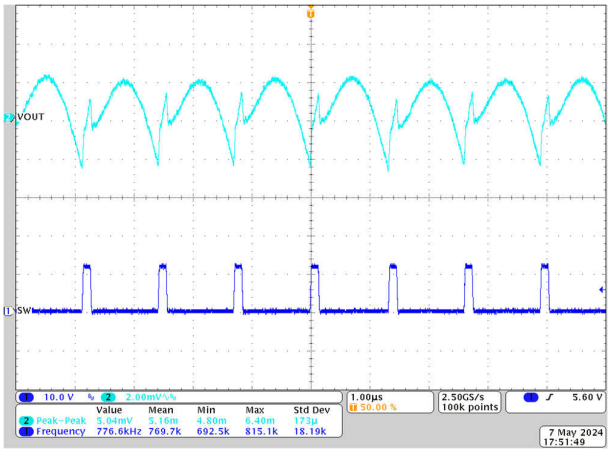


Figure 8-16. Output Voltage Ripple, 1.2V Vout, 800kHz FCCM, 25A Load

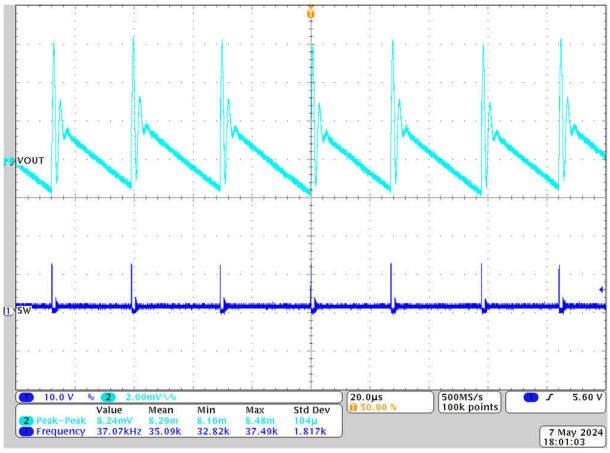


Figure 8-17. Output Voltage Ripple, 1.2V Vout, 800kHz DCM, No load

8.3 Power Supply Recommendations

The device is designed to operate from a wide input voltage supply range between 2.7V and 18V when the VCC and VDRV pins are powered by an external bias ranging from 4.75V to 5.3V. All input supplies (PVIN, VCC, and VDRV bias) must be well regulated. Proper bypassing of input supplies is also critical for noise performance, as are PCB layout and grounding scheme. See the recommendations in *Layout Guidelines*.

8.4 Layout

8.4.1 Layout Guidelines

Layout is critical for good power-supply design. Section 8.4.2 shows the recommended PCB layout configuration.

A list of PCB layout considerations using the device is listed as follows:

- Place the power components (including input and output capacitors, the inductor, and the IC) on the top side of the PCB. To shield and isolate the small signal traces from noisy power lines, insert at least one solid ground inner plane.
- PVIN-to-PGND decoupling capacitors are important for FET robustness. Besides the large volume 0603 or 0805 ceramic capacitors, TI highly recommends a 0.1µF 0402 ceramic capacitor with 25V / X7R rating on

PVIN pin 20 (top layer) to bypass any high frequency current in PVIN to PGND loop. TI recommends the 25V rating, but the rating can be lowered to 16V rating for an application with tightly regulated 12V input bus.

- When one or more PVIN-to-PGND decoupling capacitors are placed on bottom layer, extra impedance is introduced to bypass IC PVIN node to IC PGND node. Placing at least three times PVIN vias on PVIN pad (formed by pin 20 to pin 24) and at least nine times PGND vias on the thermal pad (underneath of the IC) is important to minimize the extra impedance for the bottom layer bypass capacitors.
- In addition to the PGND vias underneath the thermal pad, at least 4 PGND vias are required to be placed as close as possible to the PGND pin 7 to pin 10. At least two PGND vias are required to be placed as close as possible to the PGND pin 19. This action minimizes PGND bounces and also lowers thermal resistance.
- Place the VDRV-to-PGND decoupling capacitor as close as possible to the device. TI recommends a 2.2µF/6.3V/X7R/0603 or 4.7µF/6.3V/X6S/0603 ceramic capacitor. The voltage rating of this bypass capacitor must be at least 6.3V but no more than 10V to lower ESR and ESL. The recommended capacitor size is 0603 to minimize the capacitance drop due to DC bias effect. Make sure the VDRV to PGND decoupling loop is the smallest and make sure the routing trace is wide enough to lower impedance.
- Place the VCC-to-AGND decoupling capacitor on the same side and as close as possible to the IC. Connect VCC pin to VDRV pin with a 1ohm 0402 5% or better resistor. Placing a 1Ω resistor between the VCC pin and VDRV pin forms a RC filter on VCC pin, which greatly reduces the noise impact from power stage driver circuit. TI recommends a 2.2µF/6.3V/X7R/0603 or 4.7µF/6.3V/X6S/0603 ceramic capacitor. The voltage rating of this bypass capacitor must be at least 6.3V but no more than 10V to lower ESR and ESL.
- For remote sensing, the connections from the VOSNS/GOSNS pins to the remote location must be a pair of PCB traces with at least 12 mil trace width, and must implement Kelvin sensing across a high bypass capacitor of 0.1µF or higher. The ground connection of the remote sensing signal must be connected to GOSNS pin. The VOUT connection of the remote sensing signal must be connected to the VOSNS pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. And TI recommends to shield the pair of remote sensing lines with ground planes above and below.
- For single-end sensing, connect the VOSNS pin to a high-frequency local bypass capacitor of 0.1µF or higher, and short GOSNS to AGND with shortest trace.
- The AGND must be connected to a solid PGND plane. TI recommends to place two AGND vias close to the pin to route AGND from top layer to bottom layer, and then connect the AGND trace to the PGND vias (underneath IC) through either a net-tie or a 0Ω resistor on the bottom layer.
- Connecting a resistor from PMB_ADDR pin to AGND sets the address. Do not to have any capacitor on this pin. A capacitor on the pin likely leads to a wrong detection result for address.
- Pin 6 (DNC) is a Do-Not-Connect pin. Do not connect pin 6 to any other net including ground.
- When the device is configured with an external voltage divider, the high side resistor connects from VOSNS to VSEL/FB pins and the low side feedback resistor connects to VSEL/FB to GOSNS pins near the device.
- The return for the MSEL1 resistor, MSEL2 resistor, PMB_ADDR resistor, and VSEL/FB resistor (when using internal feedback divider) is the quiet AGND island.

8.4.2 Layout Example

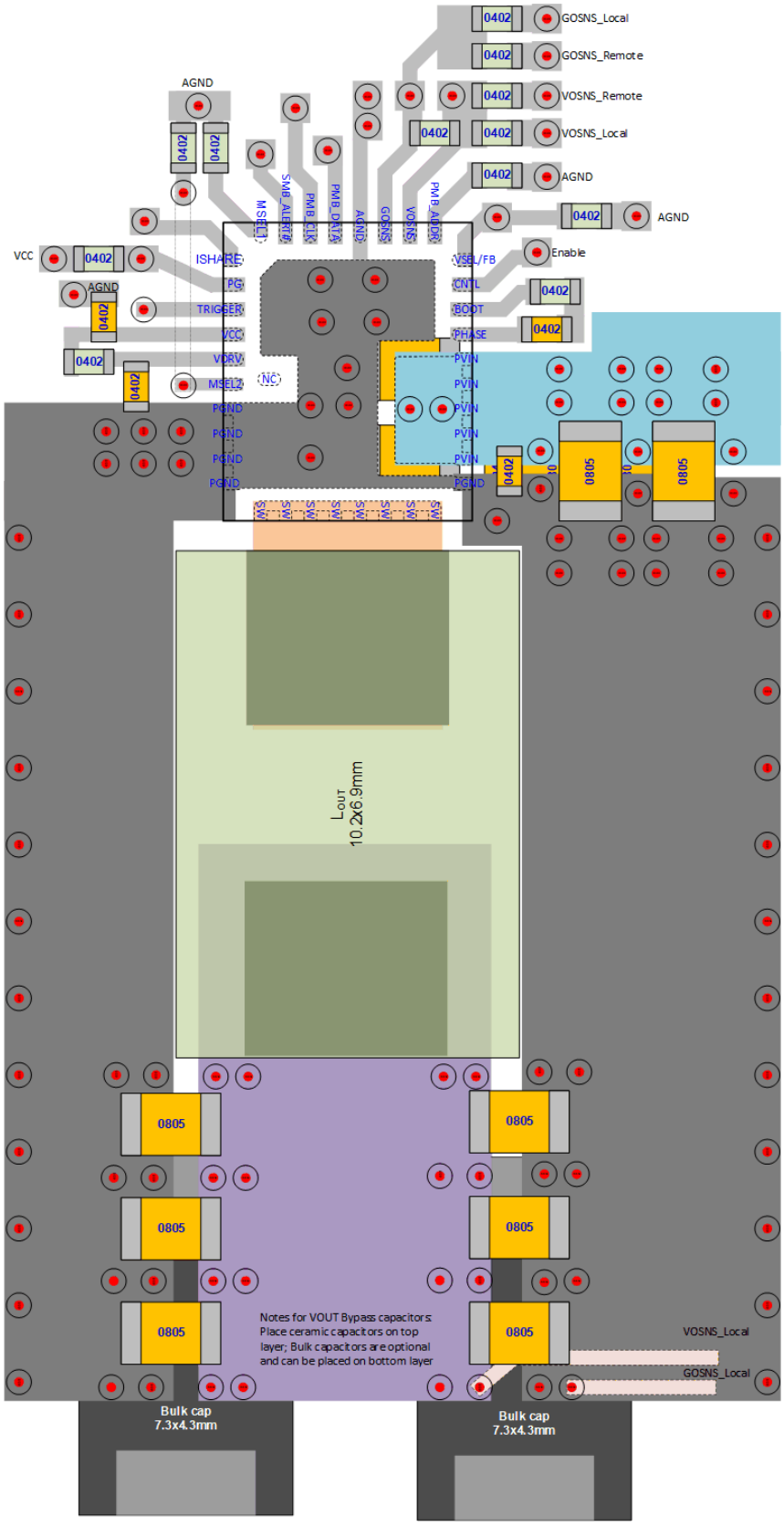


Figure 8-18. Layout Recommendation

8.4.2.1 Thermal Performance on TPS546E25EVM

The following is the thermal result captured on the EVM with PVIN = 12V, V_{OUT} = 1.2V.

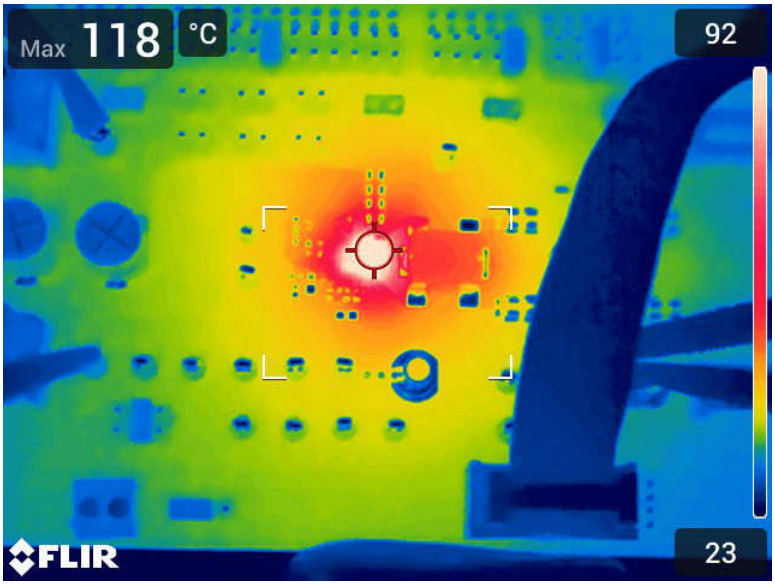


Figure 8-19. Thermal Image, 800kHz FCCM, 50A Load

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
PMBus® is a registered trademark of System Management Interface Forum (SMIF).
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2024) to Revision A (April 2025)	Page
• Changed document status from Advance Information to Production Data	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS546E25RXXR	Active	Production	WQFN-FCRLF (RXX) | 37	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T546E25
TPS546E25RXXR.A	Active	Production	WQFN-FCRLF (RXX) | 37	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T546E25

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

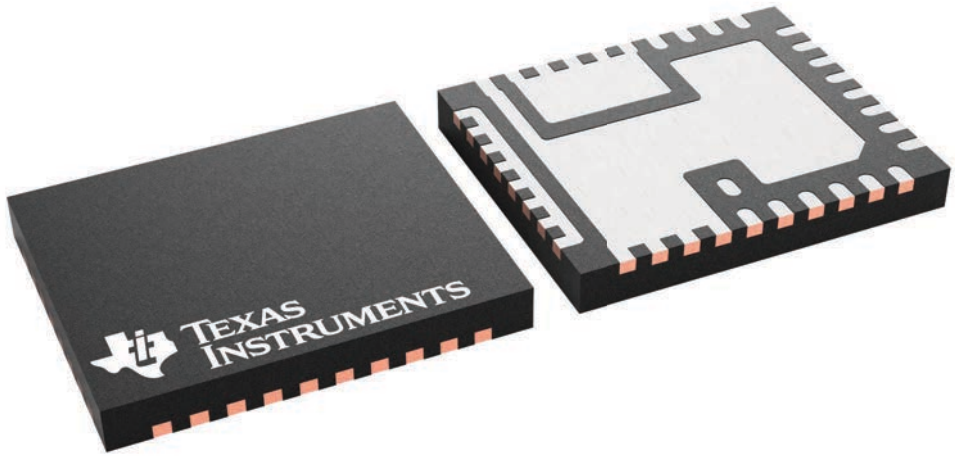
RXX 37

VQFN-FCRLF - 1.05 mm max height

5 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



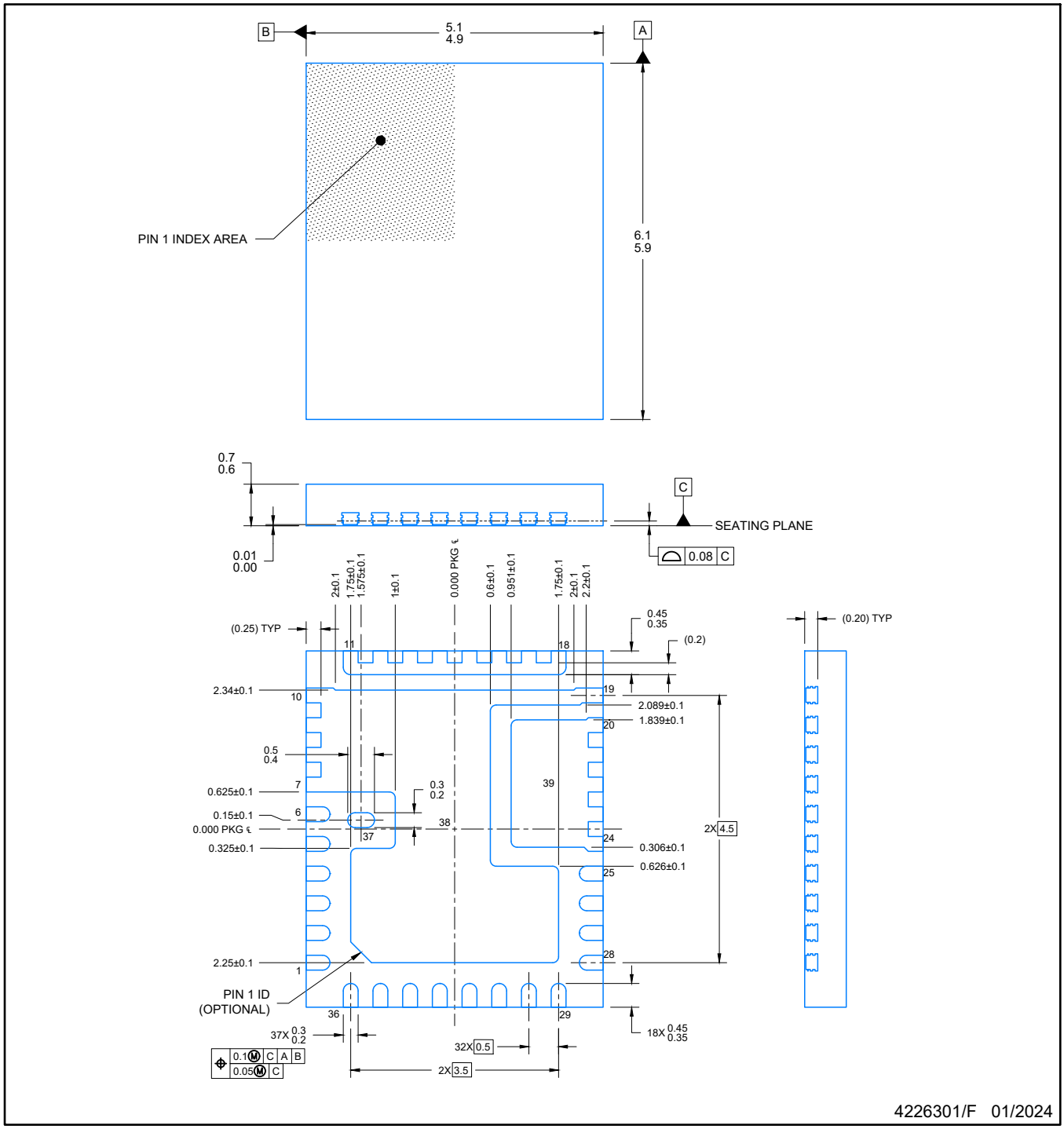
4228557/A

PACKAGE OUTLINE

RXX0037A

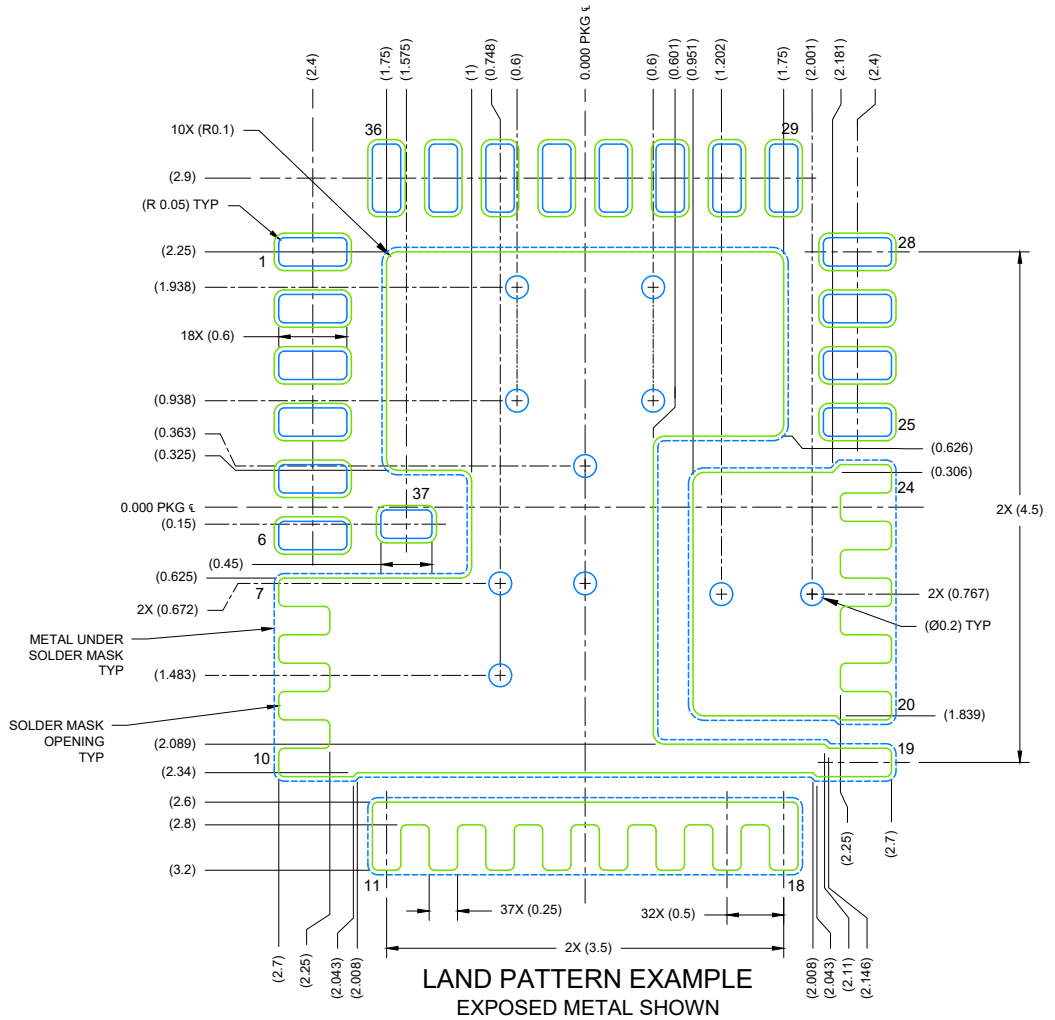
WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

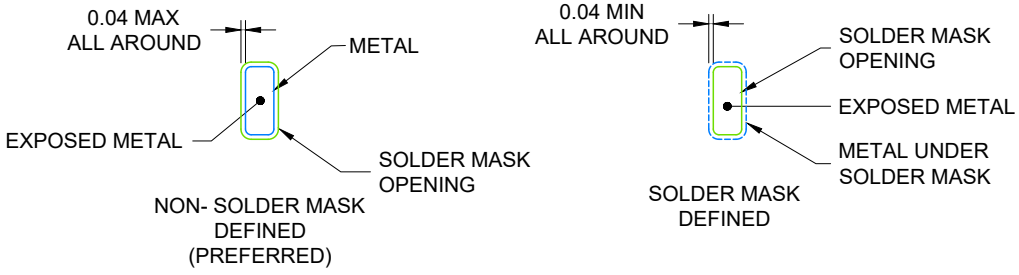
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 15X

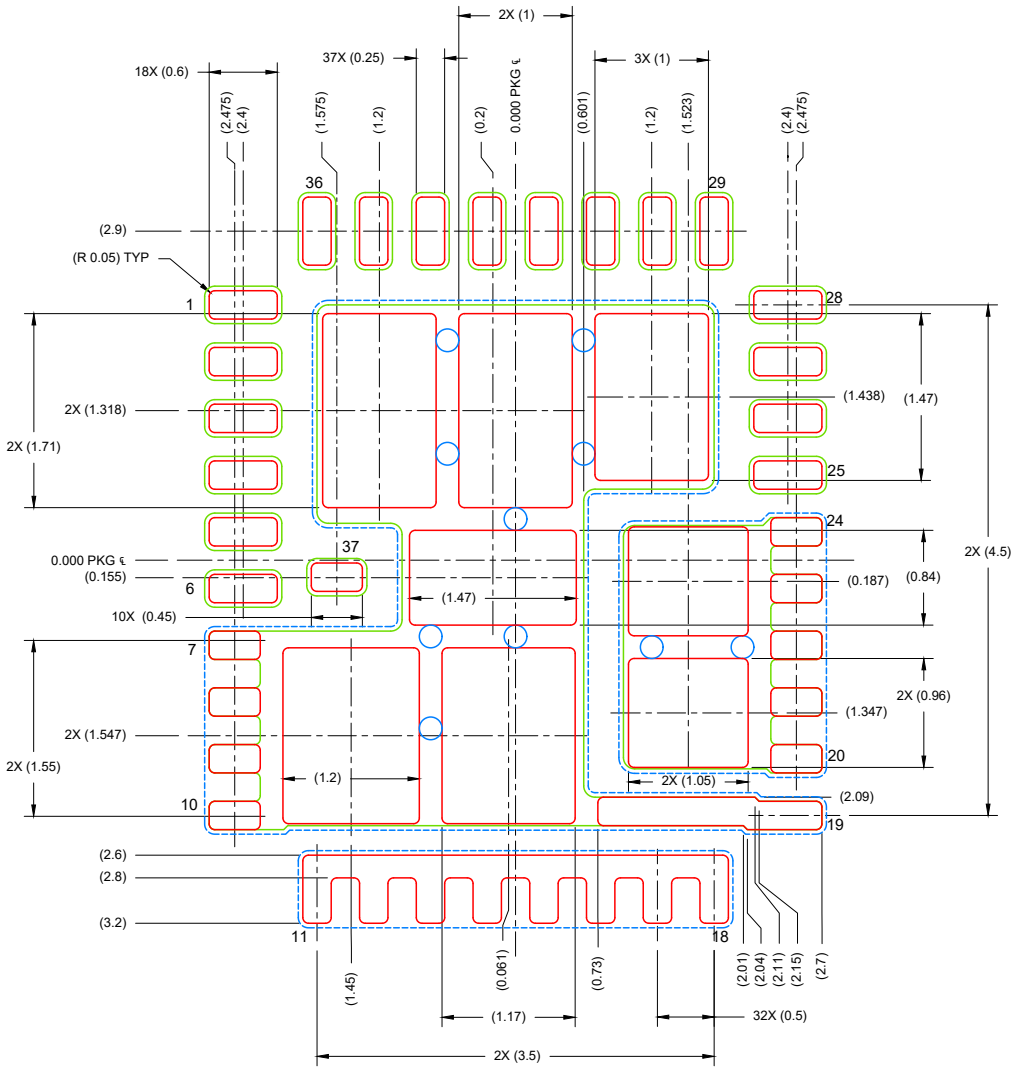


SOLDER MASK DETAILS

4226301/F 01/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
6. Recommended board layout is designed for 2oz copper for high current applications.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

SOLDER COVERAGE :
Thermal Pad connected to pin 7-10, 19 : 80%
Thermal Pad connected to pin 20-24 : 86%
SCALE: 15X

4226301/F 01/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025