# TPS55287 36-V, 4-A Buck-Boost Converter with I²C Interface

## 1 Features

- Programmable power supply (PPS) support for USB power delivery (USB PD)
  - 3.0V to 36V wide input voltage range
  - 0.8V to 22V with 10mV step programmable output voltage range
  - ±1% reference voltage accuracy
  - Adjustable output voltage compensation for voltage droop over the cable
  - Programmable output current limit with 50mA step
  - ±5% accurate output current monitoring
  - I²C interface
- High efficiency over entire load range
  - 96.7% efficiency at $V_{IN}$ = 12V, $V_{OUT}$ = 20V, and $I_{OUT}$ = 1.5A
  - Programmable PFM and FPWM mode at light load
- Avoid frequency interference and crosstalk
  - Optional clock synchronization
  - Programmable switching frequency from 200kHz to 2.2MHz
- EMI mitigation
  - Optional programmable spread spectrum
  - Lead-less package
- Rich protection features
  - Output overvoltage protection
  - Hiccup mode for output short-circuit protection
  - Thermal shutdown protection
  - 4-A average inductor current limit
- Small solution size
  - Maximum switching frequency up to 2.2MHz
  - 3.0mm × 5.0mm HotRod™ QFN package

## 2 Applications

- Wireless charger
- USB PD
- Docking station
- Industrial PC
- Power bank
- Monitor

## 3 Description

The TPS55287 is a synchronous buck-boost converter that is optimized for converting battery voltage or adapter voltage into power supply rails. The TPS55287 integrates four MOSFET switches, providing a compact solution for USB power delivery (USB PD) application.

The TPS55287 has up to 36V input voltage capability. Through the I²C interface, the output voltage of the TPS55287 can be programmed from 0.8V to 22V with 10mV step. When working in boost mode, the device can deliver 35W from a 12V input. It is capable of delivering 25W from 9V input voltage.

The TPS55287 employs an average current-mode control scheme. The switching frequency is programmable from 200kHz to 2.2MHz by an external resistor and can be synchronized to an external clock. The TPS55287 also provides optional spread spectrum to minimize peak EMI.

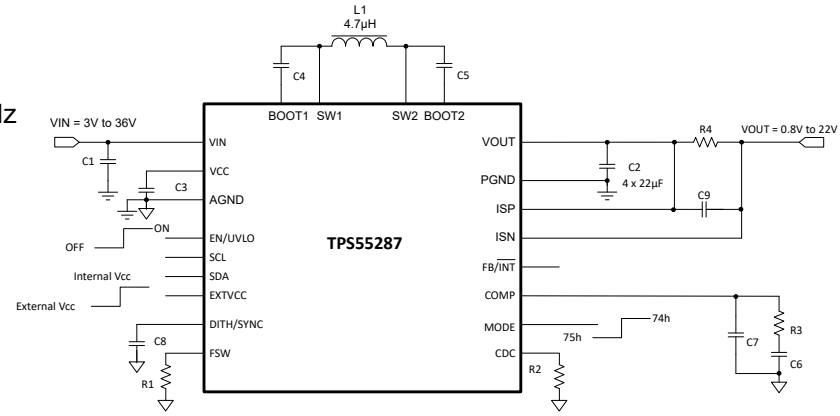
The TPS55287 offers output overvoltage protection, average inductor current limit, cycle-by-cycle peak current limit, and output short circuit protection. The TPS55287 also makes sure it safely operates with optional output current limit and hiccup-mode protection in sustained overload conditions.

The TPS55287 can use a small inductor and small capacitors with high switching frequency. It is available in a 3.0mm × 5.0mm QFN package.

**Device Information**

| PART NUMBER | PACKAGE (1) | BODY SIZE |
|---|---|---|
| TPS55287 | VQFN-HR | 3.0mm × 5.0mm |

(1) For all available packages, see the Section 12 at the end of the data sheet.




**Typical Application Circuit**

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# 4 Pin Configuration and Functions

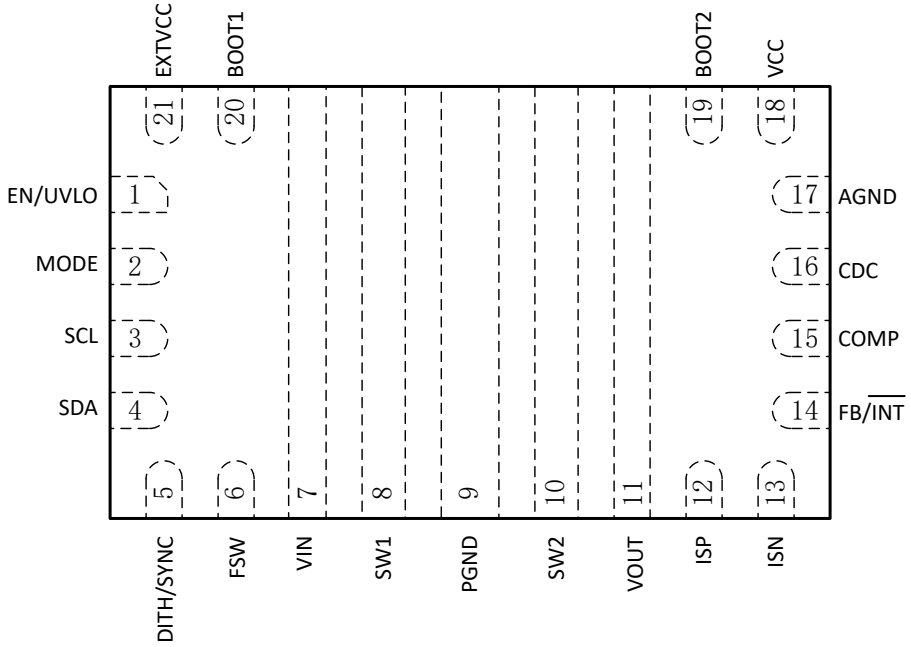



**Figure 4-1. 21-Pin VQFN-HR RYQ Package (Transparent Top View)**

**Table 4-1. Pin Functions**

| Pin | | I/O | Description |
|---|---|---|---|
| Name | NO. | | |
| EN/UVLO | 1 | I | Enable logic input and programmable input voltage undervoltage lockout (UVLO) input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode. After the voltage at the EN/UVLO pin is above the logic high voltage of 1.15 V, this pin acts as programmable UVLO input with 1.23-V internal reference. |
| MODE | 2 | I | $I^2C$ target address selection. When it is connected to the logic high voltage, the $I^2C$ target address is 74H. When it is connected to the logic low voltage, the $I^2C$ target address is 75H. |
| SCL | 3 | I | Clock of $I^2C$ interface |
| SDA | 4 | I/O | Data of $I^2C$ interface |
| DITH/SYNC | 5 | I | Dithering frequency setting and synchronous clock input. Use a capacitor between this pin and ground to set the dithering frequency. When this pin is short to ground or pulled above 1.2 V, there is no dithering function. An external clock can be applied at this pin to synchronize the switching frequency. |
| FSW | 6 | I | The switching frequency is programmed by a resistor between this pin and the AGND pin. |
| VIN | 7 | PWR | Input of the buck-boost converter |
| SW1 | 8 | PWR | The switching node pin of the buck side. It is connected to the drain of the internal buck low-side power MOSFET and the source of internal buck high-side power MOSFET. |
| PGND | 9 | PWR | Power ground of the IC |
| SW2 | 10 | PWR | The switching node pin of the boost side. It is connected to the drain of the internal boost low-side power MOSFET and the source of internal boost high-side power MOSFET. |
| VOUT | 11 | PWR | Output of the buck-boost converter |
| ISP | 12 | I | Positive input of the current sense amplifier. An optional current sense resistor connected between the ISP pin and the ISN pin can limit the output current. If the sensed voltage reaches the current limit setting value in the register, a slow constant current control loop becomes active and starts to regulate the voltage between the ISP pin and the ISN pin. Connecting the ISP pin and the ISN pin together with the VOUT pin can disable the output current limit function. |

**Table 4-1. Pin Functions (continued)**

| Pin | | I/O | Description |
|---|---|---|---|
| Name | NO. | | |
| ISN | 13 | I | Negative input of the current sense amplifier. An optional current sense resistor connected between the ISP pin and the ISN pin can limit the output current. If the sensed voltage reaches the current limit setting value in the register, a slow constant current control loop becomes active and starts to regulate the voltage between the ISP pin and the ISN pin. Connecting the ISP pin and the ISN pin together with the VOUT pin can disable the output current limit function. |
| FB/$\overline{\text{INT}}$ | 14 | I/O | When the device is set to use external output voltage feedback, connect to the center tap of a resistor divider to program the output voltage. When the device is set to use internal feedback, this pin is a fault indicator output. When there is an internal fault happening, this pin outputs logic low level. |
| COMP | 15 | O | Output of the internal error amplifier. Connect the loop compensation network between this pin and the AGND pin. |
| CDC | 16 | O | Voltage output proportional to the sensed voltage between the ISP pin and the ISN pin. Use a resistor between this pin and AGND to increase the output voltage to compensate voltage droop across the cable caused by the cable resistance. |
| AGND | 17 | — | Signal ground of the IC |
| VCC | 18 | O | Output of the internal regulator. A ceramic capacitor of more than 4.7 µF is required between this pin and the AGND pin. |
| BOOT2 | 19 | O | Power supply for high-side MOSFET gate driver in boost side. A 0.1-µF ceramic capacitor must be connected between this pin and the SW2 pin. |
| BOOT1 | 20 | O | Power supply for high-side MOSFET gate driver in buck side. A 0.1-µF ceramic capacitor must be connected between this pin and the SW1 pin. |
| EXTVCC | 21 | I | Select the internal LDO or external 5 V for VCC. When it is connected to logic high voltage, select the internal LDO. When it is connected to logic low voltage, select the external 5 V for VCC. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over the recommended operating junction temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage range at terminals (2) | VIN, SW1 | –0.3 | 42 | V |
| | BOOT1 | SW1–0.3 | SW1+6 | V |
| | VCC, SCL, SDA, FSW, COMP, FB/$\overline{\text{INT}}$, MODE, CDC, DITH/SYNC, EXTVCC | –0.3 | 6 | V |
| | VOUT, SW2, ISP, ISN | –0.3 | 25 | V |
| | EN | -0.3 | 20 | V |
| | BOOT2 | SW2–0.3 | SW2+6 | V |
| | SCL, SDA, FSW, COMP, FB/$\overline{\text{INT}}$, MODE, CDC, DITH/SYNC, EXTVCC | –0.3 | VCC+0.3 | V |
| $T_J$ | Operating Junction, $T_J$ (3) | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011, all pins(2) | ±500 | |

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | 3.0 | | 36 | V |
| $V_{OUT}$ | Output voltage range | 0.8 | | 22 | V |
| L | Effective inductance range | 1 | 4.7 | 10 | µH |
| $C_{IN}$ | Effective input capacitance range | 4.7 | 22 | | µF |
| $C_{OUT}$ | Effective output capacitance range | 10 | 100 | 1000 | µF |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | RYQ (VQFN) 21 PINS Standard | RYQ (VQFN) 21 PINS EVM (2) | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 43.4 | 27.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 22.3 | N/A | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 7.4 | N/A | °C/W |

| THERMAL METRIC(1) | | RYQ (VQFN) 21 PINS Standard | RYQ (VQFN) 21 PINS EVM (2) | UNIT |
|---|---|---|---|---|
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.7 | 0.7 | °C/W |
| $Y_{JB}$ | Junction-to-board characterization parameter | 7.2 | 11.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Measured on TPS55287Q1EVM-085, 4-layer, 2-oz/1-oz/1-oz/2-oz copper 91-mmx66-mm PCB.

## 5.5 Electrical Characteristics

$T_J$ = -40°C to 125°C, $V_{IN}$ = 12 V and $V_{OUT}$ = 20 V. Typical values are at $T_J$ = 25°C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $V_{IN}$ | Input voltage range | | 3.0 | | 36 | V |
| $V_{VIN\_UVLO}$ | Under voltage lockout threshold | $V_{IN}$ rising | 2.8 | 2.9 | 3.0 | V |
| | | $V_{IN}$ falling | 2.6 | 2.65 | 2.7 | V |
| $I_Q$ | Quiescent current into VIN pin | IC enabled, no load, no switching. $V_{IN}$ = 3.0V to 24V, $V_{OUT}$ = 0.8V, $V_{FB}$ = $V_{REF}$ + 0.1V, $R_{FSW}$ = 100kΩ | | 760 | 860 | µA |
| | Quiescent current into VOUT pin | IC enabled, no load, no switching. $V_{IN}$ = 3.0V, $V_{OUT}$ = 3V to 20V, $V_{FB}$ = $V_{REF}$ + 0.1V, $R_{FSW}$ = 100kΩ | | 760 | 860 | µA |
| $I_{SD}$ | Shutdown current into VIN pin | IC disabled, $V_{IN}$ = 3.0V to 14V, $T_J$ up to 125°C, EXTVCC pin floating | | 0.8 | 3 | µA |
| $V_{CC}$ | Internal regulator output | $I_{VCC}$ = 50mA, $V_{IN}$ = 8V, $V_{OUT}$ = 20V | 5.0 | 5.2 | 5.4 | V |
| **EN/UVLO** | | | | | | |
| $V_{EN\_H}$ | EN Logic high threshold | $V_{CC}$ = 3.0V to 5.5V | | | 1.15 | V |
| $V_{EN\_L}$ | EN Logic low threshold | $V_{CC}$ = 3.0V to 5.5V | 0.4 | | | V |
| $V_{EN\_HYS}$ | Enable threshold hysteresis | $V_{CC}$ = 3.0V to 5.5V | 0.04 | | | V |
| $V_{UVLO}$ | UVLO rising threshold at the EN/UVLO pin | $V_{CC}$ = 3.0V to 5.5V | 1.20 | 1.23 | 1.26 | V |
| $V_{UVLO\_HYS}$ | UVLO threshold hysteresis | $V_{CC}$ = 3.0V to 5.5V | | 10 | | mV |
| $I_{UVLO}$ | Sourcing current at the EN/UVLO pin | $V_{EN/UVLO}$ = 1.3V | 4.4 | 5 | 5.6 | µA |
| **OUTPUT** | | | | | | |
| $V_{OUT}$ | Output voltage range | | 0.8 | | 22 | V |
| $V_{OVP}$ | Output overvoltage protection threshold | | 22.5 | 23.5 | 24.5 | V |
| $V_{OVP\_HYS}$ | Overvoltage protection hysteresis | | | 1 | | V |
| $I_{FB\_LKG}$ | Leakage current at FB pin | $T_J$ up to 125°C | | | 100 | nA |
| $I_{VOUT\_LKG}$ | Leakage current into VOUT pin | IC disabled, $V_{OUT}$ = 20V, $V_{SW2}$ = 0V, $T_J$ up to 125°C | | 1 | 20 | µA |
| $I_{DISCHG}$ | Output discharge current | $V_{OUT}$ = 20V, $V_{CC}$ = 5.2V | 40 | 100 | 170 | mA |
| **INTERNAL REFERENCE DAC** | | | | | | |

$T_J$ = -40°C to 125°C, $V_{IN}$ = 12 V and $V_{OUT}$ = 20 V. Typical values are at $T_J$ = 25°C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OUT\_FULL}$ | Output voltage when $V_{REF}$ is set to 1.129V | VOUT_FS = 03h, REF = 0780h, $V_{REF}$ = 1.129V | 19.7 | 20 | 20.3 | V |
| | | VOUT_FS = 02h, REF = 0780h, $V_{REF}$ = 1.129V | 14.78 | 15 | 15.22 | V |
| | | VOUT_FS = 01h, REF = 0780h, $V_{REF}$ = 1.129V | 9.85 | 10 | 10.15 | V |
| | | VOUT_FS = 00h, REF = 0780h, $V_{REF}$ = 1.129V | 4.93 | 5 | 5.07 | V |
| $V_{OUT\_ZERO}$ | Output voltage when $V_{REF}$ is set to 45mV | VOUT_FS = 03h, REF = 0000h, $V_{REF}$ = 45mV | 0.74 | 0.8 | 0.86 | V |
| | | VOUT_FS = 02h, REF = 0000h, $V_{REF}$ = 45mV | 0.55 | 0.6 | 0.65 | V |
| | | VOUT_FS = 01h, REF = 0000h, $V_{REF}$ = 45mV | 0.36 | 0.4 | 0.44 | V |
| | | VOUT_FS = 00h, REF = 0000h, $V_{REF}$ = 45mV | 0.18 | 0.2 | 0.22 | V |
| **REFERENCE VOLTAGE** | | | | | | |
| $V_{REF}$ | Reference voltage at the FB/$\overline{INT}$ pin when using external feedback | External feedback with REF = 0780h | 1.117 | 1.129 | 1.141 | V |
| | | External feedback with REF = 058Ch | 0.837 | 0.846 | 0.855 | V |
| | | External feedback with REF = 0334h | 0.502 | 0.508 | 0.514 | V |
| | | External feedback with REF = 01A4h | 0.276 | 0.282 | 0.288 | V |
| **POWER SWITCH** | | | | | | |
| $R_{DS(on)}$ | Low-side MOSFET on resistance at buck side | $V_{OUT}$ = 20V, $V_{CC}$ = 5.2V | | 22 | | mΩ |
| | High-side MOSFET on resistance at buck side | $V_{OUT}$ = 20V, $V_{CC}$ = 5.2V | | 14 | | mΩ |
| | Low-side MOSFET on resistance at boost side | $V_{OUT}$ = 20V, $V_{CC}$ = 5.2V | | 11 | | mΩ |
| | High-side MOSFET on resistance at boost side | $V_{OUT}$ = 20V, $V_{CC}$ = 5.2V | | 11 | | mΩ |
| **INTERNAL CLOCK** | | | | | | |
| $f_{SW}$ | Switching frequency | $R_{FSW}$ = 100k | 180 | 200 | 220 | kHz |
| | | $R_{FSW}$ = 8.4k | 2000 | 2200 | 2400 | kHz |
| $t_{OFF\_min}$ | Minimum off time | Boost mode | | 90 | 145 | ns |
| $t_{ON\_min}$ | Minimum on time | Buck mode | | 90 | 130 | ns |
| $V_{SW}$ | Voltage at the FSW pin | | | 1 | | V |
| **CURRENT LIMIT** | | | | | | |
| $I_{LIM\_AVG}$ | Average inductor current limit | $V_{IN}$ = 8V, $V_{OUT}$ = 20V, $F_{SW}$ = 400kHz | 3.3 | 4 | 4.8 | A |
| $I_{LIM\_PK\_H}$ | Peak inductor current limit at boost high side | $V_{IN}$ = 8V, $V_{OUT}$ = 20V, $F_{SW}$ = 400kHz | | 6.7 | | A |
| $I_{LIM\_PK\_L}$ | Peak inductor current limit at boost low side | $V_{IN}$ = 8V, $V_{OUT}$ = 20V, $F_{SW}$ = 400kHz | | 6.5 | | A |
| $V_{SNS}$ | Current loop regulation voltage between ISP and ISN pin | $V_{ISN}$ = 2V to 21V, IOUT_LIMIT Register = 10111100b | 28.5 | 30 | 31.5 | mV |
| | | $V_{ISN}$ = 2V to 21V, IOUT_LIMIT Register = 11100100b | 48 | 50 | 52 | mV |
| **CABLE VOLTAGE DROOP COMPENSATION** | | | | | | |
| $V_{CDC}$ | Voltage at the CDC pin | $R_{CDC}$ = 20kΩ or floating, $V_{ISP}$ – $V_{ISN}$ = 50mV | 0.95 | 1 | 1.05 | V |
| | | $R_{CDC}$ = 20kΩ or floating, $V_{ISP}$ – $V_{ISN}$ = 2mV | | 40 | 75 | mV |

$T_J$ = -40°C to 125°C, $V_{IN}$ = 12 V and $V_{OUT}$ = 20 V. Typical values are at $T_J$ = 25°C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OUT\_CDC}$ | VOUT increase for cable droop compensation | Internal output feedback, CDC[2:0] = 111, $V_{ISP} – V_{ISN}$ = 50mV | 640 | 700 | 750 | mV |
| | | Internal output feedback, CDC[2:0] = 111, $V_{ISP} – V_{ISN}$ = 2mV | | 30 | 60 | mV |
| | | Internal output feedback, CDC[2:0] = 001, $V_{ISP} – V_{ISN}$ = 50mV | 70 | 100 | 130 | mV |
| | | Internal output feedback, CDC[2:0] = 001, $V_{ISP} – V_{ISN}$ = 10mV | | 20 | 40 | mV |
| $I_{FB\_CDC}$ | FB/$\overline{INT}$ pin sinking current | External output feedback, $R_{CDC}$ = 20kΩ, $V_{ISP} – V_{ISN}$ = 50mV | 7.23 | 7.5 | 7.87 | µA |
| | | External output feedback, $R_{CDC}$ = 20kΩ, $V_{ISP} – V_{ISN}$ = 0mV | | 0 | 0.3 | µA |
| | | External output feedback, $R_{CDC}$ = floating, $V_{ISP} – V_{ISN}$ = 50mV | | 0 | 0.3 | µA |
| **ERROR AMPLIFIER** | | | | | | |
| $I_{SINK}$ | COMP pin sink current | $V_{FB}$ = $V_{REF}$ + 400mV, $V_{COMP}$ = 1.5V, $V_{CC}$=5V | | 20 | | µA |
| $I_{SOURCE}$ | COMP pin source current | $V_{FB}$ = $V_{REF}$ - 400mV, $V_{COMP}$ = 1.5V, $V_{CC}$=5V | | 60 | | µA |
| $V_{CCLPH}$ | High clamp voltage at the COMP pin | FPWM mode, VOUT = 1.8V to 22V | | 1.3 | | V |
| $V_{CCLPL}$ | Low clamp voltage at the COMP pin | FPWM mode, VOUT = 1.8V to 22V | | 0.7 | | V |
| $G_{EA}$ | Error amplifier transconductance | | | 190 | | µA/V |
| **SOFT START** | | | | | | |
| $t_{SS}$ | Soft-start time | | 2.5 | 3.6 | 5 | ms |
| **SPREAD SPECTRUM** | | | | | | |
| $I_{DITH\_CHG}$ | Dithering charge current | $V_{DITH/SYNC}$ = 1.0V, $R_{FSW}$ = 49.9kΩ, voltage rising from 0.9V | | 2 | | µA |
| $I_{DITH\_DIS}$ | Dithering discharge current | $V_{DITH/SYNC}$ = 1.0V, $R_{FSW}$ = 49.9kΩ, voltage falling from 1.1V | | 2 | | µA |
| $V_{DITH\_H}$ | Dithering high threshold | | | 1.07 | | V |
| $V_{DITH\_L}$ | Dithering low threshold | | | 0.93 | | V |
| **SYNCHRONOUS CLOCK** | | | | | | |
| $V_{SNYC\_H}$ | Sync clock high voltage threshold | | | | 1.2 | V |
| $V_{SYNC\_L}$ | Sync clock low voltage threshold | | 0.4 | | | V |
| $t_{SYNC\_MIN}$ | Minimum sync clock pulse width | | 50 | | | ns |
| **HICCUP** | | | | | | |
| $t_{HICCUP}$ | Hiccup off time | | | 76 | | ms |
| **MODE** | | | | | | |
| $V_{MODE}$ | MODE logic high threshold | $V_{CC}$ = 3.0V to 5.5V | | | 1.2 | V |
| $V_{MODE}$ | MODE logic low threshold | $V_{CC}$ = 3.0V to 5.5V | 0.4 | | | V |
| **EXTVCC** | | | | | | |
| $V_{EXTVCC}$ | EXTVCC Logic high threshold | $V_{CC}$ = 3.0V to 5.5V | | | 1.2 | V |
| $V_{EXTVCC}$ | EXTVCC Logic Low threshold | $V_{CC}$ = 3.0V to 5.5V | 0.4 | | | V |
| **LOGIC INTERFACE** | | | | | | |
| $V_{I2C\_IO}$ | IO voltage range for $I^2C$ | | 1.7 | | 5.5 | V |
| $V_{I2C\_H}$ | $I^2C$ input high threshold | $V_{CC}$ = 3.0V to 5.5V | | | 1.2 | V |
| $V_{I2C\_L}$ | $I^2C$ input low threshold | $V_{CC}$ = 3.0V to 5.5V | 0.4 | | | V |
| $I_{FB/\overline{INT}\_H}$ | Leakage current into FB/$\overline{INT}$ pin when outputting high impedance | $V_{FB/\overline{INT}}$ = 5V | | | 100 | nA |

$T_J$ = -40°C to 125°C, $V_{IN}$ = 12 V and $V_{OUT}$ = 20 V. Typical values are at $T_J$ = 25°C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{FB/\overline{INT}\_L}$ | Output low voltage range of the FB/$\overline{INT}$ pin | Sinking 4mA current | | 0.03 | 0.1 | V |
| **PROTECTION** | | | | | | |
| $T_{SD}$ | Thermal shutdown threshold | $T_J$ rising | | 175 | | °C |
| $T_{SD\_HYS}$ | Thermal shutdown hysteresis | $T_J$ falling below Tsd | | 20 | | °C |

## 5.6 I²C Timing Characteristics

$T_J$ = -40°C to 125°C, $V_{IN}$ = 12 V and $V_{OUT}$ = 20 V. Typical values are at $T_J$ = 25°C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **I²C TIMING** | | | | | | |
| $f_{SCL}$ | SCL clock frequency | | 100 | | 1000 | kHz |
| $t_{BUF}$ | Bus free time between a STOP and START condition | Fast mode plus | 0.5 | | | µs |
| $t_{HD(STA)}$ | Hold time (repeated) START condition | | 260 | | | ns |
| $t_{LOW}$ | Low period of the SCL clock | | 0.5 | | | µs |
| $t_{HIGH}$ | High period of the SCL clock | | 260 | | | ns |
| $t_{SU(STA)}$ | Setup time for a repeated START condition | | 260 | | | ns |
| $t_{SU(DAT)}$ | Data setup time | | 50 | | | ns |
| $t_{HD(DAT)}$ | Data hold time | | 0 | | | µs |
| $t_{RCL}$ | Rise time of SCL signal | | | | 120 | ns |
| $t_{RCL1}$ | Rise time of SCL signal after a repeated START condition and after an ACK bit | | | | 120 | ns |
| $t_{FCL}$ | Fall time of SCL signal | | | | 120 | ns |
| $t_{RDA}$ | Rise time of SDA signal | | | | 120 | ns |
| $t_{FDA}$ | Fall time of SDA signal | | | | 120 | ns |
| $t_{SU(STO)}$ | Setup time of STOP condition | | 260 | | | ns |
| $C_B$ | Capacitive load for SDA and SCL | | | | 200 | pF |

## 5.7 Typical Characteristics

$V_{IN}$ = 12 V, $T_A$ = 25°C, unless otherwise noted

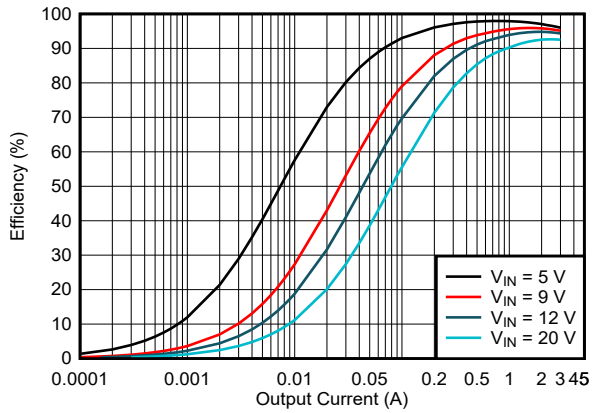



**Figure 5-1. Efficiency vs Output Current, $V_{OUT}$ = 5 V, $f_{SW}$ = 400 kHz, FPWM**

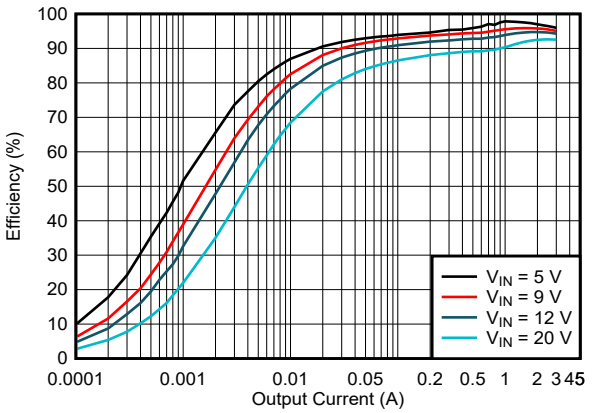



**Figure 5-2. Efficiency vs Output Current, $V_{OUT}$ = 5 V, $f_{SW}$ = 400 kHz, PFM**

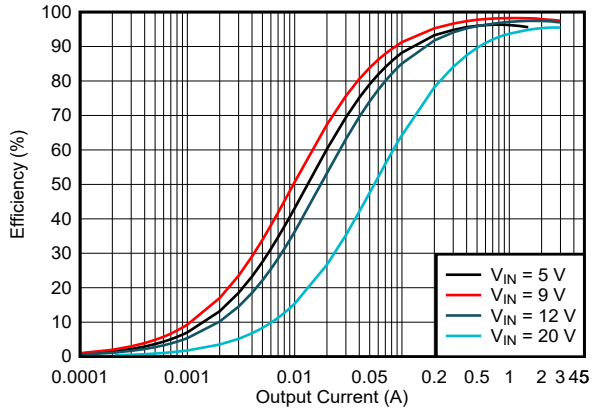



**Figure 5-3. Efficiency vs Output Current, $V_{OUT}$ = 9 V, $f_{SW}$ = 400 kHz, FPWM**

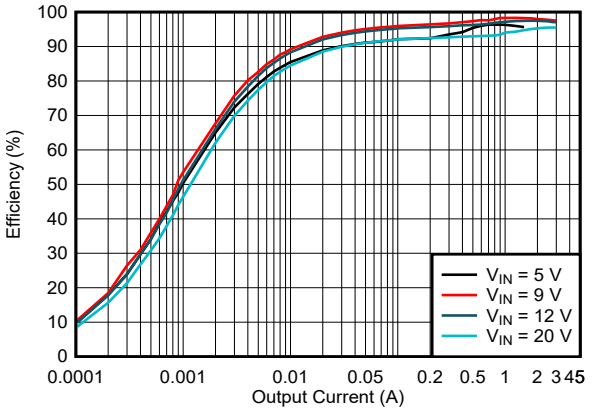



**Figure 5-4. Efficiency vs Output Current, $V_{OUT}$ = 9 V, $f_{SW}$ = 400 kHz, PFM**

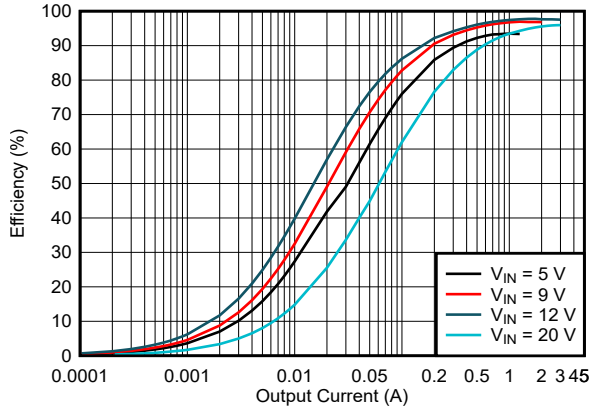



**Figure 5-5. Efficiency vs Output Current, $V_{OUT}$ = 12 V, $f_{SW}$ = 400 kHz, FPWM**

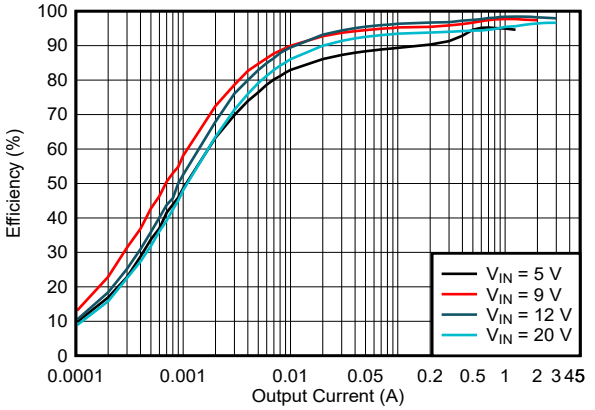



**Figure 5-6. Efficiency vs Output Current, $V_{OUT}$ = 12 V, $f_{SW}$ = 400 kHz, PFM**

## 5.7 Typical Characteristics (continued)

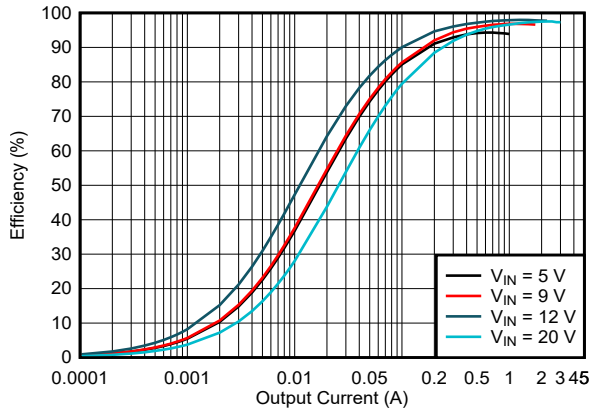



**Figure 5-7. Efficiency vs Output Current, $V_{OUT}$ = 15 V, $f_{SW}$ = 400 kHz, FPWM**

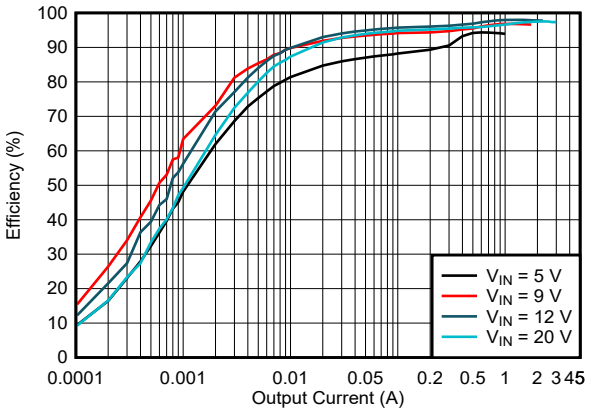



**Figure 5-8. Efficiency vs Output Current, $V_{OUT}$ = 15 V, $f_{SW}$ = 400 kHz, PFM**

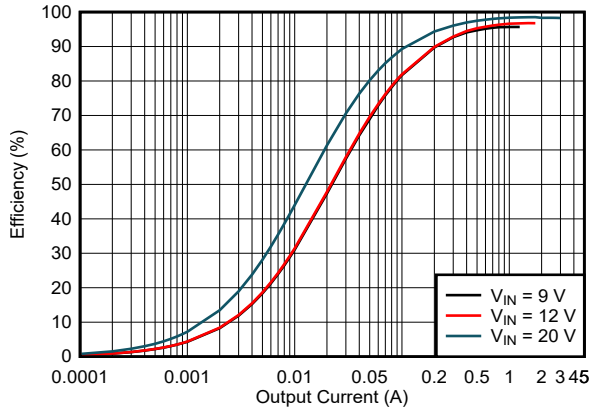



**Figure 5-9. Efficiency vs Output Current, $V_{OUT}$ = 20 V, $f_{SW}$ = 400 kHz, FPWM**

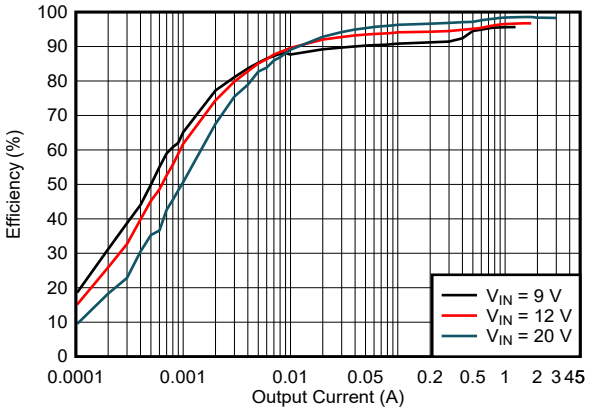



**Figure 5-10. Efficiency vs Output Current, $V_{OUT}$ = 20 V, $f_{SW}$ = 400 kHz, PFM**

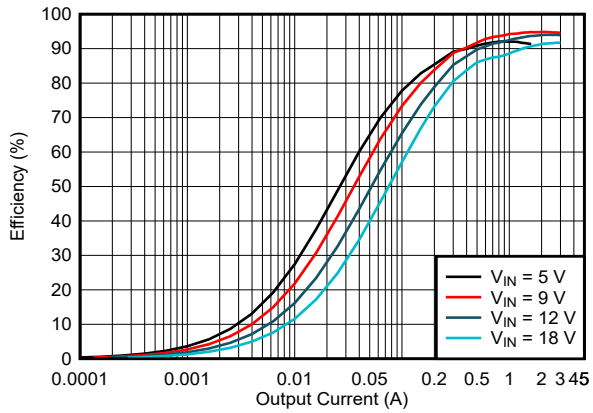



**Figure 5-11. Efficiency vs Output Current, $V_{OUT}$ = 9 V, $f_{SW}$ = 2 MHz, FPWM**

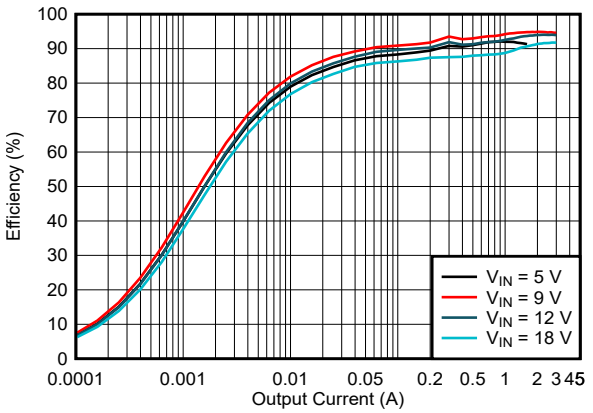



**Figure 5-12. Efficiency vs Output Current, $V_{OUT}$ = 9 V, $f_{SW}$ = 2 MHz, PFM**

## 5.7 Typical Characteristics (continued)

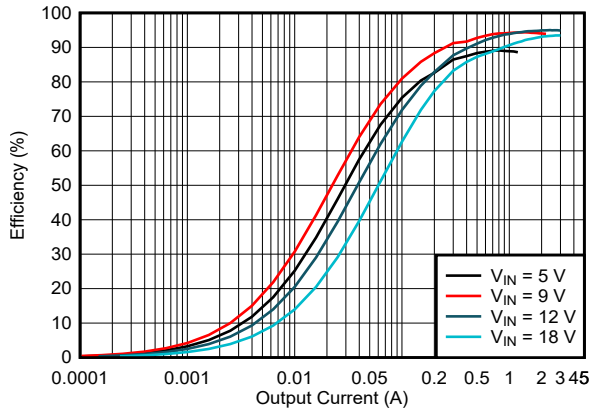



**Figure 5-13. Efficiency vs Output Current, $V_{OUT}$ = 12 V, $f_{SW}$ = 2 MHz, FPWM**

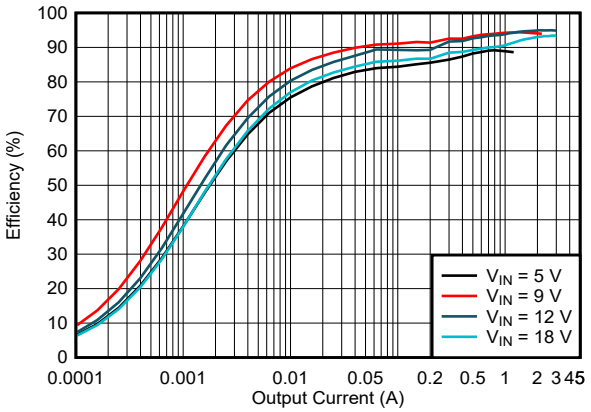



**Figure 5-14. Efficiency vs Output Current, $V_{OUT}$ = 12 V, $f_{SW}$ = 2 MHz, PFM**

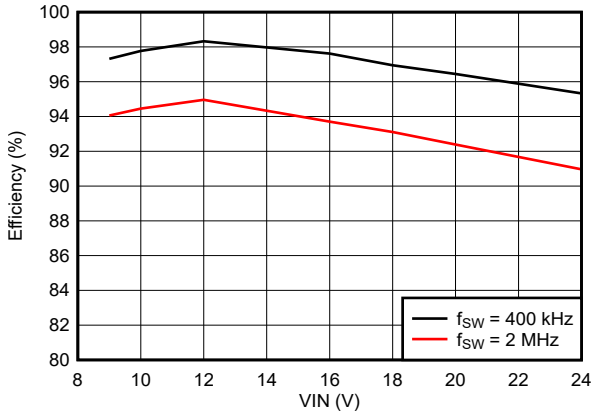



**Figure 5-15. Efficiency vs Input Voltage, $V_{OUT}$ = 12 V, $I_{OUT}$ = 2A, FPWM**

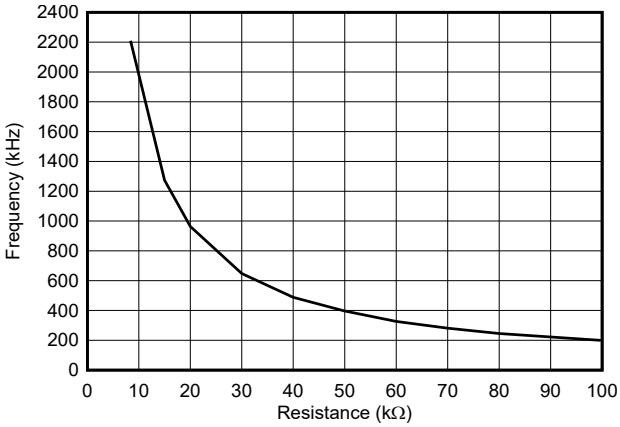



**Figure 5-16. Switching Frequency vs Setting Resistance**

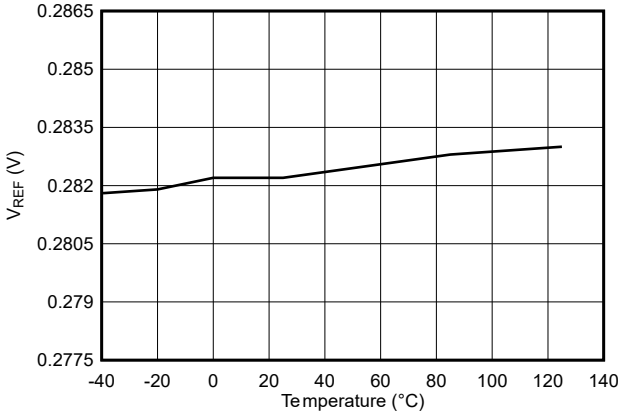



**Figure 5-17. Reference Voltage vs Temperature ($V_{REF}$ = 0.282V)**

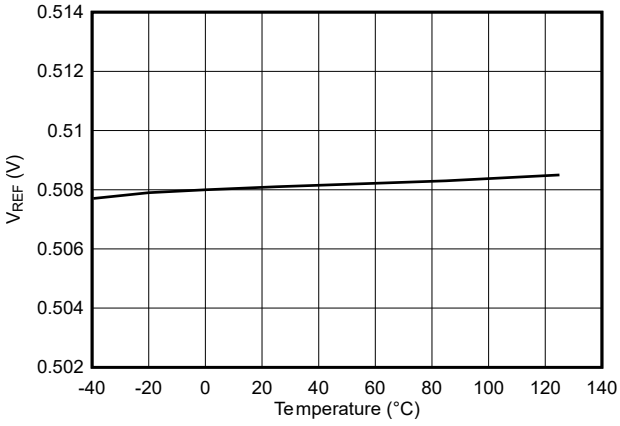



**Figure 5-18. Reference Voltage vs Temperature ($V_{REF}$ = 0.508V)**

## 5.7 Typical Characteristics (continued)

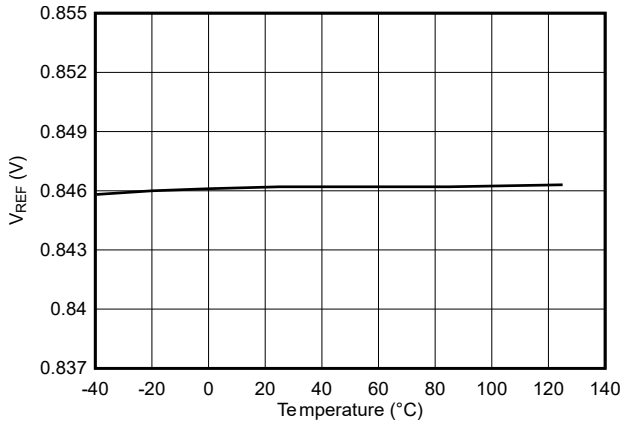



**Figure 5-19. Reference Voltage vs Temperature ($V_{REF}$ = 0.846V)**

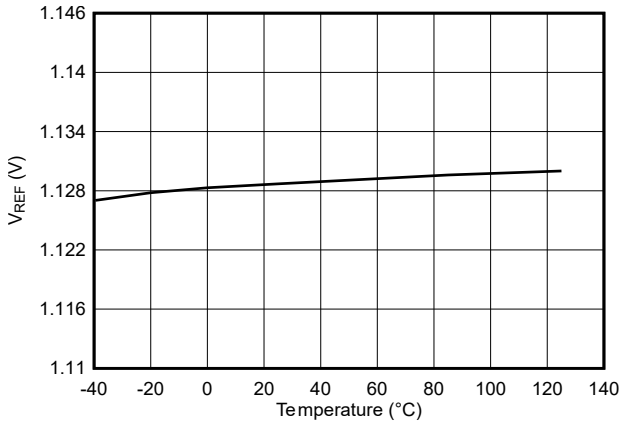



**Figure 5-20. Reference Voltage vs Temperature ($V_{REF}$ = 1.129V)**

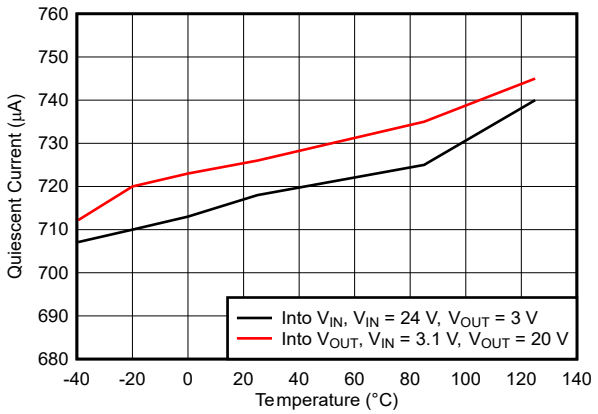



**Figure 5-21. Quiescent Current vs Temperature**

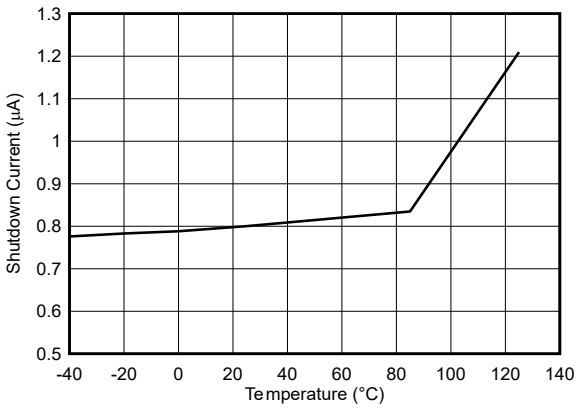



**Figure 5-22. Shutdown Current vs Temperature**

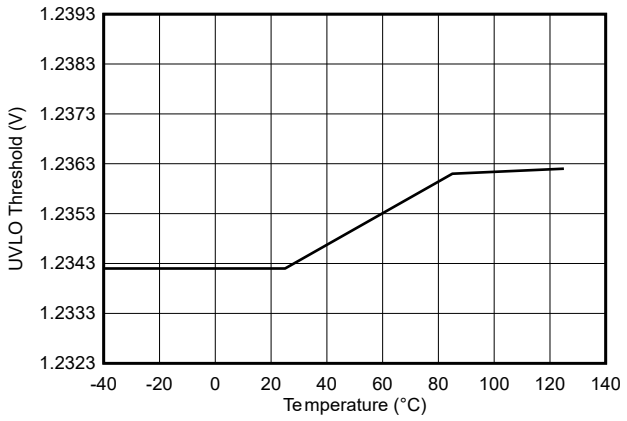



**Figure 5-23. ENABLE/UVLO Rising Threshold vs Temperature**

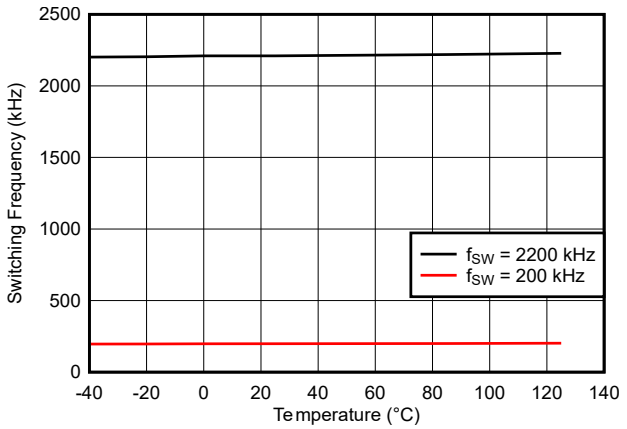



**Figure 5-24. Switching Frequency vs Temperature**

## 5.7 Typical Characteristics (continued)

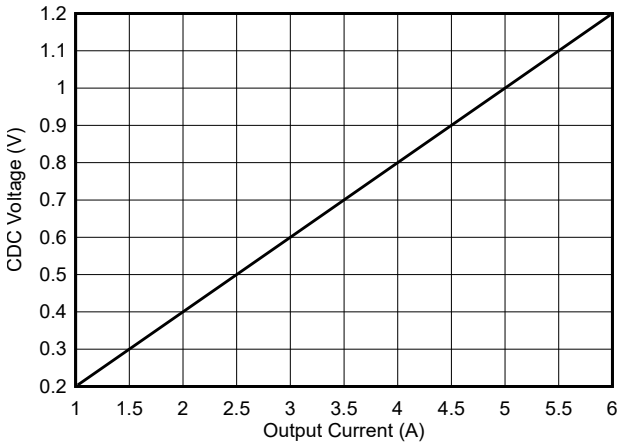



**Figure 5-25. CDC Voltage vs Output Current with $R_{SENSE}$ = 10mΩ**

# 6 Detailed Description

## 6.1 Overview

The TPS55287 is a 4A buck-boost DC-to-DC converter with the four integrated MOSFETs. The TPS55287 can operate over a wide range of 3.0V to 36V input voltage and 0.8V to 22V output voltage. The device can smoothly transition amongst buck mode, buck-boost mode, and boost mode according to the input voltage and the set output voltage. The TPS55287 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS55287 alternates between one-cycle buck mode and one-cycle boost mode.

The TPS55287 uses an average current mode control scheme. Current mode control provides simplified loop compensation, rapid response to the load transients, and inherent line voltage rejection. An error amplifier compares the feedback voltage with the internal reference voltage. The output of the error amplifier determines the average inductor current.

An internal oscillator can be configured to operate over a wide range of frequency from 200kHz to 2.2MHz. The internal oscillator can also synchronize to an external clock applied to the DITH/SYNC pin. To minimize EMI, the TPS55287 can dither the switching frequency at ±7% of the set frequency.

The TPS55287 works in fixed-frequency PWM mode at moderate to heavy load currents. In light load condition, the TPS55287 can be configured to automatically transition to PFM mode or be forced in PWM mode by setting the corresponding bit in an internal register.

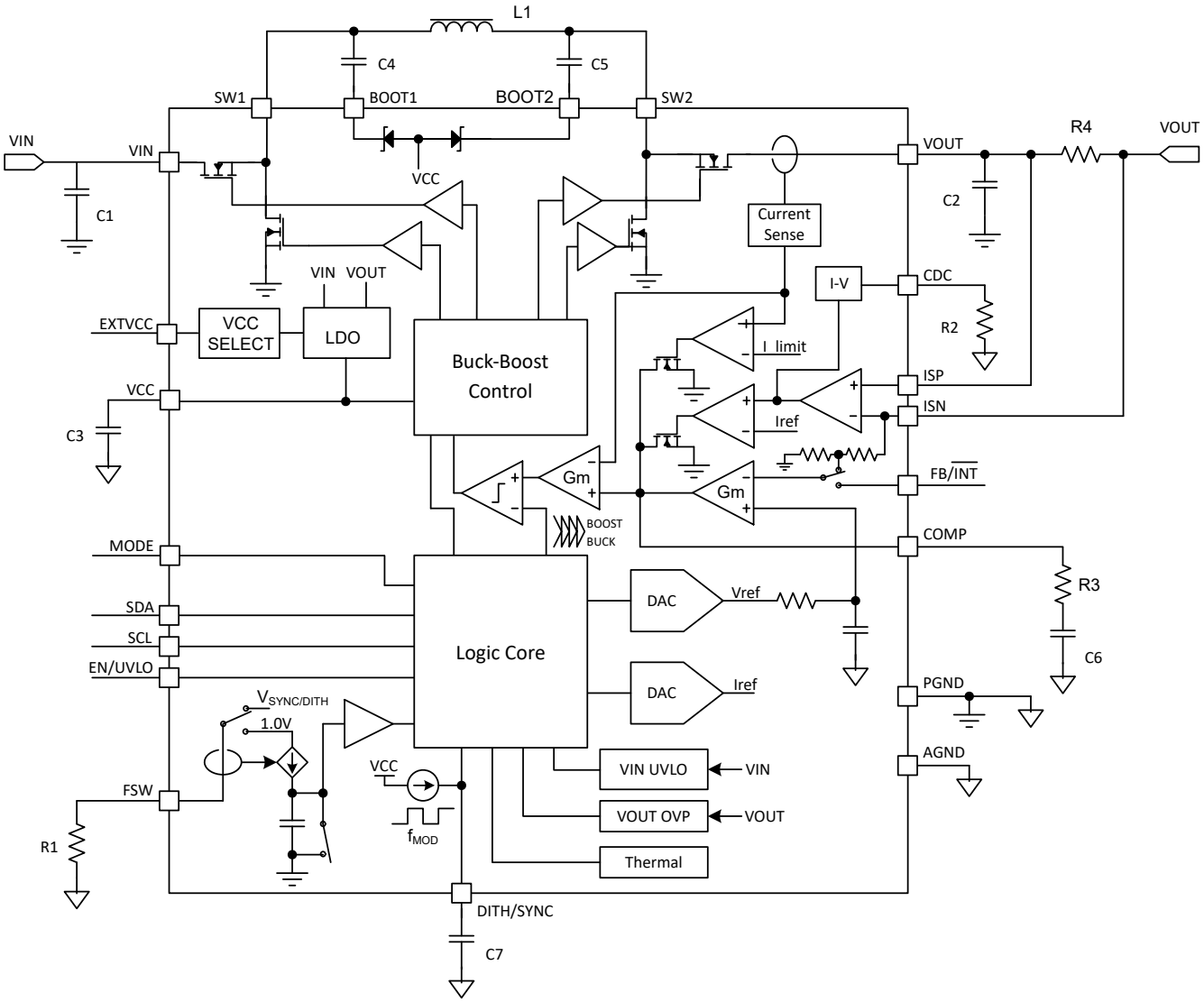
The output voltage of the TPS55287 is adjustable by setting the internal register through $I^2C$ interface. An internal 11-bit DAC adjusts the reference voltage related to the value written into the REF register. The device can also limit the output current by placing a current sense resistor in the output path. These two functions support the programmable power supply (PPS) feature of the USB PD.

The TPS55287 provides average inductor current limit of 4A typically. In addition, the device provides cycle-by-cycle peak inductor current limit during transient to protect the device against overcurrent condition beyond the capability of the device.

A precision voltage threshold of 1.23V with 5µA sourcing current at the EN/UVLO pin supports programmable input undervoltage lockout (UVLO) with hysteresis. The output overvoltage protection (OVP) feature turns off the high-side FETs to prevent damage to the devices powered by the TPS55287.

The device provides a hiccup mode option to reduce the heating in the power components when the output short circuit happens. When the hiccup mode is enabled, the TPS55287 turns off for 76ms and restarts at soft-start–up.

## 6.2 Functional Block Diagram




## 6.3 Feature Description

### 6.3.1 VCC Power Supply

An internal LDO supplies the TPS55287 outputs regulated 5.2V voltage at the VCC pin. When $V_{IN}$ is less than $V_{OUT}$, the internal LDO selects the power supply source by comparing $V_{IN}$ to a rising threshold of 6.2V with 0.3V hysteresis. When $V_{IN}$ is higher than 6.2V, the supply for LDO is $V_{IN}$. When $V_{IN}$ is lower than 5.9V, the supply for LDO is $V_{OUT}$. When $V_{OUT}$ is less than $V_{IN}$, the internal LDO selects the power supply source by comparing $V_{OUT}$ to a rising threshold of 6.2V with 0.3V hysteresis. When $V_{OUT}$ is higher than 6.2V, the supply for LDO is $V_{OUT}$. When $V_{OUT}$ is lower than 5.9V, the supply for LDO is $V_{IN}$. Table 6-1 shows the supply source selection for the internal LDO.

**Table 6-1. $V_{CC}$ Power Supply Logic**

| $V_{IN}$ | $V_{OUT}$ | Input for $V_{CC}$ LDO |
|---|---|---|
| $V_{IN}$ > 6.2V | $V_{OUT}$ > $V_{IN}$ | $V_{IN}$ |
| $V_{IN}$ < 5.9V | $V_{OUT}$ > $V_{IN}$ | $V_{OUT}$ |
| $V_{IN}$ > $V_{OUT}$ | $V_{OUT}$ > 6.2 V | $V_{OUT}$ |
| $V_{IN}$ > $V_{OUT}$ | $V_{OUT}$ < 5.9V | $V_{IN}$ |

### 6.3.2 EXTVCC Power Supply

To minimize the power dissipation of the internal LDO when both input voltage and output voltage are high, an external 5V power source can be applied at the VCC pin to supply the TPS55287. The external 5V power supply must have at least 100mA output current capability and must be within the 4.75V to 5.5V regulation range. When the EXTVCC pin is connected to logic low, the device selects the external power supply to supply the device through VCC pin. When the EXTVCC pin is connected to logic high, the device selects internal LDO.

### 6.3.3 Operation Mode Setting

By configuring the MODE pin logic status, the TPS55287 selects two different I$^2$C addresses. Table 6-2 shows the I$^2$C target address setting.

**Table 6-2. I$^2$C Target Address Setting**

| MODE Pin | I$^2$C Target Address |
|---|---|
| Low | 75h |
| High | 74h |

### 6.3.4 Input Undervoltage Lockout

When the input voltage is below 2.6V, the TPS55287 is disabled. When the input voltage is above 3V, the TPS55287 can be enabled by pulling the EN pin to a high voltage above 1.3V.

### 6.3.5 Enable and Programmable UVLO

The TPS55287 has a dual function enable and undervoltage lockout (UVLO) circuit. When the input voltage at the VIN pin is above the input UVLO rising threshold of 3V and the EN/UVLO pin is pulled above 1.15V but less than the enable UVLO threshold of 1.23V, the TPS55287 is enabled but still in standby mode. The TPS55287 starts to detect the MODE pin logic status and select the I$^2$C target address.

The EN/UVLO pin has an accurate UVLO voltage threshold to support programmable input undervoltage lockout with hysteresis. When the EN/UVLO pin voltage is greater than the UVLO threshold of 1.23V, the TPS55287 is enabled for I$^2$C communication and switching operation. A hysteresis current, $I_{UVLO\_HYS}$, is sourced out of the EN/UVLO pin to provide hysteresis that prevents on/off chattering in the presence of noise with a slowly changing input voltage.

By using resistor divider as shown in Figure 6-1, the turn-on threshold is calculated using Equation 1.

$$V_{IN(UVLO\_ON)} = V_{UVLO} \times (1 + \frac{R1}{R2}) \quad (1)$$

where

- $V_{UVLO}$ is the UVLO threshold of 1.23V at the EN/UVLO pin.

The hysteresis between the UVLO turn-on threshold and turn-off threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by Equation 2.

$$\Delta V_{IN(UVLO)} = I_{UVLO\_HYS} \times R1 \quad (2)$$

where

- $I_{UVLO\_HYS}$ is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above $V_{UVLO}$.

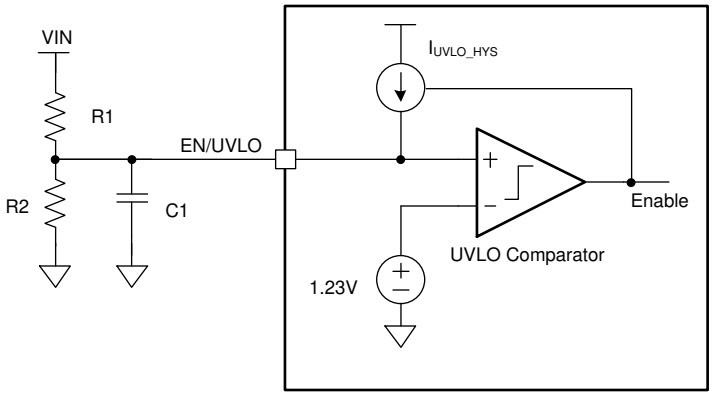



**Figure 6-1. Programmable UVLO With Resistor Divider at the EN/UVLO Pin**

Using an NMOSFET together with a resistor divider can implement both logic enable and programmable UVLO as shown in Figure 6-2. The EN logic high level must be greater than the enable threshold plus the $V_{th}$ of the NMOSFET Q1. The Q1 also eliminates the leakage current from VIN to ground through the UVLO resistor divider during shutdown mode.

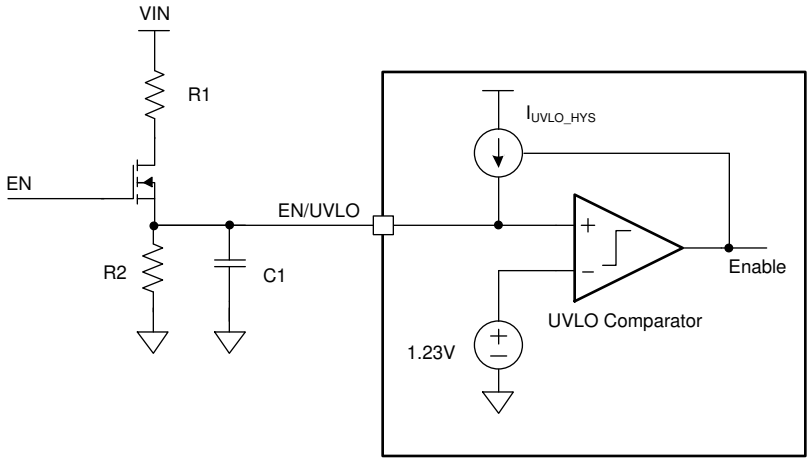



**Figure 6-2. Logic Enable and Programmable UVLO**

### *6.3.6 Soft Start*

When the input voltage is above the UVLO threshold and the voltage at the EN/UVLO pin is above the enable UVLO threshold, the TPS55287 is ready to accept the command from the $I^2C$ controller device. An $I^2C$ controller device can configure the internal registers of the TPS55287 before setting the OE bit of the register 06h. Once an $I^2C$ controller device sets the OE bit to 1, the TPS55287 starts to ramp up the output voltage by ramping an internal reference voltage from 0V to a voltage set in the internal registers 00h and 01h within 3.6ms (typical).

### *6.3.7 Shutdown and Load Discharge*

When the EN/UVLO pin voltage is pulled below 0.4 V, the TPS55287 is in shutdown mode, and all functions are disabled. All internal registers are reset to default values.

When the EN/UVLO pin is at a high logic level and the OE bit is cleared to 0, the TPS55287 turns off the switching operation but keeps the $I^2C$ interface active. Simultaneously, if the DISCHG bit in the register 06h is set to 1, the TPS55287 discharges the output voltage below 0.8 V by an internal constant current.

When the EN/UVLO pin is at high logic level, the TPS55287 output discharge current can also be enabled by setting the Force_DISCHG bit in the register 06h to 1. During output voltage transient from high voltage to low voltage, the output discharge current helps reduce the VOUT falling time in auto PFM mode or reduces the

reverse current in FPWM mode. It's not recommended to enable the discharge FET longer than 10ms due to high power loss.

### 6.3.8 Switching Frequency

The TPS55287 uses a fixed frequency average current control scheme. The switching frequency is between 200kHz and 2.2MHz set by placing a resistor at the FSW pin. An internal amplifier holds this pin at a fixed voltage of 1V. The setting resistance is between maximum of 100kΩ and minimum of 8.4kΩ. Use Equation 3 to calculate the resistance by a given switching frequency.

$$f_{SW} = \frac{1000}{0.05 \times R_{FSW} + 35} \quad (3)$$

where

- $R_{FSW}$ is the resistance at the FSW pin.

For noise-sensitive applications, the TPS55287 can be synchronized to an external clock signal applied to the DITH/SYNC pin. The duty cycle of the external clock is recommended in the range of 30% to 70%. A resistor also must be connected to the FSW pin when the TPS55287 is switching by the external clock. The external clock frequency at the DITH/SYNC pin must have lower than 0.4V low level voltage and must be within ±30% of the corresponding frequency set by the resistor. Figure 6-3 is a recommended configuration.

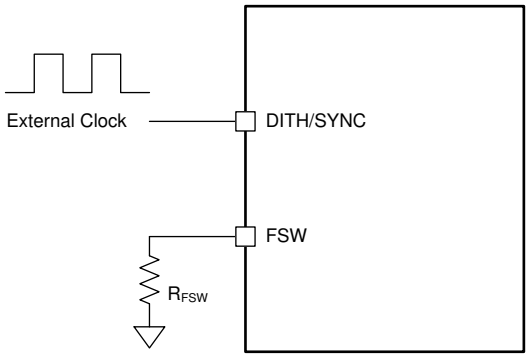



**Figure 6-3. External Clock Configuration**

### 6.3.9 Switching Frequency Dithering

The TPS55287 provides an optional switching frequency dithering that is enabled by connecting a capacitor from the DITH/SYNC pin to ground. Figure 6-4 illustrates the dithering circuit. By charging and discharging the capacitor, a triangular waveform centered at 1V is generated at the DITH/SYNC pin. The triangular waveform modulates the oscillator frequency by ±7% of the nominal frequency set by the resistance at the FSW pin. The capacitance at the DITH/SYNC pin sets the modulation frequency. A small capacitance modulates the oscillator frequency at a faster rate than a large capacitance. For the dithering circuit to effectively reduce peak EMI, the modulation rate normally is below 1kHz. Equation 4 calculates the capacitance required to set the modulation frequency, $F_{MOD}$.

$$C_{DITH} = \frac{1}{2.8 \times R_{FSW} \times F_{MOD}} (F) \quad (4)$$

where

- $R_{FSW}$ is the switching frequency setting resistance (Ω) at the FSW pin.
- $F_{MOD}$ is the modulation frequency (Hz) of the dithering.

Connecting the DITH/SYNC pin below 0.4V or above 1.2V disables switching frequency dithering. The dithering function also is disabled when an external synchronous clock is used.

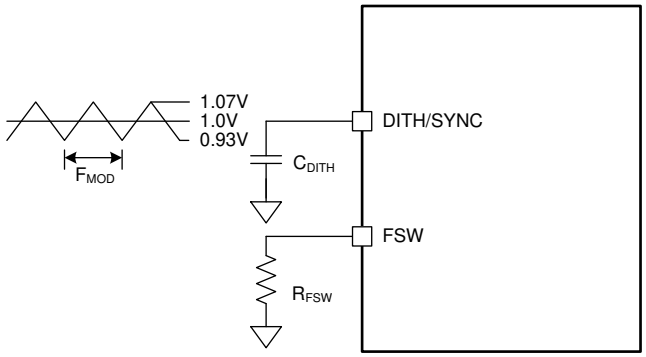



**Figure 6-4. Switching Frequency Dithering**

### *6.3.10 Inductor Current Limit*

The TPS55287 implements both peak current and average inductor current limit. The average current mode control loop uses the current sense information at the high-side MOSFET of the boost leg to clamp the maximum average inductor current to 4A (typical).

Besides the average current limit, a peak current limit protection is implemented during transient to protect the device against overcurrent conditions beyond the capability of the device.

### *6.3.11 Internal Charge Path*

Each of the two high-side MOSFET drivers is biased from its floating bootstrap capacitor, which is normally re-charged by $V_{CC}$ through both the external and internal bootstrap diodes when the low-side MOSFET is turned on. When the TPS55287 operates exclusively in the buck or boost regions, one of the high-side MOSFETs is constantly on. An internal charge path, from VOUT and BOOT2 to BOOT1 or from VIN and BOOT1 to BOOT2, charges the bootstrap capacitor to $V_{CC}$ so that the high-side MOSFET remains on.

### *6.3.12 Output Voltage Setting*

There are two ways to set the output voltage: changing the feedback ratio and changing the reference voltage. The TPS55287 has a 11-bit DAC to program the reference voltage from 45mV to 1.2V. The TPS55287 can also select an internal feedback resistor divider or an external resistor divider by setting the FB bit in register 04h. When the FB bit is set to 0, the output voltage feedback ratio is set in internal register 04h. When the FB bit is set to 1, the output voltage feedback ratio is set by an external resistor divider.

When using internal output voltage feedback settings, use Equation 8 to calculate the output voltage. There are four feedback ratios programmable by writing the INTFB[1:0] bits of register 04h. With this function, the TPS55287 can limit the maximum output voltage to different values. In addition, the minimum step of the output voltage change is also programmed to 10mV, 7.5mV, 5mV, and 2.5mV, accordingly.

When using an external output voltage feedback resistor divider as shown in Figure 6-5, use Equation 5 to calculate the output voltage with the reference voltage at the FB/$\overline{\text{INT}}$ pin.

$$V_{OUT} = V_{REF} \times (1 + \frac{R_{FB\_UP}}{R_{FB\_BT}}) \quad (5)$$

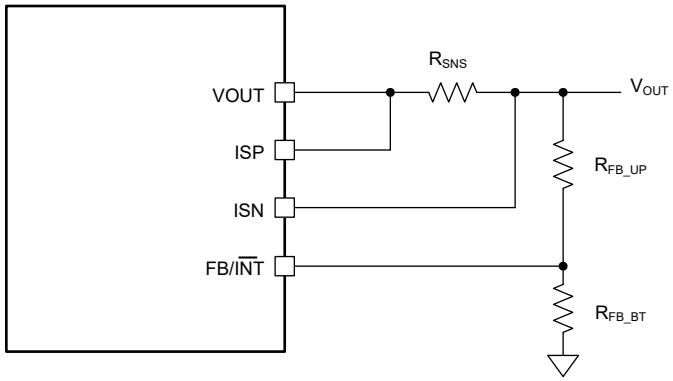



**Figure 6-5. Output Voltage Setting by External Resistor Divider**

TI recommends using 100kΩ for the up resistor, $R_{FB\_UP}$. The reference voltage, $V_{REF}$, at the FB/$\overline{INT}$ pin is programmable from 45mV to 1.2V by writing 11-bit data into registers 00h and 01h.

### *6.3.13 Output Current Monitoring and Cable Voltage Droop Compensation*

The TPS55287 outputs a voltage at the CDC pin proportional to the sensed voltage across an output current sensing resistor between the ISP pin and the ISN pin. Equation 6 shows the exact voltage at the CDC pin related to the sensed output current.

$$V_{CDC} = 20 \times (V_{ISP} - V_{ISN}) \quad (6)$$

To compensate the voltage droop across a cable from the output of the USB port to its powered device, the TPS55287 can lift its output voltage in proportion to the load current. There are two methods in the TPS55287 to implement the compensation: by setting internal register 05h or by placing a resistor between the CDC pin and AGND pin.

When using internal output voltage feedback, use the internal compensation setting. When using an external resistor divider at the FB/$\overline{INT}$ pin to set the output voltage, use the external compensation setting by placing a resistor at the CDC pin.

By default, the internal cable voltage droop compensation function is enabled with 0V added to the output voltage. Write the value into the bit CDC [2:0] in register 05h to get the desired voltage compensation.

When using external output voltage feedback, external compensation is better than the internal register for its high accuracy. The output voltage rises in proportion to the current sourcing from the CDC pin through the resistor at the CDC pin. Use 100kΩ resistance for the up resistor of the feedback resistor divider. Equation 7 shows the output voltage rise related to the sensed output current, the resistance at the CDC pin, and the up resistor of the output voltage feedback resistor divider.

$$V_{OUT\_CDC} = 3 \times R_{FB\_UP} \times \left(\frac{V_{ISP} - V_{ISN}}{R_{CDC}}\right) \quad (7)$$

where

- $R_{FB\_UP}$ is the up resistor of the resistor divider between the output and the FB/$\overline{INT}$ pin.
- $R_{CDC}$ is the resistor at the CDC pin.

Figure 6-6 shows the output voltage rise versus the sensed output current and the resistor at the CDC pin when $R_{FB\_UP}$ is 100kΩ.

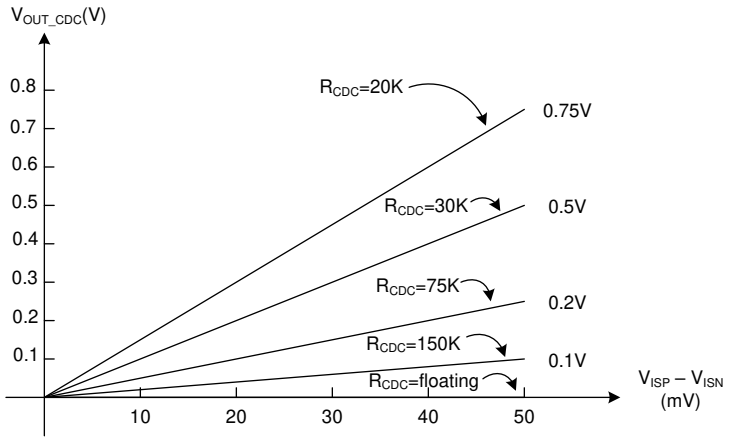



**Figure 6-6. Output Voltage Rise Versus Output Current**

### *6.3.14 Output Current Limit*

The output current limit is programmable from 0A to 6.35A by placing a 10mΩ current sensing resistor between the ISP pin and the ISN pin. Smaller resistance results in a higher current limit and larger resistance results in a lower current limit. An internal register sets the current sense voltage across the ISP pin and the ISN pin. The programmable voltage step between the ISP pin and the ISN pin is 0.5mV.

Connecting the ISP and the ISN pin together to the VOUT pin disables the output current limit because the sensed voltage is always 0. The output current limit can also be disabled by resetting the Current_Limit_EN bit in the Current_Limit register to 0.

### *6.3.15 Overvoltage Protection*

The TPS55287 has output overvoltage protection. When the output voltage at the VOUT pin is detected above 23.5 V (typical), the TPS55287 turns off two high-side FETs and turns on two low-side FETs until its output voltage drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

### *6.3.16 Output Short Circuit Protection*

In addition to the average inductor current limit, the TPS55287 implements output short-circuit protection by entering hiccup mode. To enable hiccup mode, the HICCUP bit in register 06h must be set. After a 3.6ms soft-start–up time, the TPS55287 monitors the average inductor current and output voltage. Whenever the output short circuit happens, causing the average inductor current to reach the set limit and the output voltage is below 0.8V, the TPS55287 shuts down the switching for 76ms (typical) and then repeats the soft start for 3.6ms. The hiccup mode helps reduce the total power dissipation on the TPS55287 in output short-circuit or overcurrent condition.

### *6.3.17 Thermal Shutdown*

The TPS55287 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 175°C (typical). The internal soft-start circuit is reset but all internal registers values remain unchanged when thermal shutdown is triggered. The converter automatically restarts when the junction temperature drops below the thermal shutdown hysteresis of 20°C below the thermal shutdown threshold.

## 6.4 Device Functional Modes

In light load condition, the TPS55287 can work in PFM or forced PWM mode to meet different application requirements. PFM mode decreases switching frequency to reduce the switching loss, thus it gets high efficiency at light load condition. FPWM mode keeps the switching frequency unchanged to avoid undesired low switching frequency, but the efficiency becomes lower than that of PFM mode.

By default, the TPS55287 works in PFM mode. To set the device in forced PWM mode, write the FPWM bit in the MODE register to 1.

### 6.4.1 PWM Mode

In FPWM mode, the TPS55287 keeps the switching frequency unchanged in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to reduce the average inductor current down to deliver less power from input to output. When the output current further reduces, the current through the inductor decreases to zero during the switch-off time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from the output side to input side. The efficiency is low in light load condition. However, with the fixed switching frequency, there is no audible noise or other problems that can be caused by low switching frequency in light load condition.

### 6.4.2 Power Save Mode

The TPS55287 improves the efficiency at light load condition with PFM mode. By enabling the PFM function in the internal register, the TPS55287 can work in PFM mode at light load condition. When the TPS55287 operates at light load condition, the output of the internal error amplifier decreases to make the inductor peak current down to deliver less power to the load. When the output current further reduces, the current through the inductor will decrease to zero during the switch-off time. When the TPS55287 works in buck mode, once the inductor current becomes zero, the low-side switch of the buck side is turned off to prevent the reverse current from output to ground. When the TPS55287 works in boost mode, once the inductor current becomes zero, the high side-switch of the boost side is turned off to prevent the reverse current from output to input. The TPS55287 resumes switching until the output voltage drops, so PFM mode reduces switching cycles and eliminates the power loss by the reverse inductor current to get high efficiency in light load condition.

## 6.5 Programming

The TPS55287 uses $I^2C$ interface for flexible converter parameter programming. $I^2C$ is a bi-directional 2-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). $I^2C$ devices can be considered as controllers or targets when performing data transfers. A controller is the device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target.

The TPS55287 operates as a target device with address 74h and 75h set by the MODE pin. Receiving control inputs from the controller device, like a microcontroller or a digital signal processor, reads and writes the internal registers 00h through 07h. The $I^2C$ interface of the TPS55287 supports both standard mode (up to 100 kbit/s) and fast mode plus (up to 1000 kbit/s). Both SDA and SCL must be connected to the positive supply voltage through current sources or pullup resistors. When the bus is free, both lines are in high voltage.

### 6.5.1 Data Validity

The data on the SDA line must be stable during the high level period of the clock. The high level or low level state of the data line can only change when the clock signal on the SCL line is low level. One clock pulse is generated for each data bit transferred.

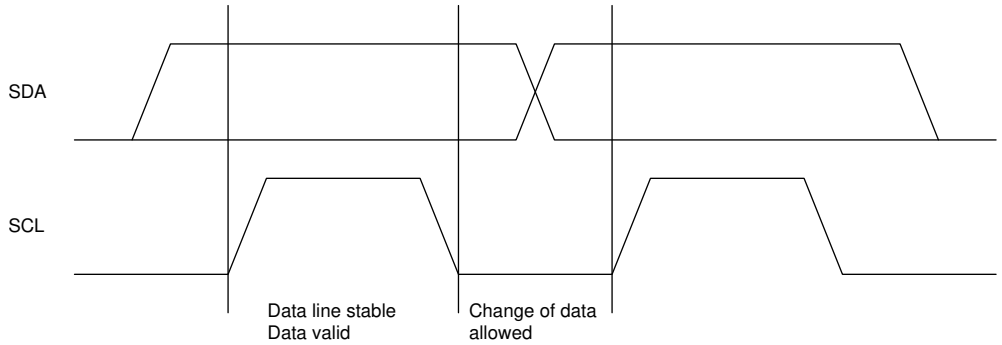



**Figure 6-7. $I^2C$ Data Validity**

### 6.5.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A high level to low level transition on the SDA line while SCL is at high level defines a START condition. A low level to high level transition on the SDA line when the SCL is at high level defines a STOP condition.

START and STOP conditions are always generated by the controller. The bus is considered busy after the START condition, and free after the STOP condition.

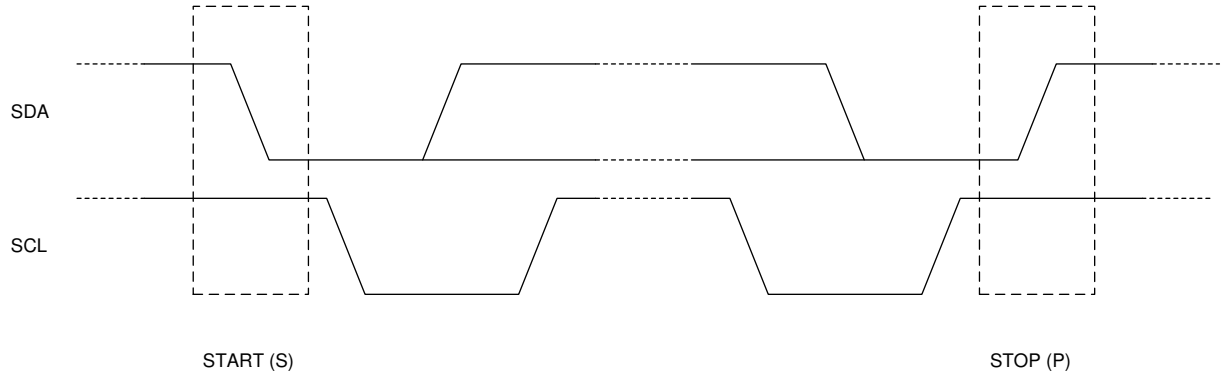



**Figure 6-8. I²C START and STOP Conditions**

### 6.5.3 Byte Format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the controller into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and release the clock line SCL.

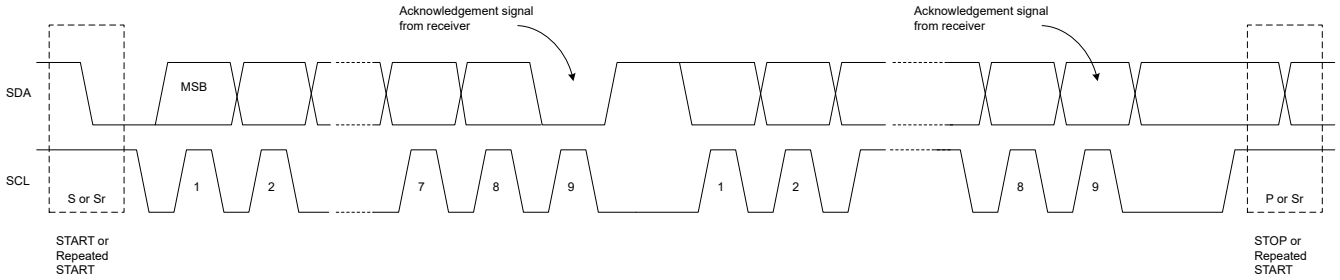



**Figure 6-9. Byte Format**

### 6.5.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte can be sent. All clock pulses, including the acknowledge ninth clock pulse, are generated by the controller.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line to low level and it remains stable low level during the high level period of this clock pulse.

The Not Acknowledge signal is when SDA remains high level during the ninth clock pulse. The controller can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

### 6.5.5 Target Address and Data Direction Bit

After the START, a target address is sent. This address is seven bits long followed by the eighth bit as a data direction bit (bit R/$\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

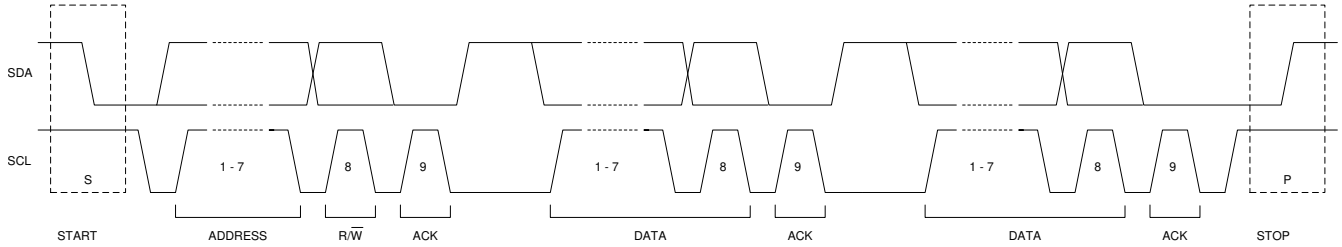



**Figure 6-10. Target Address and Data Direction**

### *6.5.6 Single Read and Write*

Figure 6-11 and Figure 6-12 show the single-byte write and single-byte read format of the $I^2C$ communication.

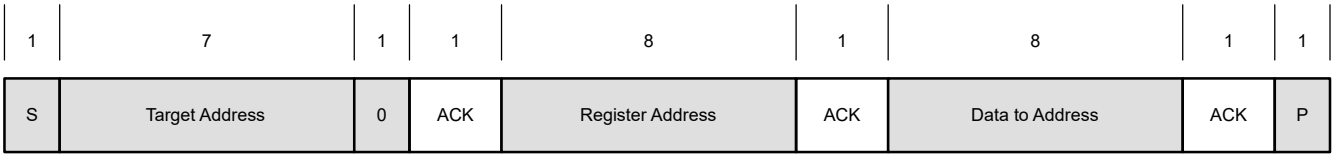



**Figure 6-11. Single-Byte Write**


**Figure 6-12. Single-Byte Read**

If the register address is not defined, the TPS55287 sends back NACK and goes back to the idle state.

### *6.5.7 Multiread and Multiwrite*

The TPS55287 supports multiread and multiwrite.

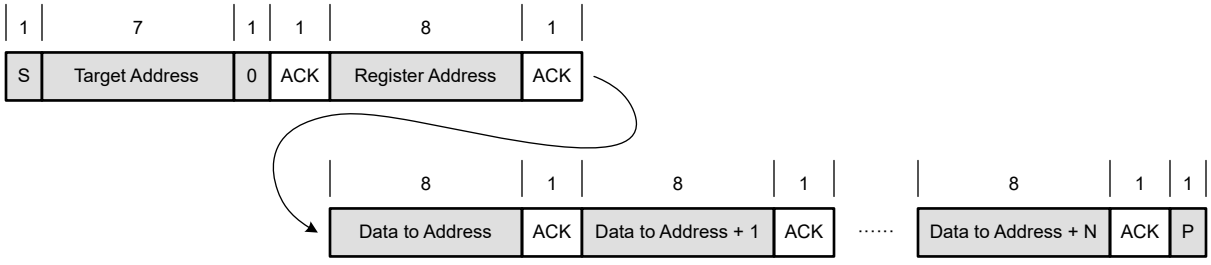



**Figure 6-13. Multibyte Write**

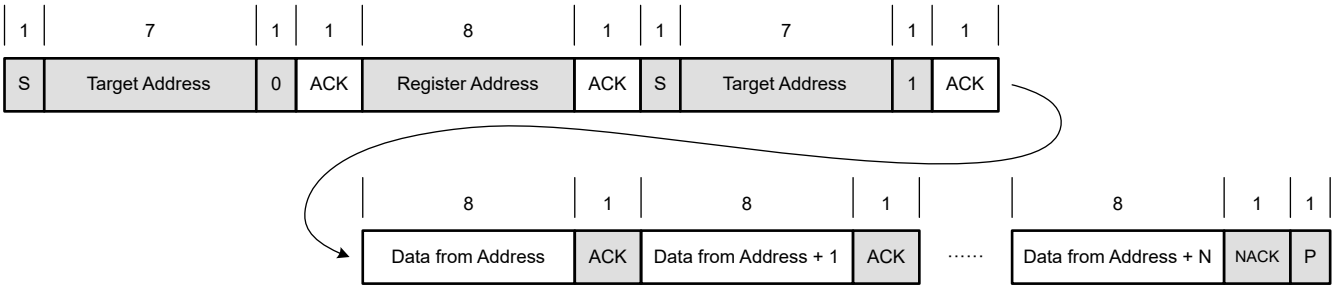



**Figure 6-14. Multibyte Read**

## 6.6 Register Maps

Table 6-3 lists the memory-mapped registers for the device registers. All register offset addresses not listed in Table 6-3 should be considered as reserved locations, and the register contents should not be modified.

**Table 6-3. Device Registers**

| Address | Acronym | Register Name | Section |
|---|---|---|---|
| 0h, 1h | REF | Reference Voltage | Go |
| 2h | IOUT_LIMIT | Current Limit Setting | Go |
| 3h | VOUT_SR | Slew Rate | Go |
| 4h | VOUT_FS | Feedback Selection | Go |
| 5h | CDC | Cable Compensation | Go |
| 6h | MODE | Mode Control | Go |
| 7h | STATUS | Operating Status | Go |

### 6.6.1 REF Register (Address = 0h, 1h)

REF is shown in Figure 6-15 and Figure 6-16 and described in Table 6-4.

Return to Summary Table.

REF sets the internal reference voltage of the TPS55287. The 01h register is the high byte and the 00h register is the low byte. One LSB of register 00h stands for 0.5645 mV of the internal reference voltage. The default register value is 00000001 10100100b of 282mV. When the register value is 00000000 00000000b, the reference voltage is 45 mV. When the register value is 00000111 10000000b, the reference voltage is 1.129 V. The output voltage of the TPS55287 also depends on the output feedback ratio, which is either set by INTFB bit in register 04h or set by an external resistor divider.

When using internal output voltage feedback, the output voltage $V_{OUT}$ is calculated by Equation 8.

$$V_{OUT} = \frac{V_{REF}}{INTFB} \quad (8)$$

The REF register can be configured by an $I^2C$ controller before setting the OE bit in register 06h. For 5-V output voltage, set the REF register value to 00000001 10100100b. To set the internal reference voltage, write the register 00h first, then write the register 01h.

**Figure 6-15. REF_LSB**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VREF | | | | | | | |

**Figure 6-16. REF_MSB**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | VREF | | |

**Table 6-4. REF Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-11 | Reserved | R/W | 000000b | Reserved |
| 10-0 | VREF | R/W | 001 10100100b | Sets the internal reference voltage<br>000 00000000b = 45-mV reference voltage<br>000 00000001b = 45.5645-mV reference voltage<br>000 00000010b = 46.129-mV reference voltage<br>..... = .....<br>001 10100100b = 282-mV reference voltage (Default)<br>..... = .....<br>011 00110100b = 508-mV reference voltage<br>..... = .....<br>101 10001100b = 846-mV reference voltage<br>..... = .....<br>111 10000000b = 1129-mV reference voltage<br>..... = .....<br>111 11111110b = 1200-mV reference voltage |

### 6.6.2 IOUT_LIMIT Register (Address = 2h) [reset = 11100100h]

IOUT_LIMIT is shown in Figure 6-17 and described in Table 6-5.

Return to Summary Table.

IOUT_LIMIT sets the current limit target voltage between the ISP pin and the ISN pin. The default value in the current limit register is 11100100b standing for 50 mV. One LSB stands for 0.5 mV. The bit7 enables the current limit or disables the current limit.

**Figure 6-17. IOUT_LIMIT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Current_Limit_EN | Current_Limit_Setting | | | | | | |
| R/W-1b | R/W-1100100b | | | | | | |

**Table 6-5. IOUT_LIMIT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | Current_Limit_EN | R/W | 1b | Enable or disable current limit.<br>0b = Current limit disabled<br>1b = Current limit enabled (Default) |
| 6-0 | Current_Limit_Setting | R/W | 1100100b | Sets the current limit target voltage between the ISP pin and the ISN pin<br>0000000b = $V_{ISP}$-$V_{ISN}$ = 0 (mV)<br>0000001b = $V_{ISP}$-$V_{ISN}$ = 0.5 (mV)<br>0000010b = $V_{ISP}$-$V_{ISN}$ = 1 (mV)<br>0000011b = $V_{ISP}$-$V_{ISN}$ = 1.5 (mV)<br>0000100b = $V_{ISP}$-$V_{ISN}$ = 2.0 (mV)<br>..... = .....<br>1100100b = $V_{ISP}$-$V_{ISN}$ = 50.0 (mV) (Default)<br>..... = .....<br>1111111b = $V_{ISP}$-$V_{ISN}$ = 63.5 (mV) |

### 6.6.3 VOUT_SR Register (Address = 3h) [reset = 00000001h]

VOUT_SR is shown in Figure 6-18 and described in Table 6-6.

Return to Summary Table.

Register 03h sets the slew rate of the output voltage change and the response delay time after the output current exceeds the setting output current limit.

The OCP_DELAY [1:0] bits set the response time of the TPS55287 when the output overcurrent limit is hit. This allows the TPS55287 to output high current in a relative short duration time. The default setting is 128 µs so that the TPS55287 immediately limits the output current.

The SR [1:0] bits set 1.25 mV/µs, 2.5 mV/µs, 5 mV/µs, and 10 mV/µs slew rate for output voltage change.

**Figure 6-18. VOUT_SR Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | OCP_DELAY | | RESERVED | | SR | |
| R/W-0b | | R/W-00b | | R/W-00b | | R/W-01b | |

**Table 6-6. VOUT_SR Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED | R/W | 00b | Reserved |
| 5-4 | OCP_DELAY | R/W | 00b | Sets the response time of the device when the output overcurrent limit is reached<br>00b = 128 µs (Default)<br>01b = Delay 1.024 × 3 ms<br>10b = Delay 1.024 × 6 ms<br>11b = Delay 1.024 × 12 ms |
| 3-2 | RESERVED | R/W | 00b | Reserved |
| 1-0 | SR | R/W | 01b | Sets slew rate for output voltage change<br>00b = 1.25-mV/µs output change slew rate<br>01b = 2.5-mV/µs output change slew rate (Default)<br>10b = 5-mV/µs output change slew rate<br>11b = 10-mV/µs output change slew rate |

### 6.6.4 VOUT_FS Register (Address = 4h) [reset = 00000011h]

VOUT_FS is shown in Figure 6-19 and described in Table 6-7.

Return to Summary Table.

Register 04h sets the selection for the output feedback voltage, either by an internal resistor divider or external resistor divider, and sets the internal feedback ratio when using internal feedback resistor divider.

**Figure 6-19. VOUT_FS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FB | RESERVED | | | | | INTFB | |
| R/W-0b | R/W-00000b | | | | | R/W-11b | |

**Table 6-7. VOUT_FS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | FB | R/W | 0b | Output feedback voltage<br>0b = Use internal output voltage feedback. The FB/$\overline{INT}$ pin is the indicator for output short circuit protection, overcurrent status, and overvoltage status (Default).<br>1b = Use external output voltage feedback. The FB/$\overline{INT}$ pin is the feedback input of the output voltage. |
| 6-2 | RESERVED | R | 00000b | Reserved |
| 1-0 | INTFB | R/W | 11b | Internal feedback ratio<br>00b = Set internal feedback ratio to 0.2256<br>01b = Set internal feedback ratio to 0.1128<br>10b = Set internal feedback ratio to 0.0752<br>11b = Set internal feedback ratio to 0.0564 (Default) |

**Table 6-8. Output Voltage vs Internal Reference**

| INTFB1 | INTFB0 | REF=0000h | REF=001Ah | REF=0050h | REF=00F0h | REF=0780h | Output Voltage Step |
|---|---|---|---|---|---|---|---|
| 0 | 0 | | | | 0.8 V | 5 V | 2.5 mV |
| 0 | 1 | | | 0.8 V | | 10 V | 5 mV |
| 1 | 0 | | 0.8 V | | | 15 V | 7.5 mV |
| 1 | 1 | 0.8 V | | | | 20 V | 10 mV |

### 6.6.5 CDC Register (Address = 5h) [reset = 11100000h]

CDC is shown in Figure 6-20 and described in Table 6-9.

Return to Summary Table.

Register 05h sets masks for SC bit, OCP bit, and OVP bit in register 07h. In addition, register 05h sets the voltage rise added to the setting output voltage with respect to the sensed differential voltage between the ISP pin and the ISN pin.

**Figure 6-20. CDC Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SC_MASK | OCP_MASK | OVP_MASK | RESERVED | CDC_OPTION | CDC | | |
| R/W-1b | R/W-1b | R/W-1b | R/W-0b | R/W-0b | R/W-000b | | |

**Table 6-9. CDC Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SC_MASK | R/W | 1b | Short circuit mask<br>0b = Disabled SC indication<br>1b = Enable SC indication (Default) |
| 6 | OCP_MASK | R/W | 1b | Over current mask<br>0b = Disabled OCP indication<br>1b = Enable OCP indication (Default) |
| 5 | OVP_MASK | R/W | 1b | Over voltage mask<br>0b = Disabled OVP indication<br>1b = Enable OVP indication (Default) |
| 4 | RESERVED | R/W | 0b | Reserved |
| 3 | CDC_OPTION | R/W | 0b | Select the cable voltage droop compensation approach.<br>0b = Internal CDC compensation by the register 05H (Default)<br>1b = External CDC compensation by a resistor at the CDC pin |
| 2-0 | CDC | R/W | 000b | Compensation for voltage droop over the cable<br>000b = 0-V output voltage rise with 50 mV at $V_{ISP}$ - $V_{ISN}$ (Default)<br>001b = 0.1-V output voltage rise with 50 mV at $V_{ISP}$ - $V_{ISN}$<br>010b = 0.2-V output voltage rise with 50 mV at $V_{ISP}$ - $V_{ISN}$<br>011b = 0.3-V output voltage rise with 50 mV at $V_{ISP}$ - $V_{ISN}$<br>100b = 0.4-V output voltage rise with 50 mV at $V_{ISP}$ - $V_{ISN}$<br>101b = 0.5-V output voltage rise with 50 mV at $V_{ISP}$ - $V_{ISN}$<br>110b = 0.6-V output voltage rise with 50 mV at $V_{ISP}$ - $V_{ISN}$<br>111b = 0.7-V output voltage rise with 50 mV at $V_{ISP}$ - $V_{ISN}$ |

### 6.6.6 MODE Register (Address = 6h) [reset = 00100000h]

MODE is shown in Figure 6-21 and described in Table 6-10.

Return to Summary Table.

MODE controls the operating mode of the TPS55287.

**Figure 6-21. MODE Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OE | FSW | HICCUP | DISCHG | Reserved | Reserved | FPWM | Reserved |
| R/W-0b | R/W-0b | R/W-1b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b |

**Table 6-10. MODE Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | OE | R/W | 0b | Output enable<br>0b = Output disabled (Default)<br>1b = Output enable |
| 6 | FSWDBL | R/W | 0b | Switching frequency doubling in buck-boost mode<br>0b = Keep the switching frequency unchanged during buck-boost mode (Default)<br>1b = Double the switching frequency during buck-boost mode |
| 5 | HICCUP | R/W | 1b | Hiccup mode<br>0b = Disable the hiccup during output short circuit protection.<br>1b = Enable the hiccup during output short circuit protection (Default) |
| 4 | DISCHG | R/W | 0b | Output discharge<br>0b = Disabled VOUT discharge when the device is in shutdown mode (Default)<br>1b = Enable VOUT discharge. VOUT is discharged to ground by an internal 100mA current sink in shutdown mode (OE bit is cleared to 0) |
| 3 | Force_DISCHG | R/W | 0b | Force output dischage<br>Force output discharge helps reduce the VOUT falling time in auto PFM mode when set VOUT to lower voltage. TI does not recommend enabling this bit longer than 10ms at high VOUT range (>10V) due to high power loss.<br>0b = Disabled VOUT discharge FET(Default)<br>1b = Force enable VOUT discharge FET. VOUT is discharged to ground by an internal 100mA current sink |
| 2 | RESERVED | R | 0b | Reserved |
| 1 | FPWM | R/W | 0b | Select operating mode at light load condition<br>0b = PFM operating mode at light load condition (Default)<br>1b = FPWM operating mode at light load condition |
| 0 | RESERVED | R | 0b | Reserved |

### 6.6.7 STATUS Register (Address = 7h) [reset = 00000011h]

STATUS is shown in Figure 6-22 and described in Table 6-11.

Return to Summary Table.

The STATUS register stores the operating status of the TPS55287. When any of the SCP bit, the OCP bit, or the OVP bit are set, and the corresponding mask bit in register 05h is set as well, the FB/$\overline{INT}$ pin outputs low logic level to indicate the situation. Reading register 07h clears the SCP bit, OCP bit, and OVP bit. After the SCP bit, OCP bit, or OVP bit is set, it does not reset until the register is read. If the situation still exists, the corresponding bit is set again.

**Figure 6-22. STATUS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCP | OCP | OVP | Reserved | Reserved | Reserved | STATUS | |
| R-0b | R-0b | R-0b | R/W-0b | R/W-0b | R/W-0b | R-11b | |

**Table 6-11. STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SCP | R | 0b | Short circuit protection<br>0b = No short circuit<br>1b = Short circuit happens. Does not reset until it is read. |
| 6 | OCP | R | 0b | Overcurrent protection<br>0b = No output overcurrent<br>1b = Output current hits the current limit sensed at the ISP and the ISN pin. Does not reset until it is read. |
| 5 | OVP | R | 0b | Overvoltage protection<br>0b = No OVP<br>1b = Output voltage exceeds the OVP threshold. Does not reset until it is read. |
| 4 | RESERVED | R | 0b | Reserved |
| 3 | RESERVED | R | 0b | Reserved |
| 2 | RESERVED | R | 0b | Reserved |
| 1-0 | STATUS | R | 11b | Operating status<br>00b = Boost<br>01b = Buck<br>10b = Buck-Boost<br>11b = Reserved |

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

The TPS55287 can operate over a wide range of 3.0-V to 36-V input voltage and output 0.8 V to 22 V. The device can transition among buck mode, buck-boost mode, and boost mode smoothly according to the input voltage and the setting output voltage. The TPS55287 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS55287 operates in one-cycle buck and one-cycle boost mode alternately. The switching frequency is set by an external resistor. To reduce the switching power loss in high power conditions, set the switching frequency below 500 kHz.

## 7.2 Typical Application

The TPS55287 provides a small size solution for USB PD power supply application with the input voltage ranging from 9 V to 36 V.

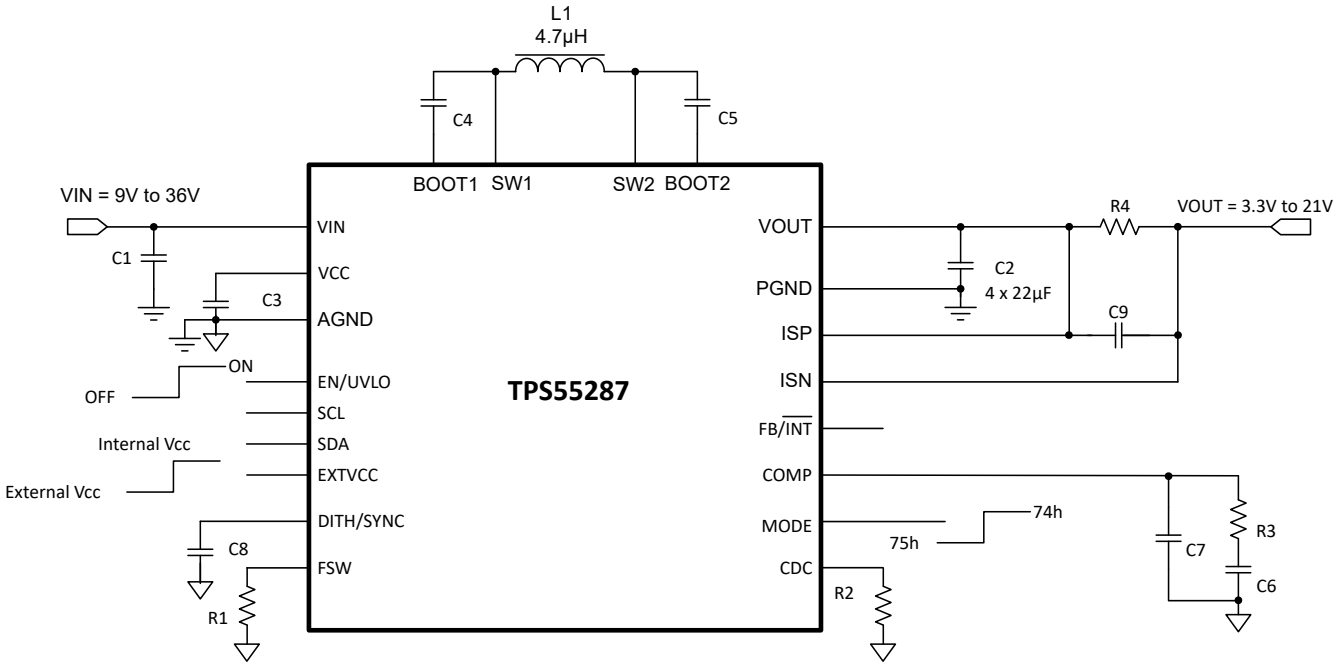



**Figure 7-1. USB PD Power Supply With 9-V to 36-V Input Voltage**

### 7.2.1 Design Requirements

The design parameters are listed in Table 7-1:

**Table 7-1. Design Parameters**

| Parameters | Values |
|---|---|
| Input voltage | 9 V to 36 V |
| Output voltage | 3.3 V to 20 V |
| Output current limit | 2.25 A |
| Output voltage ripple | ±50 mV |
| Operating mode at light load | FPWM |

### 7.2.2 Detailed Design Procedure

#### 7.2.2.1 Switching Frequency

The switching frequency of the TPS55287 is set by a resistor at the FSW pin. Use Equation 3 to calculate the resistance for the desired frequency. To reduce the switching power loss with such a high current application, a 1% standard resistor of 49.9 kΩ is selected for 400-kHz switching frequency for this application.

#### 7.2.2.2 Output Voltage Setting

The TPS55287 has $I^2C$ interface to set the internal reference voltage. A microcontroller can easily set the desired output voltage by writing the proper data into the reference voltage registers through $I^2C$ bus.

#### 7.2.2.3 Inductor Selection

Since the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications: inductance, saturation current, and DC resistance.

The TPS55287 is designed to work with inductor values between 1 µH and 10 µH. The inductor selection is based on consideration of both buck and boost modes of operation.

For buck mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum input voltage. In CCM, Equation 9 shows the relationship between the inductance and the inductor ripple current.

$$L = \frac{(V_{IN(MAX)} - V_{OUT}) \times V_{OUT}}{\Delta I_{L(P-P)} \times f_{SW} \times V_{IN(MAX)}} \quad (9)$$

where

- $V_{IN(MAX)}$ is the maximum input voltage.
- $V_{OUT}$ is the output voltage.
- $\Delta I_{L(P-P)}$ is the peak to peak ripple current of the inductor.
- $f_{SW}$ is the switching frequency.

For a certain inductor, the inductor ripple current achieves maximum value when $V_{OUT}$ equals half of the maximum input voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

For boost mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum output voltage. In CCM, Equation 10 shows the relationship between the inductance and the inductor ripple current.

$$L = \frac{V_{IN} \times (V_{OUT(MAX)} - V_{IN})}{\Delta I_{L(P-P)} \times f_{SW} \times V_{OUT(MAX)}} \quad (10)$$

where

- $V_{IN}$ is the input voltage.
- $V_{OUT(MAX)}$ is the maximum output voltage.
- $\Delta I_{L(P-P)}$ is the peak-to-peak ripple current of the inductor.
- $f_{SW}$ is the switching frequency.

For a certain inductor, the inductor ripple current achieves maximum value when $V_{IN}$ equals to the half of the maximum output voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

For this application example, a 4.7-µH inductor is selected, which produces approximate maximum inductor current ripple of 50% of the highest average inductor current in buck mode and 50% of the highest average inductor current in boost mode.

In buck mode, the inductor DC current equals to the output current. In boost mode, the inductor DC current can be calculated with Equation 11.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{11}$$

where

- $V_{OUT}$ is the output voltage.
- $I_{OUT}$ is the output current.
- $V_{IN}$ is the input voltage.
- $\eta$ is the power conversion efficiency.

For a given maximum output current of the TPS55287, the maximum inductor DC current happens at the minimum input voltage and maximum output voltage. Set the inductor current limit of the TPS55287 higher than the calculated maximum inductor DC current to make sure the TPS55287 has the desired output current capability.

In boost mode, the inductor ripple current is calculated with Equation 12.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{L \times f_{SW} \times V_{OUT}} \tag{12}$$

where

- $\Delta I_{L(P-P)}$ is the inductor ripple current.
- L is the inductor value.
- $f_{SW}$ is the switching frequency.
- $V_{OUT}$ is the output voltage.
- $V_{IN}$ is the input voltage.

Therefore, the inductor peak current is calculated with Equation 13.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \tag{13}$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI, but in the same way, load transient response time is increased. The selected inductor must have higher saturation current than the calculated peak current.

The conversion efficiency is dependent on the resistance of its current path. The switching loss associated with the switching MOSFETs, and the inductor core loss. Therefore, the overall efficiency is affected by the

inductor DC resistance (DCR), equivalent series resistance (ESR) at the switching frequency, and the core loss. Table 7-2 lists recommended inductors for the TPS55287. In this application example, the Coilcraft inductor XAL7070-472 is selected for its small size, high saturation current, and small DCR.

**Table 7-2. Recommended Inductors**

| Part Number | L (µH) | DCR (Maximum) (mΩ) | Saturation Current/Heat Rating Current (A) | Size (L × W × H mm) | Vendor(1) |
|---|---|---|---|---|---|
| XAL7070-472ME | 4.7 | 14.3 | 15.2/10.5 | 7.5 × 7.2 × 7.0 | Coilcraft |
| VCHA085D-4R7MS6 | 4.7 | 15.6 | 16.0/8.8 | 8.7 × 8.2 × 5.2 | Cyntec |
| IHLP4040DZER4R7M01 | 4.7 | 16.5 | 17/9.5 | 10.2 × 10.2 × 4.0 | Vishay |

(1) See the *Third-party Products* disclaimer.

#### 7.2.2.4 Input Capacitor

In buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitors is given by Equation 14.

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} \quad (14)$$

where

- $I_{CIN(RMS)}$ is the RMS current through the input capacitor.
- $I_{OUT}$ is the output current.

The maximum RMS current occurs at the output voltage is half of the input voltage, which gives $I_{CIN(RMS)} = I_{OUT} / 2$. Ceramic capacitors are recommended for their low ESR and high ripple current capability. A total of 20 µF effective capacitance is a good starting point for this application. Add a 0.1-µF/0402 package ceramic capacitor and place it close to VIN pin and GND pin to suppress high frequency noise.

#### 7.2.2.5 Output Capacitor

In boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by Equation 15, where the minimum input voltage and the maximum output voltage correspond to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (15)$$

where

- $I_{COUT(RMS)}$ is the RMS current through the output capacitor.
- $I_{OUT}$ is the output current.

In this example, the maximum output ripple RMS current is 2.5 A.

The ESR of the output capacitor causes an output voltage ripple given by Equation 16 in boost mode.

$$V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \times R_{COUT} \quad (16)$$

where

- $R_{COUT}$ is the ESR of the output capacitance.

The capacitance also causes a capacitive output voltage ripple given by Equation 17 in boost mode. When input voltage reaches the minimum value and the output voltage reaches the maximum value, there is the largest output voltage ripple caused by the capacitance.

$$V_{RIPPLE(CAP)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)}{C_{OUT} \times f_{SW}} \quad (17)$$

Typically, a combination of ceramic capacitors and bulk electrolytic capacitors is needed to provide low ESR, high ripple current, and small output voltage ripple. From the required output voltage ripple, use Equation 16 and Equation 17 to calculate the minimum required effective capacitance of the $C_{OUT}$.

Add a 0.1-µF/0402 package ceramic capacitor and place it close to VOUT pin and GND pin to suppress high frequency noise.

#### 7.2.2.6 Output Current Limit

The output current limit is implemented by placing a current sense resistor between the ISP and ISN pins along with setting a limit voltage between the ISP pin and the ISN pin through register 02h. The maximum value of the limit voltage between the ISP and ISN pins is 63.5 mV. The default limit voltage is 50 mV. The current sense resistor between the ISP and ISN pins should be selected to ensure that the output current limit is set high enough for output. The output current limit setting resistor is given by Equation 18.

$$R_{SNS} = \frac{V_{SNS}}{I_{OUT\_LIMIT}} \quad (18)$$

where

- $V_{SNS}$ is the current limit setting voltage between the ISP and ISN pins.
- $I_{OUT\_LIMIT}$ is the desired output current limit.

Because the power dissipation is large, make sure the current sense resistor has enough power dissipation capability with a large package.

#### 7.2.2.7 Loop Stability

The TPS55287 uses average current control scheme. The inner current loop uses internal compensation and requires the inductor value must be larger than $1.2/f_{SW}$. The outer voltage loop requires an external compensation. The COMP pin is the output of the internal voltage error amplifier. An external compensation network comprised of resistor and ceramic capacitors is connected to the COMP pin.

The TPS55287 operates in buck mode or boost mode. Therefore, both buck and boost operating modes require loop compensations. The restrictive one of both compensations is selected as the overall compensation from a loop stability point of view. Typically for a converter designed either work in buck mode or boost mode, the boost mode compensation design is more restrictive due to the presence of a right half plane zero (RHPZ).

The power stage in boost mode can be modeled by Equation 18.

$$G_{PS}(s) = \frac{R_{LOAD} \times (1-D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{ESRZ}}\right) \times \left(1 - \frac{s}{2\pi \times f_{RHPZ}}\right)}{1 + \frac{s}{2\pi \times f_P}} \quad (19)$$

where

- $R_{LOAD}$ is the output load resistance.
- D is the switching duty cycle in boost mode.
- $R_{SENSE}$ is the equivalent internal current sense resistor, which is 0.055 Ω.

The power stage has two zeros and one pole generated by the output capacitor and load resistance. Use Equation 20 to Equation 22 to calculate them.

$$f_P = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}} \quad (20)$$

$$f_{ESRZ} = \frac{1}{2\pi \times R_{COUT} \times C_{OUT}} \quad (21)$$

$$f_{RHPZ} = \frac{R_{LOAD} \times (1-D)^2}{2\pi \times L} \quad (22)$$

The internal transconductance amplifier together with the compensation network at the COMP pin constitutes the control portion of the loop. The transfer function of the control portion is shown by Equation 23.

$$G_C(s) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{COMZ}}\right)}{\left(1 + \frac{s}{2\pi \times f_{COMP1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{COMP2}}\right)} \quad (23)$$

where

- $G_{EA}$ is the transconductance of the error amplifier.
- $R_{EA}$ is the output resistance of the error amplifier.
- $V_{REF}$ is the reference voltage input to the error amplifier.
- $V_{OUT}$ is the output voltage.
- $f_{COMP1}$ and $f_{COMP2}$ are the pole's frequency of the compensation network.
- $f_{COMZ}$ is the zero's frequency of the compensation network.

The total open-loop gain is the product of $G_{PS}(s)$ and $G_C(s)$. The next step is to choose the loop crossover frequency, $f_C$, at which the total open-loop gain is 1, namely 0 dB. The higher in frequency that the loop gain stays above 0 dB before crossing over, the faster the loop response. It is generally accepted that the loop gain cross over 0 dB at the frequency no higher than the lower of either 1/10 of the switching frequency, $f_{SW}$, or 1/5 of the RHPZ frequency, $f_{RHPZ}$.

Then, set the value of $R_C$, $C_C$, and $C_P$ by Equation 24 to Equation 26.

$$R_C = \frac{2\pi \times V_{OUT} \times R_{SENSE} \times C_{OUT} \times f_C}{(1-D) \times V_{REF} \times G_{EA}} \quad (24)$$

where

- $f_C$ is the selected crossover frequency.

$$C_C = \frac{R_{LOAD} \times C_{OUT}}{2 \times R_C} \quad (25)$$

$$C_P = \frac{R_{COUT} \times C_{OUT}}{R_C} \quad (26)$$

If the calculated $C_P$ is less than 10 pF, it can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

### 7.2.3 Application Curves

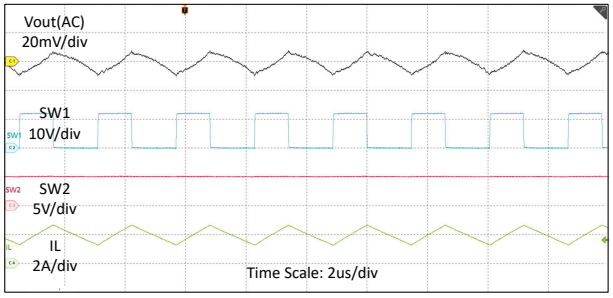



**Figure 7-2. Switching Waveforms in $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V, $I_O$ = 2 A, FPWM**

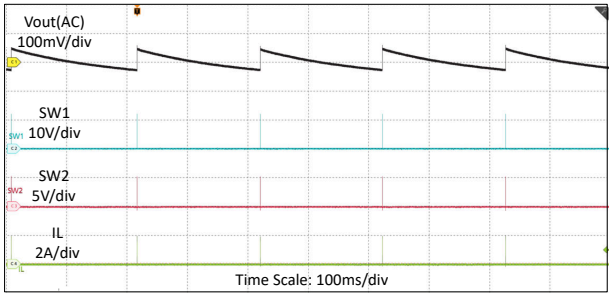



**Figure 7-3. Switching Waveforms in $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V, $I_O$ = 0 A, PFM**

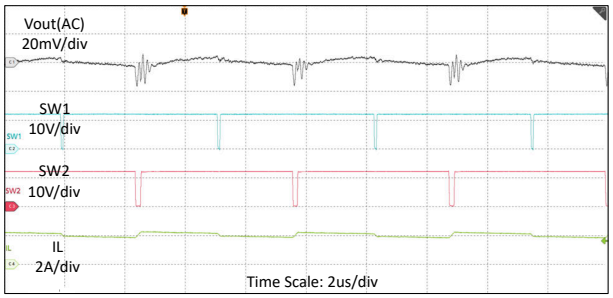



**Figure 7-4. Switching Waveforms in $V_{IN}$ = 12 V, $V_{OUT}$ = 12 V, $I_O$ = 2 A, FPWM**

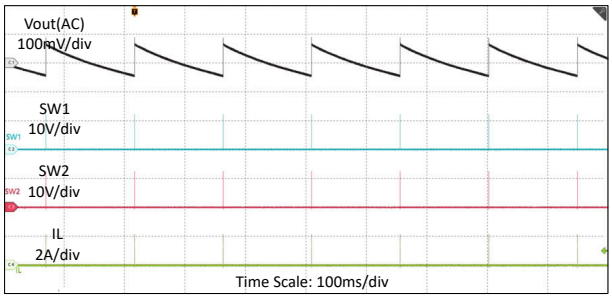



**Figure 7-5. Switching Waveforms in $V_{IN}$ = 12 V, $V_{OUT}$ = 12 V, $I_O$ = 0 A, PFM**

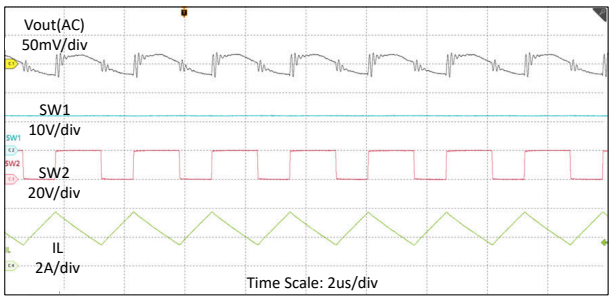



**Figure 7-6. Switching Waveforms in $V_{IN}$ = 12 V, $V_{OUT}$ = 20 V, $I_O$ = 1.5 A, FPWM**

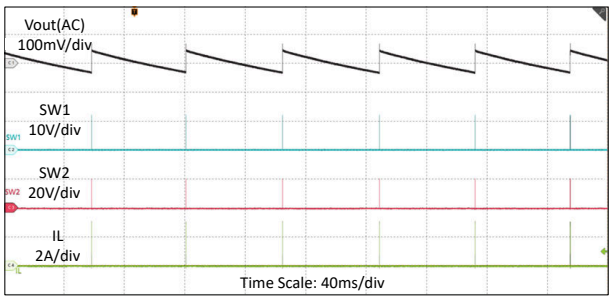



**Figure 7-7. Switching Waveforms in $V_{IN}$ = 12 V, $V_{OUT}$ = 20 V, $I_O$ = 0 A, PFM**

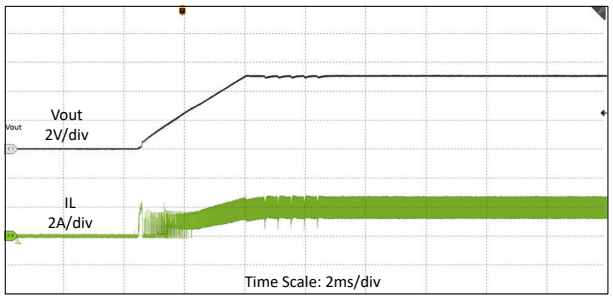



**Figure 7-8. Start-up Waveforms in $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V, $R_{LOAD}$ = 2.5 Ω, FPWM**

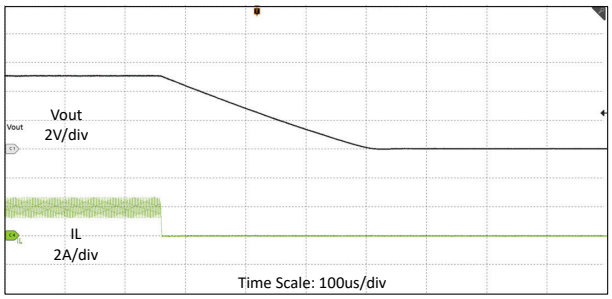



**Figure 7-9. Shutdown Waveforms in $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V, $R_{LOAD}$ = 2.5 Ω, FPWM**

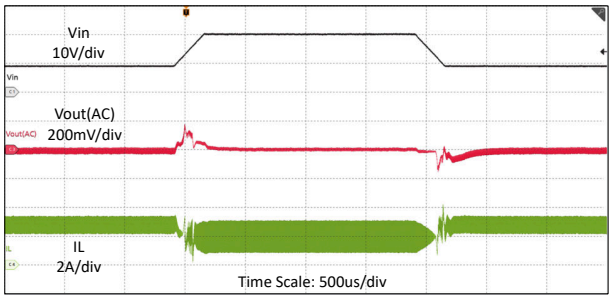



**Figure 7-10. Line Transient Waveforms in $V_{IN}$ = 9 V to 20 V, $V_{OUT}$ = 12 V, $I_O$ = 2 A with 200-µs Slew Rate, FPWM**

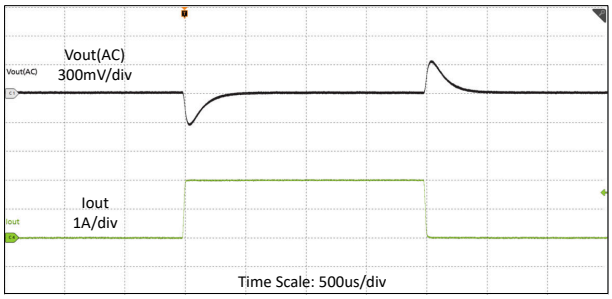



**Figure 7-11. Load Transient Waveforms in $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V, $I_O$ = 0 A to 2 A with 20-µs Slew Rate, FPWM**

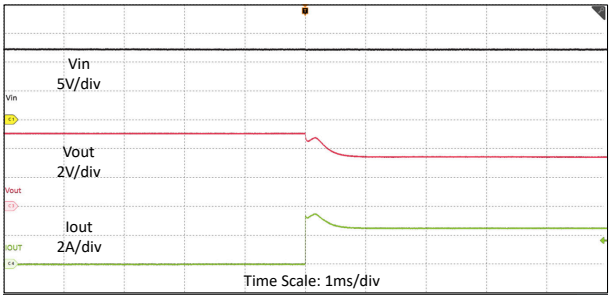



**Figure 7-12. Output Current Limit Waveforms in $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V, $R_{LOAD}$ = 1.5 Ω, $R_{SNS}$ = 20 mΩ FPWM**

# 8 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 3.0 V to 36 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an aluminum electrolytic capacitor with a value of 100 µF.

# 9 Layout

## 9.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator can suffer from instability and noise problems.

- Place the 0.1-µF small package (0402) ceramic capacitors close to the VIN/VOUT pins to minimize high frequency current loops. This improves the radiation of high-frequency noise (EMI) and efficiency.
- Use multiple GND vias near PGND pin to connect the PGND to the internal ground plane. This also improves thermal performance.
- Minimize the SW1 and SW2 loop areas as these are high dv/dt nodes. Use a ground plane under the switching regulator to minimize interplane coupling.
- Use Kelvin connections to $R_{SENSE}$ for the current sense signals ISP and ISN and run lines in parallel from the $R_{SENSE}$ terminals to the IC pins. Place the filter capacitor for the current sense signal as close to the IC pins as possible.
- Place the BOOT1 bootstrap capacitor close to the IC and connect directly to the BOOT1 to SW1 pins. Place the BOOT2 bootstrap capacitor close to the IC and connect directly to the BOOT2 and SW2 pins.
- Place the VCC capacitor close to the IC with wide and short trace. The GND terminal of the VCC capacitor should be directly connected with PGND plane through three to four vias.
- Isolate the power ground from the analog ground. The PGND plane and AGND plane are connected at the terminal of the VCC capacitor. Thus the noise caused by the MOSFET driver and parasitic inductance does not interface with the AGND and internal control circuit.
- Place the compensation components as close to the COMP pin as possible. Keep the compensation components, feedback components, and other sensitive analog circuitry far away from the power components, switching nodes SW1 and SW2, and high-current trace to prevent noise coupling into the analog signals.
- To improve thermal performance, it is recommended to use thermal vias beneath the TPS55287 connecting the VIN pin to a large VIN area, and the VOUT pin to a large VOUT area separately.

## 9.2 Layout Example

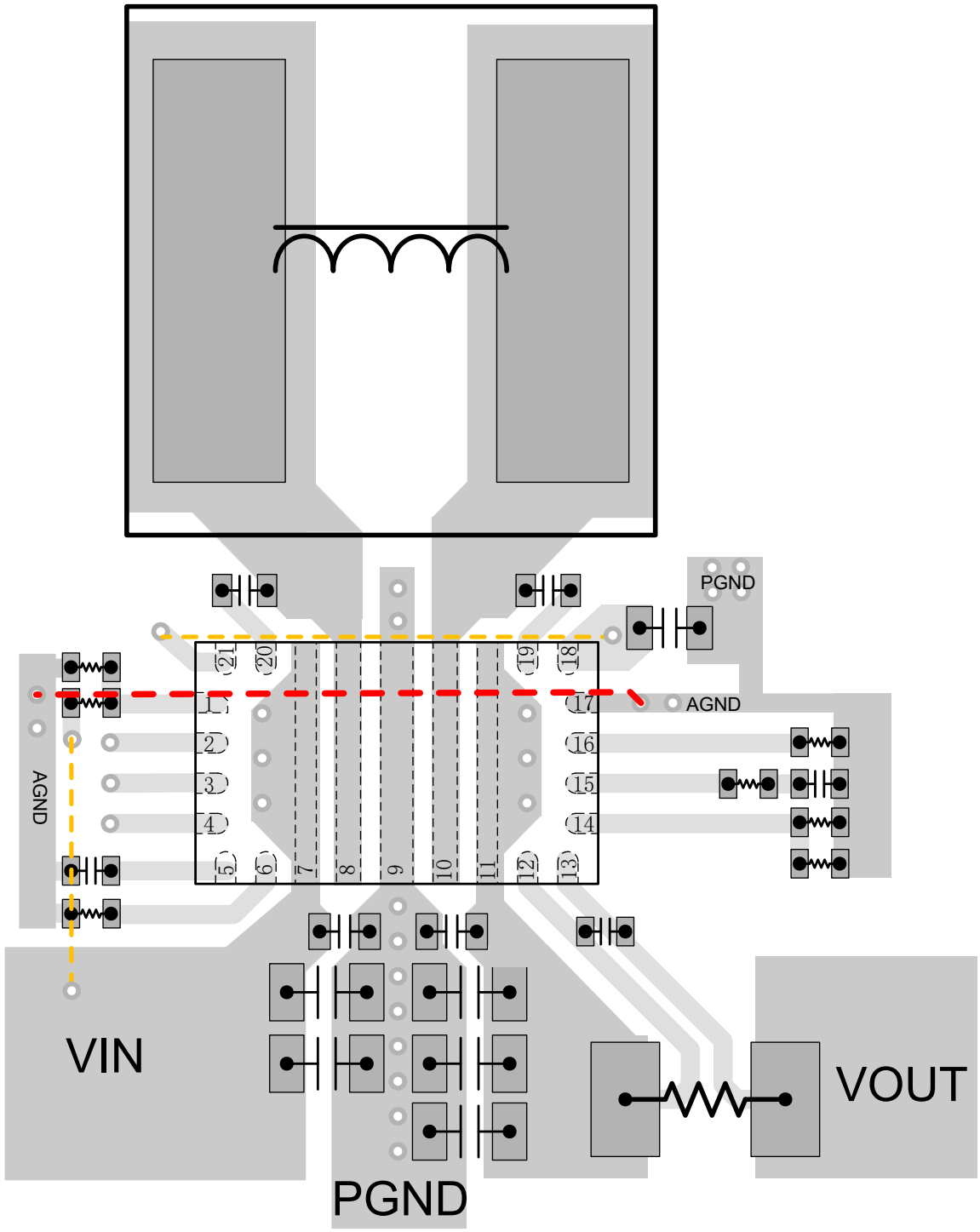



**Figure 9-1. Layout Example**

# 10 Device and Documentation Support

## 10.1 Device Support

### *10.1.1 Third-Party Products Disclaimer*

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 10.4 Trademarks

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## 10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| August 2024 | * | Initial Release |

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS55287RYQR | Active | Production | VQFN-HR (RYQ) \| 21 | 3000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 55287 |
| TPS55287RYQR.A | Active | Production | VQFN-HR (RYQ) \| 21 | 3000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 55287 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF TPS55287 :**

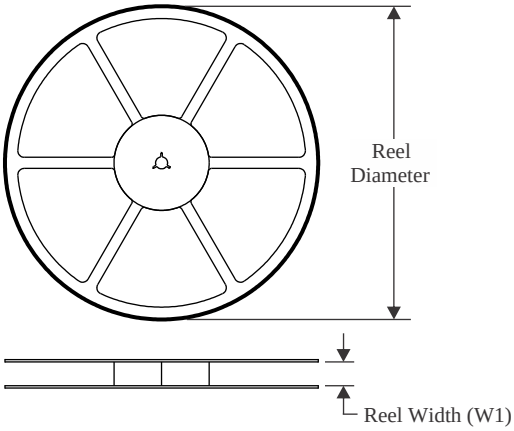
- Automotive : TPS55287-Q1

NOTE: Qualified Version Definitions:

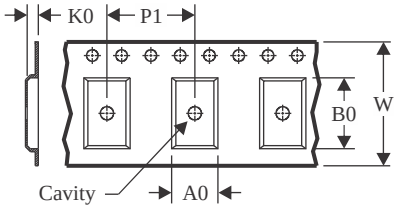
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

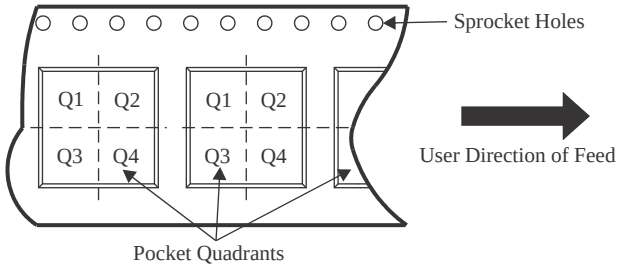



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

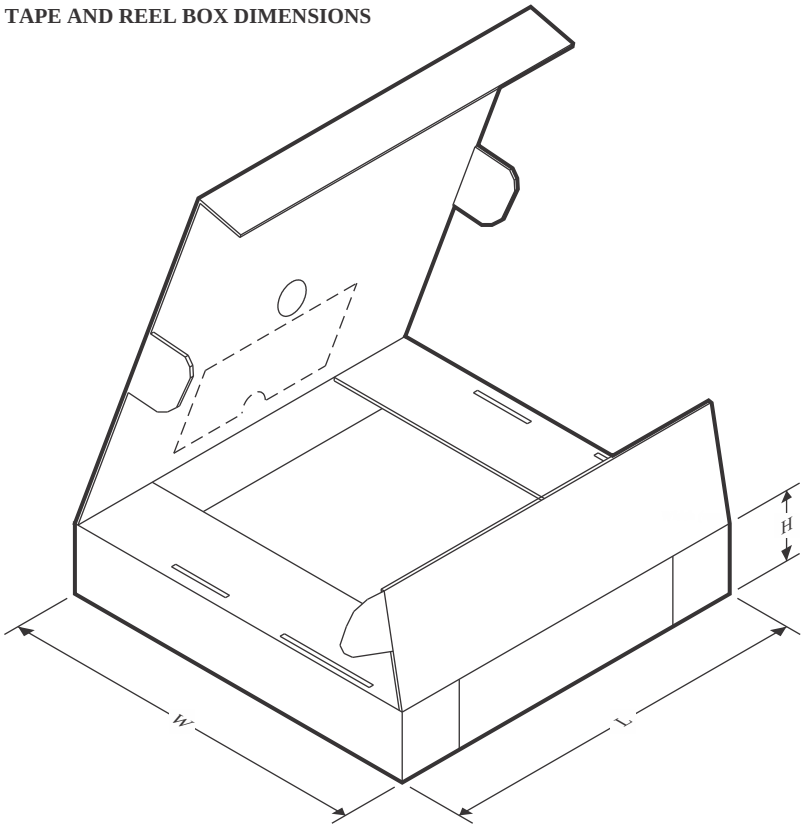
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS55287RYQR | VQFN-HR | RYQ | 21 | 3000 | 330.0 | 12.4 | 3.2 | 5.25 | 1.2 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS55287RYQR | VQFN-HR | RYQ | 21 | 3000 | 360.0 | 360.0 | 36.0 |

# GENERIC PACKAGE VIEW

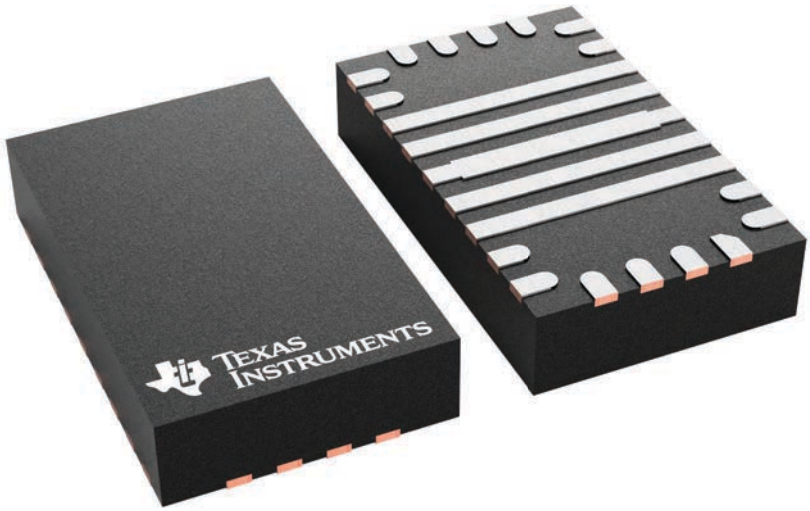
## RYQ 21

## VQFN - 1 mm max height

**5 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



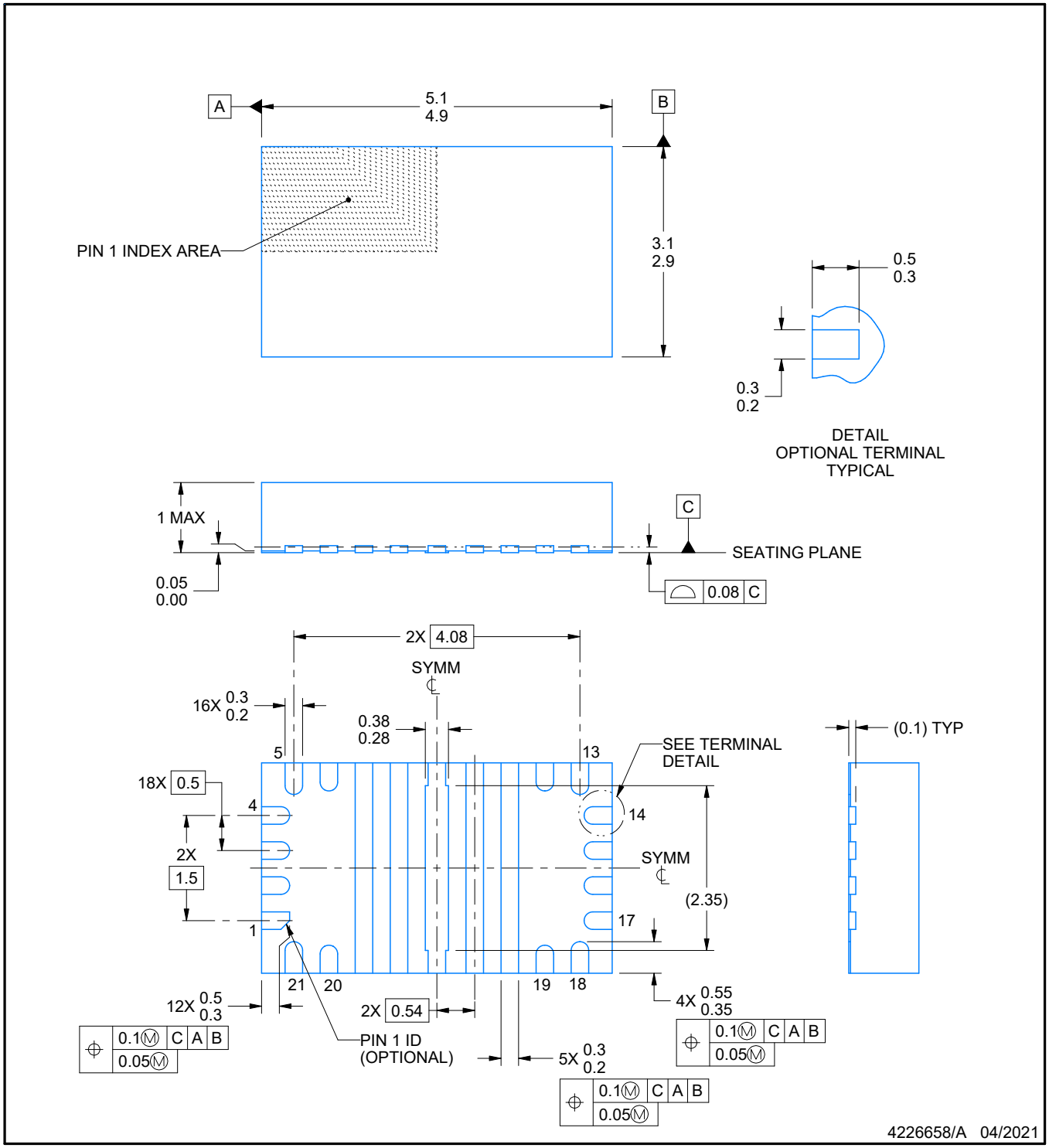

4228970/A

# RYQ0021A

# PACKAGE OUTLINE

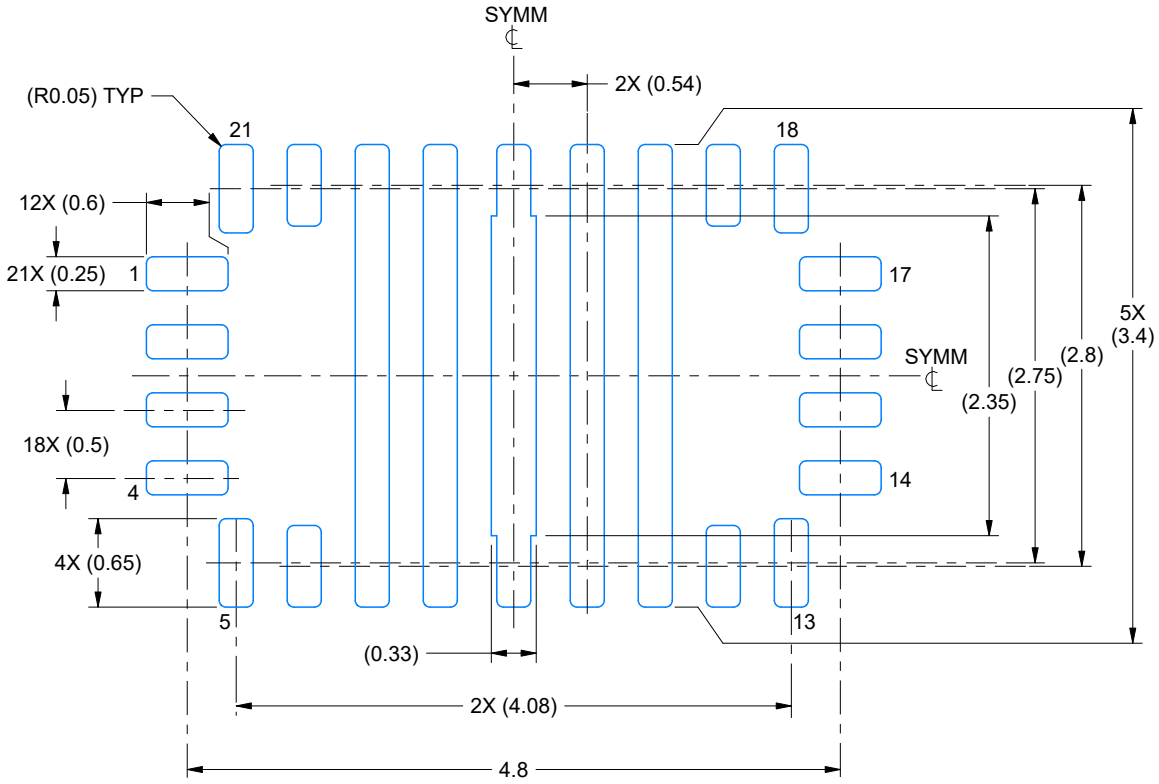
## VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

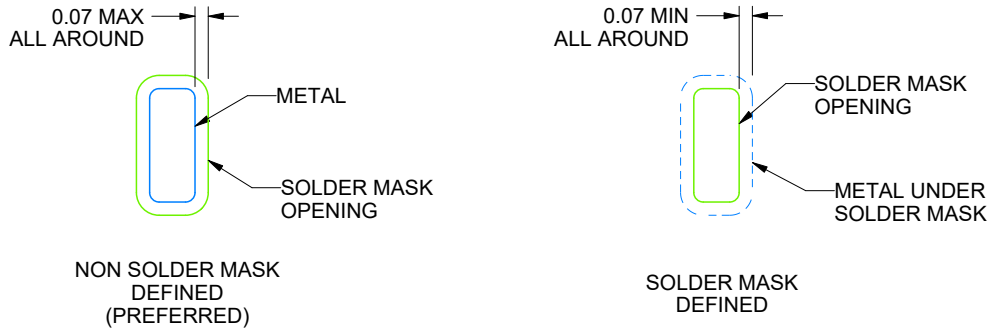



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:18X




SOLDER MASK DETAILS

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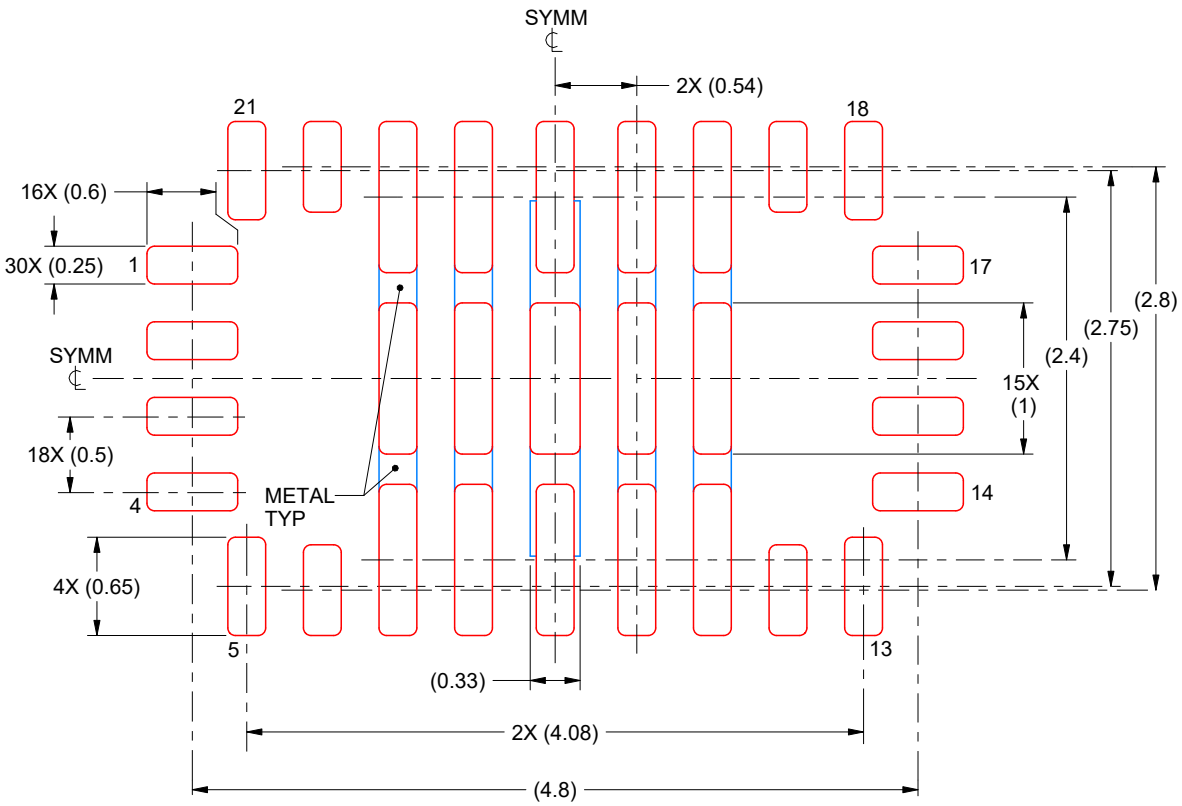
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PIN 7,8, 10 & 11 SOLDER COVERAGE = 88%
PIN 9 SOLDER COVERAGE = 64%
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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