



TPS56528 4.5-V to 18-V Input, 5-A Synchronous Step-Down Converter With Advanced Eco-Mode™

1 Features

- D-CAP2™ Mode Enables Fast Transient Response
- Low Output Ripple and Allows Ceramic Output Capacitor
- Wide V_{IN} Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.6 V to 7 V
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications –68 mΩ (High-Side) and 37 mΩ (Low-Side)
- High Efficiency, Less Than 10 μ A at Shutdown
- High Initial Band-Gap Reference Accuracy
- Prebiased Soft Start
- 650-kHz Switching Frequency (f_{SW})
- Cycle-By-Cycle Overcurrent Limit
- Advanced Auto-Skip Eco-Mode™ for High Efficiency at Light Load
- Power Good Output
- Fixed Soft Start: 1 ms

2 Applications

- Wide Range of Applications for Low Voltage Systems
 - Digital TV Power Supply
 - High Definition Blu-ray Disc™ Players
 - Networking Home Terminals
 - Digital Set-Top Boxes (STB)

3 Description

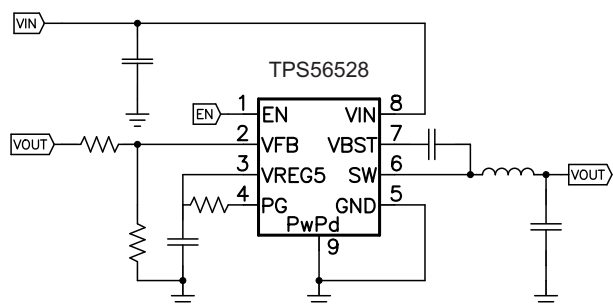
The TPS56528 device is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS56528 enables system designers to complete the suite of various end-equipment power bus regulators with a cost-effective, low component count, low standby current solution. The main control loop for the TPS56528 uses the D-CAP2™ mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and advanced Eco-Mode™ operation at light loads. Advanced Eco-Mode™ allows the TPS56528 to maintain high efficiency during lighter load conditions. The TPS56528 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V V_{IN} input. The output voltage can be programmed between 0.6 V and 7 V. The device also features a fixed 1-ms soft-start time and power good output. The TPS56528 is available in the 8-pin SO PowerPAD™ package, and designed to operate from –40°C to 85°C.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS56528	SO PowerPAD (8)	4.89 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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Transient Response

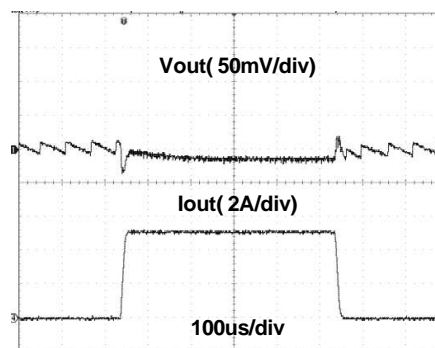


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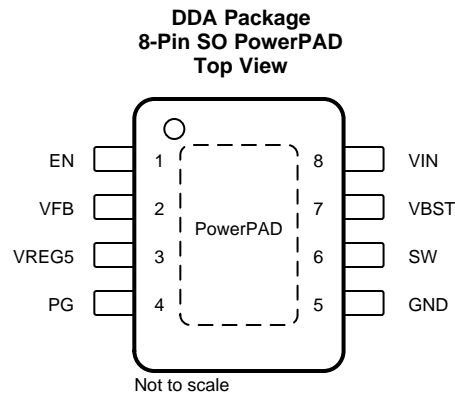
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2013) to Revision B	Page
<ul style="list-style-type: none"> Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1

Changes from Original (April 2013) to Revision A	Page
<ul style="list-style-type: none"> Changed the device From: Product Preview To: Production 	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	EN	I	Enable input control. EN is active high and must be pulled up to enable the device.
2	VFB	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
3	VREG5	O	5.5-V power supply output. A capacitor (0.47 μ F typical) must be connected to GND. VREG5 is not active when EN is low.
4	PG	O	Open-drain power good output.
5	GND	—	Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
6	SW	O	Switch node connection between high-side NFET and low-side NFET.
7	VBST	O	Supply input for the high-side FET gate drive circuit. Connect 0.1- μ F capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
8	VIN	I	Input voltage supply pin.
—	PowerPAD	—	Thermal pad of the package. This pad must be soldered to achieve appropriate dissipation and must be connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	VIN and EN	−0.3	20	V
	VBST	−0.3	26	
	VBST (10-ns-transient)	−0.3	28	
	VBST (vs SW)	−0.3	6.5	
	VFB and PG	−0.3	6.5	
	SW	−2	20	
	SW (10-ns-transient)	−3	22	
Output voltage	VREG5	−0.3	6.5	V
	GND	−0.3	0.3	
Voltage from GND to thermal pad, V _{diff}		−0.2	0.2	V
Operating junction temperature, T _J		−40	150	°C
Storage temperature, T _{stg}		−55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Supply input voltage	4.5	18	V
V _I	Input voltage	VBST	−0.1	24
		VBST (10-ns-transient)	−0.1	27
		VBST(vs SW)	−0.1	6
		PG	−0.1	5.7
		EN	−0.1	18
		VFB	−0.1	5.5
		SW	−1.8	18
		SW (10-ns-transient)	−3	21
		GND	−0.1	0.1
V _O	Output voltage (VREG5)	−0.1	5.7	V
I _O	Output current (I _{VREG5})	0	5	mA
T _A	Operating free-air temperature	−40	85	°C
T _J	Operating junction temperature	−40	150	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS56528	UNIT
		DDA (SO PowerPAD)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	44.4	°C/W
R _{θJCTop}	Junction-to-case (top) thermal resistance	51.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	27.8	°C/W
ψ _{JT}	Junction-to-top characterization parameter	8.7	°C/W
ψ _{JB}	Junction-to-board characterization parameter	27.7	°C/W
R _{θJCbot}	Junction-to-case (bottom) thermal resistance	5.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _(VIN)	Operating non-switching supply current	V _{IN} current, T _A = 25°C, EN = 5 V, V _(FB) = 0.7 V		170	350	μA
I _(VINSN)	Shutdown supply current	V _{IN} current, T _A = 25°C, EN = 0 V		3.8	10	μA
LOGIC THRESHOLD						
V _(EN)	EN high-level input voltage	EN	1.6			V
	EN low-level input voltage	EN			0.6	V
R _(EN)	EN pin resistance to GND	V _{EN} = 12 V	180	350	700	kΩ
V _{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V _(FBTH)	V _(FB) threshold voltage	T _A = 25°C, V _O = 1.05 V, I _O = 10 mA, advanced Eco-Mode operation		606		mV
		T _A = 25°C, V _O = 1.05 V, continuous mode operation	593	600	607	mV
		T _A = -40 to 85°C, V _O = 1.05 V, continuous mode operation ⁽¹⁾	588	600	612	mV
I _(VFB)	V _(FB) input current	V _(FB) = 0.7 V, T _A = 25°C		0	±0.15	μA
SW DISCHARGE						
I _(DISCHG)	SW discharge current	EN = 0 V, SW = 1 V, T _A = 25°C	1	1.5		mA
V _(REG5) OUTPUT						
V _(VREG5)	V _{REG5} output voltage	T _A = 25°C, 6.0 V < V _{IN} < 18 V, 0 < I _(VREG5) < 5 mA	5.2	5.5	5.7	V
I _(VREG5)	Output current	V _{IN} = 6 V, V _(REG5) = 4 V, T _A = 25°C	20			mA
MOSFET						
R _{DS(on)}	High-side switch resistance	25°C, V _(BST) - SW = 5.5 V		68		mΩ
	Low-side switch resistance	25°C		37		mΩ
CURRENT LIMIT						
I _(ocd)	Current limit	L _{OUT} = 1.5 μH ⁽¹⁾	5.5	6.2	7.8	A
THERMAL SHUTDOWN						
T _(SDN)	Thermal shutdown threshold	Shutdown temperature ⁽¹⁾		165		°C
		Hysteresis ⁽¹⁾		35		
POWER GOOD						
V _(THPG)	PG threshold	VFB rising (good)	85%	90%	95%	
		VFB falling (Fault)		85%		
IPG	PG sink current	PG = 0.5 V	2	4		mA

(1) Not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range, $V_{IN} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V _{OVP}	Output OVP threshold	OVP Detect (L>H)	125%			
V _{UVP}	Output UVP threshold	UVP detect (H>L)	65%			
UVLO						
UVLO	UVLO threshold	Wake-up V _{REG5} voltage	3.45	3.75	4.05	V
		Hysteresis V _{REG5} voltage	0.13	0.32	0.48	

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
ON-TIME TIMER CONTROL						
t _{ON}	On-time	V _{IN} = 12 V, V _O = 1.05 V	150			ns
t _{OFF(MIN)}	Minimum off-time	T _A = 25°C, V _{FB} = 0.5 V	260	310	ns	
SOFT START						
t _{SS}	Soft-start time	Internal soft-start time	0.7	1	1.3	ms
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
t _{UVPDEL}	Output UVP delay	to hiccup state	7			μs
t _{UVPEN}	Output UVP enable delay	Relative to soft-start time	x1.7			

6.7 Typical Characteristics

$V_{IN} = 12\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

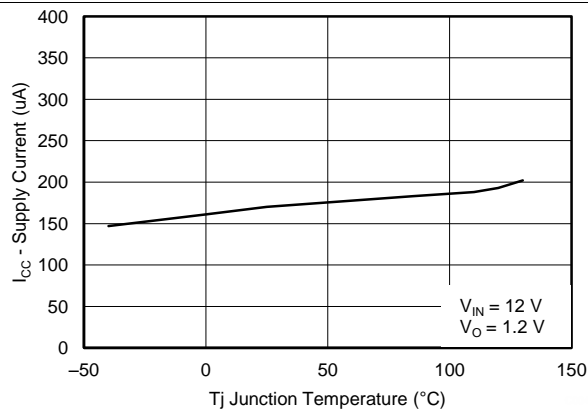


Figure 1. VIN Supply Current vs Junction Temperature

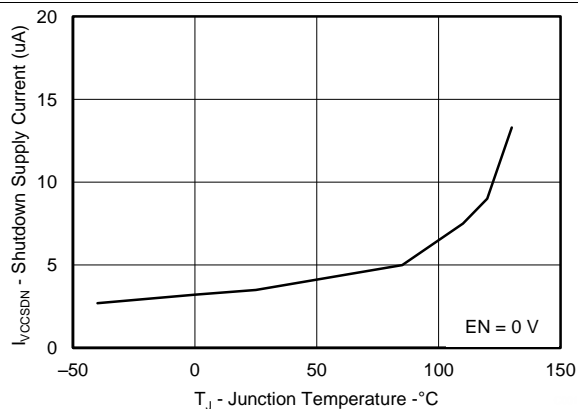


Figure 2. VIN Shutdown Current vs Junction Temperature

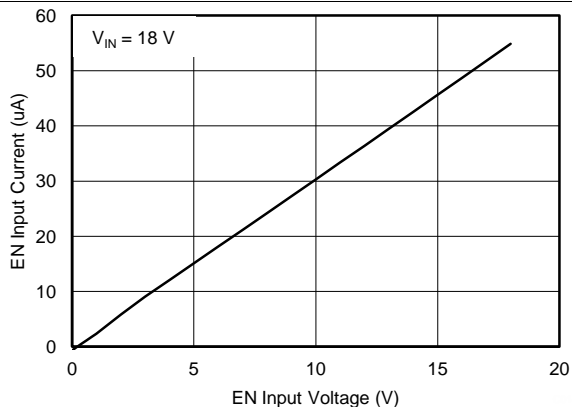


Figure 3. EN Current vs EN Voltage

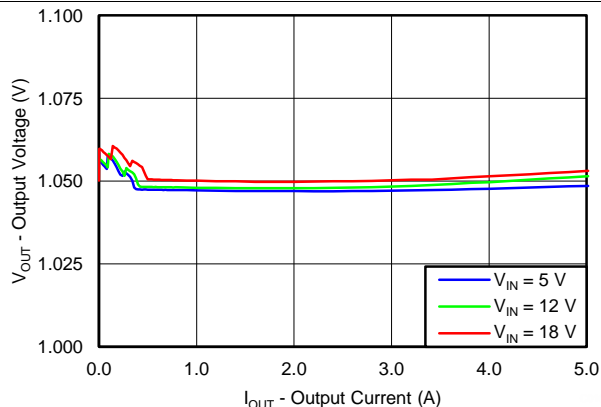


Figure 4. 1.05-V Output Voltage vs Output Current

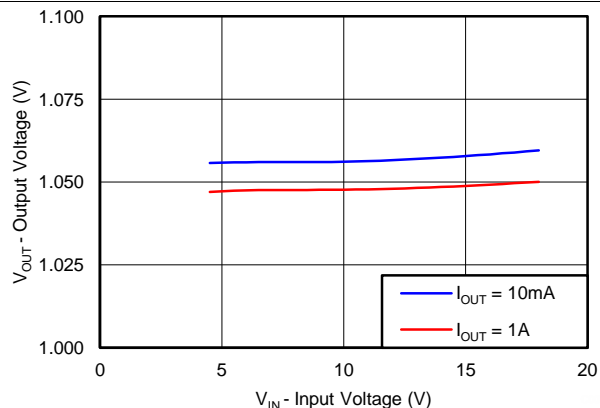


Figure 5. 1.05-V Output Voltage vs Input Voltage

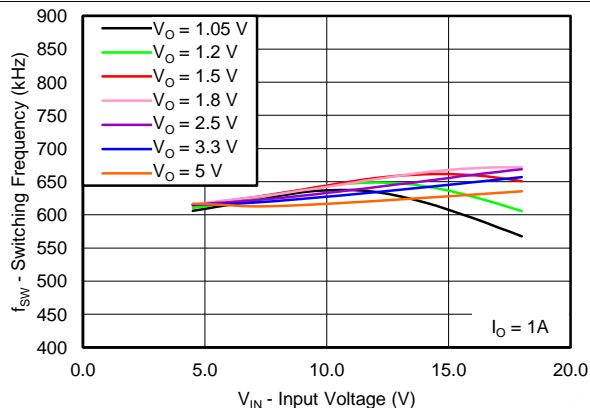


Figure 6. Switching Frequency vs Input Voltage

Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

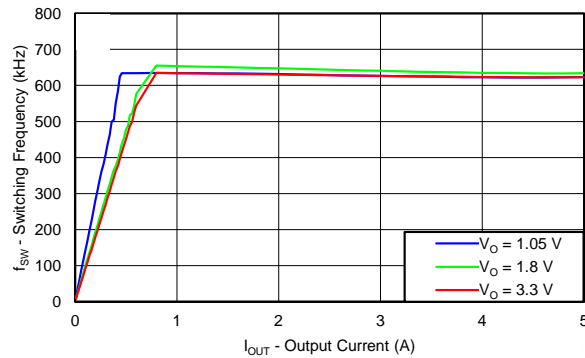


Figure 7. Switching Frequency vs Output Current

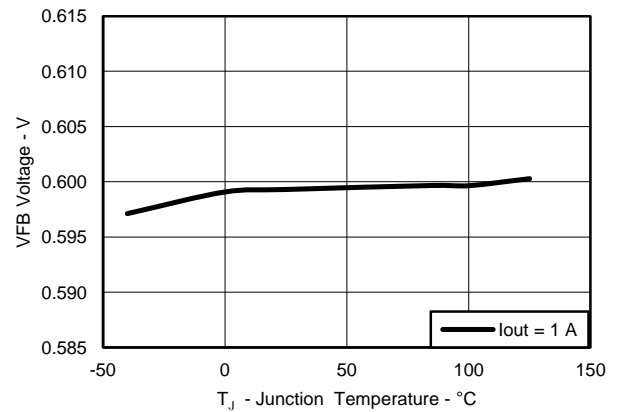


Figure 8. VFB Voltage vs Junction Temperature

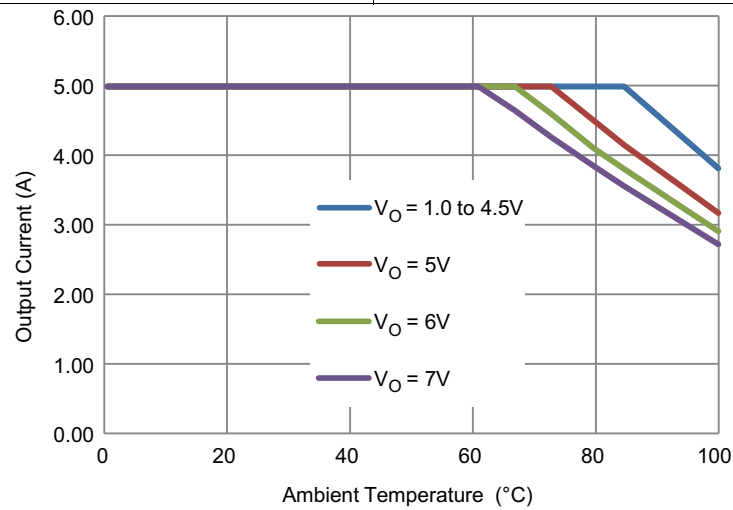


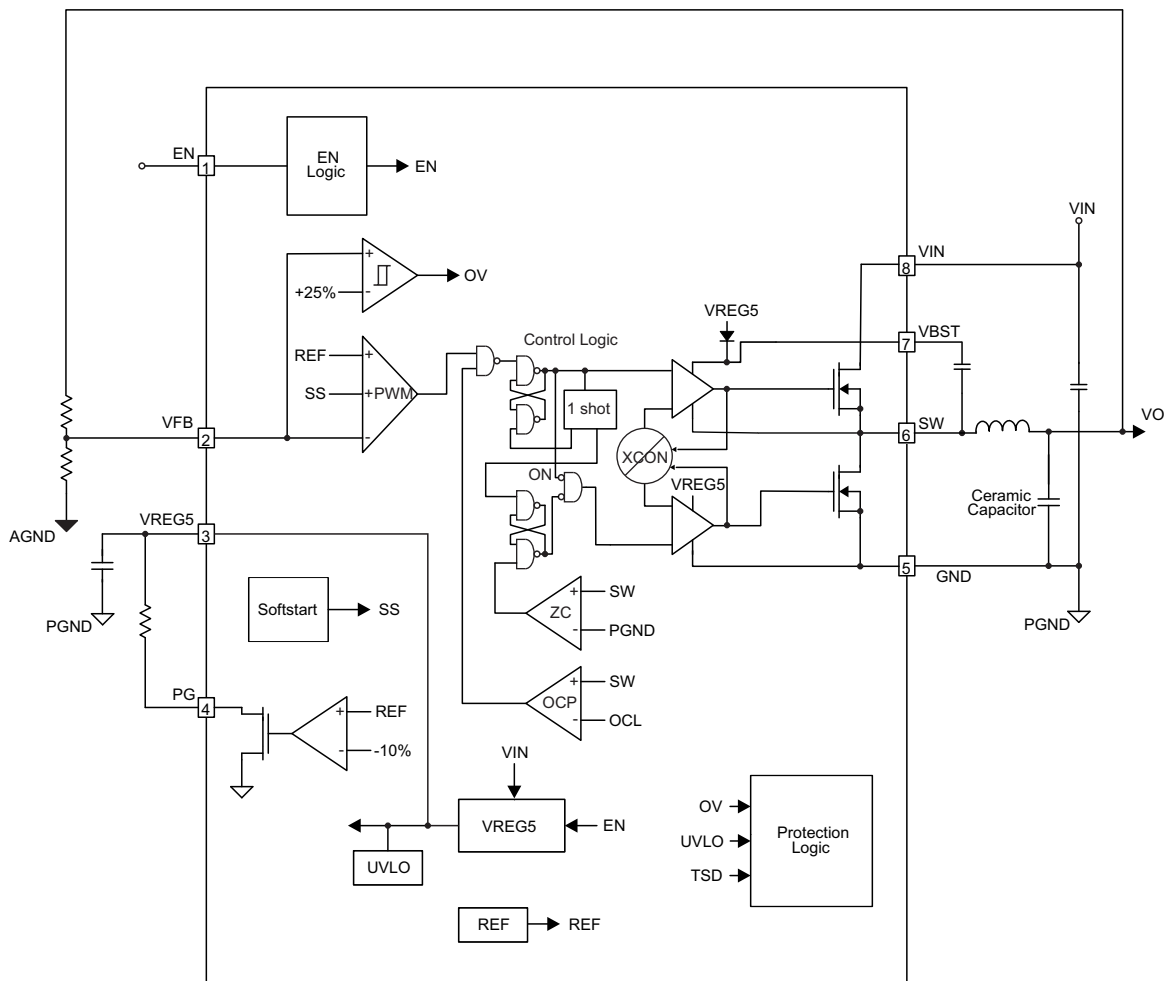
Figure 9. Output Current vs Ambient Temperature

7 Detailed Description

7.1 Overview

The TPS5652 is a 5-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low-ESR output capacitors including ceramic and special polymer types. And also PG output can be used for sequence operation.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 PWM Operation

The main control loop of the TPS56528 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one shot is set by the converter input voltage, V_{IN} , and the output voltage, V_O , to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the requirement for ESR-induced output ripple from D-CAP2™ mode control.

7.3.2 PWM Frequency and Adaptive On-Time Control

TPS56528 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS56528 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage; therefore, when the duty ratio is V_{OUT}/V_{IN} , the frequency is constant.

7.3.3 Soft Start and Prebiased Soft Start

The TPS56528 has an internal 1-ms soft start. When the EN pin becomes high, internal soft-start function begins ramping up the reference voltage to the PWM comparator.

The TPS56528 contains a unique circuit to prevent current from being pulled from the output during start-up if the output is prebiased. When the soft start commands a voltage higher than the prebias level (internal soft start becomes greater than feedback voltage V_{FB}), the controller slowly activates synchronous rectification by starting the first low-side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by $(1-D)$, where D is the duty cycle of the converter. This scheme prevents the initial sinking of the prebias output, and ensure that the out voltage (V_O) starts and ramps up smoothly into regulation and the control loop is given time to transition from prebiased start-up to normal mode operation.

7.3.4 Power Good

The power good function is activated after soft start has finished. The power good function becomes active after $1.7 \times$ soft-start time. When the output voltage becomes within -10% of the target value, internal comparators detect power good state and the power good signal becomes high. The power good output, PG is an open-drain output. If the feedback voltage goes under 15% of the target value, the power good signal becomes low.

7.3.5 Output Discharge Control

TPS56528 discharges the output through the SW pin when EN is low, or the controller is turned off by the protection functions (UVP, UVLO and thermal shutdown). The internal regular low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

7.3.6 Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN} , V_{OUT} , the on-time and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current, I_{OUT} . The TPS56528 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching

Feature Description (continued)

cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of overcurrent protection. The peak current is the average load current plus one half of the peak-to-peak inductor current. The valley current is the average load current minus one half of the peak-to-peak inductor current. Because the valley current is used to detect the overcurrent threshold, the load current is higher than the overcurrent threshold. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This protection is non-latching. When the VFB voltage becomes lower than 65% of the target voltage, the UVP comparator detects it. After 7 μ s detecting the UVP voltage, device shut downs and restarts after hiccup time.

When the overcurrent condition is removed, the output voltage returns to the regulated value.

7.3.7 UVLO Protection

Undervoltage lockout protection (UVLO) monitors the voltage of the V_{REG5} pin. When the V_{REG5} voltage is lower than UVLO threshold voltage, the TPS56528 is shut off. This protection is non-latching.

7.3.8 Thermal Shutdown

TPS56528 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.

7.4 Device Functional Modes

7.4.1 Advanced Auto-Skip Eco-Mode™ Control

The TPS56528 is designed with advanced auto-skip Eco-Mode™ to increase higher light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced. If the output current is reduced enough, the inductor current ripple valley reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying low-side MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept approximately the same as is in continuous conduction mode. The off-time increases as it takes more time to discharge the output capacitor to the level of the reference voltage with smaller load current. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in [Equation 1](#).

$$I_{OUT(LL)} = \frac{1}{2 \cdot L \cdot f_{sw}} \cdot \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \quad (1)$$

8 Application and Implementation

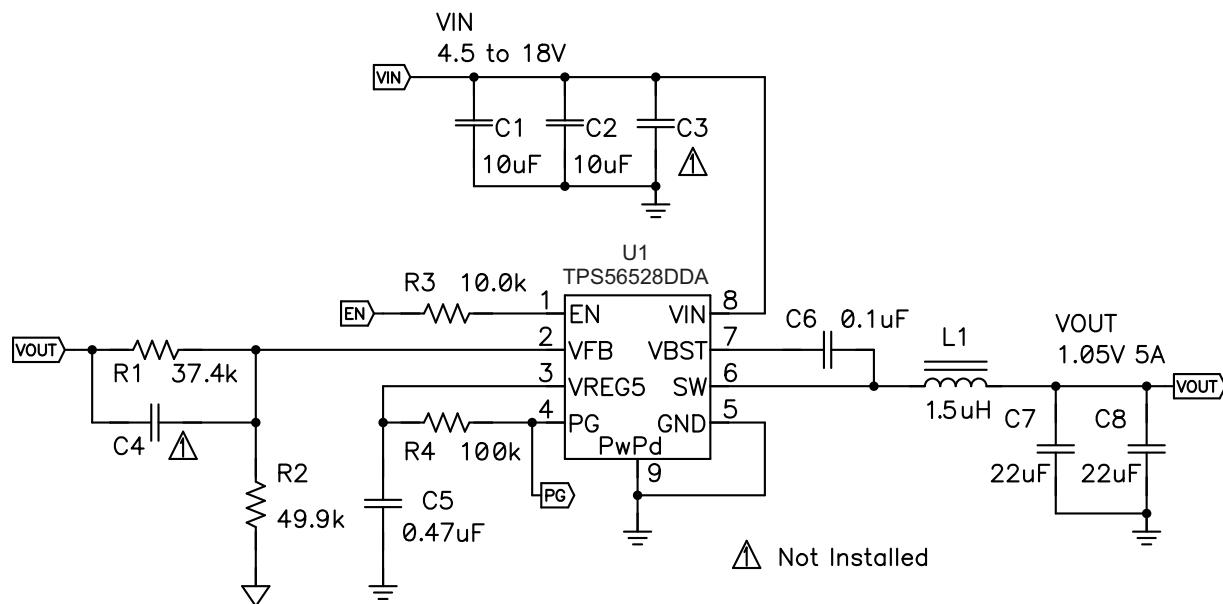
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS56528 is a 4.5-V to 18-V input step-down DC-DC converter with an output voltage adjustable from 0.6 V to 7 V and capable of output currents up to 5 A.

8.2 Typical Application



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Figure 10. Typical Application Schematic

8.2.1 Design Requirements

Table 1 lists the design parameters for this application example.

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage range, V_{IN}	4.5 to 18 V
Output voltage, V_{OUT}	1.05 V
Output current, I_{OUT}	5 A
Switching Frequency	650 KHz
Output voltage ripple, V_{OUT} ripple	< 20 mV
Input voltage ripple, V_{IN} ripple	< 100 mV

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends using 1% tolerance or better divider resistors. Start by using [Equation 2](#) to calculate V_{OUT} .

To improve efficiency at light loads, consider using larger value resistors, high resistance is more susceptible to noise, and the voltage errors from the VFB input current are more noticeable.

$$V_{OUT} = 0.60 \times \left(1 + \frac{R1}{R2} \right) \quad (2)$$

8.2.2.2 Output Filter Selection

The output filter used with the TPS56528 is an LC circuit. This LC filter has double pole in [Equation 3](#).

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output setpoint resistor divider network and the internal gain of the TPS56528. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of [Equation 3](#) is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement, use the values recommended in [Table 2](#).

Table 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF) ⁽¹⁾			L1 (μH)			C7 + C8 (μF)
			MIN	TYP	MAX	MIN	TYP	MAX	
1	33.2	49.9	5	33	100	1	1.5	4.7	20 to 68
1.05	37.4	49.9	5	33	100	1	1.5	4.7	20 to 68
1.2	49.9	49.9	5	22	47	1	1.5	4.7	20 to 68
1.5	75.0	49.9	5	15	33	1	1.5	4.7	20 to 68
1.8	100	49.9	5	10	22	1	1.5	4.7	20 to 68
2.5	158	49.9	5	10	22	1.5	2.2	4.7	20 to 68
3.3	226	49.9	2	5	15	1.5	2.2	4.7	20 to 68
5	365	49.9	2	5	10	2.2	3.3	4.7	20 to 68
6.5	487	49.9	2	2	10	2.2	3.3	4.7	20 to 68

(1) Optional

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed-forward capacitor (C4) in parallel with R1

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using [Equation 4](#), [Equation 5](#), and [Equation 6](#). The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f_{SW} .

Ensure the chosen inductor is rated for the peak current of [Equation 5](#) and the RMS current of [Equation 6](#).

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (6)$$

For this design example, the calculated peak current is 5.51 A and the calculated RMS current is 5.01 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS56528 is intended for use with ceramic or other low-ESR capacitors. Recommended values range from 20 μ F to 68 μ F. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{Co(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design, two TDK C3216X5R0J226M 22- μ F output capacitors are used. The typical ESR is 2 m Ω each. The calculated RMS current is 0.284 A and each output capacitor is rated for 4 A.

8.2.2.3 Input Capacitor Selection

The TPS56528 requires an input decoupling capacitor and a bulk capacitor is required depending on the application. A ceramic capacitor over 10 μ F is recommended for the decoupling capacitor. An additional 0.1- μ F capacitor (C3) from pin 8 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating requires greater than the maximum input voltage.

8.2.2.4 Bootstrap Capacitor Selection

A 0.1- μ F ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends using a ceramic capacitor.

8.2.2.5 VREG5 Capacitor Selection

A 0.47- μ F ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. TI recommends using a ceramic capacitor.

8.2.3 Application Curves

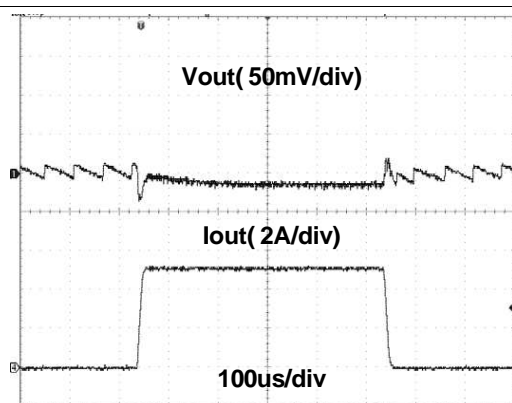


Figure 11. 1.05-V, Load Transient Response

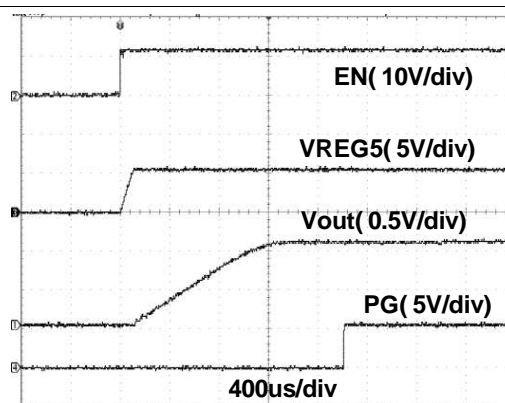


Figure 12. Start-Up Waveform

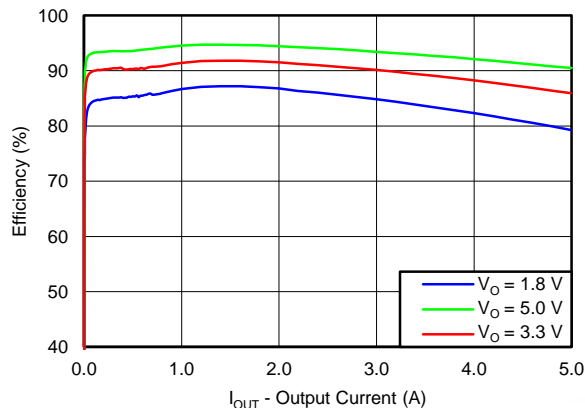


Figure 13. Efficiency vs Output Current

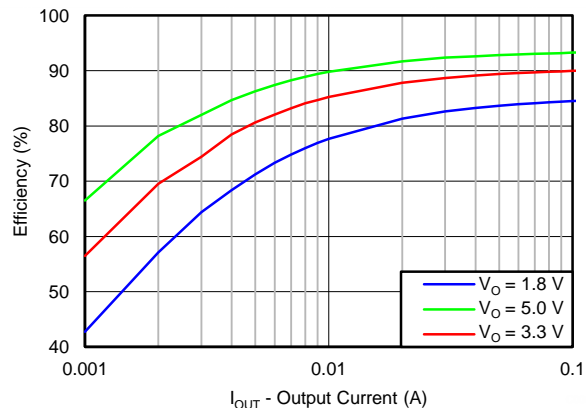
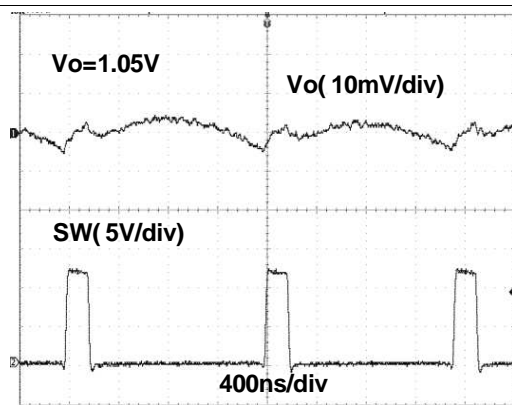
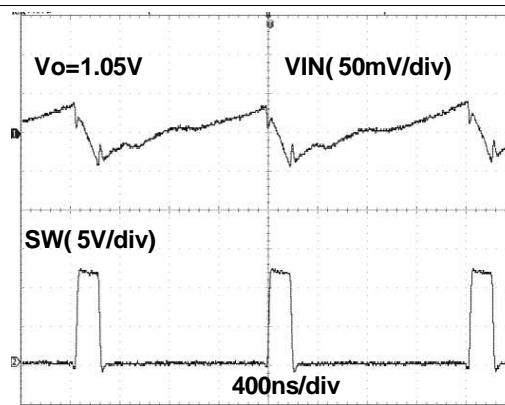


Figure 14. Light Load Efficiency vs Output Current



($I_O = 5\text{ A}$)

Figure 15. Voltage Ripple at Output



($I_O = 5\text{ A}$)

Figure 16. Voltage Ripple at Input

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 4.5 V and 18 V. This input supply must be well regulated. If the input supply is placed more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 μF is a typical choice.

10 Layout

10.1 Layout Guidelines

1. The TPS56528 can supply large load currents up to 5 A, so heat dissipation may be a concern. The top-side area adjacent to the TPS56528 must be filled with ground as much as possible to dissipate heat.
2. The bottom side area directly below the IC must a dedicated ground area. It must be directed connected to the thermal pad of the device using vias as shown. The ground area must be as large as practical. Additional internal layers can be dedicated as ground planes and connected to vias as well.
3. Keep the input switching current loop as small as possible.
4. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections must be brought from the output to the feedback pin of the device.
5. Keep analog and non-switching components away from switching components.
6. Make a single point connection from the signal ground to power ground.
7. Do not allow switching current to flow under the device.
8. Keep the pattern lines for VIN and PGND broad.
9. Exposed pad of device must be connected to PGND with solder.
10. VREG5 capacitor must be placed near the device, and connected to PGND.
11. Output capacitor must be connected to a broad pattern of the PGND.
12. Voltage feedback loop must be as short as possible, and preferably with ground shield.
13. Lower resistor of the voltage divider which is connected to the VFB pin must be tied to SGND.
14. Providing sufficient via is preferable for VIN, SW, and PGND connection.
15. PCB pattern for VIN, SW, and PGND must be as broad as possible.
16. VIN capacitor must be placed as near as possible to the device.

10.2 Layout Example

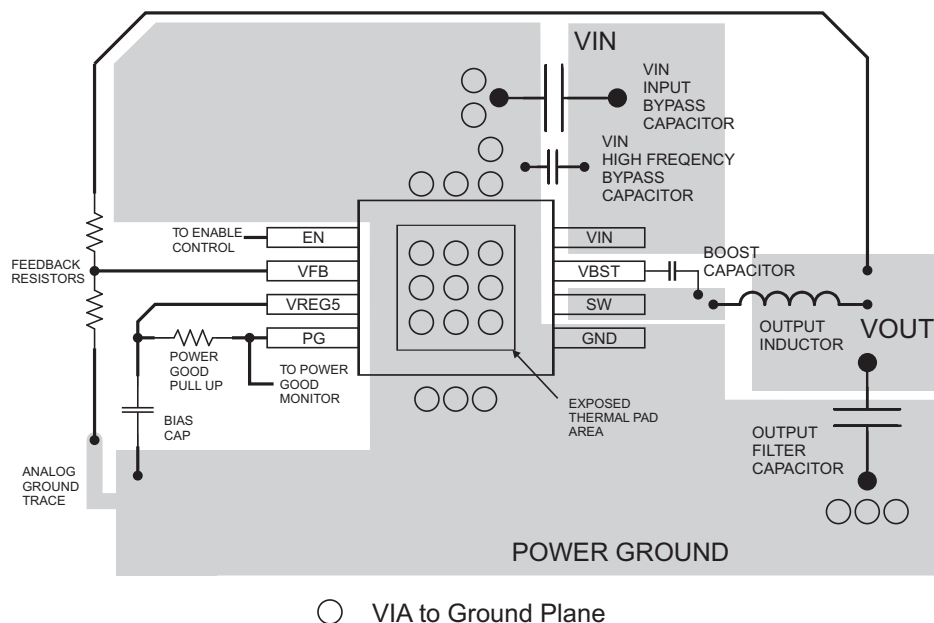


Figure 17. PCB Layout

10.3 Thermal Information

This 8-pin SO PowerPAD package incorporates an exposed thermal pad that is designed to be directly to an external heat sink. The thermal pad must be soldered directly to the printed-circuit board (PCB). After soldering, the PCB can be used as a heat sink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, see [PowerPAD™ Thermally Enhanced Package](#) (SLMA002) and [PowerPAD™ Made Easy](#) (SLMA004).

The exposed thermal pad dimensions for this package are shown in [Figure 18](#).

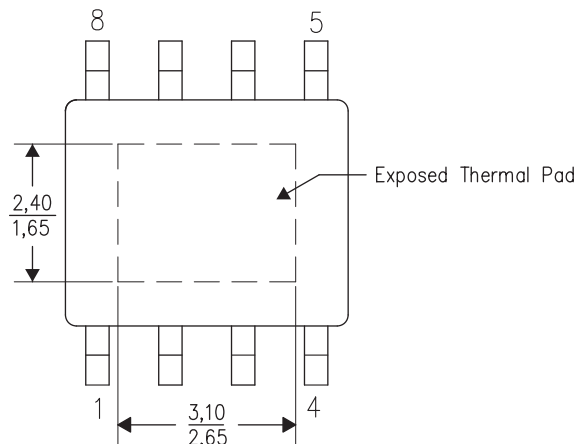


Figure 18. Thermal Pad Dimensions (Top View)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- [PowerPAD™ Thermally Enhanced Package](#) (SLMA002)
- [PowerPAD™ Made Easy](#) (SLMA004)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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Blu-ray Disc is a trademark of Blu-ray Disc Association.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS56528DDA	Active	Production	SO PowerPAD (DDA) 8	75 TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	56528
TPS56528DDA.A	Active	Production	SO PowerPAD (DDA) 8	75 TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	56528
TPS56528DDAR	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	56528
TPS56528DDAR.A	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	56528

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS56528DDAR	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS56528DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS56528DDA	DDA	HSOIC	8	75	517	7.87	635	4.25
TPS56528DDA.A	DDA	HSOIC	8	75	517	7.87	635	4.25



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



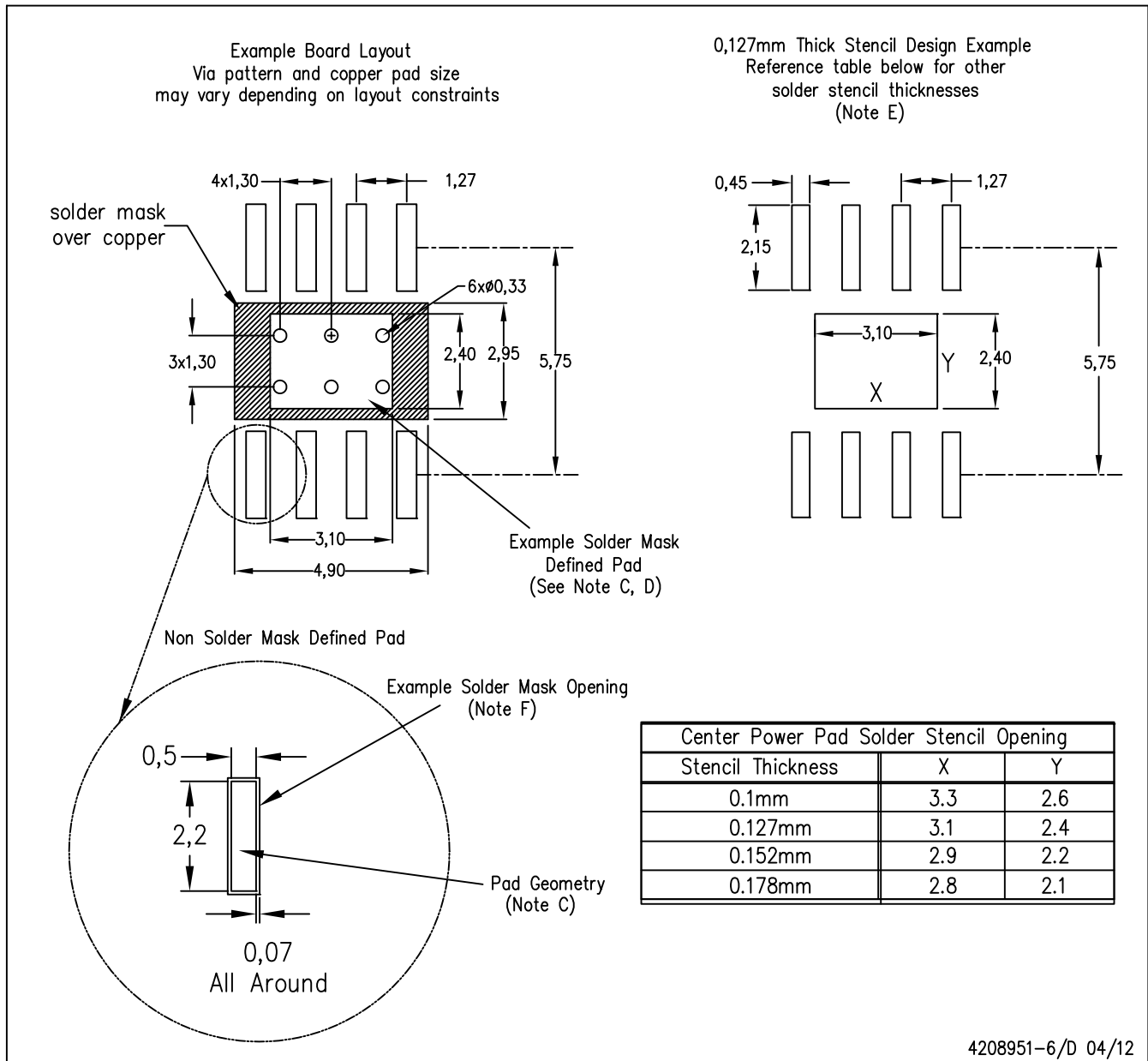
4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

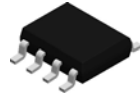
DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

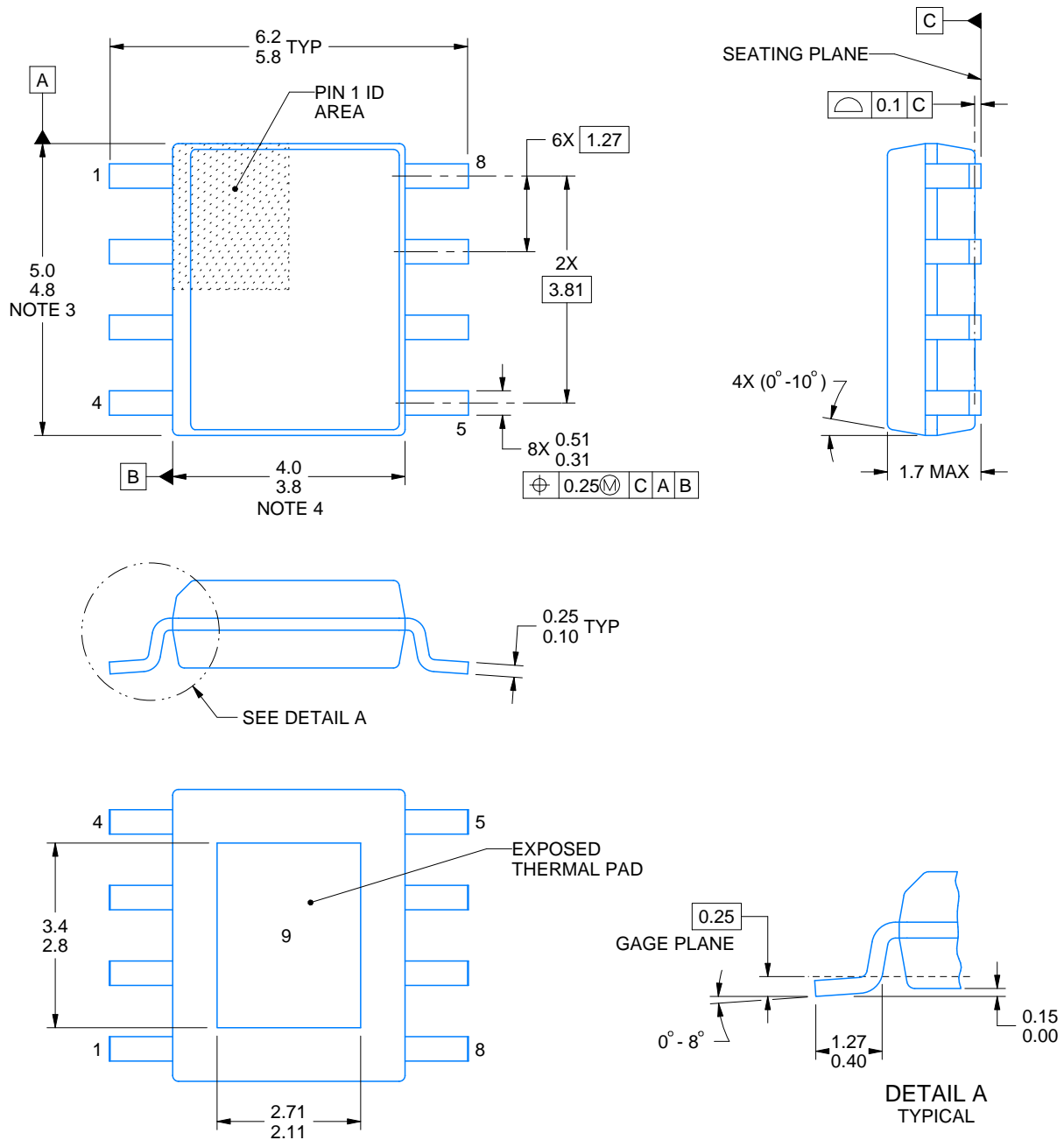
PowerPAD is a trademark of Texas Instruments.

DDA0008B

PACKAGE OUTLINE

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

PowerPAD is a trademark of Texas Instruments.

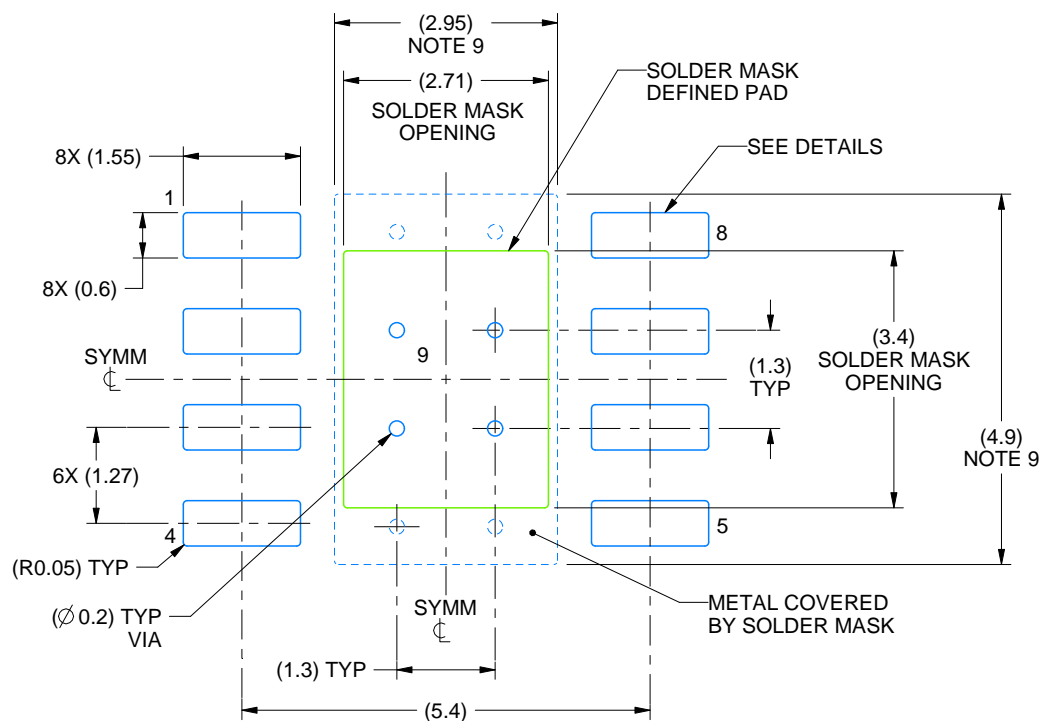
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

EXAMPLE BOARD LAYOUT

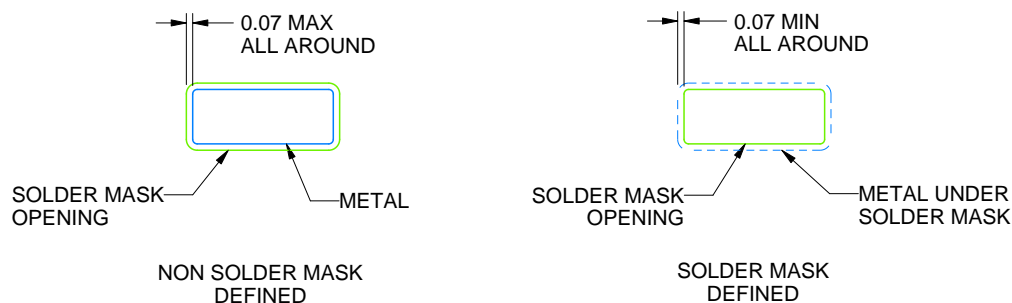
DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

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NOTES: (continued)

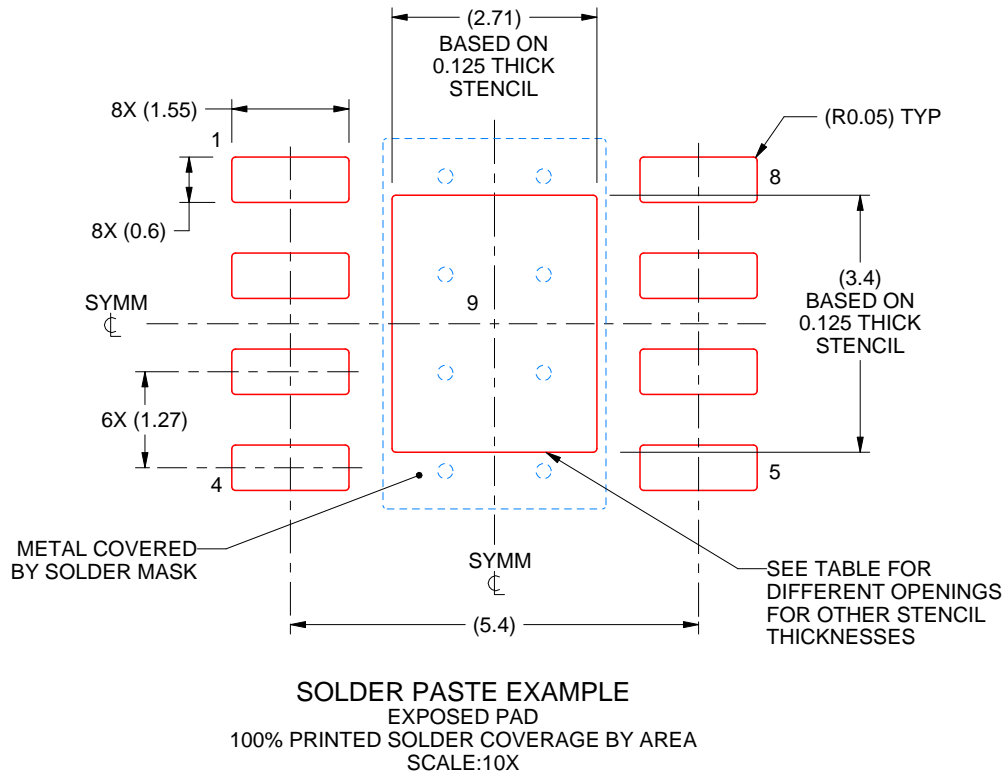
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/B 09/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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