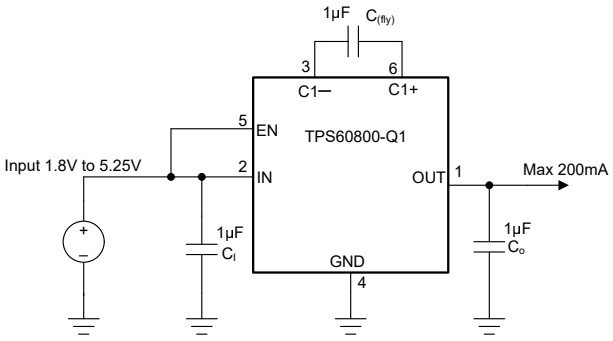
TPS60800-Q1 Unregulated, 200mA, Automotive, Charge Pump Voltage Inverter

1 Features

- Qualified for automotive applications
- AEC-Q100 test guidance with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
- Inverts input supply voltage
- Up to 200mA output current
- Only three small 1µf ceramic capacitors needed
- Input voltage range from 1.8V to 5.25V
- Device quiescent current typical 340µA
- PowerSave-Mode for Improved Efficiency at Low Output Currents
- Efficiency greater than 90% over a wide output current range
- Integrated active Schottky diode for start-up into load
- Available in 6-pin SOT563 package
- Next generation of TPS60400-Q1
- Evaluation module available: TPS60800Q1EVM-068

2 Applications

- Automotive infotainment
- Automotive cluster
- LCD bias
- Operational amplifier supply
- Onboard charger
- Humanoid robot position sensor



Typical Application

3 Description

The TPS60800-Q1 generates an unregulated negative output voltage from an input voltage ranging from 1.8V to 5.25V. The devices are typically supplied by a preregulated supply rail of 5V or 3.3V. As TPS60800-Q1 supports wide input voltage range, two or three NiCd, NiMH, or alkaline battery cells, as well as one Li-Ion cell can also power the device.

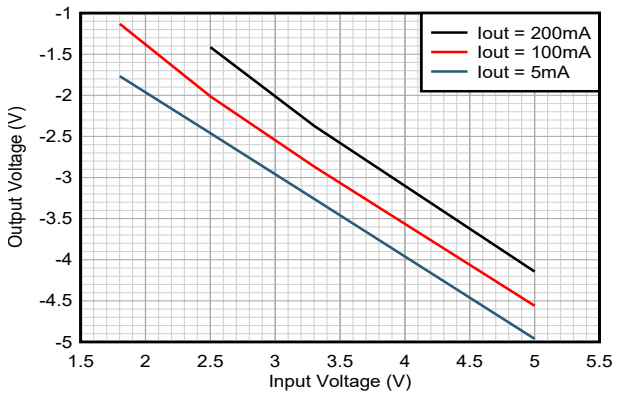
Only three external 1µF capacitors are required to build a complete DC-DC charge pump inverter. Assembled in a 6-pin SOT563 package, the complete converter can be built on a 40mm2 board area. Additional board area and component count reduction is achieved by replacing the Schottky diode that is typically needed for start-up into load by integrated circuitry.

The TPS60800-Q1 can deliver a maximum output current of 200mA with a typical conversion efficiency of greater than 90% over a wide output current range. TPS60800-Q1 comes with a variable switching frequency to reduce operating current in applications with a wide load range and enables the design with low-value capacitors.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
TPS60800-Q1	DRL (SOT563, 6)	1.6mm × 1.6mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Output Voltage vs Input Voltage

Table of Contents

4 Device Comparison Table

PART NUMBER	TYPICAL FLYING CAPACITOR [µF]	FEATURE
TPS60800QDRLRQ1	1	Variable switching frequency 500kHz – 750kHz

5 Pin Configuration and Functions

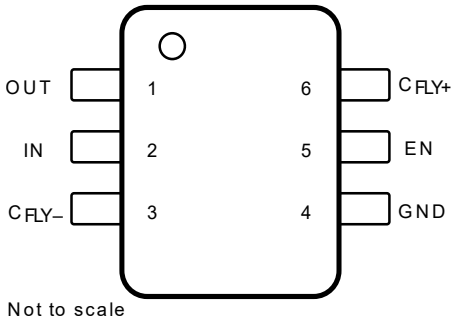


Figure 5-1. DRL Package, SOT563 6 Pins (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
CFLY+	6	—	Positive terminal of the flying capacitor $C_{(fly)}$
EN	5	I	Active high enables input
CFLY–	3	—	Negative terminal of the flying capacitor $C_{(fly)}$
GND	4	—	Ground
IN	2	I	Supply input. Connect to an input supply in the 1.8V to 5.25V range. Bypass IN to GND with a capacitor that has the same value as the flying capacitor.
OUT	1	O	Power output with $V_O = -V_I$. Bypass OUT to GND with the output filter capacitor C_O.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range	IN to GND	–0.3	5.5	V
	OUT to GND	–5.5	0.3	V
	$C_{FLY–}$ to GND	0.3	V_O – 0.3	V
	C_{FLY+} to GND	–0.3	V_I + 0.3	V
Continuous power dissipation		See *Power Dissipation*		
Continuous output current			200	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}	Storage temperature, T_{stg}	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Input voltage range, V_{IN}	1.8		5.25	V
Output current range at OUT, I_O			200	mA
Input capacitor, C_I		$C_{(fly)}$ (1)		µF
Flying capacitor, $C_{(fly)}$		1		µF
Output capacitor, C_O		1	100	µF
Operating junction temperature, T_J	–40		125	°C

(1) Refer to Device Comparison Table for C_{fly} Values.

6.4 Thermal Information

THERMAL METRIC(1)		TPS60800DRL 6 pin SOT563 JEDEC	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	222.3	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	87.8	
$R_{θJB}$	Junction-to-board thermal resistance	109.1	
$ψ_{JT}$	Junction-to-top characterization parameter	4.9	
$ψ_{JB}$	Junction-to-board characterization parameter	108.0	
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

T_J = –40°C to 125°C. Typical values are at T_J = 25°C and V_{IN} = 5V, C_I = $C_{(fly)}$ = C_O = 1uF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage range	At T_J = –40°C to 125°C, R_L = 5kΩ		1.8		5.25	V
I_O	Maximum output current at V_O	V_{IN} < 2.5V			100		mA
I_O	Maximum output current at V_O	V_{IN} ≥ 2.5V			200		mA
V_O	Output voltage				–V_I		V
I_{SD}	Shutdown current	At T_J = –40°C to 85°C ; EN=0V				0.35	µA
I_{SD}	Shutdown current	At T_J = –40°C to 125°C ; EN = 0V				1.5	µA
V_{P-P}	Output voltage ripple	I_O = 5mA	$C_{(fly)}$ = 1µF, C_O = 1µF		10		mV_{P-P}
I_Q	Quiescent current (no-load input current)	EN = High, V_{IN} = 5V			340	1000	µA
f_{OSC}	Internal switching frequency				160 to 500(1)	750	kHz
	Output impedance at 25°C, V_{IN} = 5V	C_I = $C_{(fly)}$ = C_O = 1µF			5		Ω
V_{IH}	Enable pin input voltage high	1.8V ≤ V_{IN} ≤ 5.25		1.2			V
V_{IL}	Enable pin input voltage low	1.8V ≤ V_{IN} ≤ 5.25				0.4	V
I_D	Output discharge current	V_{IN} = 5V	C_I = $C_{(fly)}$ = C_O = 1µF		70		mA

(1) Typical value is from no load to full load current

6.6 Typical Characteristics

Table 6-1. Table of Graphs

			FIGURE
η	Efficiency	vs Output current at V_{IN} = 3.3V, 5V and T_A = 25°C TPS60800-Q1	Figure 6-1
I_I	Input current	vs Output current at V_{IN} = 3.3V, 5V and T_A = 25°C TPS60800-Q1	Figure 6-2
I_S	Supply current	vs Input voltage at T_A = -40°C, 25°C, 85°C, 125°C and I_O = 0mA TPS60800-Q1	Figure 6-3
	Output resistance	vs Input voltage at T_A = -40°C, 25°C, 85°C, 125°C and I_O = 30mA TPS60800-Q1, C_I = $C_{(fly)}$ = C_O = 1µF	Figure 6-4
V_O	Output voltage	vs Output current at T_A = 25°C and V_{IN}=1.8V, 2.5V, 3.3V, 5V TPS60800-Q1, C_I = $C_{(fly)}$ = C_O = 1µF	Figure 6-5
f_{OSC}	Switching frequency	vs Temperature (T_A) at V_{IN} = 1.8V, 2.5V, 3.3V, 5V and I_O = 100mA TPS60800-Q1	Figure 6-6
f_{OSC}	Switching frequency	vs Output current at V_{IN} = 1.8V, 2.5V, 3.3V, 5.0V and T_A = 25°C TPS60800-Q1	Figure 6-7
	Output Ripple and Noise	V_{IN} = 5V, I_O = 30mA, C_I = $C_{(fly)}$ = C_O = 1µF TPS60800-Q1	Figure 8-2

6.6 Typical Characteristics (continued)

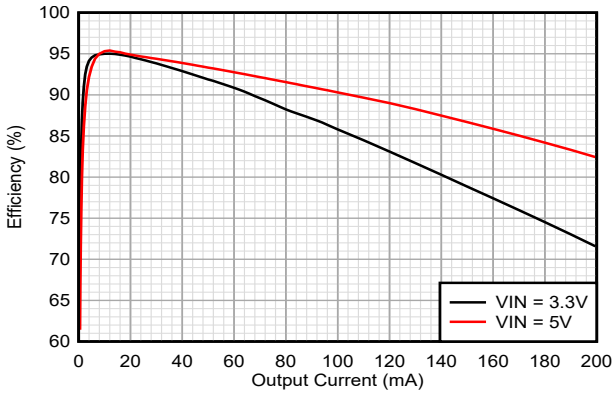


Figure 6-1. Efficiency vs Output Current

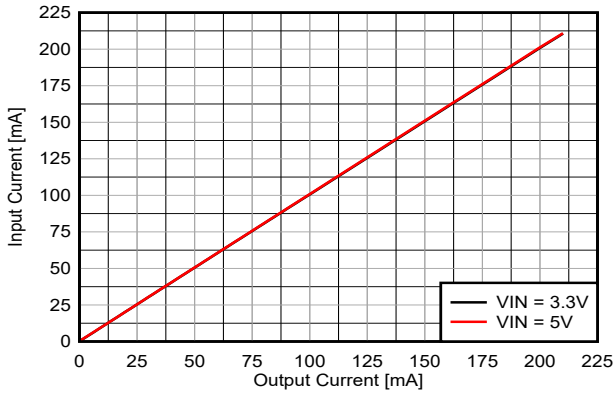


Figure 6-2. Input Current vs Output Current

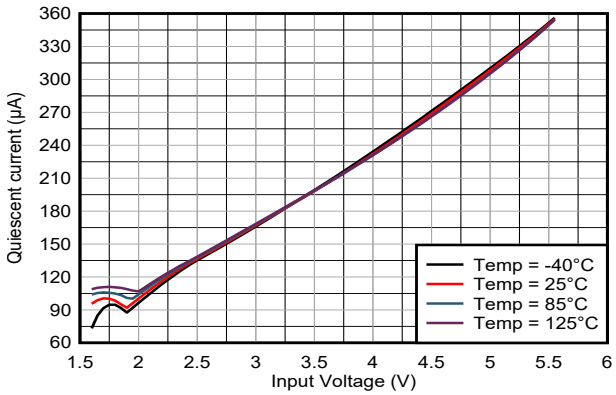


Figure 6-3. Supply Current vs Input Voltage

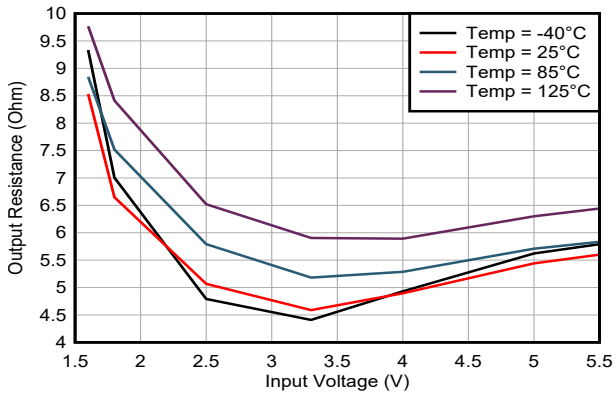


Figure 6-4. Output Resistance vs Input Voltage

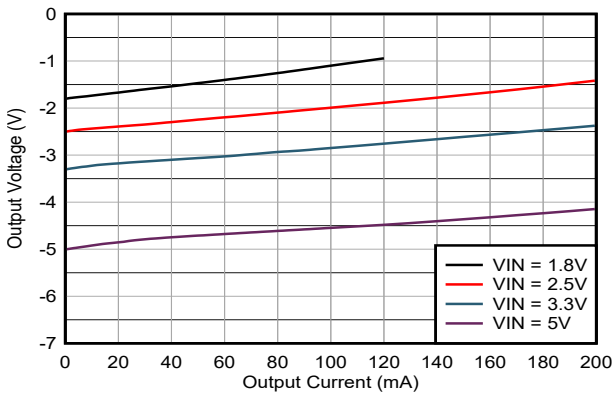


Figure 6-5. Output Voltage vs Output Current

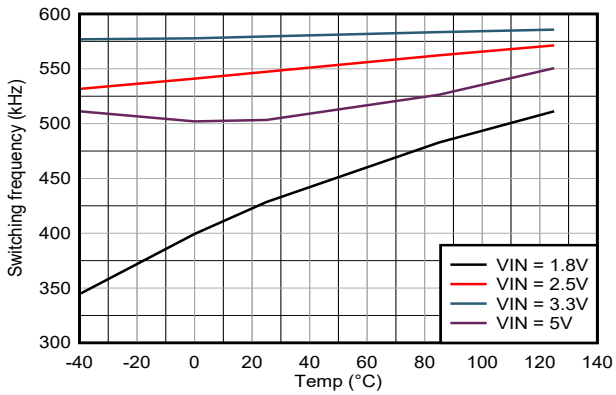


Figure 6-6. Switching Frequency vs Free-Air Temperature

6.6 Typical Characteristics (continued)

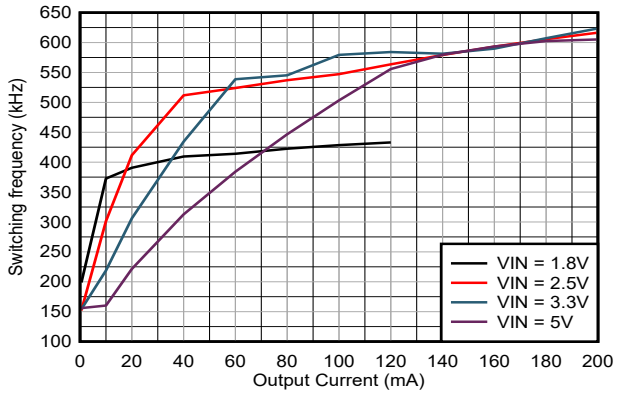


Figure 6-7. Switching Frequency vs Output Current

7 Detailed Description

7.1 Overview

The TPS60800-Q1 charge pump inverts the voltage applied to the input. For the highest performance, use low equivalent series resistance (ESR) capacitors (for example, ceramic). During the first half-cycle, switches S2 and S4 open, switches S1 and S3 close, and capacitor ($C_{(fly)}$) charges to the voltage at V_I. During the second half-cycle, S1 and S3 open, S2 and S4 close. This action connects the positive terminal of $C_{(fly)}$ to GND and the negative to V_O. By connecting $C_{(fly)}$ in parallel, C_O is charged negative. The actual voltage at the output is more positive than $–V_I$, because switches S1-S4 have resistance and the load drains charge from C_O.

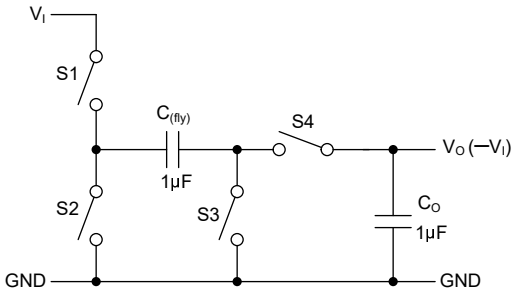
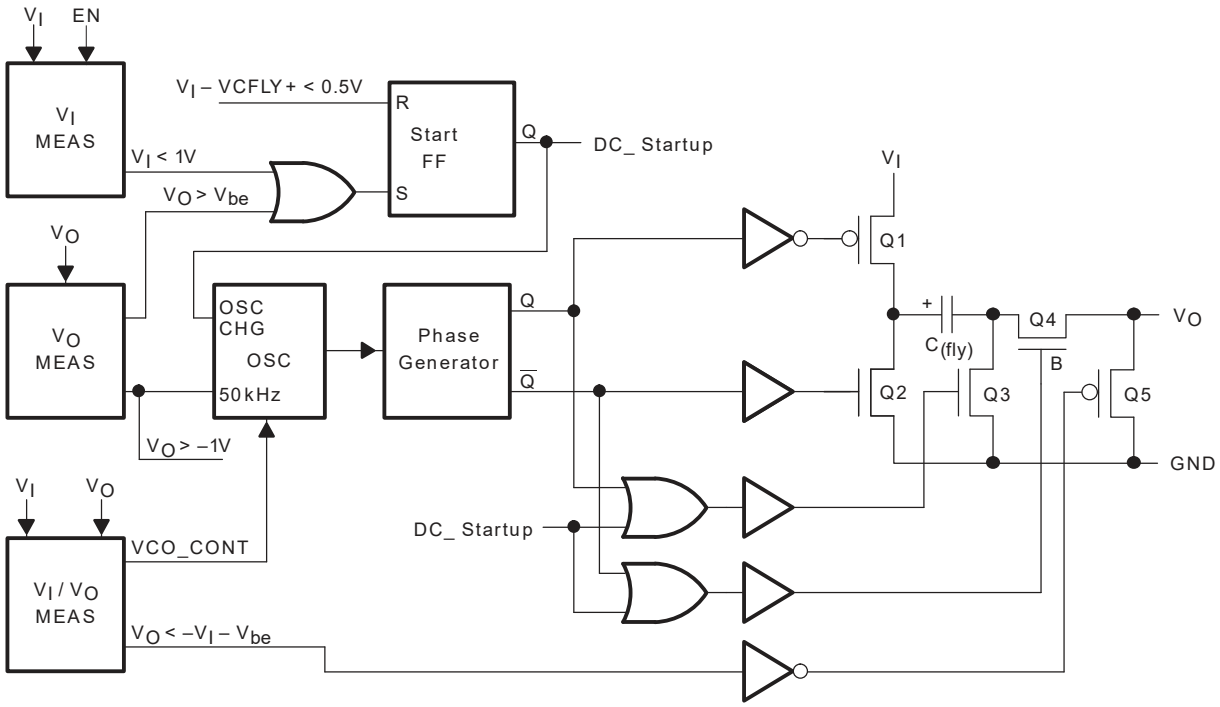


Figure 7-1. Operating Principle

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Charge-Pump Output Resistance

The TPS60800-Q1 is not a voltage regulator. The charge pump output source resistance is approximately 5Ω at room temperature (with V_I = 5V), and V_O approaches –5V when lightly loaded. V_O droops toward GND as load current increases as given by Equation 1.

$$V_O = -(V_I - R_O \times I_O) \quad (1)$$

$$R_O \approx \frac{1}{(f_{OSC} \times C_{fly})} + \left(4 \times \left(2 \times R_{SWITCH} + ESR_{C(FLY)}\right)\right) + ESR_{C(O)} \quad (2)$$

where:

R_O= Output resistance of the converter

R_{SWITCH} = Resistance of a single MOSFET switch inside the converter

f_{OSC} = Oscillator frequency

7.3.2 Efficiency Considerations

The power efficiency of a switched-capacitor voltage converter is affected by three factors: the internal losses in the converter IC, the resistive losses of the capacitors, and the conversion losses during charge transfer between the capacitors. The internal losses are associated with the internal functions of the IC, such as driving the switches, oscillator, and so forth. These losses are affected by operating conditions such as input voltage, temperature, and frequency. The next two losses are associated with the output resistance of the voltage converter circuit. Switch losses occur because of the on-resistance of the MOSFET switches in the IC. Charge-pump capacitor losses occur because of the ESR. The relationship between these losses and the output resistance is given by Equation 3.

$$P_{CAPACITOR\ LOSSES} + P_{CONVERSION\ LOSSES} = I_O^2 \times R_O \quad (3)$$

The first term is the effective resistance from an ideal switched-capacitor circuit. Conversion losses occur during the charge transfer between $C_{(fly)}$ and C_O when there is a voltage difference between them. The power loss is given by Equation 4.

$$P_{CONV.\ LOSS} = \left[\left(\frac{1}{2} \times C_{fly} \times \left(V_I^2 - V_O^2\right)\right) + \left(\frac{1}{2} \times C_O \times \left(V_{RIPPLE}^2 - 2 \times V_O \times V_{RIPPLE}\right)\right)\right] \times f_{OSC} \quad (4)$$

The efficiency of TPS60800-Q1 is dominated by the quiescent supply current at low output current and by the output impedance at higher current as given by Equation 5.

$$\eta \cong \frac{I_O}{(I_O + I_Q)} \times \left(1 - \frac{I_O \times R_O}{V_O}\right) \quad (5)$$

where, I_Q = quiescent current.

7.4 Device Functional Modes

7.4.1 Active-Schottky Diode

For a short period of time, when the input voltage is applied, but the inverter is not yet working, the output capacitor is charged positive by the load. To prevent the output being pulled above GND, a Schottky diode must be added in parallel to the output. The function of this diode is integrated into the TPS60800-Q1 devices, which gives a defined start-up performance and saves board space.

A current sink and a diode in series can approximate the behavior of a typical, modern operational amplifier. Figure 7-2 shows the current into this typical load at a given voltage. The TPS60800-Q1 devices are optimized to start into these loads.

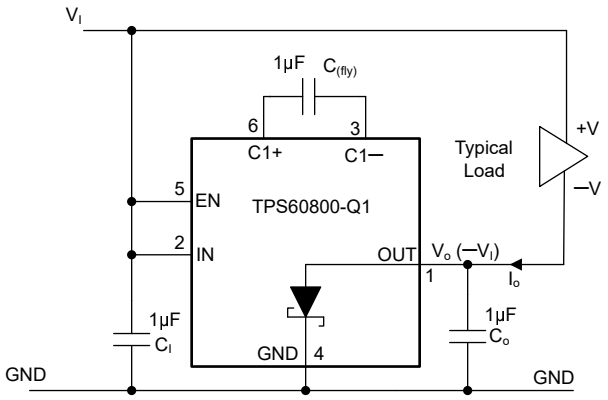


Figure 7-2. Typical Load

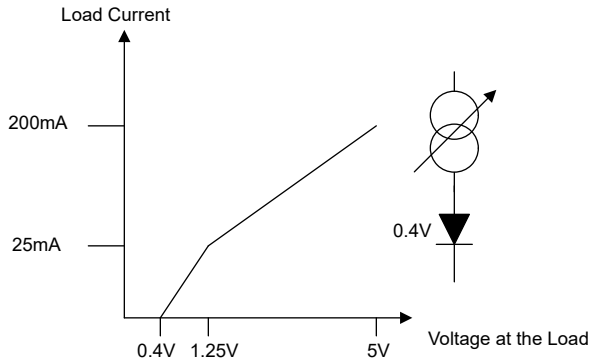


Figure 7-3. Maximum Start-Up Current

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS60800-Q1 generates an unregulated negative output voltage from an input voltage ranging from 1.8V to 5.25V.

8.2 Typical Application

The most common application for TPS60800-Q1 is a charge-pump voltage inverter (see Figure 8-1). This application requires only two external components; capacitors $C_{(fly)}$ and C_O, plus a bypass capacitor (C_I), if necessary. Refer to the *Capacitor Selection* section for suggested capacitor types.

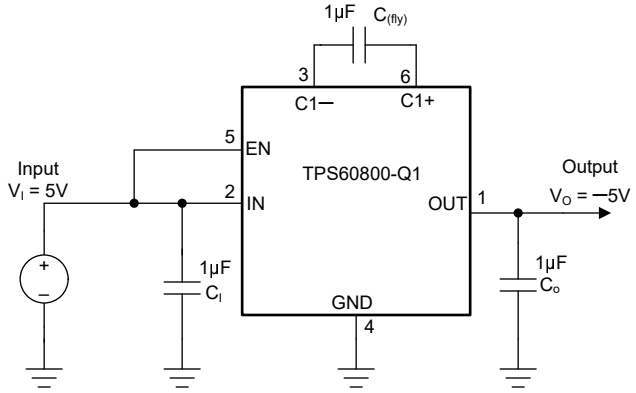


Figure 8-1. Typical Operating Circuit

8.2.1 Design Requirements

The TPS60800-Q1 is used as an inverting DC-DC converter and can generate an unregulated negative output voltage from an input voltage ranging from 1.8V to 5.25V. Additionally, the device has up to 200mA of output current capability.

8.2.2 Detailed Design Procedure

For the maximum output current and best performance, TI recommends three ceramic capacitors of 1µF (TPS60800-Q1). For lower currents or higher allowed output voltage ripple, other capacitors can also be used. TI recommends that the output capacitors has a minimum value of 1µF. With flying capacitors lower than 1µF, the maximum output power decreases.

8.2.2.1 Capacitor Selection

To maintain the lowest output resistance, use capacitors with low ESR (see Table 8-1). The charge-pump output resistance is a function of $C_{(fly)}$ and C_O ESR. Therefore, minimizing the ESR of the charge-pump capacitors minimizes the total output resistance. The capacitor values are closely linked to the required output current and the output noise and ripple requirements. Only using 1µF capacitors of the same type is possible. Ceramic capacitors provide the lowest output voltage ripple because ceramic capacitors typically have the lowest ESR-rating.

8.2.2.2 Input Capacitor (C_I)

Bypass the incoming supply to reduce the ac impedance and the impact of the TPS60800-Q1 switching noise. The recommended bypassing depends on the circuit configuration and where the load is connected. When the inverter is loaded from OUT to GND, current from the supply switches between 2 × I_O and zero. Therefore, use a large bypass capacitor (for example, equal to the value of $C_{(fly)}$) if the supply has high ac impedance. When the inverter is loaded from IN to OUT, the circuit draws 2 × I_O constantly, except for short switching spikes. A 0.1µF bypass capacitor is sufficient.

8.2.2.3 Flying Capacitor ($C_{(fly)}$)

Increasing the flying capacitor size reduces the output resistance. Small values increases the output resistance. Above a certain point, increasing $C_{(fly)}$ capacitance has a negligible effect, because the output resistance becomes dominated by the internal switch resistance and capacitor ESR.

8.2.2.4 Output Capacitor (C_O)

Increasing the output capacitor size reduces the output ripple voltage. Decreasing the ESR reduces both output resistance and ripple. Smaller capacitance values can be used with light loads if higher output ripple can be tolerated. Use Equation 6 to calculate the peak-to-peak ripple.

$$V_{O(ripple)} = \frac{I_O}{f_{OSC} \times C_O} + 2 \times I_O \times ESR_{CO} \quad (6)$$

Table 8-1. Recommended Capacitor Values

DEVICE	V_I [V]	I_O [mA]	C_I [µF]	$C_{(fly)}$ [µF]	C_O [µF]
TPS60800-Q1	1.8V to 5.25V	100	1	1	1
TPS60800-Q1	2.5V to 5.25V	200	1	1	1

Table 8-2. Recommended Capacitors

MANUFACTURER	PART NUMBER	SIZE	CAPACITANCE	TYPE
Murata	GCM188R71E105KA64D	0603	1µF	Ceramic
TDK	CGA3E1X7R1E105K080AE	0603	1µF	Ceramic

8.2.2.5 Power Dissipation

As given in *Thermal Information*, the thermal resistance $R_{\Theta JB}$ of TPS60800-Q1 is 109.1°C/W. $R_{\Theta JB}$ refers to the thermal resistance between the device junction temperature and the surrounding board temperature. The following equations calculate the highest allowable board temperature under full power conditions, subject to the device junction temperature not exceeding 125°C.

The thermal resistance $R_{\Theta JB}$ can be calculated using Equation 7.

$$R_{\theta JB} = \frac{T_J - T_B}{P_D} \quad (7)$$

where:

T_J is the junction temperature, T_B is the board temperature and P_D is the power dissipated by the device.

The maximum power dissipation can be calculated by using the following Equation 8.

$$P_D = V_I \times I_I - V_O \times I_O = V_{I(max)} \times \left(I_O + I_{(Supply)}\right) - V_O \times I_O \quad (8)$$

The maximum power dissipation happens with maximum input voltage and maximum output current.

At maximum load the maximum supply current is 1mA (see Equation 9).

$$P_D = 5V \times (200mA + 1mA) - 4.15V \times 200mA = 175mW \quad (9)$$

With this maximum power rating and thermal resistance, $R_{\Theta JB}$, the maximum junction temperature rise above the board temperature can be calculated using Equation 10.

$$\Delta T_J = R_{\theta JB} \times P_D = 109.1℃/W \times 175mW = 19.09℃ \quad (10)$$

This equation means that the power dissipation increases T_J by < 20°C with respect to the board temperature.

The junction temperature of the device must not exceed 125°C.

This limit implies the IC can easily be used up to board temperatures given by Equation 11.

$$T_B = T_{J(max)} - \Delta T_J = 125℃ - 20℃ = 105℃ \quad (11)$$

8.2.3 Application Curve

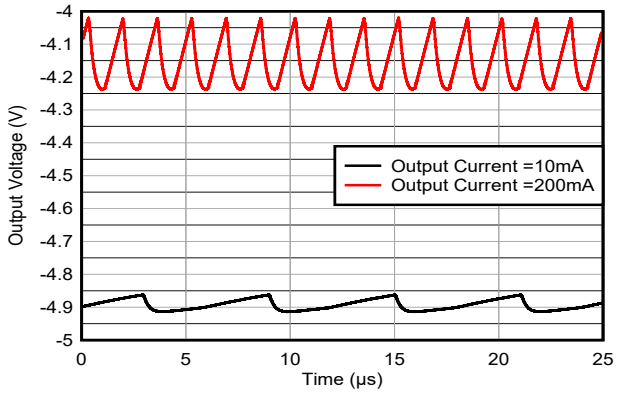


Figure 8-2. Output Voltage vs Time for TPS60800-Q1

8.3 System Examples

8.3.1 RC-Post Filter

To reduce the output voltage ripple, an RC post filter can be used as shown in the following figure.

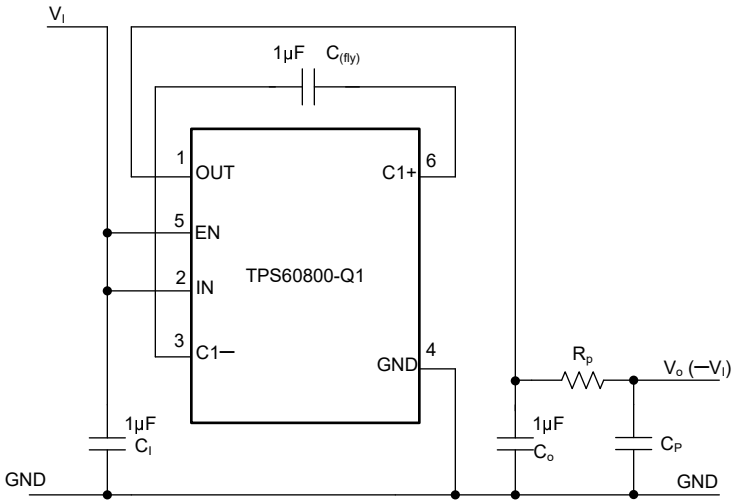


Figure 8-3. TPS60800-Q1 With RC-Post Filter

An output filter can easily be formed with a resistor (R_P) and a capacitor (C_P). Cutoff frequency is given by Equation 12:

$$f_c = \frac{1}{2 \times \pi \times R_P \times C_P} \tag{12}$$

and the ratio V_O/V_{OUT} is determined by Equation 13:

$$\left|\frac{V_O}{V_{OUT}}\right| = \frac{1}{\sqrt{1 + (2 \times \pi \times f \times R_P \times C_P)^2}} \tag{13}$$

$$\text{with } R_P = 50\Omega,\ C_P = 0.1\mu F \text{ and } f = 250kHz: \left|\frac{V_O}{V_{OUT}}\right| = 0.125 \tag{14}$$

The equation refers only to the relation between output and input of the ac ripple voltages of the filter.

8.3.2 Rail Splitter

A switched-capacitor voltage inverter can be configured as a high efficiency rail-splitter. This circuit provides a bipolar power supply that is useful in battery powered systems to supply dual-rail ICs, like operational amplifiers. Moreover, the SOT563 package and associated components require very little board space.

The maximum input voltage between V_I and GND in Figure 8-4 (or between IN and OUT at the device) must not exceed 5.5V.

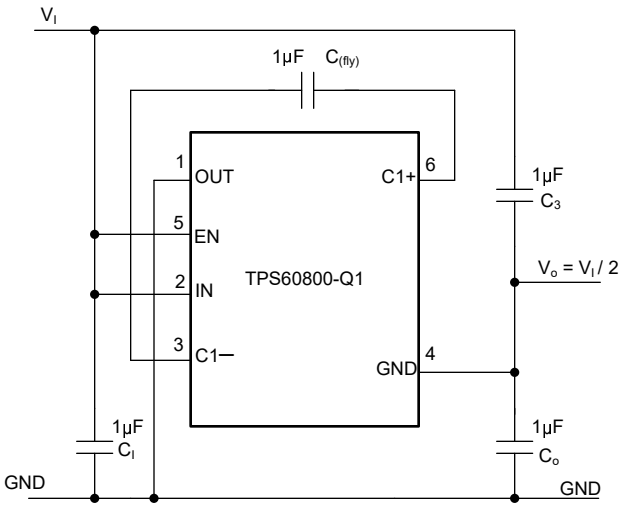


Figure 8-4. TPS60800-Q1 as a High-Efficiency Rail Splitter

After power is applied, the flying capacitor ($C_{(fly)}$) connects alternately across the output capacitors C_3 and C_O. This action equalizes the voltage on those capacitors and draws current from V_I to V_O as required to maintain the output at $1/2V_I$.

8.3.3 Combined Doubler, Inverter

The application allows to generate a voltage rail at a level of –Vi as well as 2 × Vi (V(pos)) as shown in Figure 8-5.

Capacitors C_I, $C_{(fly)}$, and C_O form the inverter, while C1 and C2 form the doubler. C1 and $C_{(fly)}$ are the flying capacitors; C_O and C2 are the output capacitors. Because both the inverter and doubler use part of the charge-pump circuit, loading either output causes both outputs to decline toward GND. Make sure the sum of the currents drawn from the two outputs does not exceed 200mA. The maximum output current at $V_{(pos)}$ must not exceed 100mA. If the negative output is loaded, this current must be further reduced.

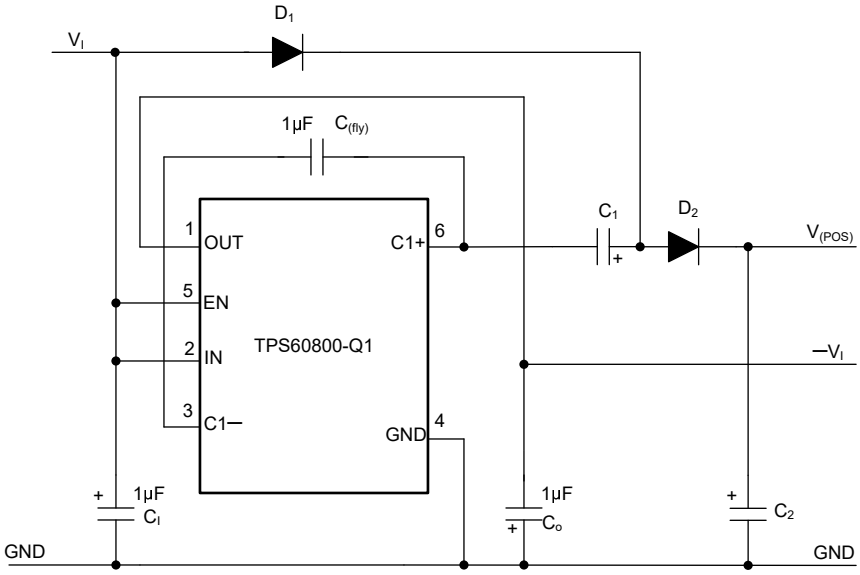


Figure 8-5. TPS60800-Q1 as Doubler, Inverter

8.3.4 Cascading Devices

Two devices can be cascaded to produce an even larger negative voltage (see Figure 8-6). The unloaded output voltage is normally $–2 \times V_I$, but this amount is reduced slightly by the output resistance of the first device multiplied by the quiescent current of the second. When cascading more than two devices, the output resistance rises dramatically.

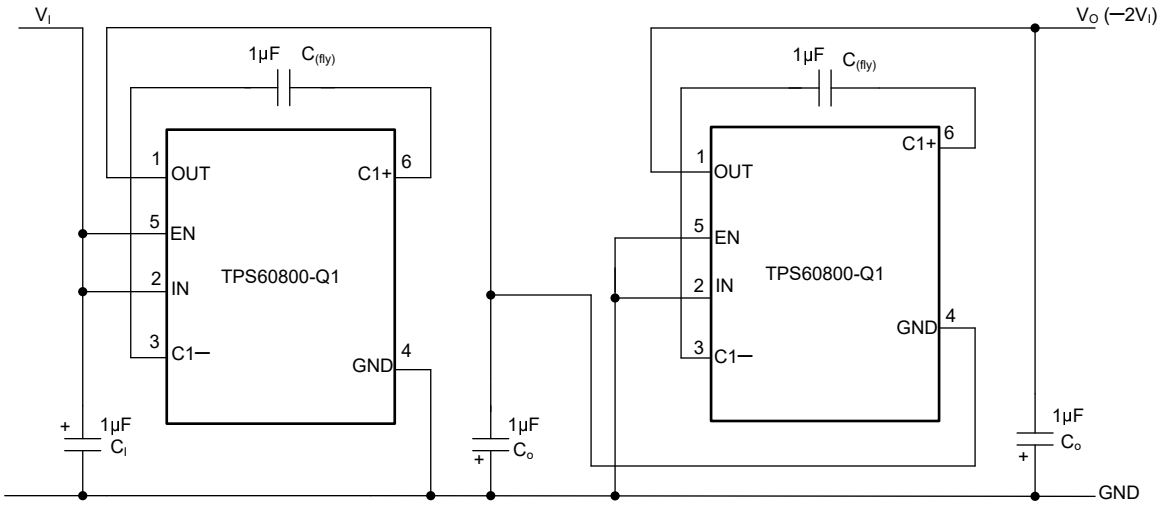


Figure 8-6. Doubling Inverter

8.3.5 Paralleling Devices

The application allows to increase the output current by using two or more in parallel as shown in Figure 8-7.

Paralleling multiple TPS60800-Q1 reduces the output resistance. Each device requires a flying capacitor ($C_{(fly)}$), but the output capacitor (C_O) serves all devices. Increase the value of C_O by a factor of n, where n is the number of parallel devices. Equation 2 describes the calculation of output resistance.

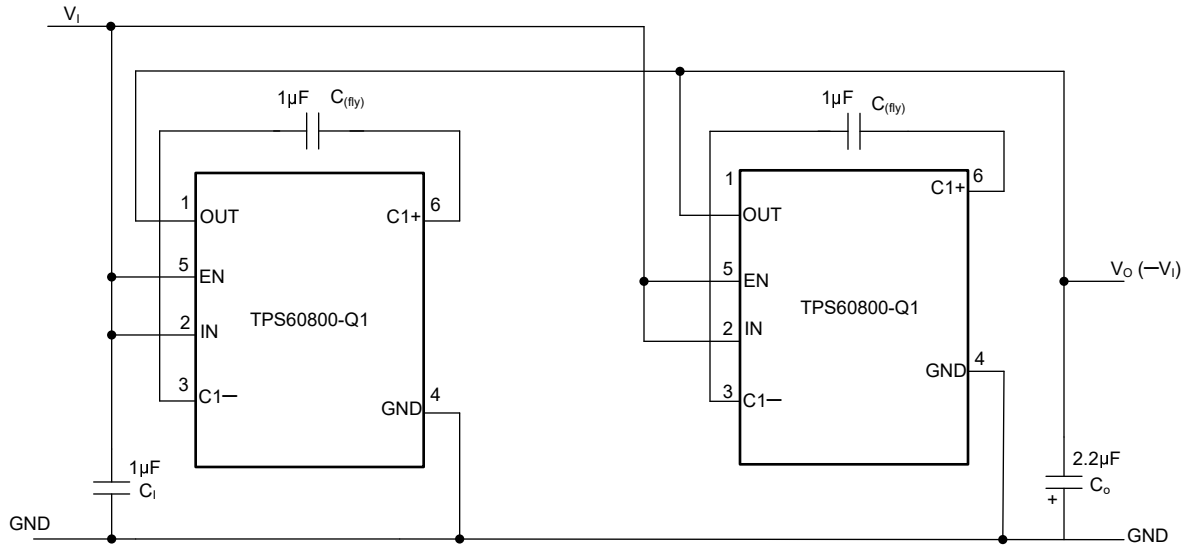


Figure 8-7. Paralleling Devices

8.3.6 Step-Down Charge Pump

The application generates an output voltage of 1/2 of the input voltage as shown in Figure 8-9.

By exchanging GND with OUT (connecting the GND pin with OUT and the OUT pin with GND), a step-down charge pump can easily be formed. In the first cycle S1 and S3 are closed, and $C_{(fly)}$ with C_O in series are charged. Assuming the same capacitance, the voltage across $C_{(fly)}$ and C_O is split equally between the capacitors. In the second cycle, S2 and S4 close and both capacitors with $V_I/2$ across are connected in parallel.

The maximum input voltage between V_I and GND in the schematic (or between IN and OUT at the device) must not exceed 5.5V.

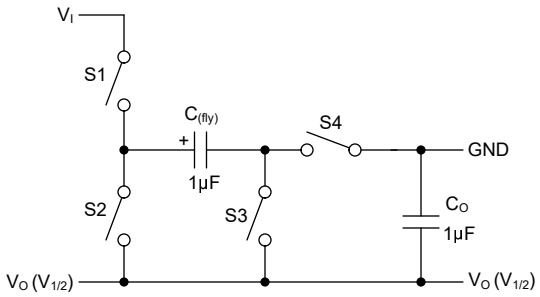


Figure 8-8. Step-Down Principle

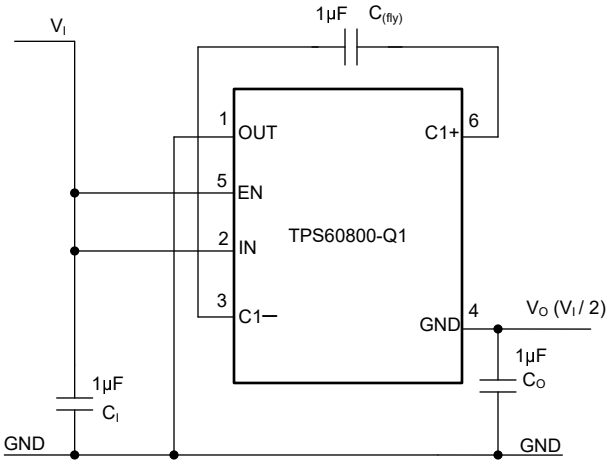


Figure 8-9. Step-Down Charge Pump Connection

8.4 Power Supply Recommendations

The TPS60800-Q1 has no special requirements for the power supply. The power supply output must rated according to the supply voltage, output voltage, and output current of the TPS60800-Q1.

8.5 Layout

8.5.1 Layout Guidelines

Solder all capacitors as close as possible to the IC. A PCB layout proposal for a dual-layer board is shown in Figure 8-10. Care has been taken to connect all capacitors as close as possible to the circuit to achieve optimized output voltage ripple performance. Please refer to the evaluation module user's guide in the product folder for more details on the layout.

8.5.2 Layout Example

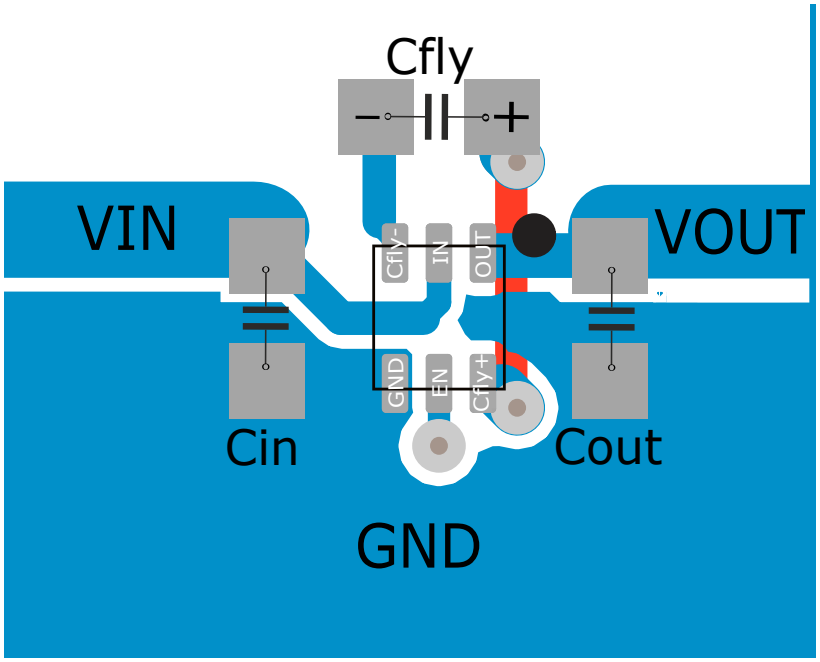


Figure 8-10. Recommended PCB Layout for TPS60800-Q1 (Top Layer)

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
May 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS60800QDRLRQ1	Active	Production	SOT-5X3 (DRL) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LAMY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

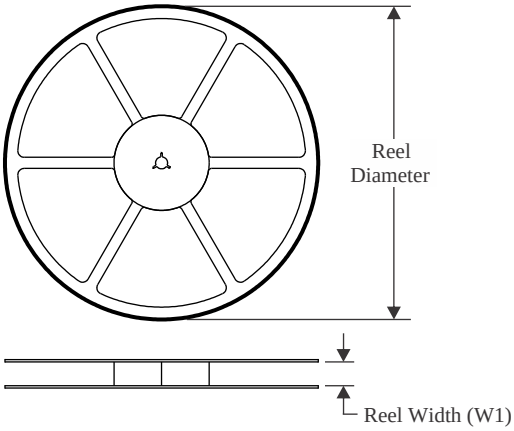
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

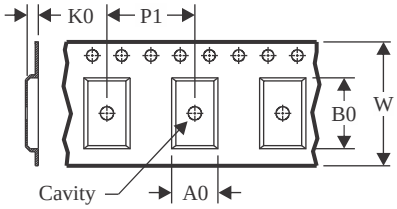
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

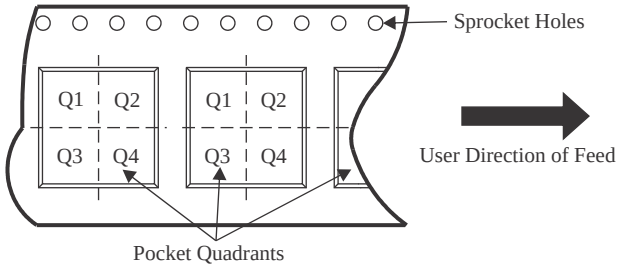


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

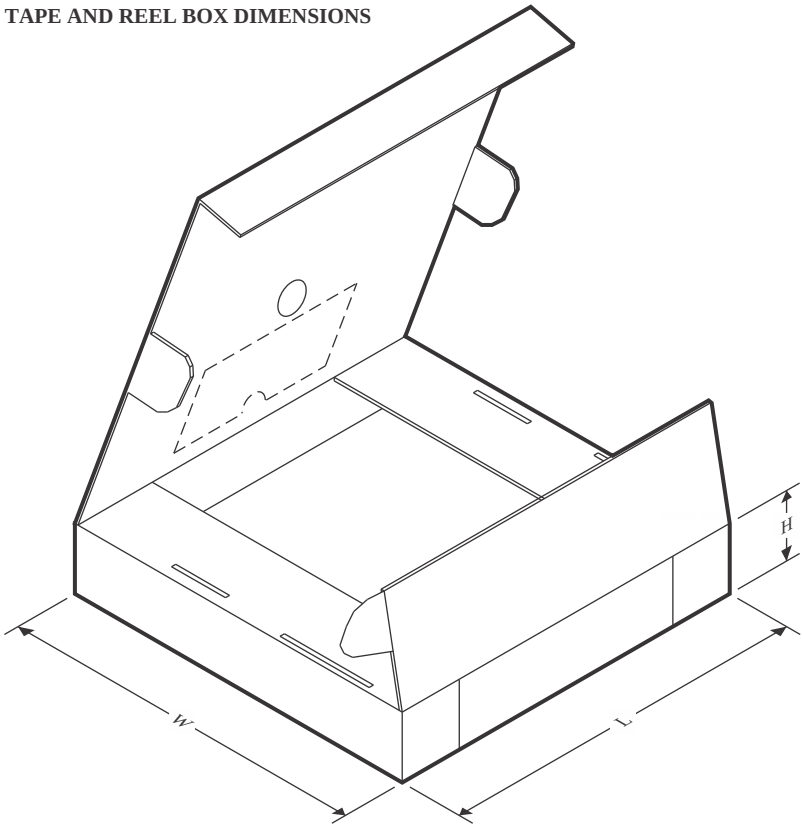
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60800QDRLRQ1	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

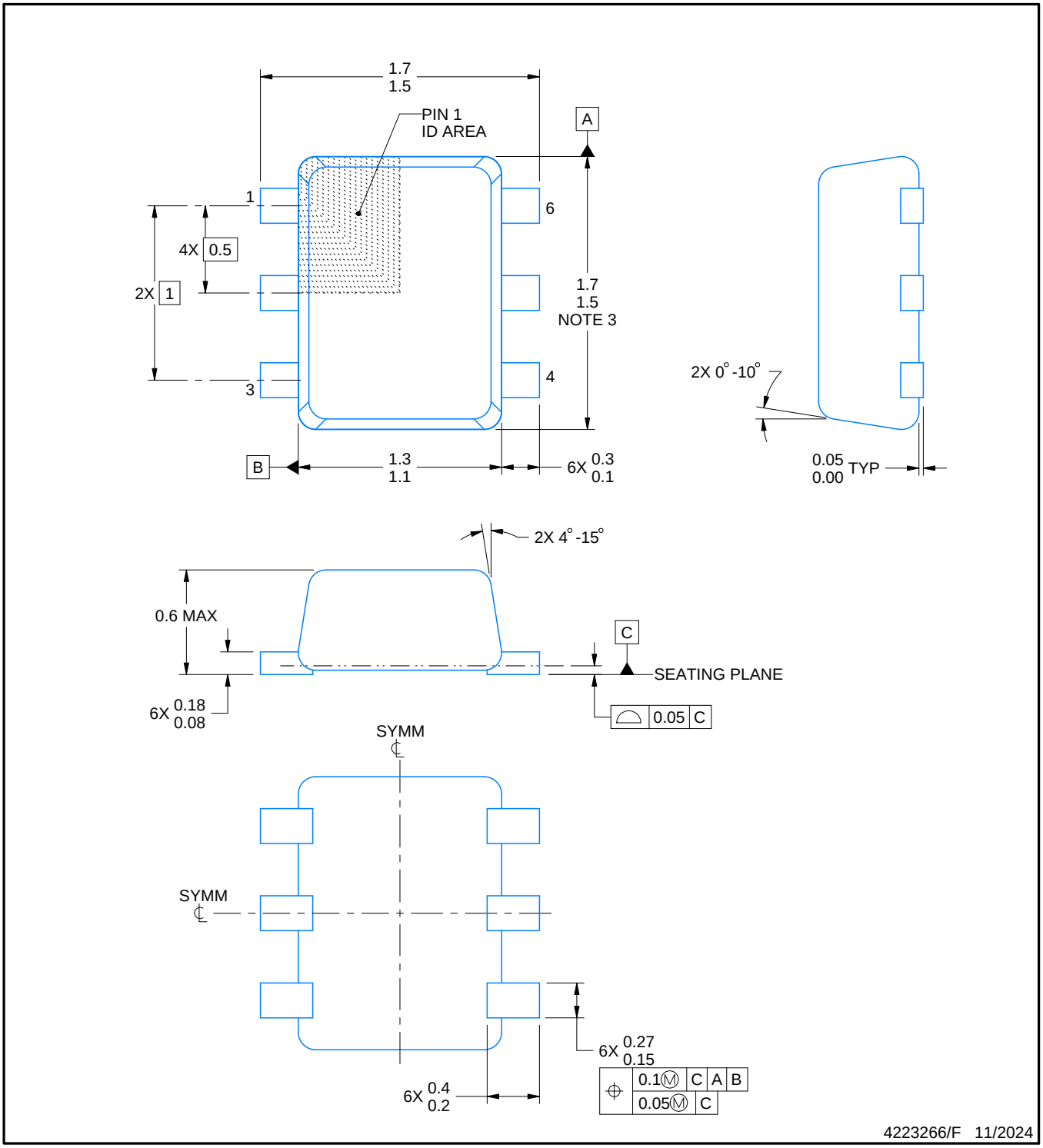
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60800QDRLRQ1	SOT-5X3	DRL	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

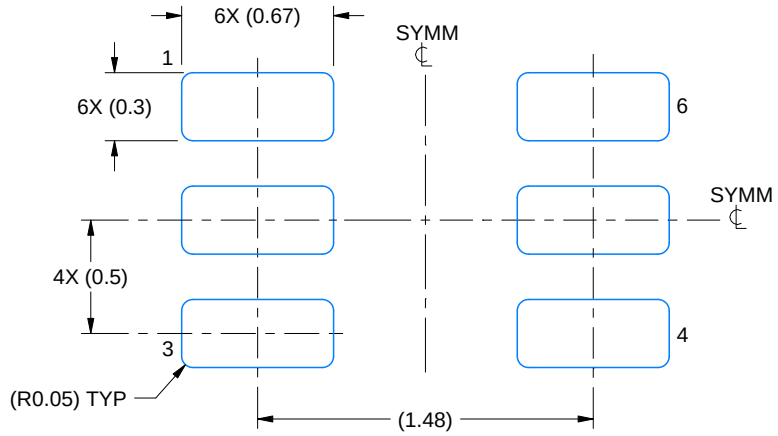
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

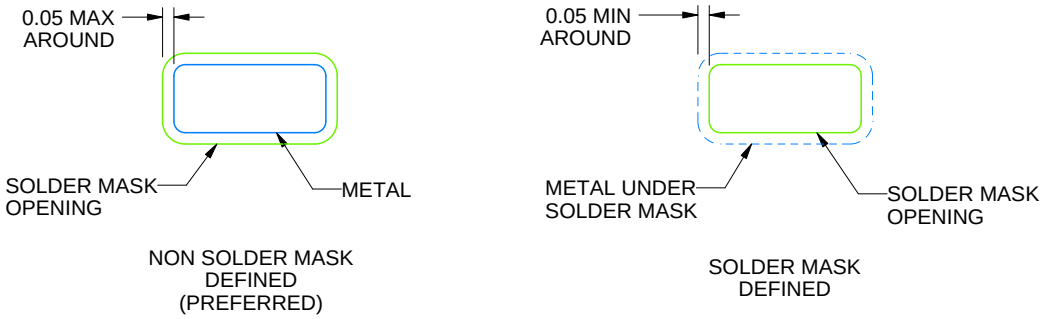
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

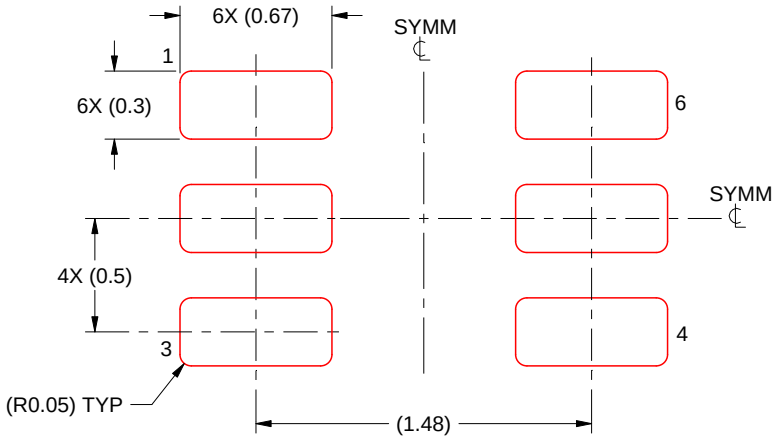
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025