TPS62590-Q1 Automotive 2.25-MHz 1-A Step-Down Converter In 2-mm × 2-mm SON Package

1 Features

- Qualified for Automotive Applications
- Output Current up to 1000 mA
- Input Voltage Range from 2.5 V to 6 V
- High Efficiency Step Down Converter
- Output Voltage Accuracy in PWM mode ±2.5%
- Typical 15-µA Quiescent Current
- 2.25 MHz Fixed Frequency Operation
- Power Save Mode at Light Load Currents
- 100% Duty Cycle for Lowest Dropout

2 Applications

- Automotive Infotainment and Cluster
  - Head Unit
  - Navigation
  - Display
- Advanced Driver Assistance System (ADAS)
  - Front Cameras
  - Blind Spot Monitoring
  - Lane Departure Warning
  - Park Assist

3 Description

The TPS62590-Q1 device is a high-efficiency synchronous step-down converter, optimized for space constrained applications and very low quiescent current requirements. It provides up to 1000-mA output current from preregulated low voltage rails and consumes 15 uA (typical) in power-save mode.

With an input voltage range of 2.5 V to 6 V and an output voltage accuracy of 2.5%, the device is targeted to power a large variety of automotive applications.

The TPS62590-Q1 family operates at a 2.25-MHz fixed switching frequency and enters a power-save mode at light load currents to maintain a high efficiency over the entire load current range.

The power-save mode is optimized for low output-voltage ripple. For low-noise applications, the device can be forced into fixed-frequency PWM mode by pulling the MODE pin high. In the shutdown mode, the current consumption is reduced to less than 1 µA. The TPS62590-Q1 allows the use of small inductors and capacitors to achieve a small solution size.

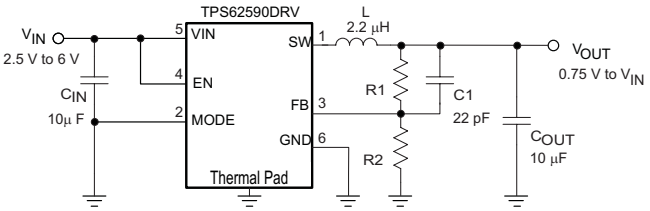
The TPS62590-Q1 is available in a 2-mm × 2-mm 6-pin SON package with a thermal pad for improved thermal performance.

Device Information[1]

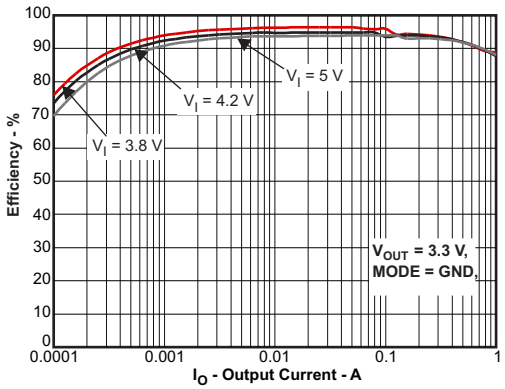
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62590-Q1	SON (6)	2.00 mm × 2.00

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Efficiency vs Load Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2012) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added additional features ... 1
- Added 2.25 MHz in the title ... 1
- Deleted " Available in a 2-mm × 2-mm × 0,8-mm SON Package" and "For Improved Features Set, See TPS62290" from the *Features* section ... 1
- Changed first two paragraphs of the *Description* section ... 1
- Added Effective inductance, Effective output capacitance, and Feed-forward capacitance parameters in *Recommended Operating Conditions*. ... 4
- Updated values in *Thermal Information* ... 4
- Added *External Feed-Forward Capacitor* section ... 15
- Updated paragraph in *Output Filter Design (Inductor and Output Capacitor)* section ... 15

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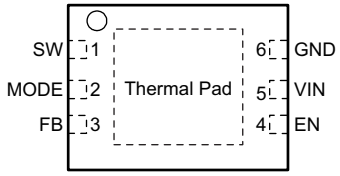
5 Pin Configuration and Functions

DRV Package
6-Pin SON With Exposed Thermal pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SW	O	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
2	MODE	I	MODE pin = high forces the device to operate in fixed-frequency PWM mode. Mode pin = low enables the power-save mode with automatic transition from PFM mode to fixed-frequency PWM mode.
3	FB	I	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output-voltage option, connect this pin directly to the output capacitor.
4	EN	I	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
5	VIN	PWR	VIN power supply pin
6	GND	GND	GND supply pin
—	Thermal pad	—	Must be soldered to achieve appropriate power dissipation. Should be connected to GND.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage(2)	–0.3	7	V
	Voltage range at EN, MODE	–0.3	V_{IN} +0.3, ≤ 7	V
	Voltage on SW	–0.3	7	V
	Peak output current	Internally limited		A
T_J	Maximum operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	2.5		6	V
	Output voltage range for adjustable voltage	0.75		V_{IN}	V
T_A	Operating ambient temperature	–40		105	°C
T_J	Operating junction temperature	–40		125	°C
L_{OUT}	Effective inductance	1.5		4.7	µH
C_{OUT}	Effective output-capacitance	4.7		22	µF
Cf	Feed-forward capacitance	22		33	pF
C_{IN}	Effective input-capacitance	10			µF

6.4 Thermal Information

THERMAL METRIC(1)(2)		TPS62590-Q1 DRV (SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Simulated values based on four layer FR4 board (2-oz, 1-oz, 1-oz, 2-oz copper) with size: 76 mm × 114 mm × 1.6 mm

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6.5 Electrical Characteristics

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 10 µF 0603, C_{OUT} = 10 µF 0603, L = 2.2 µH; see *Parameter Measurement Information*.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_I	Input voltage range		2.5		6	V
I_O	Output current(1)	V_{IN} 2.7 V to 6 V			1000	mA
		V_{IN} 2.5 V to 2.7 V			600	
I_Q	Operating quiescent current	I_O = 0 mA, PFM mode enabled (MODE = GND) device not switching, See (2)		15		µA
		I_O = 0 mA, switching with no load (MODE = V_{IN}) PWM mode, V_O = 1.8 V, V_{IN} = 3 V		3.8		mA
I_{SD}	Shutdown current	EN = GND		0.5		µA
UVLO	Undervoltage lockout threshold	Falling		1.85		V
		Rising		1.95		
ENABLE, MODE						
V_{IH}	High-level input voltage, EN, MODE	2.5 V ≤ V_{IN} ≤ 6 V	1		V_{IN}	V
V_{IL}	Low-level input voltage, EN, MODE	2.5 V ≤ V_{IN} ≤ 6 V	0		0.4	V
I_I	Input bias current, EN, MODE	EN, MODE = GND or V_{IN}		0.01	1	µA
POWER SWITCH						
$r_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V, T_A = 25°C		250		mΩ
	Low-side MOSFET on-resistance			190		
I_{LIMF}	Forward current limit MOSFET high-side and low-side	V_{IN} = V_{GS} = 3.6 V, T_A = 25°C	1.19	1.4	1.78	A
T_{SD}	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		
OSCILLATOR						
f_{SW}	Oscillator frequency	2.5 V ≤ V_{IN} ≤ 6 V		2.25		MHz
OUTPUT						
V_O	Adjustable output voltage range		0.75		V_I	V
V_{ref}	Reference voltage			600		mV
$V_{FB(PWM)}$	Feedback voltage	MODE = V_{IN}, PWM mode, 2.5 V ≤ V_{IN} ≤ 6 V, See (3)	–2.5%	0%	2.5%	
$V_{FB(PFM)}$	Feedback voltage, PFM mode	MODE = GND, device in PFM mode, 1% voltage positioning active, See (2)		1%		
	Load regulation			–1		%/A
$t_{Start\ Up}$	Start-up time	Time from active EN to reach 95% of V_O		500		µs
t_{Ramp}	V_O ramp-up time	Time to ramp from 5% to 95% of V_O		250		µs
I_{lkg}	Leakage current into SW pin	V_I = 3.6 V, V_I = V_O = V_{SW}, EN = GND, See (4)		0.1	1	µA

(1) Not production tested.
(2) In PFM mode, the internal reference voltage is set to typ. 1.01 × V_{ref} . See *Parameter Measurement Information*.
(3) For V_{IN} = V_O + 1 V
(4) In fixed output-voltage versions, the internal resistor divider network is disconnected from the FB pin.

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6.6 Typical Characteristics

Table 1. Table Of Graphs

		FIGURE
Efficiency	vs Output Current V_{OUT} = 1.8 V (Power-Save Mode)	Figure 1
	vs Output Current V_{OUT} = 1.8 V (Forced PWM Mode)	Figure 2
	vs Output Current V_{OUT} = 3.3 V (Power-Save Mode)	Figure 3
	vs Output Current V_{OUT} = 3.3 V (Forced PWM Mode)	Figure 4
Output Voltage	vs Output Current V_{OUT} = 1.8 V (Forced PWM Mode)	Figure 5
	vs Output Current V_{OUT} = 1.8 V (Power-Save Mode)	Figure 6
	vs Output Current V_{OUT} = 3.3 V (Forced PWM Mode)	Figure 7
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	PWM Line Transient	Figure 12
	Typical Performance – PFM Mode	Figure 13
	Typical Performance – PWM Mode	Figure 14
Shutdown Current	into VIN vs. Input Voltage	Figure 15
Quiescent Current	vs Input Voltage	Figure 16
Static Drain-Source On-State Resistance	vs Input Voltage	Figure 17
		Figure 18

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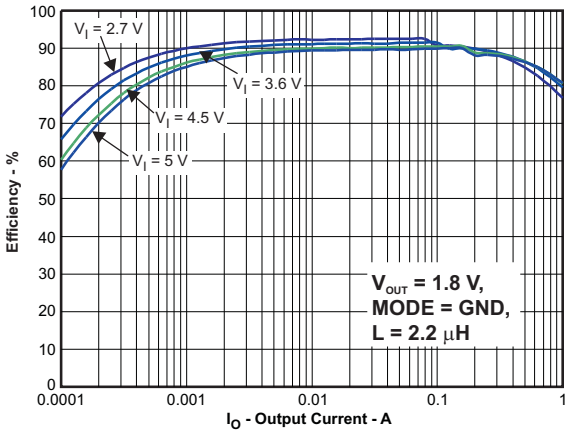

Figure 1. Efficiency vs Output Current for V_{OUT} = 1.8 V (Power-Save Mode)

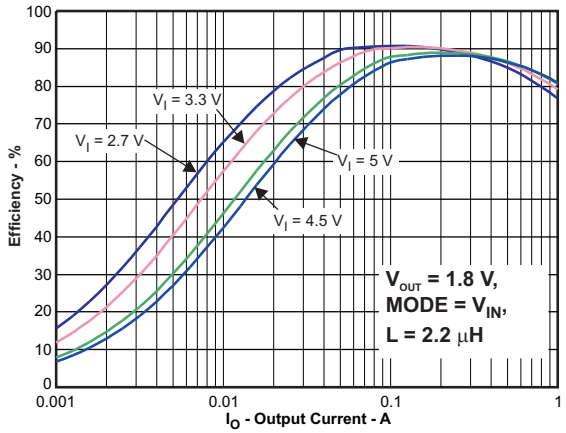

Figure 2. Efficiency vs Output Current for V_{OUT} = 1.8 V (Forced PWM Mode)

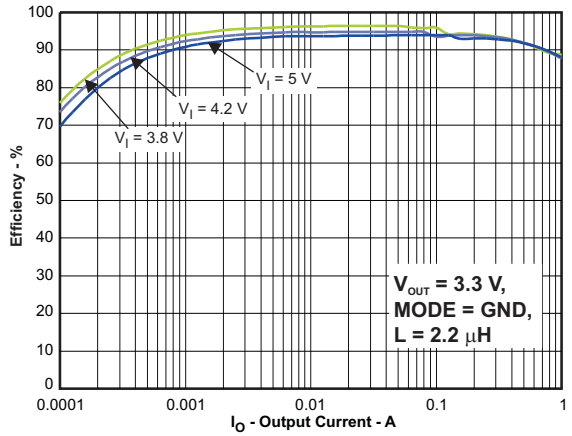

Figure 3. Efficiency vs Output Current for V_{OUT} = 3.3 V (Power-Save Mode)

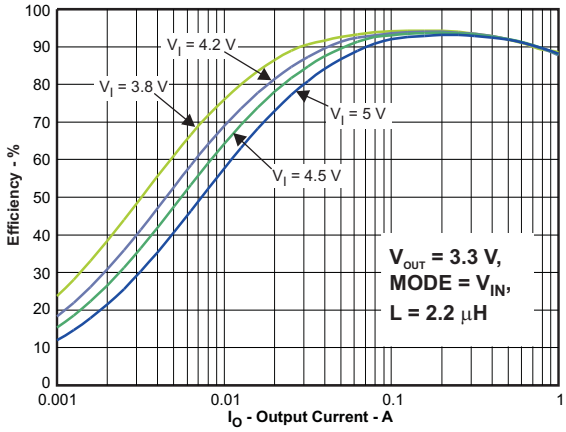

Figure 4. Efficiency vs Output Current for V_{OUT} = 3.3 V (Forced PWM Mode)

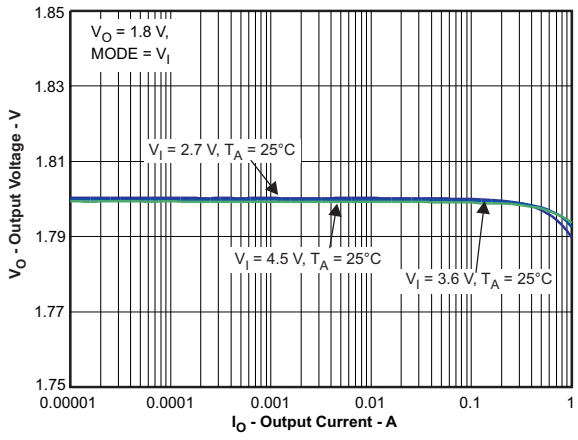

Figure 5. Output Voltage vs Output Current vs Input Voltage for V_{OUT} = 1.8 V (Power Saver Mode)

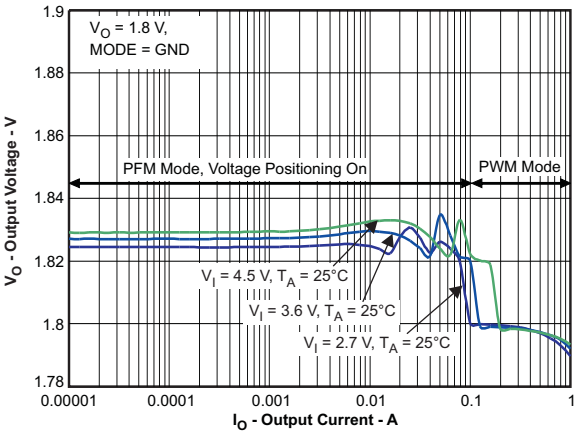

Figure 6. Output Voltage vs Output Current vs Input Voltage for V_{OUT} = 1.8 V (Forced PWM Mode)

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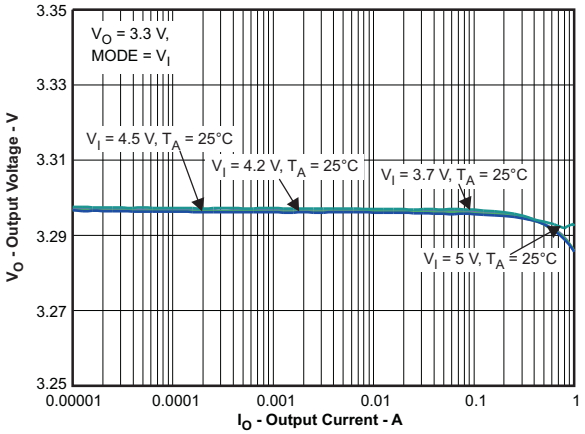

Figure 7. Output Voltage vs Output Current vs Input Voltage for V_{OUT} = 3.3 V (Forced PWM Mode)

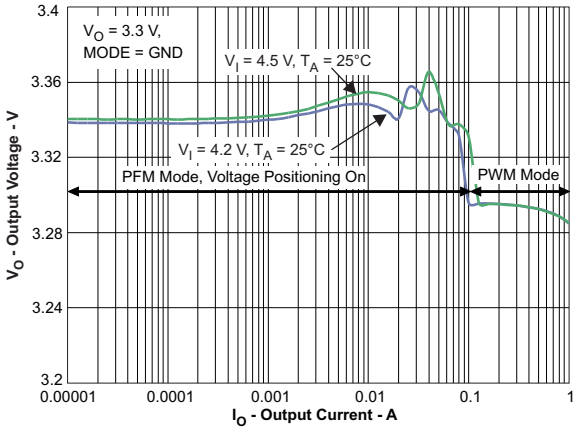

Figure 8. Output Voltage vs Output Current vs Input Voltage for V_{OUT} = 3.3 V (Power Saver Mode)

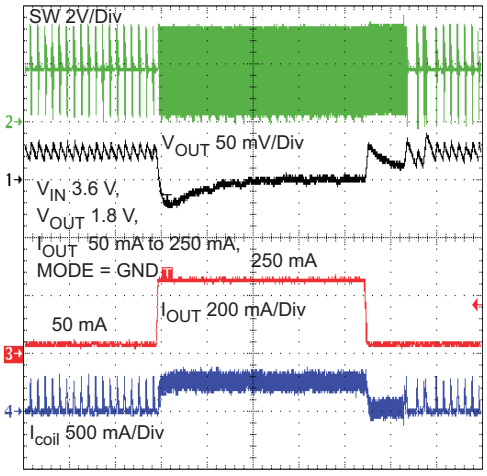

Figure 9. PFM to PWM to PFM Load Transient

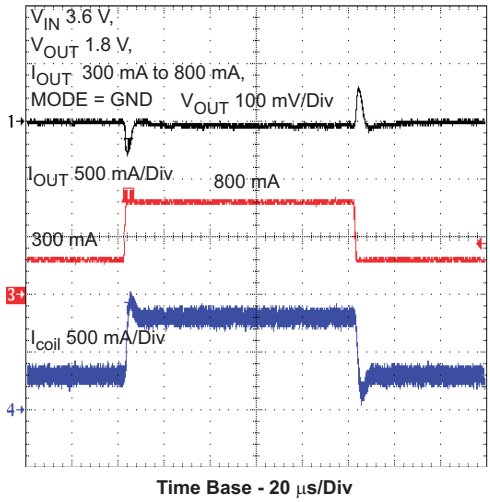

Figure 10. PWM Load Transient

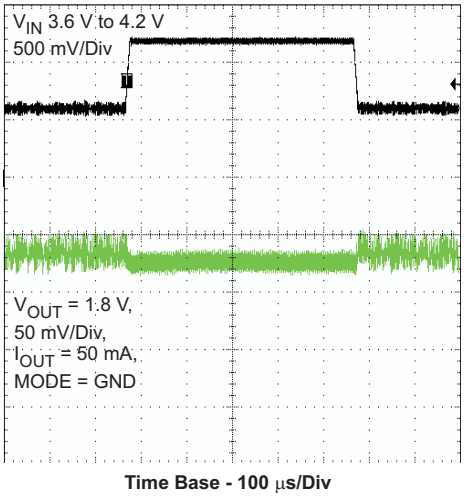

Figure 11. PFM Line Transient

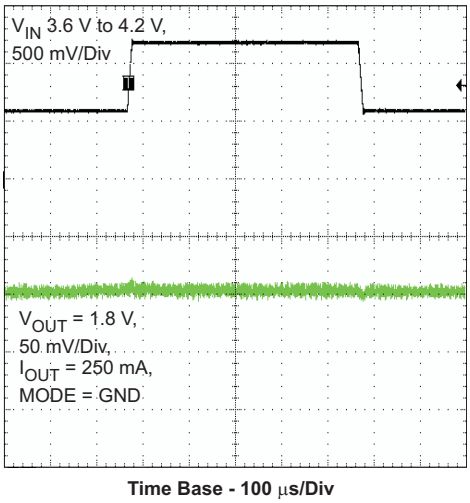

Figure 12. PWM Line Transient

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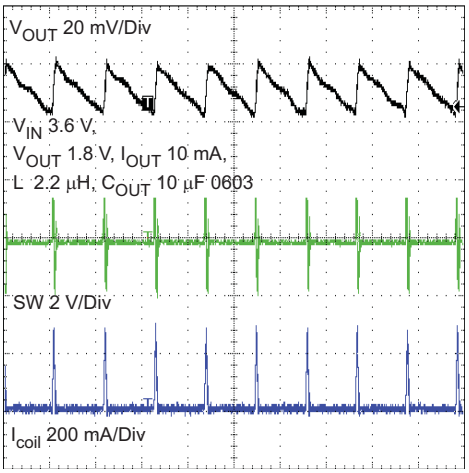


Figure 13. Typical Performance – PFM Mode

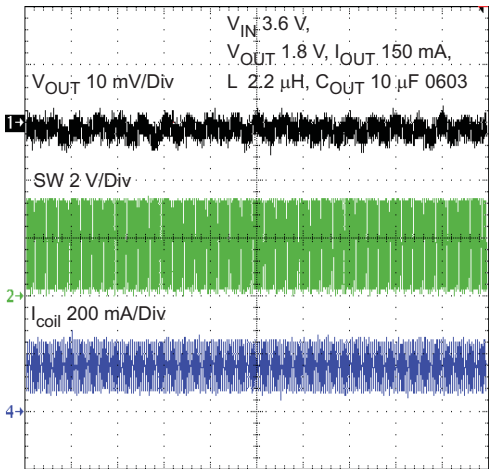


Figure 14. Typical Performance – PWM Mode

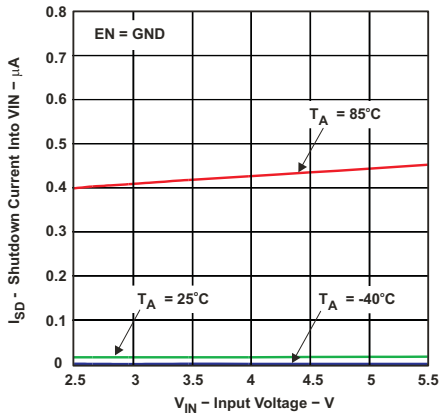


Figure 15. Shutdown Current Into VIN vs Input Voltage

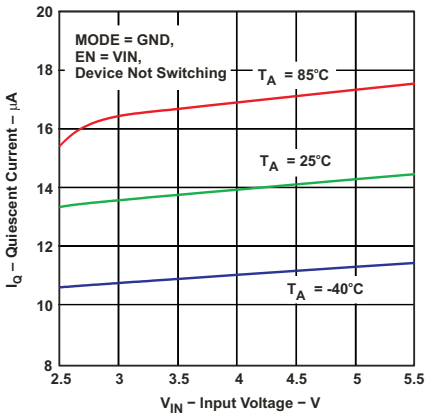


Figure 16. Quiescent Current vs Input Voltage

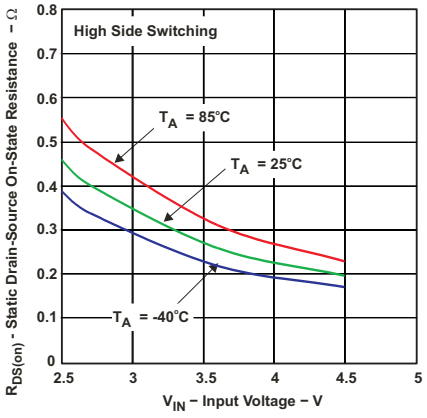


Figure 17. Static Drain-Source On-State Resistance vs Input Voltage

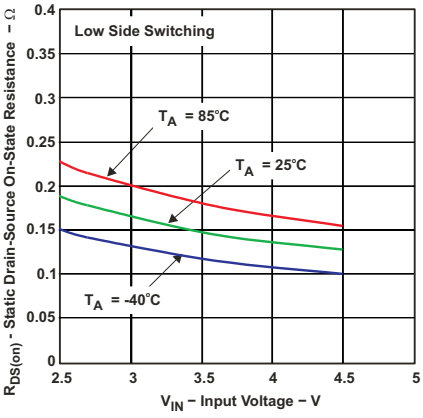
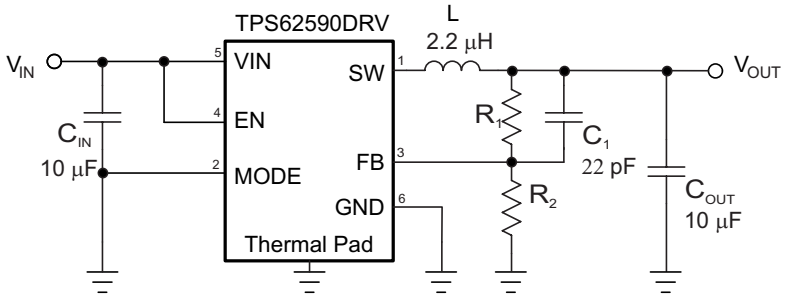


Figure 18. Static Drain-Source On-State Resistance vs Input Voltage

7 Parameter Measurement Information



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8 Detailed Description

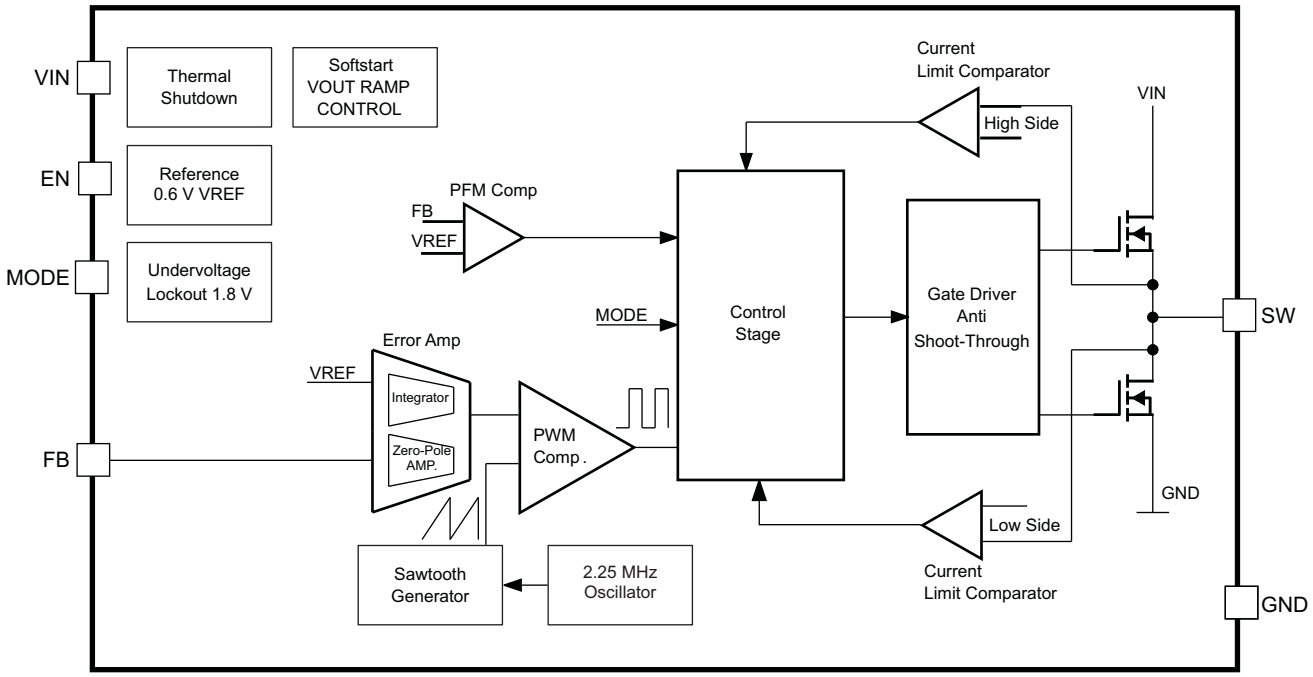
8.1 Overview

The TPS62590-Q1 step-down converter operates with typically 2.25-MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter power-save mode and operates then in PFM mode.

During PWM mode, the converter uses a unique fast-response voltage-mode controller scheme with input-voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current flows now from the input capacitor via the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current-limit comparator also turns off the switch if the current limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current flows now from the inductor to the output capacitor and to the load. It returns to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the high-side MOSFET switch.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable

The device is enabled setting EN pin to high. During start-up time $t_{Start\ Up}$, the internal circuits are settled. Afterwards, the device activates the soft-start circuit. The EN input can be used to control power sequencing in a system with various dc/dc converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and get a sequencing of supply rails. With EN = GND, the device enters shutdown mode. In this mode, all circuits are disabled. In fixed-output-voltage versions, the internal resistor divider network is disconnected from the FB pin.

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Feature Description (continued)

8.3.2 Mode Selection

The MODE pin allows mode selection between forced PWM mode and power-save mode.

Connecting this pin to GND enables the power-save mode with automatic transition between PWM and PFM modes. Pulling the MODE pin high forces the converter to operate in fixed-frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

8.3.3 Soft Start

The TPS62590-Q1 has an internal soft-start circuit that controls the ramp-up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within typically 250 µs. This limits the inrush current in the converter during ramp-up and prevents possible input voltage drops when a battery or high-impedance power source is used. The soft-start circuit is enabled within start-up time $t_{Start\ Up}$.

8.3.4 Short-Circuit Protection

The high-side and low-side MOSFET switches are short-circuit protected with maximum switch current = I_{LIMF}. The current in the switches is monitored by current-limit comparators. Once the current in the high-side MOSFET switch exceeds the threshold of its current-limit comparator, it turns off and the low-side MOSFET switch is activated to ramp down the current in the inductor and high-side MOSFET switch. The high-side MOSFET switch can only turn on again once the current in the low-side MOSFET switch has decreased below the threshold of its current-limit comparator.

8.3.5 100% Duty-Cycle Low-Dropout Mode

The device starts to enter 100% duty-cycle mode once the input voltage comes close the nominal output voltage. To maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing VIN, the high-side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_O max + I_O max \times (r_{DS(on)} max + R_L) \quad (1)$$

with

- $V_O max$ = nominal output voltage plus maximum output-voltage tolerance
- $I_O max$ = maximum output current plus inductor ripple current
- $r_{DS(on)} max$ = maximum P-channel switch $r_{DS(on)}$
- R_L = DC-resistance of the inductor

8.3.6 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the output stage of the converter. The undervoltage lockout threshold is typically 1.85 V with falling V_{IN}.

8.3.7 Thermal Shutdown

As soon as the junction temperature T_J exceeds 140°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

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8.4 Device Functional Modes

8.4.1 Power-Save Mode

The power-save mode is enabled with the MODE pin set to low level. If the load current decreases, the converter enters power-save mode automatically. During power-save mode, the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage 1% above the nominal output voltage typically. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous-conduction mode.

During the power-save mode, the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of VOUT nominal + 1%, the device starts a PFM current pulse. For this, the high-side MOSFET switch turns on and the inductor current ramps up. After the on-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage rises. If the output voltage is equal to or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15-µA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses is generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a fast single-threshold comparator, the output voltage ripple during PFM mode can be kept small. The PFM pulse is time-controlled, which allows modifying the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values minimizes the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values.

The PFM mode is left and PWM mode entered in case the output current can no longer be supported in PFM mode. The power-save mode can be disabled by setting the MODE pin to high. The converter then operates in fixed-frequency PWM mode.

8.4.2 Dynamic Voltage Positioning

This feature reduces the voltage under- and overshoots at load steps from light to heavy load and vice versa. It is active in power-save mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

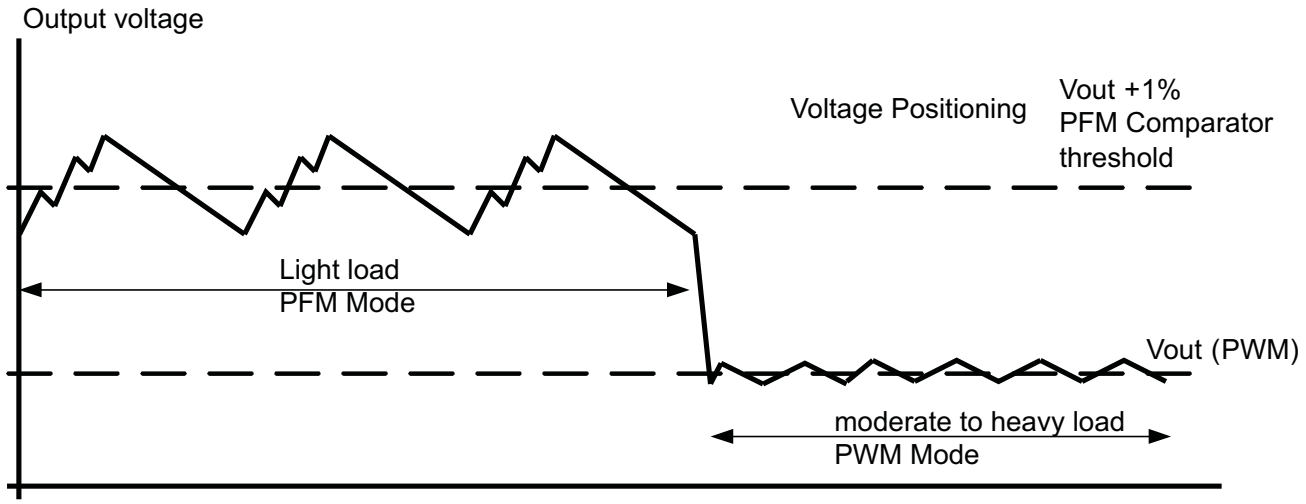

Figure 19. Operation In Power-Save Mode

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS62590-Q1 device is a highly efficient, synchronous step-down, DC-DC converter with an adjustable output voltage and an output current of up to 1 A. The device can be used in buck converter applications with an input range from 2.5 V to 6 V. The TPS62590-Q1 device is optimized for space constrained applications and consumes 15-µA current (typ) in power-save mode.

9.2 Typical Application

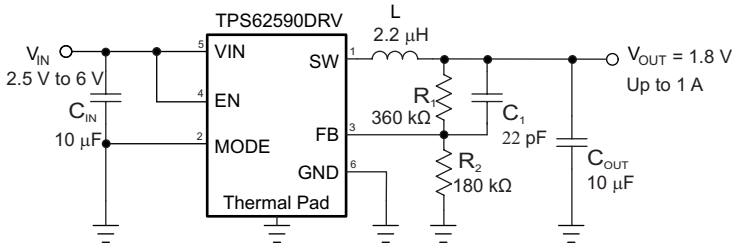

Figure 20. TPS62590-Q1DRV Adjustable 1.8 V

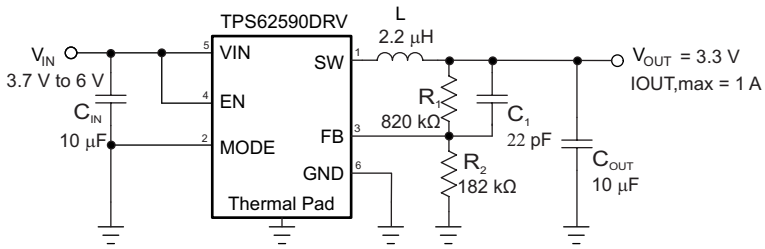

Figure 21. TPS62590-Q1DRV Adjustable 3.3 V

9.2.1 Design Requirements

The input voltage for this device must be from 2.5 V to 6 V. The output voltage must be set using an external voltage divider. The internal compensation network of the device is optimized for an LC output filter that is composed of a 2.2-µH inductor and a 10-µF ceramic capacitor with a external feed-forward capacitor of 22 pF. The *Recommended Operating Conditions* table specifies the allowed range for input voltages, output voltages, output current, output inductor and output buffer capacitor. The values listed in this table must be followed when designing the regulator. Low-ESR ceramic capacitors should be used at the input and output for better filtering and ripple performance. The *Detailed Design Procedure* section provides the necessary equations and guidelines for selecting external components for this regulator.

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Typical Application (continued)

9.2.2 Detailed Design Procedure

Table 2 lists the recommended components for the circuit shown in *Parameter Measurement Information*.

Table 2. List of Components

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER	VALUE
C_{IN}	GRM188R60J106M	Murata	10-µF, 6.3-V. X5R ceramic
C_{OUT}	GRM188R60J106M	Murata	10-µF, 6.3-V. X5R ceramic
C_1		Murata	22-pF, ceramic
L_1	LPS3015	Coilcraft	2.2 µH, 110 mΩ
R_1, R_2	Values depending on the programmed output voltage		

9.2.2.1 Output Voltage Setting

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

where

- internal reference voltage V_{REF} = 0.6 V typically

To minimize the current through the feedback divider network, R2 should be 180 kΩ or 360 kΩ. The sum of R1 and R2 should not exceed approximately 1 MΩ, to keep the network robust against noise.

9.2.2.2 External Feed-Forward Capacitor

An external feedforward capacitor C1 is required for optimum load-transient response. The value of C1 should be in the range between 22 pF and 33 pF.

9.2.2.3 Output Filter Design (Inductor and Output Capacitor)

The *Recommended Operating Conditions* table lists the allowed range of inductor and capacitor. For stable operation, L and C values of the output filter should not fall below 1-µH effective inductance and 3.5-µF effective capacitance.

9.2.2.3.1 Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

The inductor selection also impacts the output-voltage ripple in PFM mode. Higher inductor values lead to lower output-voltage ripple and higher PFM frequency; lower inductor values lead to a higher output-voltage ripple but lower PFM frequency.

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Equation 3 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 4. This is recommended because during heavy load transients the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \tag{3}$$

$$I_L max = I_{OUT} max + \frac{\Delta I_L}{2} \tag{4}$$

where

- f = Switching frequency (2.25 MHz, typical)
- L = Inductor Value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter.

Accepting larger values of ripple current allows the use of low inductance values, but results in higher output voltage ripple, greater core losses, and lower output-current capability.

The total losses of the coil have a strong impact on the efficiency of the dc/dc conversion and consist of both the losses in the dc resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

9.2.2.3.2 Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the TPS62590-Q1 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output-voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode, and the RMS ripple current is calculated as:

$$I_{RMSC_{OUT}} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{5}$$

The overall output voltage ripple under the same conditions is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \tag{6}$$

At light load currents, the converter operates in power-save mode, and the output-voltage ripple is dependent on the output capacitor and inductor values. Larger output capacitor and inductor values minimize the voltage ripple in PFM mode and tighten dc output accuracy in PFM mode.

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9.2.2.3.3 Input Capacitor Selection

The buck converter has a natural pulsating input current; therefore, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 10-µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the V_{IN} pin. The ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

9.2.3 Application Curves

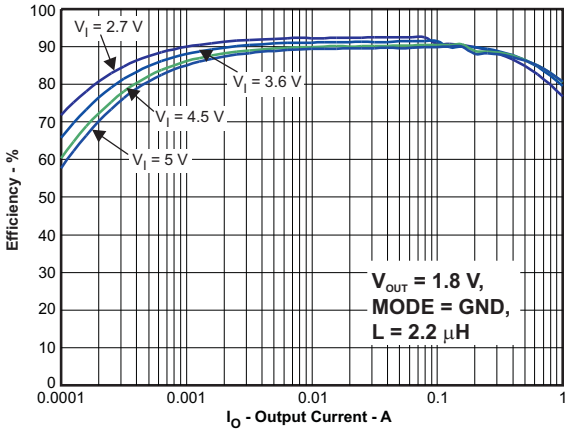

Figure 22. Efficiency vs Output Current for V_{OUT} = 1.8 V (Power-Save Mode)

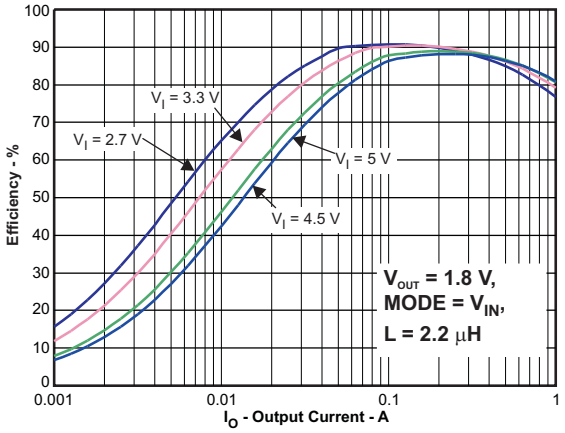

Figure 23. Efficiency vs Output Current for V_{OUT} = 1.8 V (Forced PWM Mode)

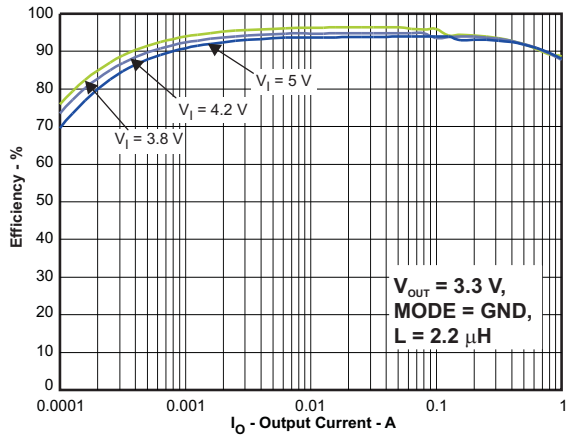

Figure 24. Efficiency vs Output Current for V_{OUT} = 3.3 V (Power-Save Mode)

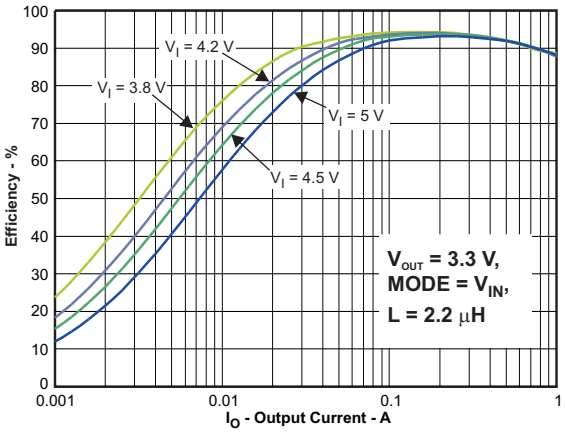

Figure 25. Efficiency vs Output Current for V_{OUT} = 3.3 V (Forced PWM Mode)

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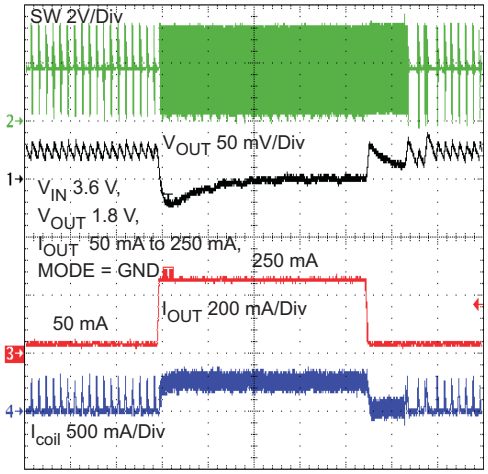

Figure 26. PFM to PWM to PFM Load Transient

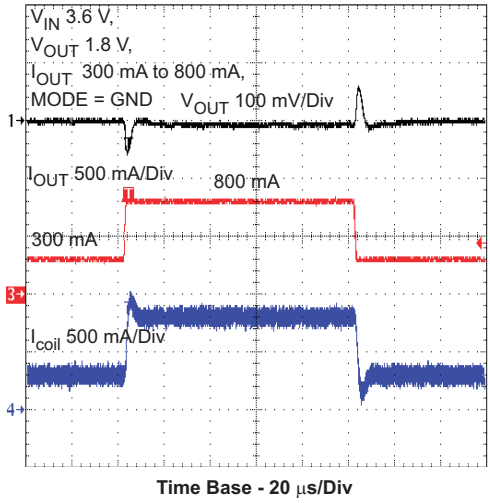

Figure 27. PWM Load Transient

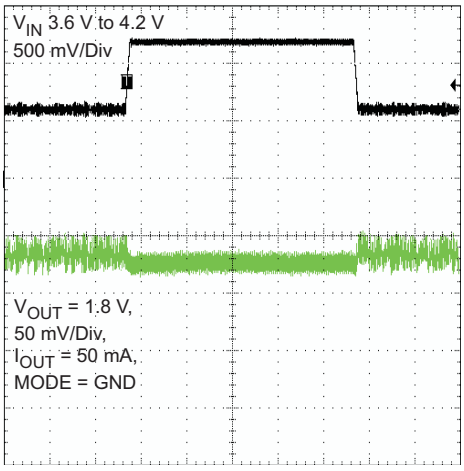

Figure 28. PFM Line Transient

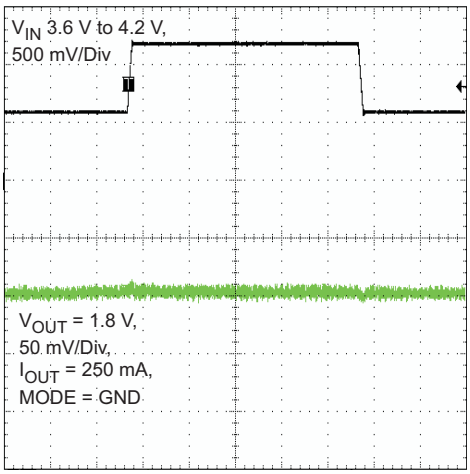

Figure 29. PWM Line Transient

10 Power Supply Recommendations

The TPS62590-Q1 device is designed to operate for an input voltage range from 2.5 V to 6 V. For the VIN pin, TI recommends a low ESR ceramic capacitor with a typical value of 10 µF for most applications. Capacitance derating for aging, temperature, and DC bias must be taken into account while determining the capacitor value.

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11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues, and EMI problems.

The following list details some generic layout guidelines for the TPS62590-Q1 device:

- It is critical to provide a low-inductance, low-impedance ground path and hence use wide and short traces for the main current paths.
- The input capacitor, output capacitor, and inductor should be placed as close as possible to the IC pins.
- Connect the GND pin of the device to the thermal pad of the PCB and use this pad as a star point.
- Use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Connect these ground nodes together at the thermal pad (star point) underneath the IC.
- Keep the traces to the GND pin, coming from small-signal components and the high current of the output capacitors, as short as possible to avoid ground noise.
- The output feedback line should be connected close to the output capacitor and routed away from noisy components and traces (for example, the SW line).
- Trace to the FB pin from voltage divider resistors center point should be as short as possible and should be away from noise sources, such as the inductor or the SW line.
- Add multiple thermal via's on the device thermal pad for better thermal performance.

11.2 Layout Example

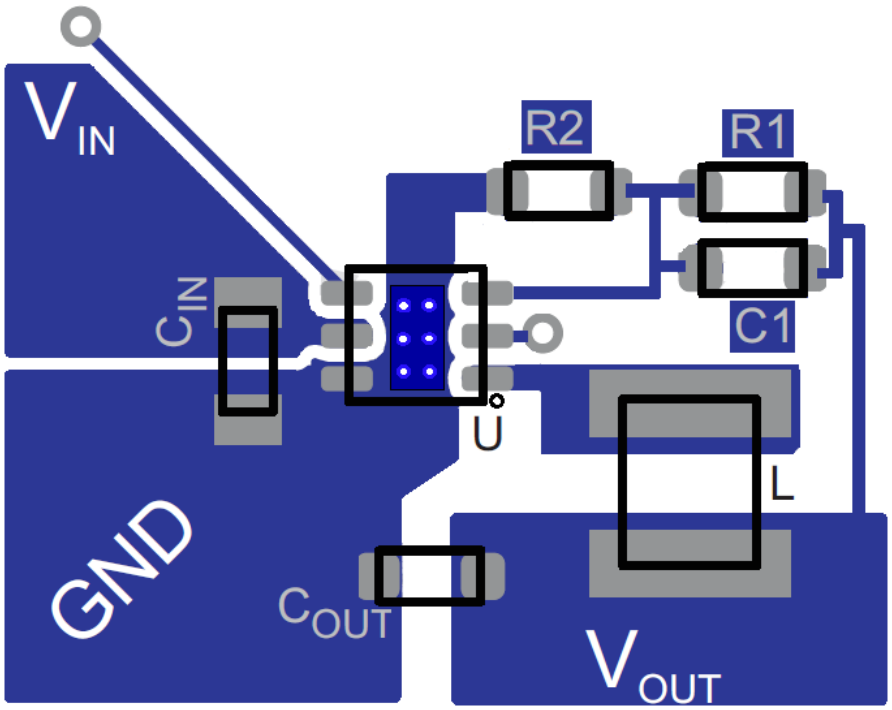

Figure 30. Layout

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62590TDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	QWT
TPS62590TDRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	QWT
TPS62590TDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	QWT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS62590-Q1 :

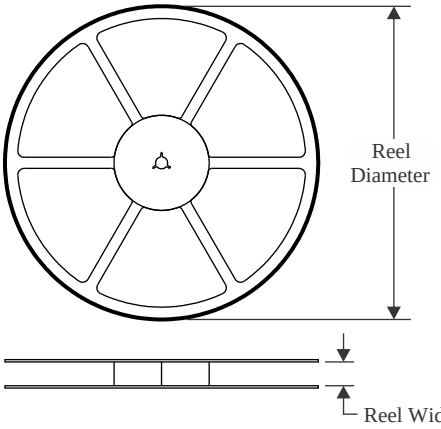
- Catalog : TPS62590

NOTE: Qualified Version Definitions:

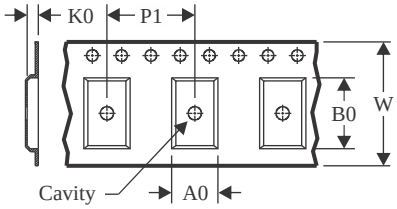
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

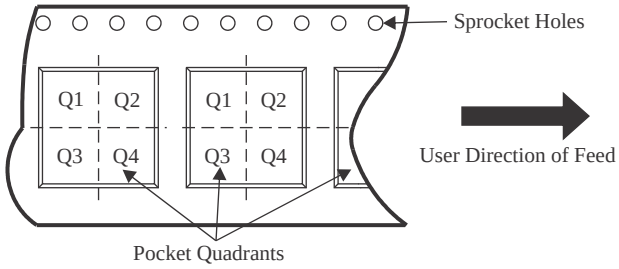


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

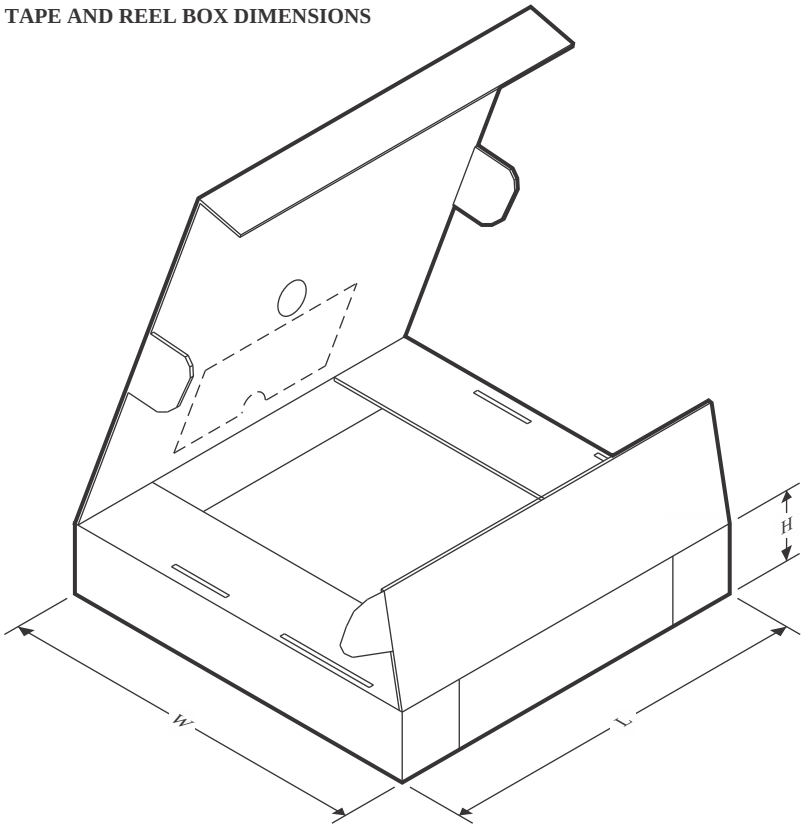
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62590TDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62590TDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

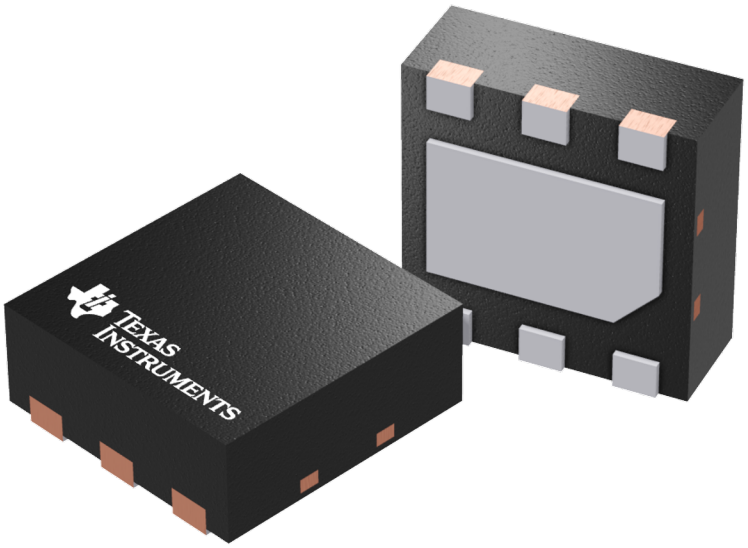


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62590TDRVRQ1	WSON	DRV	6	3000	213.0	191.0	35.0
TPS62590TDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



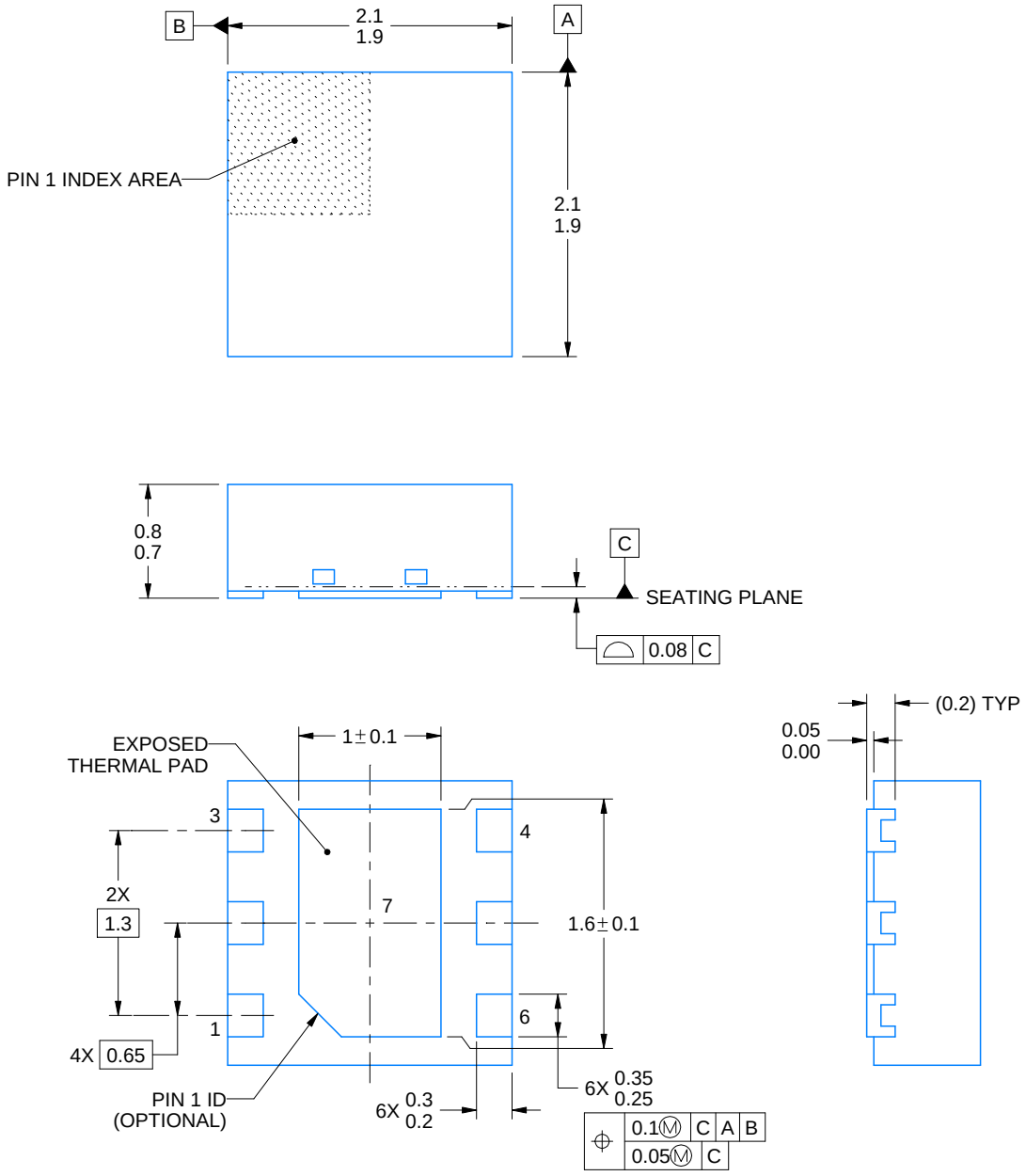
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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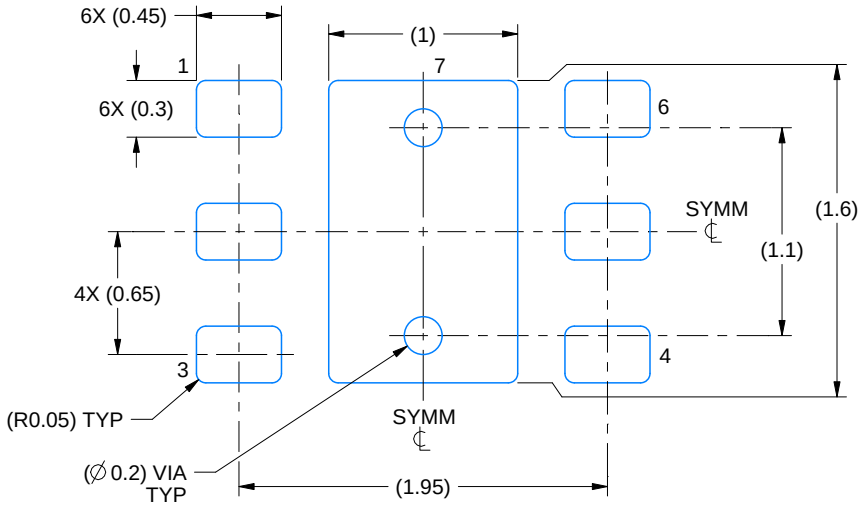
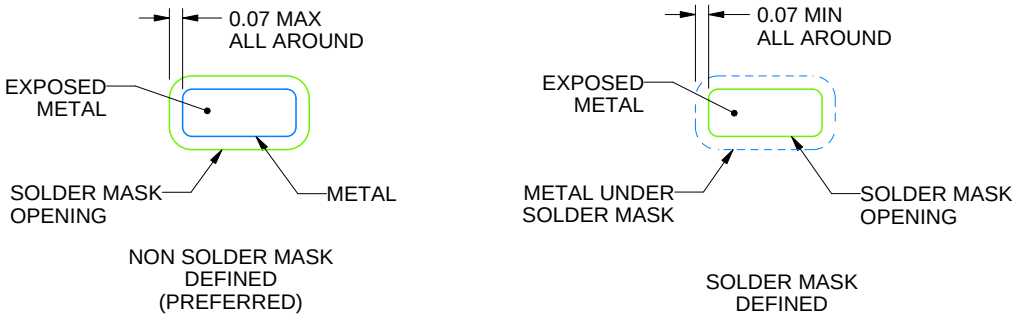
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

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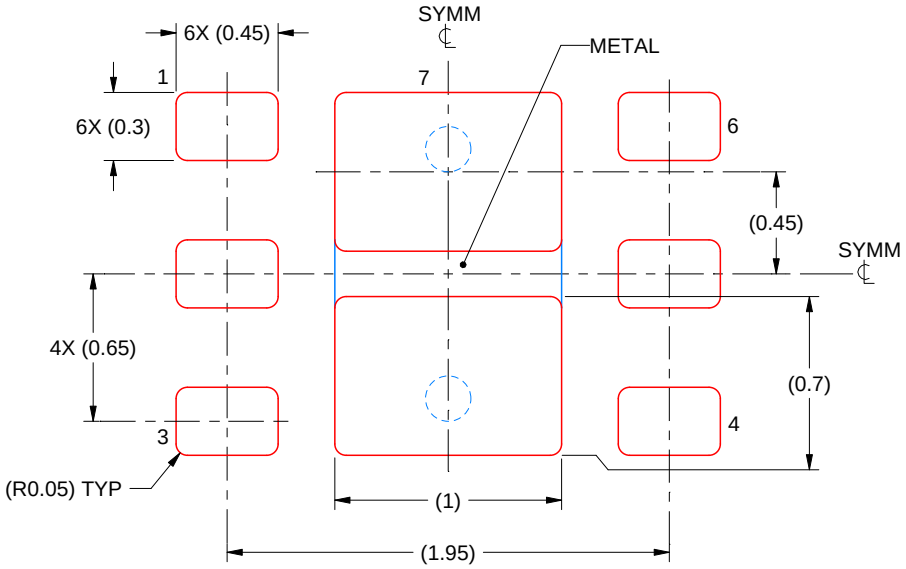
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



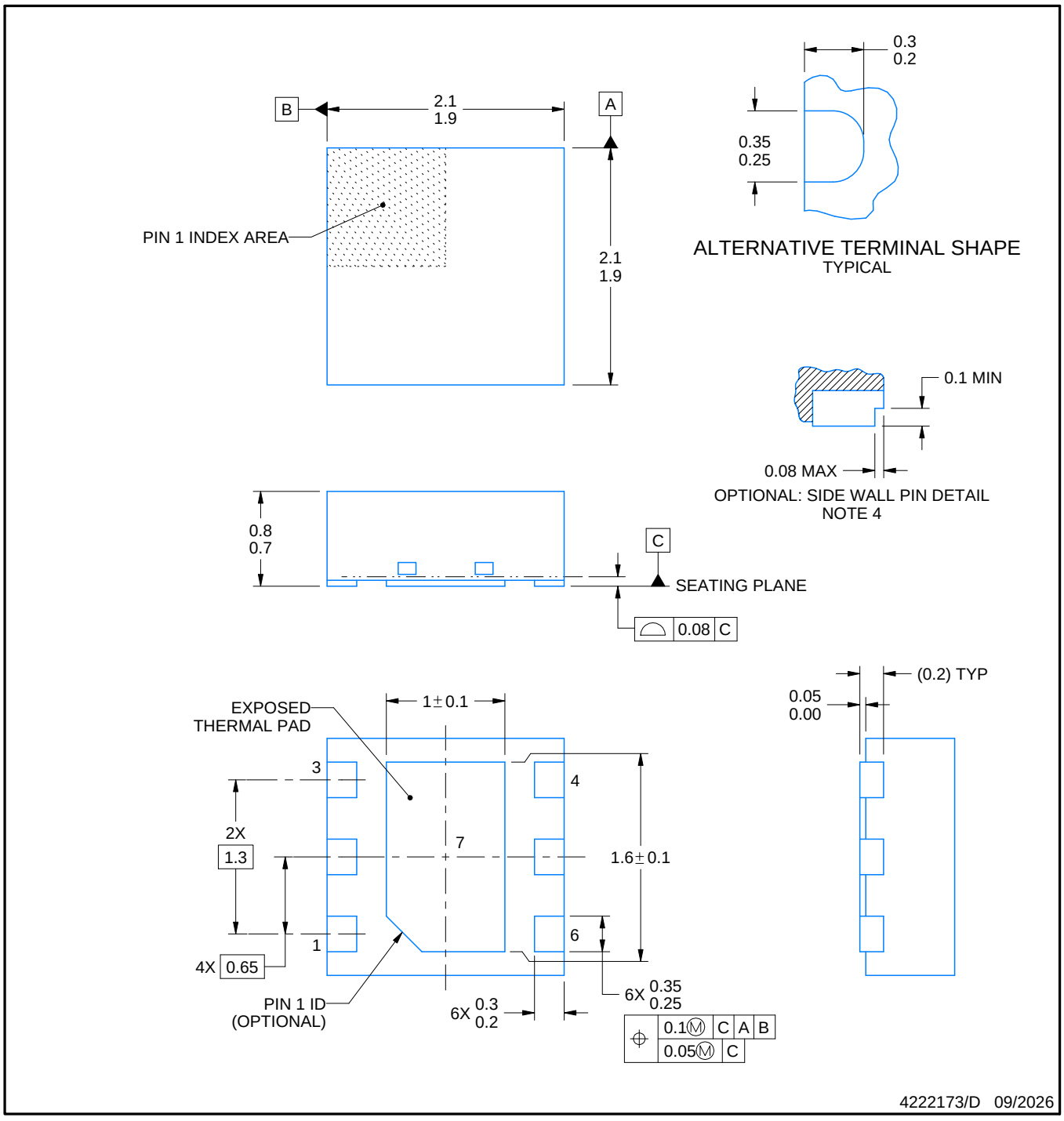
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

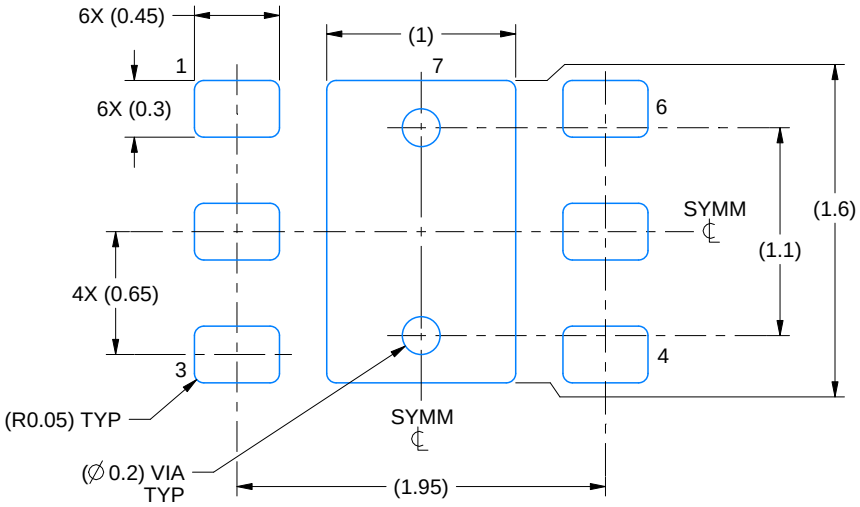
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

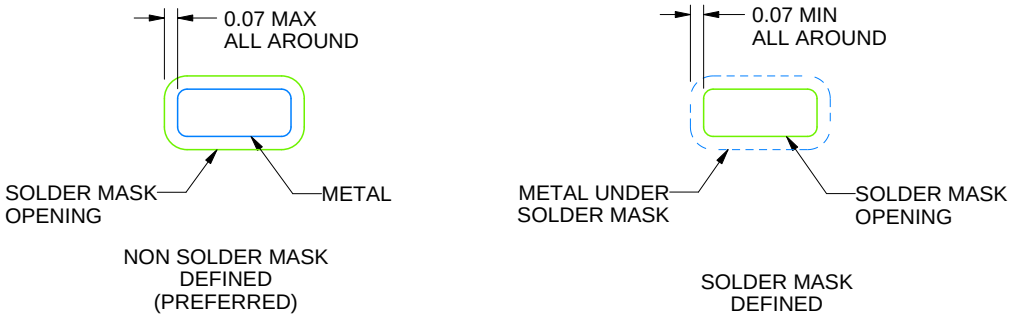


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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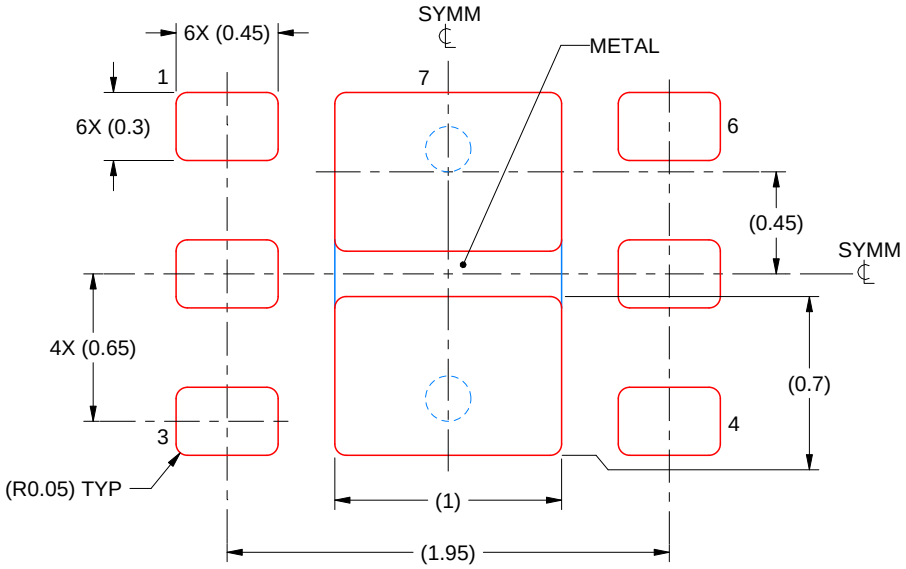
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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