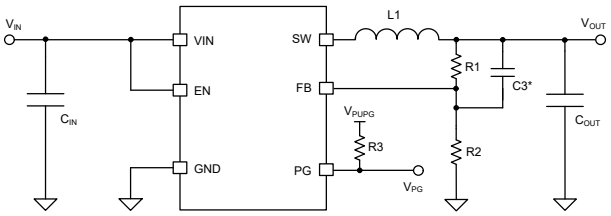
# TPS62A02x-Q1, 2A, High-Efficiency, Automotive, Synchronous Buck Converters in an SOT-563 Package

## 1 Features

- 2.5V to 5.5V input voltage range
- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C $T_A$
- 0.6V to $V_{IN}$ adjustable output voltage range
- 42mΩ and 27.5mΩ low $R_{DSON}$ switches
- < 28µA quiescent current
- 1.5% feedback accuracy (–40°C to 125°C)
- 100% mode operation
- 2.2MHz switching frequency
- Power save mode or FPWM parts available
- Power-good output pin
- Short-circuit protection (HICCUP)
- Internal soft start-up
- Active output discharge
- Thermal shutdown protection
- Pin-to-pin compatible with the TPS62A01-Q1
- $C_{IN}$ of 4.7µF, $C_{OUT}$ of 22µF and 1µH inductor

## 2 Applications

- Front camera
- Surround view system ECU
- Automotive cluster display




**Typical Application**

## 3 Description

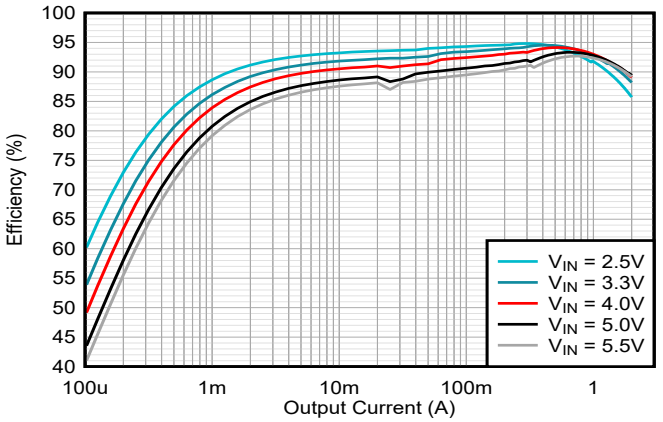
The TPS62A02-Q1 and TPS62A02A-Q1 are synchronous, step-down, buck DC-DC converters optimized for high efficiency and compact design size. The devices integrate switches capable of delivering an output current up to 2A. At medium to heavy loads, the devices operate in pulse width modulation (PWM) mode with 2.2MHz switching frequency. At light load, the TPS62A02-Q1 automatically enters a power save mode (PSM) to maintain high efficiency over the entire load current range. In shutdown, the current consumption is minimal as well. The TPS62A02A-Q1 variant of this device operates in forced PWM across the whole load current range and maintains a constant switching frequency.

The TPS62A02x-Q1 devices provide an adjustable output voltage through an external resistor divider. An internal soft-start circuit limits the inrush current during start-up and a power good signal indicates when the output voltage is at target. Overcurrent protection and thermal shutdown protect application and device. The devices are available in an SOT-563 package.

**Device Information**

| PART NUMBER(3) | OPERATION MODE | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|---|
| TPS62A02-Q1 | PSM, PWM | DRL (SOT-563, 6) | 1.60mm × 1.60mm |
| TPS62A02A-Q1 | FPWM | | |

(1) For more information, see the Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) See the *Device Comparison Table*.




**Efficiency vs Output Current at $5V_{IN}$**

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## 4 Device Comparison Table

| PART NUMBER | OUTPUT CURRENT | PACKAGE | OPERATION MODE |
|---|---|---|---|
| TPS62A02-Q1 | 2A | SOT-563 | PSM, PWM |
| TPS62A02A-Q1 | 2A | SOT-563 | FPWM |

## 5 Pin Configuration and Functions

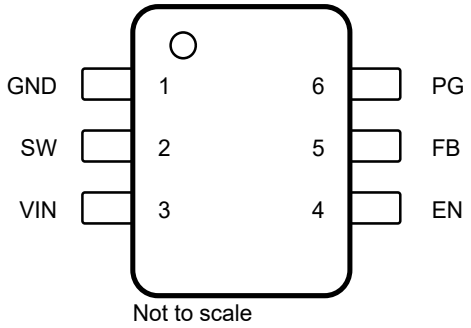


**Figure 5-1. 6-Pin DRL SOT-563 Package (Top View)**

**Table 5-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | 1 | G | Ground pin |
| SW | 2 | O | Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin. |
| VIN | 3 | I | Power supply voltage pin |
| EN | 4 | I | Device enable logic input. Logic high enables the device. Logic low disables the device and turns the device into shutdown. Do not leave the pin floating. |
| FB | 5 | I | Feedback pin for the internal control loop. Connect this pin to an external feedback divider. |
| PG | 6 | O | Power-good open-drain output pin. The pullup resistor cannot be connected to any voltage higher than 5.5V. If unused, leave the pin open or connect to GND. |

(1) I = Input, O = Output, G = Ground

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Pin voltage(2) | VIN, EN, PG | –0.3 | 6 | V |
| | SW, DC | –0.3 | $V_{IN}$ + 0.3 | V |
| | SW, transient < 10ns | –3.0 | 10 | V |
| | FB | –0.3 | 3 | V |
| Operating junction temperature | $T_J$ | –40 | 150 | °C |
| Storage temperature | $T_{stg}$ | –55 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 (1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | ±500 | |

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input supply voltage range | | 2.5 | | 5.5 | V |
| $V_{OUT}$ | Output voltage range | | 0.6 | | $V_{IN}$ | V |
| $I_{OUT}$ | Output current range | TPS62A02-Q1 | | | 2 | A |
| L | Effective inductance | | 0.3 | 1.0 | 1.2 | µH |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ < 1.2V | | 44 | | µF |
| $C_{OUT}$ | Output capacitance | 1.2V ≤ $V_{OUT}$ < 1.8V | | 22 | | µF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ ≥ 1.8V | | 22 | | µF |
| $I_{PG}$ | Power-Good input current capability | | 0 | | 1 | mA |
| $T_J$ | Operating junction temperature | | –40 | | 150 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPS62A02x-Q1 DRL (SOT-563) 6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 157.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 92.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 45.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 4.0 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 45.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.


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## 6.5 Electrical Characteristics

$T_J$ = –40°C to +150°C, $V_{IN}$ = 2.5V to 5.5V. Typical values are at $T_J$ = 25°C and $V_{IN}$ = 5V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $I_{Q(VIN)}$ | VIN quiescent current | Non-switching, $V_{EN}$ = High, $V_{FB}$ = 610mV | | 28 | | µA |
| $I_{SD(VIN)}$ | VIN shutdown supply current | $V_{EN}$ = Low | | 0.15 | 10 | µA |
| **UVLO** | | | | | | |
| $V_{UVLO(R)}$ | VIN UVLO rising threshold | $V_{IN}$ rising | 2.3 | 2.4 | 2.5 | V |
| $V_{UVLO(F)}$ | VIN UVLO falling threshold | $V_{IN}$ falling | 2.2 | 2.3 | 2.4 | V |
| **ENABLE** | | | | | | |
| $V_{EN(R)}$ | EN high-level input voltage | EN rising, enable switching | | | 0.8 | V |
| $V_{EN(F)}$ | EN low-level input voltage | EN falling, disable switching | 0.4 | | | V |
| $V_{EN(LKG)}$ | EN Input leakage current | $V_{EN}$ = 5V | | | 250 | nA |
| **REFERENCE VOLTAGE** | | | | | | |
| $V_{FB}$ | FB voltage | PWM mode | 591 | 600 | 609 | mV |
| | Load dependent output voltage drop (load regulation) | PWM mode | | 0.15 | | %/A |
| $I_{FB(LKG)}$ | FB input leakage current | $V_{FB}$ = 0.6V | | | 100 | nA |
| **SWITCHING FREQUENCY** | | | | | | |
| $f_{SW(FCCM)}$ | Switching frequency, FPWM operation | $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V | | 2200 | | kHz |
| **STARTUP** | | | | | | |
| | Internal fixed soft-start time | From EN = High to $V_{FB}$ = 0.56V; $V_{OUT}$ = 0.6V | 0.3 | | 1.2 | ms |
| **POWER STAGE** | | | | | | |
| $R_{DSON(HS)}$ | High-side MOSFET on-resistance | $V_{IN}$ = 5V | | 42 | | mΩ |
| $R_{DSON(LS)}$ | Low-side MOSFET on-resistance | $V_{IN}$ = 5V | | 28 | | mΩ |
| **OVERCURRENT PROTECTION** | | | | | | |
| $I_{HS(OC)}$ | High-side peak current limit | TPS62A02-Q1; VIN = 3.3V | 2.7 | 3.3 | | A |
| $I_{LS(OC)}$ | Low-side valley current limit | TPS62A02-Q1; VIN = 3.3V | | 3.2 | | A |
| $IL_{PEAK(min)}$ | Peak inductor current in PSM | | | 0.5 | | A |
| **POWER GOOD** | | | | | | |
| $V_{PGTH}$ | Power-Good threshold | PG high to low (falling edge), FB falling | | 93.5 | | % |
| $V_{PGTH}$ | Power-Good threshold | PG low to high (rising edge), FB rising | | 96 | | % |
| | PG delay falling | | | 35 | | µs |
| | PG delay rising | | | 11 | | µs |
| $I_{PG(LKG)}$ | PG pin Leakage current when open drain output is high | $V_{PG}$ = 5V | | | 100 | nA |
| | PG pin output low-level voltage | $I_{PG}$ = 1mA | | | 300 | mV |
| **OUTPUT DISCHARGE** | | | | | | |
| | Output discharge current on SW pin | $V_{IN}$ = 3V, $V_{OUT}$ = 2.0V | | 120 | | mA |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{J(SD)}$ | Thermal shutdown threshold | Temperature rising | | 165 | | °C |
| $T_{J(HYS)}$ | Thermal shutdown hysteresis | | | 20 | | °C |

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# 7 Typical Characteristics

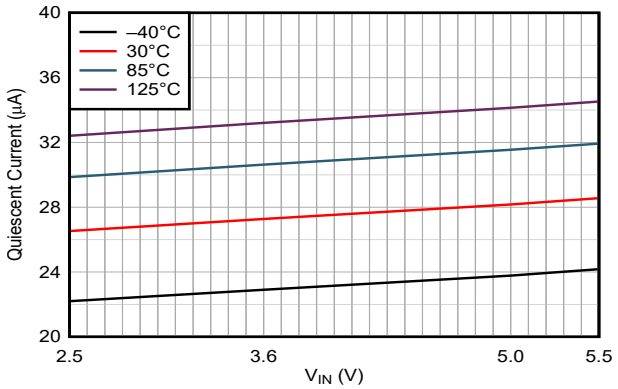


**Figure 7-1. Quiescent Current vs Input Voltage**

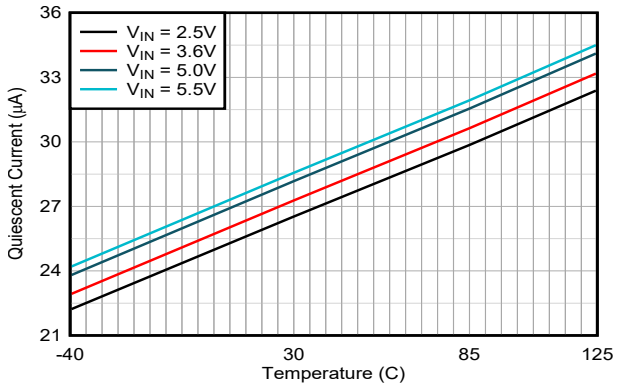


**Figure 7-2. Quiescent Current vs Junction Temperature**

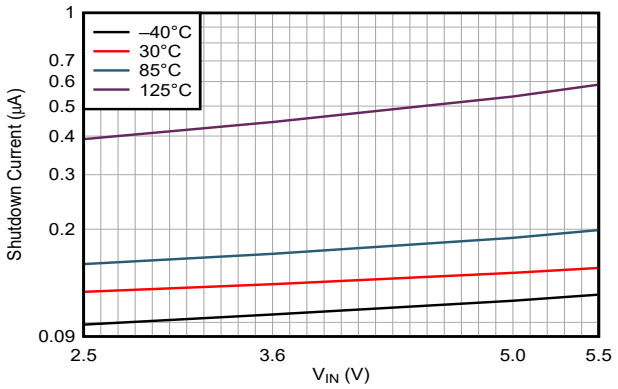


**Figure 7-3. Shutdown Current vs Input Voltage**

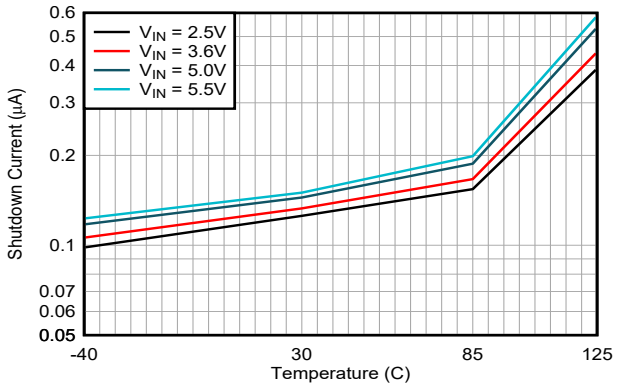


**Figure 7-4. Shutdown Current vs Junction Temperature**


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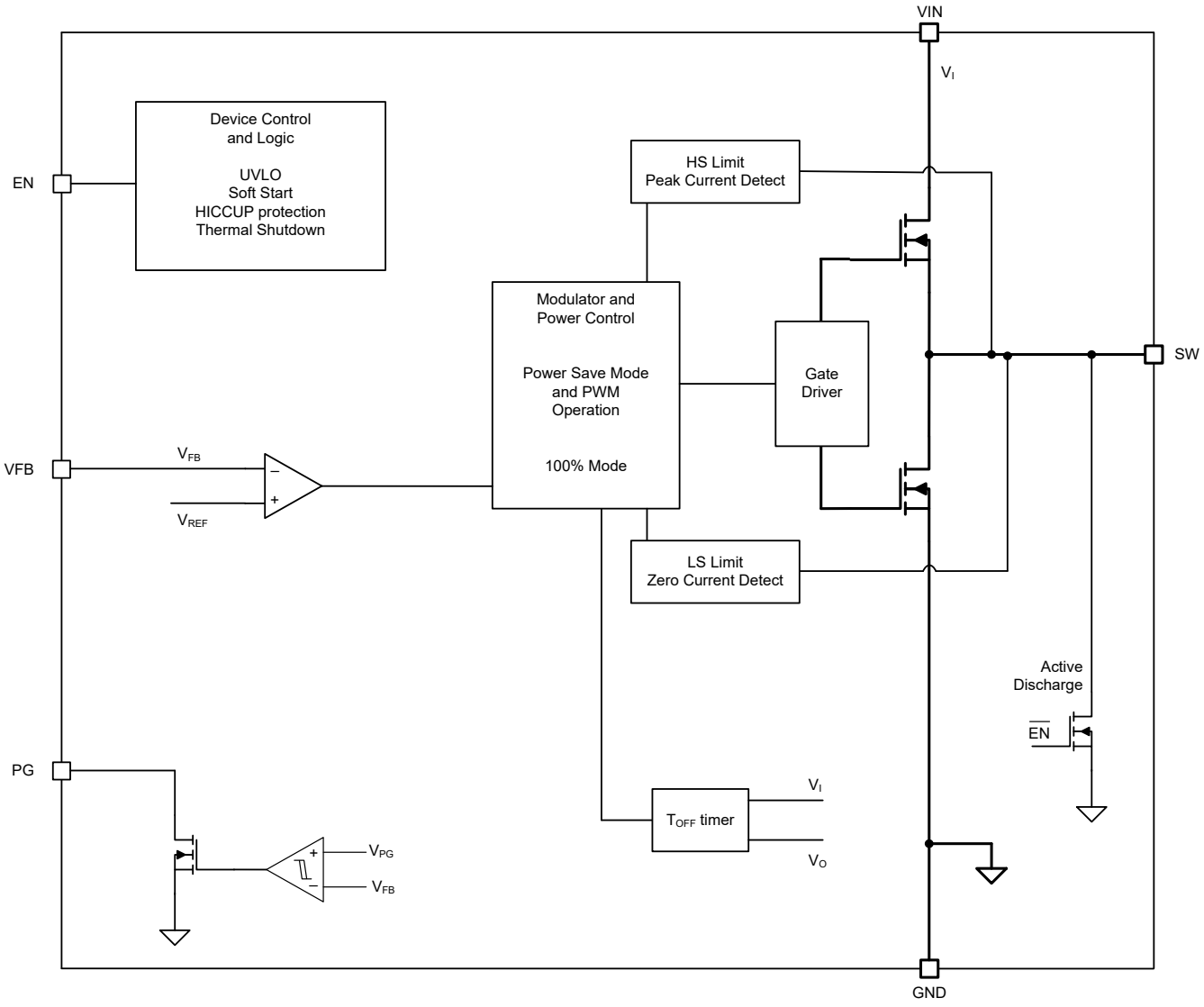
# 8 Detailed Description

## 8.1 Overview

The TPS62A02-Q1 and TPS62A02A-Q1 are a family of high-efficiency, synchronous, step-down converters. The devices operates with an adaptive off time with a peak current control scheme. The TPS62A02A-Q1 has a typical operating frequency of 2.2MHz and uses pulse width modulation (PWM) for output voltage regulation. Based on the $V_{IN}/V_{OUT}$ ratio, a simple circuit sets the required off time for the low-side MOSFET, making the switching frequency relatively constant regardless of the variation of the input voltage, output voltage, and load current. The TPS62A02-Q1 reduces the switching frequency at light load to save power.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Power Save Mode

The device automatically enters power save mode to improve efficiency at light load when the inductor current becomes discontinuous. In power save mode, the converter reduces the switching frequency and minimizes current consumption. In power save mode, the output voltage rises slightly above the nominal output voltage. This effect minimizes by increasing the output capacitor or adding a feedforward capacitor.

### 8.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (1)$$

where

- $R_{DS(ON)}$ = High-side FET on-resistance
- $R_L$ = Inductor ohmic resistance (DCR)

### 8.3.3 Soft Start

After enabling the device, internal soft-start circuitry ramps up the output voltage, which reaches the nominal output voltage during start-up time, avoiding excessive inrush current and creating a smooth voltage rise slope. Internal soft-start circuitry also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TPS62A02x-Q1 is able to start into a prebiased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to the nominal value.

### 8.3.4 Switch Current Limit and Short-Circuit Protection (HICCUP)

The switch current limit prevents the device from high inductor current and drawing excessive current from the battery or input rail. Due to internal propagation delay, the AC peak current can exceed the static current limit during that time. Excessive current can occur with a shorted or saturated inductor, an overload, or shorted output circuit condition. If the inductor current reaches the threshold $I_{LIM}$, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current with an adaptive off time.

When this switch current limit is triggered 32 times, the device stops switching to protect the output. The device then automatically starts a new start-up after a typical delay time of 100µs has passed. This action is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears. HICCUP protection is also enabled during the start-up.

### 8.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than $V_{UVLO}$.

### 8.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds $T_{J(SD)}$. When the device temperature falls below the threshold by $T_{J(HYS)}$, the device returns to normal operation automatically.

## 8.4 Device Functional Modes

### 8.4.1 Enable and Disable

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and not left floating.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### 8.4.2 Power Good

The TPS62A02x-Q1 has a built-in power-good (PG) feature to indicate whether the output voltage has reached the target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. VIN must remain present for the PG pin to stay low. If not used, the power-good can be tied to GND or left open. The PG indicator has a deglitch to avoid the signal indicating glitches or transient responses from the loop.

**Table 8-1. Power-Good Indicator Functional Table**

| LOGIC SIGNALS | | | | PG STATUS |
|---|---|---|---|---|
| $V_I$ | EN PIN | THERMAL SHUTDOWN | $V_O$ | |
| $V_I$ > UVLO | HIGH | NO | $V_O$ ≧ target | High impedance |
| | | | $V_O$ < target | LOW |
| | | YES | x | LOW |
| | LOW | x | x | LOW |
| 1.8V ≦ $V_I$ ≦ UVLO | x | x | x | LOW |
| $V_I$ < 1.8V | x | x | x | Undefined |

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# 9 Application and Implementation

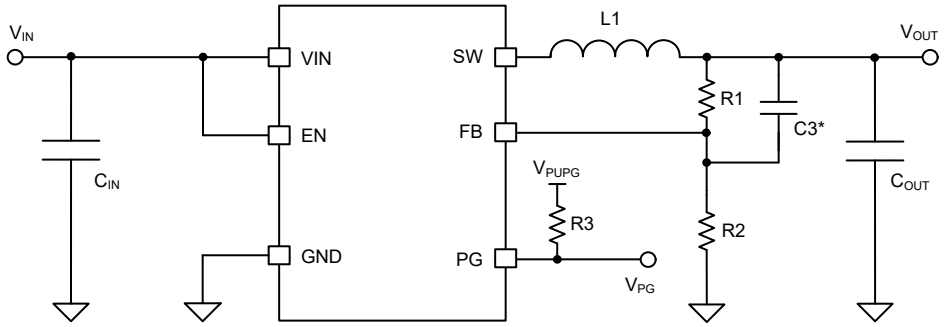
**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

## 9.2 Typical Application




A. C3 is optional

**Figure 9-1. TPS62A02-Q1 Typical Application Circuit**

### *9.2.1 Design Requirements*

For this design example, use the parameters listed in Table 9-1 as the input parameters

**Table 9-1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage | 2.5V to 5.5V |
| Output voltage | 1.8V |
| Maximum output current | 2A |

Table 9-2 lists the components used for the example.

**Table 9-2. List of Components**

| REFERENCE | DESCRIPTION | MANUFACTURER(1) |
|---|---|---|
| C1 | 4.7µF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BR71A475KA73L | Murata |
| C2 | 22µF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BZ71A226KE15L | Murata |
| L1 | 1µH, Power Inductor, XGL3520-102MEC | Coilcraft |
| R1, R2, R3 | R1 = 200kΩ, R2 = 100kΩ, R3 = 499kΩ, Chip resistor, 1%, size 0603 | Std. |
| C3 | Optional up to 120pF, checked with 10pF for 3.3V, 15pF for 1.8V, and 22pF for 1.2V VOUT using this bill of material. When implementing changes, make sure phase margin of > 45 degrees through Bode measurement. | Std. |

(1) See the *Third-Party Products Disclaimer*.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### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Setting the Output Voltage

The output voltage of the TPS62A02-Q1 is adjustable. The output voltage can be set from 0.6V to $V_{IN}$ using a resistor divider from $V_{OUT}$ to GND. The voltage at the FB pin is regulated to 600mV. The value of the output voltage is set by the output resistor divider. The values of these resistors can be calculated by Equation 2 or by using the resistor values from Table 9-3. TI recommends to choose resistor values that allow a current of at least 2µA, meaning the value of $R_2$ must not exceed 400kΩ. Lower resistor values have a positive impact on accuracy and robustness.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) \quad (2)$$

**Table 9-3. Setting the Output Voltage**

| NOMINAL OUTPUT VOLTAGE $V_{OUT}$ | $R_1$ | $R_2$ | EXACT OUTPUT VOLTAGE |
|---|---|---|---|
| 0.75V | 10kΩ | 40.2kΩ | 0.7493V |
| 0.8V | 16.9kΩ | 51kΩ | 0.7988V |
| 1.0V | 20kΩ | 30kΩ | 1.0V |
| 1.1V | 39.2kΩ | 47kΩ | 1.101V |
| 1.2V | 68kΩ | 68kΩ | 1.2V |
| 1.5V | 76.8kΩ | 51kΩ | 1.5V |
| 1.8V | 80.6kΩ | 40.2kΩ | 1.803V |
| 2.5V | 47.5kΩ | 15kΩ | 2.5V |
| 3.3V | 88.7kΩ | 19.6kΩ | 3.315V |

#### 9.2.2.2 Feed Forward Capacitor CFF

A feedforward capacitor reduces the output ripple in PSM and improves the load transient response. The optimum value for $C_{FF}$ depends on the impedance of the feedback divider, the required transient voltage and the accepted ringing. If no ringing of VOUT is accepted then the optimum $C_{FF}$ is 10pF for 3.3V VOUT, 15pF for 1.8V and 22pF for 1.2V assuming the bottom resistor (R2) of the feedback divider been selected as 100kΩ. More information about $C_{FF}$ selection and optimization can be found in application report *Feedforward Capacitor to Improve Stability and Bandwidth With the TPS621-Family and TPS821-Family* application note

#### 9.2.2.3 Inductor Selection

The TPS62A02-Q1 is designed for inductors with an effective inductance between 300nH and 1.2µH inductor with a switching frequency of typically 2.2MHz. Inductor selection follows these tradeoffs:

- Larger inductance
  - Helps achieving a higher efficiency at output currents below 1A
  - Has a positive impact on current ripple
  - Results in lower output voltage ripple
  - Decreases transient response performance
- Smaller inductance
  - Has a positive impact on inductor form factor at given maximum current capability
  - Is therefore more cost effective
  - Causes a larger inductor current ripple
  - Reduces efficiency
  - Causes larger negative inductor current in forced PWM mode at low or no output current

See Section 6.3 for details.

The inductor selection is affected by several conditions like input voltage range, output voltage, target output voltage ripple with specific output capacitance, and corresponding inductor current ripple. The inductor selection also has influence on the PWM-to-PFM transition point and efficiency. The inductor must be rated for the correct saturation current and average current. The DCR with the influence on converter efficiency must be as low as

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possible. Smaller inductor form factor typically leads to either higher DCR and lower current capabilities or to lower inductance. There are two main types of inductors available for use in buck converters:

- Ferrite inductors
- Iron powder inductors

Iron powder power inductors are very safe to use because the saturation of the magnetic material is soft. This means the inductance decrease resulting from the inductor current is relatively small and even. Even if iron powder inductors are operated close to the data sheet saturation current, there is low risk of damaging the TPS62A02-Q1 by overcurrent. The current rise is slow enough for the overcurrent protection of the TPS62A02-Q1 to still be effective. Contrary to iron powder inductors, a ferrite inductor can have a steep saturation curve. This steep saturation curve results in a much faster inductor current increase after the saturation is reached. There is a potential risk that the current rise is so quick that the overcurrent limit circuit inside the TPS62A02-Q1 cannot follow. Therefore, the application designer planning a saturation current reserve with ferrite inductors, which is large enough to cover the inductor tolerances and special cases like short-circuit and application start-up, is good practice.

Equation 3 calculates the maximum inductor current.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \tag{3}$$

$$\Delta I_{L(max)} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L_{min}} \times \frac{1}{f_{SW}} \tag{4}$$

where

- $I_{L(max)}$ is the maximum inductor current.
- $\Delta I_{L(max)}$ is the peak-to-peak inductor ripple current.
- Lmin is the minimum inductance at the operating point.

#### 9.2.2.4 Input Capacitor

For most applications, 4.7µF nominal is sufficient and recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. TI recommends a low-ESR multilayer ceramic capacitor (MLCC) for the best filtering. The capacitor must be placed between $V_{IN}$ and GND as close as possible to those pins.

#### 9.2.2.5 Output Capacitor

The architecture of the TPS62A02-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep the low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends to use X7R or X8R dielectric. Using a higher value has advantages, like smaller voltage ripple and a tighter DC output accuracy in power save mode. Up to 47µF can be added to the output per default. Higher values above 47µF can be achieved if verified through a bode plot. The peak current mode architecture of the TPS62A02-Q1 is very tolerant to large output capacitance.


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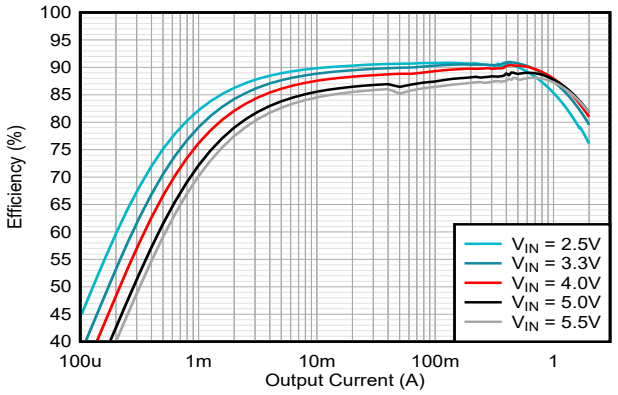
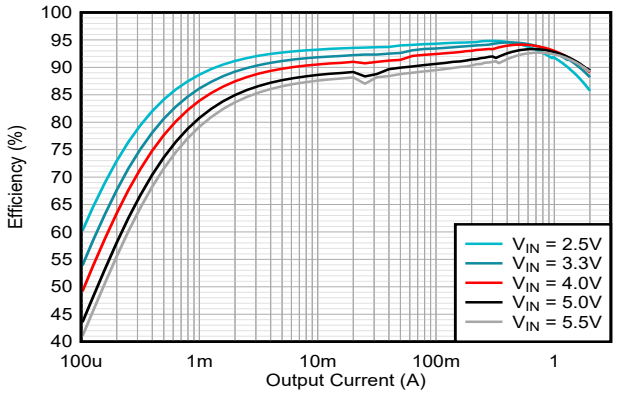
### 9.2.3 Application Curves



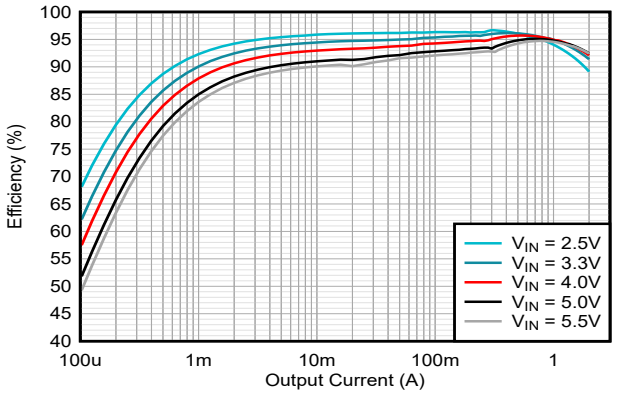

TPS62A02-Q1 (PSM/PWM) SOT-563 (DRL)

**Figure 9-2. 0.6V Output Efficiency**



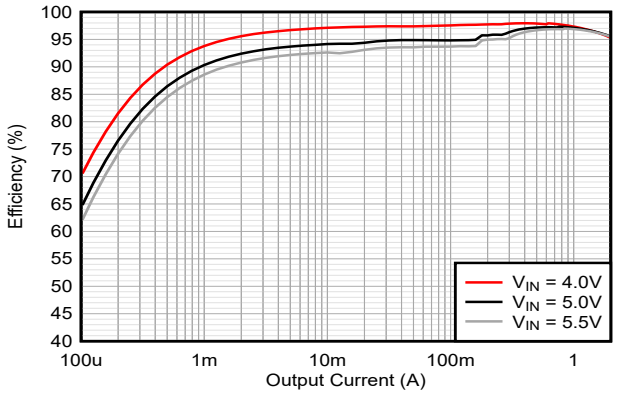

TPS62A02-Q1 (PSM/PWM) SOT-563 (DRL)

**Figure 9-3. 1.2V Output Efficiency**



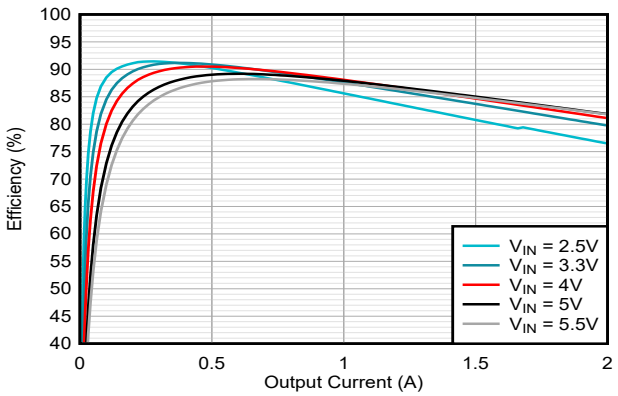

TPS62A02-Q1 (PSM/PWM) SOT-563 (DRL)

**Figure 9-4. 1.8V Output Efficiency**



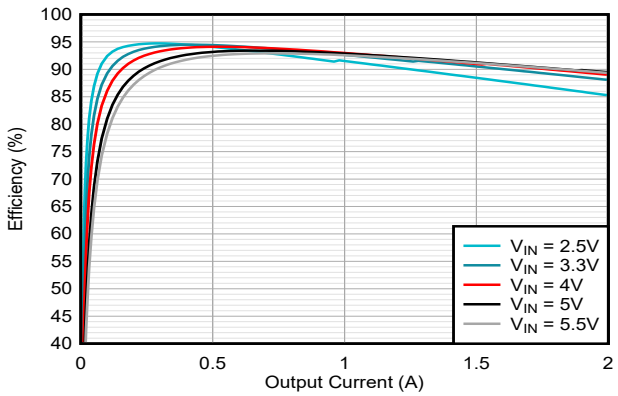

TPS62A02-Q1 (PSM/PWM) SOT-563 (DRL)

**Figure 9-5. 3.3V Output Efficiency**




TPS62A02A-Q1 (FPWM) SOT-563 (DRL)

**Figure 9-6. 0.6V Output Efficiency**




TPS62A02A-Q1 (FPWM) SOT-563 (DRL)

**Figure 9-7. 1.2V Output Efficiency**

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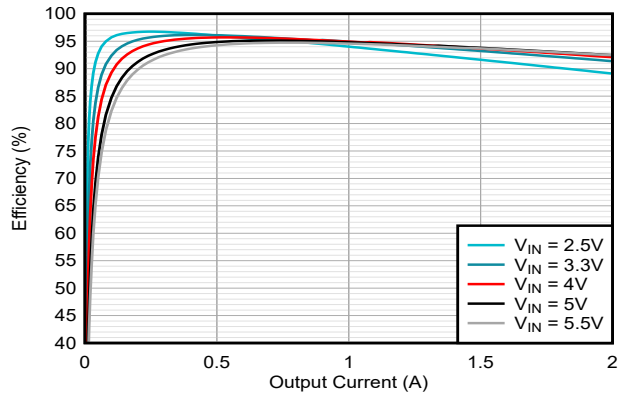
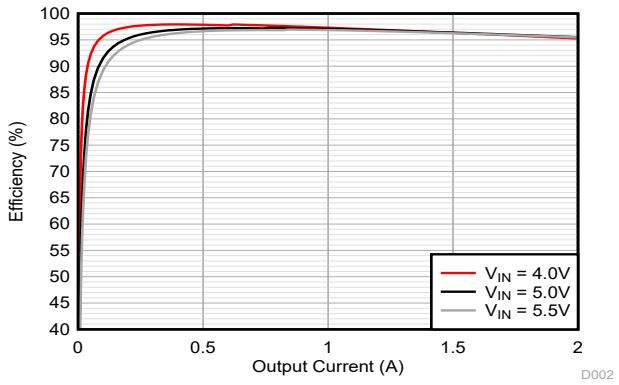


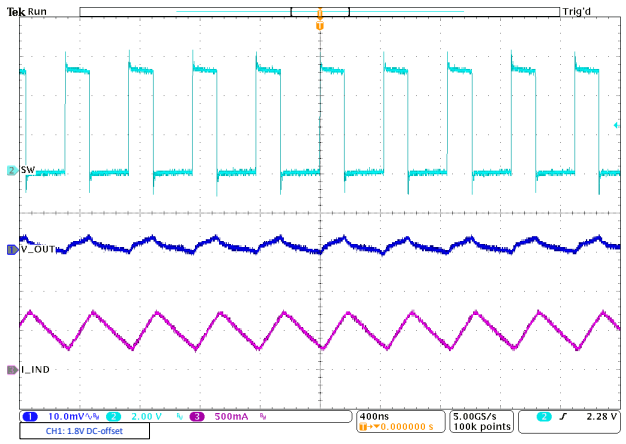

TPS62A02A-Q1 (FPWM) SOT-563 (DRL)

**Figure 9-8. 1.8V Output Efficiency**



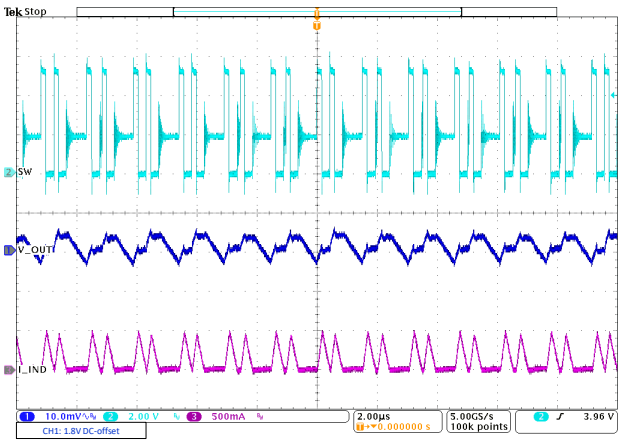

TPS62A02A-Q1 (FPWM) SOT-563 (DRL)

**Figure 9-9. 3.3V Output Efficiency**



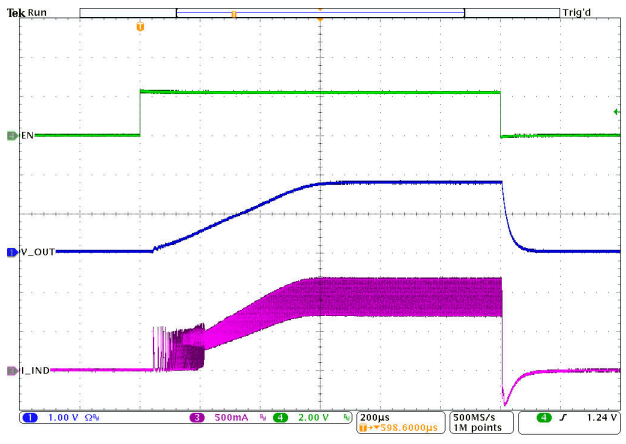

$I_{OUT}$ = 500mA

**Figure 9-10. PWM Operation**



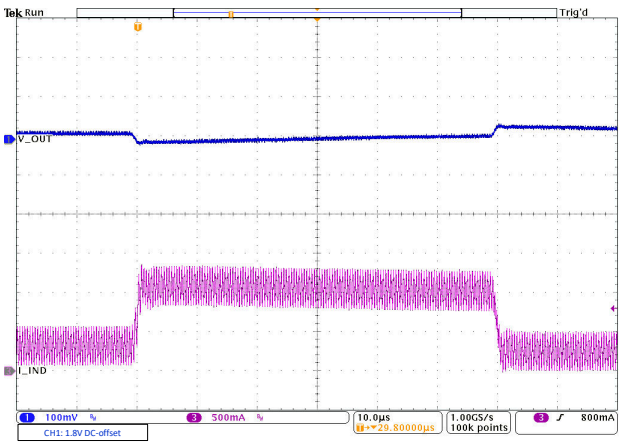

$I_{OUT}$ = 100mA

**Figure 9-11. Power Save Mode Operation**




$I_{OUT}$ = 1A

**Figure 9-12. Start-Up with Load**




Load step: 0.3A to 1A

**Figure 9-13. Load Transient**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## 9.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5V to 5.5V. Make sure that the input power supply has a sufficient current rating for the application.

## 9.4 Layout

### *9.4.1 Layout Guidelines*

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TPS62A02x-Q1 device.

- Place the input and output capacitors and the inductor as close as possible to the IC. This action keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- Connect the low side of the input and output capacitors properly to the GND pin to avoid a ground potential shift.
- The sense traces connected to FB is a signal trace. Special care must be taken to avoid noise being induced. Keep these traces away from SW nodes.
- Use a common ground. GND layers can be used for shielding.

See Figure 9-14 for the recommended PCB layout.

### *9.4.2 Layout Example*

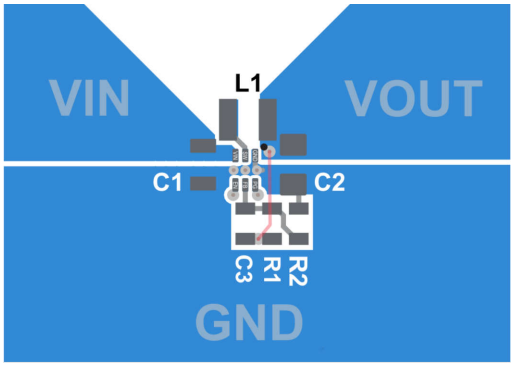


**Figure 9-14. TPS62A02x-Q1 PCB Layout Recommendation**

# 10 Device and Documentation Support

## 10.1 Device Support

### *10.1.1 Third-Party Products Disclaimer*

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## 10.2 Documentation Support

### *10.2.1 Related Documentation*

Texas Instruments, *Feedforward Capacitor to Improve Stability and Bandwidth With the TPS621-Family and TPS821-Family* application note

## 10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 11 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| April 2025 | * | Initial Release |

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS62A02AQDRLRQ1 | Active | Production | SOT-5X3 (DRL) \| 6 | 4000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1UZ |
| TPS62A02QDRLRQ1 | Active | Production | SOT-5X3 (DRL) \| 6 | 4000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1V1 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS62A02-Q1, TPS62A02A-Q1 :**

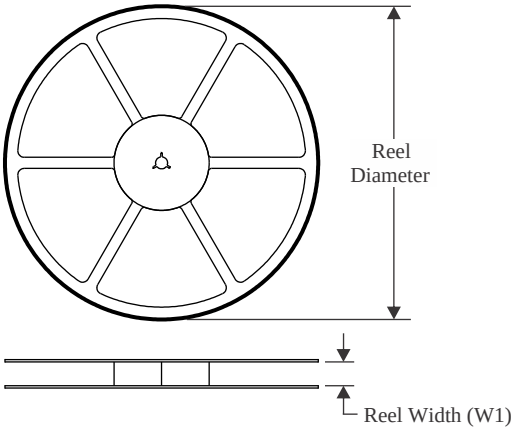
- Catalog : TPS62A02, TPS62A02A

NOTE: Qualified Version Definitions:

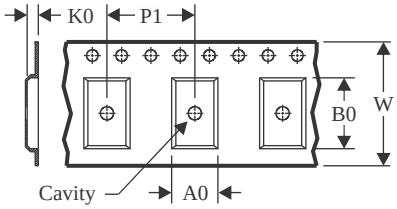
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

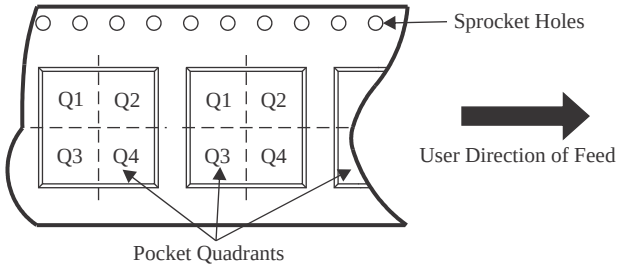



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

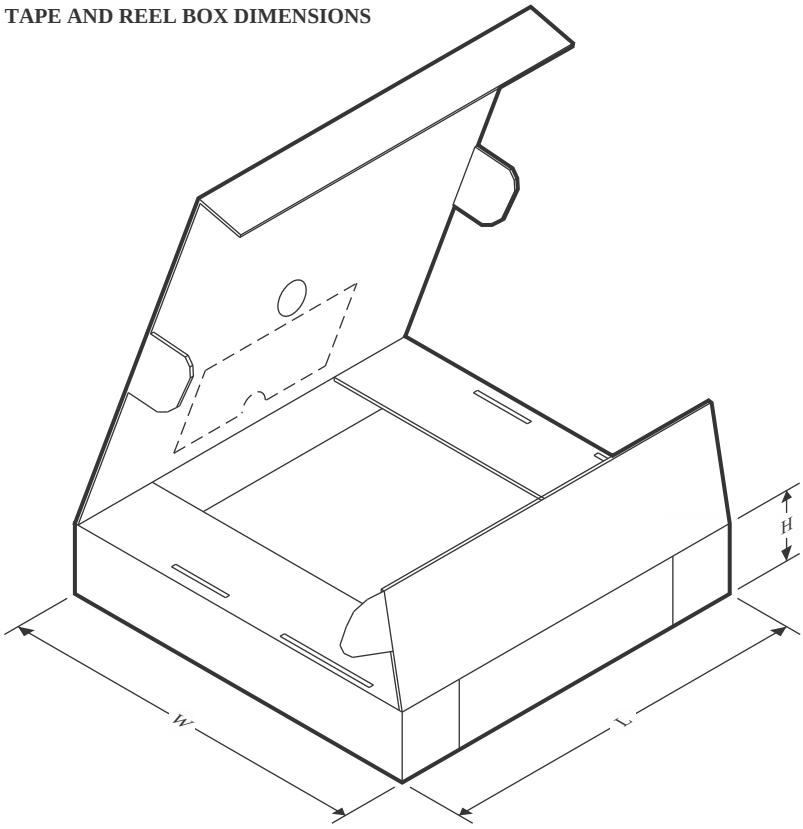
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS62A02AQDRLRQ1 | SOT-5X3 | DRL | 6 | 4000 | 180.0 | 8.4 | 2.0 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

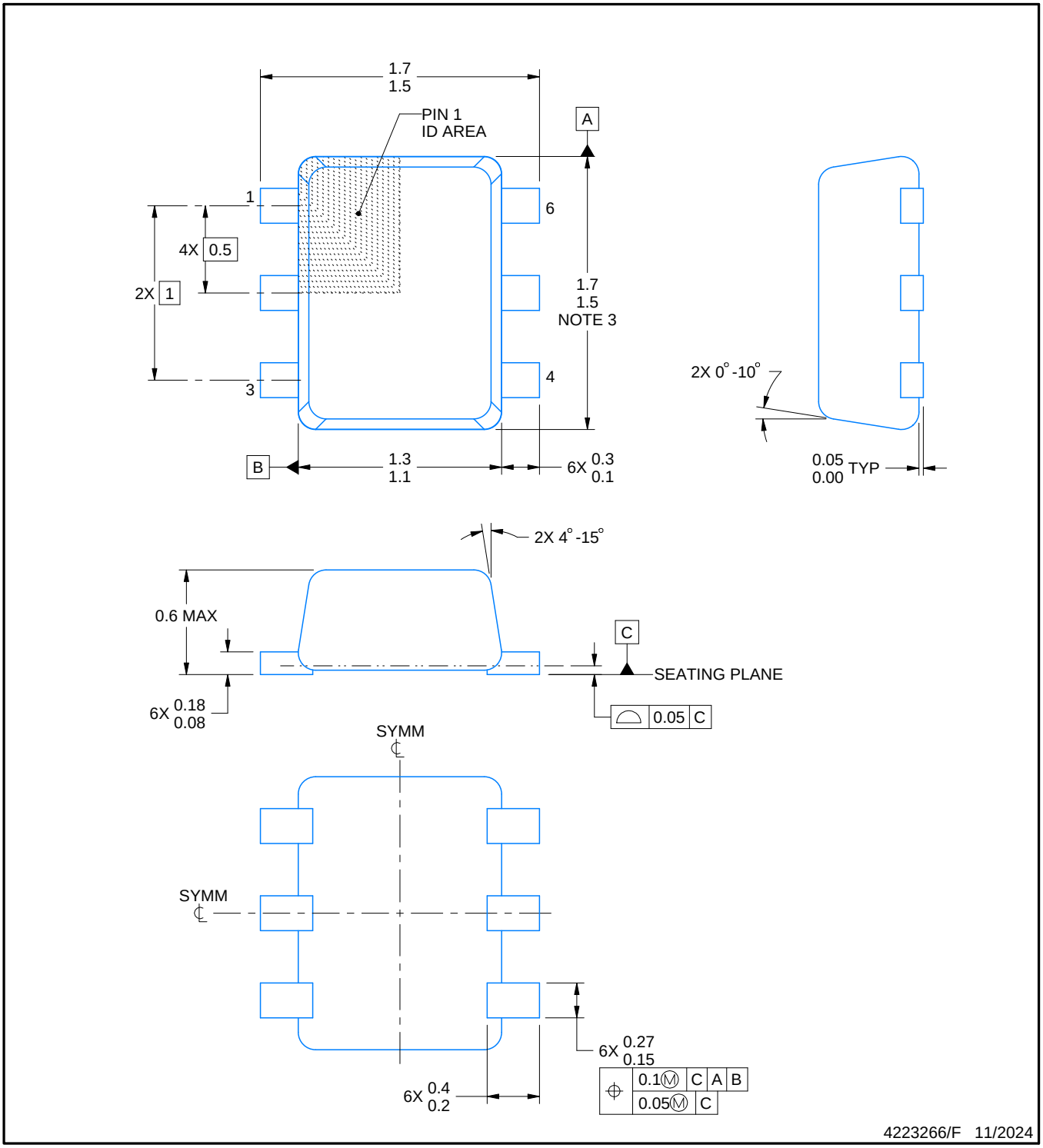
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS62A02AQDRLRQ1 | SOT-5X3 | DRL | 6 | 4000 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DRL0006A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




NOTES:

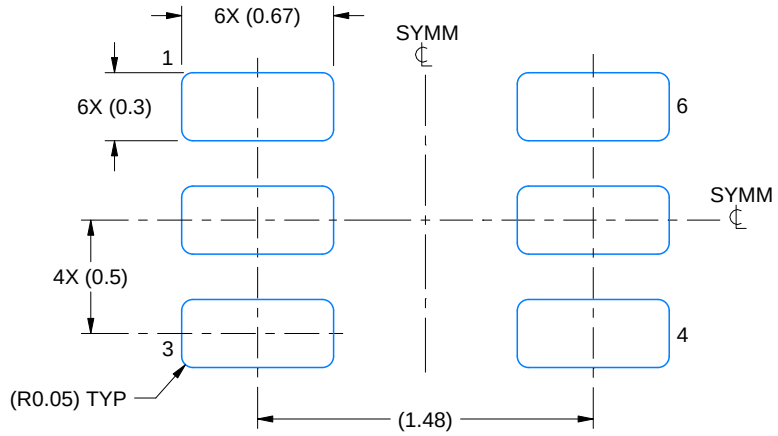
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

# EXAMPLE BOARD LAYOUT

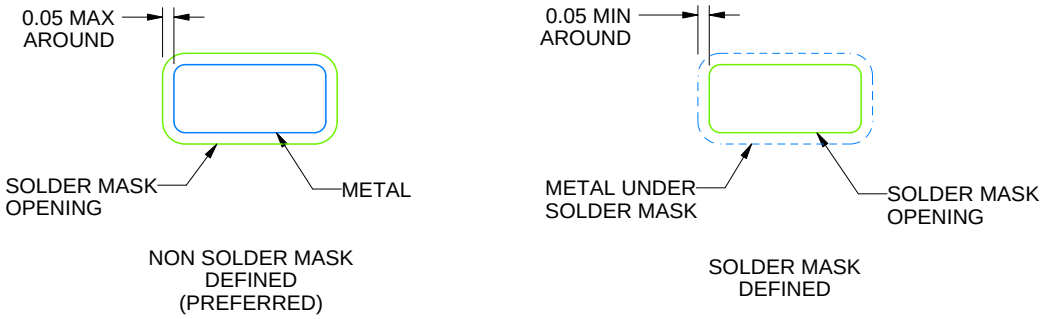
## DRL0006A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




LAND PATTERN EXAMPLE
SCALE:30X




SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

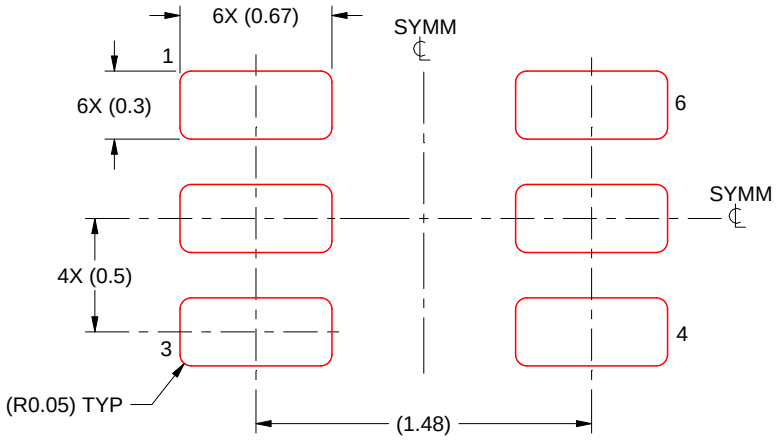
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

## DRL0006A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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