HIGH INPUT VOLTAGE BUCK-BOOST CONVERTER WITH 2A SWITCH CURRENT

Check for Samples: TPS63060-EP

FEATURES

- **Up to 93% Efficiency**
- **2A/1A Output Current at 5V in Buck Mode**
- **1.3A Output Current at 5V in Boost Mode (VIN>4V)**
- **Automatic Transition Between Step Down and Boost Mode**
- **Typical Device Quiescent Current less than 30µA**
- **Input Voltage Range: 2.5V to 12V**
- **Fixed and Adjustable Output Voltage Options from 2.5V to 8V**
- **Power Save Mode for Improved Efficiency at Low Output Power**
- **Forced Fixed Frequency Operation at 2.4MHz and Synchronization Possible**
- **Power Good Output**
- **Buck-Boost Overlap Control™**
- **Load Disconnect During Shutdown**
- **Overtemperature Protection**
- **Overvoltage Protection**
- **Available in a 3-mm × 3-mm, SON-10 Package**

APPLICATIONS

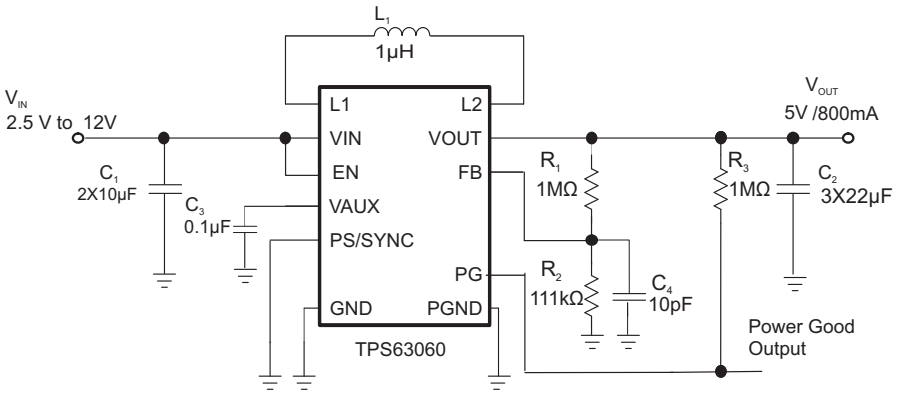
- **Dual LI-Ion Application**
- **DSC's and Camcorders**
- **Notebook Computer**
- **Industrial Metering Equipment**
- **Ultra Mobile PC's and Mobile Internet Devices**
- **Personal Medical Products**
- **High Power LED's**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C to 125°C) Temperature Range**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

DESCRIPTION

The TPS63060 provides a power supply solution for products powered by either three-cell up to six-cell alkaline, NiCd or NiMH battery, or a one-cell or dual-cell Li-Ion or Li-polymer battery. Output currents can go as high as 2A while using a dual-cell Li-Ion or Li-Polymer Battery, and discharge it down to 5V or lower. The buck-boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters Power Save mode to maintain high efficiency over a wide load current range. The Power Save mode can be disabled, forcing the converter to operate at a fixed switching frequency. The maximum average current in the switches is limited to a typical value of 2.25A. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery. The device is packaged in a 10-pin SON PowerPAD™ package measuring 3mm × 3mm (DSC).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_J	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	SON - DSC	TPS63060MDSCTEP	SLL	V62/14602-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage range	VIN, VOUT, PS/SYNC, EN, FB	–0.3	17	V
	L1, L2	-0.3	V_{IN}+0.3	V
	FB, V_{AUX}	-0.3	7.5	V
Operating virtual junction temperature range, T_J		–55	150	°C
Storage temperature range T_{stg}		-65	150	°C
ESD rating(2)	Human Body Model - (HBM)		3	kV
	Machine Model - (MM)		200	V
	Charge Device Model - (CDM)		1	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS63060-EP DSC 10 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	48.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	54.8	
θ_{JB}	Junction-to-board thermal resistance(4)	19.8	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.1	
ψ_{JB}	Junction-to-board characterization parameter(6)	19.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	4.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

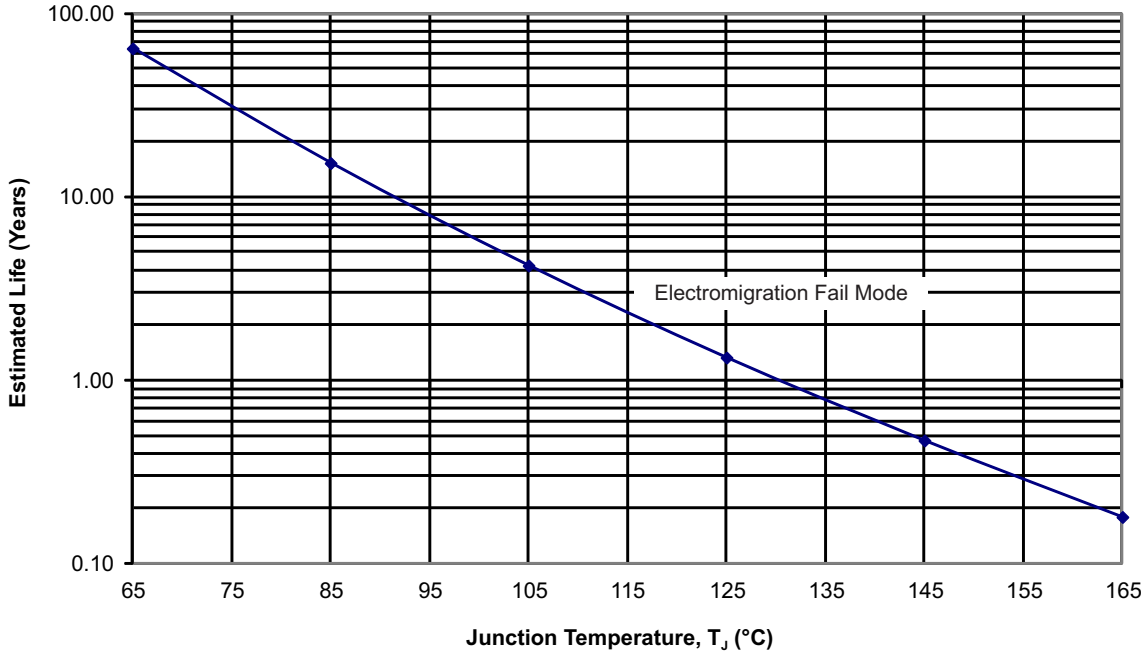
RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage at VIN	2.5		12	V
Output Current I_{out} with V_{IN} = 10V to 12V			1	A
Operating junction temperature range, T_J	–55		125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE							
V_{IN}	Input voltage range			2.5		12	V
V_{IIN}	Minimum input voltage for startup					2.5	V
V_{OUT}	Output voltage range			2.5		8	V
	Minimum duty cycle in step down conversion				10	20	%
V_{FB}	Feedback voltage		PS/SYNC = V_{IN}	495	500	505	mV
V_{FB}	Feedback voltage		PS/SYNC = GND Referenced to 500mV	0.6		6	%
f	Oscillator frequency			1850	2400	3000	kHz
	Frequency range for synchronization			2200	2400	2600	kHz
I_{SW}	Average inductance current limit		V_{IN} = 5V, T_J = 25°C	2000	2250	2500	mA
	High side switch on resistance		V_{IN} = 5V		90		mΩ
	Low side switch on resistance		V_{IN} = 5V		95		mΩ
	Line regulation		Power Save Mode disabled		0.5		%
	Load regulation		Power Save Mode disabled		0.5		%
I_q	Quiescent current	VIN	I_O = 0 mA, V_{EN} = V_{IN} = 5V, V_{OUT} = 5V		30	64	µA
		VOUT			7	28	µA
I_S	Shutdown current		V_{EN} = 0 V, V_{IN} = 5V		0.3	2	µA
CONTROL STAGE							
V_{AUX}	Maximum bias voltage		V_{IN} > V_{OUT}	V_{IN}		7	V
			V_{IN} < V_{OUT}	V_{OUT}		7	V
I_{AUX}	Load current at V_{AUX}					1	mA
UVLO	Under voltage lockout threshold		V_{IN} voltage decreasing	1.8	1.9	2.2	V
	UVLO hysteresis				300		mV
V_{IL}	EN, PS/SYNC input low voltage					0.4	V
V_{IH}	EN, PS/SYNC input high voltage			1.2			V
	EN, PS/SYNC input current		Clamped on GND or V_{IN}		0.01	0.2	µA
	PG output low voltage		V_{OUT} = 5V, I_{PGL} = 10 µA		0.04	0.4	V
	PG output leakage current				0.01	0.1	µA
	Output overvoltage protection			12		16	V
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

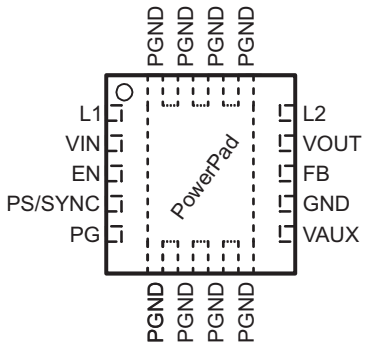
(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) Enhanced plastic product disclaimer applies.

Figure 1. TPS63060-EP Operating Life Derating Chart

PIN ASSIGNMENTS

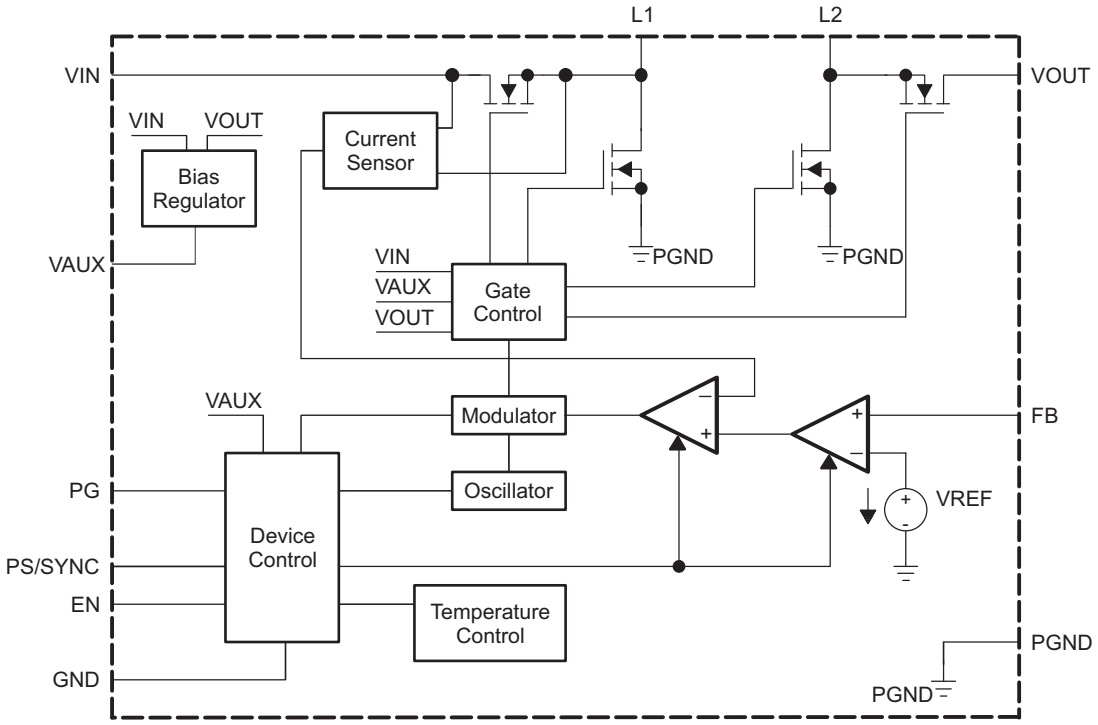
DSC PACKAGE
(TOP VIEW)



Pin Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
EN	3	I	Enable input. (1 enabled, 0 disabled)
FB	8	I	Voltage feedback of adjustable versions, must be connected to VOUT on fixed output voltage versions
GND	7		Control / logic ground
L1	1	I	Connection for Inductor
L2	10	I	Connection for Inductor
PS/SYNC	4	I	Enable / disable power save mode (1 disabled, 0 enabled, clock signal for synchronization)
PG	5	O	Output power good (1 good, 0 failure; open drain)
PGND	PowerPAD™		Power ground
VIN	2	I	Supply voltage for power stage
VOUT	9	O	Buck-boost converter output
VAUX	6		Connection for Capacitor
PowerPAD™			Must be soldered to achieve appropriate power dissipation. Must be connected to PGND.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

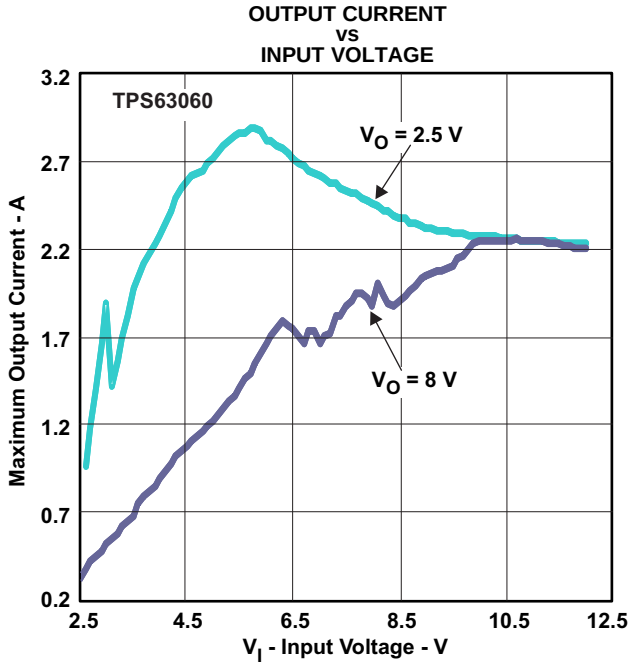


Figure 2.

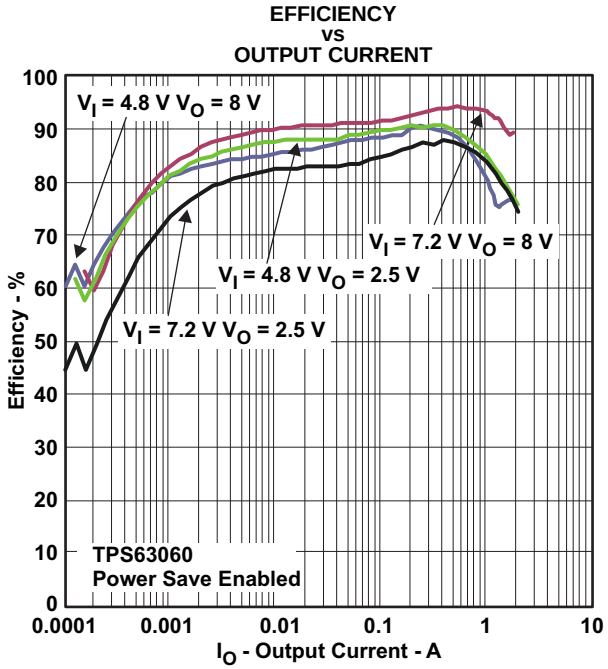


Figure 3.

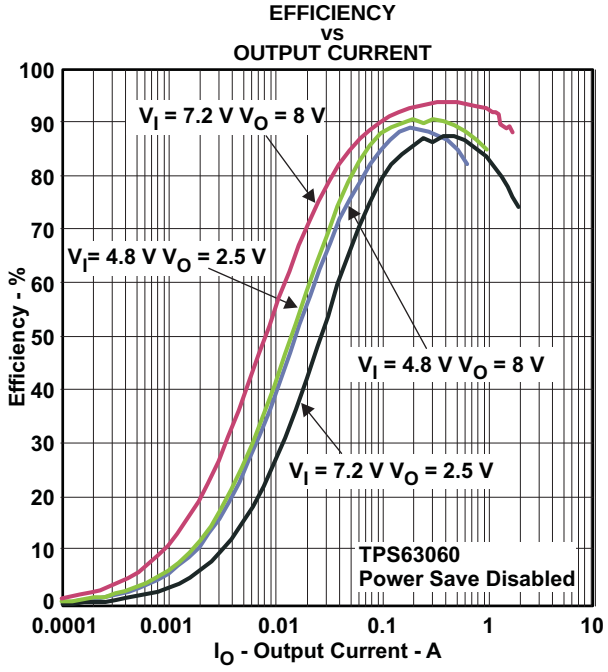


Figure 4.

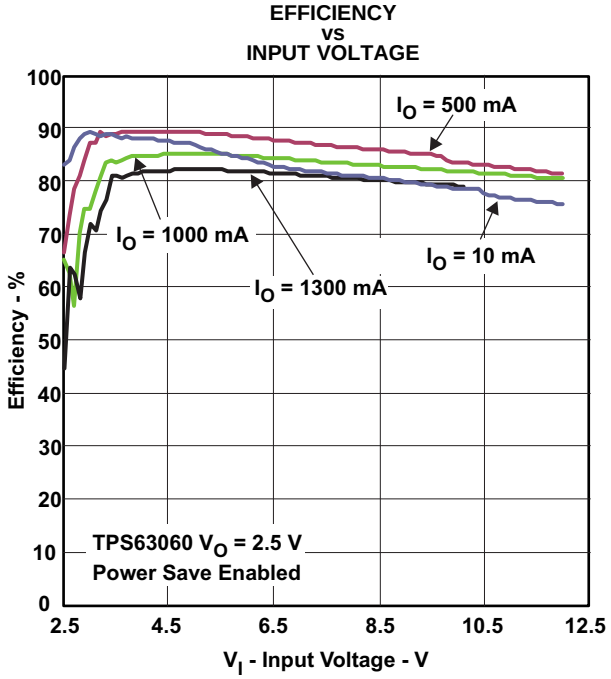


Figure 5.

TYPICAL CHARACTERISTICS (continued)

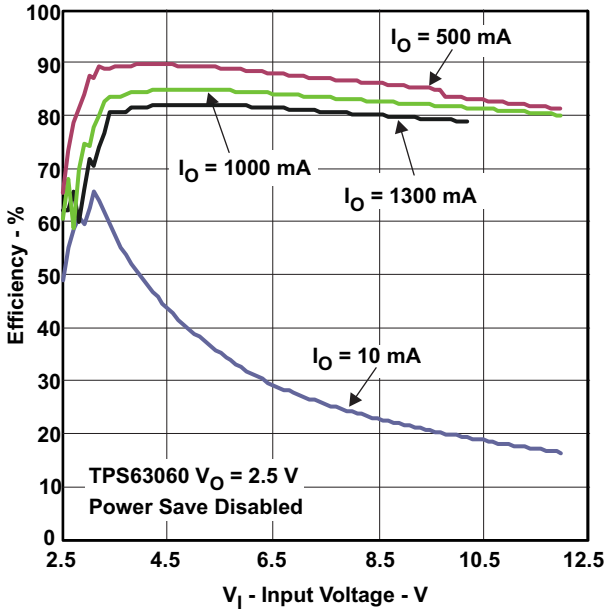


Figure 6.

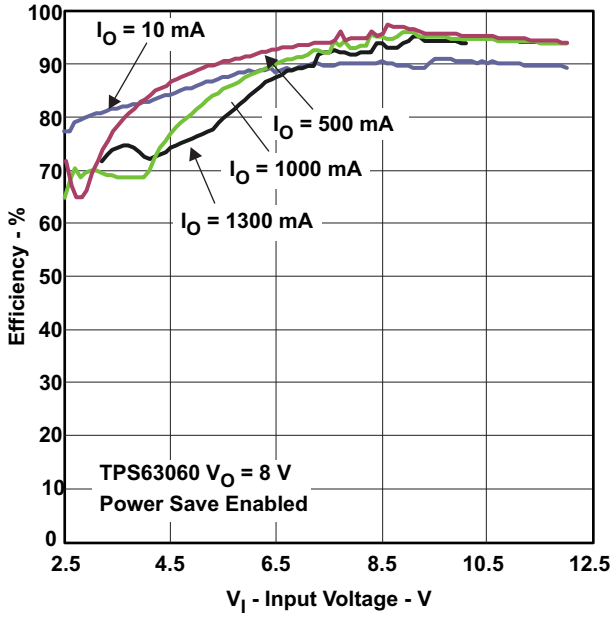


Figure 7.

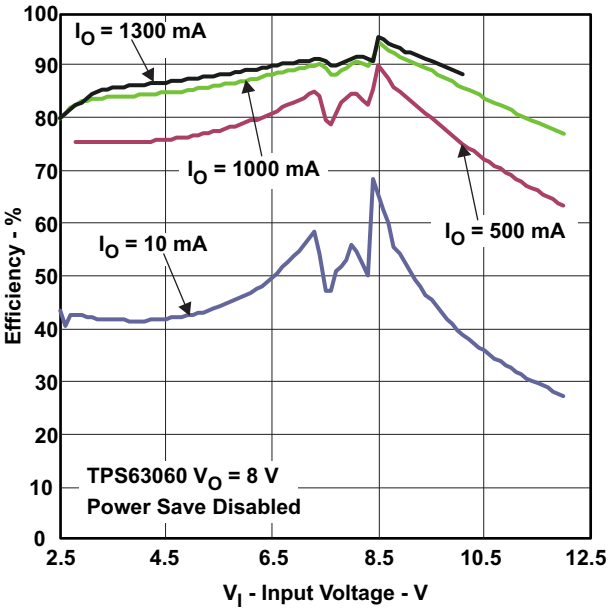


Figure 8.

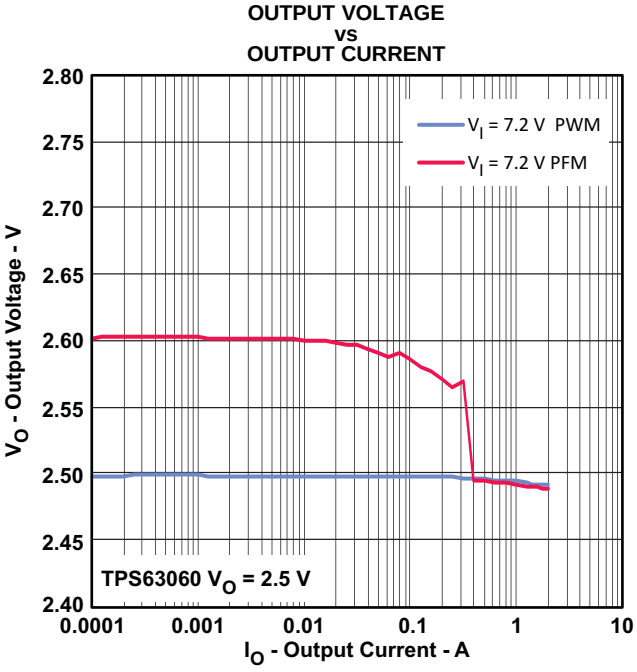


Figure 9.

TYPICAL CHARACTERISTICS (continued)

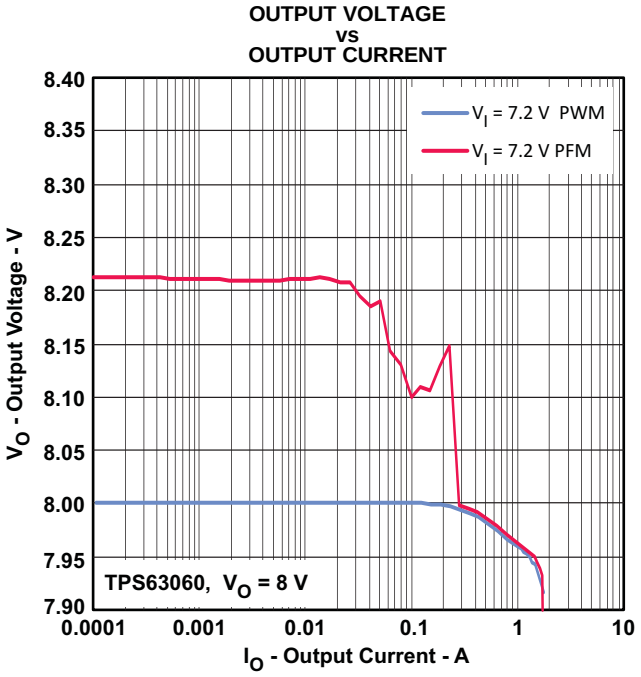


Figure 10.

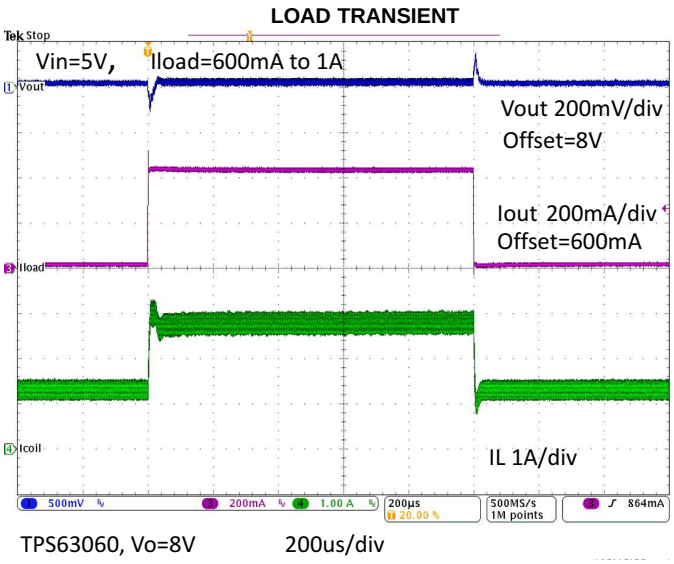


Figure 11.

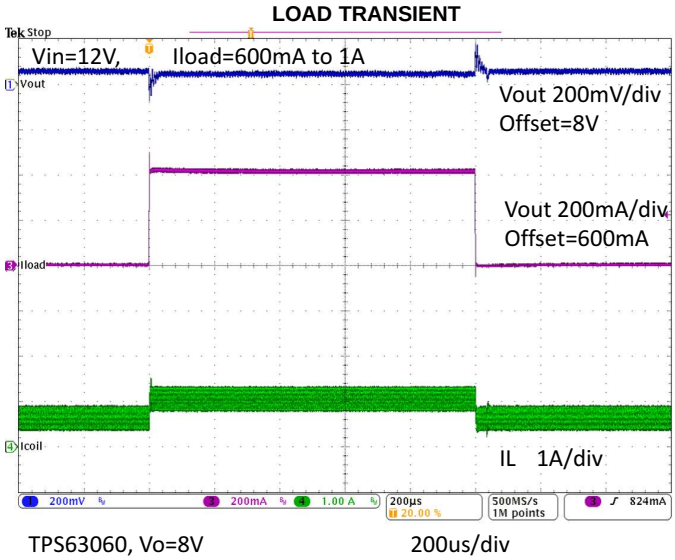


Figure 12.

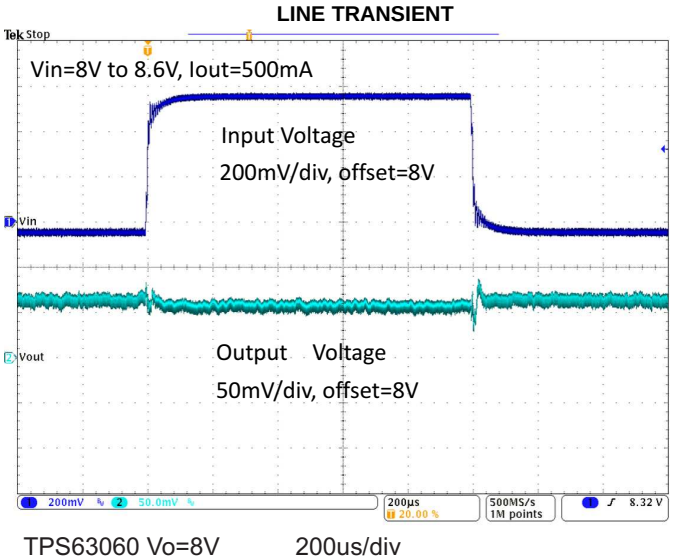
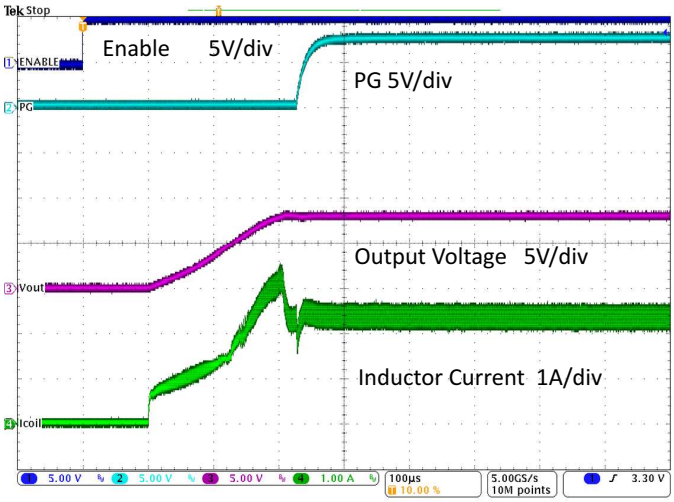


Figure 13.

TYPICAL CHARACTERISTICS (continued)

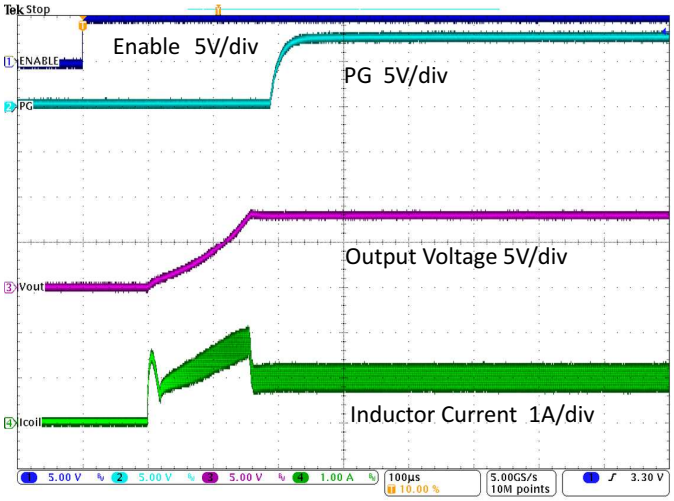
STARTUP AFTER ENABLE



TPS63060, Vo=8V 100us/div Vin=5V, Io=1A

Figure 14.

STARTUP AFTER ENABLE



TPS63060, Vo=8V 100us/div Vin=12V Io=1A

Figure 15.

Shutdown Current versus Input Voltage

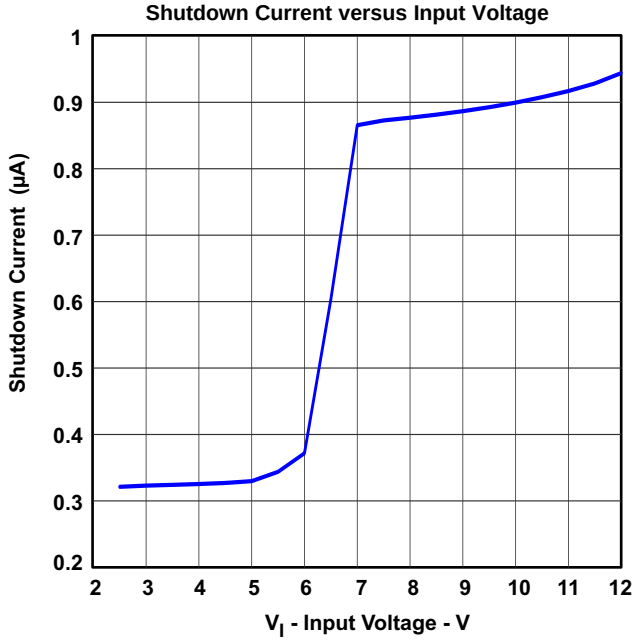


Figure 16.

Quiescent Current versus Input Voltage

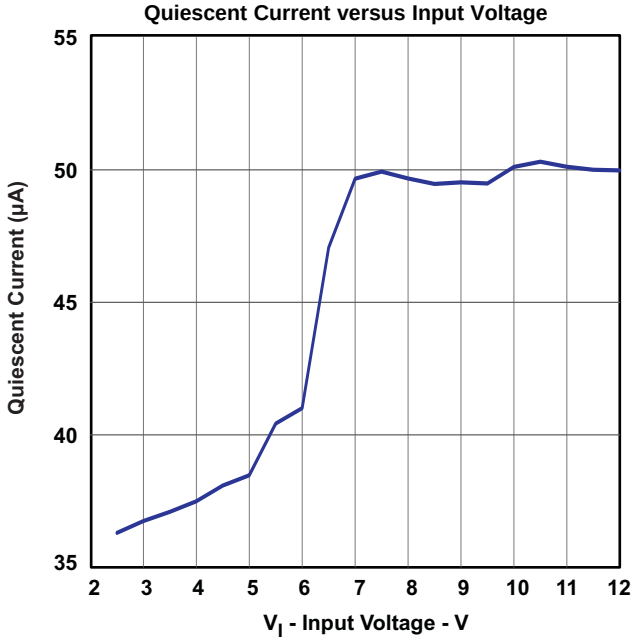


Figure 17.

PARAMETER MEASUREMENT INFORMATION

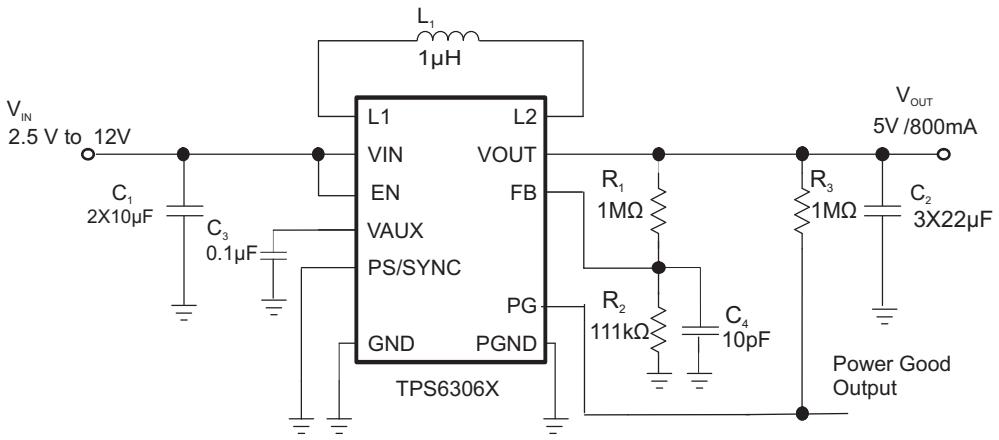


Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS63060	Texas Instruments
L1	1µH, 3 mm x 3 mm x 1.5 mm	Coilcraft , XFL4020-102
C1	2 x 10 µF 16V, 0805, X5R ceramic	Taiyo Yuden, EMK212BJ
C2	3 × 22 µF 16V, 0805, X5R ceramic	Taiyo Yuden, LMK212BJ
C3	0.1 µF, X5R ceramic	
C4	10pF, ceramic	
R1, R2	Depending on the output voltage: R1=0, C4 and R2 n.a.	

DETAILED DESCRIPTION

The controller circuit of the device is based on an average current mode topology. The controller also uses input and output voltage feedforward. Changes of input and output voltage are monitored and immediately can change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. At adjustable output voltages, a resistive voltage divider must be connected to that pin. At fixed output voltages, FB must be connected to the output voltage to directly sense the voltage. Fixed output voltage versions use a trimmed internal resistive divider. The feedback voltage will be compared with the internal reference voltage to generate a stable and accurate output voltage.

The device uses 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range. To avoid ground shift problems due to the high currents in the switches, two separate ground pins GND and PGND are used. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point, ideally, close to the GND pin. Due to the 4-switch topology, the load is always disconnected from the input during shutdown of the converter. To protect the device from overheating an internal temperature sensor is implemented.

Buck-Boost Operation

To regulate the output voltage at all possible input voltage conditions, the device automatically switches from buck operation to boost operation and back as required. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a step down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are permanently switching. Controlling the switches this way allows the converter to maintain high efficiency at the most important point of operation, when the input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses.

Control Loop Description

The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. Figure 18 shows the control loop.

The non inverting input of the transconductance amplifier Gmc can be assumed to be constant. The output of Gmv defines the average inductor current. The current through resistor RS, which represents the actual inductor current, is compared to the desired value and the difference, or current error, is amplified and compared to the sawtooth ramp of either the Buck or the Boost.

The Buck-Boost Overlap Control™ makes sure that the classical buck-boost function, which would cause two switches to be on every half a cycle, is avoided. Thanks to this block whenever all switches becomes active during one clock cycle, the two ramps are shifted away from each other. However, when there is no switching activities because there is a gap between the ramps, the ramps are moved closer together. As a result the number of classical buck-boost cycles or no switching is reduced to a minimum and high efficiency values are achieved.

Slope compensation is not required to avoid subharmonic oscillation which are otherwise observed when working with peak current mode control with D>0.5.

Nevertheless the amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input. This purpose is reached limiting the gain of the current amplifier.

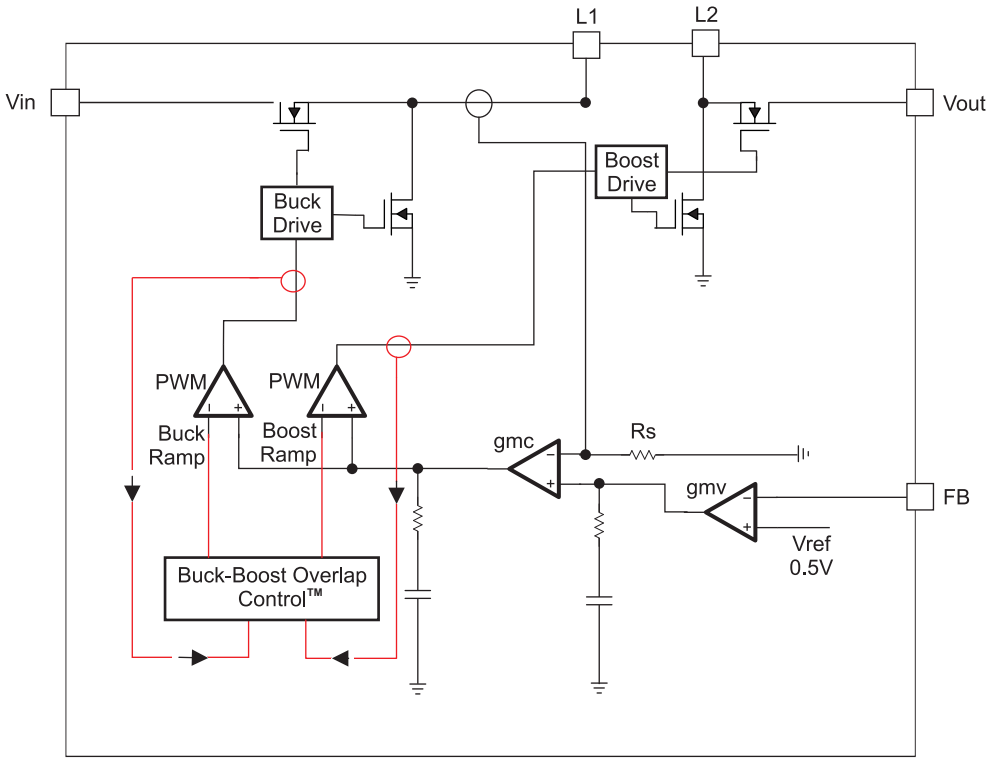


Figure 18. Average Current Mode Control

Power-save mode and synchronization

The PS/SYNC pin can be used to select different operation modes. Power Save Mode is used to improve efficiency at light load. To enable Power-Save, PS/SYNC must be set low. If PS/SYNC is set low then Power Save Mode is entered when the average inductor current gets lower then about 100mA. At this point the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency.

During the Power Save Mode, the output voltage is monitored with a comparator by the threshold comp low and comp high. When the device enters Power Save Mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the value of output capacitance. As the output voltage falls below the comp low threshold set to 2.5% typical above Vout, the device ramps up the output voltage again, by starting operation using a programmed average inductor current higher than required by the current load condition. Operation can last for one or several pulses. The converter continues these pulses until the comp high threshold, set to typically 3.5% above Vout nominal, is reached and the average inductor current gets lower than about 100mA. When the load increases above the minimum forced inductor current of about 100mA, the device will automatically switch to PWM mode.

The Power Save Mode can be disabled by programming the PS/SYNC high. Connecting a clock signal at PS/SYNC forces the device to synchronize to the connected clock frequency.

Synchronization is done by a PLL to lower and higher frequencies compared to the internal clock. The PLL can also tolerate missing clock pulses without the converter malfunctioning. The PS/SYNC input supports standard logic thresholds.

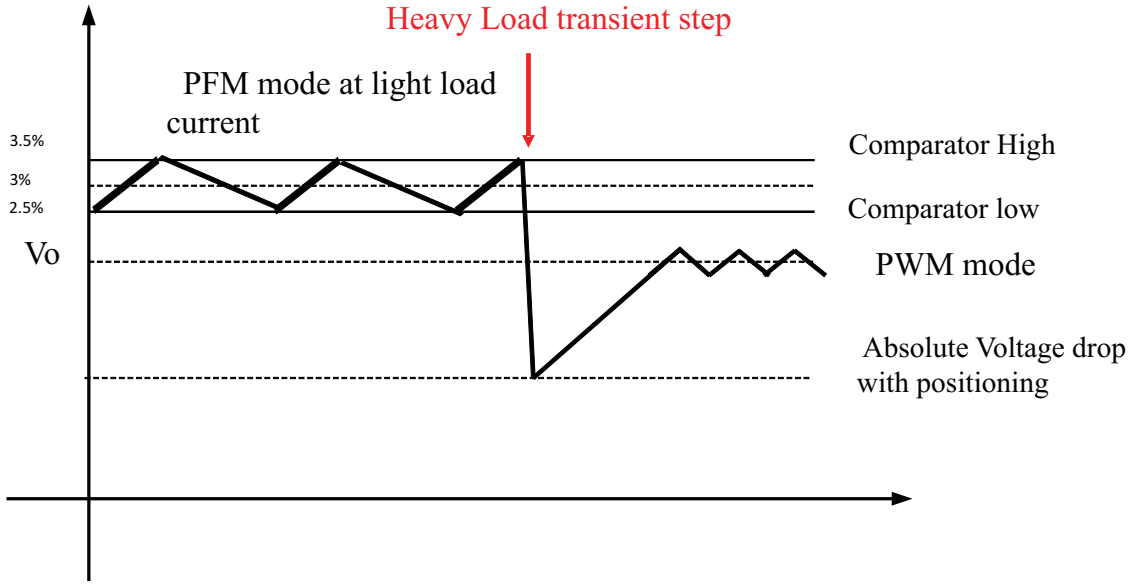


Figure 19. Power-Save Mode Thresholds and Dynamic Voltage Positioning

Dynamic voltage positioning

As detailed in Figure 19, the output voltage is typically 3% above the nominal output voltage at light load currents, as the device is in Power Save Mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. This allows the converter to operate with a small output capacitor and still have a low absolute voltage drop during heavy load transient changes. See Figure 19 for detailed operation of the Power Save Mode

Dynamic Current limit

In order to keep the output voltage regulated when the power source becomes weaker the device has implemented a dynamic current limit function. The maximum current allowed through the switch depends on the voltage applied at the input terminal of the TPS6306X. The curve in Figure 20 shows this dependency, and the I_{SW} versus V_{IN}. The dynamic current limit has its lowest value when reaching the minimum recommended supply voltage at V_{IN}.

Given the I_{SW} value from Figure 20, is then possible to calculate the output current reached in boost mode using Equation 1 and Equation 2 and in buck mode using Equation 3 and Equation 4.

Duty Cycle Boost $$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (1)$$

Maximum Output Current Boost $$I_{OUT} = \eta \times I_{SW} \times (1 - D) \quad (2)$$

Duty Cycle Buck $$D = \frac{V_{OUT}}{V_{IN}} \quad (3)$$

Maximum Output Current Buck $$I_{OUT} = I_{SW} \quad (4)$$

With,

η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as an assumption)
f = Converter switching frequency (typical 2.4 MHz)
L = Selected inductor value

If the die temperature increases above the recommended maximum temperature, the dynamic current limit becomes active. The current limit is reduced with temperature increasing.

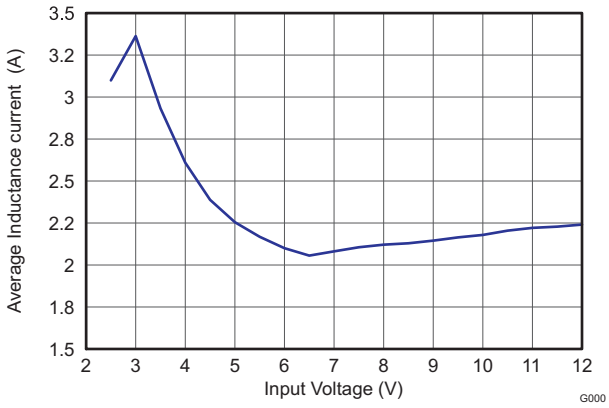


Figure 20. Average Inductance Current versus Input Voltage

Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents flowing from the input.

Power Good

The device has a built in power good function to indicate whether the output voltage is regulated properly. As soon as the average inductor current gets limited to a value below the current the voltage regulator demands for maintaining the output voltage the power good output gets low impedance. The output is open drain, so its logic function can be adjusted to any voltage level the connected logic is using, by connecting a pull up resistor to the supply voltage of the logic. By monitoring the status of the current control loop, the power good output provides the earliest indication possible for an output voltage break down and leaves the connected application a maximum time to safely react.

Softstart and Short Circuit Protection

After being enabled, the device starts operating. The average current limit ramps up from an initial 400mA following the output voltage increasing. At an output voltage of about 1.2V, the current limit is at its nominal value. If the output voltage does not increase, the current limit will not increase. There is no timer implemented. Thus, the output voltage overshoot at startup, as well as the inrush current, is kept at a minimum. The device ramps up the output voltage in a controlled manner even if a large capacitor is connected at the output. When the output voltage does not increase above 1.2V, the device assumes a short circuit at the output, and keeps the current limit low to protect itself and the application. At a short on the output during operation, the current limit is also kept under 2A typically (minimum average inductance current).

Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage will not work anymore. Therefore, overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. The implemented overvoltage protection circuit monitors the output voltage internally as well. If it reaches the overvoltage threshold, the voltage amplifier regulates the output voltage to this value.

Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VIN is lower than approximately its threshold (see the *Electrical Characteristics* table). When in operation, the device automatically enters the shutdown mode if the voltage on VIN drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see the Electrical Characteristics table) the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

APPLICATION INFORMATION

DESIGN PROCEDURE

The TPS6306x series of buck-boost converter has internal loop compensation. Therefore, the external L-C filter has to be selected to work with the internal compensation. When selecting the output filter a low limit for the inductor value exists to avoid subharmonic oscillation which could be caused by a far too fast ramp up of the amplified inductor current. For the TPS6306x series, the minimum inductor value should be kept at 1µH. Selecting a larger output capacitor value is less critical because the corner frequency moves to lower frequencies. To simplify this process, Table 2 outlines possible inductor and capacitor value combinations.

Table 2. Output Filter Selection (Average Inductance current up to 2A)

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)		
	44	66	100
1.0	√	√(3)	√
1.5	√	√	√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) Typical application. Other check mark indicates recommended filter combinations

Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, with the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. Equation 1 and Equation 5 show how to calculate the peak current I_{PEAK}. Only the equation which defines the switch current in boost mode is reported because this is providing the highest value of current and represents the critical current value for selecting the right inductor.

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \quad (5)$$

With,

D =Duty Cycle in Boost mode
f = Converter switching frequency (typical 2.4 MHz)
L = Selected inductor value
η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as an assumption)

Note: The calculation must be done for the minimum input voltage which is possible to have in boost mode

Consideration must be given to the load transients and error conditions that can cause higher inductor currents. This must be taken into consideration when selecting an appropriate inductor. See Table 3 for typical inductors.

The size of the inductor can also affect the stability of the feedback loop. In particular the boost transfer function exhibits a right half-plane zero, whose frequency is inverse proportional to the inductor value and the load current. This means higher is the value of inductance and load current more possibilities has the right half plane zero to be moved at lower frequency. This could degrade the phase margin of the feedback loop. It is recommended to choose the inductor's value in order to have the frequency of the right half plane zero >400kHz. The frequency of the RHPZ can be calculated using Equation 6.

$$f_{RHPZ} = \frac{(1 - D)^2 \times Vout}{2\pi \times Iout \times L} \quad (6)$$

With,

D =Duty Cycle in Boost mode

Note: The calculation must be done for the minimum input voltage which is possible to have in boost mode

Table 3. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPLIER	SIZE (LxWxH mm)	Isat/DCR
1 µH	Coilcraft XFL4020-102	4 x 4 x 2.1	5.1A/10.8 mΩ
1 µH	TOKO DEM2815 1226AS-H-1R0N	3 x 3.2 x 1.5	2.7A/27 mΩ
1.5µH	Coilcraft XFL4020-152	4 x 4 x 2.1	4.4A/ 14.40mΩ

Capacitor selection

Input Capacitor

At least a 20µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended.

Output Capacitor

For the output capacitor, use of a small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC is recommended. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the VOUT and PGND pins of the IC. The recommended typical output capacitor value is 66µF with a variance as outlined in Table 2.

There is also no upper limit for the output capacitance value. Larger capacitors will cause lower output voltage ripple as well as lower output voltage drop during load transients.

When choosing input and output capacitors, it needs to be kept in mind, that the value of capacitance experiences significant losses from their rated value depending on the operating temperature and the operating DC voltage. It's not uncommon for a small surface mount ceramic capacitor to lose 50% and more of it's rated capacitance. For this reason, it is important to use a larger value of capacitance or a capacitor with higher voltage rating in order to ensure the required capacitance at the full operating voltage.

Bypass Capacitor

To make sure that the internal control circuits are supplied with a stable low noise supply voltage, a capacitor is connected between VAUX and GND. Using a ceramic capacitor with a value of 0.1µF is recommended. The capacitor needs to be placed close to the VAUX pin. The value of this capacitor should not be higher than 0.22µF.

Setting the Output Voltage

When the adjustable output voltage version TPS63060 is used, the output voltage is set by the external resistor divider. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500mV. The maximum recommended value for the output voltage is 8V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01µA, and the voltage across the resistor between FB and GND, R_2, is typically 500 mV. Based on these two values, the recommended value for R2 should be lower than 500kΩ, in order to set the divider current at 3µA or higher. It is recommended to keep the value for this resistor in the range of 200kΩ. From that, the value of the resistor connected between VOUT and FB, R1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 7:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (7)$$

A small capacitor C4=10pF, in parallel with R2 needs to be placed when using the Power Save Mode and the adjustable version, to provide filtering and improve the efficiency at light load.

LAYOUT CONSIDERATIONS

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, short traces are recommended as well, separation from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the PowerPAD™
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table please check the Thermal Characteristics Application Note (SZZA017) and the IC Package Thermal Metrics Application Note (SPRA953).

TYPICAL APPLICATION

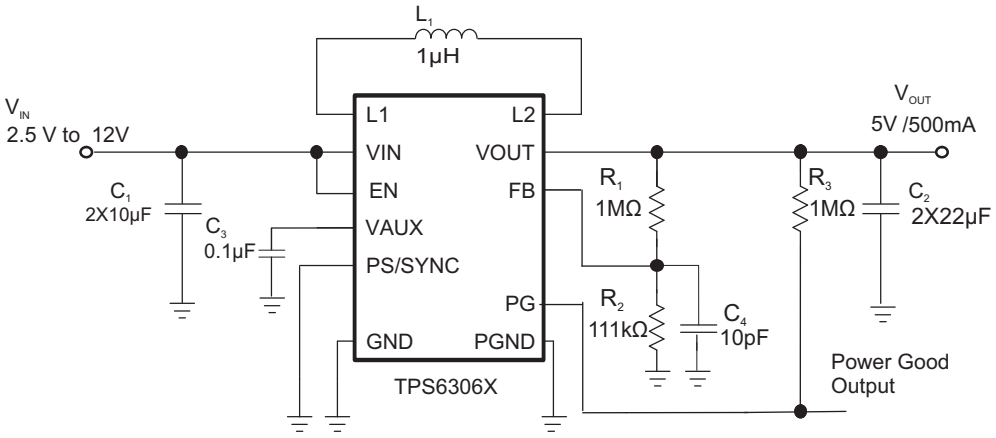


Figure 21. 5V and 500mA from 1 or 2 cell Li-Ion

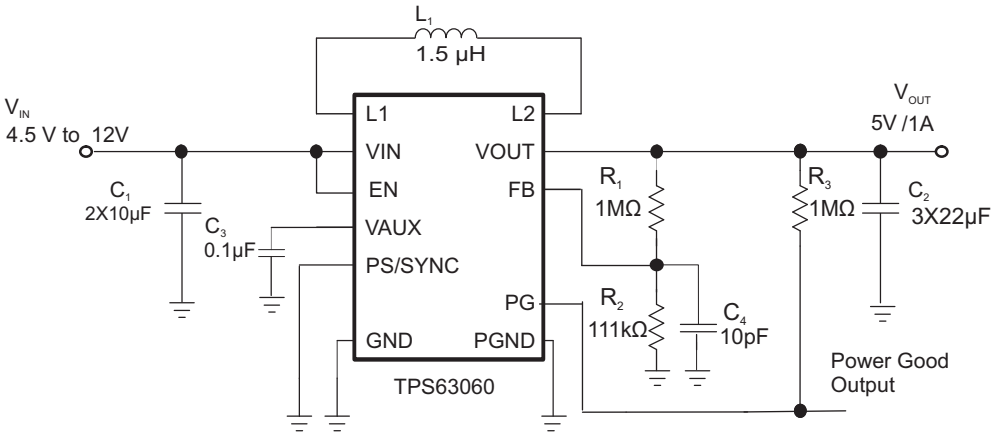


Figure 22. 5V and 1A from Input Voltage up to 12V

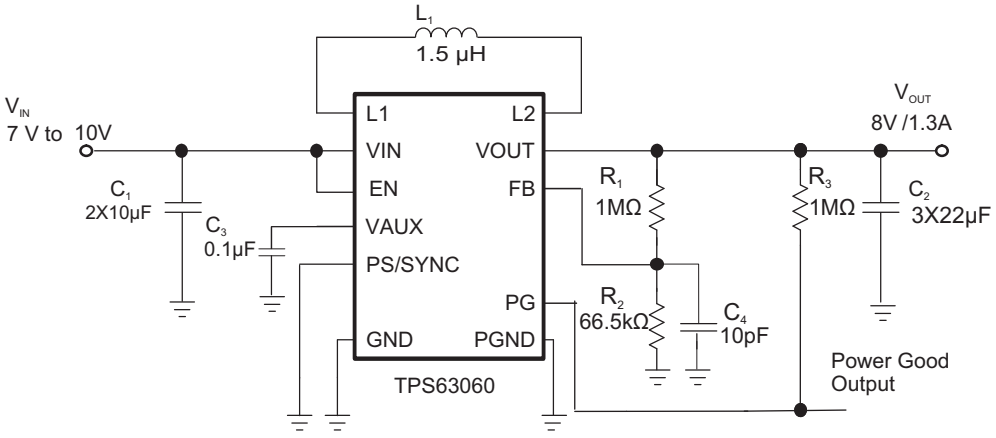


Figure 23. 8V and 1.3A from 2 cell Li-Ion

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS63060MDSCTEP	Active	Production	WSON (DSC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	SLL
V62/14602-01XE	Active	Production	WSON (DSC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	SLL

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS63060-EP :

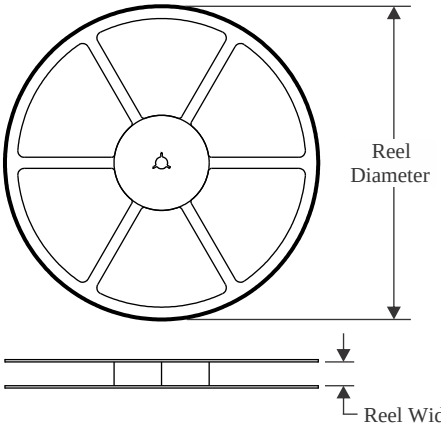
- Catalog : TPS63060

NOTE: Qualified Version Definitions:

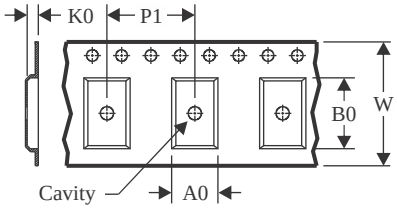
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

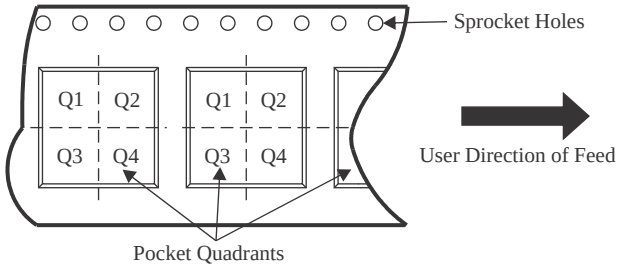


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

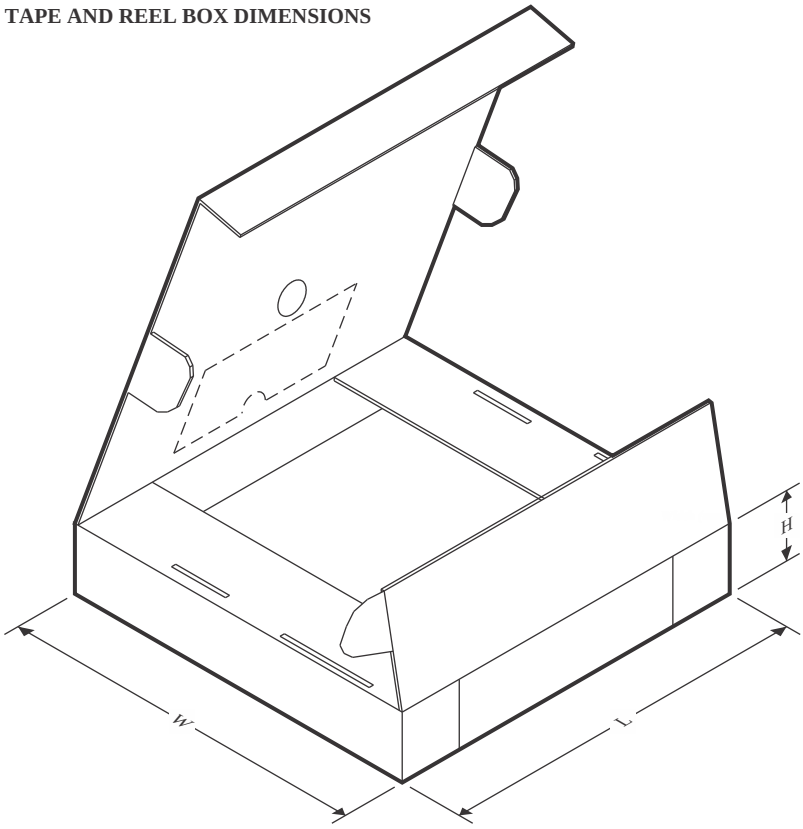
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63060MDSCTEP	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



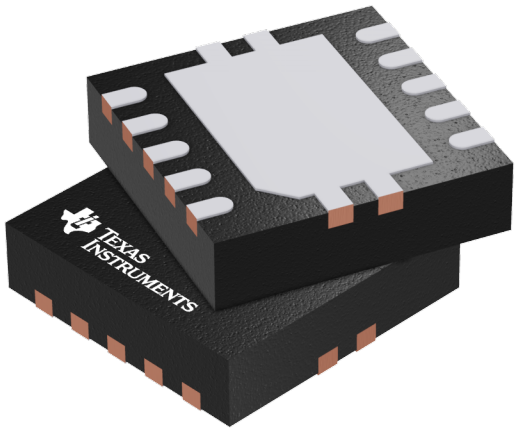
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63060MDSCTEP	WSON	DSC	10	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

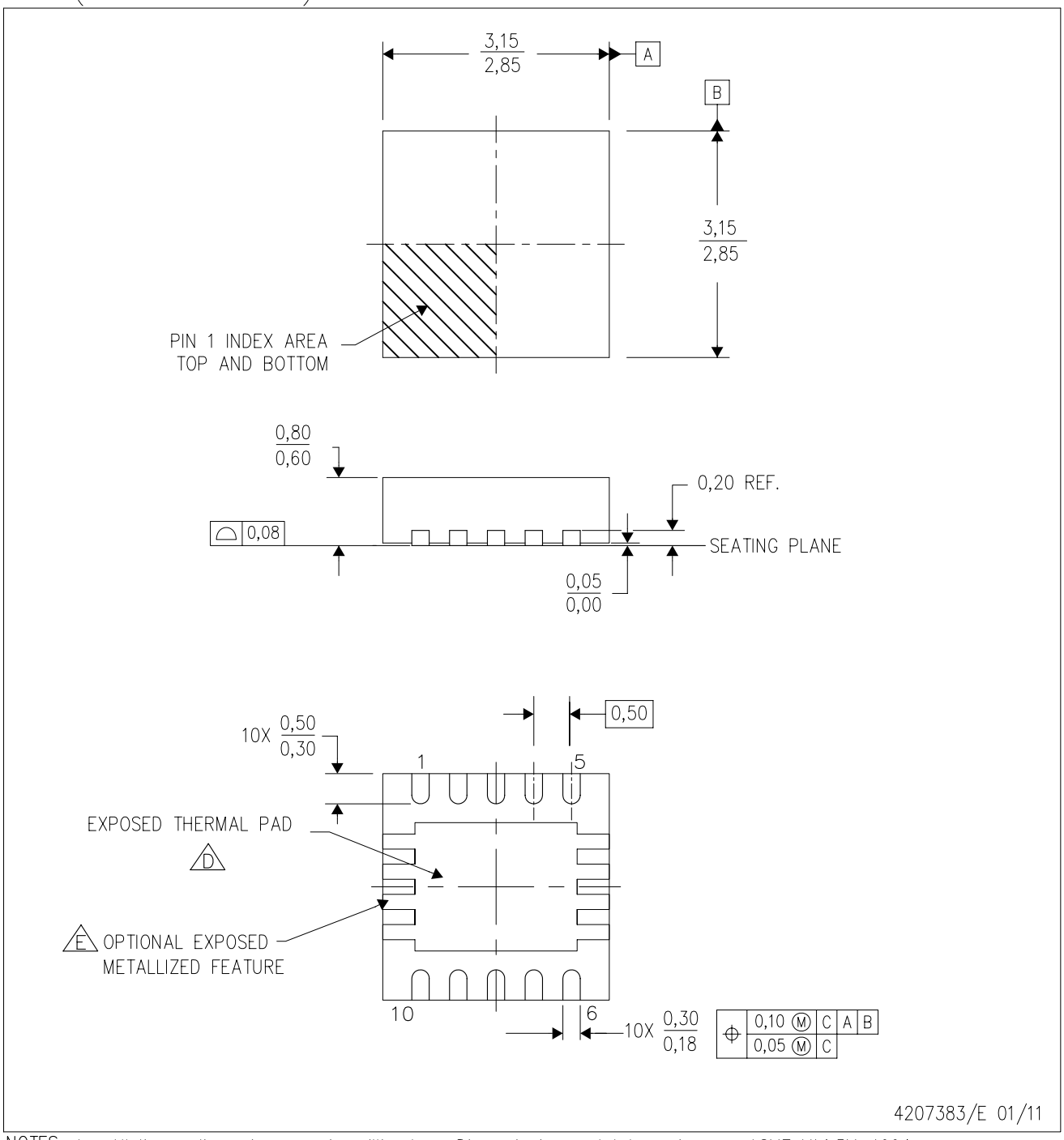
DSC 10 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

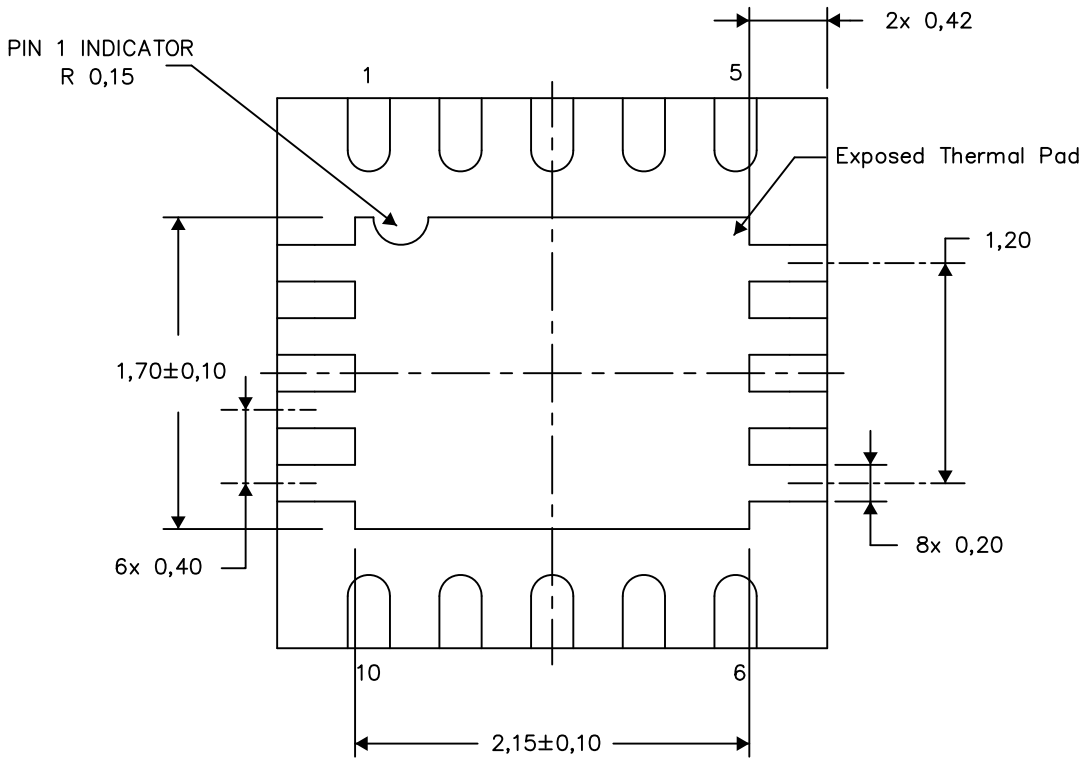
DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



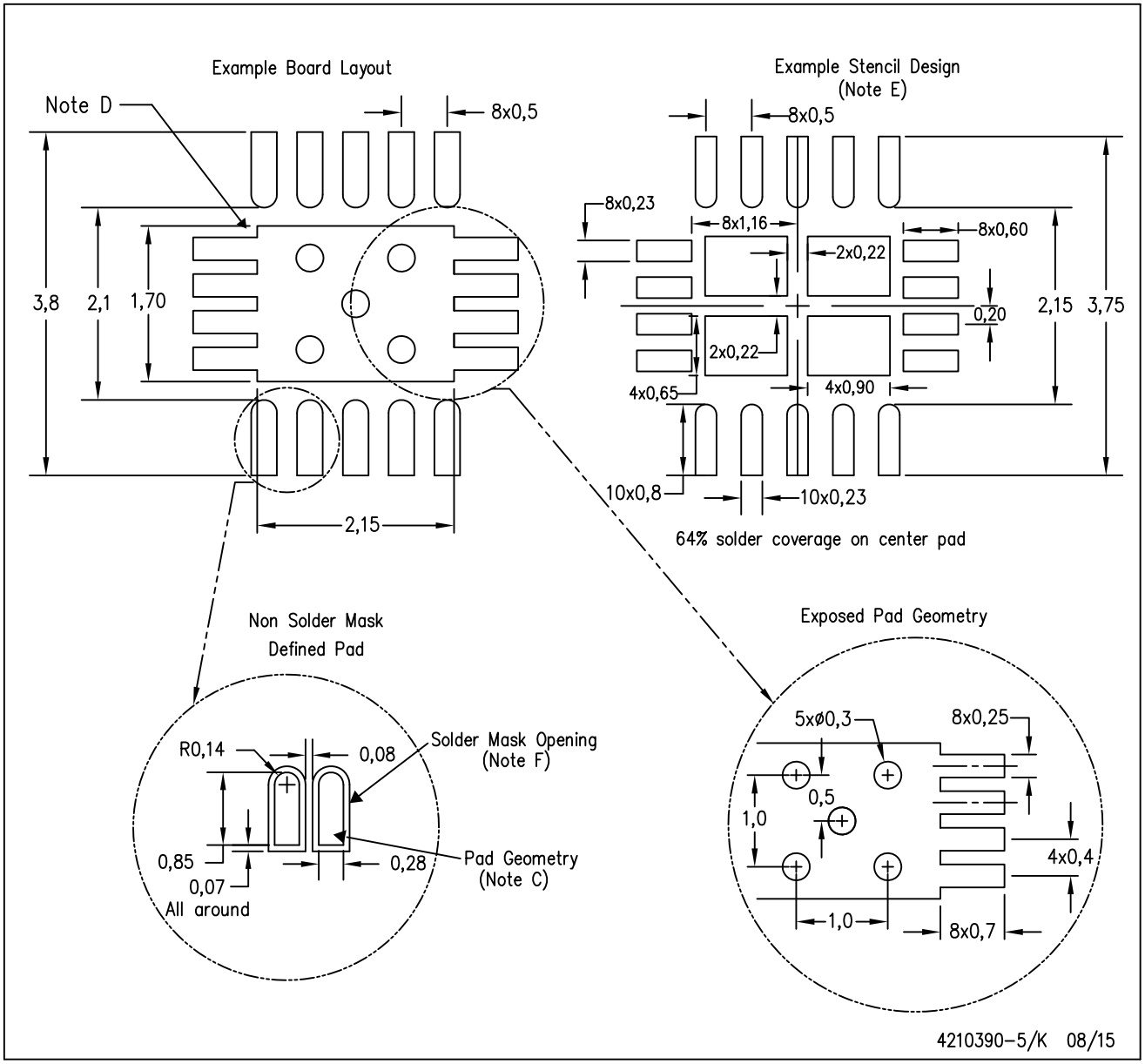
Bottom View

Exposed Thermal Pad Dimensions

4210391–5/Q 08/15

NOTE: A. All linear dimensions are in millimeters

DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025