TPS65265 4.5-V to 17-V Input Voltage, 5-A/3-A/2-A Output Current Triple Synchronous Step-Down Converter

1 Features

- Operating input voltage range 4.5 V to 17 V
- Feedback reference voltage 0.6 V ±1.33%
- Continuous output current 5 A/3 A/2 A
- Adjustable clock frequency from 250 kHz to 2.3 MHz
- External synchronization oscillator
- 120° out of phase for Buck1, Buck2, Buck3
- Dedicated enable pins for each buck
- Fixed SS time for each buck (2.4 ms)
- Automatic power-up, power-down sequence and adjustable interval time between bucks (6 combinations)
- Support Pulse Skipping Mode (PSM) and Forced Continuous Current Mode (FCCM)
- Output voltage power-good indicator and adjustable delay time
- Thermal overloading protection
- 32-pin QFN (RHB) 5-mm × 5-mm package

2 Applications

- DTV
- Set-top boxes/OTT
- Home gateway and access point networks
- Surveillance

3 Description

The TPS65265 incorporates triple synchronous buck converters with 4.5-V to 17-V wide input voltage range that encompassed most intermediate bus voltage operating off 5-, 9-, 12- or 15-V power bus or battery. The converter with constant frequency peak current mode is designed to simplify its application while giving designers options to optimize the system according to targeted applications. The switching frequency of the converters can be adjustable from 250 kHz to 2.3 MHz with an external resistor or external clock. 120° out-of-phase operation between Buck1, Buck2, and Buck3 minimizes the input filter requirements.

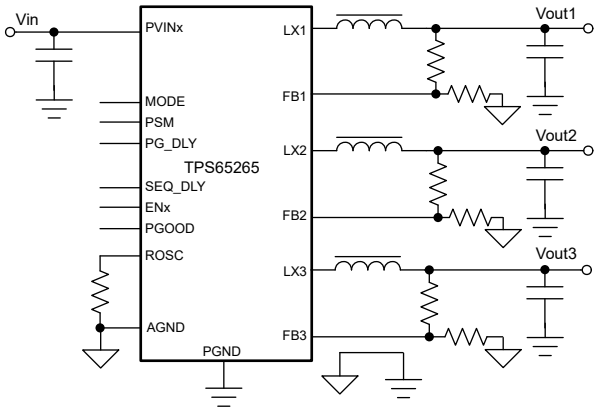
The TPS65265 operates in pulse skipping mode (PSM) with driving MODE pin to high or leaving float and operates in force continuous current mode (FCC) with connecting MODE pin to GND. PSM mode provides high efficiency by reducing switching losses at light load and FCC mode reduces noise susceptibility and RF interference.

The TPS65265 is available in a 32-pin thermal enhanced QFN (RHB) 5-mm × 5-mm thin package.

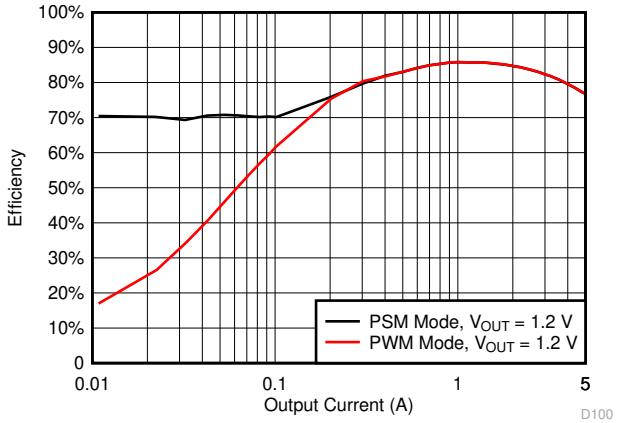
Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65265	RHB (VQFN, 32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application Circuit



Efficiency vs Output Load

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

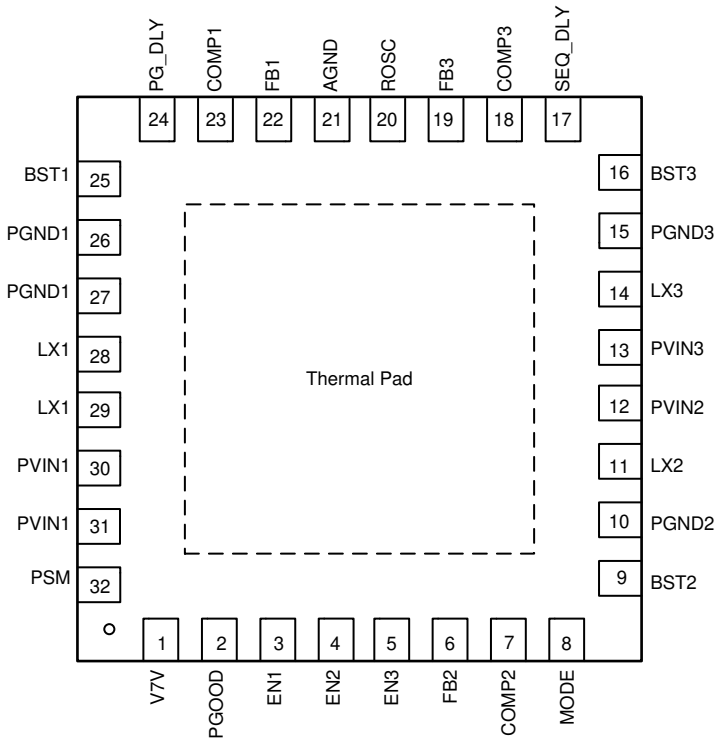
Changes from Revision A (December 2015) to Revision B (May 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Removed color from images throughout the document	1
• Renamed section 5 to *Device Comparison Table*	3
• Change the description of V7V pin in Table 6-1	3
• Changed the recommended value of capacitor from V7V pin to power ground in *V7V Low Dropout Regulator and Bootstrap*	20
• Changed the recommended value of C5 in Figure 9-1	26

Changes from Revision * (December 2015) to Revision A (December 2015)	Page
• Changed device status to production data and released full data sheet	1

5 Device Comparison Table

PART NUMBER	DESCRIPTION	COMMENTS
TPS65261, TPS65261-1	4.5 V to 18 V, triple bucks with input voltage power failure indicator	Triple bucks 3-A/2-A/2-A output current, features an open drain RESET signal to monitor input power failure, automatic power sequencing
TPS65262, TPS65262-1	4.5 V to 18 V, triple bucks with dual adjustable LDOs	Triple bucks 3-A/1-A/1-A output current, automatic power sequencing, dual LDOs 100 mA/200 mA for TPS65262, 350 mA/150 mA for TPS65262-1
TPS65263	4.5 V to 18 V, triple bucks with I^2C interface	Triple bucks 3-A/2-A/2-A output current, I^2C controlled dynamic voltage scaling (DVS)
TPS65266	2.7 V to 6.5 V, triple bucks	Triple bucks 3 A/2 A/2 A

6 Pin Configuration and Functions



There is no electric signal down bonded to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.

Figure 6-1. RHB Package 32-Lead Plastic QFN Top View

Table 6-1. Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	V7V	Internal LDO for gate driver and internal controller. Connect a 10-µF capacitor from the pin to power ground
2	PGOOD	An open drain output, asserts low if output voltage of any buck beyond regulation range due to thermal shutdown, over-current, under-voltage or ENx shut down.
3	EN1	Enable for buck1. Float to enable. Can use this pin to adjust the input undervoltage lockout (UVLO) of buck1 with a resistor divider.
4	EN2	Enable for buck2. Float to enable. Can use this pin to adjust the input UVLO of buck2 with a resistor divider.
5	EN3	Enable for buck3. Float to enable. Can use this pin to adjust the input UVLO of buck3 with a resistor divider.
6	FB2	Feedback Kelvin sensing pin for buck2 output voltage. Connect this pin to buck2 resistor divider.
7	COMP2	Error amplifier output and Loop compensation pin for buck2. Connect a series resistor and capacitor to compensate the control loop of buck2 with peak current PWM mode.

Table 6-1. Pin Functions (continued)

PIN		DESCRIPTION
NO.	NAME	
8	MODE	When floating, Buck1/2/3 are controlled separate by EN1/2/3. When tied to HIGH or tied to GND, an automatic power-up/power-down sequence is provided according to states of EN1, EN2 and EN3 pins.
9	BST2	Boot strapped supply to the high side floating gate driver in buck2. Connect a capacitor (recommend 47nF) from BST2 pin to LX2 pin.
10	PGND2	Power ground connection of buck2. Connect PGND2 pin as close as practical to the (-) terminal of PVIN2 input ceramic capacitor.
11	LX2	Switching node connection to the inductor and bootstrap capacitor for buck2. The voltage swing at this pin is from a diode voltage below the ground up to PVIN2 voltage.
12	PVIN2	Input power supply for buck2. Connect PVIN2 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10 µF).
13	PVIN3	Input power supply for buck3. Connect PVIN3 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10 µF).
14	LX3	Switching node connection to the inductor and bootstrap capacitor for buck3. The voltage swing at this pin is from a diode voltage below the ground up to PVIN3 voltage.
15	PGND3	Power ground connection of buck3. Connect PGND3 pin as close as practical to the (-) terminal of PVIN3 input ceramic capacitor.
16	BST3	Boot strapped supply to the high side floating gate driver in buck3. Connect a capacitor (recommend 47nF) from BST3 pin to LX3 pin.
17	SEQ_DLY	Delay time programmable between bucks at automatic power sequencing mode. Connect an external capacitor to set the interval delay time.
18	COMP3	Error amplifier output and Loop compensation pin for buck3. Connect a series resistor and capacitor to compensate the control loop of buck3 with peak current PWM mode.
19	FB3	Feedback Kelvin sensing pin for buck3 output voltage. Connect this pin to buck3 resistor divider.
20	ROSC	Oscillator frequency programmable pin. Connect an external resistor to set the switching frequency.
21	AGND	Analog ground common to buck controllers and other analog circuits.
22	FB1	Feedback Kelvin sensing pin for buck1 output voltage. Connect this pin to buck1 resistor divider.
23	COMP1	Error amplifier output and Loop compensation pin for buck1. Connect a series resistor and capacitor to compensate the control loop of buck1 with peak current PWM mode.
24	PG_DLY	PGOOD delay programmable pin. Connect an external capacitor to set the delay time.
25	BST1	Boot strapped supply to the high side floating gate driver in buck1. Connect a capacitor (recommend 47nF) from BST1 pin to LX1 pin.
26, 27	PGND1	Power ground connection of Buck1. Connect PGND1 pin as close as practical to the (-) terminal of PVIN1 input ceramic capacitor.
28, 29	LX1	Switching node connection to the inductor and bootstrap capacitor for buck1. The voltage swing at this pin is from a diode voltage below the ground up to PVIN1 voltage.
30, 31	PVIN1	Input power supply for buck1. Connect PVIN1 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 22 µF).
32	PSM	Ties to HIGH or leaves floating, PSM mode; Ties to GND, FCCM mode.
PAD		There is no electric signal down bonded to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
PVIN1, PVIN2, PVIN3, PGOOD	–0.3	20	V
LX1, LX2, LX3	–1.0	19	V
LX1, LX2, LX3 (maximum withstand voltage transient <10 ns)	–1.0	21	V
BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins, respectively	–0.3	7	V
EN1, EN2, EN3, V7V, MODE, PSM	–0.3	7	V
FB1, FB2, FB3, COMP1 , COMP2, COMP3, ROSC, SEQ_DLY, PG_DLY	–0.3	3.6	V
AGND, PGND1, PGND2, PGND3	–0.3	0.3	V
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
PVIN1, PVIN2, PVIN3	4.5	17	V
LX1, LX2, LX3 (Maximum withstand voltage transient <10 ns)	–0.8	19	V
BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively	–0.1	6.8	V
EN1, EN2, EN3, V7V, MODE, PSM	–0.1	6.3	V
FB1, FB2, FB3, COMP1 , COMP2, COMP3, ROSC, SEQ_DLY, PG_DLY	–0.1	3.3	V
Operating junction temperature, T_J	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS65265 RHB (QFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_J = –40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
V_{IN}	Input voltage range		4.5		17	V
UVLO	VIN undervoltage lockout	VIN rising	3.6	3.8	4	V
		VIN falling	3.0	3.2	3.4	V
		Hysteresis		600		mV
IDD_{SDN}	Shutdown supply current	PVIN = 12 V, EN1 = EN2 = EN3 = MODE = 0 V	9	11.5	14	µA
IDD_{Q_NSW}	Input quiescent current without buck1/2/3 switching	EN1 = EN2 = EN3 = 5 V, FB1 = FB2 = FB3 = 0.8 V	550	680	800	µA
IDD_{Q_NSW1}		EN1 = 5 V, EN2 = EN3 = 0 V, FB1 = 0.8 V	280	350	425	µA
IDD_{Q_NSW2}		EN2 = 5 V, EN1 = EN3 = 0 V, FB2 = 0.8 V	280	350	425	µA
IDD_{Q_NSW3}		EN3 = 5 V, EN1 = EN2 = 0 V, FB3 = 0.8 V	280	350	425	µA
V_{7V}	V7V LDO output voltage	PVIN1 = 12 V, V_{7V} load current = 0 A	5.9	6.1	6.3	V
I_{OCP_V7V}	V7V LDO current limit		110	177	235	mA
FEEDBACK VOLTAGE REFERENCE						
V_{FB}	Feedback voltage	V_{COMP} = 1.2 V	0.592	0.6	0.608	V
Buck1, Buck2, Buck3						
V_{ENXH}	EN1/2/3 high-level input voltage		1.08	1.15	1.22	V
V_{ENXL}	EN1/2/3 low-level input voltage		1.06	1.12	1.17	V
I_{ENX1}	EN1/2/3 pullup current	ENx = 1 V	2.3	2.9	3.4	µA
I_{ENX2}	EN1/2/3 pullup current	ENx = 1.5 V	5.1	6	6.8	µA
I_{ENhys}	hysteresis current			3.1		µA
t_{ON_MIN}	Minimum on time	I_{load} = 100 mA		75	120	ns
G_{m_EA}	Error amplifier transconductance	–2 µA < I_{COMPX} < 2 µA	174	350	530	µS
$G_{m\_PS1/2/3}$	COMP1/2/3 voltage to inductor current G_m (1)	I_{LX} = 0.5 A		12		A/V
I_{LIMIT1}	buck1 peak inductor current limit		6.0	8.0	9.6	A
$I_{LIMITSOURCE1}$	buck1 low-side source current limit		5.3	7.7	10	A
$I_{LIMITSINK1}$	buck1 low-side sink current limit			1.4		A
I_{LIMIT2}	buck2 peak inductor current limit		3.85	5.2	6.65	A
$I_{LIMITSOURCE2}$	buck2 low-side source current limit		3	4.8	5.5	A
$I_{LIMITSINK2}$	buck2 low-side sink current limit			1.2		A
I_{LIMIT3}	buck3 peak inductor current limit		2.6	3.6	4.45	A
$I_{LIMITSOURCE3}$	buck3 low-side source current limit		2.6	3.7	4.6	A
$I_{LIMITSINK3}$	buck3 low-side sink current limit			1.2		A
t_{Hiccup_wait}	Overcurrent wait time(1)			256		cycles
t_{Hiccup_re}	Hiccup time before restart(1)			8192		cycles
R_{dson_HS1}	buck1 high-side switch resistance	PVIN = 12 V		39		mΩ
R_{dson_LS1}	buck1 low-side switch resistance	PVIN = 12 V		25		mΩ
R_{dson_HS2}	buck2 high-side switch resistance	PVIN = 12 V		52		mΩ
R_{dson_LS2}	buck2 low-side switch resistance	PVIN = 12 V		43		mΩ
R_{dson_HS3}	buck3 high-side switch resistance	PVIN = 12 V		70		mΩ

7.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{dson_LS3}	buck3 low-side switch resistance	PVIN = 12 V		65		mΩ
PGOOD, MODE, PSM, SEQ_DLY, PG_DLY						
V_{th_PG}	Feedback voltage threshold	FBx undervoltage falling		92.5		%VREF
		FBx undervoltage rising		95		%VREF
		FBx overvoltage rising		107.5		%VREF
		FBx overvoltage falling		105		%VREF
$t_{DEGLITCH(PG)\_F}$	PGOOD falling edge deglitch time			256		cycles
$t_{DEGLITCH(PG)\_R}$	PGOOD rising edge deglitch time			256		cycles
I_{PG}	PGOOD pin leakage				0.08	µA
V_{LOW_PG}	PGOOD pin low voltage	PVIN1 = 12 V, I_{SINK} = 1 mA			0.25	V
V_{MODE_H}	MODE high level input voltage		2.4	2.6	2.8	V
V_{MODE_L}	MODE low level input voltage		0.11	0.16	0.23	V
V_{PG_DLYTH}	PG_DLY threshold		1.4	1.5	1.6	V
I_{PG_DLY}	PG_DLY pullup current	PG_DLY = 0.5 V	2.0	3.0	4.1	µA
V_{SEQ_DLYTH1}	SEQ_DLY threshold		0.7	0.75	0.8	V
V_{SEQ_DLYTH2}	SEQ_DLY threshold		1.4	1.5	1.58	V
I_{SEQ_DLY}	SEQ_DLY pullup current	SEQ_DLY = 0.5 V	2	3	4.1	µA
V_{PSMH}	PSM pin high level input voltage		1.3	1.4	1.55	V
V_{PSML}	PSM pin low level input voltage		1	1.1	1.2	V
OSCILLATOR						
F_{SW}	Switching frequency	R_{OSC} = 82.5 kΩ	580	610	640	kHz
F_{SW_range}	Switching frequency		250		2300	kHz
t_{SYNC_w}	Clock sync minimum pulse width		80			ns
F_{SYNC_HI}	Clock sync high threshold				2	V
V_{SYNC_LO}	Clock sync low threshold		0.4			V
THERMAL PROTECTION						
T_{TRIP_OTP}	Thermal protection trip point(1)	Temperature rising		160		°C
T_{HYST_OTP}		Hysteresis		20		°C

(1) Lab validation result

7.6 Typical Characteristics

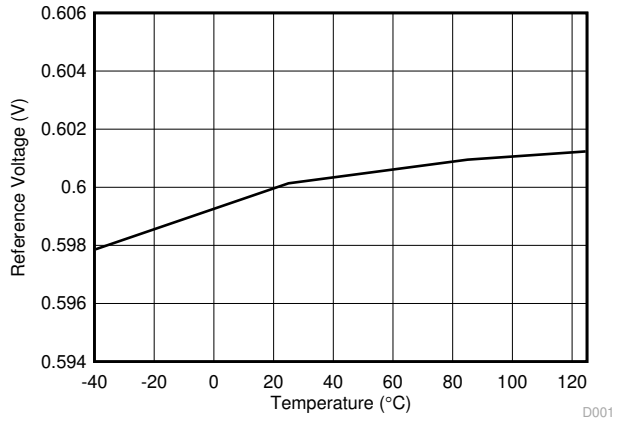


Figure 7-1. Voltage Reference vs Temperature

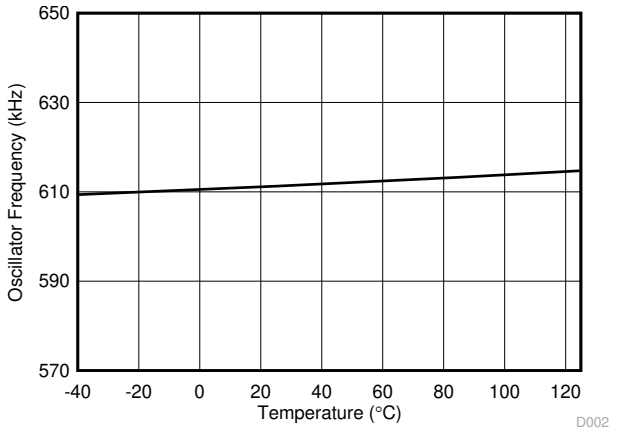


Figure 7-2. Oscillator Frequency vs Temperature

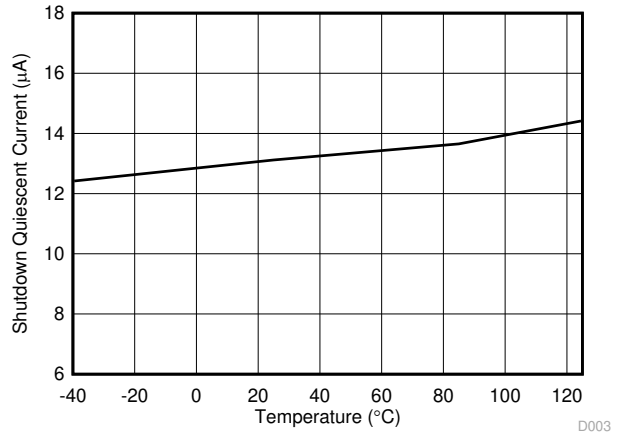


Figure 7-3. Shutdown Quiescent vs Temperature

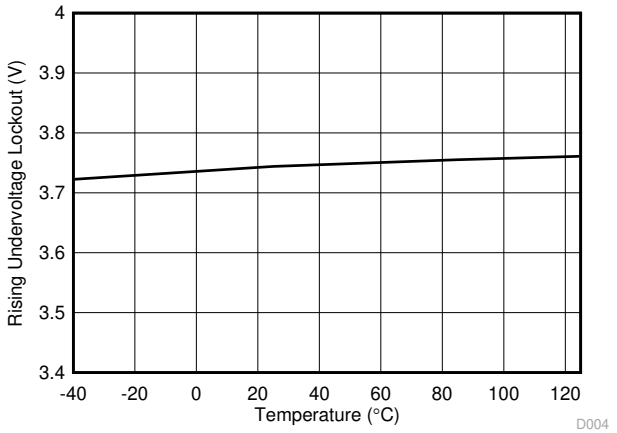


Figure 7-4. Vin UVLO Raising vs Temperature

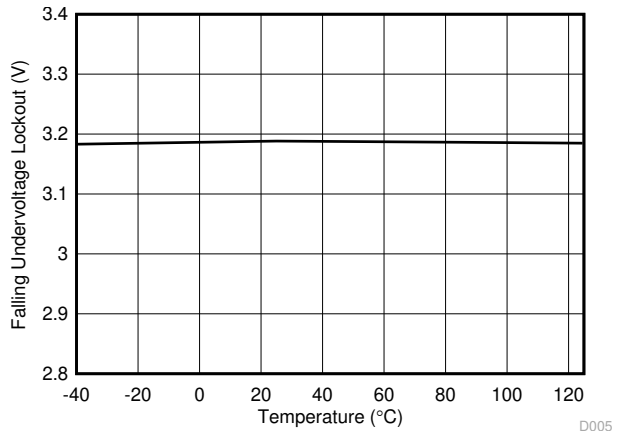


Figure 7-5. Vin UVLO Falling vs Temperature

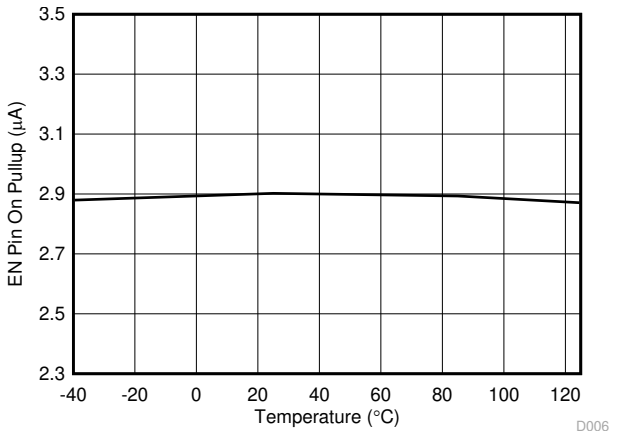


Figure 7-6. EN Pin Pullup Current vs Temperature, EN = 1.0 V

7.6 Typical Characteristics (continued)

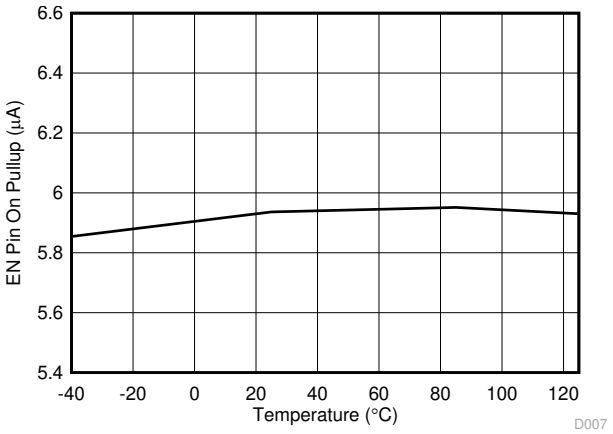


Figure 7-7. EN Pin Pullup Current vs Temperature, EN = 1.5 V

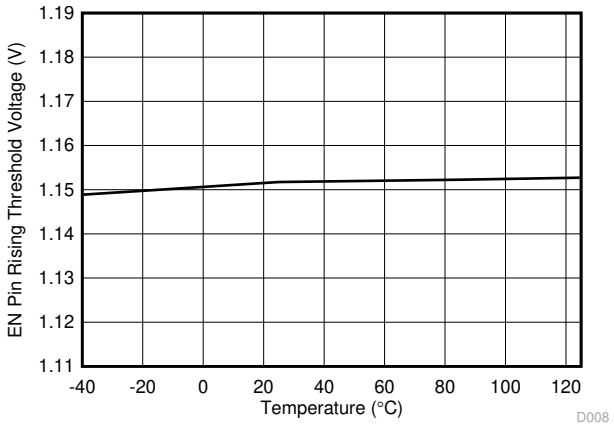


Figure 7-8. EN Pin Threshold Raising vs Temperature

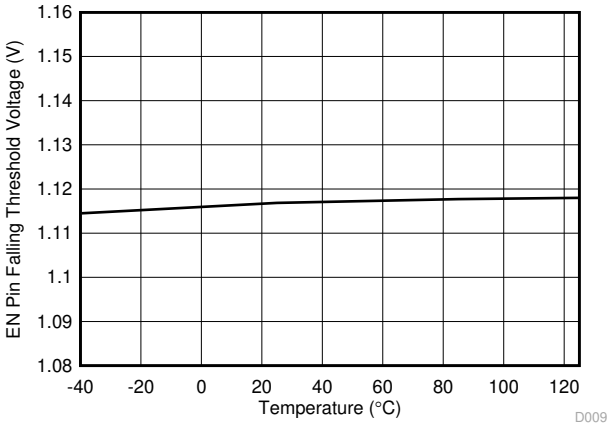


Figure 7-9. EN Pin Threshold Falling vs Temperature

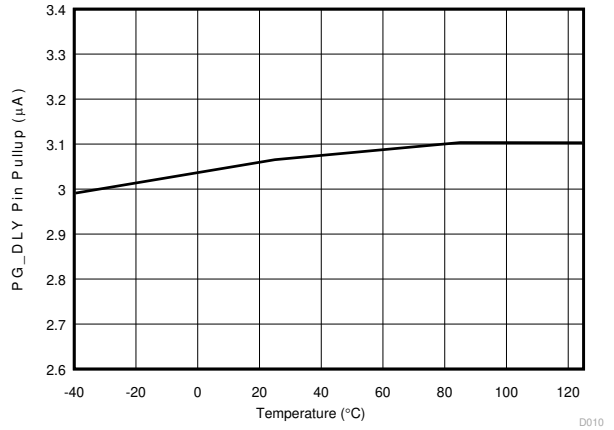


Figure 7-10. PG_DLY Pin Pullup Current vs Temperature, PG_DLY = 0.5 V

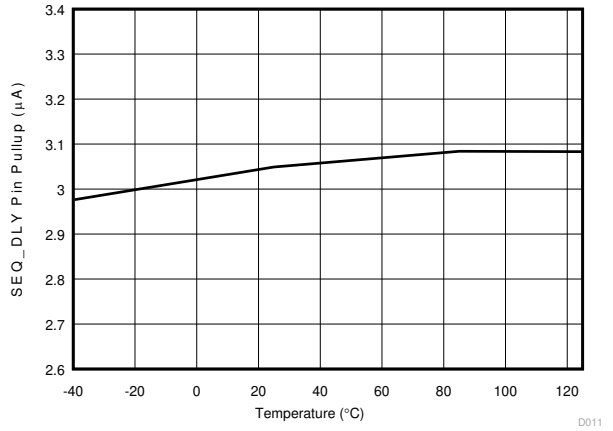


Figure 7-11. SEQ_DLY Pin Pullup Current vs Temperature, PG_DLY = 0.5 V

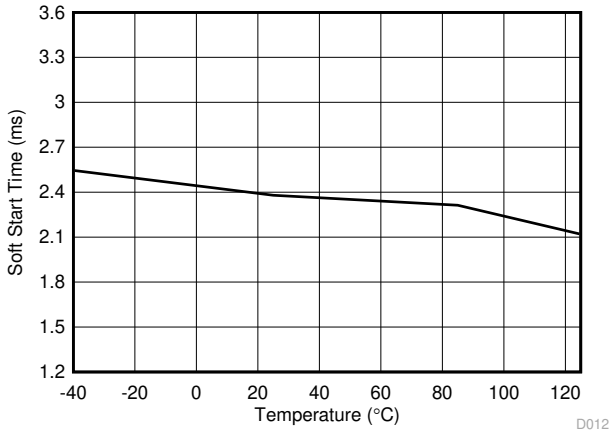


Figure 7-12. Soft-Start Time vs Temperature

7.6 Typical Characteristics (continued)

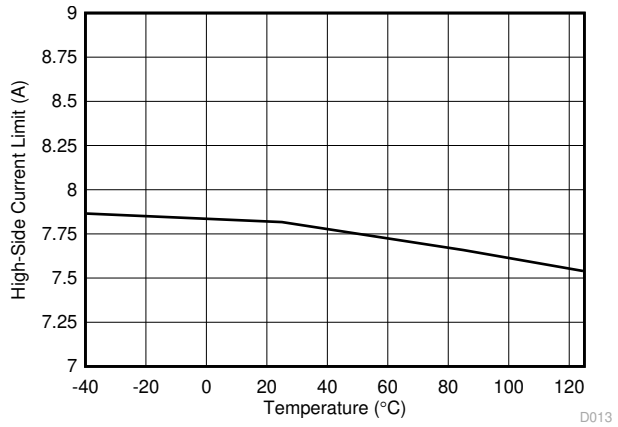


Figure 7-13. Buck1 High-Side Current Limit vs Temperature

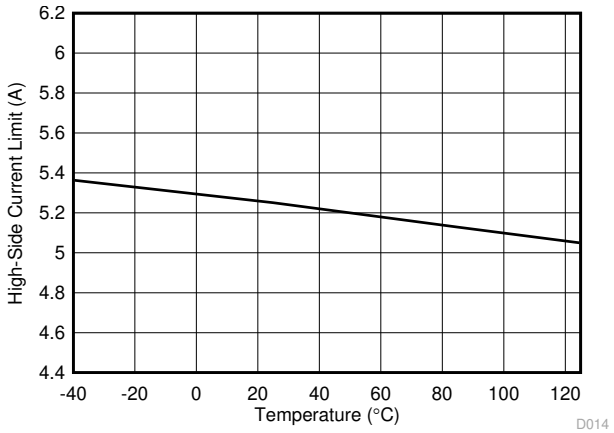


Figure 7-14. Buck2 High-Side Current Limit vs Temperature

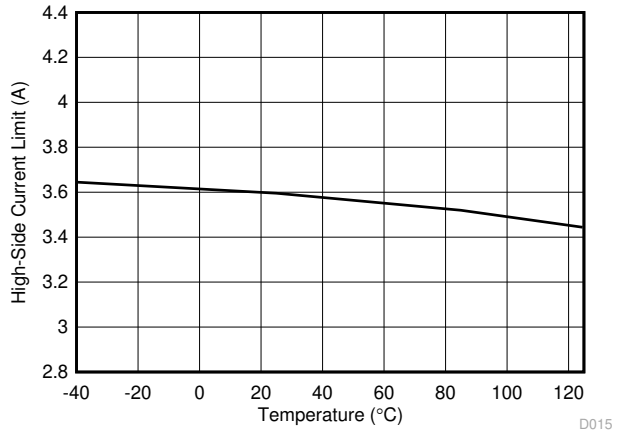


Figure 7-15. Buck3 High-Side Current Limit vs Temperature

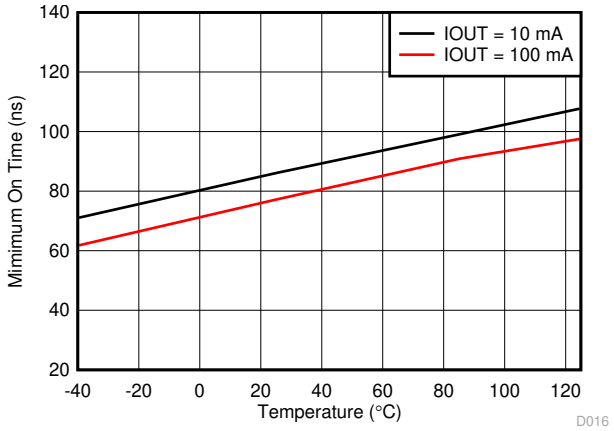


Figure 7-16. Minimum On Time vs Temperature

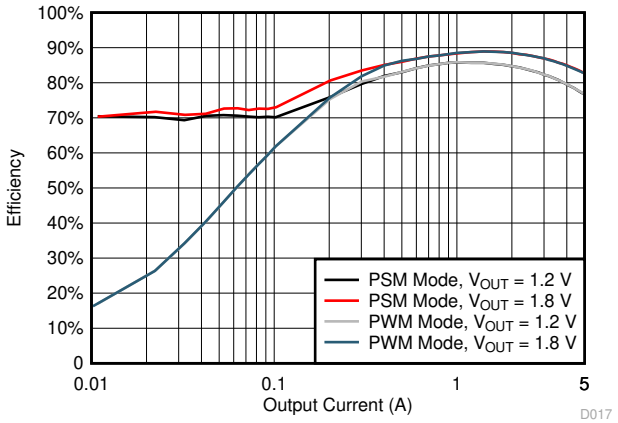


Figure 7-17. Buck1 Efficiency, V_{IN} = 12 V, F_{sw} = 610 kHz

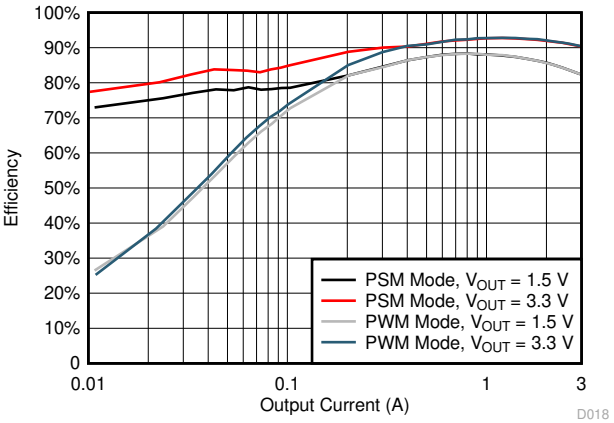


Figure 7-18. Buck2 Efficiency, V_{IN} = 12 V, F_{sw} = 610 kHz

7.6 Typical Characteristics (continued)

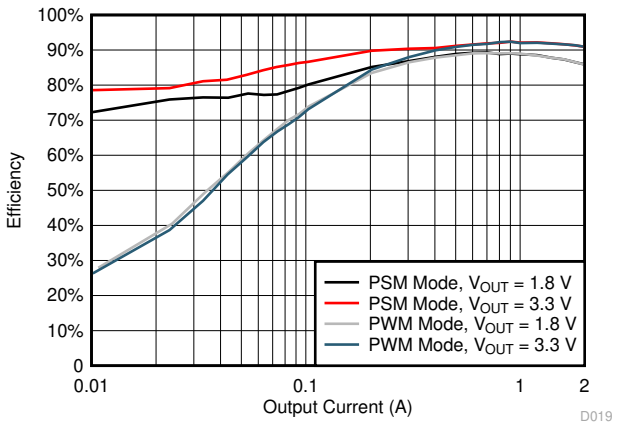


Figure 7-19. Buck3 Efficiency, V_{IN} = 12 V, F_{sw} = 610 kHz

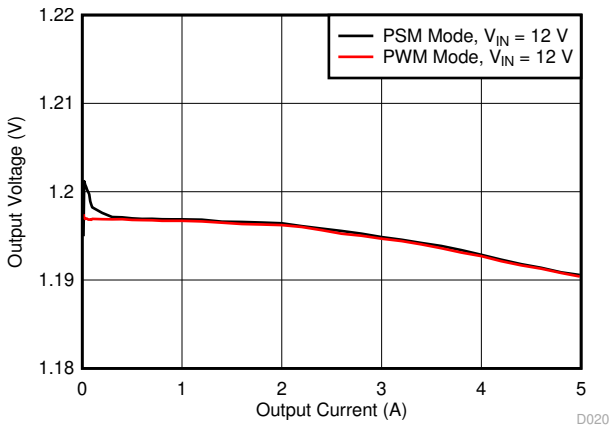


Figure 7-20. Buck1, Load Regulation

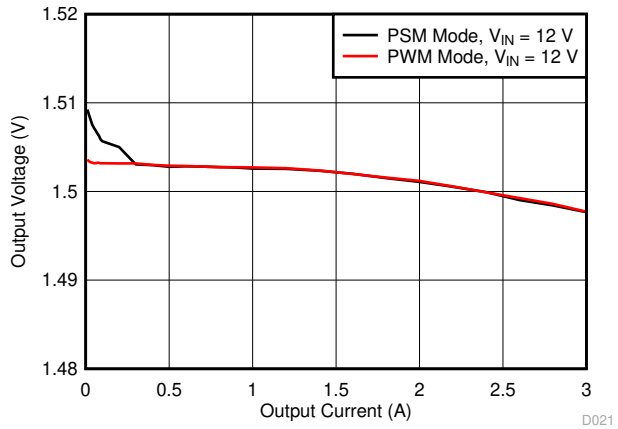


Figure 7-21. Buck2, Load Regulation

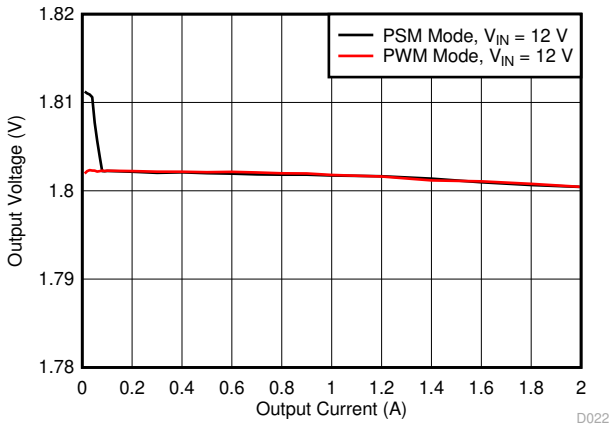


Figure 7-22. Buck3, Load Regulation

8 Detailed Description

8.1 Overview

The TPS65265 is a monolithic triple synchronous step-down (buck) converter with 5-A/3-A/2-A output currents. A wide 4.5-V to 17-V input supply voltage range encompasses most intermediate bus voltages operating off 5-V, 9-V, 12-V, or 15-V power bus. The feedback voltage reference for each buck is 0.6 V. Each buck is independent with dedicated enable, soft-start and loop compensation pins.

The TPS65265 implements a constant frequency, peak current mode control that simplifies external loop compensation. The wide switching frequency of 250 kHz to 2.3 MHz allows optimizing system efficiency, filtering size and bandwidth. The switching frequency can be adjusted with an external resistor connecting between ROSC pin and ground. The switching clock is 120° out-of-phase operation from the clocks of buck1, buck2, and buck3 channels to reduce input current ripple, input capacitor size and power supply induced noise.

The TPS65265 has been designed for safe monotonic startup into pre-biased loads. The default start up is when VIN is typically 3.8 V. The ENx pin also can be used to adjust the input voltage undervoltage lockout (UVLO) with an external resistor divider. In addition, the ENx pin has an internal 2.9μA current source, so the EN pin can be floating for automatically powering up the converters.

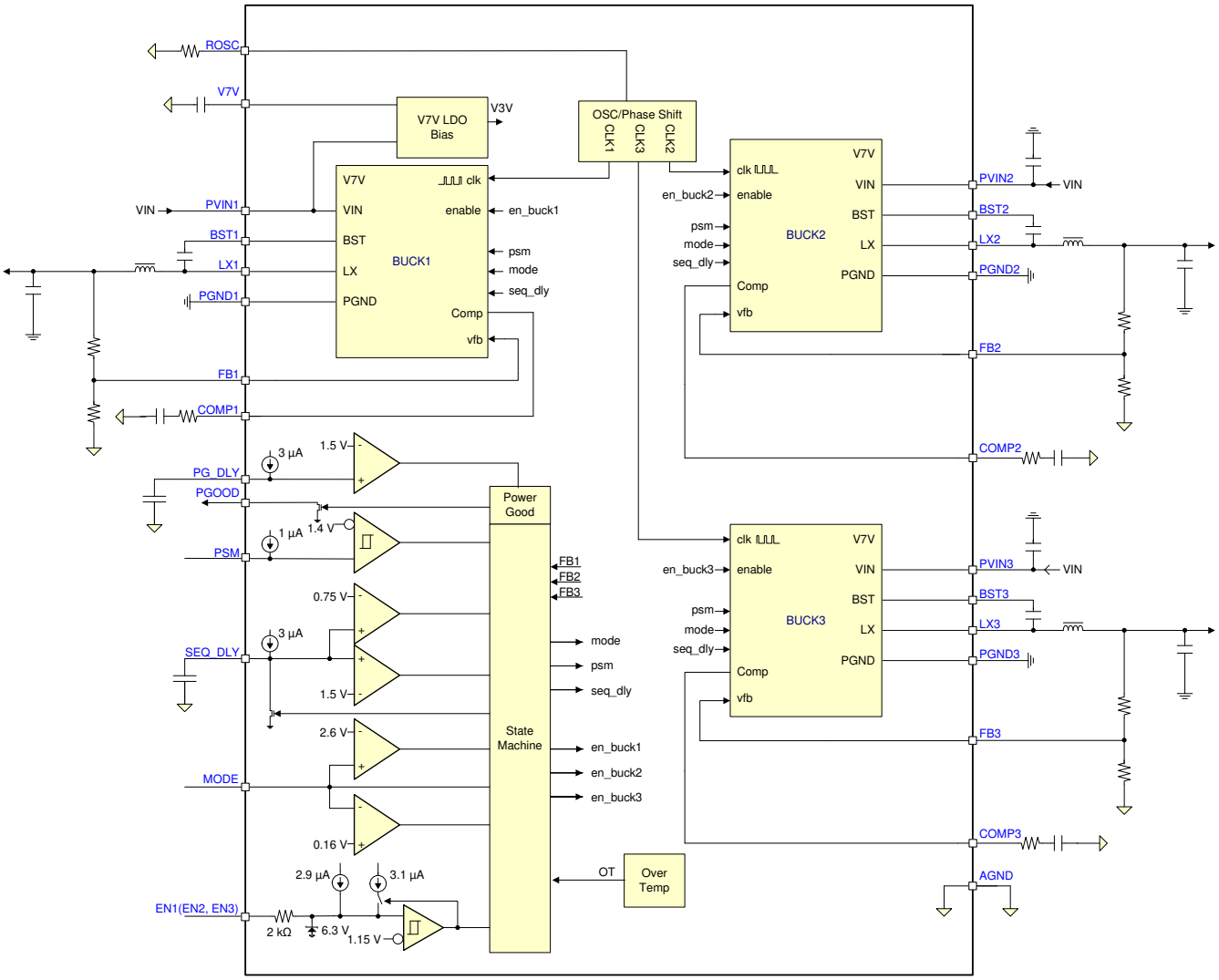
The TPS65265 reduces the external component count by integrating the bootstrap circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BST and LX pins. A UVLO circuit monitors the bootstrap capacitor voltage VBST-VLX in each buck. When V_{BST}-V_{LX} voltage drops to the threshold, LX pin is pulled low to recharge the bootstrap capacitor. The TPS65265 can operate at 100% duty cycle as long as the bootstrap capacitor voltage is higher than the BOOT-LX UVLO threshold which is typically 2.2 V.

The TPS65265 features PGOOD pin to supervise each output voltage of buck converters. The TPS65265 has power good comparators with hysteresis, which monitor the output voltages through feedback voltages. When all bucks are in regulation range and power sequence is done, PGOOD is asserted to high after the adjustable delay time.

The TPS65265 operates in PSM with connecting PSM pin to high or leaving float and operates in force continuous current mode (FCC) with driving PSM pin to GND.

The TPS65265 is protected from overload and over temperature fault conditions. The converter minimizes excessive output overvoltage transients by taking advantage of the power good comparator. When the output is over, the high-side MOSFET is turned off until the internal feedback voltage is lower than 105% of the 0.6V reference voltage. The TPS65265 implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections to avoid inductor current runaway. If the overcurrent condition has lasted for more than the OC wait time (256 clock cycle), the converter will shut down and restart after the hiccup time (8192 clock cycles). The TPS65265 shuts down if the junction temperature is higher than thermal shutdown trip point. When the junction temperature drops 20°C typically below the thermal shutdown trip point, the TPS65265 will be restarted under control of the soft start circuit automatically.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adjusting the Output Voltage

The output voltage of each buck is set with a resistor divider from the output of buck to the FB pin. TI recommends to use 1% tolerance or better resistors.

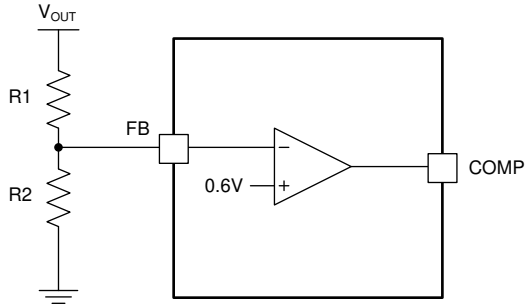


Figure 8-1. Voltage Divider Circuit

$$R_2 = R_1 \times \frac{0.6}{V_{out} - 0.6} \quad (1)$$

To improve efficiency at light loads consider using larger value resistors. If the values are too high, the regulator is more sensitive to noise. The recommended resistor values are shown in Table 8-1.

Table 8-1. Output Resistor Divider Selection

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)
1	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	31.6	10
3.3	45.3	10
3.3	22.6	4.99
5	73.2	10
5	36.5	4.99

8.3.2 Mix PGOOD, PG_DLY Functions

The PGOOD pin is an open drain output and withstands voltage higher to 17 V. After feedback voltage of each buck is between 95% (rising) and 105% (falling) of the internal voltage reference and PG_DLY pin voltage overs 1.5 V, the PGOOD pin pull-down is deasserted and the pin floats. TI recommends to use a pullup resistor between the values of 10 kΩ and 100 kΩ to a voltage source that is below 17 V.

The PGOOD pin is pulled low when any feedback voltage of buck is lower than 92.5% (falling), greater than 107.5% (rising) of the nominal internal reference voltage, or PG_DLY pin voltage is below 1.5V (typical). Also, the PGOOD is pulled low, if the input voltage is under-voltage locked up, thermal shutdown is asserted, the EN pin is pulled low or the converter is in soft-start period.

Different combinations of PGOOD, PG_DLY can implement different functions.

8.3.2.1 Programmable PGOOD DELAY

An internal 3-μA pullup current source is connected to PG_DLY pin. The PGOOD delay time can be programmed by connecting a capacitor between PG_DLY pin and ground. The delay time can be calculated as Equation 2.

$$t_{pgood\_delay} = \frac{V_{PG\_DLY} \times C_1}{I_p} \quad (2)$$

where

- V_{PG_DLY} = 1.5 V
- I_p = 3 μA

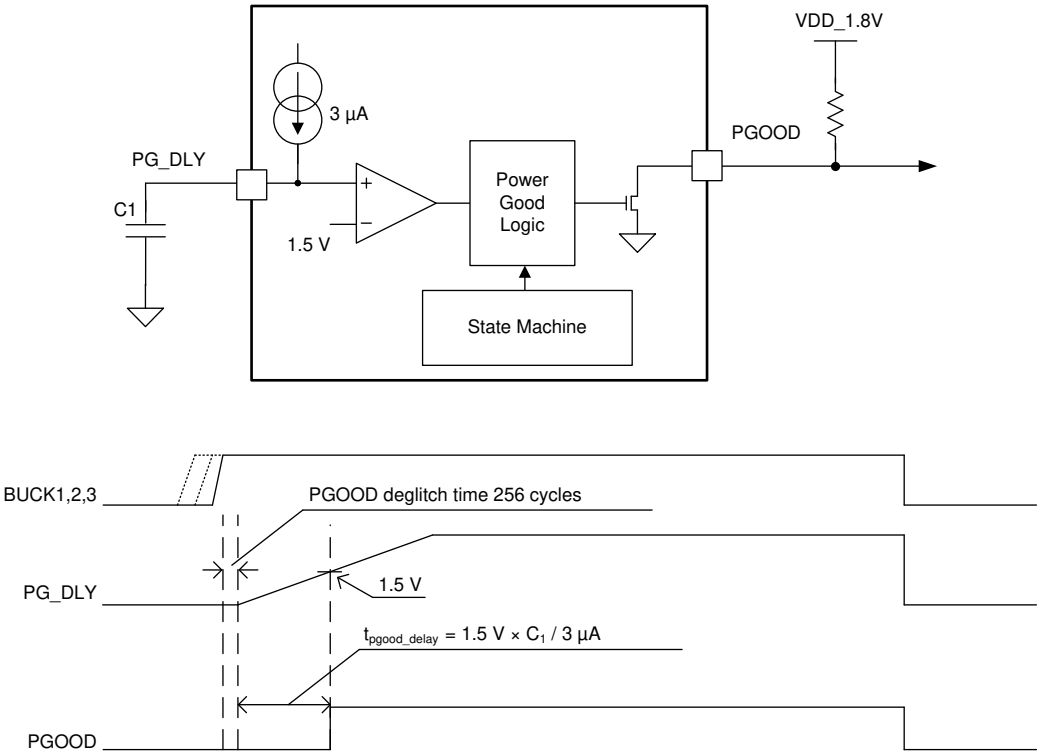


Figure 8-2. Power Good Delay Timing Diagram

8.3.2.2 Relay Control

PGOOD pin can implement one buck output's relay control through an N-MOSFET, circuit as in Figure 8-3.

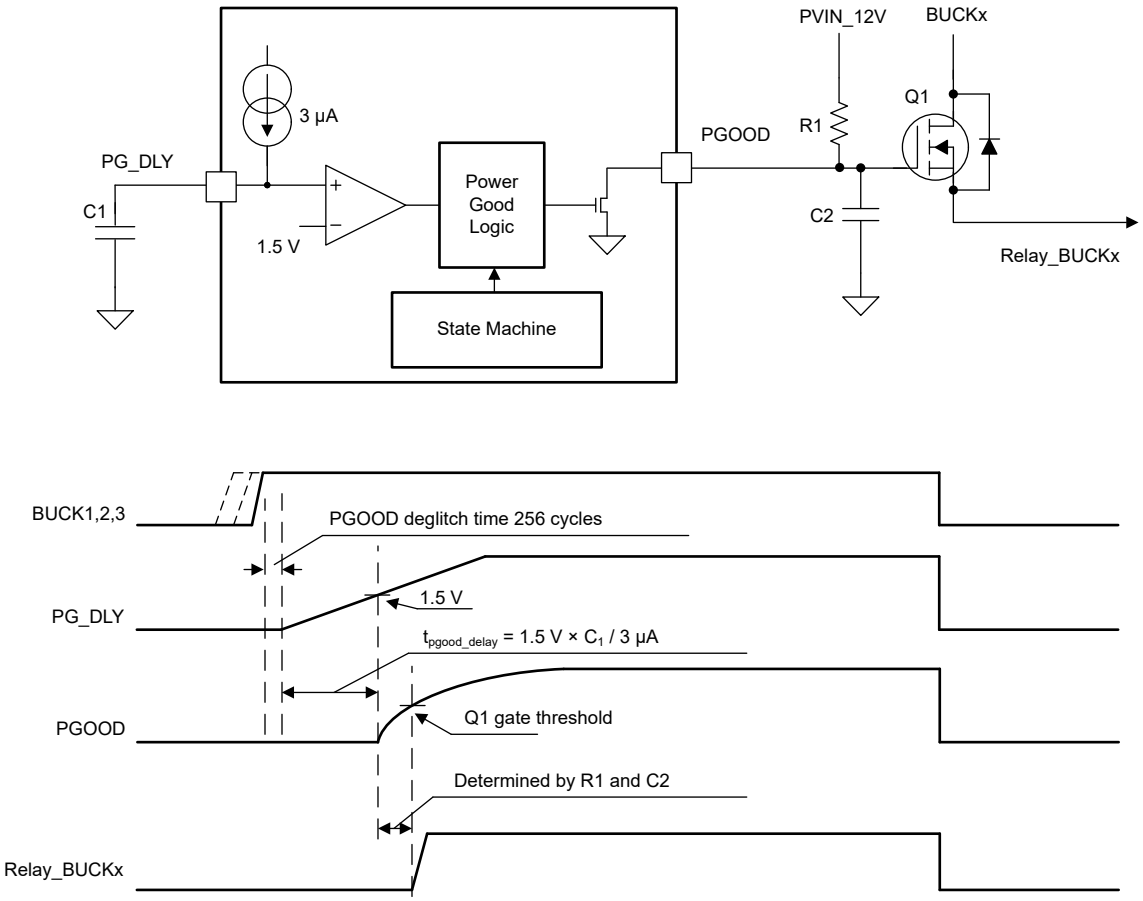


Figure 8-3. Relay Control Circuit

8.3.3 Enable and Adjusting UVLO

The EN1/2/3 pin provides electrical on/off control of the device. After the EN1/2/3 pin voltage exceeds the threshold voltage, the device starts operation. If each ENx pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low I_q state.

The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the PVIN1 pin. The device is disabled when the PVIN1 pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 600 mV. If an application requires a higher UVLO threshold on the PVIN1, in split-rail applications, then the ENx pin can be configured as shown in Figure 8-4. When using the external UVLO function TI recommends to set the hysteresis to be greater than 500 mV.

The EN pin has a small pullup current I_p which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h after the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 3 and Equation 4.

$$R_1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_P\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (3)$$

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_1\left(I_h + I_P\right)} \quad (4)$$

where

- I_h = 3.1µA
- I_p = 2.9 µA
- $V_{ENRISING}$ = 1.15 V
- $V_{ENFALLING}$ = 1.12 V

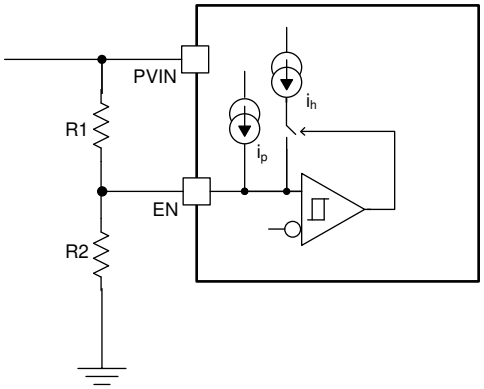


Figure 8-4. Adjustable PVIN UVLO, PVIN > 4.5 V

8.3.4 Soft-Start Time

TPS65265 has fixed 2.4-ms (typical) soft-start time.

8.3.5 Power-Up Sequencing

TPS65265 features a comprehensive sequencing circuit for the three bucks. If MODE pin was tied to HIGH or tied to GND and at the same time EN1 or EN2 (or both) was (were) pulled high, the automatic power-up and power-down sequence function is active. If MODE pin was left floating, three Buck on/off were separately controlled by three enable pin.

8.3.5.1 External Power Sequencing

The TPS65265 has dedicated enable pin and soft-start pin for each converter. The converter enable pins are biased by a current source that allows for easy sequencing by the addition of an external capacitor. Disabling the converter with an active pulldown transistor on the ENx pin allows for a predictable powerdown timing operation. The Figure 8-5 shows the timing diagram of a typical buck power-up sequence with connecting a capacitor at ENx pin.

A typical 1.4-µA current is charging ENx pin from input supply. When ENx pin voltage rise to typical 0.4 V, the internal V7V LDO turns on. A 2.9-µA pullup current is sourcing ENx. After ENx pin voltage reaches to ENx enabling threshold, 3.1-µA hysteresis current sources to the pin to improve noise sensitivity. After soft start time of 2.4 ms (typical), PGOOD monitor is enabled. If all output voltages are in the regulation and after PGOOD delay time, PGOOD is asserted.

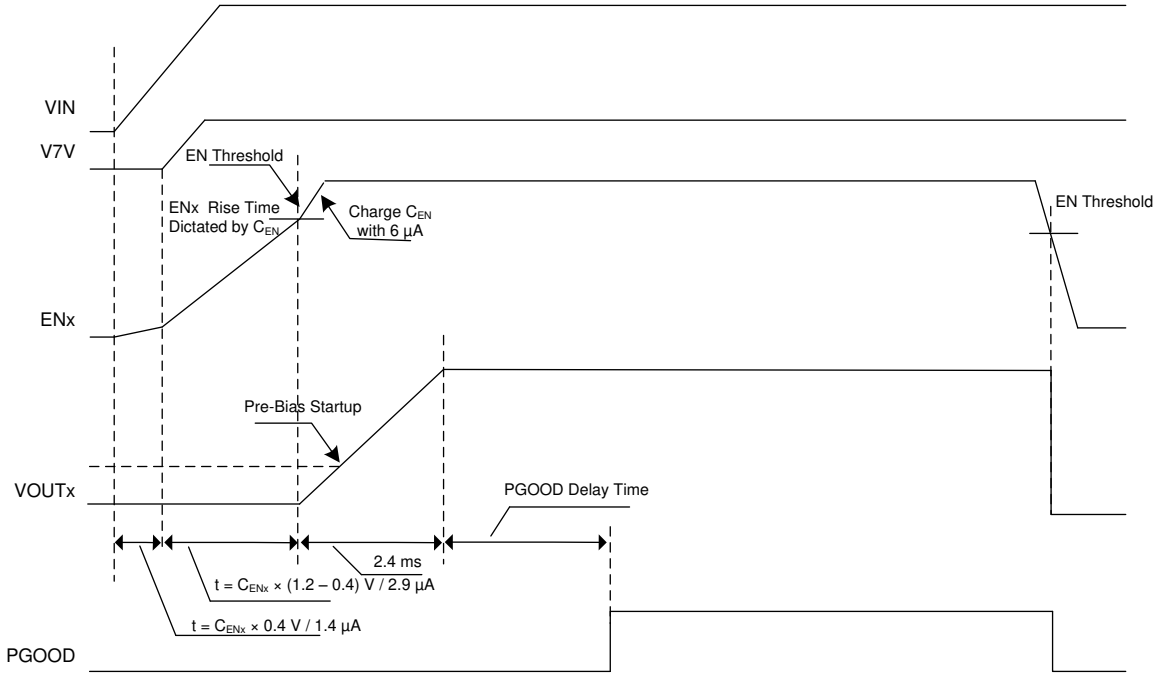


Figure 8-5. Startup Power Sequence

8.3.5.2 Automatic Power Sequencing

The TPS65265 starts with a predefined power-up and power-down sequence when MODE pin ties HIGH or ties to GND. As shown in Table 8-2, the sequence is determined by the different combinations of EN1 and EN2 status. EN3 is used to start and stop the converters. Figure 8-6 shows the power sequencing when MODE ties to GND, EN1, and EN2 are tied to HIGH.

An internal 3-µA pullup current source is connected to SEQ_DLY pin. The interval time between bucks can be programmed by connecting a capacitor between SEQ_DLY pin and ground. The interval time can be calculated with Equation 5.

$$t_1 = \frac{V_1 \times C_1}{i_p} \tag{5}$$

$$t_2 = \frac{(V_2 - V_1) \times C_1}{i_p} \tag{6}$$

where

- V_1 = 0.75 V
- V_2 = 1.5 V
- I_p = 3 µA

Table 8-2. Power Sequencing

	MODE	EN1	EN2	EN3	START SEQUENCING	SHUTDOWN SEQUENCING
Automatic Power Sequencing	Connect to GND	High	High	Used to start and stop bucks in sequence	buck1 → buck2 → buck3	buck3 → buck2 → buck1
	Connect to GND	Low	High		buck2 → buck1 → buck3	buck3 → buck1 → buck2
	Connect to GND	High	Low		buck2 → buck3 → buck1	buck1 → buck3 → buck2
	Connect to high or float	High	High		buck1 → buck3 → buck2	buck2 → buck3 → buck1
	Connect to high or float	Low	High		buck3 → buck1 → buck2	buck2 → buck1 → buck3
	Connect to high or float	High	Low		buck3 → buck2 → buck1	buck1 → buck2 → buck3
	Connect to GND	Low	Low	Reserved	Reserved	Reserved
	Connect to high or float	Low	Low	Reserved	Reserved	Reserved
Externally Controlled Sequencing	Floating	Used to start and stop buck1	Used to start and stop buck2	Used to start and stop buck3	x	x

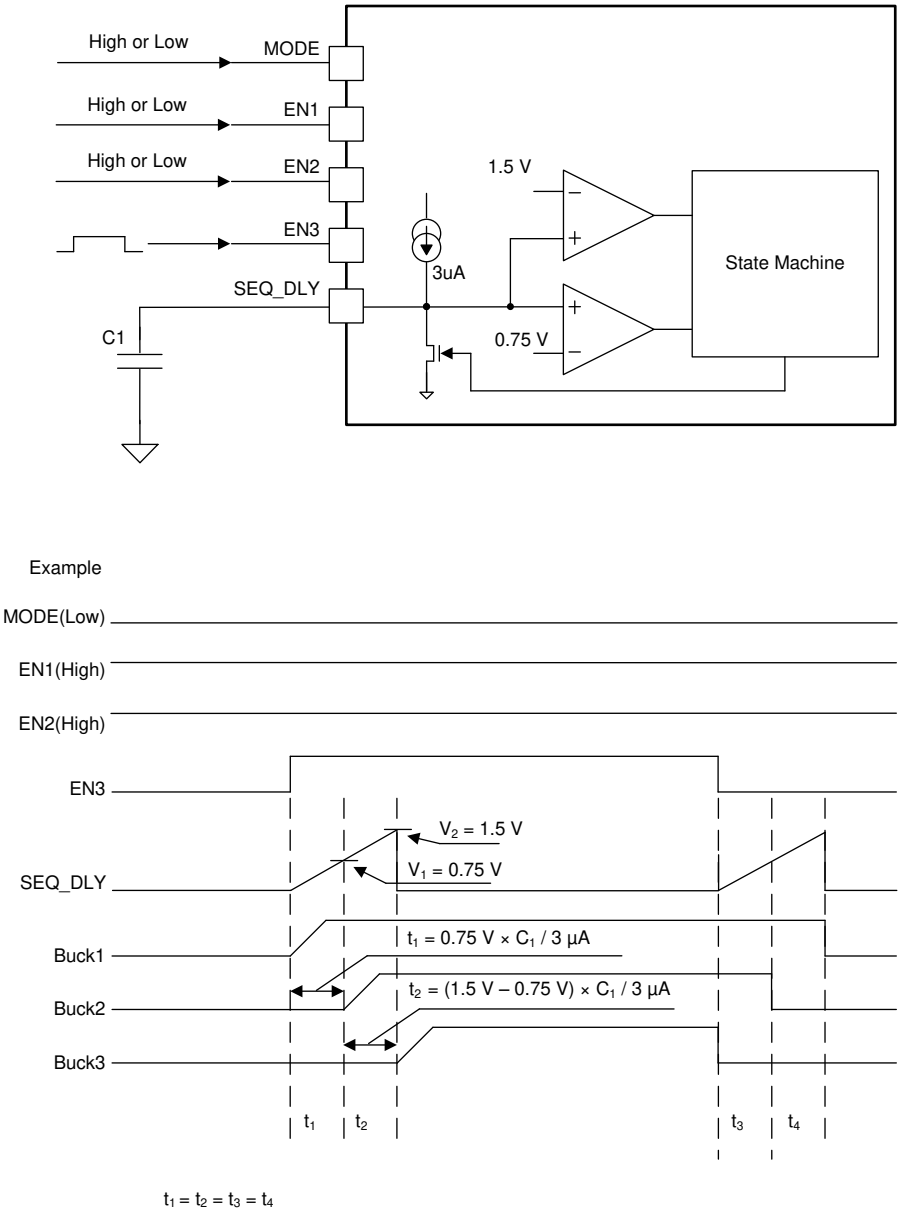


Figure 8-6. Automatic Power Sequencing

8.3.6 V7V Low Dropout Regulator and Bootstrap

Power for the high-side and low-side MOSFET drivers and most other internal circuitry is derived from the V7V pin. The internal built-in low dropout linear regulator (LDO) supplies 6.1 V (typical) from PVIN1 to V7V. A 10-µF ceramic capacitor must be connected from V7V pin to power ground.

If the input voltage, PVIN1, decreases to UVLO threshold voltage, the UVLO comparator detects V7V pin voltage and forces the converter off.

Each high-side MOSFET driver is biased from the floating bootstrap capacitor CB, shown in Figure 8-7, which is normally recharged during each cycle through an internal low-side MOSFET or the body diode of low-side MOSFET when the high-side MOSFET turns off. The boot capacitor is charged when the BST pin voltage is less than PVIN and BST-LX voltage is below regulation. The recommended value of this ceramic capacitor is 47 nF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10V or higher is recommended because of the stable characteristics over temperature and voltage. Each low-side MOSFET driver is powered from V7V pin directly.

To improve dropout, the device is designed to operate at 100% duty cycle as long as the BST to LX pin voltage is greater than the BST-LX UVLO threshold, which is typically 2.2 V. When the voltage between BST and LX drops below the BST-LX UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged.

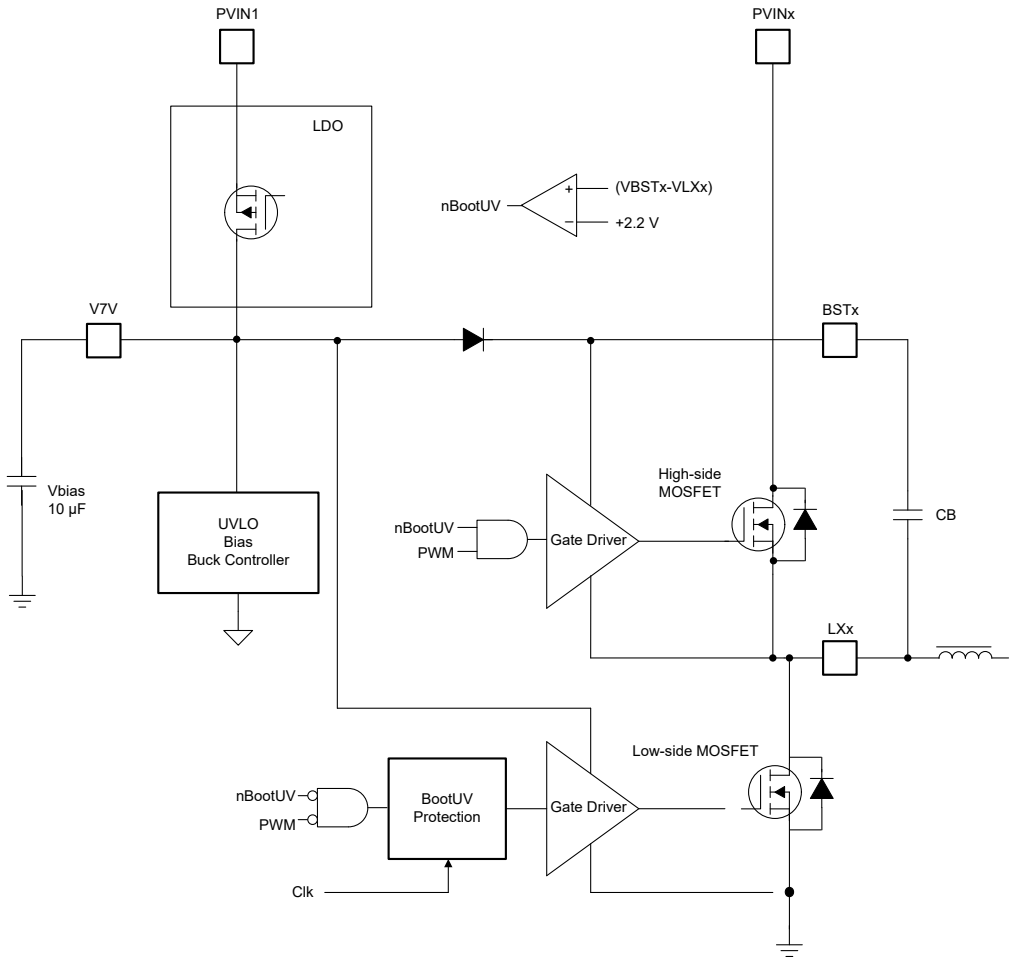


Figure 8-7. V7V Linear Dropout Regulator and Bootstrap Voltage Diagram

8.3.7 Out of Phase Operation

To reduce input ripple current, three switching clocks are 120° out-of-phase. This enables the system having less input current ripple to reduce input capacitors' size, cost, and EMI.

8.3.8 Output Overvoltage Protection (OVP)

The device incorporates an output OVP circuit to minimize output voltage overshoot. When the output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications with small output capacitance, the load can respond faster than the error amplifier. This leads to the possibility of an output overshoot. Each buck compares the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET turns on at the next clock cycle.

8.3.9 PSM

The TPS65265 can enter high-efficiency PSM operation at light load current when PSM pin connects to high or leave floating.

When a controller is enabled for PSM operation, the peak inductor current is sensed and compared with 180 mA current typically. Because the integrated current comparator catches the peak inductor current only, the average load current entering PSM varies with the applications and external output filters. In PSM, the sensed peak inductor current is clamped at 180 mA.

When a controller operates in PSM, the inductor current is not allowed to reverse. The reverse current comparator turns off the low-side MOSFET when the inductor current reaches zero, preventing it from reversing and going negative.

Due to the delay in the circuit and current comparator t_{dly} (typical 50 ns at PVIN = 12 V), the real peak inductor current threshold to turn off high-side power MOSFET must shift higher depending on inductor inductance and input/output voltages. The threshold of peak inductor current to turn off high-side power MOSFET can be calculated by Equation 7.

$$IL_{PEAK} = 180\ mA + \frac{V_{in} - V_{out}}{L} \times tdly \tag{7}$$

After the charge accumulated on Vout capacitor is more than loading need, COMP pin voltage drops to low voltage driven by error amplifier. There is an internal comparator at COMP pin. If comp voltage is lower than 0.35 V, power stage stops switching to save power.

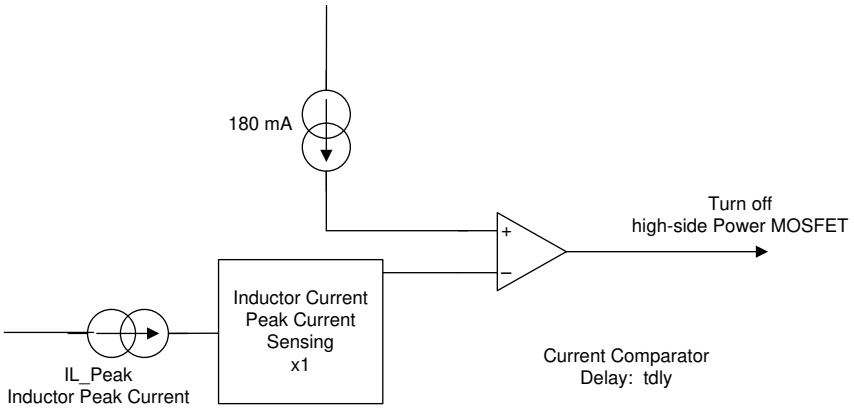


Figure 8-8. PSM Current Comparator

8.3.10 Slope Compensation

To prevent the sub-harmonic oscillations when the device operates at duty cycles greater than 50%, the device adds built-in slope compensation, which is a compensating ramp to the switch current signal.

8.3.11 Overcurrent Protection

The device is protected from over current conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

8.3.11.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle by cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference, the high-side switch is turned off.

8.3.11.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET can also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 256 switching cycles shown in Figure 8-9, the device will shut down itself and restart after the hiccup time of 8192 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent condition.

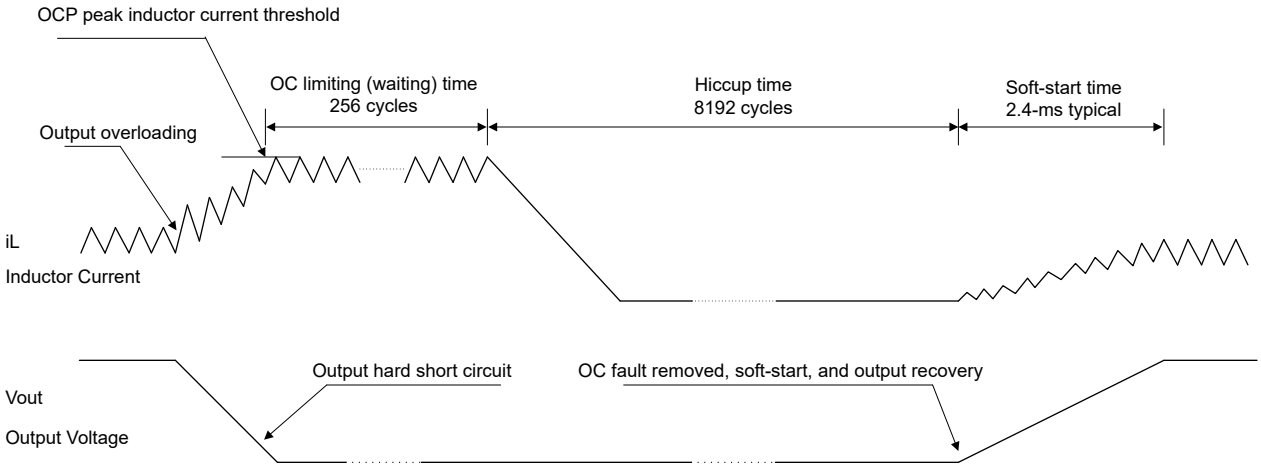


Figure 8-9. Overcurrent Protection

8.3.12 Adjustable Switching Frequency

The ROSC pin can be used to set the switching frequency by connecting a resistor to GND. The switching frequency of the device is adjustable from 250 kHz to 2.3 MHz.

To determine the switching frequency for a given ROSC resistance, use Equation 8 or the curve in Figure 8-10. To reduce the solution size one must set the switching frequency as high as possible, but tradeoffs of the supply efficiency and minimum controllable on time must be considered.

$$f_{osc}\,(kHz) = 30975 \times R_{osc}\,(k\Omega)^{-0.889} \quad (8)$$

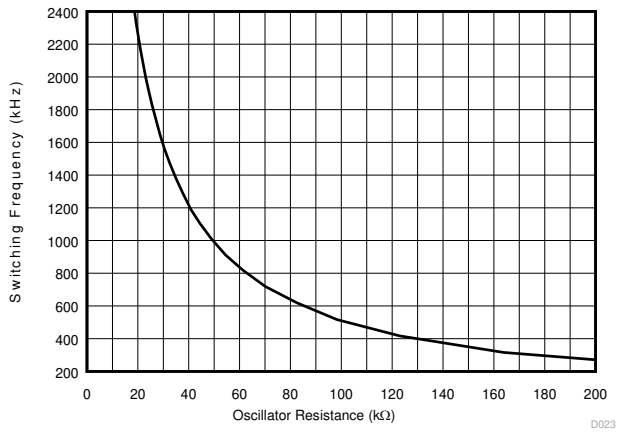


Figure 8-10. Switching Frequency versus ROSC

When an external clock applies to ROSC pin, the internal phase locked loop (PLL) has been implemented to allow internal clock synchronizing to an external clock between 250 kHz and 2.3 MHz. To implement the clock synchronization feature, connect a square wave clock signal to the ROSC pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.4 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of ROSC pin.

In applications where both resistor mode and synchronization mode are needed, the device can be configured as shown in Figure 8-11. Before an external clock is present, the device works in resistor mode and ROSC resistor sets the switching frequency. When an external clock is present, the synchronization mode overrides the resistor mode. The first time the ROSC pin is pulled above the ROSC high threshold (2.0 V), the device switches from the resistor mode to the Synchronization mode and the ROSC pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. TI does not recommend to switch from the synchronization mode back to the resistor mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by ROSC resistor.

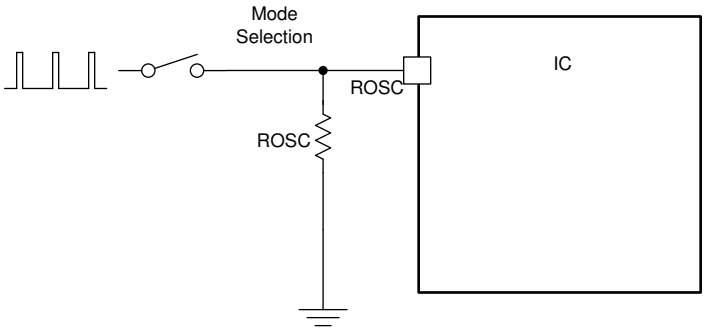


Figure 8-11. Works With Resistor Mode and Synchronization Mode

8.3.13 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 140°C typically.

8.4 Device Functional Modes

8.4.1 Operation With VIN < 4 V (Minimum VIN)

The device operates with input voltages above 4 V. The maximum UVLO voltage is 4 V and will operate at input voltages above 4 V. The typical UVLO voltage is 3.8 V and the device can operate at input voltages above that point. The device also can operate at lower input voltages, the minimum UVLO voltage is 3.6V (rising) and 3V (falling). At input voltages below the UVLO minimum voltage, the devices will not operate.

8.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.08 V minimum and 1.22 V maximum. With EN held below that voltage the device is disabled and switching is inhibited. The IC quiescent current is reduced in this state. When input voltage is above the UVLO threshold and the EN voltage is increased above the rising edge threshold, the device becomes active. Switching is enabled, and the internal soft-start sequence is initiated as shown in Figure 8-7 to Figure 9-5.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The device is triple synchronous step down dc/dc converter. It is typically used to convert a higher dc voltage to lower dc voltages with continuous available output current of 5 A/3 A/2 A. .

9.2 Typical Application

The following design procedure can be used to select component values for the TPS65265. This section presents a simplified discussion of the design process

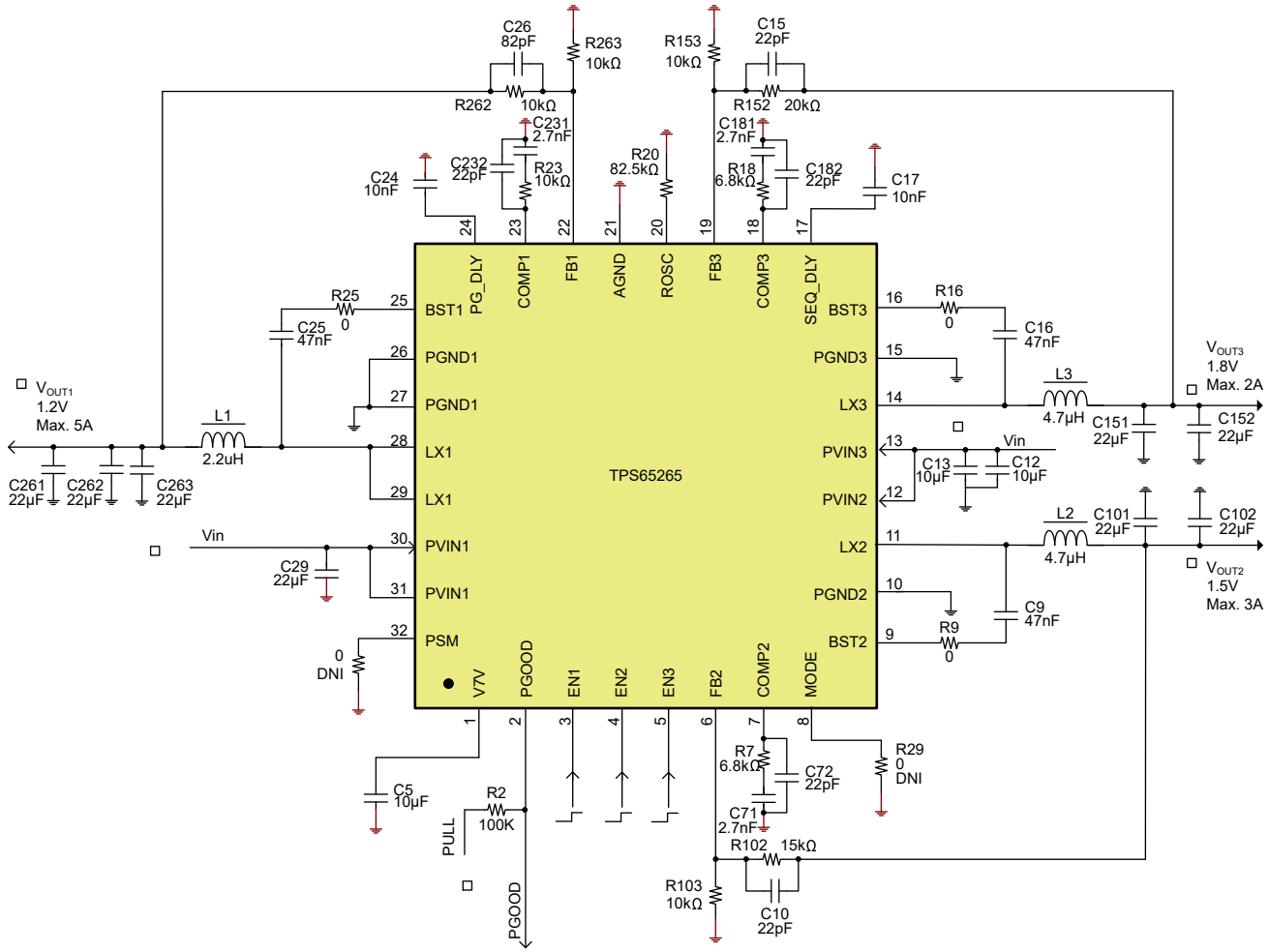


Figure 9-1. Typical Application Circuit

9.2.1 Design Requirements

This example details the design of triple synchronous step-down converter. A few parameters must be known to start the design process. These parameters are typically determined at the system level. For this example, start with the following known parameters shown in Table 9-1.

Table 9-1. Design Parameters

PARAMETER	VALUE
Vout1	1.2 V
Iout1	5 A
Vout2	1.5 V
Iout2	3 A
Vout3	1.8 V
Iout3	2 A
Transient response 1-A load step	±5%
Input voltage	12-V normal, 4.5 V to 17 V
Output voltage ripple	±1%
Switching frequency	610 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Output Inductor Selection

To calculate the value of the output inductor, use Equation 9. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, LIR is normally from 0.1 to 0.3 for the majority of applications.

$$L = \frac{V_{IN\ max} - V_{OUT}}{I_O \times LIR} \times \frac{V_{OUT}}{V_{IN\ max} \times f_{SW}} \tag{9}$$

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 11 and Equation 12.

$$I_{ripple} = \frac{V_{IN\ max} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN\ max} \times f_{SW}} \tag{10}$$

$$I_{Lrms} = \sqrt{I_O^2 + \frac{\left(\frac{V_{OUT} \times (V_{IN\ max} - V_{OUT})}{V_{IN\ max} \times L \times f_{SW}}\right)^2}{12}} \tag{11}$$

$$I_{Lpeak} = I_{OUT} + \frac{I_{ripple}}{2} \tag{12}$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

9.2.2.2 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator cannot. This situation must occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 13 shows the minimum output capacitance necessary to accomplish this.

$$C_O = \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \tag{13}$$

where

- ΔI_{out} is the change in output current
- f_{sw} is the regulators switching frequency
- ΔV_{out} is the allowable change in the output voltage.

Equation 14 calculates the minimum output capacitance needed to meet the output voltage ripple specification.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{Oripple}}{I_{Oripple}}} \tag{14}$$

where

- f_{sw} is the switching frequency.
- V_{ripple} is the maximum allowable output voltage ripple.
- I_{ripple} is the inductor ripple current.

Equation 15 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification.

$$R_{esr} < \frac{V_{Oripple}}{I_{Oripple}} \tag{15}$$

Additional capacitance de-ratings for aging, temperature and DC bias must be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Equation 16 can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{Lrms} = \frac{V_{OUT} \times \left(V_{IN\ max} - V_{OUT}\right)}{\sqrt{12} \times V_{IN\ max} \times L \times f_{SW}} \tag{16}$$

9.2.2.3 Input Capacitor Selection

The TPS65265 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance on the PVIN input voltage pins. In some applications additional bulk capacitance can also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of The TPS65265. The input ripple current can be calculated using Equation 17.

$$I_{INrms} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN\ min}} \times \frac{(V_{IN\ min} \times V_{OUT})}{V_{IN\ min}}} \tag{17}$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 18.

$$\Delta V_{IN} = \frac{I_{OUT\,max} \times 0.25}{C_{IN} \times f_{SW}} \tag{18}$$

9.2.2.4 Loop Compensation

The TPS65265 incorporates a peak current mode control scheme. The error amplifier is a trans-conductance amplifier with a gain of 350 µS. A typical type II compensation circuit adequately delivers a phase margin between 30 and 90 degrees. Cb adds a high frequency pole to attenuate high frequency noise when needed. To calculate the external compensation components, follow the following steps.

1. Select switching frequency fsw that is appropriate for application depending on L and C sizes, output ripple, EMI, and so forth. Switching frequency between 600 kHz to 1 MHz gives best trade-off between performance and cost. To optimize efficiency, lower switching frequency is desired.
2. Set up crossover frequency, f_c, which is typically between 1/5 and 1/20 of f_{sw}.
3. R_C can be determined by

$$R_C = \frac{2\pi \times f_c \times V_o \times C_o}{G_{m\_EA} \times V_{ref} \times G_{m\_PS}} \tag{19}$$

   where

   - G_{m_EA} is the error amplifier gain (350 µS).
   - G_{m_PS} is the power stage voltage to current conversion gain (12 A/V).

4. Calculate C_C by placing a compensation zero at or before the dominant pole ($f_p = \frac{1}{C_o \times R_L \times 2\pi}$).

$$C_c = \frac{R_L \times C_o}{R_C} \tag{20}$$

5. Optional C_b can be used to cancel the zero from the ESR associated with C_O.

$$C_b = \frac{R_{ESR} \times C_o}{R_C} \tag{21}$$

6. Type III compensation can be implemented with the addition of one capacitor, C1. This allows for slightly higher loop bandwidths and higher phase margins. If used, C1 is calculated from Equation 22.

$$C_1 = \frac{1}{2\pi \times R_1 \times f_c} \quad (22)$$

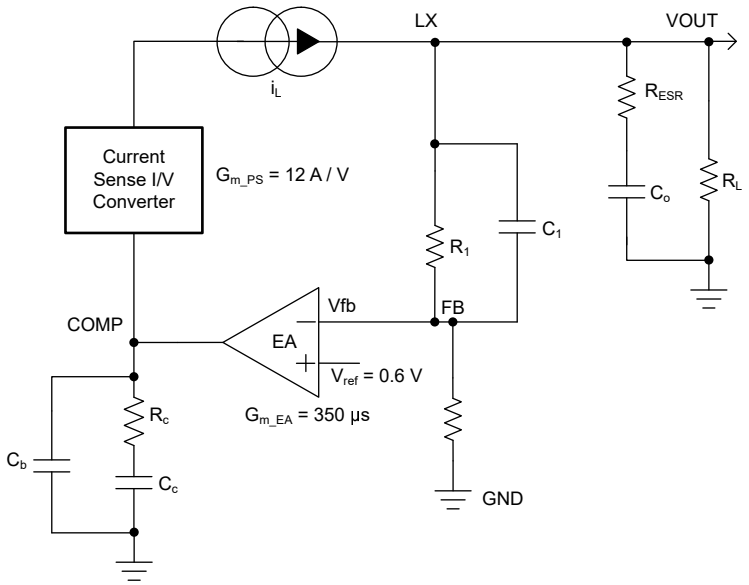


Figure 9-2. DC-DC Loop Compensation

9.2.3 Application Curves

T_A = 25°C, V_{IN} = 12 V, V_{OUT1} = 1.2 V, V_{OUT2} = 1.5 V, V_{OUT3} = 1.8 V F_{SW} = 610 kHz (unless otherwise noted)

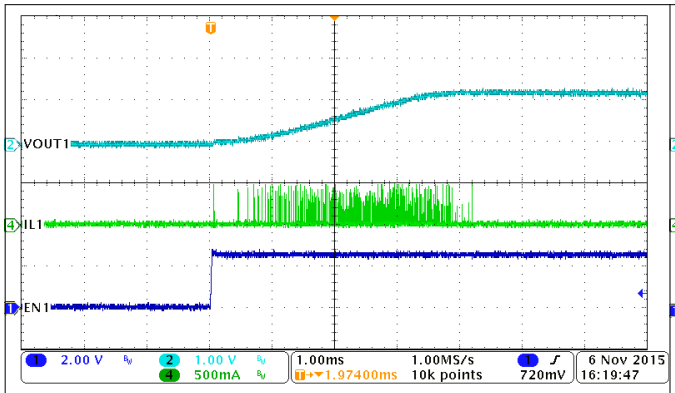


Figure 9-3. Buck1, PSM Mode, Soft-Start, Iout = 0 A

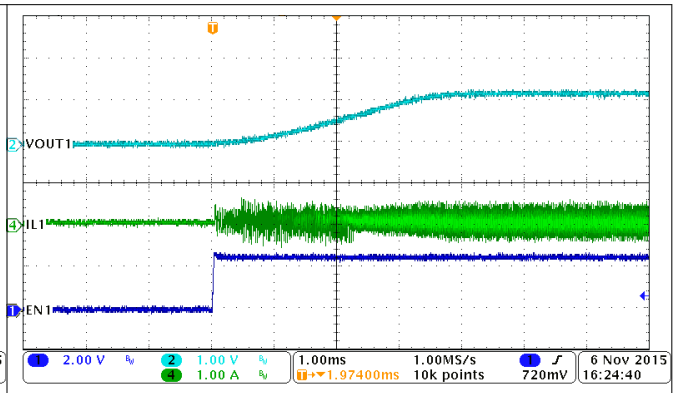


Figure 9-4. Buck1, FCC Mode, Soft-Start, Iout = 0 A

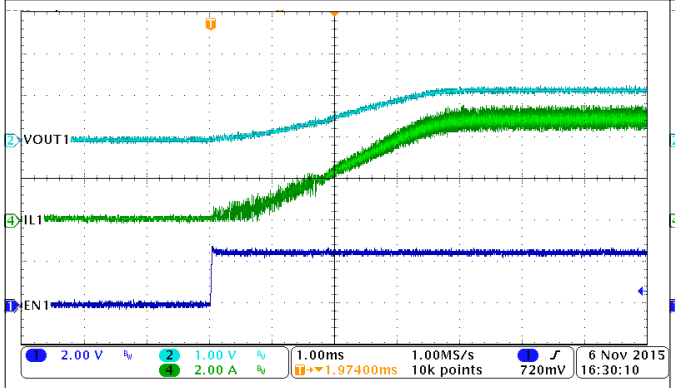


Figure 9-5. Buck1, PSM Mode, Soft-Start, Iout = 5 A

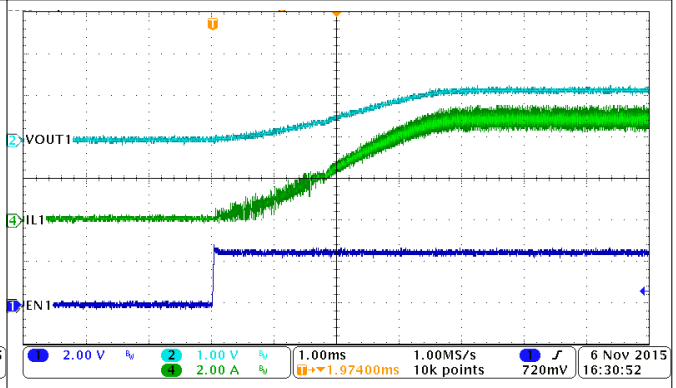


Figure 9-6. Buck1, FCC Mode, Soft-Start, Iout = 5 A

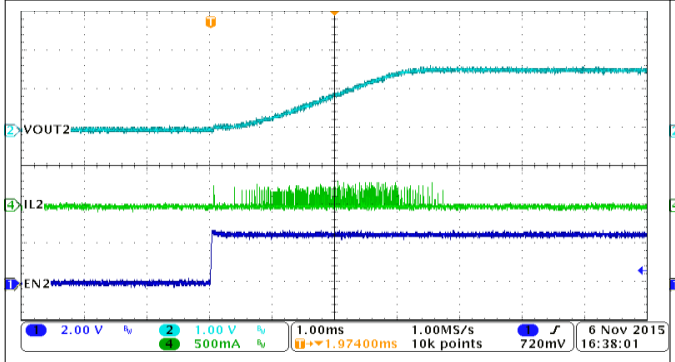


Figure 9-7. Buck2, PSM Mode, Soft-Start, Iout = 0 A

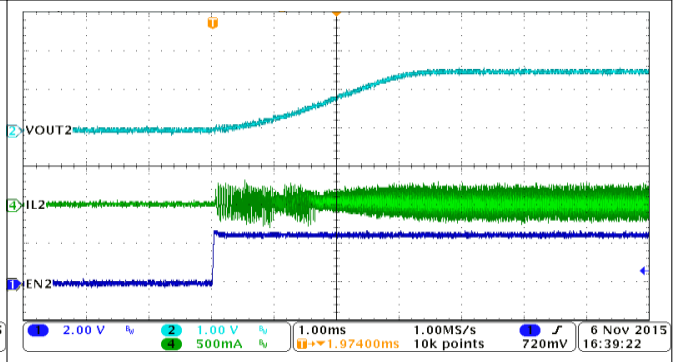


Figure 9-8. Buck2, FCC Mode, Soft-Start, Iout = 0 A

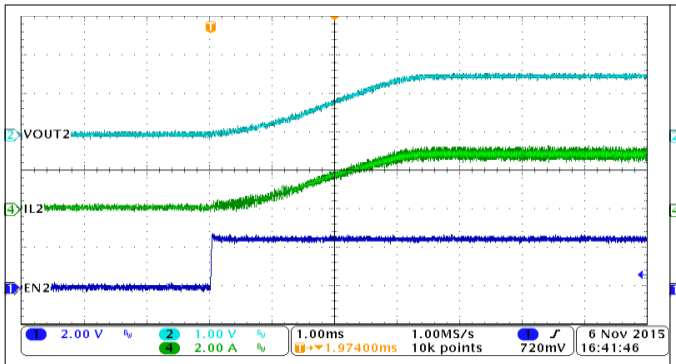


Figure 9-9. Buck2, PSM Mode, Soft-Start, Iout = 3 A

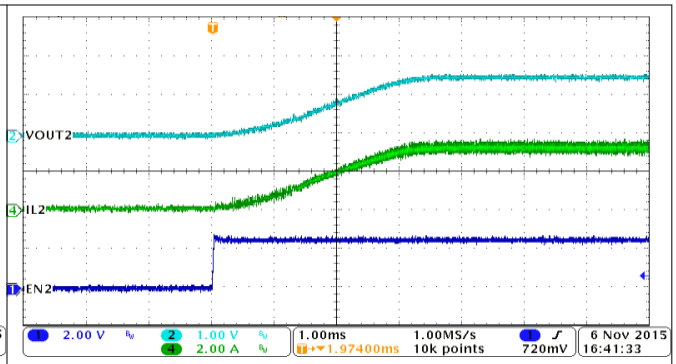


Figure 9-10. Buck2, FCC Mode, Soft-Start, Iout = 3 A

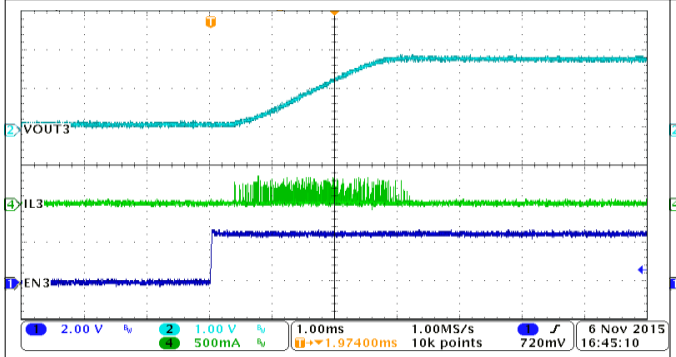


Figure 9-11. Buck3, PSM Mode, Soft-Start, Iout = 0 A

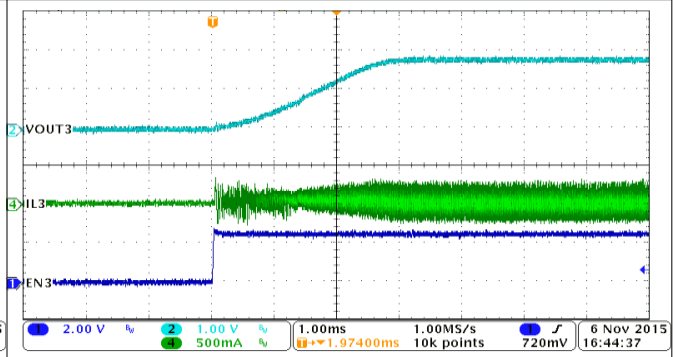


Figure 9-12. Buck3, FCC Mode, Soft-Start, Iout = 0 A

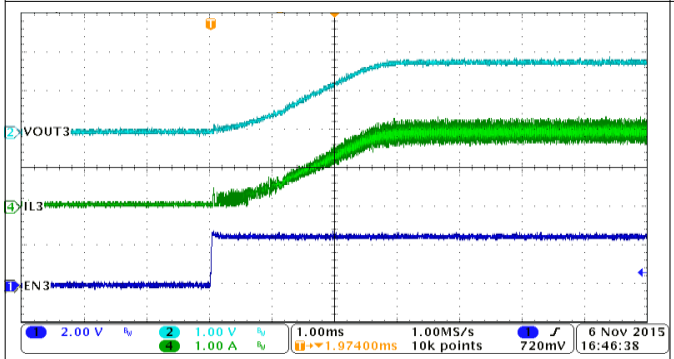


Figure 9-13. Buck3, PSM Mode, Soft-Start, Iout = 2 A

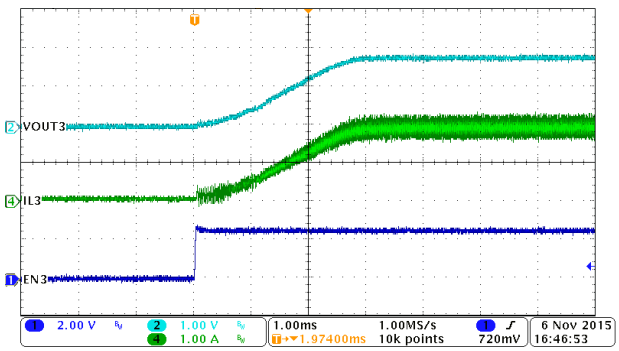


Figure 9-14. Buck3, FCC Mode, Soft-Start, Iout = 2 A

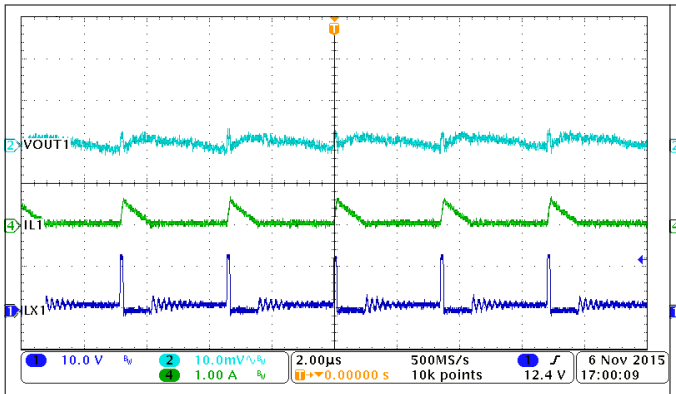


Figure 9-15. Buck1, PSM Mode, Output Ripple, Light Load

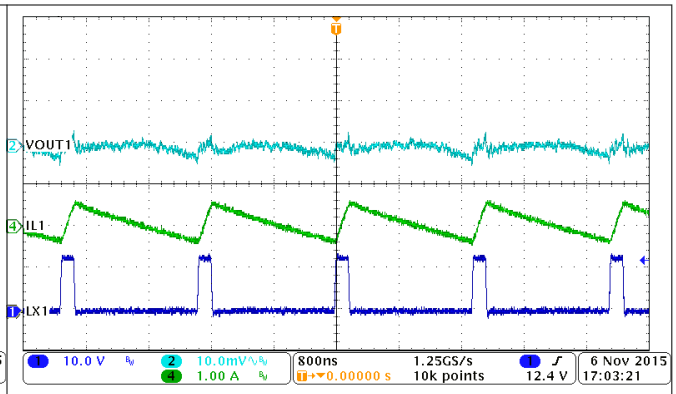


Figure 9-16. Buck1, FCC Mode, Iout = 0 A

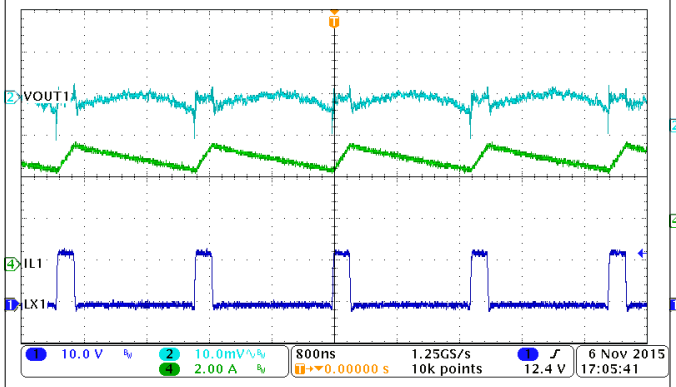


Figure 9-17. Buck1, Output Ripple, Iout = 5 A

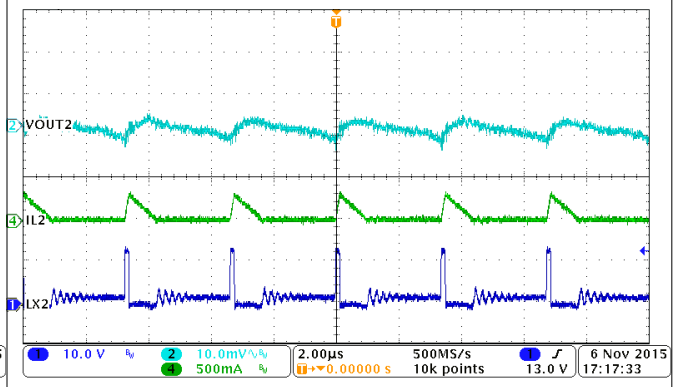


Figure 9-18. Buck2, PSM Mode, Output Ripple, Light Load

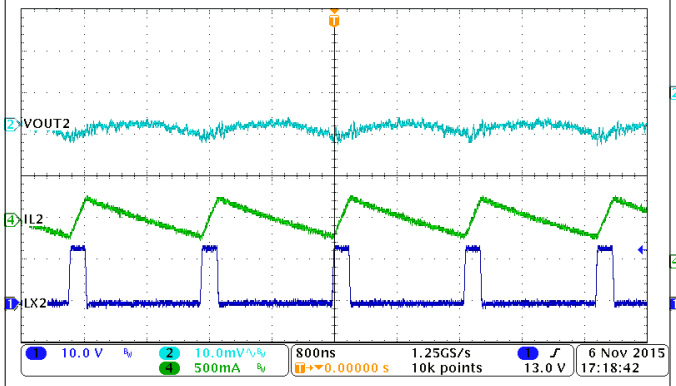


Figure 9-19. Buck2, FCC Mode, Iout = 0 A

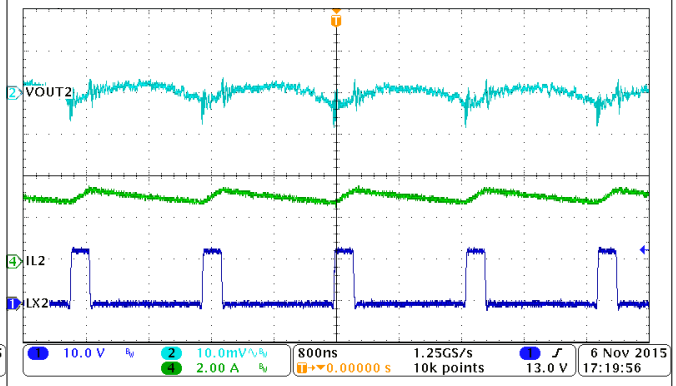


Figure 9-20. Buck2, Output Ripple, Iout = 3 A

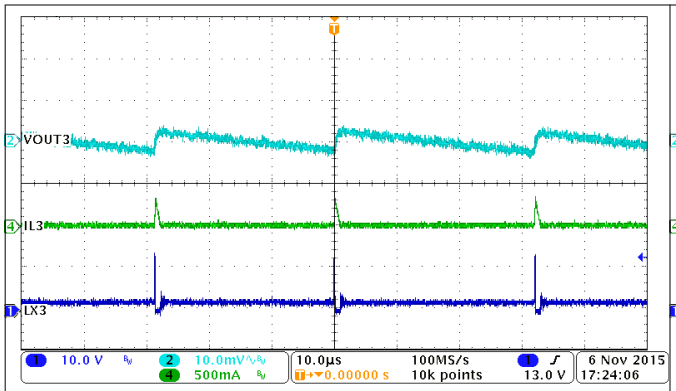


Figure 9-21. Buck3, PSM Mode, Output Ripple, Light Load

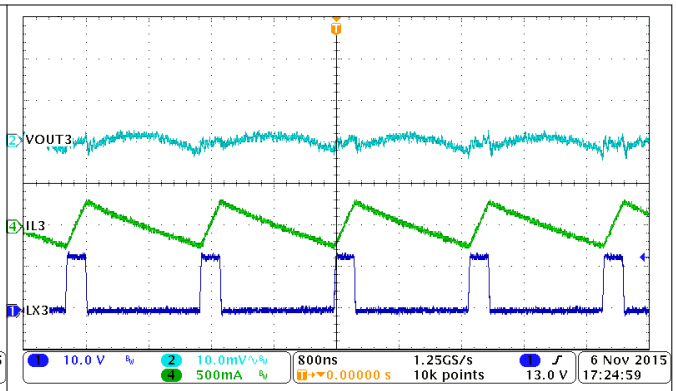


Figure 9-22. Buck3, FCC Mode, Iout = 0 A

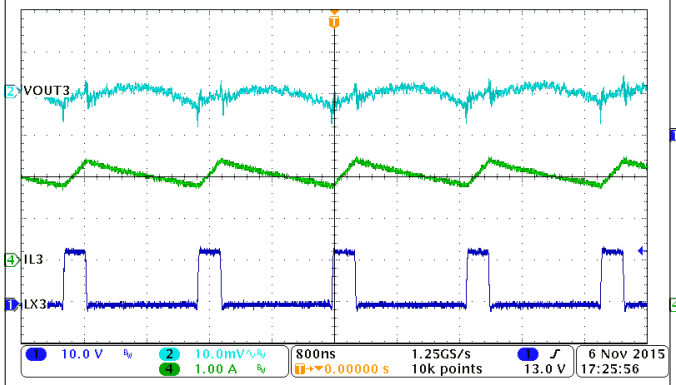


Figure 9-23. Buck3, Output Ripple, Iout = 2 A

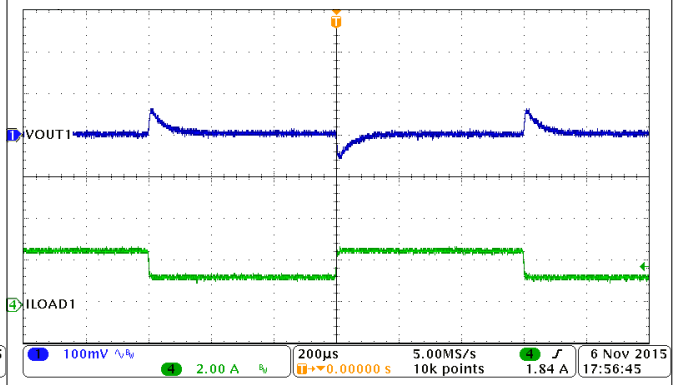


Figure 9-24. Buck1, Load Transient, 1.25 A to 2.5 A, SR 0.25 A/µs

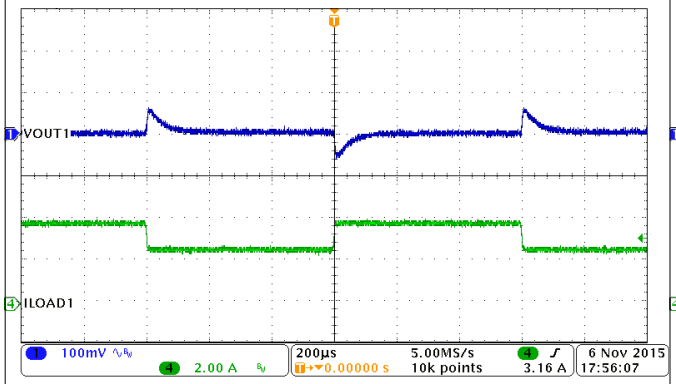


Figure 9-25. Buck1, Load Transient, 2.5 A to 3.75 A, SR 0.25 A/µs

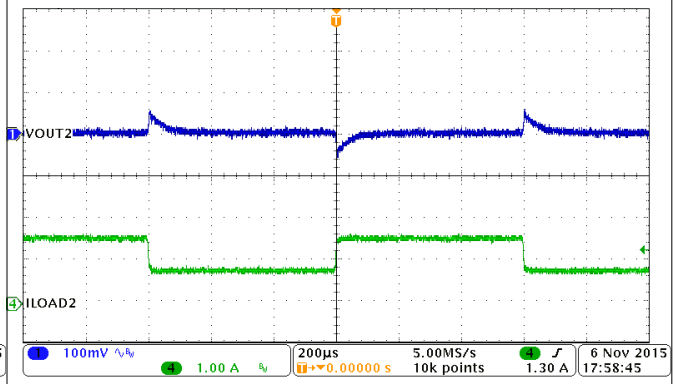


Figure 9-26. Buck2, Load Transient, 0.75 A to 1.5 A, SR 0.25 A/µs

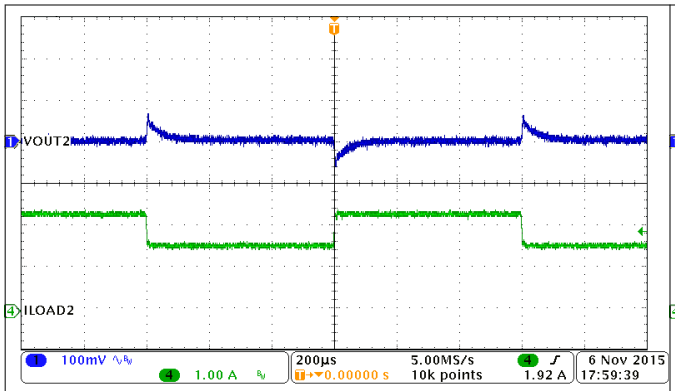


Figure 9-27. Buck2, Load Transient, 1.5 A to 2.25 A, SR 0.25 A/µs

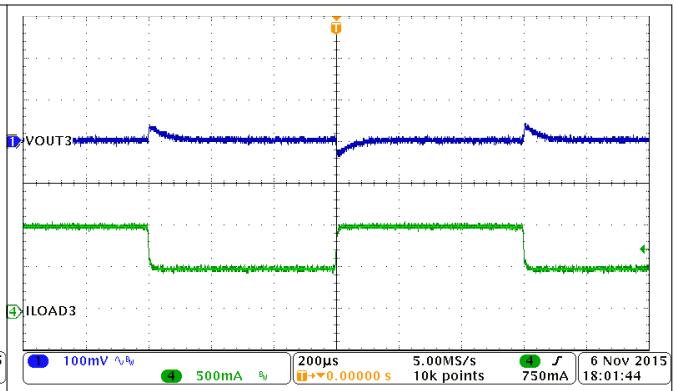


Figure 9-28. Buck3, Load Transient, 0.5 A to 1 A, SR 0.25 A/µs

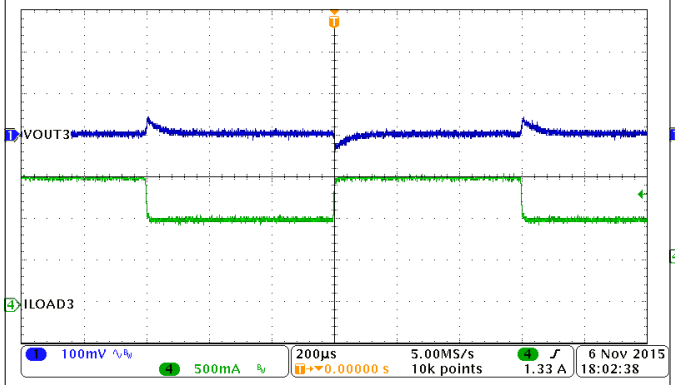


Figure 9-29. Buck3, Load Transient, 1 A to 1.5 A, SR 0.25 A/µs

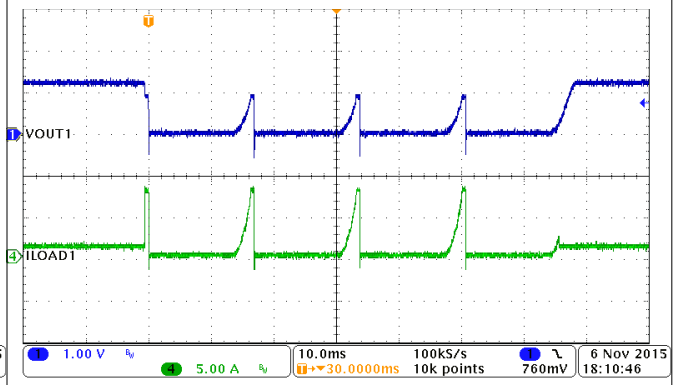


Figure 9-30. Buck1, Hiccup and Recovery

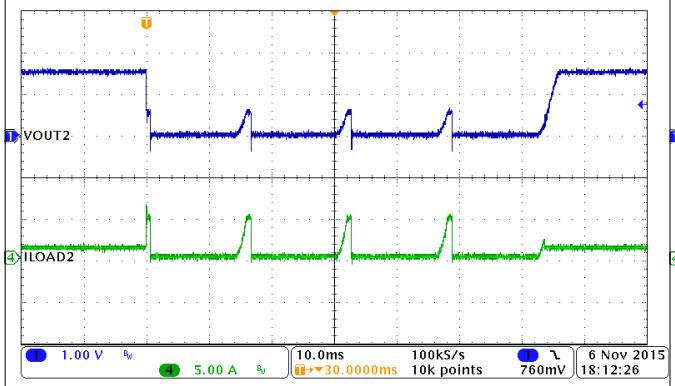


Figure 9-31. Buck2, Hiccup and Recovery

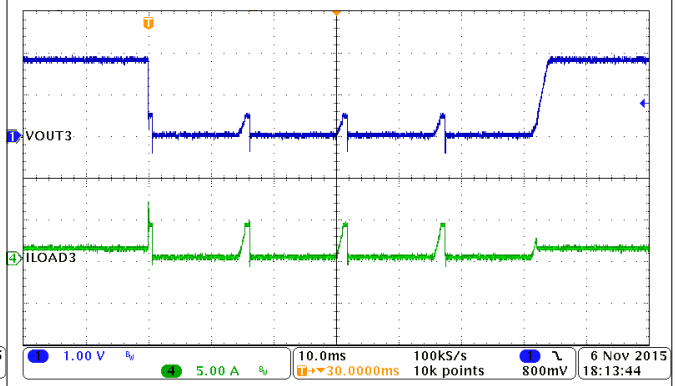


Figure 9-32. Buck3, Hiccup and Recovery

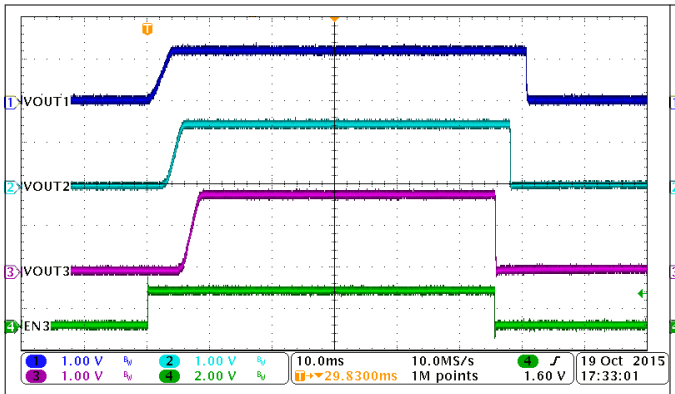


Figure 9-33. Automatic Power Sequencing, MODE = LOW, EN1 = HIGH, EN2 = HIGH

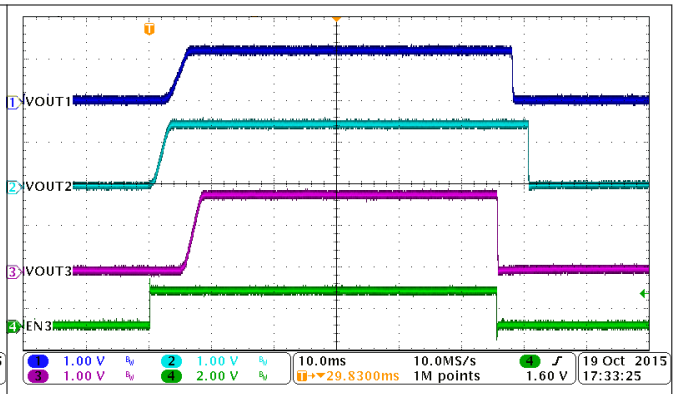


Figure 9-34. Automatic Power Sequencing, MODE = LOW, EN1 = LOW, EN2 = HIGH

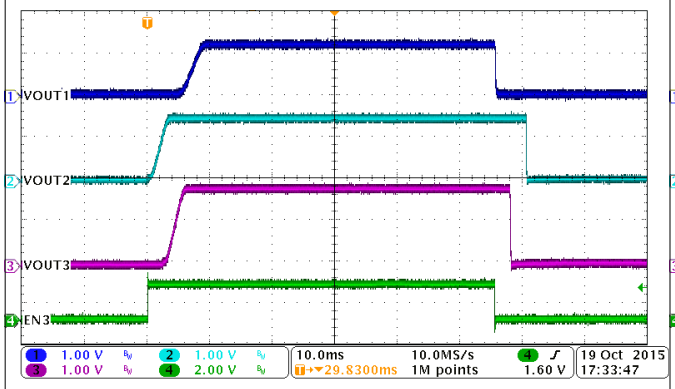


Figure 9-35. Automatic Power Sequencing, MODE = LOW, EN1 = HIGH, EN2 = LOW

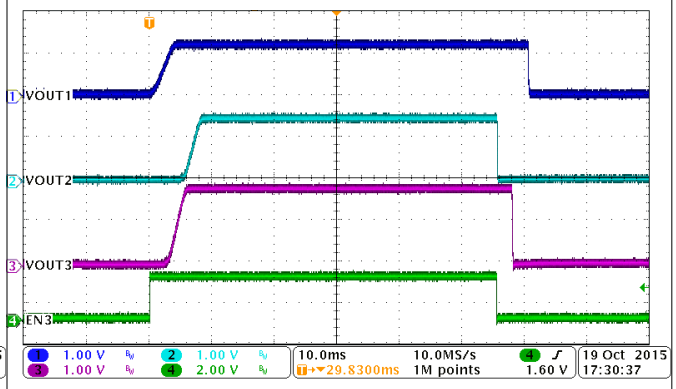


Figure 9-36. Automatic Power Sequencing, MODE = HIGH, EN1 = HIGH, EN2 = HIGH

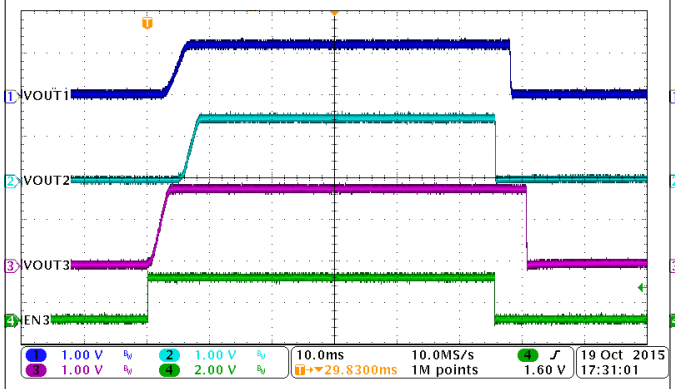


Figure 9-37. Automatic Power Sequencing, MODE = HIGH, EN1 = LOW, EN2 = HIGH

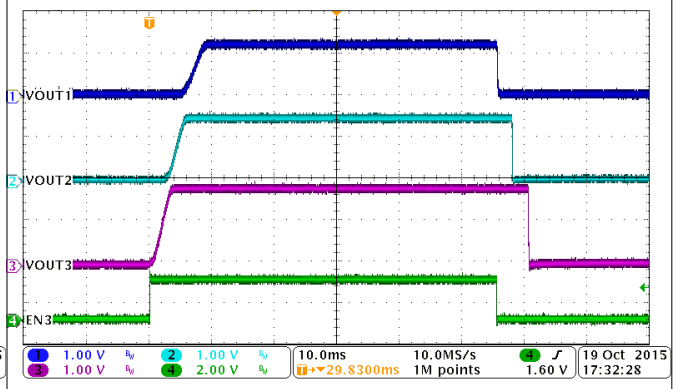


Figure 9-38. Automatic Power Sequencing, MODE = HIGH, EN1 = HIGH, EN2 = LOW

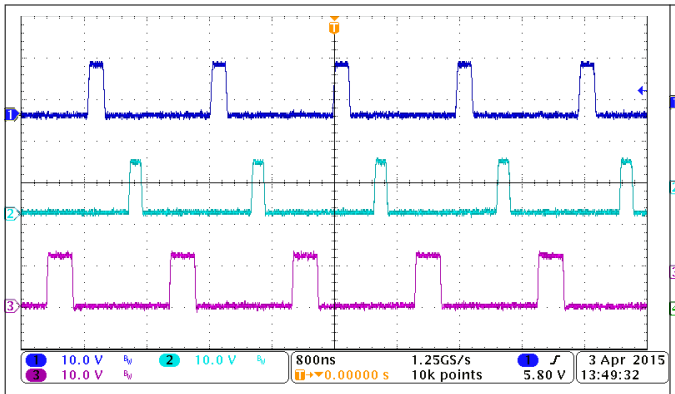


Figure 9-39. 120° Out of Phase for Buck1, Buck2, Buck3

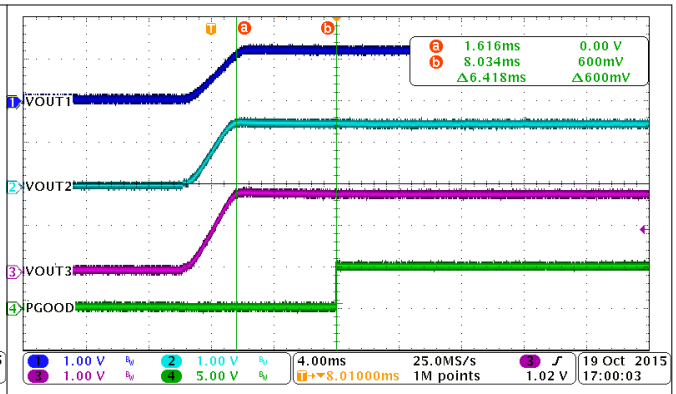


Figure 9-40. PGOOD Delay, C_{PG_DLY} = 10 nF

9.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4.5 V and 17 V. This input power supply must be well regulated. If the input supply is located more than a few inches from the TPS65265 converter additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

9.4 Layout

9.4.1 Layout Guidelines

The TPS65265 can be layout on 2-layer PCB, illustrated Figure 9-41.

Layout is a critical portion of good power supply design. See Figure 9-41 for a PCB layout example. The top contains the main power traces for PVIN, VOUT, and LX. Also on the top layer are connections for the remaining pins of the TPS65265 and a large top side area filled with ground. The top layer ground area must be connected to the bottom layer ground using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS65265 device to provide a thermal path from the exposed thermal pad land to ground. The bottom layer acts as ground plane connecting analog ground and power ground.

For operation at full rated load, the top-side ground area together with the bottom side ground plane must provide adequate heat dissipating area. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the PVIN pin must be bypassed to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric. Take care to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections. The PVIN pin must also be bypassed to ground using a low-ESR ceramic capacitor with X5R or X7R dielectric.

Because the LX connection is the switching node, the output inductor must be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground must use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components must be grounded to the analog ground path.

The FB and COMP pins are sensitive to noise so the resistors and capacitors must be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown.

9.4.2 Layout Example

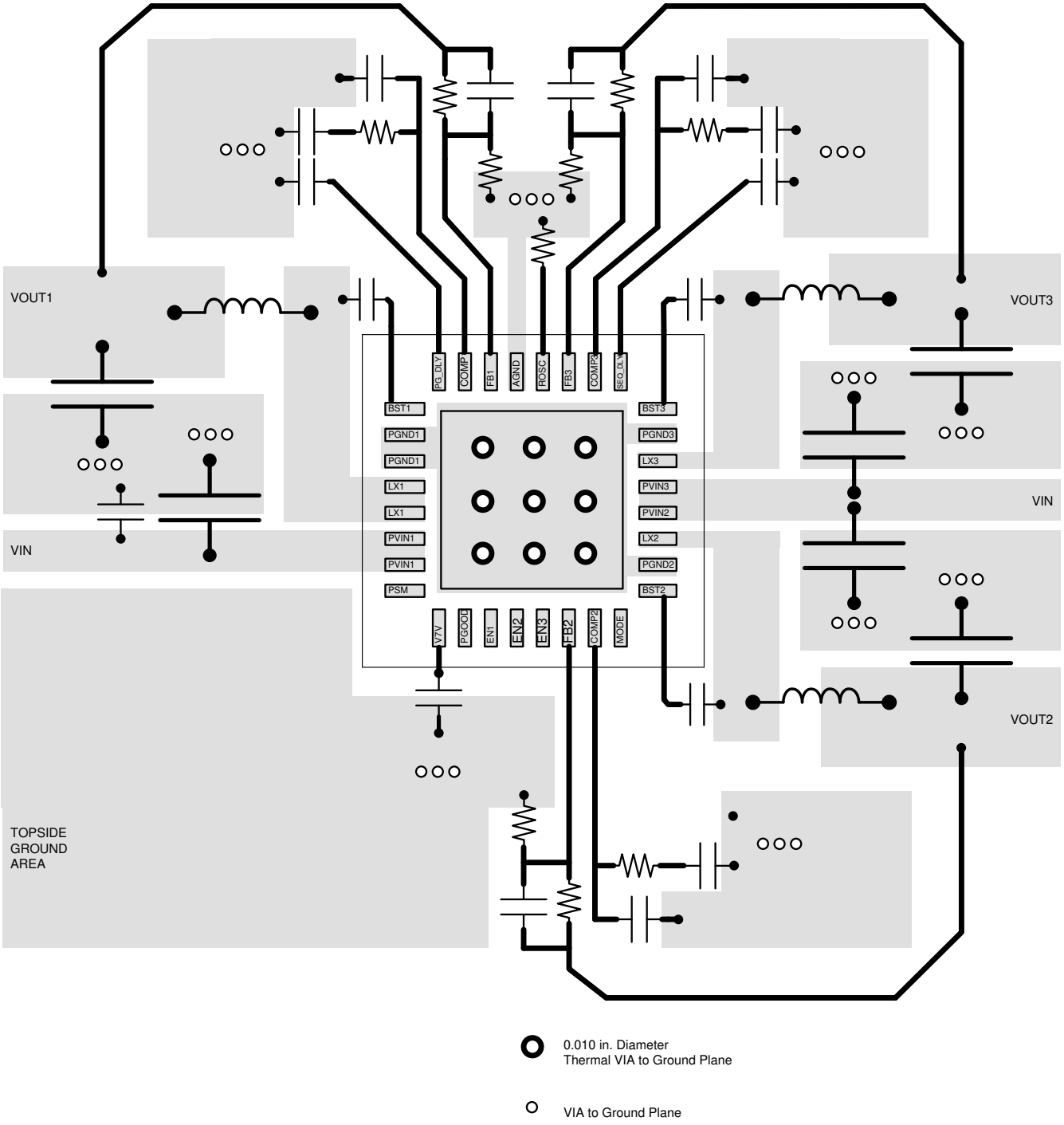


Figure 9-41. PCB Layout

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65265RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65265
TPS65265RHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65265
TPS65265RHBRG4	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65265
TPS65265RHBRG4.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65265
TPS65265RHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65265
TPS65265RHBT.A	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 65265

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

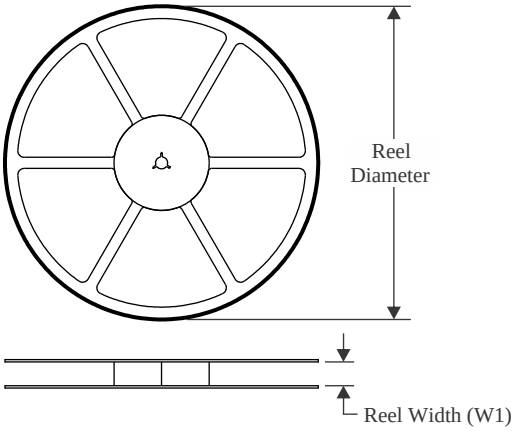
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

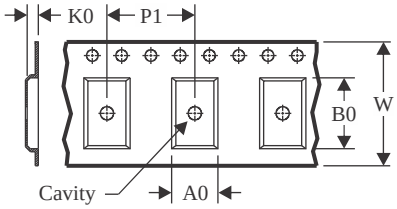
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

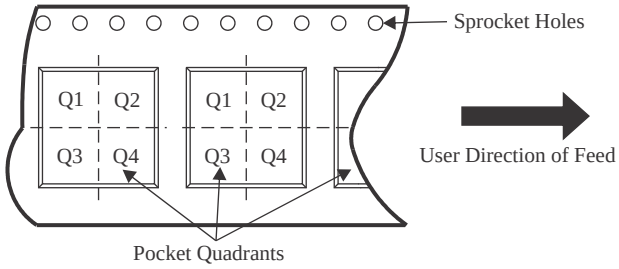


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

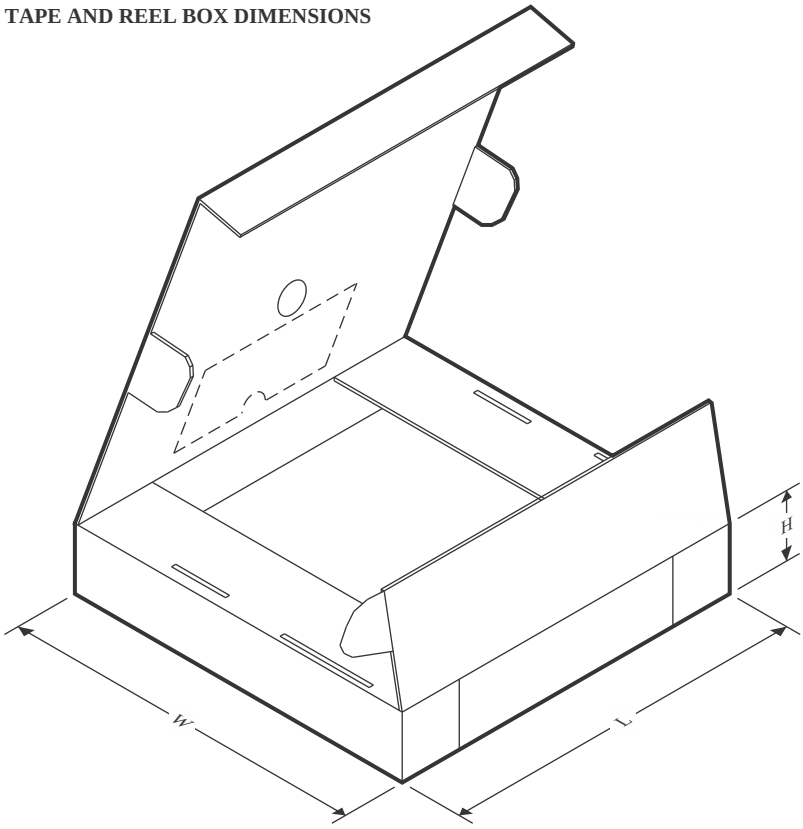
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65265RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65265RHBRG4	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65265RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65265RHBR	VQFN	RHB	32	3000	346.0	346.0	33.0
TPS65265RHBRG4	VQFN	RHB	32	3000	346.0	346.0	33.0
TPS65265RHBT	VQFN	RHB	32	250	182.0	182.0	20.0

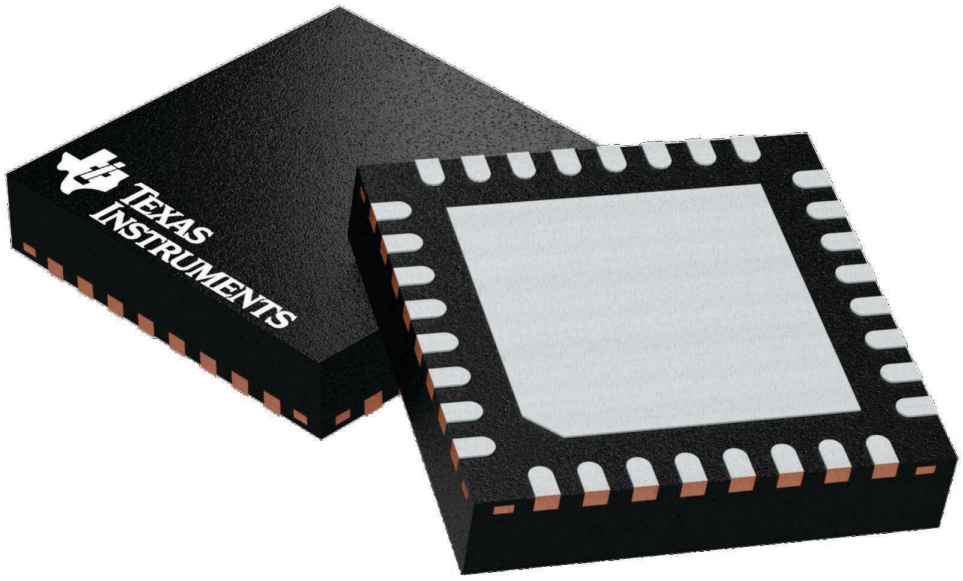
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

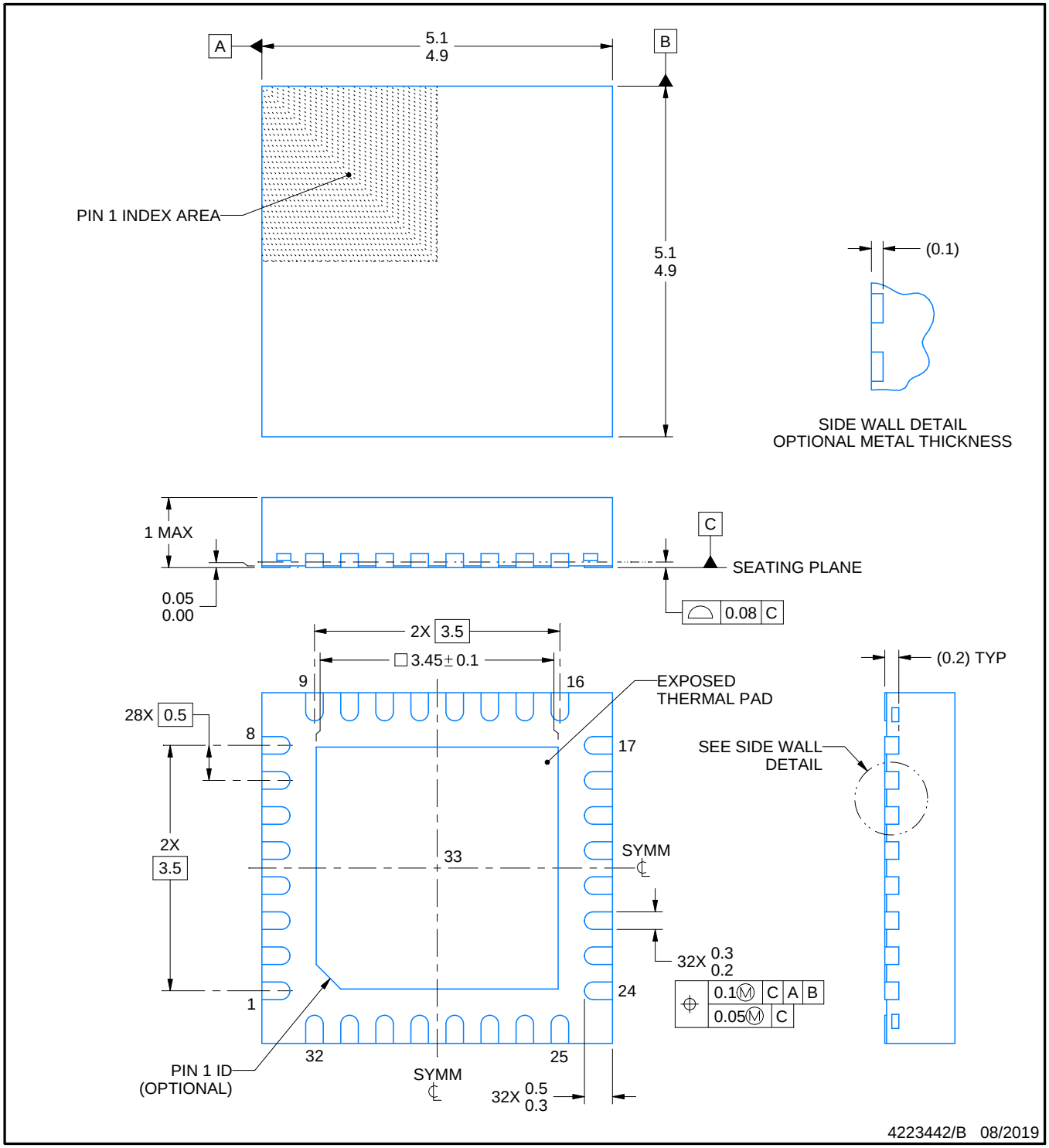
4224745/A

RHB0032E

PACKAGE OUTLINE

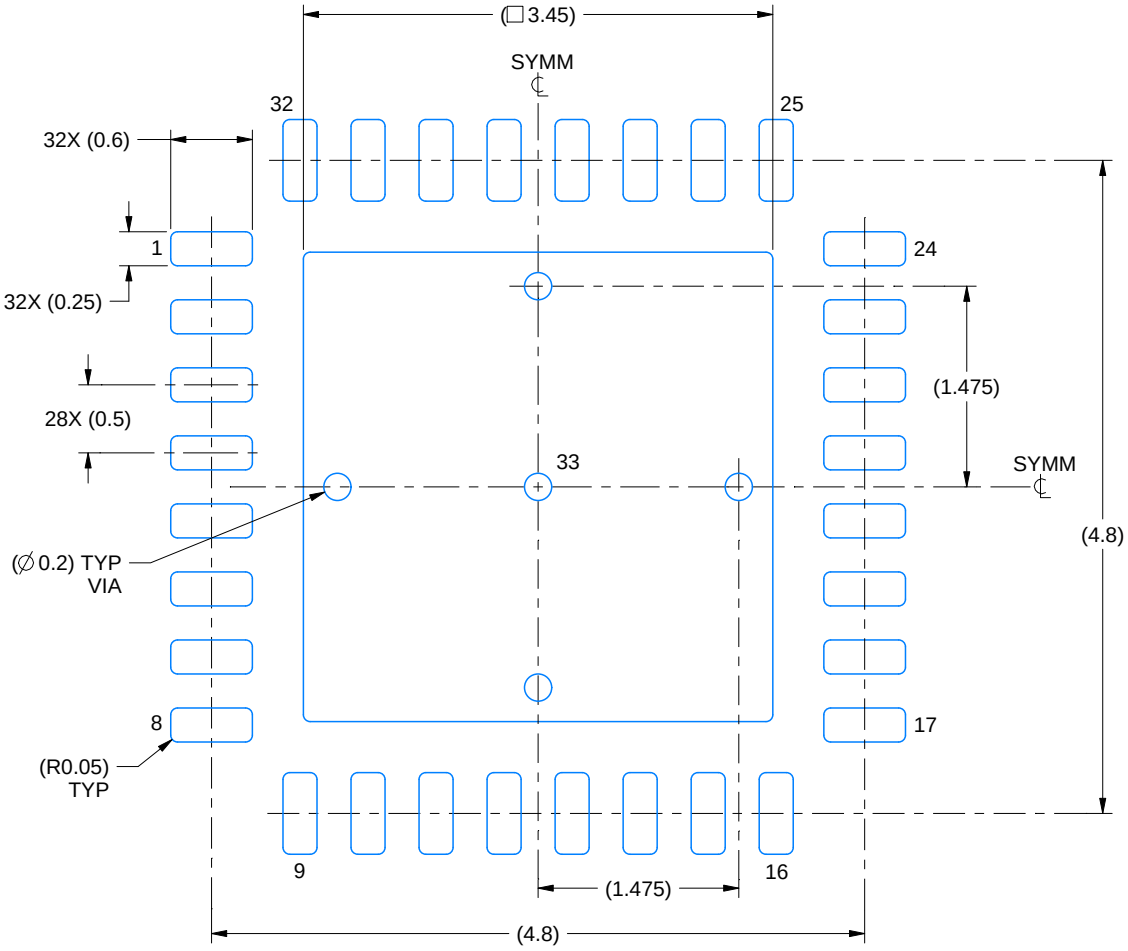
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

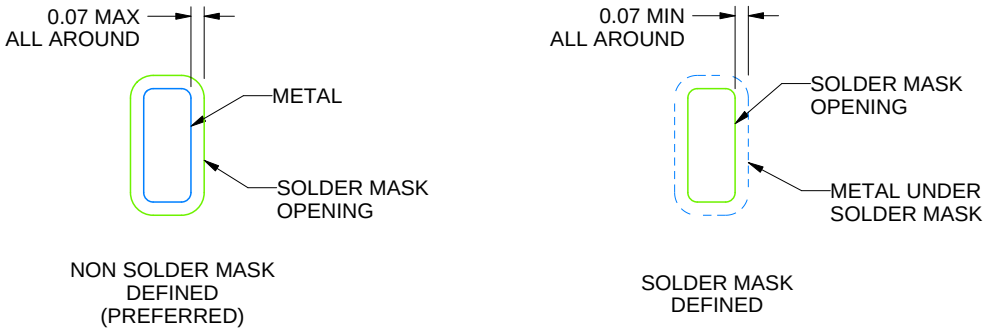


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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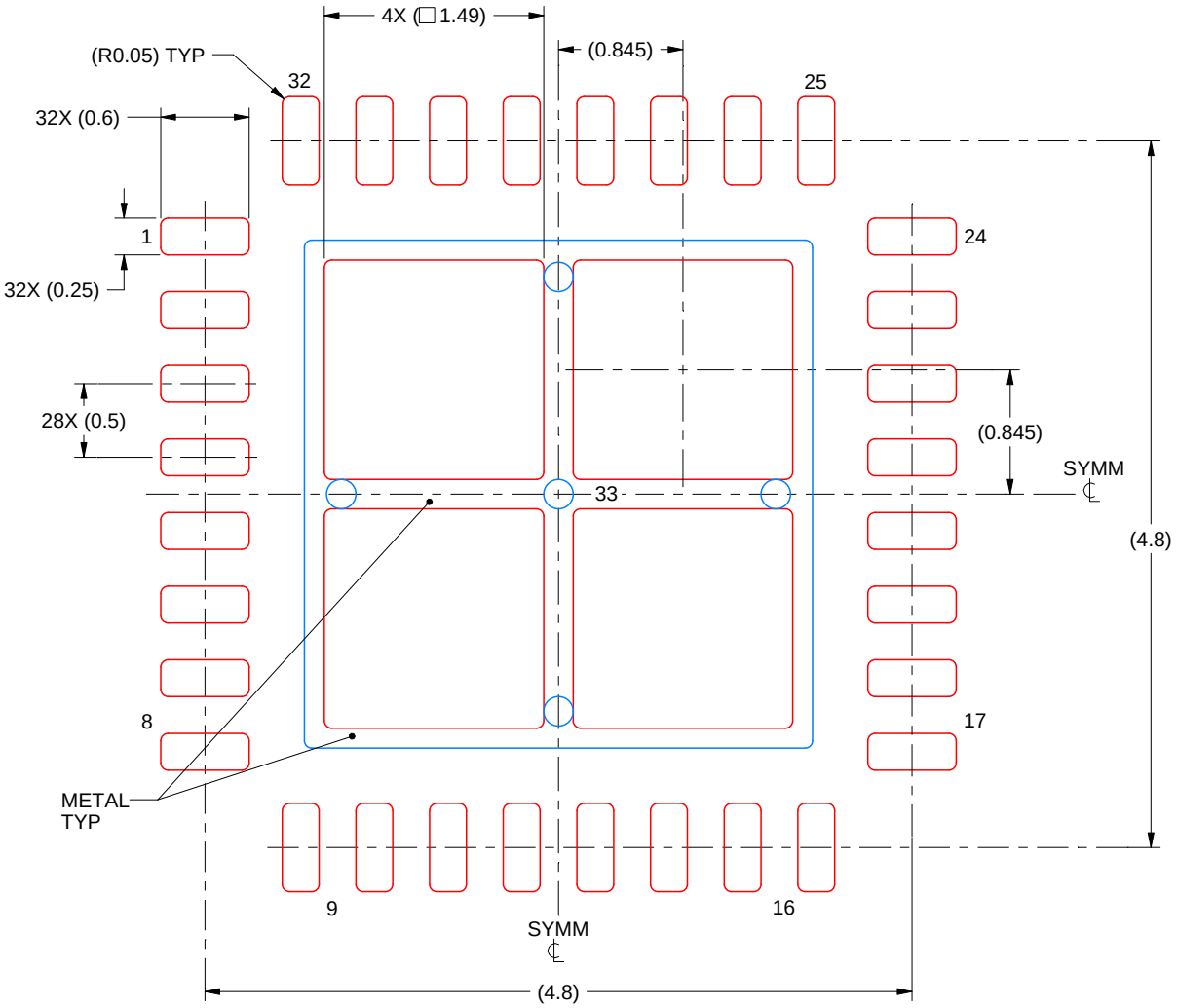
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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