TPS709-Q1 Automotive, 150mA, 30V, 1µA I_Q Voltage Regulator With Enable

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to 125°C, T_A
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Input voltage range: 2.7V to 30V
- Ultra-low I_Q: 1µA
- Reverse current protection
- Low $I_{SHUTDOWN}$: 150nA
- Supports 200mA peak output
- 2% accuracy over temperature
- Available in fixed-output voltages: 1.2V to 6.5V
- Thermal shutdown and overcurrent protection
- Packages: SOT-23-5, WSON-6

2 Applications

- Automotive
- Infotainment
- Body control modules
- Navigation systems

3 Description

The TPS709-Q1 series of linear regulators are ultra-low, quiescent current devices designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. Quiescent current of only 1µA makes these devices designed for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety.

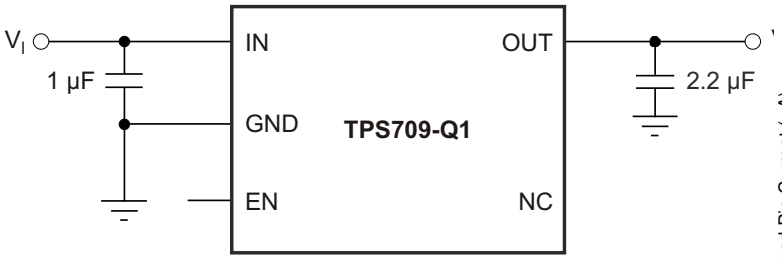
These regulators can be put into shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150nA, typical.

The TPS709-Q1 series is available in WSON-6 and SOT-23-5 packages.

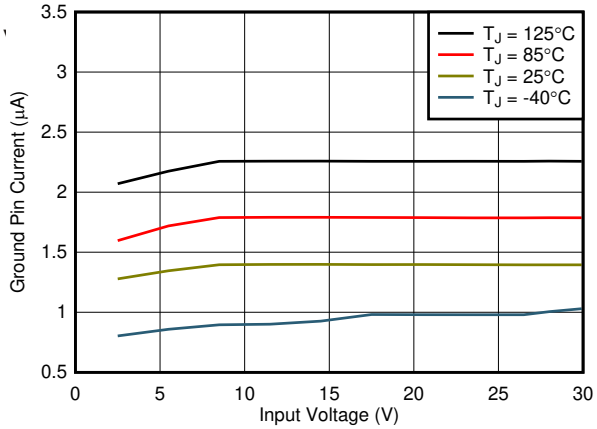
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS709-Q1	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DRV (WSON, 6)	2mm × 2mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit



GND Current vs V_{IN} and Temperature

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4 Pin Configuration and Functions

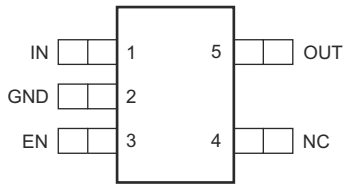


Figure 4-1. DBV Package, SOT-23-5 (Top View)

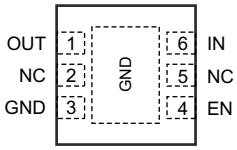


Figure 4-2. DRV Package, WSON-6 (Top View)

Table 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DRV	DBV		
EN	4	3	I	Enable pin. Driving this pin high enables the device. Driving this pin low puts the device into low current shutdown. This pin can be left floating to enable the device. The maximum voltage must remain below 6.5 V.
GND	3	2	—	Ground
IN	6	1	I	Unregulated input to the device
NC	2, 5	4	—	No internal connection
OUT	1	5	O	Regulated output voltage. Connect a small 2.2-µF or greater ceramic capacitor from this pin to ground to assure stability.
Thermal pad		—	—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings

specified at T_J = –40°C to 125°C, unless otherwise noted; all voltages are with respect to GND.(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	32	V
	V_{EN}	–0.3	7	V
	V_{OUT}	–0.3	7	V
Maximum output current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Junction temperature, T_J		–55	150	°C
Ambient temperature, T_A		–40	125	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		30	V
V_{OUT}	Output voltage	1.2		6.5	V
I_{OUT}	Output current	0		150	mA
V_{EN}	Enable voltage	0		6.5	V
C_{IN}	Input capacitor		1		µF
C_{OUT}	Output capacitor	2	2.2	47	µF
T_J	Operating junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS709-Q1				UNIT
		DBV (SOT-23-5)		DRV (WSON-6)		
		Legacy chip	New chip	Legacy chip	New chip	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.9	176.5	73.1	82.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	127.4	97.9	97.0	101.25	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.4	40.9	42.6	49.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.8	19.1	2.9	5.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	38.4	40.7	42.9	49.14	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	12.8	19.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

at –40°C ≤ T_J , T_A ≤ 125°C, V_{IN} = $V_{OUT(nom)}$ + 1V or 2.7V (whichever is greater), I_{OUT} = 1mA, V_{EN} = 2V, and C_{IN} = C_{OUT} = 2.2µF ceramic, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.7		30	V
V_{OUT}	Output voltage range		1.2		6.5	V
V_{OUT}	DC output accuracy	V_{OUT} < 3.3 V	–2		2	%
		V_{OUT} ≥ 3.3 V	–1		1	
ΔV_{OUT}	Line regulation	($V_{OUT(nom)}$ + 1 V, 2.7 V) ≤ V_{IN} ≤ 30 V		3	10	mV
	Load regulation	V_{IN} = $V_{OUT(typ)}$ + 1.5 V or 3 V (whichever is greater), 100 µA ≤ I_{OUT} ≤ 150 mA		20	50	
V_{DO}	Dropout voltage(1) (2)	TPS70933, I_{OUT} = 50 mA		295	650	mV
		TPS70933, I_{OUT}= 150 mA		975	1540	
		TPS70950, I_{OUT}= 50 mA		245	500	
		TPS70950, I_{OUT}= 150 mA		690	1200	
I_{CL}	Output current limit(3)	$_{VOUT}$= 0.9 × $V_{OUT(nom)}$	200	320	500	mA
I_{GND}	Ground pin current	I_{OUT}= 0 mA, V_{OUT} ≤ 3.3 V		1.3	2.55	µA
		I_{OUT}= 0 mA, V_{OUT} > 3.3 V		1.4	2.7	
		I_{OUT}= 100 µA, V_{IN} = 30 V		6.7	10	
		I_{OUT}= 150 mA		350		
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4 V, V_{IN} = 2.7 V		150		nA
PSRR	Power-supply rejection ratio	f = 10 Hz		80		dB
		f = 100 Hz		62		
		f = 1 kHz		52		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT}= 10 mA, V_{IN} = 2.7 V, V_{OUT} = 1.2 V		190		µVRMS
$V_{EN(HI)}$	Enable pin high-level input voltage	Device enabled	0.9			V
$V_{EN(LOW)}$	Enable pin low-level input voltage	Device disabled	0		0.4	V
I_{EN}	EN pin current	EN = 1.0 V, V_{IN} = 5.5 V		300		nA
I_{REV}	Reverse current (flowing out of IN pin)	V_{OUT} = 3 V, V_{IN} = V_{EN} = 0 V		10		nA
	Reverse current (flowing into OUT pin)	V_{OUT} = 3 V, V_{IN} = V_{EN} = 0 V		100		
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		158		°C
		Reset, temperature decreasing		140		
T_J	Operating junction temperature		–40		125	°C

(1) V_{DO} is measured with V_{IN} = 0.98 × $V_{OUT(nom)}$.
(2) Dropout is only valid when V_{OUT} ≥ 2.8V because of the minimum input voltage limits.
(3) Measured with V_{IN} = V_{OUT} + 3V for V_{OUT} ≤ 2.5V. Measured with V_{IN} = V_{OUT} + 2.5V for V_{OUT} > 2.5V.

5.6 Timing Requirements

at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1V or 2.7V (whichever is greater), R_L = 47Ω, V_{EN} = 2V, and C_{IN} = C_{OUT} = 2.2µF ceramic, unless otherwise noted. Typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-up time[1]	$V_{OUT(nom)}$ ≤ 3.3V		200	600	µs
		$V_{OUT(nom)}$ > 3.3V		500	1500	

(1) Startup time = time from EN assertion to 0.95 × $V_{OUT(nom)}$ and load = 47Ω.

5.7 Switching Characteristics

Specifications apply for T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.4V, whichever is greater, V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{STR}	Start-up time (V_{EN})	From V_{EN} > $V_{EN(HI)}$ to V_{OUT} = 95% of $V_{OUT(NOM)}$, 1V/us	From V_{EN} > $V_{EN(HI)}$ to V_{OUT} = 95% of $V_{OUT(NOM)}$, 1V/us		200		µs

5.8 Typical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

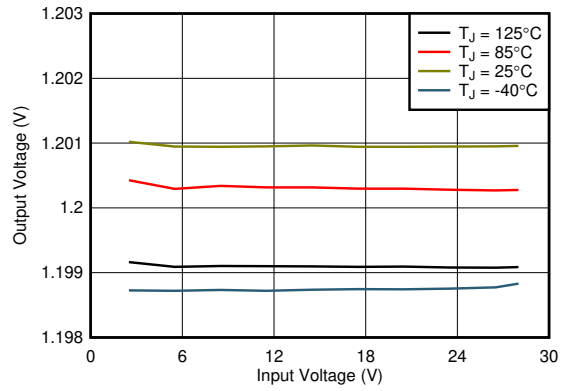


Figure 5-1. 1.2-V Line Regulation vs V_{IN} and Temperature

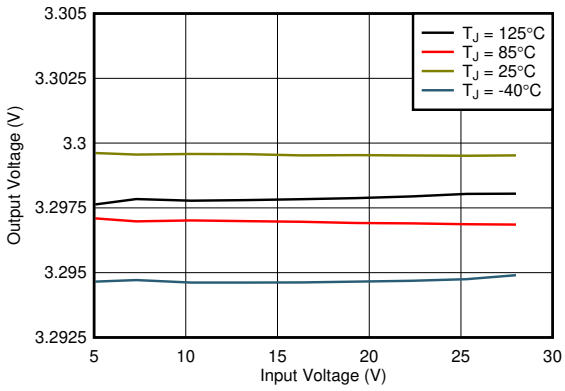


Figure 5-2. 3.3-V Line Regulation vs V_{IN} and Temperature

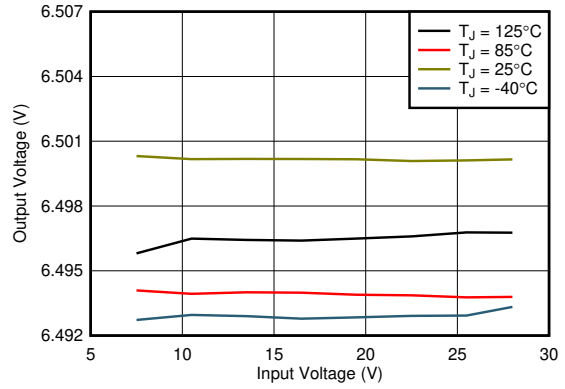


Figure 5-3. 6.5-V Line Regulation vs V_{IN} and Temperature

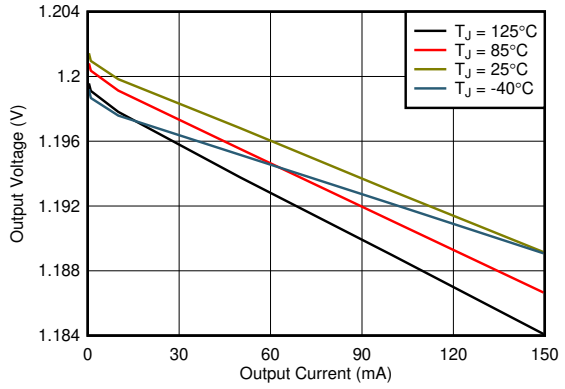


Figure 5-4. 1.2-V Load Regulation vs I_{OUT} and Temperature

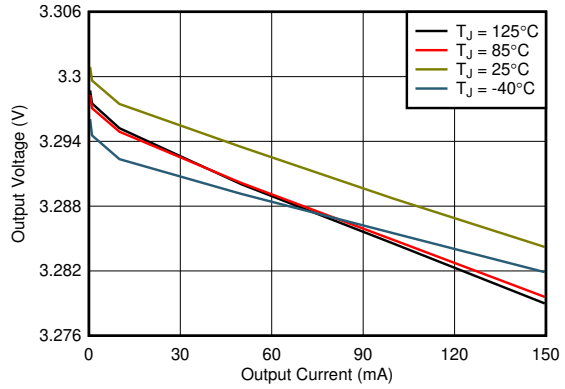


Figure 5-5. 3.3-V Load Regulation vs I_{OUT} and Temperature

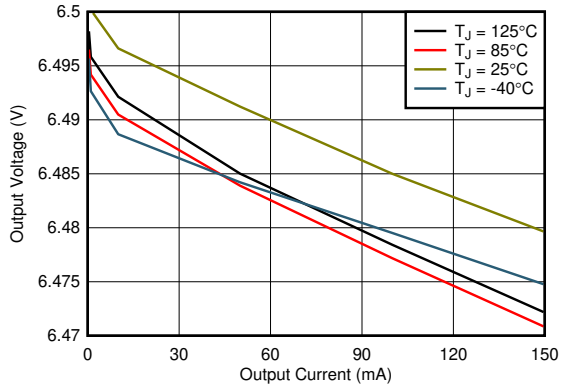


Figure 5-6. 6.5-V Load Regulation vs I_{OUT} and Temperature

5.8 Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

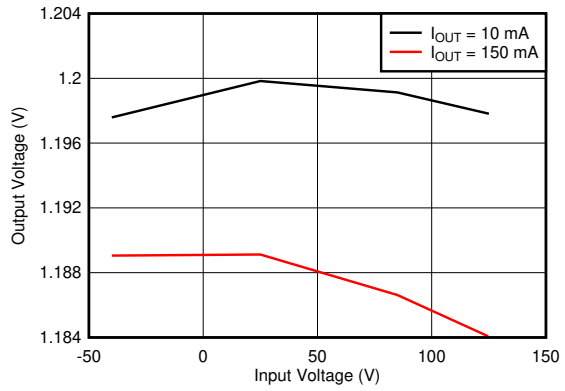


Figure 5-7. 1.2-V Output Voltage vs Temperature

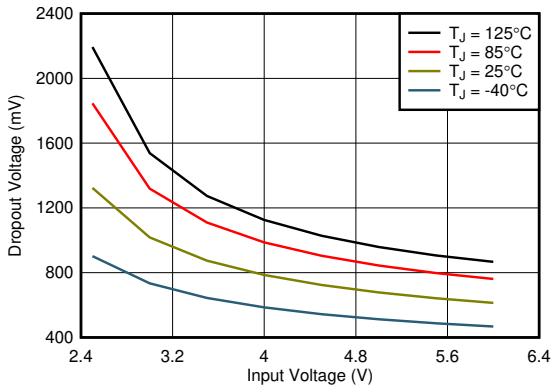


Figure 5-8. 6.5-V Dropout Voltage vs V_{IN} and Temperature

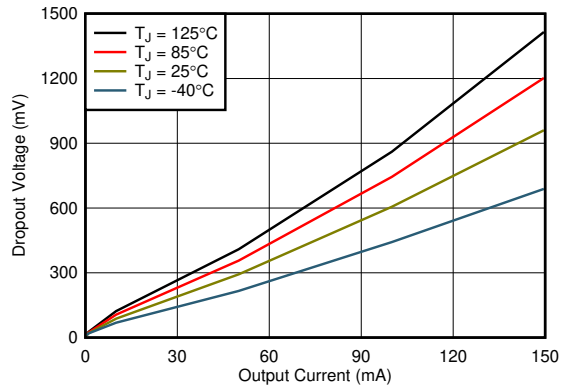


Figure 5-9. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

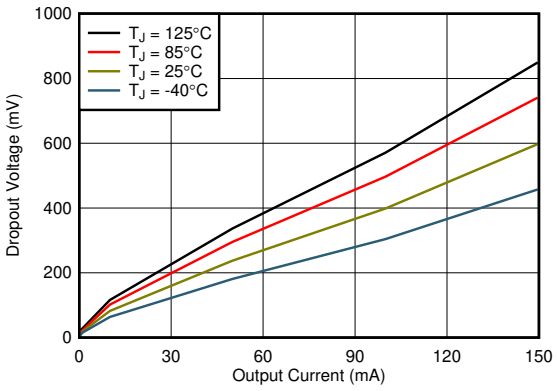


Figure 5-10. Dropout Voltage vs I_{OUT} and Temperature

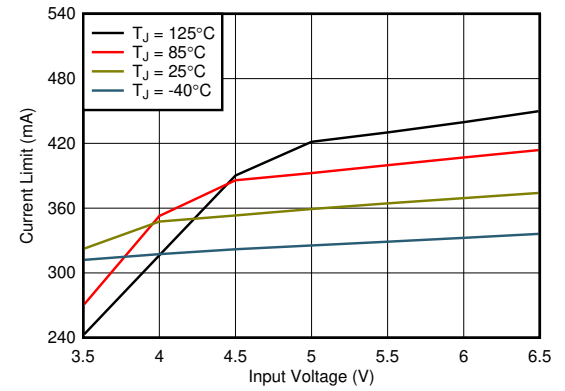


Figure 5-11. 1.2-V Current Limit vs V_{IN} and Temperature

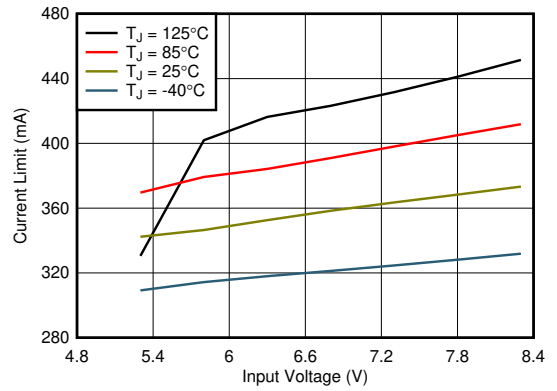


Figure 5-12. 3.3-V Current Limit vs V_{IN} and Temperature

5.8 Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

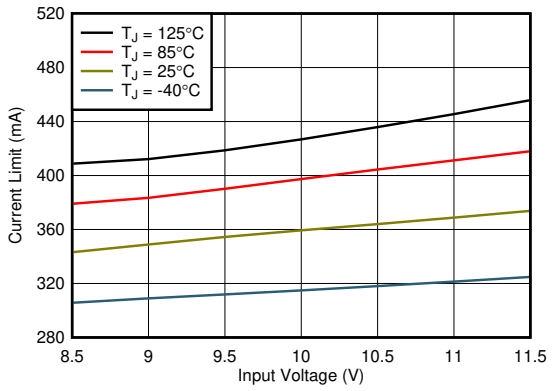


Figure 5-13. 6.5-V Current Limit vs V_{IN} and Temperature

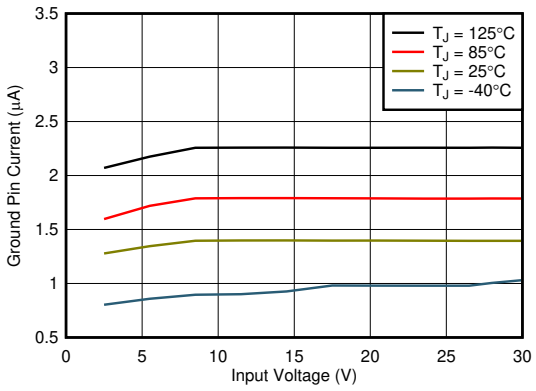


Figure 5-14. 1.2-V Ground Pin Current vs V_{IN} and Temperature

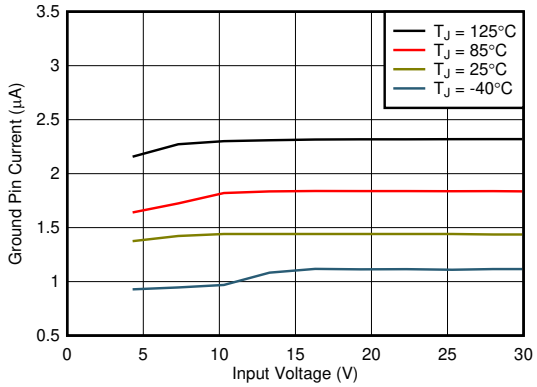


Figure 5-15. 3.3-V Ground Pin Current vs V_{IN} and Temperature

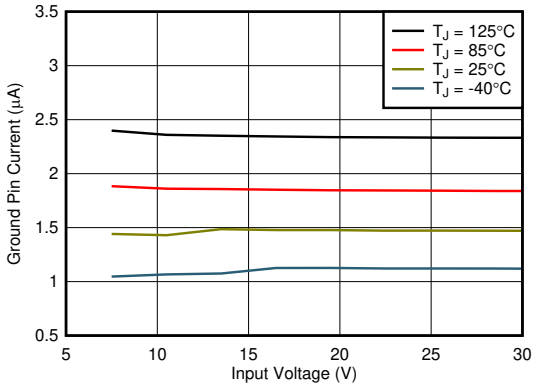


Figure 5-16. 6.5-V Ground Pin Current vs V_{IN} and Temperature

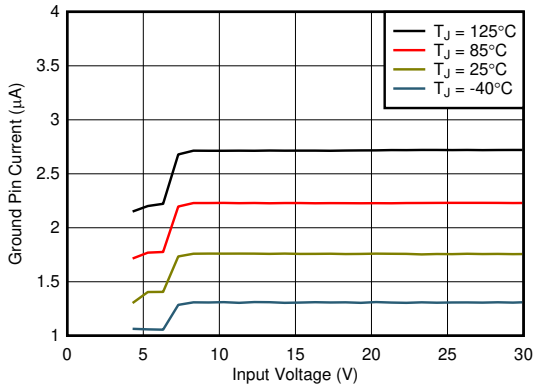


Figure 5-17. 3.3-V Ground Current vs V_{IN} and Temperature with EN Floating

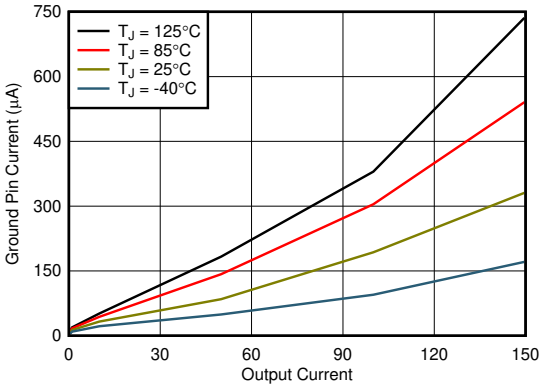


Figure 5-18. 1.2-V Ground Pin Current vs I_{OUT} and Temperature

5.8 Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

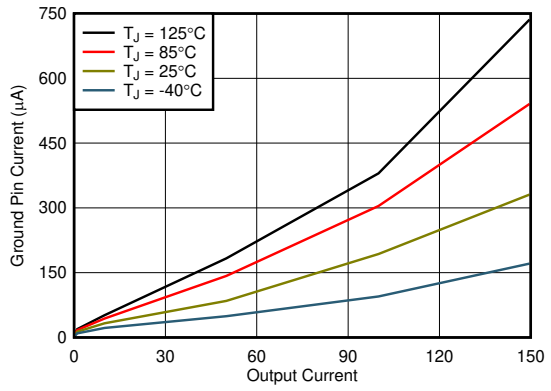


Figure 5-19. 3.3-V Ground Pin Current vs I_{OUT} and Temperature

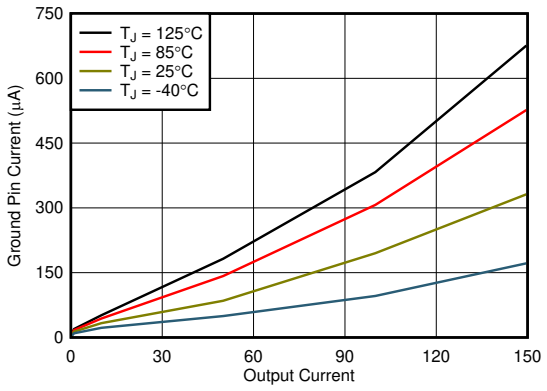


Figure 5-20. 6.5-V Ground Pin Current vs I_{OUT} and Temperature

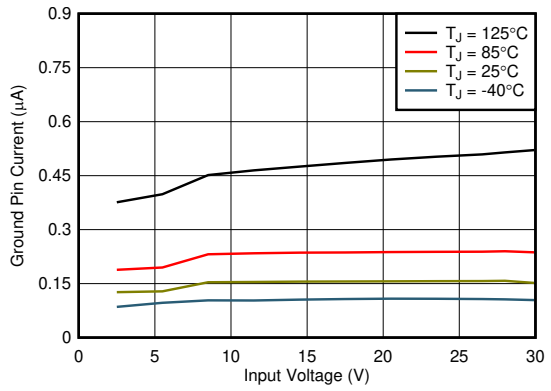


Figure 5-21. 1.2-V Shutdown Current vs V_{IN} and Temperature

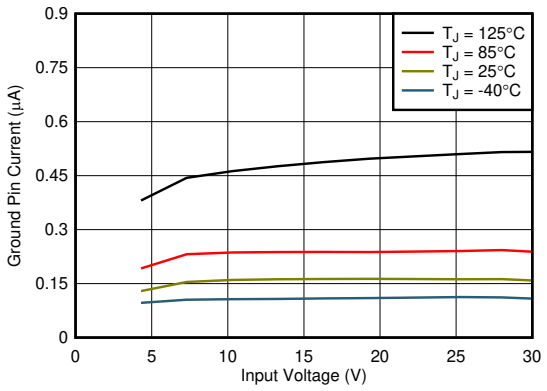


Figure 5-22. 3.3-V Shutdown Current vs V_{IN} and Temperature

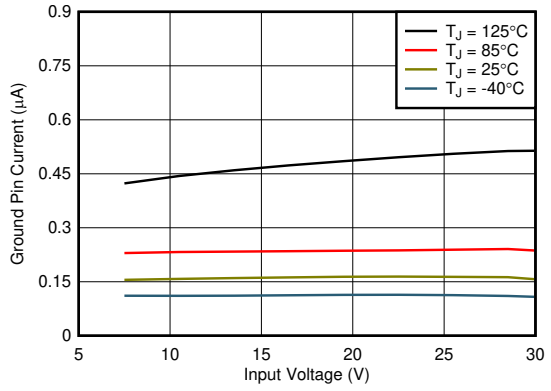


Figure 5-23. 6.5-V Shutdown Current vs V_{IN} and Temperature

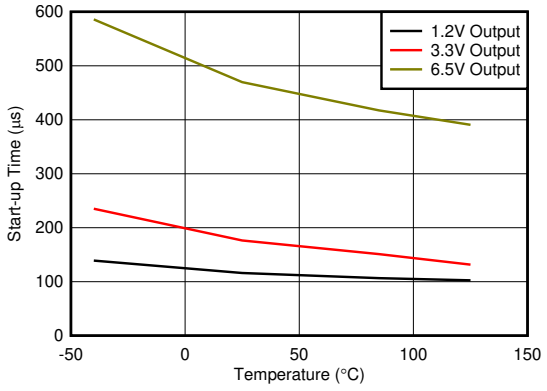


Figure 5-24. Start-Up Time vs Temperature

5.8 Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

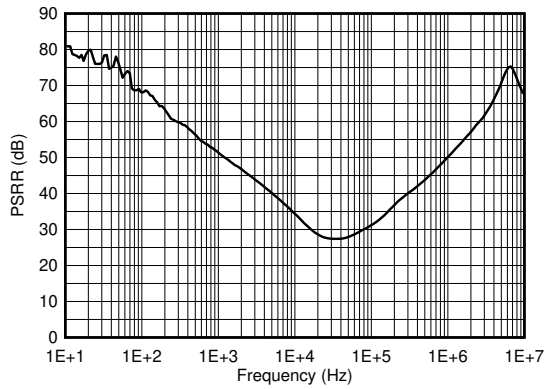


Figure 5-25. Power-Supply Rejection Ratio vs Frequency

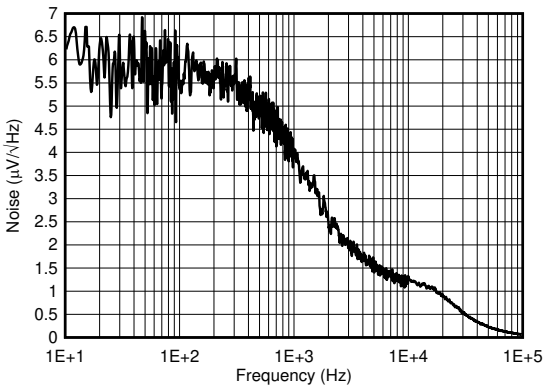
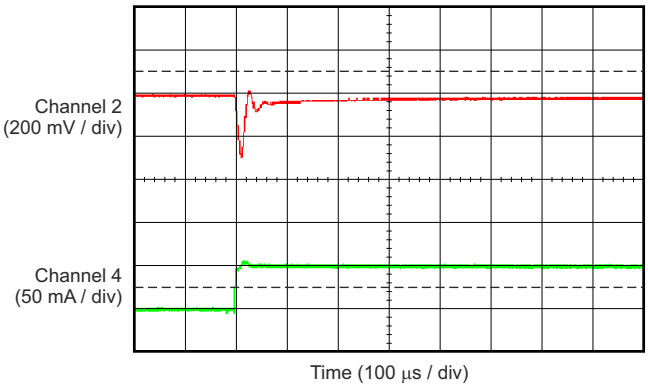
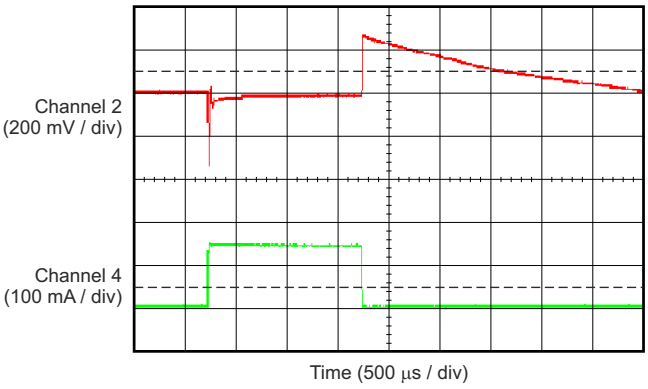


Figure 5-26. Noise



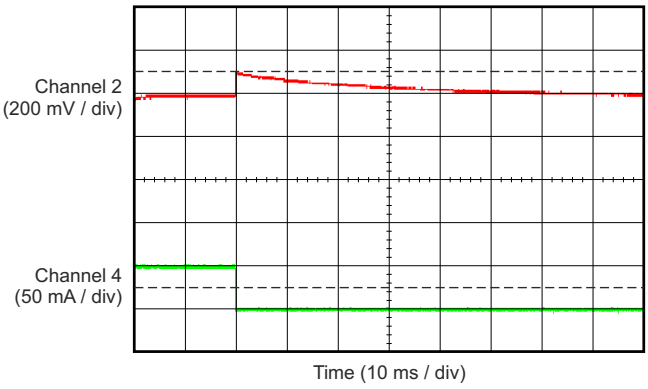
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 2.7 V

Figure 5-27. TPS70912-Q1 Load Transient (0 mA to 50 mA)



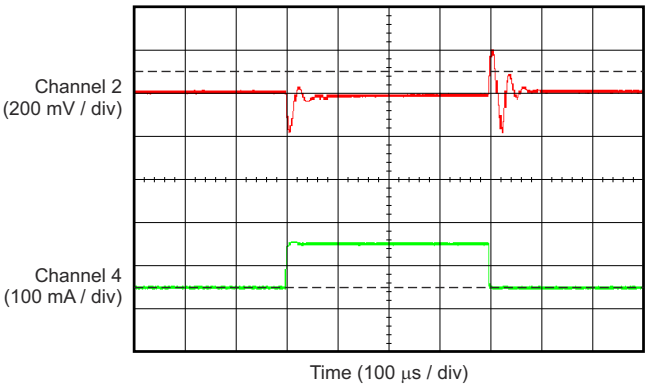
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 2.7 V

Figure 5-28. TPS70912-Q1 Load Transient (1 mA to 150 mA)



Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 2.7 V

Figure 5-29. TPS70912-Q1 Load Transient (50 mA to 0 mA)

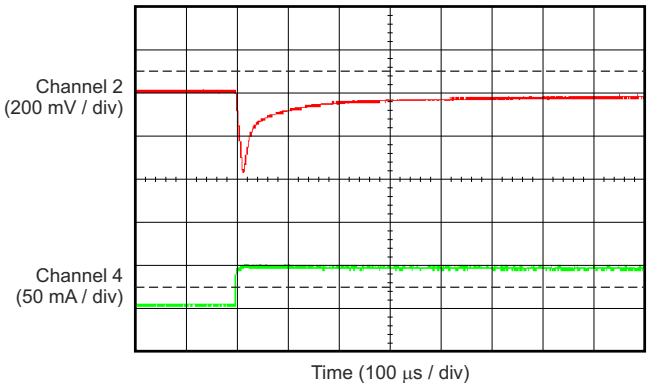


Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 2.7 V

Figure 5-30. TPS70912-Q1 Load Transient (50 mA to 150 mA)

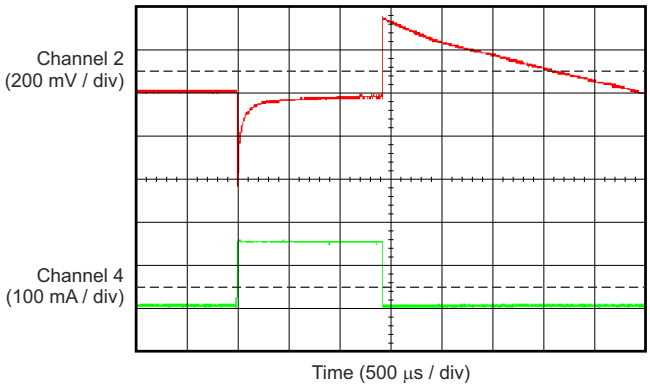
5.8 Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.



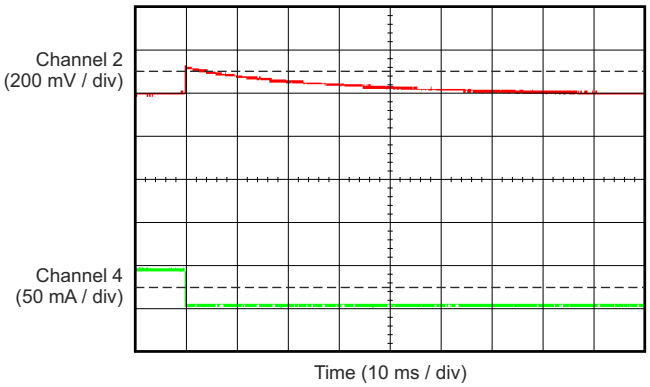
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 5-31. TPS70933-Q1 Load Transient (0 mA to 50 mA)



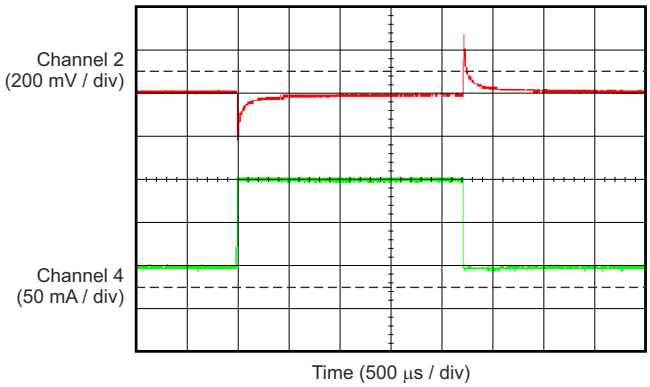
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 5-32. TPS70933-Q1 Load Transient (1 mA to 150 mA)



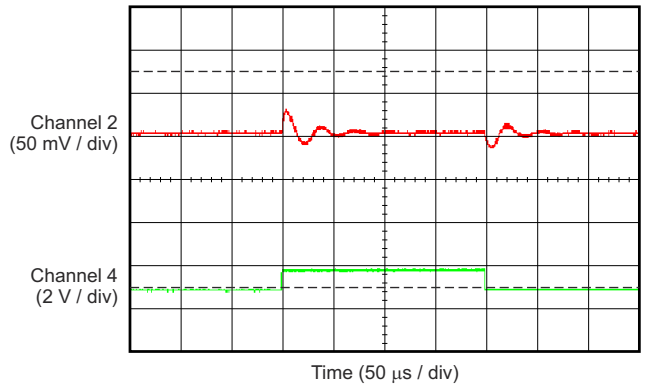
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 5-33. TPS70933-Q1 Load Transient (50 mA to 0 mA)



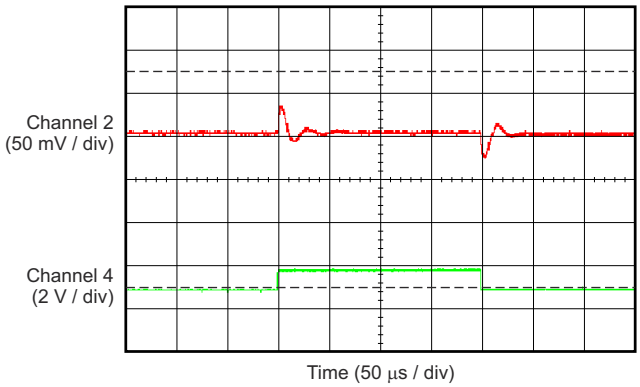
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 5-34. TPS70933-Q1 Load Transient (50 mA to 150 mA)



Channel 2 = V_{OUT}, channel 4 = V_{IN}, I_{OUT} = 10 mA

Figure 5-35. TPS70912-Q1 Line Transient (2.7 V to 3.7 V)

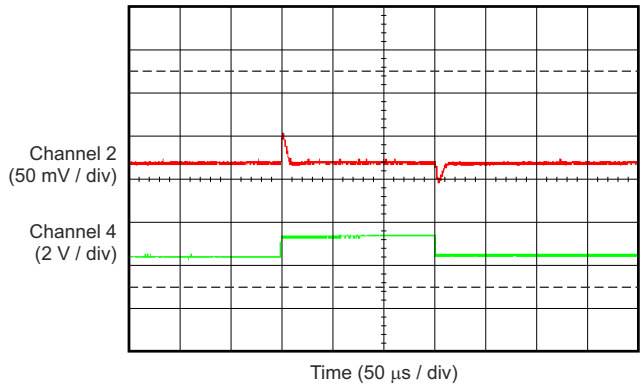


Channel 2 = V_{OUT}, channel 4 = V_{IN}, I_{OUT} = 50 mA

Figure 5-36. TPS70912-Q1 Line Transient (2.7 V to 3.7 V)

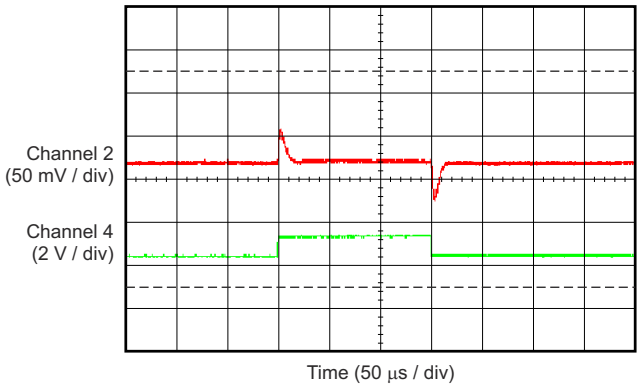
5.8 Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.



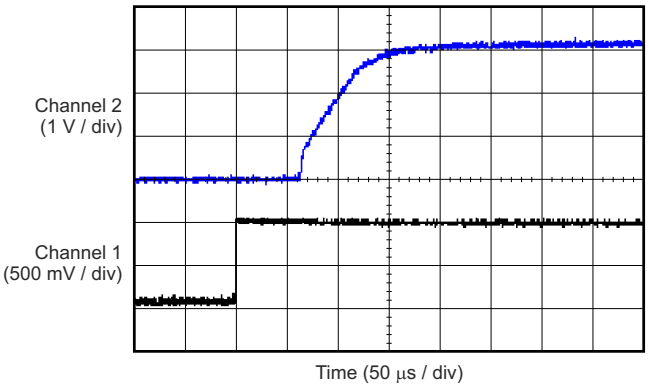
Channel 2 = V_{OUT}, channel 4 = V_{IN}, I_{OUT} = 10 mA

Figure 5-37. TPS70933-Q1 Line Transient (4.3 V to 5.3 V)



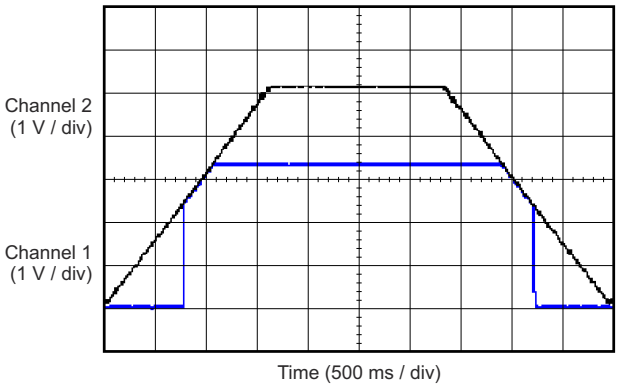
Channel 2 = V_{OUT}, channel 4 = V_{IN}, I_{OUT} = 50 mA

Figure 5-38. TPS70933-Q1 Line Transient (4.3 V to 5.3 V)



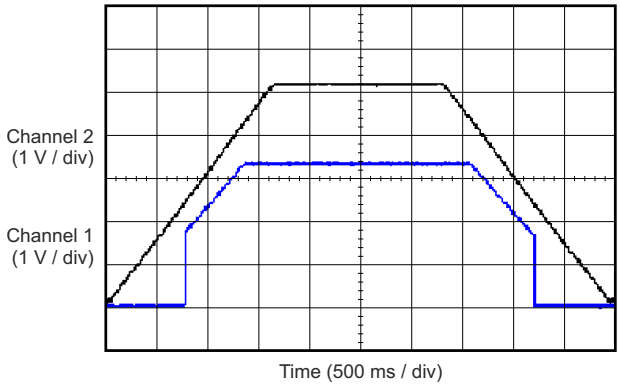
Channel 1 = EN, channel 2 = V_{OUT}, V_{IN} = 4.3 V, C_{OUT} = 2.2 µF, TPS70633

Figure 5-39. Power-Up With Enable



Channel 1 = V_{IN}, channel 2 = V_{OUT}, I_{OUT} = 3 mA, TPS70633

Figure 5-40. Power-Up and Power-Down Response



Channel 1 = V_{IN}, channel 2 = V_{OUT}, I_{OUT} = 150 mA, TPS70633

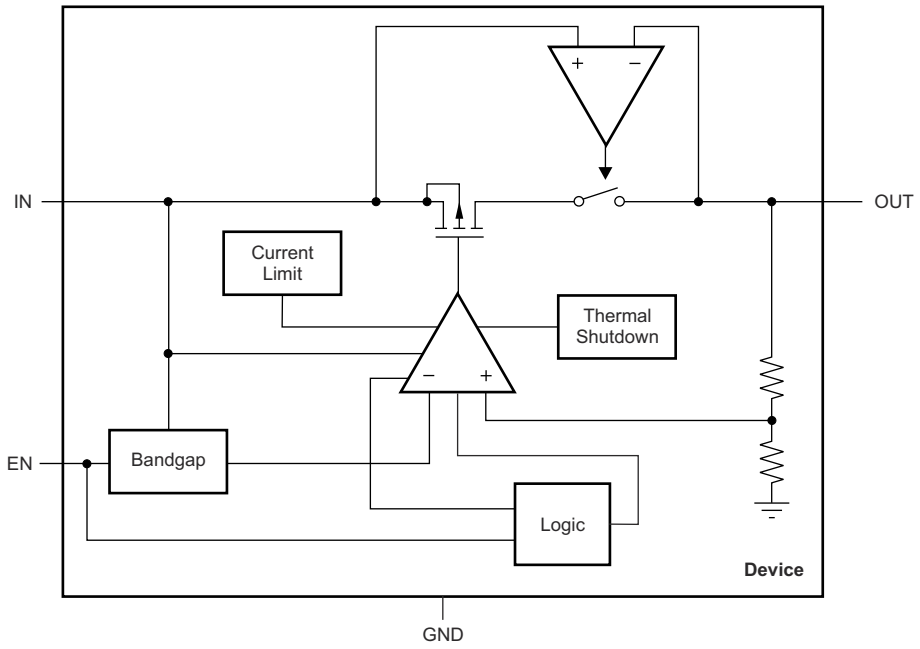
Figure 5-41. Power-Up and Power-Down Response

6 Detailed Description

6.1 Overview

The TPS709-Q1 series are ultralow quiescent current, low-dropout (LDO) linear regulators. The TPS709-Q1 offers reverse current protection to block any discharge current from the output into the input. The TPS709-Q1 also features current limit and thermal shutdown for reliable operation.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Undervoltage Lockout (UVLO)

The TPS709-Q1 uses an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry operates properly.

6.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$ (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.4 V.

6.3.3 Reverse Current Protection

The TPS709-Q1 has integrated reverse current protection. Reverse current protection prevents the flow of current from the OUT pin to the IN pin when output voltage is higher than input voltage. The reverse current protection circuitry places the power path in high impedance when the output voltage is higher than the input voltage. This setting reduces leakage current from the output to the input to 10 nA, typical. The reverse current protection is always active regardless of the enable pin logic state or if the OUT pin voltage is greater than 1.8 V. Reverse current can flow if the output voltage is less than 1.8 V and if input voltage is less than the output voltage.

If voltage is applied to the input pin, then the maximum voltage that can be applied to the OUT pin is the lower of three times the nominal output voltage or 6.5 V. For example, if the 1.2-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 3.6 V. If the 3.3-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 6.5 V.

6.3.4 Internal Current Limit

The TPS709-Q1 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and can be measured as ($V_{OUT} = I_{LIMIT} \times R_{LOAD}$). The PMOS pass transistor dissipates [($V_{IN} – V_{OUT}$) × I_{LIMIT}] until a thermal shutdown is triggered and the device turns off. When cool, the device is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the *Thermal Information* section for more details.

The TPS709-Q1 is characterized over the recommended operating output current range up to 150 mA. The internal current limit begins to limit the output current at a minimum of 200 mA of output current.

6.3.5 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 158°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C, maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The TPS709-Q1 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS709-Q1 into thermal shutdown degrades device reliability.

6.4 Device Functional Modes

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

6.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 6-1 shows the conditions that lead to the different modes of operation.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN(low)}$	—	$T_J > 158°C$

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS709-Q1 consumes low quiescent current and delivers excellent line and load transient performance. This performance, combined with low noise and good PSRR with little (V_{IN} – V_{OUT}) headroom, makes these devices designed for RF portable applications, current limit, and thermal protection. The TPS709-Q1 devices are specified from –40°C to 125°C.

7.1.1 Input and Output Capacitor Considerations

The TPS709-Q1 devices are stable with output capacitors with an effective capacitance of 2.0 µF or greater for output voltages below 1.5 V. For output voltages equal or greater than 1.5 V, the minimum effective capacitance for stability is 1.5 µF. The maximum capacitance for stability is 47 µF. The equivalent series resistance (ESR) of the output capacitor must be between 0 Ω and 0.2 Ω for stability.

The effective capacitance is the minimum capacitance value of a capacitor after taking into account variations resulting from tolerances, temperature, and dc bias effects. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and ESR over temperature.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 2.2-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR.

7.1.2 Dropout Voltage

The TPS709-Q1 uses a PMOS-pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS-pass transistor is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS-pass transistor. V_{DO} approximately scales with the output current because the PMOS transistor functions like a resistor in dropout.

The ground pin current of many linear voltage regulators increases substantially when the device is operated in dropout. This increase in ground pin current while operating in dropout can be several orders of magnitude larger than when the device is not in dropout. The TPS709-Q1 employs a special control loop that limits the increase in ground pin current while operating in dropout. This functionality allows for the most efficient operation while in dropout conditions that can greatly increase battery run times.

7.1.3 Transient Response

As with any regulator, increasing the output capacitor size reduces over- and undershoot magnitude, but increases transient response duration.

7.2 Typical Application

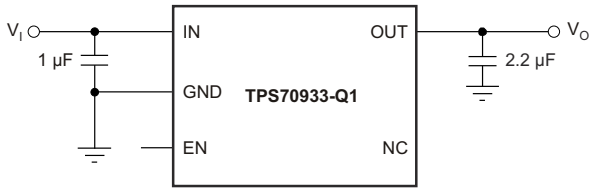


Figure 7-1. 3.3-V, Low-I_Q Rail

7.2.1 Design Requirements

Table 7-1 summarizes the design requirements for Figure 7-1.

Table 7-1. Design Requirements for a 3.3-V, Low-I_Q Rail Application

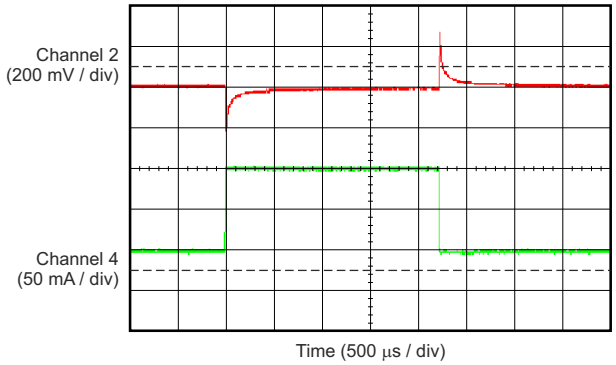
PARAMETER	DESIGN SPECIFICATION
V_{IN}	4.3 V
V_{OUT}	3.3 V
$I_{(IN)}$ (no load)	< 5 µA
I_{OUT} (max)	150 mA

7.2.2 Detailed Design Procedure

Select a 2.2-µF, 10-V X7R output capacitor to satisfy the minimum output capacitance requirement with a 3.3-V dc bias.

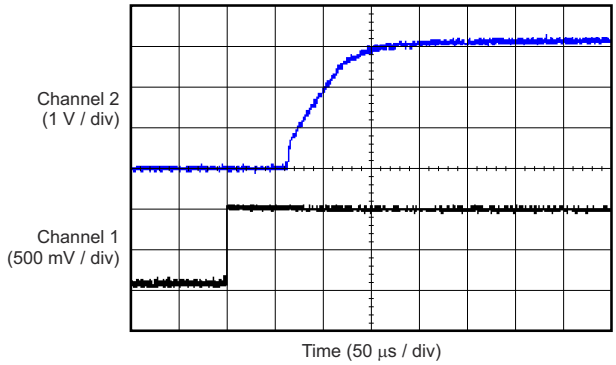
Select a 1.0-µF, 10-V X7R input capacitor to provide input noise filtering and eliminate high-frequency voltage transients.

7.2.3 Application Curves



Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 7-2. TPS70933-Q1 Load Transient (50 mA to 150 mA)



Channel 1 = EN, channel 2 = V_{OUT}, V_{IN} = 4.3 V, C_{OUT} = 2.2 µF, TPS70933-Q1

Figure 7-3. Power-Up with Enable

7.3 Power Supply Recommendations

This device is designed to operate with an input supply range of 2.7 V to 30 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

7.4.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Input and output capacitors must be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection must be connected directly to the device GND pin. High ESR capacitors may degrade PSRR performance.

7.4.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 1.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (1)$$

Figure 7-4 shows the maximum ambient temperature versus the power dissipation of the TPS709-Q1. This figure assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to make sure the TPS709-Q1 does not operate above a junction temperature of 125°C.

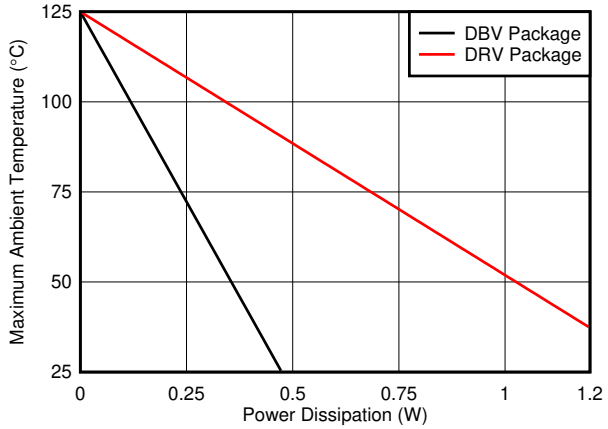


Figure 7-4. Maximum Ambient Temperature vs Device Power Dissipation

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in the *Thermal Information*. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 2.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{2}$$

where:

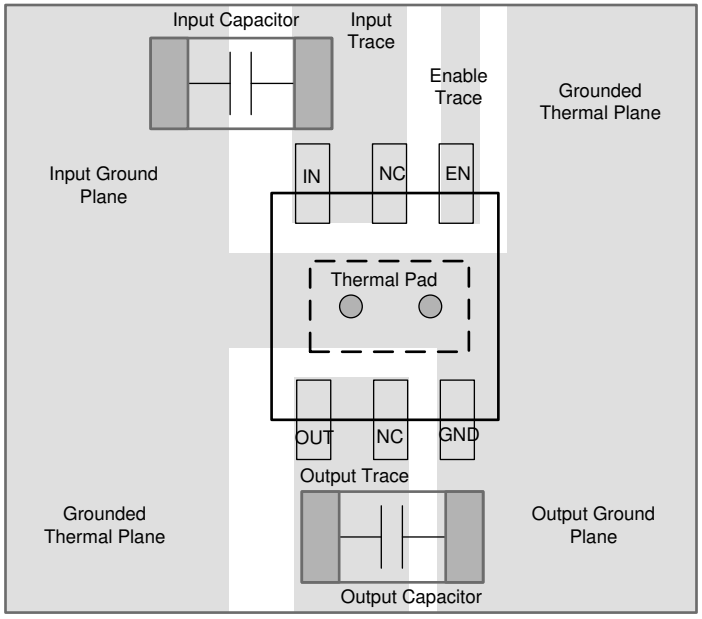
- P_D is the power dissipation shown by Equation 1,
- T_T is the temperature at the center-top of the device package,
- T_B is the PCB temperature measured 1 mm away from the device package *on the PCB surface*.

Note

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

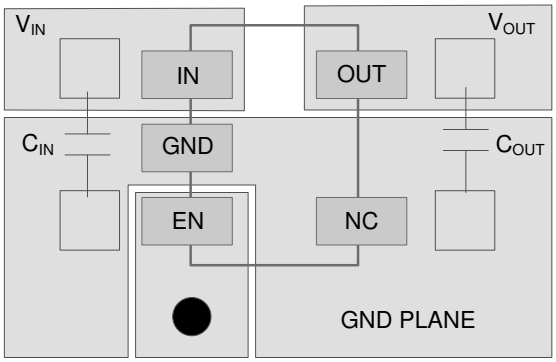
For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.

7.4.2 Layout Examples



Designates thermal vias.

Figure 7-5. WSON Layout Example



Represents via used for application-specific connections.

Figure 7-6. SOT23-5 Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS709-Q1. The TPS70933EVM-110 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS709 is available through the product folders under *Simulation Models*.

8.1.2 Device Nomenclature

Table 8-1. Available Options

PRODUCT[1]	DESCRIPTION
TPS709**xx(x)**Q ***yyy z*** Q1 or TPS709**xx(x)**Q ***yyy z*** **M3** Q1	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **yyy** is the package designator. **z** is the tape and reel quantity (R = 3000, T = 250).This device ships with either the legacy chip (CSO: TI1) or the new chip (CSO:RFB), which uses the latest manufacturing flow. The reel packaging label provides CSO information to distinguish which chip is used. Device performance for new and legacy chips is denoted throughout the document. **M3** is a suffix designator only significant for the new chip with CSO:RFB, which uses the latest manufacturing flow.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS70933EVM-110 Evaluation Module* user's guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2018) to Revision D (August 2025)	Page
• Added links to *Applications* section	1
• Added thermal information for both DBV & DRV manufactured at new A/T site	4
• Changed *Available Options* table	22

Changes from Revision B (March 2015) to Revision C (June 2018)	Page
• Changed from: Dropout Voltage (V) to: Dropout Voltage (mV) in Figure 5-8, Figure 5-9, and Figure 5-10	7
• Deleted last sentence from *Shutdown* section	14
• Changed text From: "input supply range of 2.7 V to 6.5 V:" To: " input supply range of 2.7 V to 30 V." in the *Section 7.3* section	18

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS70930QDBVRM3Q1	Active	Preproduction	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS70912QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLR
TPS70912QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLR
TPS70912QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLR
TPS70912QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJD
TPS70912QDRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJD
TPS70912QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJD
TPS70915QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJE
TPS70915QDRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJE
TPS70915QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJE
TPS70918QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLS
TPS70918QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLS
TPS70918QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLS
TPS70918QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJF
TPS70918QDRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJF
TPS70918QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJF
TPS70925QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLT
TPS70925QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLT
TPS70925QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLT
TPS70925QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJG
TPS70925QDRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJG
TPS70925QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJG
TPS70927QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJH
TPS70927QDRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJH
TPS70927QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJH
TPS70928QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLU
TPS70928QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLU
TPS70928QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLU
TPS70928QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS70928QDRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJI
TPS70928QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJI
TPS70930QDBVRM3Q1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLV
TPS70930QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLV
TPS70930QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLV
TPS70930QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLV
TPS70930QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJJ
TPS70930QDRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJJ
TPS70930QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJJ
TPS70933QDBVRM3Q1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLJ
TPS70933QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLJ
TPS70933QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLJ
TPS70933QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLJ
TPS70933QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJK
TPS70933QDRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJK
TPS70933QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJK
TPS70936QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLW
TPS70936QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLW
TPS70936QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLW
TPS70950QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLX
TPS70950QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLX
TPS70950QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLX
TPS70950QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJL
TPS70950QDRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJL
TPS70950QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJL

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS709-Q1 :

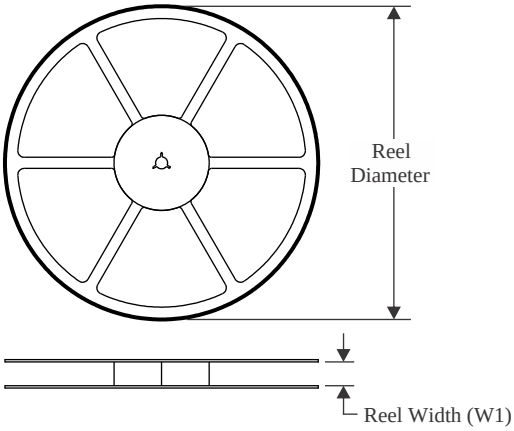
- Catalog : TPS709

NOTE: Qualified Version Definitions:

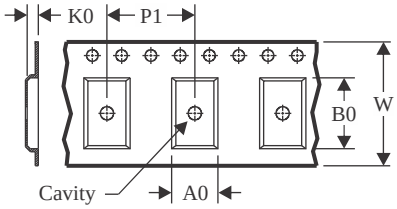
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

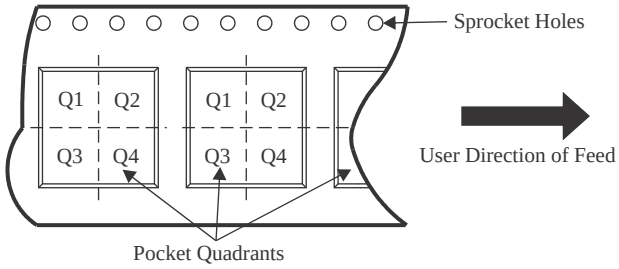


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

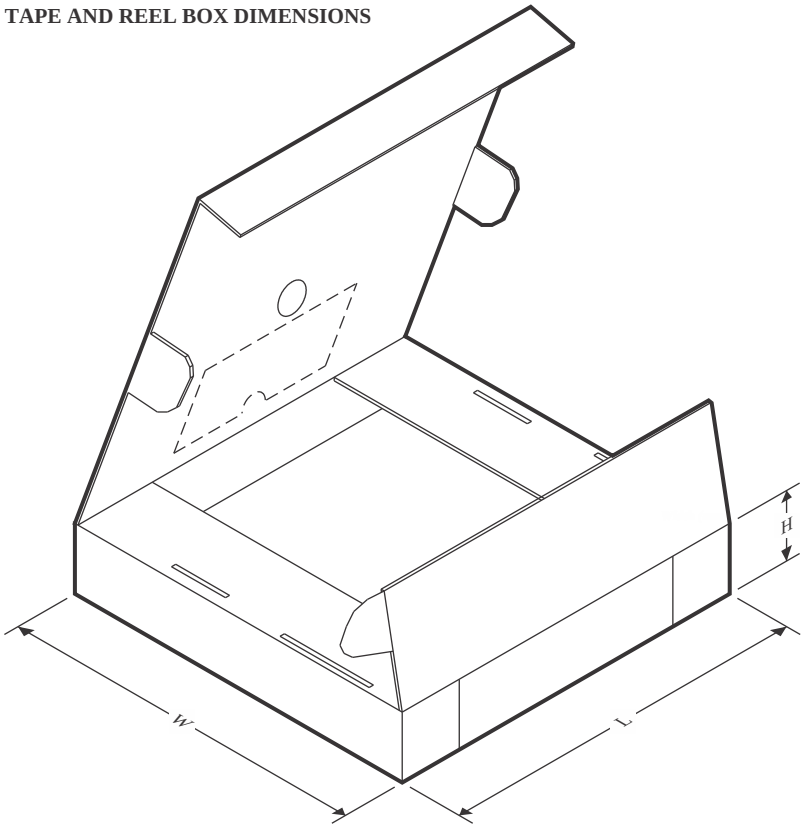


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70912QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70912QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70915QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70918QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70918QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70925QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70925QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70927QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70928QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70928QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70930QDBVRM3Q1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS70930QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70930QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70933QDBVRM3Q1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS70933QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70933QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70936QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS70936QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70912QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70912QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70915QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70918QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70918QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70925QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70925QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70927QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70928QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70928QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70930QDBVRM3Q1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS70930QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70930QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70933QDBVRM3Q1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS70933QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70933QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70936QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS70936QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0

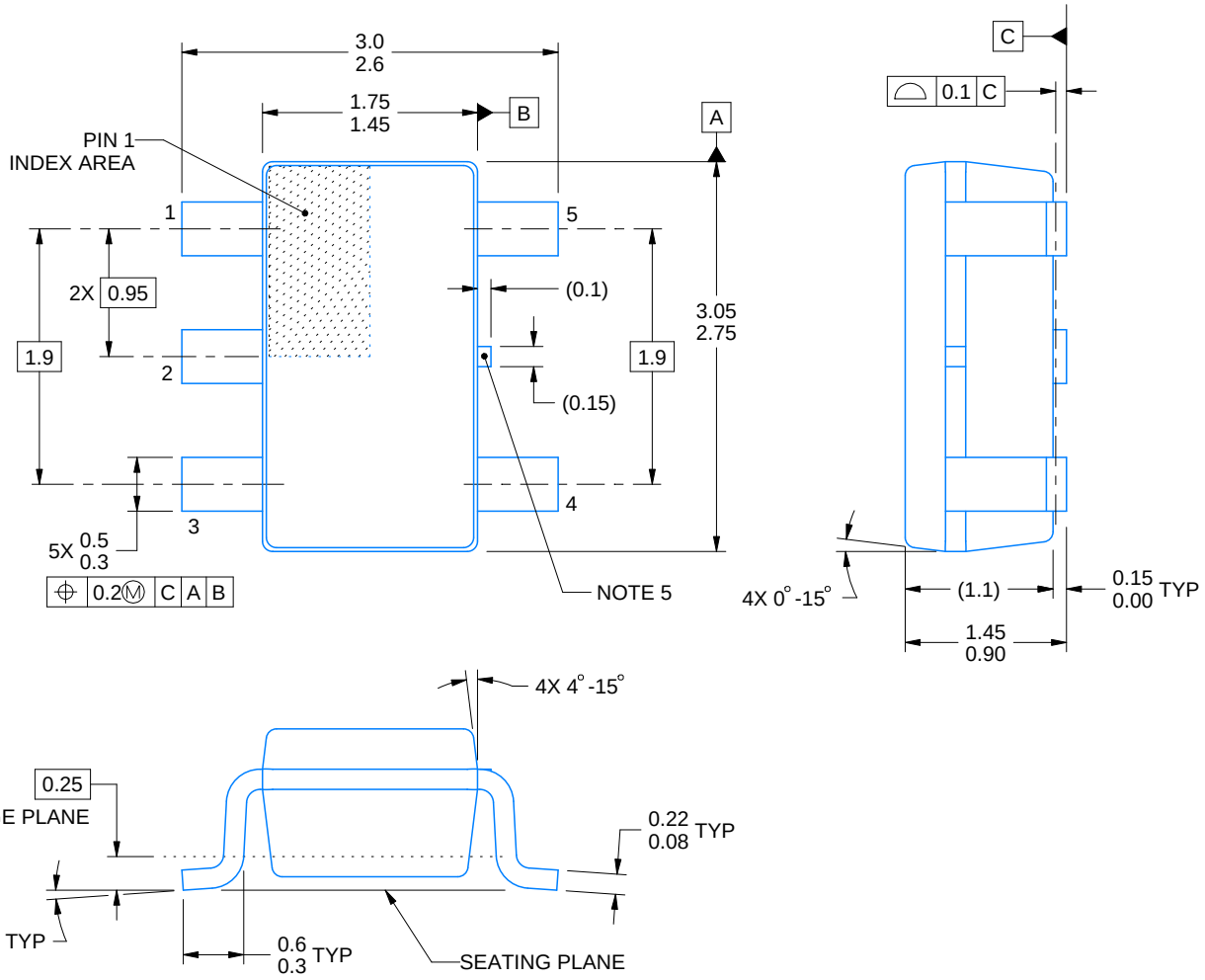
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70950QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70950QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

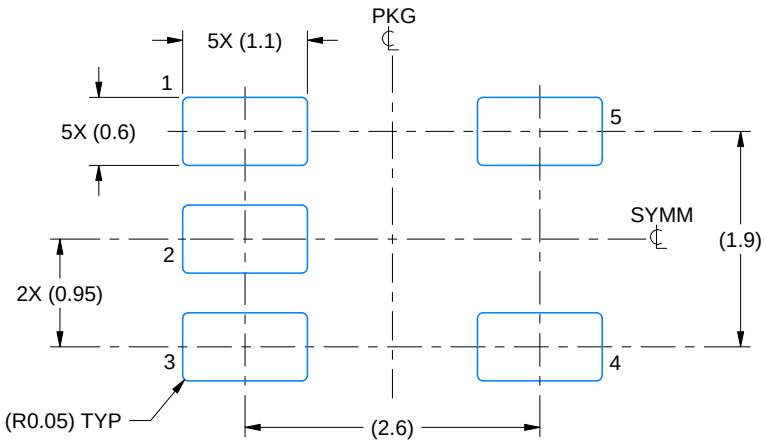
SMALL OUTLINE TRANSISTOR



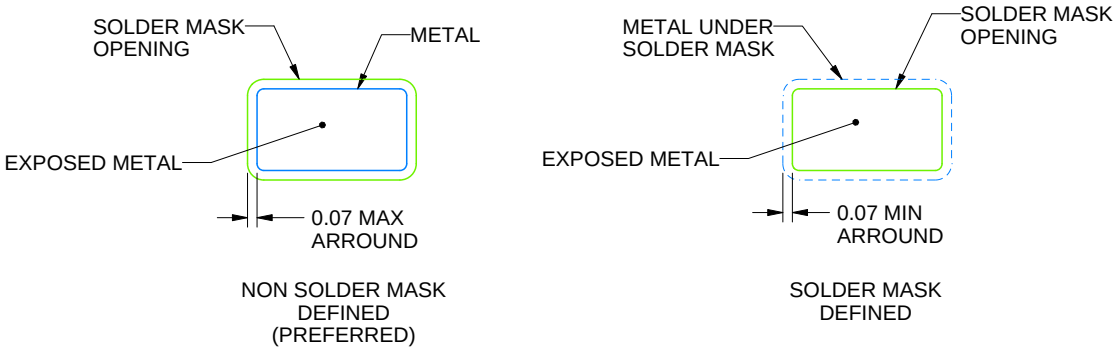
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

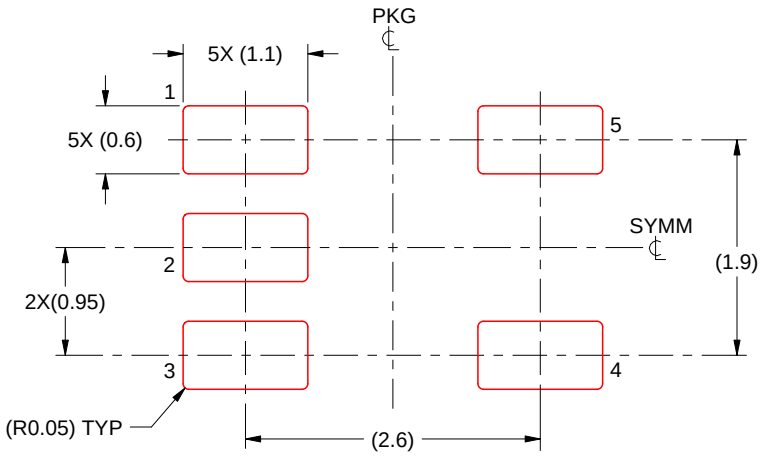


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

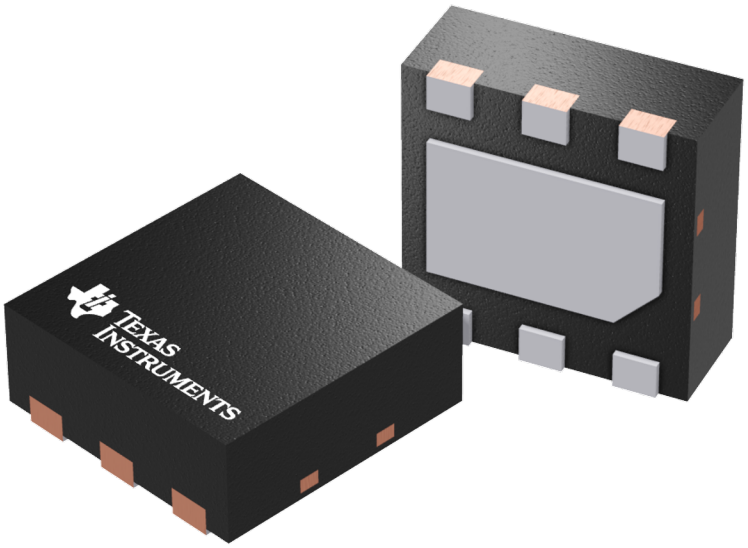
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



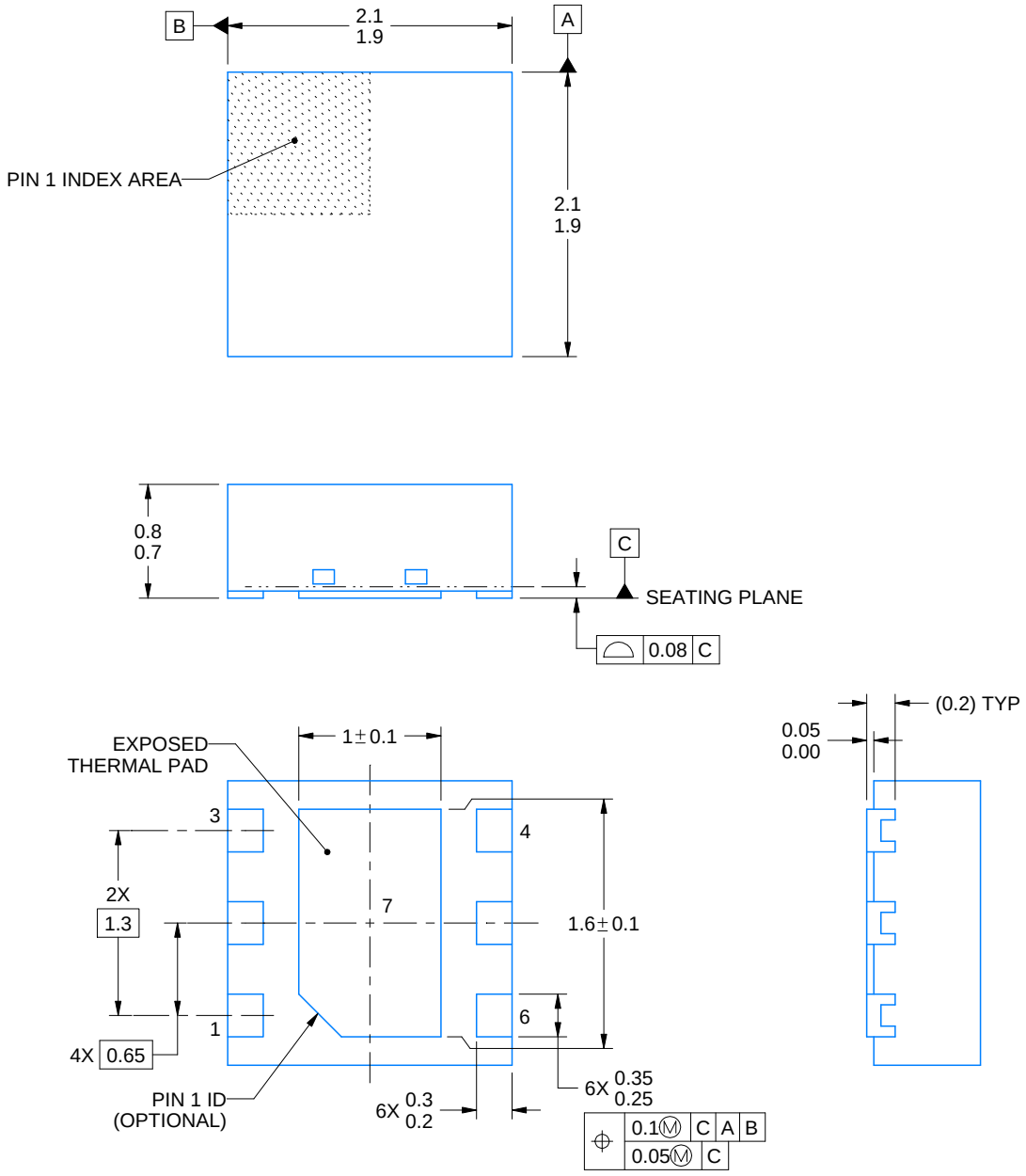
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

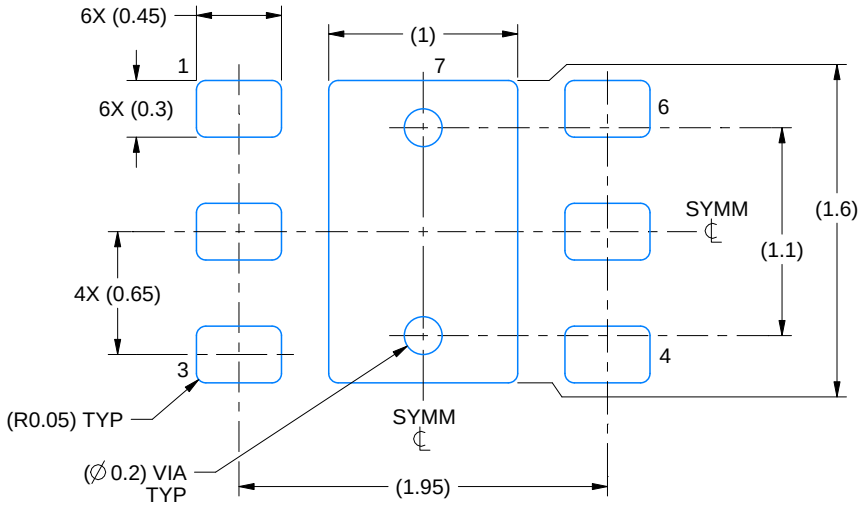
PLASTIC SMALL OUTLINE - NO LEAD



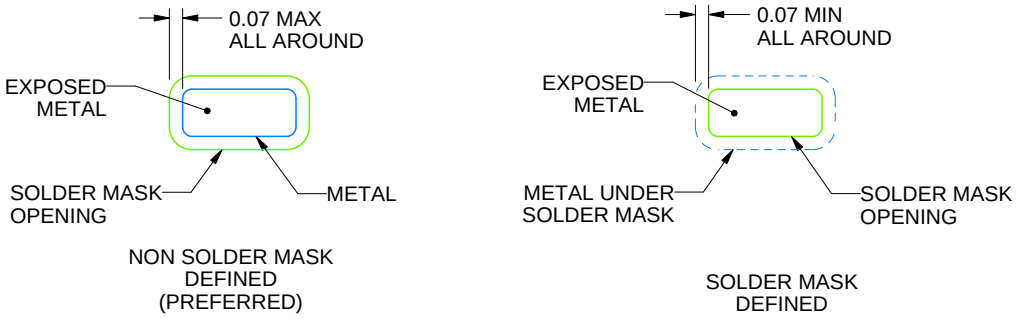
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

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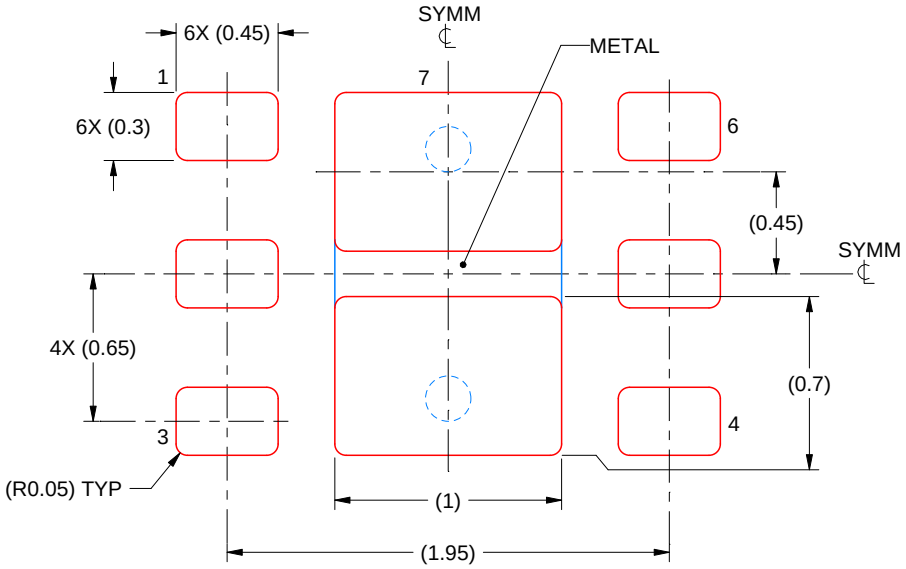
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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