TPS715A-NM
24-V High Input Voltage, Micropower, 80-mA LDO Voltage Regulator

1 Features

- 24-V Maximum Input Voltage
- Low 3.2-μA Quiescent Current at 80 mA
- Stable With Any Capacitor (≥ 0.47 μF)
- 80-mA Specified Current
- Available in Fixed and Adjustable (1.2 V to 15 V) Versions
- Specified Current Limit
- 3-mm × 3-mm and 2-mm × 2-mm SON Packages
- –40°C to 125°C Specified Junction Temperature Range
- For MSP430-Specific Output Voltages See TPS715xx

2 Applications

- Ultralow Power Microcontrollers
- Industrial and Automotive Applications
- Video Surveillance and Security Systems
- Portable, Battery-Powered Equipment
- Medical Imaging

3 Description

The TPS715A-NM low-dropout (LDO) voltage regulators offer the benefits of high input voltage, low-dropout voltage, low-power operation, and miniaturized packaging. The devices operate over an input range of 2.5 V to 24 V and are stable with any capacitor (≥ 0.47 μF). The high maximum input voltage combined with excellent power dissipation capability makes this device particularly well-suited to industrial and automotive applications.

A PMOS pass element functions as a low-value resistor. The low dropout voltage, typically 670 mV at 80 mA of load current, is directly proportional to the load current. The low quiescent current (3.2 μA typically) is nearly constant over the entire range of output load current (0 mA to 80 mA).

The TPS715A-NM is available in a 3-mm × 3-mm package ideal for high power dissipation and a small 2-mm × 2-mm package ideal for handheld and ultra-portable applications. The 3-mm × 3-mm package is also available as a non-magnetic package for medical imaging applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS715A-NM	SON (8), DRB	3.00 mm × 3.00 mm
	SON (6), DRV	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

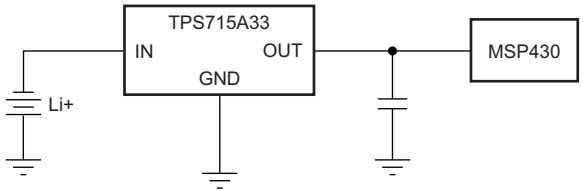
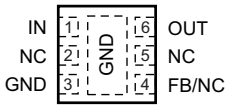


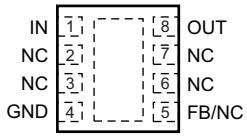
Table of Contents

4 Pin Configuration and Functions

DRV Package
6-Pin SON
Top View



DRB Package
8-Pin SON
Top View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	8-PIN SON		6-PIN SON			
	FIXED	ADJ.	FIXED	ADJ.		
FB	—	5	—	4	I	Adjustable version. This pin is used to set the output voltage.
GND	4, Pad	4, Pad	3, Pad	3, Pad	—	Ground
IN	1	1	1	1	I	Unregulated input voltage
NC	2, 3, 5, 6, 7	2, 3, 6, 7	2, 4, 5	2, 5	—	No connection. Can be left open or tied to ground for improved thermal performance.
OUT	8	8	6	6	O	Regulated output voltage, any output capacitor ≥ 0.47 µF can be used for stability.

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input supply voltage, V_{IN}	–0.3	24	V
Peak output current	Internally limited		
Continuous total power dissipation	See *Thermal Information*		
Junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.5		24	V
I_{OUT}	Output current	0		80	mA
C_{IN}	Input capacitor	0	0.047		µF
C_{OUT}	Output capacitor	0.47	1		µF

5.4 Thermal Information

THERMAL METRIC[1]		TPS715A-NM		UNIT
		DRV (SON)	DRB (SON)	
		6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.5	69	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	110.5	76.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.9	44.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.2	8.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.3	44.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	18.3	27.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 1 µF, unless otherwise noted. The TPS715A01 device is tested with V_{OUT} = 2.8 V. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage[1]		V_{IN}	I_{OUT} = 10 mA	2.5		24	V
			I_{OUT} = 80 mA	3		24	
Voltage range (TPS715A01)		V_{OUT}		1.2		15	V
Output voltage accuracy[1]	TPS715A01		V_{OUT} + 1 V ≤ V_{IN} ≤ 24 V, 1.2 V ≤ V_{OUT} ≤ 15V, 0 ≤ I_{OUT} ≤ 80 mA	0.96 × $V_{OUT(nom)}$	$V_{OUT(nom)}$	1.04 × $V_{OUT(nom)}$	V
	TPS715A33		4.3 V < V_{IN} < 24 V, 0 ≤ I_{OUT} ≤ 80 mA	3.135	3.3	3.465	
Output voltage line regulation[1]		$\Delta V_{OUT}/\Delta V_{IN}$	V_{OUT} + 1 V < V_{IN} ≤ 24 V		20	60	mV
Load regulation		$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 100 µA to 80 mA		35		mV
Dropout voltage V_{IN} = $V_{OUT(NOM)}$ – 0.1 V		V_{DO}	I_{OUT} = 80 mA		670	1120	mV
Output current limit		I_{CL}	V_{OUT} = 0 V	160		1100	mA
Ground pin current		I_{GND}	T_J = –40°C to 85°C, 0 mA ≤ I_{OUT} ≤ 80 mA		3.2	4.2	µA
			0 mA ≤ I_{OUT} ≤ 80 mA		3.2	4.8	
			V_{IN} = 24 V, 0 mA ≤ I_{OUT} ≤ 80 mA			5.8	
Power-supply ripple rejection		PSRR	f = 100 kHz, C_{OUT} = 10 µF		60		dB
Output noise voltage		V_{IN}	BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		575		µVrms

(1) Minimum V_{IN} = V_{OUT} + V_{DO}, or the value shown for input voltage, whichever is greater.

5.6 Typical Characteristics

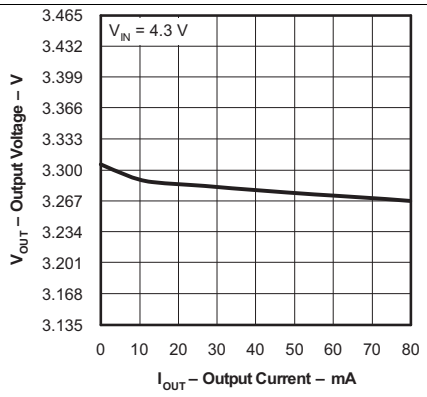


Figure 1. TPS715A33 Output Voltage vs Output Current

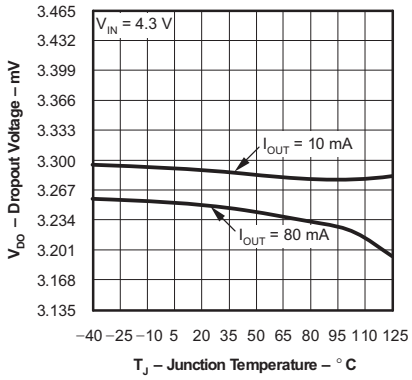


Figure 2. TPS715A33 Dropout Voltage vs Junction Temperature

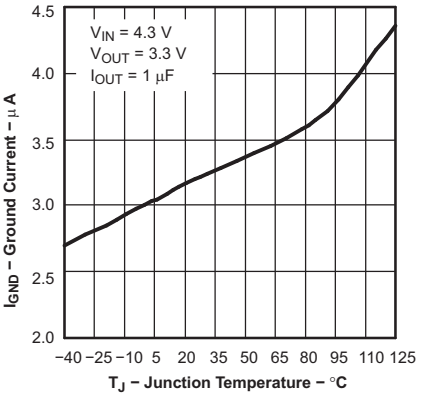


Figure 3. Ground Current vs Junction Temperature

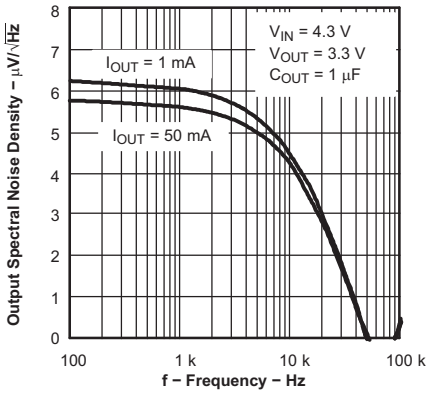


Figure 4. Output Spectral Noise Density vs Frequency

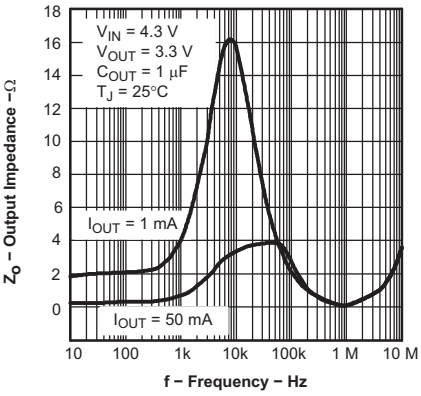


Figure 5. Output Impedance vs Frequency

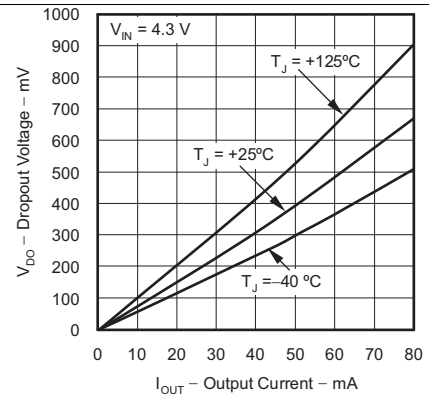


Figure 6. TPS715A33 Dropout Voltage vs Output Current

Typical Characteristics (continued)

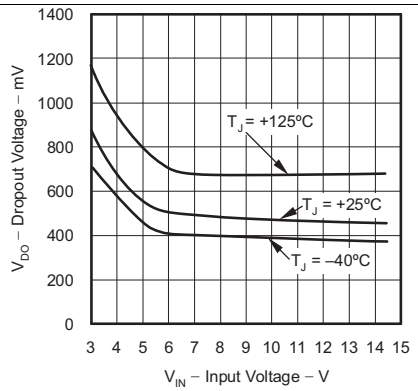


Figure 7. TPS715A01 Dropout Voltage vs Input Voltage

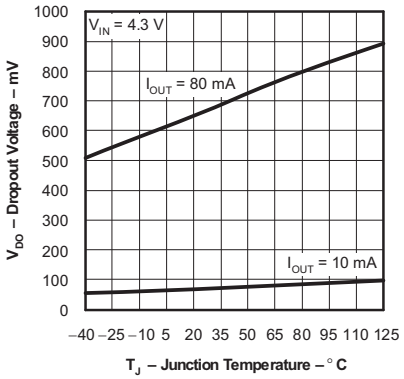


Figure 8. TPS715A33 Dropout Voltage vs Junction Temperature

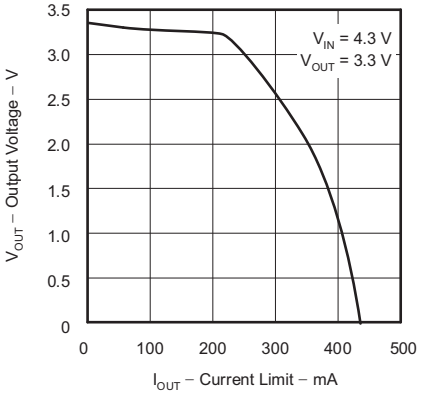


Figure 9. Output Voltage vs Current Limit

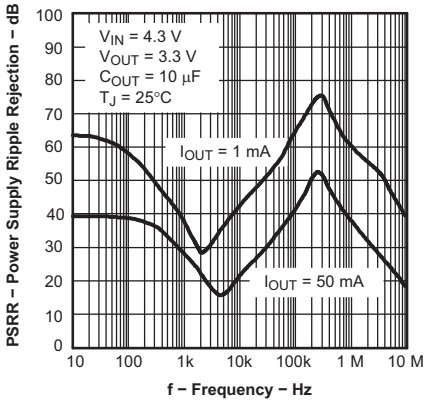


Figure 10. Power-Supply Ripple Rejection vs Frequency

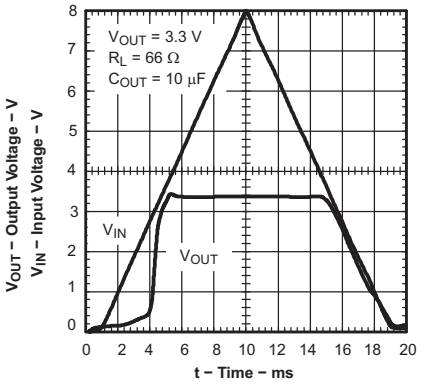


Figure 11. Power-Up and Power-Down

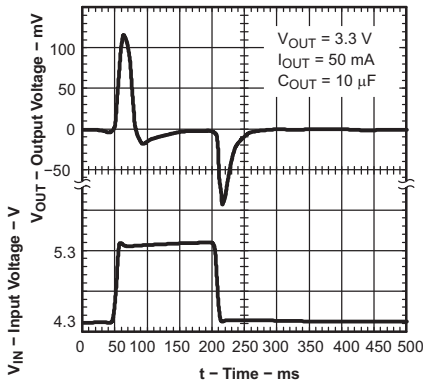


Figure 12. Line Transient Response

Typical Characteristics (continued)

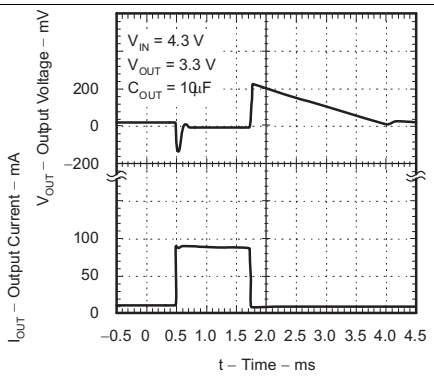


Figure 13. Load Transient Response

6 Detailed Description

6.1 Overview

The TPS715A-NM family of low dropout regulators consumes only 3.2 µA of current and offers a wide input voltage range and low-dropout voltage in a small package. The devices operate over an input range of 2.5 V to 24 V and are stable with any capacitor greater than or equal to 0.47 µF. The low quiescent current makes the TPS715A-NM ideal for powering battery management devices. Specifically, because the TPS715A-NM is enabled as soon as the applied voltage reaches the minimum input voltage, the output is quickly available to power continuously-operating, battery-charging devices.

6.2 Functional Block Diagrams

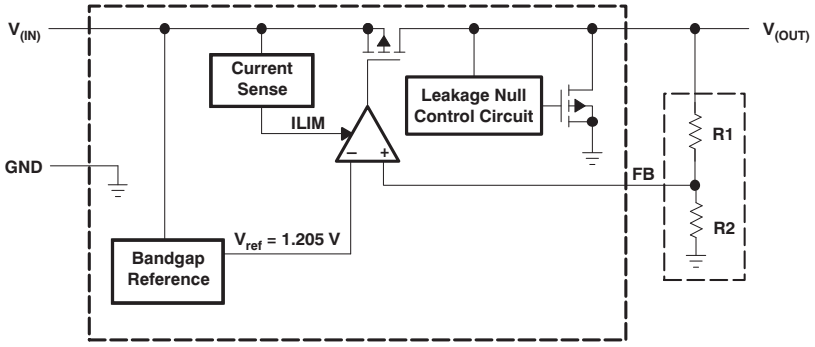


Figure 14. Functional Block Diagram—Adjustable Version

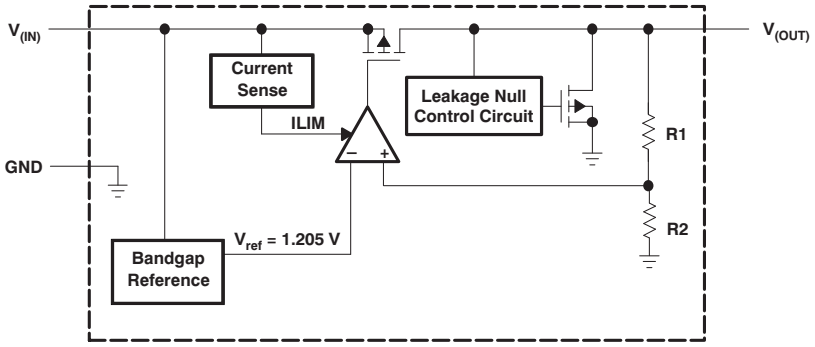


Figure 15. Functional Block Diagram—Fixed Version

6.3 Feature Description

6.3.1 Wide Supply Range

This device has an operational input supply range of 2.5 V to 24 V, allowing for a wide range of applications. This wide supply range is ideal for applications that have either large transients or high dc voltage supplies.

6.3.2 Low Supply Current

This device only requires 3.2 µA (typical) of supply current and has a maximum current consumption of 5.8 µA at –40°C to 125°C.

6.3.3 Stable With Any Capacitor ≥ 0.47 µF

Any capacitor, including both ceramic and tantalum, greater than or equal to 0.47 µF properly stabilizes this loop.

6.3.4 Internal Current Limit

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases.

NOTE

If a current limit occurs and the resulting output voltage is low, excessive power is dissipated across the LDO, resulting in possible damage to the device.

6.3.5 Reverse Current

The TPS715A-NM device PMOS-pass transistor has a built-in back diode that conducts current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting may be required.

6.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Disabled	—	—

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than 125°C.

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

7 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The TPS715A-NM family of LDO regulators is optimized for ultralow-power applications such as the MSP430 microcontroller. The ultralow-supply current of the TPS715A-NM device maximizes efficiency at light loads, and its high input voltage range makes the device suitable for supplies such as unconditioned solar panels.

7.2 Typical Applications

7.2.1 Typical Application (Fixed-Voltage Version)

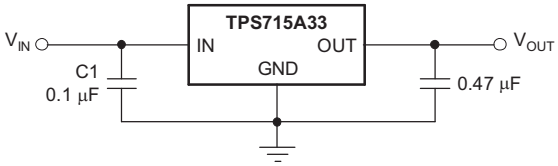


Figure 16. Typical Application Circuit (Fixed-Voltage Version)

7.2.1.1 Design Requirements

7.2.1.1.1 Power the MSP430 Microcontroller

Several versions of the TPS715A-NM are ideal for powering the MSP430 microcontroller. Table 2 shows potential applications of some voltage versions.

Table 2. Typical MSP430 Applications

DEVICE	V_{OUT} (TYP)	APPLICATION
TPS715A19	1.9 V	$V_{OUT(min)}$ > 1.8 V required by many MSP430s. Allows lowest power consumption operation.
TPS715A23	2.3 V	$V_{OUT(min)}$ > 2.2 V required by some MSP430s flash operation.
TPS715A30	3 V	$V_{OUT(min)}$ > 2.7 V required by some MSP430s flash operation.
TPS715A345	3.45 V	$V_{OUT(max)}$ < 3.6 V required by some MSP430s. Allows highest speed operation.

The TPS715A-NM family of devices offers many output voltage versions to allow the supply voltage to be optimized for the MSP430, thereby minimizing the supply current consumed by the MSP430.

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 External Capacitor Requirements

Although not required, a 0.047-µF or larger input bypass capacitor, connected between IN and GND and located close to the device, is recommended to improve transient response and noise rejection of the power supply as a whole. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

The TPS715A-NM device requires an output capacitor connected between OUT and GND to stabilize the internal control loop. Any capacitor (including ceramic and tantalum) greater than or equal to 0.47 µF properly stabilizes this loop. The X7R- or X5R-type capacitors are recommended because these capacitors have a wider temperature specification and lower temperature coefficient, but other types of capacitors can be used.

7.2.1.2.2 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage ($V_{DO} = V_{IN} - V_{OUT}$). However, in the *Electrical Characteristics* table, V_{DO} is defined as the $V_{IN} - V_{OUT}$ voltage at the rated current, where the pass-FET is fully enhanced in the ohmic region of operation and is characterized by the classic $R_{DS(on)}$ of the FET. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary. If the input falls below this V_{DO} limit ($V_{IN} < V_{OUT} + V_{DO}$), then the output voltage decreases to follow the input voltage.

Dropout voltage is always determined by the $R_{DS(on)}$ of the main pass-FET. Therefore, if the LDO operates below the rated current, then the V_{DO} for that current scales accordingly. $R_{DS(on)}$ can be calculated using Equation 1.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

7.2.1.3 Application Curves

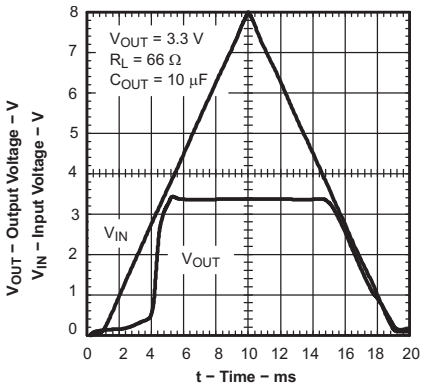


Figure 17. Power-Up and Power-Down

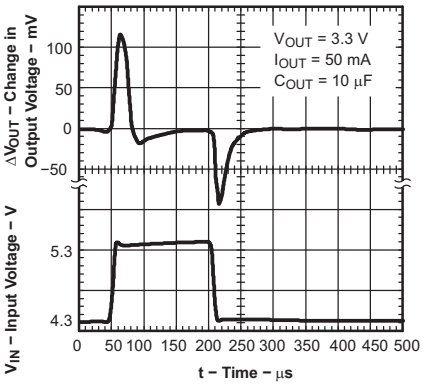


Figure 18. Line Transient Response

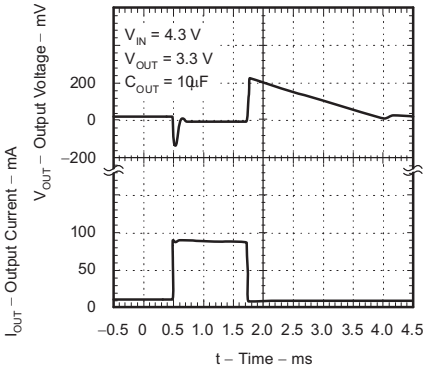
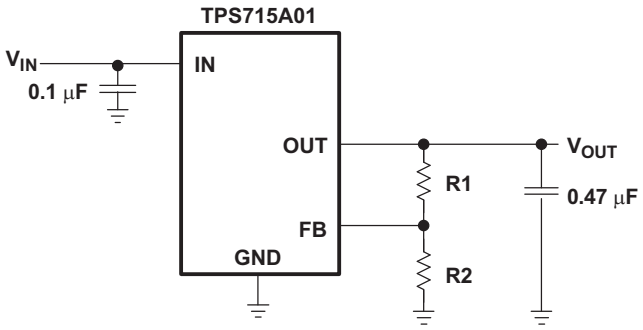


Figure 19. Load Transient Response

7.2.2 TPS715A01 Adjustable LDO Regulator Programming



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2
1.8 V	392 kΩ	806 kΩ
2.8 V	1.07 MΩ	806 kΩ
5.0 V	2.55 MΩ	806 kΩ

Figure 20. TPS715A01 Adjustable LDO Regulator Programming

7.2.2.1 Detailed Design Procedure

7.2.2.1.1 Setting V_{OUT} for the TPS715A01 Adjustable LDO

The TPS715A-NM family of devices contains an adjustable-version, the TPS715A01 device, that sets the output voltage using an external resistor divider as shown in Figure 20. The output voltage operating range is 1.2 V to 15 V, and is calculated using Equation 2.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

where

- V_{REF} = 1.205 V (typical)

Choose resistors R1 and R2 to allow approximately 1.5-µA of current through the resistor divider. Lower value resistors can be used for improved noise performance, but consume more power. Avoid higher resistor values because leakage current into or out of FB across R1, R2 creates an offset voltage that is proportional to V_{OUT} divided by V_{REF}. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 µA, and then calculate R1 using Equation 3.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times 2 \quad (3)$$

Figure 20 shows this configuration.

7.3 Do's and Don'ts

Place at least one 0.47-µF capacitor as close as possible to the OUT and GND pins of the regulator.

Do not connect the output capacitor to the regulator using a long, thin trace.

Connect an input capacitor of 0.047 µF as close as possible to the IN and GND pins of the regulator for best performance.

Do not exceed the absolute maximum ratings.

8 Power Supply Recommendations

The TPS715A-NM is designed to operate with an input voltage supply range from 2.5 V to 24 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

9 Layout

9.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the printed-circuit-board and as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. TI strongly discourages using vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or the resistor divider because doing so negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is recommended to be embedded either in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane assures accuracy of the output voltage and shields the LDO from noise.

9.2 Layout Example

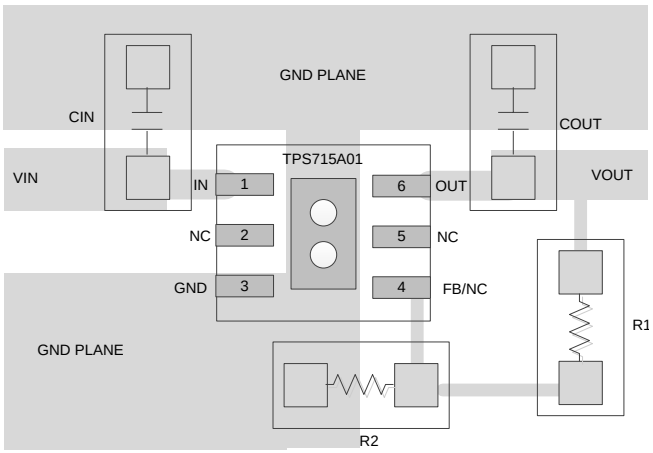


Figure 21. Example Layout for the TPS715A01DRV

9.3 Power Dissipation

To ensure reliable operation, worst-case junction temperature must not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 4.

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (4)$$

where

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information* table)
- T_A is the ambient temperature

The regulator power dissipation is calculated using Equation 5.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

For a higher power package version of the TPS715A-NM, see the TPS715A-NM.

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS715A-NM. The TPS715AXXEVM-065 evaluation module (and related user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

10.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS715A-NM is available through the product folders under *Tools & Software*.

10.1.2 Device Nomenclature

Table 3. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS715A-NM**xxyyyz**	**xx** is nominal output voltage (for example 33 = 3.3V, 01 = adjustable) **yyy** is package designator **z** is package quantity

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- *TPS715AxxEVM User Guide*, SLVU122
- *LDO Noise Demystified*, SLAA412
- *LDO PSRR Measurement Simplified*, SLAA414
- *A Topical Index of TI LDO Application Notes*, SBVA026

10.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS715A01DRBT-NM	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	ANONM
TPS715A01DRBT-NM.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	ANONM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

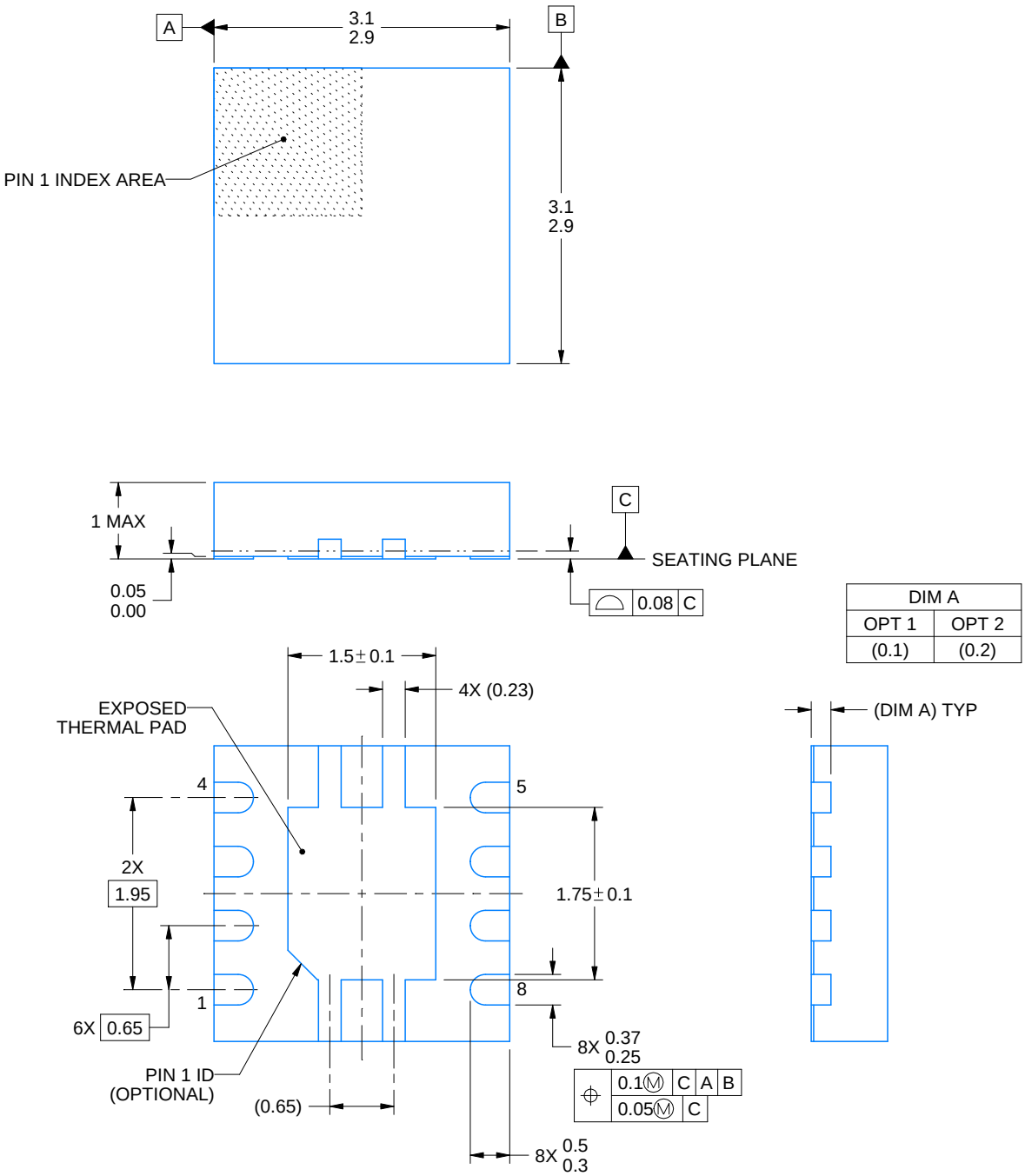
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

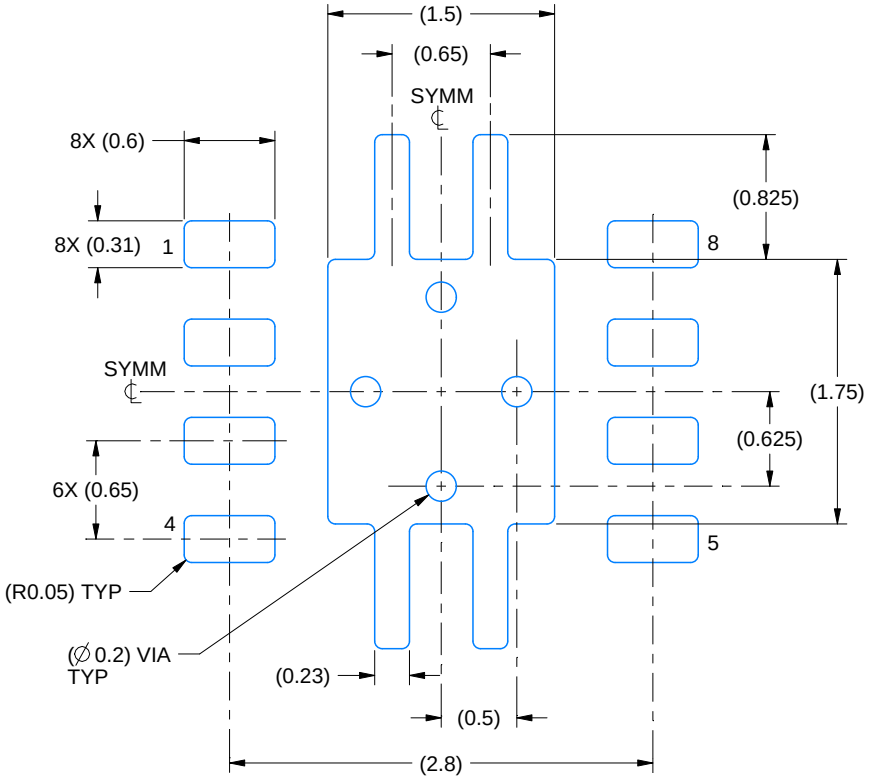
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

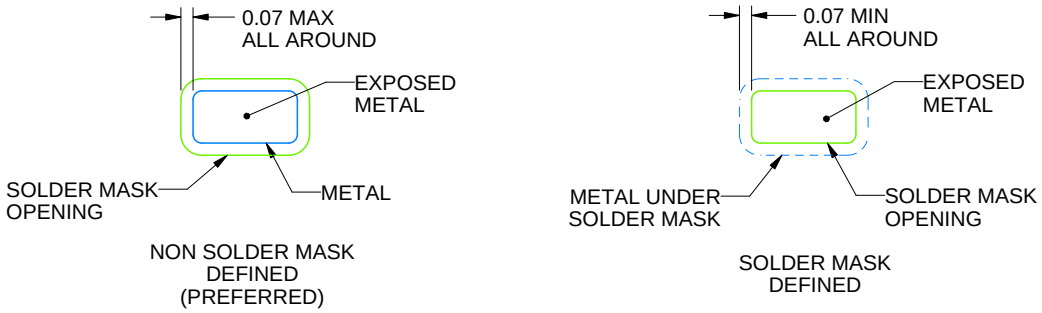
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

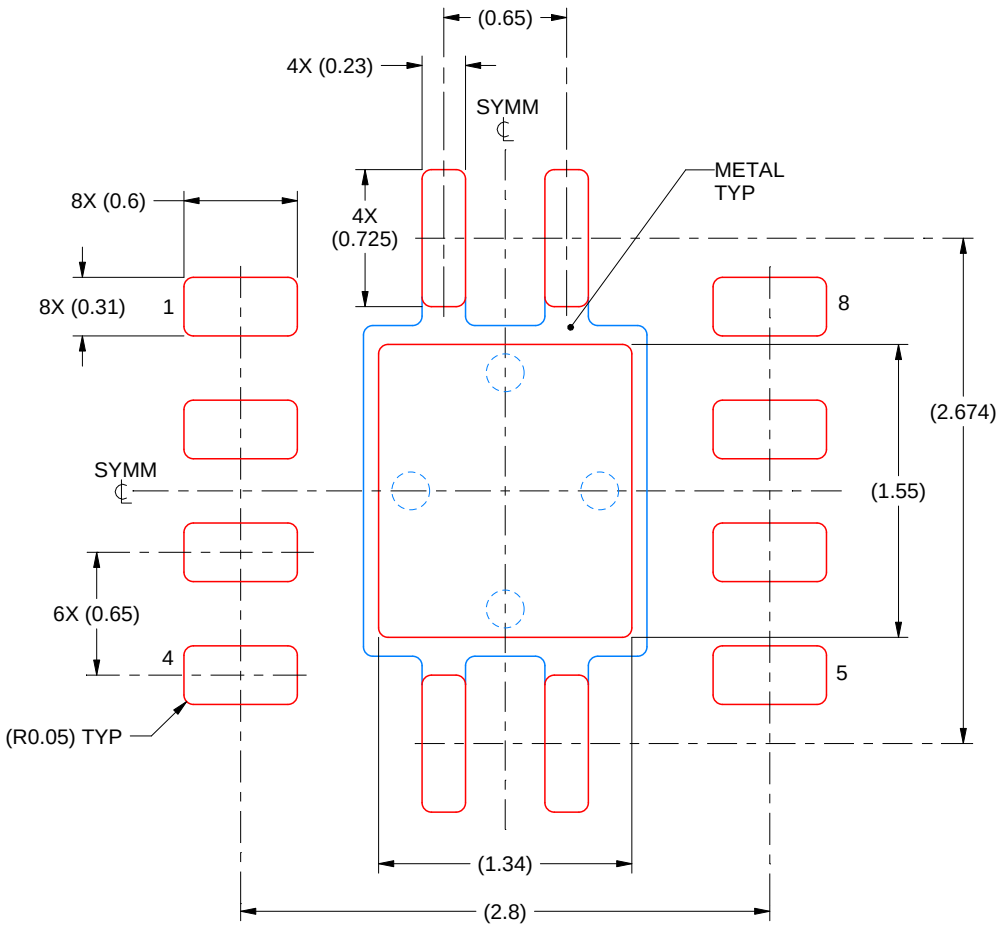


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025