TPS732 Capacitor-Free, NMOS, 250mA, Low-Dropout Regulator With Reverse Current Protection

1 Features

- Stable with no output capacitor or any value or type of capacitor
- Input voltage range: 1.7V to 5.5V
- Ultra-low dropout voltage: 40mV typical at 250mA
- Excellent load transient response—with or without optional output capacitor
- NMOS topology provides low reverse leakage current
- Low noise: 30μV_{RMS} typical (from 10kHz to 100kHz)
- 0.5% initial accuracy
- 1% overall accuracy (line, load, and temperature)
- Less than 1µA maximum I_Q in shutdown mode
- Thermal shutdown and specified minimum and maximum current limit protection
- Available in multiple output voltage versions:
  - Fixed outputs from 1.2V to 5V
  - Adjustable outputs from 1.2V to 5.5V
  - Custom outputs available

2 Applications

- Portable and battery-powered equipment
- Post-regulation for switching supplies
- Noise-sensitive circuitry such as VCOs
- Point of load regulation for DSPs, FPGAs, ASICs, and microprocessors

3 Description

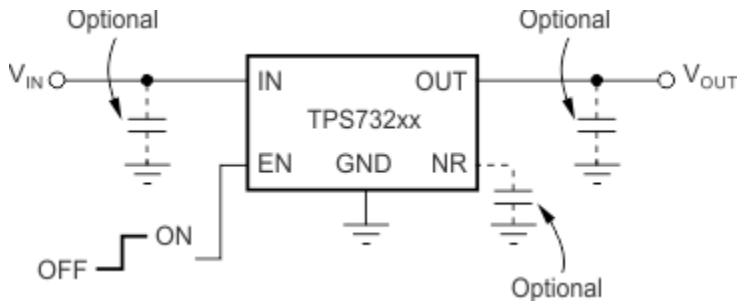
The TPS732 low-dropout (LDO) voltage regulator uses an NMOS pass transistor in a voltage-follower configuration. This topology is stable using output capacitors with low equivalent series resistance (ESR), and even allows operation without a capacitor. The device also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

The TPS732 uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is less than 1µA and designed for portable applications. The extremely low output noise (30μV_{RMS} with 0.1µF C_{NR}) is designed for powering VCOs. This device is protected by thermal shutdown and foldback current limit.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS732	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DCQ (SOT-223, 6)	6.5mm × 7.06mm
	DRB (VSON, 8)	3mm × 3mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit for Fixed-Voltage Versions

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

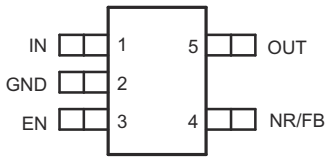


Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)

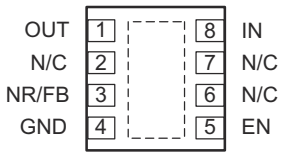


Figure 4-2. DRB Package, 8-Pin VSON With Exposed Thermal Pad (Top View)

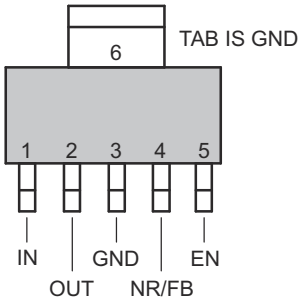


Figure 4-3. DCQ Package, 6-Pin SOT-223 (Top View)

Table 4-1. Pin Functions

PIN				TYPE[1]	DESCRIPTION
NAME	NO.				
	SOT-23	SOT-223	VSON		
EN	3	5	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See the *Enable Pin and Shutdown* section under *Feature Description* for more details. Connect EN to IN if not used.
FB	4	4	3	I	Adjustable voltage version only—this pin is the input to the control loop error amplifier, and is used to set the output voltage of the device.
GND	2	3, 6	4, Pad	—	Ground.
IN	1	1	8	I	Input supply.
NR	4	4	3	—	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal band gap, reducing output noise to very low levels.
OUT	5	2	1	O	Output of the regulator. There are no output capacitor requirements for stability.

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6	V
	Enable, V_{EN}	–0.3	6	
	Output, V_{OUT}	–0.3	5.5	
	V_{NR}, V_{FB}	–0.3	6	
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.7		5.5	V
I_{OUT}	Output current	0		250	mA
T_J	Operating junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS732 New silicon			UNIT
		DRB (VSON)	DCQ (SOT-223)	DBV (SOT-23)	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.4	76	185.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.6	46.6	82.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.0	18.1	53.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.8	8.6	21.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	17.6	52.7	°C/W

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5.4 Thermal Information (continued)

THERMAL METRIC[1]		TPS732 New silicon			UNIT
		DRB (VSON)	DCQ (SOT-223)	DBV (SOT-23)	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Thermal Information

THERMAL METRIC[1] [2]		TPS732 Legacy silicon[3]			UNIT
		DRB (VSON)	DCQ (SOT-223)	DBV (SOT-23)	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.3	53.1	205.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.8	35.2	119	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.8	7.8	35.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.7	2.9	12.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25	7.7	34.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the DRB, DCQ, and DBV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:

a. i. DRB: The exposed pad is connected to the PCB ground layer through a 2×2 thermal via array.
ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3×2 thermal via array.
iii. DBV: There is no exposed pad with the DBV package.

b. i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
iii. DBV: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.

c. These data are generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, see the Power Dissipation section of this datasheet.

5.6 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V[1] , I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted). Typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range[1]			1.7		5.5	V
V_{FB}	Internal reference (TPS73201)	T_J = 25°C		1.198	1.204	1.210	V
V_{OUT}	Output voltage range (TPS73201) [2]			V_{FB}		5.5 - V_{DO}	V
	Accuracy[1] [3]	Nominal	T_J = 25°C	–0.5		0.5	%
		V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V; 10mA ≤ I_{OUT} ≤ 250mA	–1	±0.5	1	

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5.6 Electrical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V(1) , I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted). Typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{OUT(\Delta VIN)}$	Line regulation (1)	$V_{OUT(nom)}$ + 0.5V ≤ V_{IN} ≤ 5.5V		0.01		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	1mA ≤ I_{OUT} ≤ 250mA		0.002		%/mA
		10mA ≤ I_{OUT} ≤ 250mA		0.0005		
V_{DO}	Dropout voltage(4) (V_{IN} = $V_{OUT(NOM)}$ - 0.1V)	I_{OUT} = 250mA		40	150	mV
$Z_{O(DO)}$	Output impedance in dropout	1.7V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$	250	425	600	mA
I_{SC}	Short-circuit current	V_{OUT} = 0V		300		mA
I_{REV}	Reverse leakage current(5) ($-I_{IN}$)	V_{EN} ≤ 0.5V, 0V ≤ V_{IN} ≤ V_{OUT}		0.1	10	µA
I_{GND}	Ground pin current	I_{OUT} = 10mA (I_Q), legacy silicon		400	550	µA
		I_{OUT} = 10mA (I_Q), new silicon		400	630	
I_{GND}	Ground pin current	I_{OUT} = 10mA (I_Q), V_{OUT} = 5V only, new silicon		580	700	µA
I_{GND}	Ground pin current	I_{OUT} = 250mA		650	950	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5V, –40°C ≤ T_J ≤ 100°C, legacy silicon		0.02	1	µA
		V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5V, new silicon		0.02	1	
I_{FB}	Feedback pin current (TPS73201)			0.1	0.3	µA
PSRR	Power-supply rejection ratio (ripple rejection)	f = 100Hz, I_{OUT} = 250mA		58		dB
		f = 10kHz, I_{OUT} = 250mA		37		
V_N	Output noise voltage, BW = 10Hz to 100kHz	C_{OUT} = 10µF, no C_{NR}		27 × V_{OUT}		μV_{RMS}
		C_{OUT} = 10µF, C_{NR} =0.01µF		8.5 × V_{OUT}		
$V_{EN(high)}$	EN pin high (enabled)		1.7		V_{IN}	V
$V_{EN(low)}$	EN pin low (shutdown)		0		0.5	V
$I_{EN(high)}$	Enable pin current (enabled)	V_{EN} = 5.5V		0.02	0.1	µA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		
T_J	Operating junction temperature		–40		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7V, whichever is greater.
(2) TPS73201 is tested at V_{OUT} = 2.5V.
(3) Tolerance of external resistors not included in this specification.
(4) V_{DO} is not measured for output versions with $V_{OUT(nom)}$ < 1.8V, because minimum V_{IN} = 1.7V.
(5) Fixed-voltage versions only; refer to *Application Information* section for more information.

5.7 Switching Characteristics

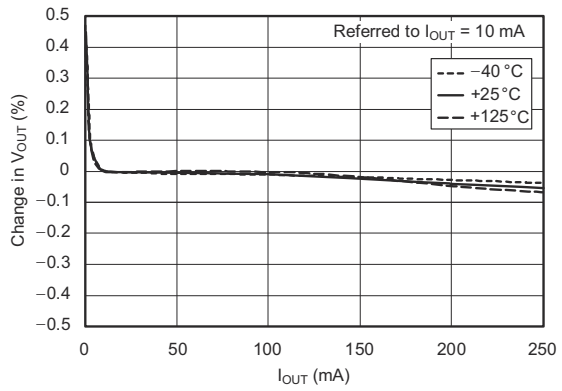
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-up time	V_{OUT} = 3V, R_L = 30Ω, C_{OUT} = 1µF, C_{NR} = 0.01µF		600		µs

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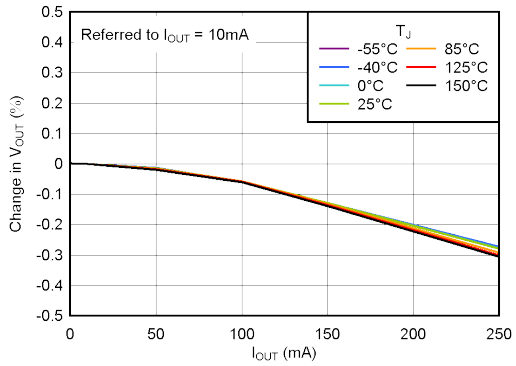
5.8 Typical Characteristics

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



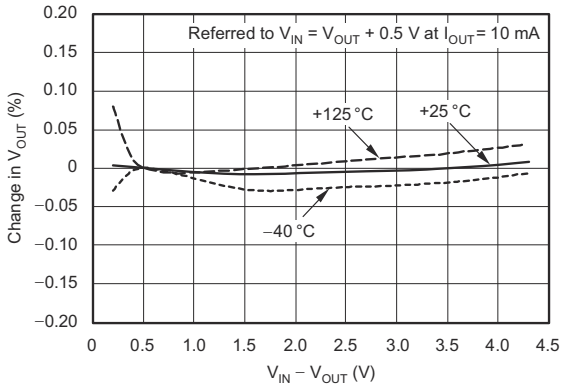
Legacy silicon

Figure 5-1. Load Regulation



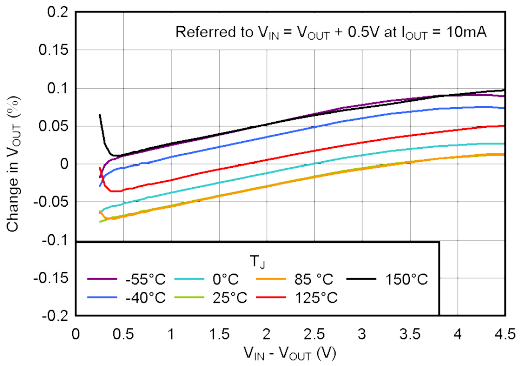
New silicon

Figure 5-2. Load Regulation



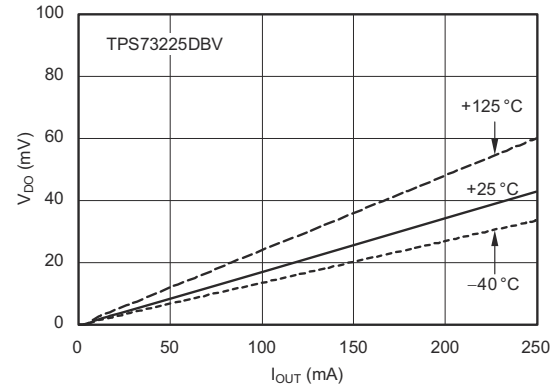
Legacy silicon

Figure 5-3. Line Regulation



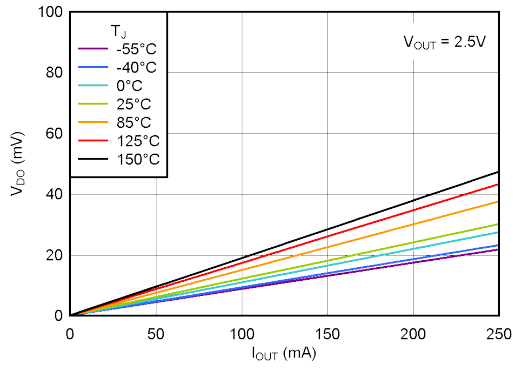
New silicon

Figure 5-4. Line Regulation



Legacy silicon

Figure 5-5. Dropout Voltage vs Output Current



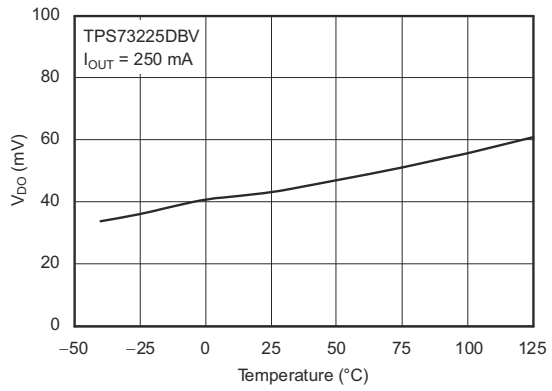
New silicon

Figure 5-6. Dropout Voltage vs Output Current

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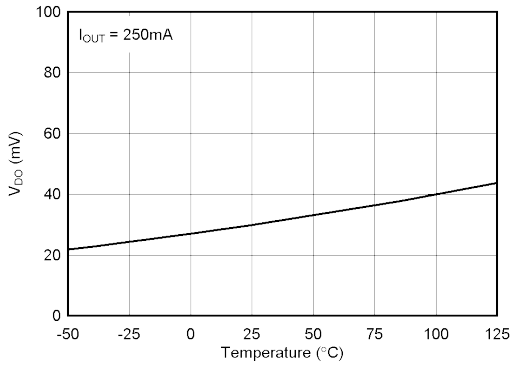
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



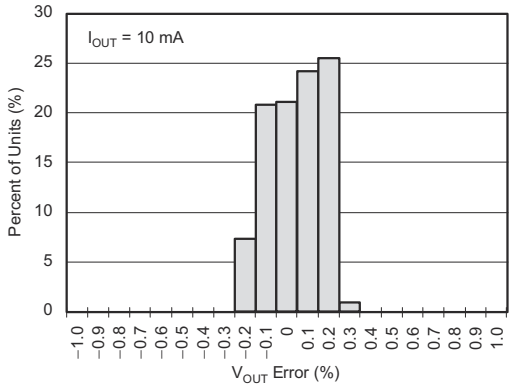
Legacy silicon

Figure 5-7. Dropout Voltage vs Temperature



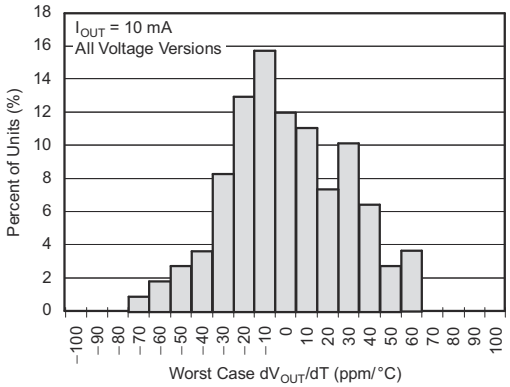
New silicon

Figure 5-8. Dropout Voltage vs Temperature



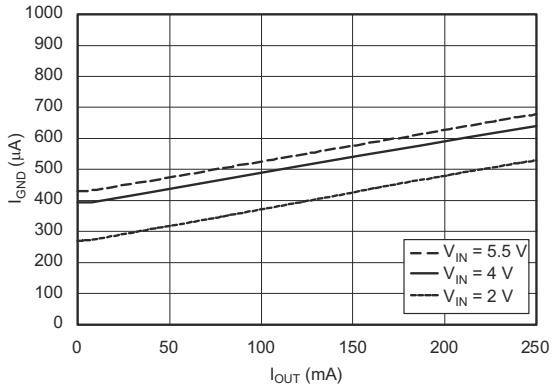
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Figure 5-9. Output Voltage Accuracy Histogram



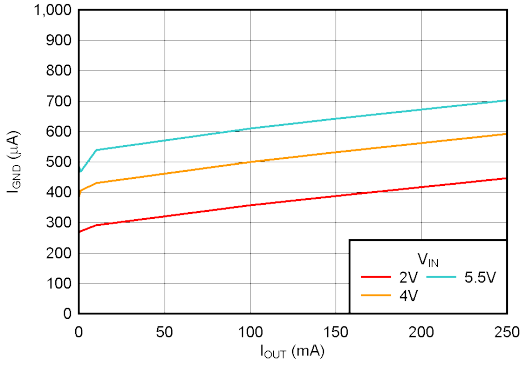
Legacy silicon

Figure 5-10. Output Voltage Drift Histogram



Legacy silicon

Figure 5-11. Ground Pin Current vs Output Current



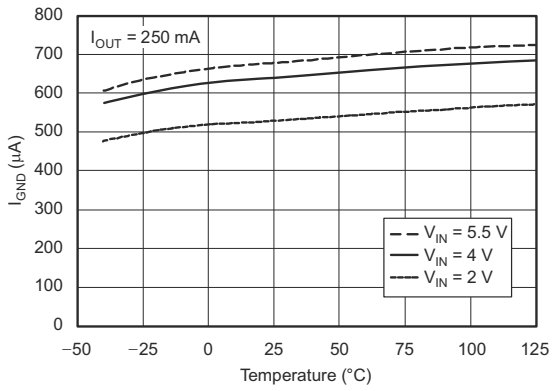
New silicon

Figure 5-12. Ground Pin Current vs Output Current

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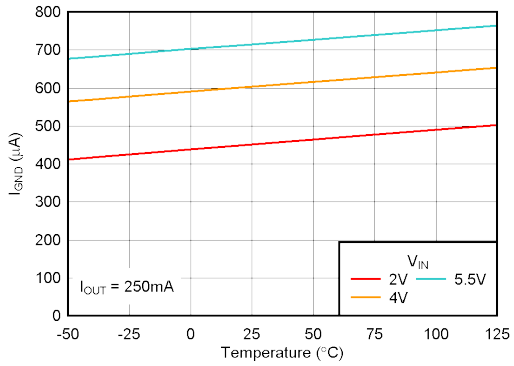
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



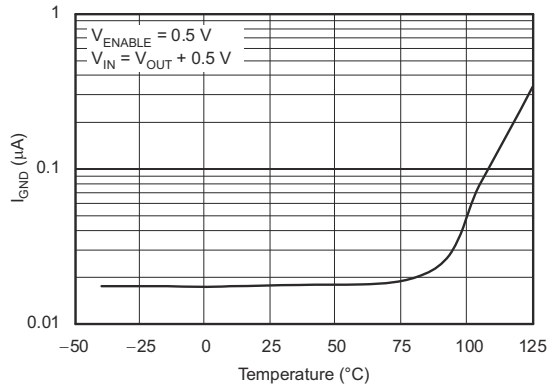
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Figure 5-13. Ground Pin Current vs Temperature



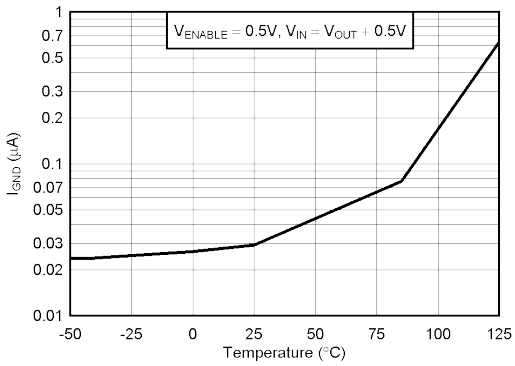
New silicon

Figure 5-14. Ground Pin Current vs Temperature



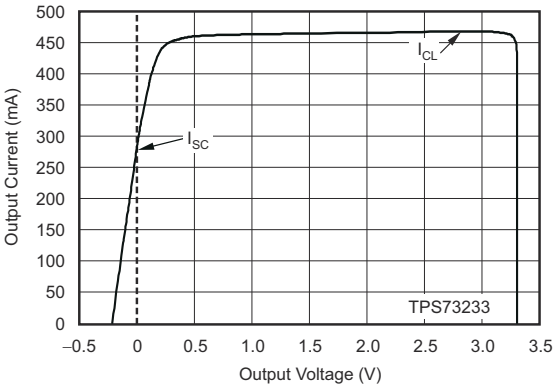
Legacy silicon

Figure 5-15. Ground Pin Current in Shutdown vs Temperature



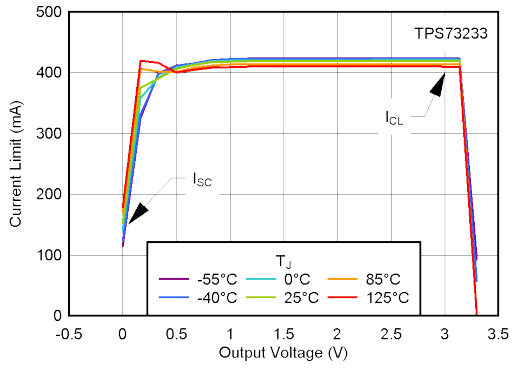
New silicon

Figure 5-16. Ground Pin Current in Shutdown vs Temperature



Legacy silicon

Figure 5-17. Current Limit vs V_{OUT} (Foldback)



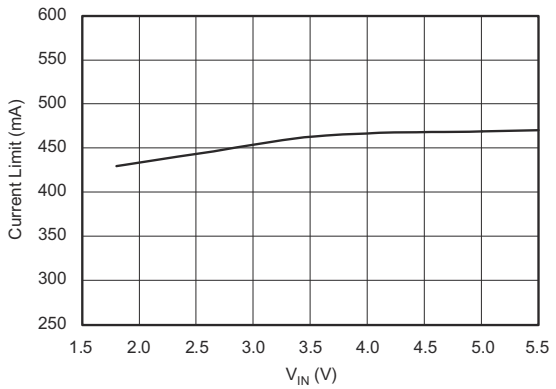
New silicon

Figure 5-18. Current Limit vs V_{OUT} (Foldback)

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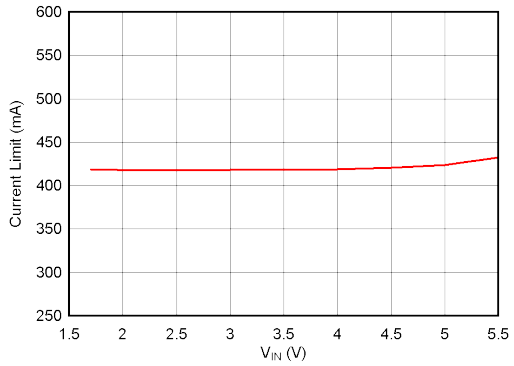
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



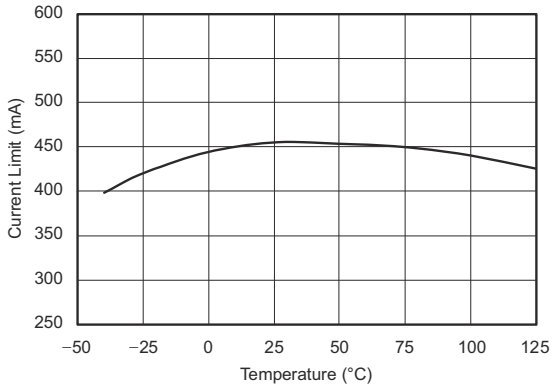
Legacy silicon

Figure 5-19. Current Limit vs V_{IN}



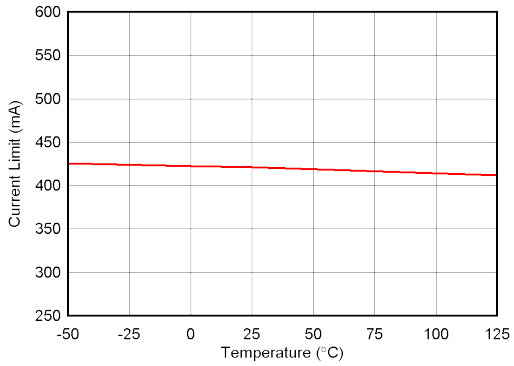
New silicon

Figure 5-20. Current Limit vs V_{IN}



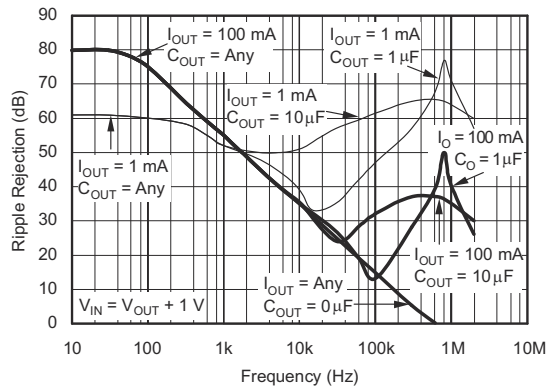
Legacy silicon

Figure 5-21. Current Limit vs Temperature



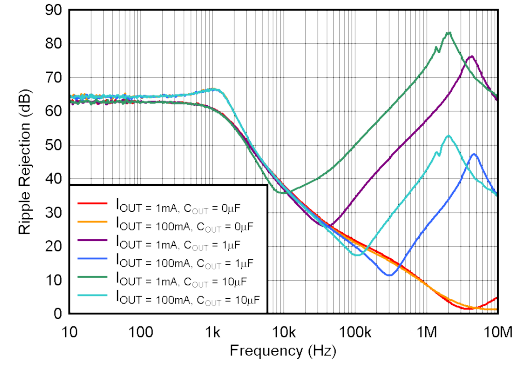
New silicon

Figure 5-22. Current Limit vs Temperature



Legacy silicon

Figure 5-23. PSRR (Ripple Rejection) vs Frequency



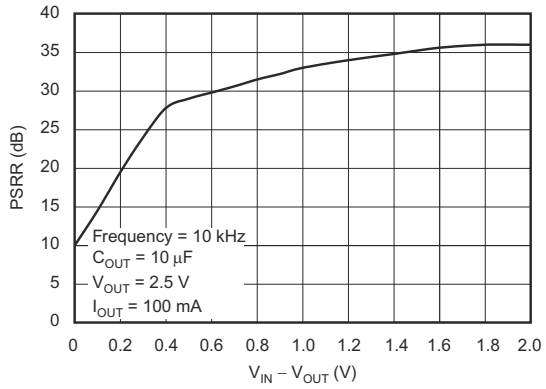
New silicon

Figure 5-24. PSRR (Ripple Rejection) vs Frequency

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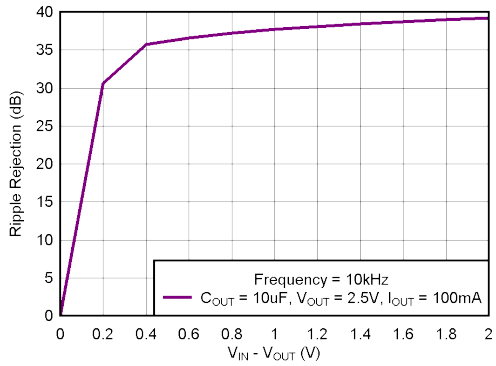
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



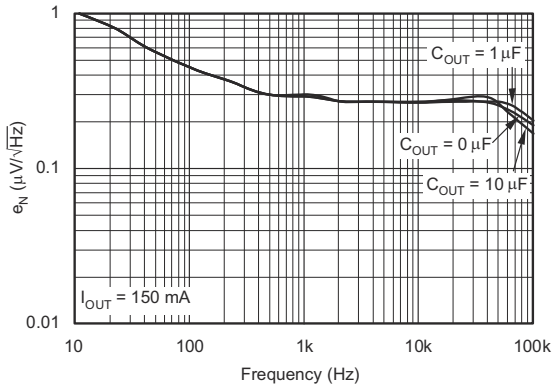
Legacy silicon

Figure 5-25. PSRR (Ripple Rejection) vs (V_{IN} – V_{OUT})



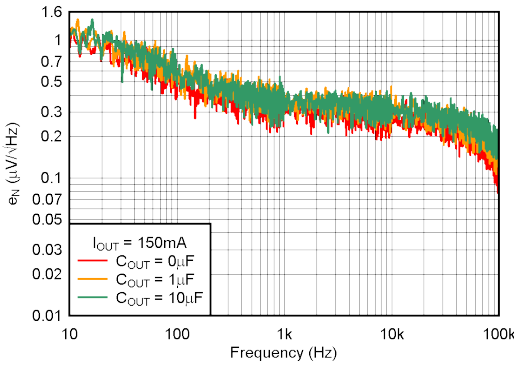
New silicon

Figure 5-26. PSRR (Ripple Rejection) vs (V_{IN} – V_{OUT})



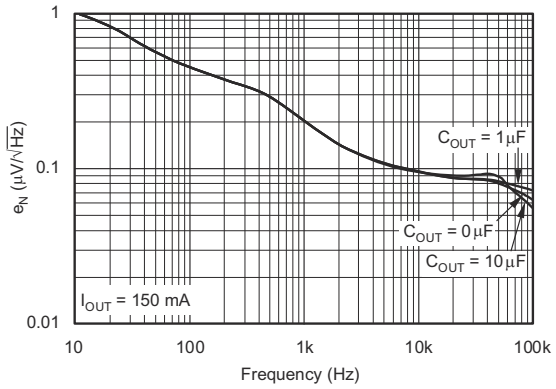
Legacy silicon

Figure 5-27. Noise Spectral Density C_{NR} = 0µF



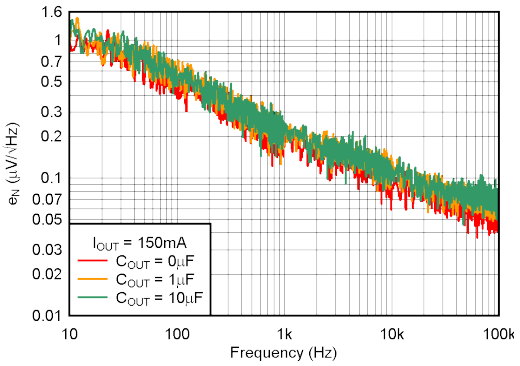
New silicon

Figure 5-28. Noise Spectral Density C_{NR} = 0µF



Legacy silicon

Figure 5-29. Noise Spectral Density C_{NR} = 0.01µF



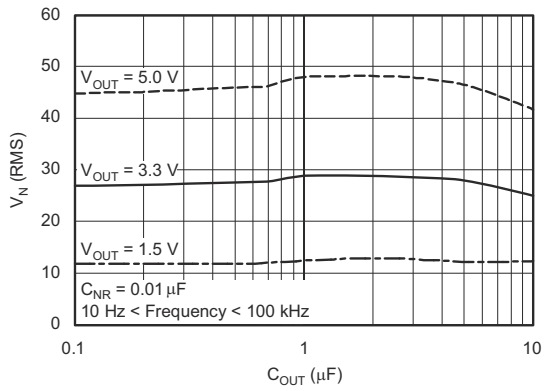
New silicon

Figure 5-30. Noise Spectral Density C_{NR} = 0.01µF

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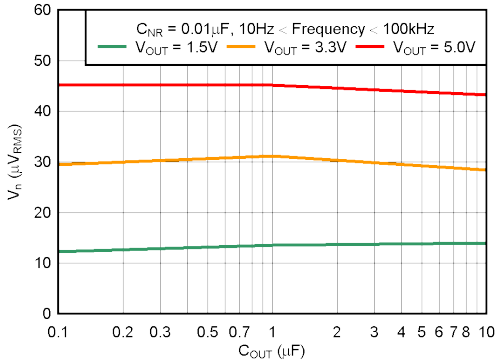
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



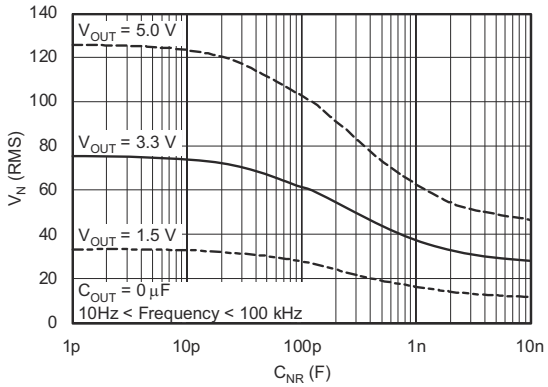
Legacy silicon

Figure 5-31. RMS Noise Voltage vs C_{OUT}



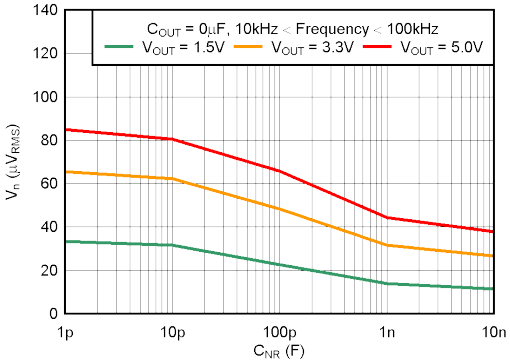
New silicon

Figure 5-32. RMS Noise Voltage vs C_{OUT}



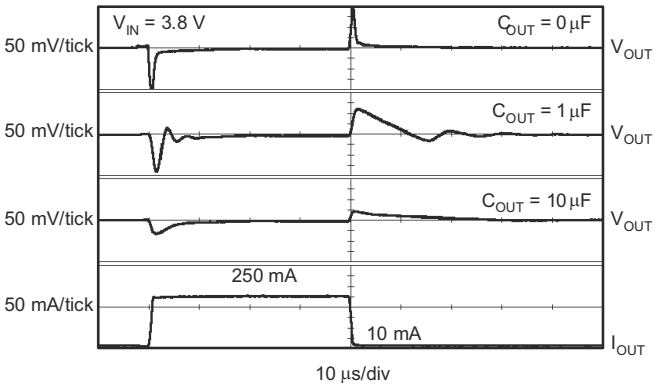
Legacy silicon

Figure 5-33. RMS Noise Voltage vs C_{NR}



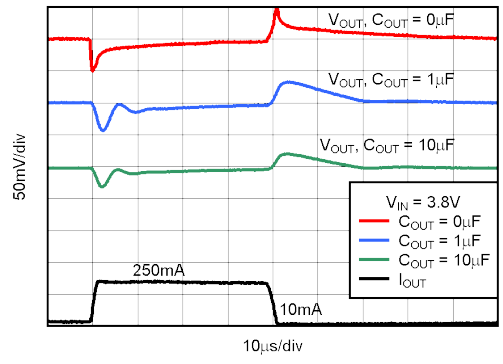
New silicon

Figure 5-34. RMS Noise Voltage vs C_{NR}



Legacy silicon

Figure 5-35. TPS73233 Load Transient Response



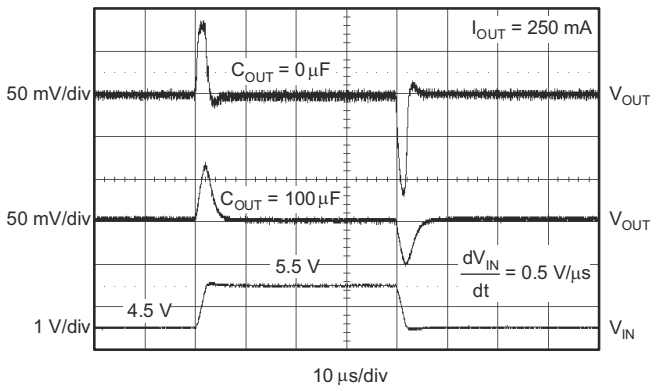
New silicon

Figure 5-36. TPS73233 Load Transient Response

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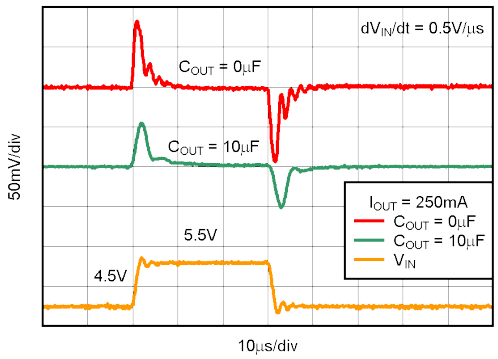
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



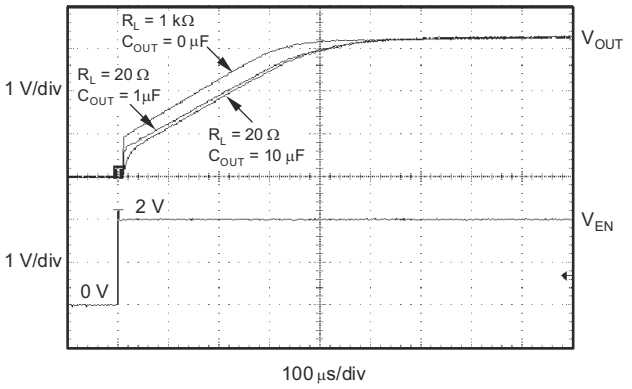
Legacy silicon

Figure 5-37. TPS73233 Line Transient Response



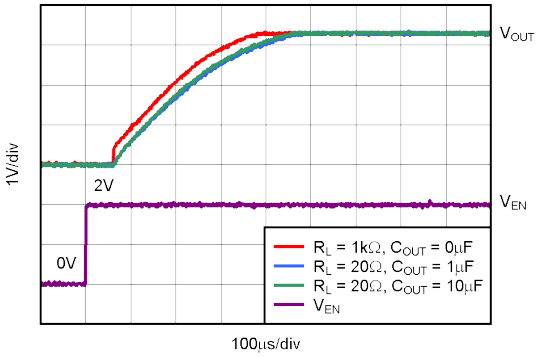
New silicon

Figure 5-38. TPS73233 Line Transient Response



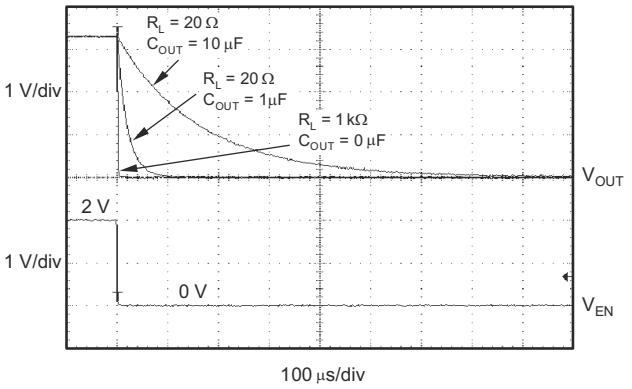
Legacy silicon

Figure 5-39. TPS73233 Turn-On Response



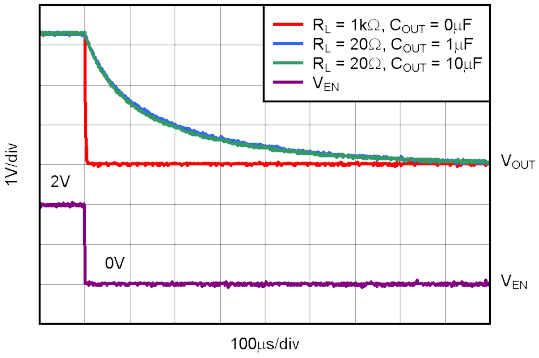
New silicon

Figure 5-40. TPS73233 Turn-On Response



Legacy silicon

Figure 5-41. TPS73233 Turn-Off Response



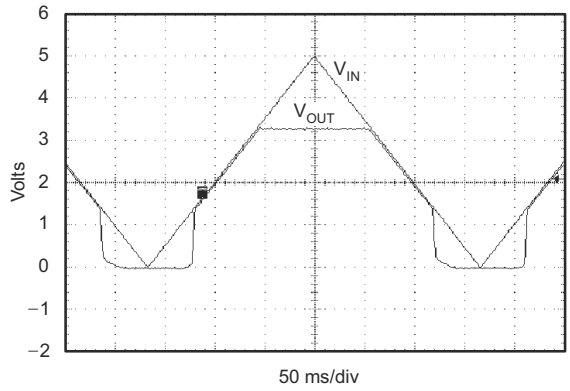
New silicon

Figure 5-42. TPS73233 Turn-Off Response

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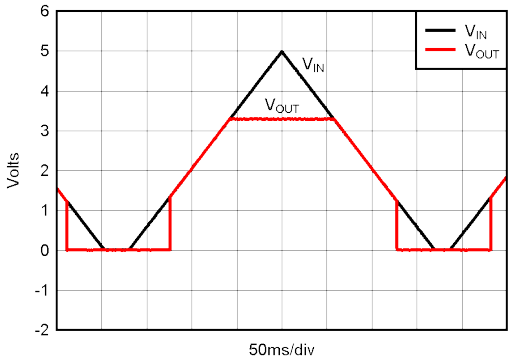
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



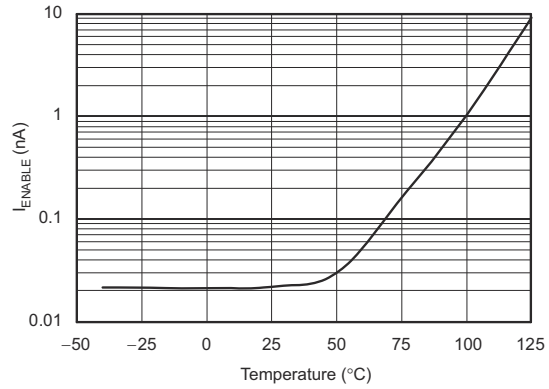
Legacy silicon

Figure 5-43. TPS73233 Power-Up and Power-Down



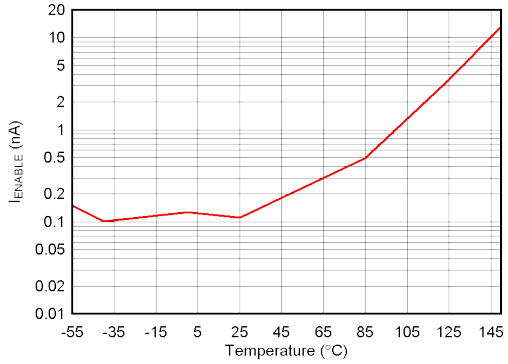
New silicon

Figure 5-44. TPS73233 Power-Up and Power-Down



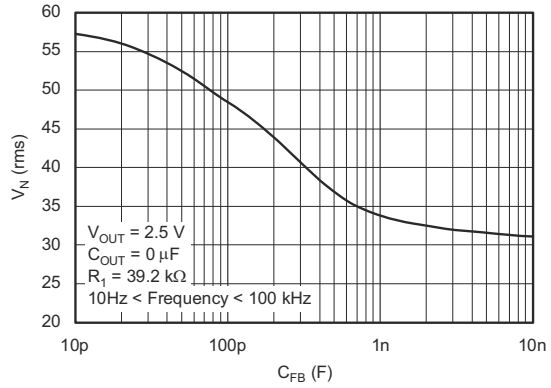
Legacy silicon

Figure 5-45. I_{ENABLE} vs Temperature



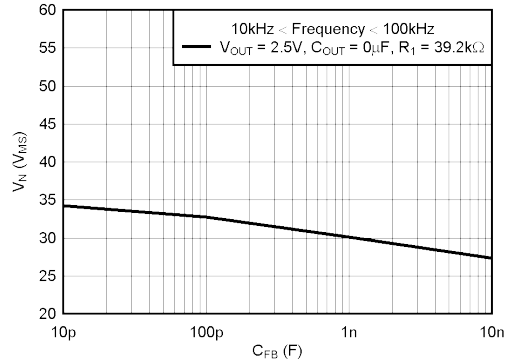
New silicon

Figure 5-46. I_{ENABLE} vs Temperature



Legacy silicon

Figure 5-47. TPS73201 RMS Noise Voltage vs C_{FB}



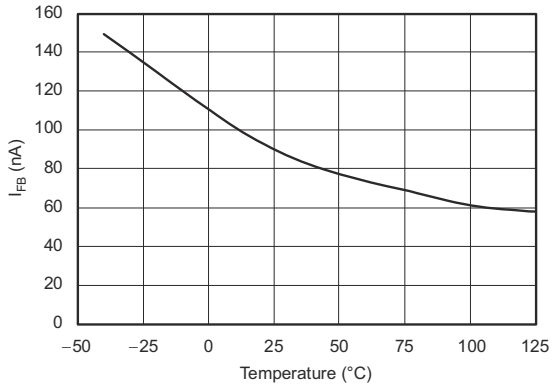
New silicon

Figure 5-48. TPS73201 RMS Noise Voltage vs C_{FB}

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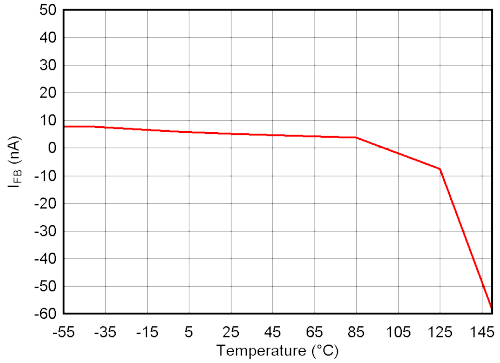
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



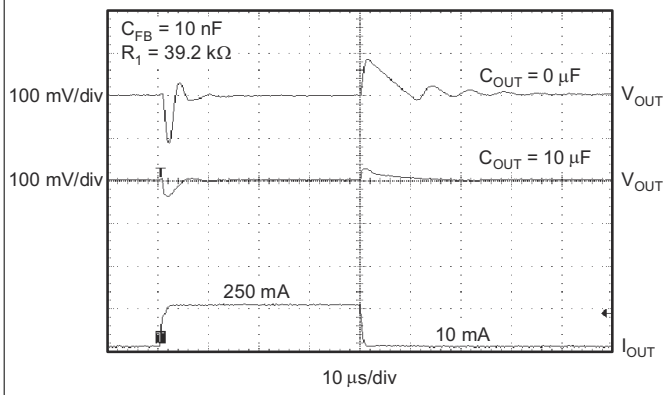
Legacy silicon

Figure 5-49. TPS73201 I_{FB} vs Temperature



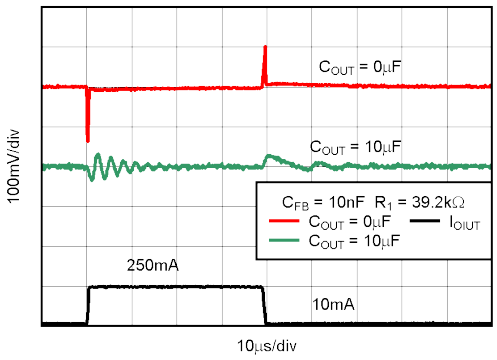
New silicon

Figure 5-50. TPS73201 I_{FB} vs Temperature



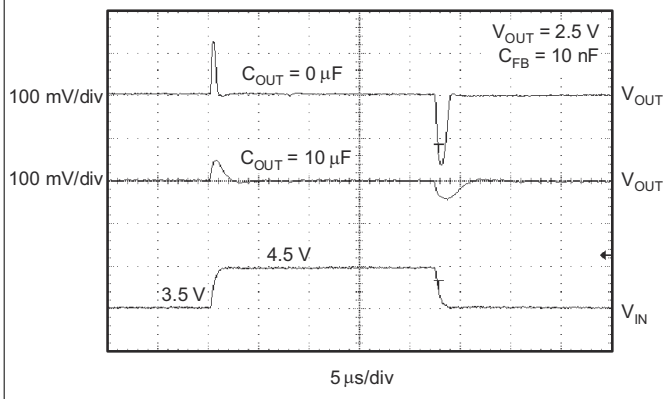
Legacy silicon

Figure 5-51. TPS73201 Load Transient, Adjustable Version



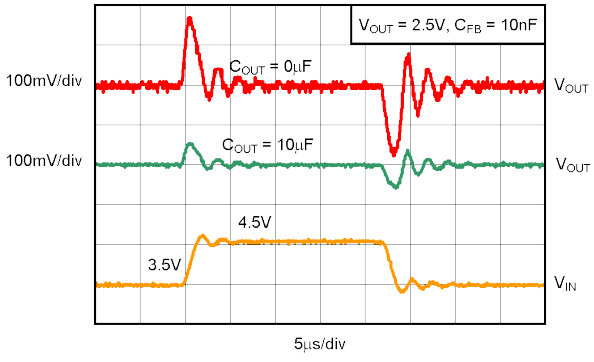
New silicon

Figure 5-52. TPS73201 Load Transient, Adjustable Version



Legacy silicon

Figure 5-53. TPS73201 Line Transient, Adjustable Version



New silicon

Figure 5-54. TPS73201 Line Transient, Adjustable Version

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6 Detailed Description

6.1 Overview

The TPS732 low-dropout linear regulator operates down to an input voltage of 1.7V and supports output voltages down to 1.2V while sourcing up to 250mA of load current. This linear regulator uses an NMOS pass transistor with an integrated 4MHz charge pump to provide a dropout voltage of less than 150mV at full load current. This unique architecture also permits stable regulation over a wide range of output capacitors. Furthermore, the TPS732 does not require any output capacitor for stability. The increased insensitivity to the output capacitor value and type makes this linear regulator designed for powering a load where the effective capacitance is unknown.

The TPS732 also features a noise-reduction (NR) pin that allows for additional reduction of the output noise. With a noise reduction capacitor of 0.01µF connected from the NR pin to GND, the TPS73215 typical output noise is 12.75µV_{RMS}. The low noise output featured by the TPS732 makes the device designed for powering VCOs or any other noise-sensitive load.

6.2 Functional Block Diagrams

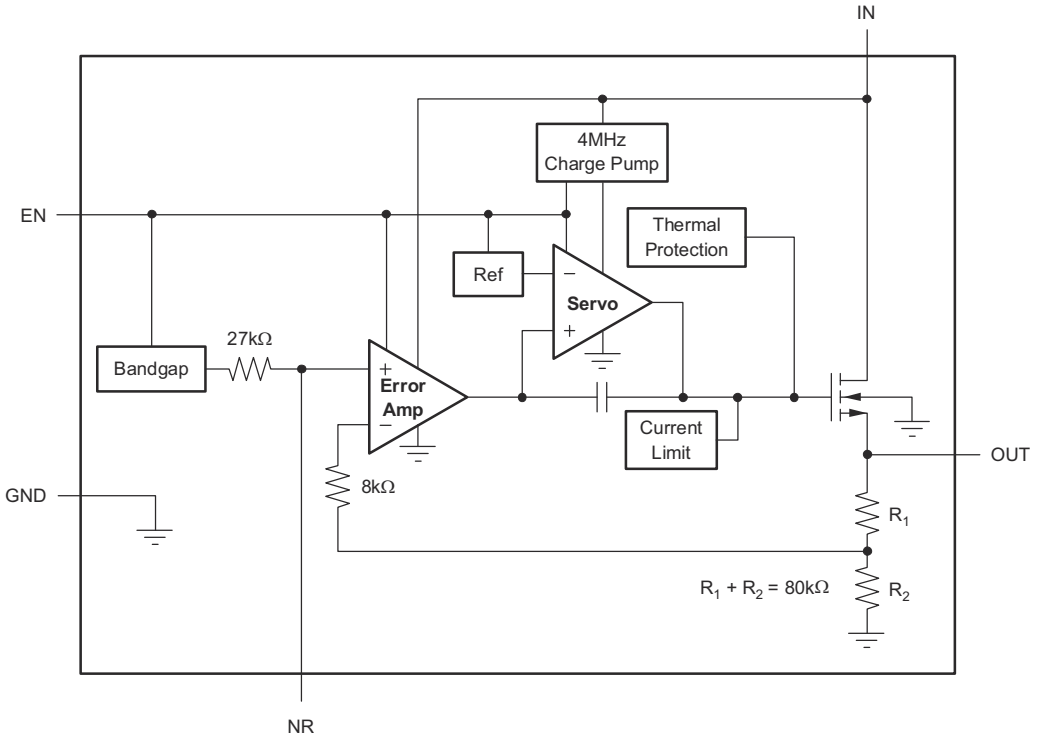


Figure 6-1. Fixed-Voltage Version

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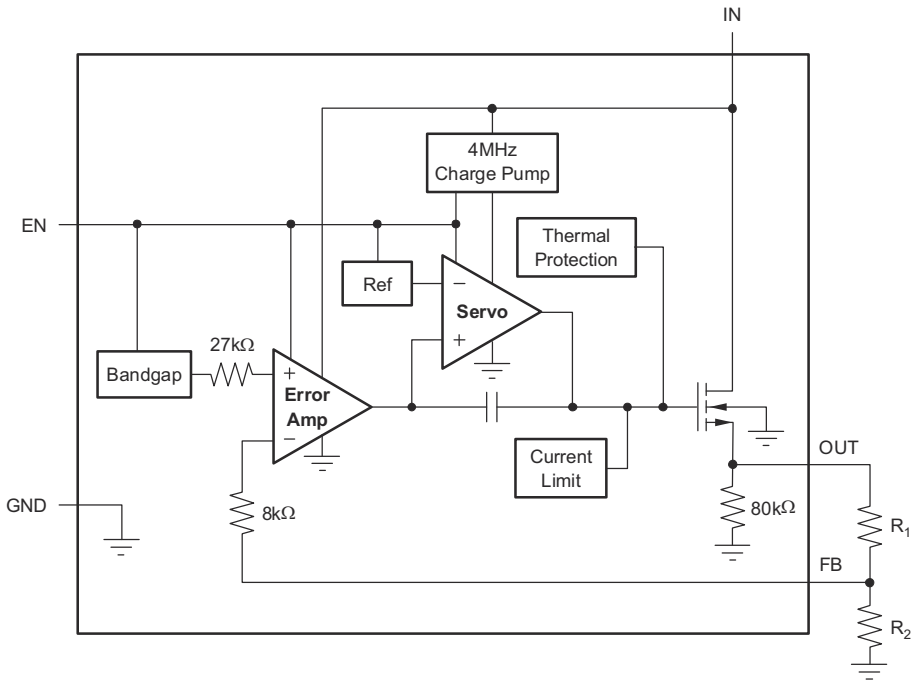


Table 1. Standard 1% Resistor Values for Common Output Voltages

V_O	R_1	R_2
1.2V	Short	Open
1.5V	23.2kΩ	95.3kΩ
1.8V	28.0kΩ	56.2kΩ
2.5V	39.2kΩ	36.5kΩ
2.8V	44.2kΩ	33.2kΩ
3.0V	46.4kΩ	30.9kΩ
3.3V	52.3kΩ	30.1kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1 || R_2 \cong 19k\Omega$ for best accuracy.

Figure 6-2. Adjustable-Voltage Version

6.3 Feature Description

6.3.1 Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS732 and generates approximately $32\mu V_{RMS}$ (10Hz to 100kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_{IN} = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Because the value of V_{REF} is 1.2V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (2)$$

An internal 27kΩ resistor in series with the noise-reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise-reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

for C_{NR} = 10nF.

This noise-reduction effect is shown as *RMS Noise Voltage vs C_{NR}* (Figure 5-33) in the Typical Characteristics section.

The TPS73201 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the feedback pin (FB) reduces output noise and improves load transient performance.

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The TPS732 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass transistor above V_{OUT}. The charge pump generates approximately 250µV of switching noise at approximately 4MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

6.3.2 Internal Current Limit

The TPS732 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5V. See Figure 5-17 in the *Typical Characteristics* section for a graph of I_{OUT} vs V_{OUT}.

From Figure 5-17 approximately –0.2V of V_{OUT} results in a current limit of 0mA. Therefore, if OUT is forced below –0.2V before EN goes high, the device potentially does not start up. In applications that work with both a positive and negative voltage supply, enable the TPS732 first.

6.3.3 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5V (maximum) turns the regulator off and drops the GND pin current to approximately 10nA. When EN is used to shut down the regulator, all charge is removed from the pass transistor gate. A V_{EN} above 1.7V (minimum) turns the regulator on and the output ramps back up to a regulated V_{OUT} (see Figure 5-39).

When shutdown capability is not required, connect EN to V_{IN}. However, the pass transistor potentially does not discharge using this configuration, causing the pass transistor to be left on (enhanced) for a significant time after V_{IN} is removed. This scenario results in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output potentially overshoots upon power up.

Current limit foldback prevents device start-up under some conditions. See the *Internal Current Limit* section.

6.3.4 Dropout Voltage

The TPS732 uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass transistor is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the NMOS pass transistor.

For large step changes in load current, the TPS732 requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the DC dropout. Values of (V_{IN} – V_{OUT}) above this line provide normal transient response.

Operating in the transient dropout region causes an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to DC dropout levels], the TPS732 takes a couple of hundred microseconds to return to the specified regulation accuracy.

6.3.5 Reverse Current

The NMOS pass transistor of the TPS732 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass transistor is pulled low. To make sure all charge is removed from the gate of the pass transistor, drive the EN pin low before the input voltage is removed. If this process is not done, the pass transistor is potentially left on because of stored charge on the transistor.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Reverse current is specified as the current flowing out of the IN pin resulting from the voltage applied on the OUT pin. Additional current flows into the OUT pin from the 80kΩ internal resistor divider to ground (see Figure 6-1 and Figure 6-2).

For the TPS73201, reverse current potentially flows when V_{FB} is more than 1V above V_{IN}.

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6.4 Device Functional Modes

6.4.1 Normal Operation With 1.7V ≤ V_{IN} ≤ 5.5V and V_{EN} ≥ 1.7V

The TPS732 requires an input voltage of at least 1.7V to function properly and attempt to maintain regulation.

When operating the device near 5.5V, suppress any transient spikes that exceed the 6V absolute maximum voltage rating. Never operate the device at a DC voltage greater than 5.5V.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS732 LDO regulator uses an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS732 designed for portable applications. This regulator offers a wide selection of fixed-output voltage versions and an adjustable-output version. All versions have thermal and overcurrent protection, including foldback current limit.

7.2 Typical Application

Figure 7-1 shows the basic circuit connections for the fixed-voltage models. Figure 7-2 gives the connections for the adjustable-voltage version (TPS73201).

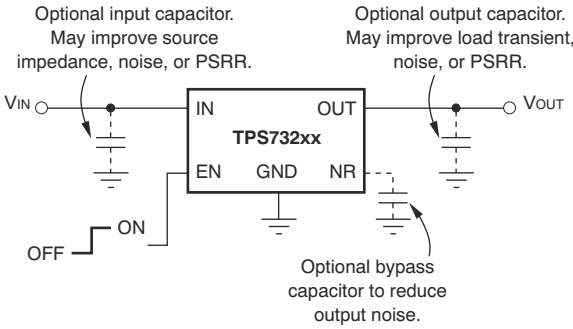


Figure 7-1. Typical Application Circuit for Fixed-Voltage Versions

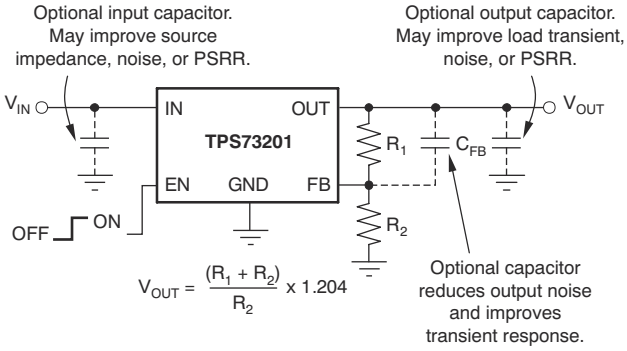


Figure 7-2. Typical Application Circuit for Adjustable-Voltage Version

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7.2.1 Design Requirements

R_1 and R_2 are calculated for any output voltage using the formula below. Sample resistor values for common output voltages are given in Figure 6-2.

$$V_{OUT} = \frac{(R_1 + R_2)}{R_2} \times 1.204 \quad (4)$$

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19kΩ. This 19kΩ, in addition to the internal 8kΩ resistor, presents the same impedance to the error amplifier as the 27kΩ band-gap reference output. This impedance helps compensate for leakages into the error amplifier terminals.

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1µF to 1µF, low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor is necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS732 does not require an output capacitor for stability and has maximum phase margin with no capacitor. The device is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing potentially occurs when the product of C_{OUT} and total ESR drops below 50nF × Ω. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

7.2.2.2 Transient Response

The low open-loop output impedance provided by the NMOS pass transistor in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1µF) from the OUT pin to ground reduces undershoot magnitude but increases the duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the OUT pin to the FB pin also improves transient response.

The TPS732 does not have active pulldown when the output is overvoltage. This feature allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This feature also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot is reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal or external load resistance. The rate of decay is given by:

(Fixed voltage versions)

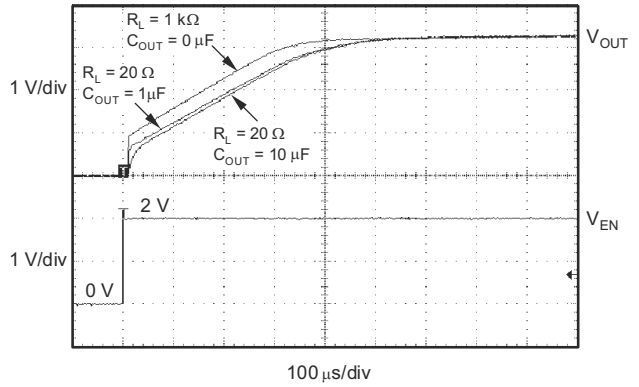
$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (5)$$

(Adjustable voltage version)

$$\frac{dV}{dt} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \left|\right| \left[R_1 + R_2\right] \left|\right| R_{LOAD}} \quad (6)$$

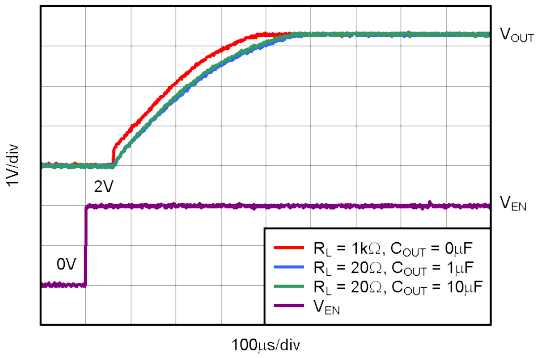
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7.2.3 Application Curves



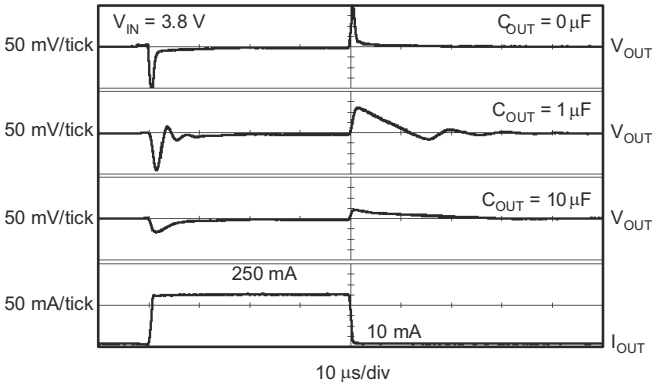
Legacy silicon

Figure 7-3. TPS73233 Turn-On Response



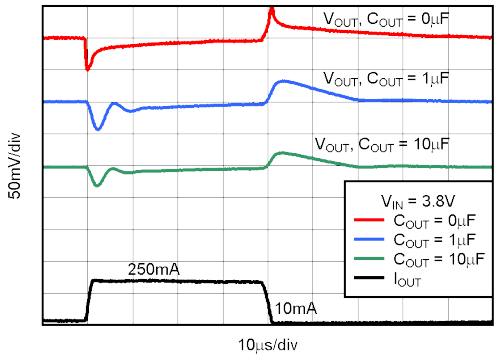
New silicon

Figure 7-4. TPS73233 Turn-On Response



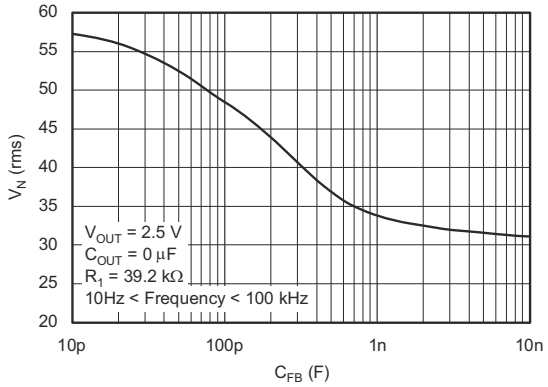
Legacy silicon

Figure 7-5. TPS73233 Load Transient Response



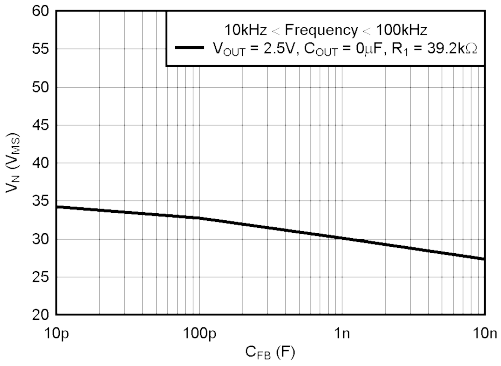
New silicon

Figure 7-6. TPS73233 Load Transient Response



Legacy silicon

Figure 7-7. TPS73201 RMS Noise Voltage vs C_{FB}

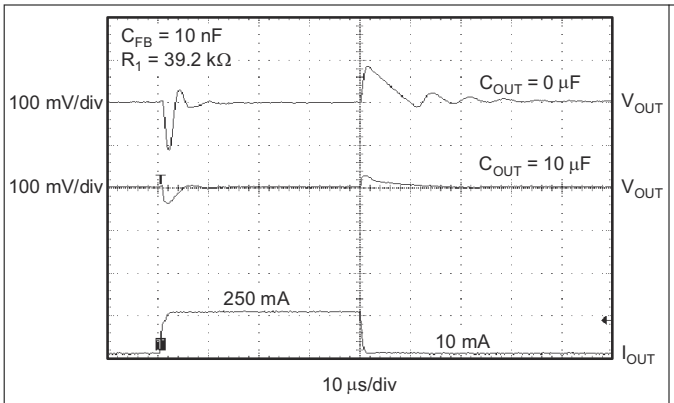


New silicon

Figure 7-8. TPS73201 RMS Noise Voltage vs C_{FB}

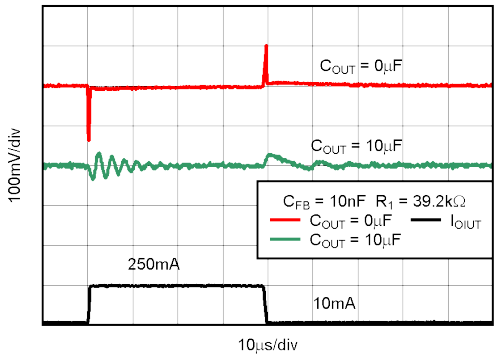
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7.2.3 Application Curves (continued)



Legacy silicon

Figure 7-9. TPS73201 Load Transient, Adjustable Version



New silicon

Figure 7-10. TPS73201 Load Transient, Adjustable Version

7.3 Power Supply Recommendations

This device is designed to operate from an input voltage supply range from 1.7V and 5.5V. The input voltage range provides adequate headroom for the device to have a regulated output. Make sure this input supply is well regulated. If the input supply is noisy, additional input capacitors with low ESR help improve output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

To improve AC performance such as PSRR, output noise, and transient response, design the PCB with ground plane connections for V_{IN} and V_{OUT} capacitors, and connect the ground plane at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

7.4.1.1 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit potentially cycles on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage caused by overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of the application. This level produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS732 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS732 into thermal shutdown degrades device reliability.

7.4.1.1.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat-sink effectiveness.

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Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass transistor (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (7)$$

Power dissipation is minimized by using the lowest possible input voltage necessary to provide the required output voltage.

7.4.2 Layout Examples

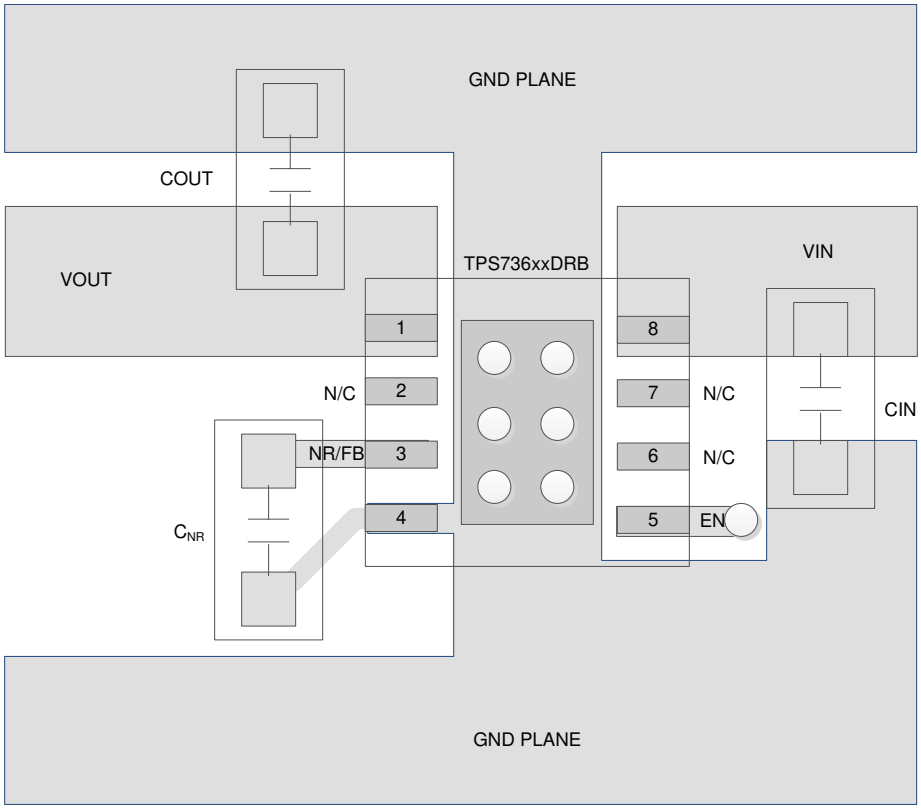


Figure 7-11. Fixed Output Voltage Option Layout (DRB Package)

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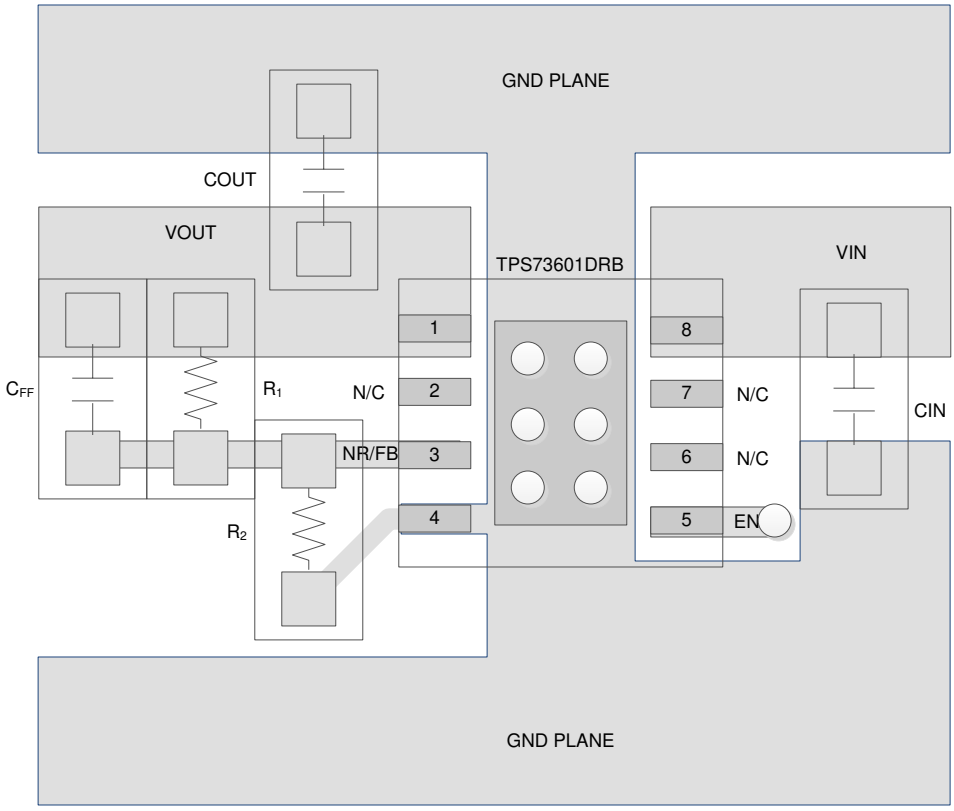


Figure 7-12. Adjustable Output Voltage Option Layout (DRB Package)

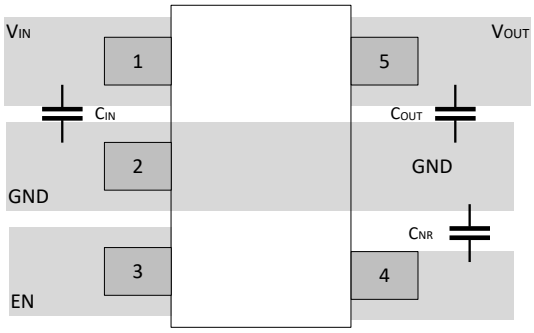


Figure 7-13. Layout Example for the DBV Package Fixed Version

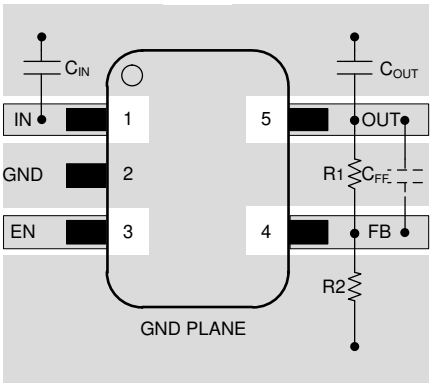


Figure 7-14. Layout Example for the DBV Package Adjustable Version

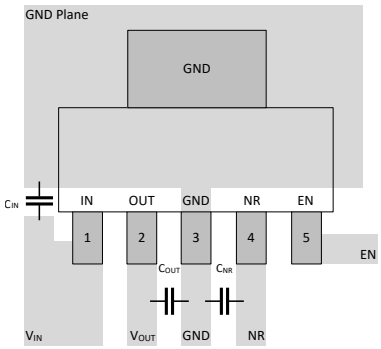


Figure 7-15. Layout Example for the DCQ Package Fixed Version

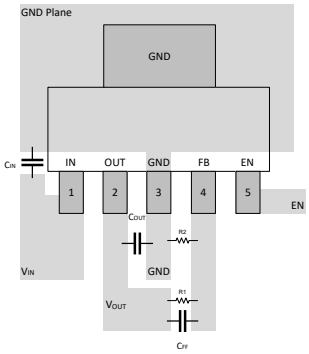


Figure 7-16. Layout Example for the DCQ Package Adjustable Version

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS732. Request the TPS73201DRBEVM-518 evaluation module (and related user guide) at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS732 is available through the product folders under *Simulation Models*.

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT(1)	DESCRIPTION
TPS732**xxyyyz*(M3)***	**xx** is the nominal output voltage (for example, 25 = 2.5V; 01 = Adjustable). **yyy** is the package designator. **z** is the tape and reel quantity (R = 3000, T = 250). **M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the *legacy silicon* (CSO: DLN) or the *new silicon* (CSO: RFB). The reel packaging label provides CSO information to distinguish which silicon is being used. Device performance for new and legacy silicon is denoted throughout the document.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, *Regulating V_{OUT} Below 1.2V Using an External Reference* application note
- Texas Instruments, *TPS73x01DRBEVM-518 User's Guide*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision R (May 2025) to Revision S (April 2026)	Page
• Added silicon 5V output ground current specification	5

Changes from Revision Q (September 2024) to Revision R (May 2025)	Page
• Added new silicon DBV thermals	4
• Updated DRB (VSON) for DRB0008A package outline	4
• Changed *legacy chip* to *legacy silicon* in *Device Nomenclature* table	27

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73201DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 125	PS73201
TPS73201DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	PS73201
TPS73201DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS73201
TPS73201DCQRM3	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73201
TPS73201DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DRBRG4	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DRBRM3	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DRBRM3.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ
TPS73201DRBT	Obsolete	Production	SON (DRB) | 8	-	-	Call TI	Call TI	-40 to 125	PJEQ
TPS73213DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BWD
TPS73213DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BWD
TPS73215DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T38
TPS73215DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T38
TPS73215DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 125	PS73215
TPS73215DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73215
TPS73215DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73215
TPS73216DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T50
TPS73216DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T50
TPS73216DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T50

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73218DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T37
TPS73218DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T37
TPS73218DBVRG4	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T37
TPS73218DBVRG4.A	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T37
TPS73218DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T37
TPS73218DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	T37
TPS73218DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 125	PS73218
TPS73218DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73218
TPS73218DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73218
TPS73219DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	CGE
TPS73219DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	CGE
TPS73219DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	CGE
TPS73219DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	CGE
TPS73225DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T36
TPS73225DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T36
TPS73225DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T36
TPS73225DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T36
TPS73225DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T36
TPS73225DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T36
TPS73225DBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T36
TPS73225DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 125	PS73225
TPS73225DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73225
TPS73225DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73225
TPS73230DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T39
TPS73230DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T39
TPS73230DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T39
TPS73230DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T39
TPS73230DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	T39
TPS73230DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73230
TPS73230DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73230
TPS73233DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T40

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73233DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T40
TPS73233DBVR1G4	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T40
TPS73233DBVR1G4.A	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T40
TPS73233DBVRM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T40
TPS73233DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T40
TPS73233DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T40
TPS73233DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 125	PS73233
TPS73233DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73233
TPS73233DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73233
TPS73250DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T41
TPS73250DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T41
TPS73250DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T41
TPS73250DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T41
TPS73250DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T41
TPS73250DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T41
TPS73250DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73250
TPS73250DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73250

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS732 :

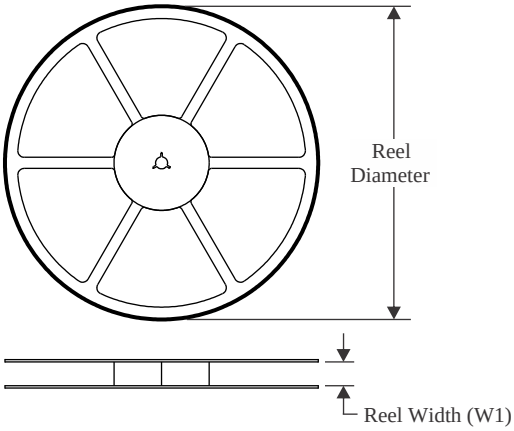
- Automotive : TPS732-Q1

NOTE: Qualified Version Definitions:

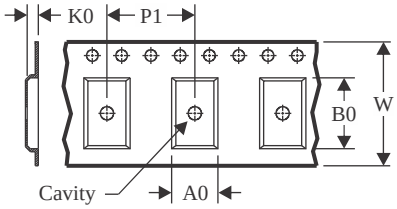
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

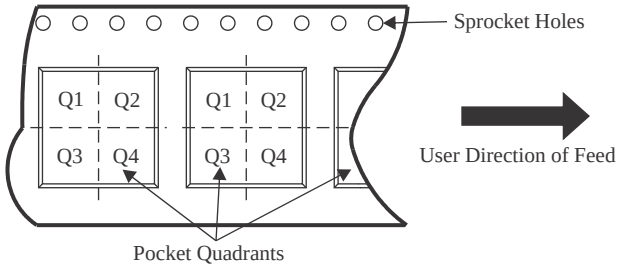


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

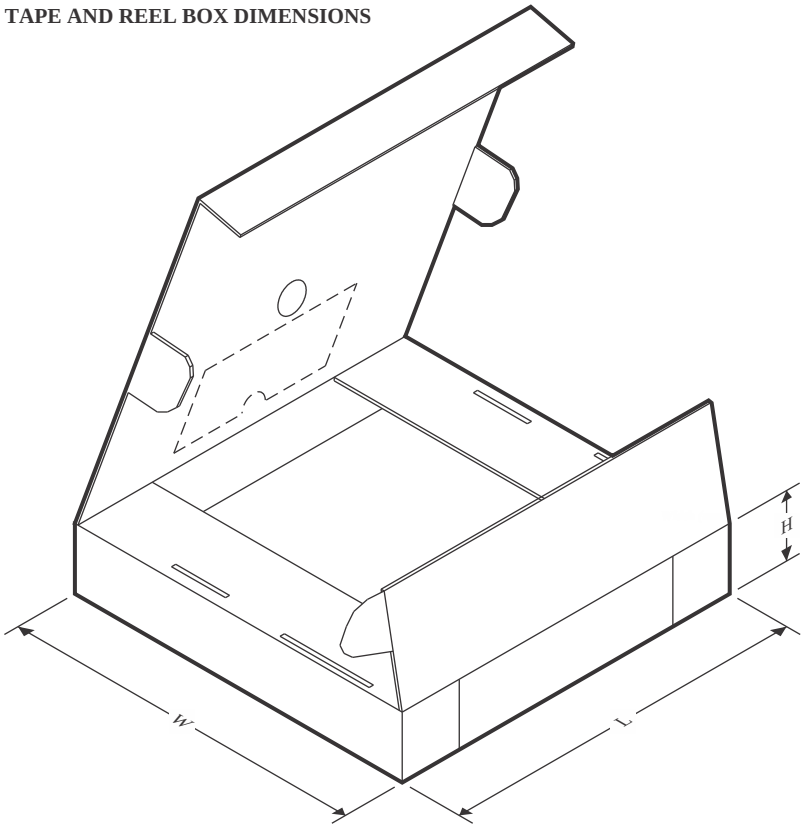


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73201DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73201DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS73201DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73201DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73201DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73201DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73201DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS73201DCQRM3	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS73201DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73201DRBRM3	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73213DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73215DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73215DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS73216DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73218DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73218DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73218DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73218DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS73219DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73219DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73225DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73225DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73225DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73225DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73225DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73230DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73230DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73230DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73233DBVR1G4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73233DBVR1G4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73233DBVRM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73233DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73233DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS73250DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73250DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73250DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73250DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73201DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73201DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73201DBVRG4	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73201DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73201DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS73201DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73201DCQR	SOT-223	DCQ	6	2500	366.0	364.0	50.0
TPS73201DCQRM3	SOT-223	DCQ	6	2500	366.0	364.0	50.0
TPS73201DRBR	SON	DRB	8	3000	360.0	360.0	36.0
TPS73201DRBRM3	SON	DRB	8	3000	367.0	367.0	35.0
TPS73213DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73215DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73215DCQR	SOT-223	DCQ	6	2500	366.0	364.0	50.0
TPS73216DBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
TPS73218DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73218DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73218DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73218DCQR	SOT-223	DCQ	6	2500	366.0	364.0	50.0

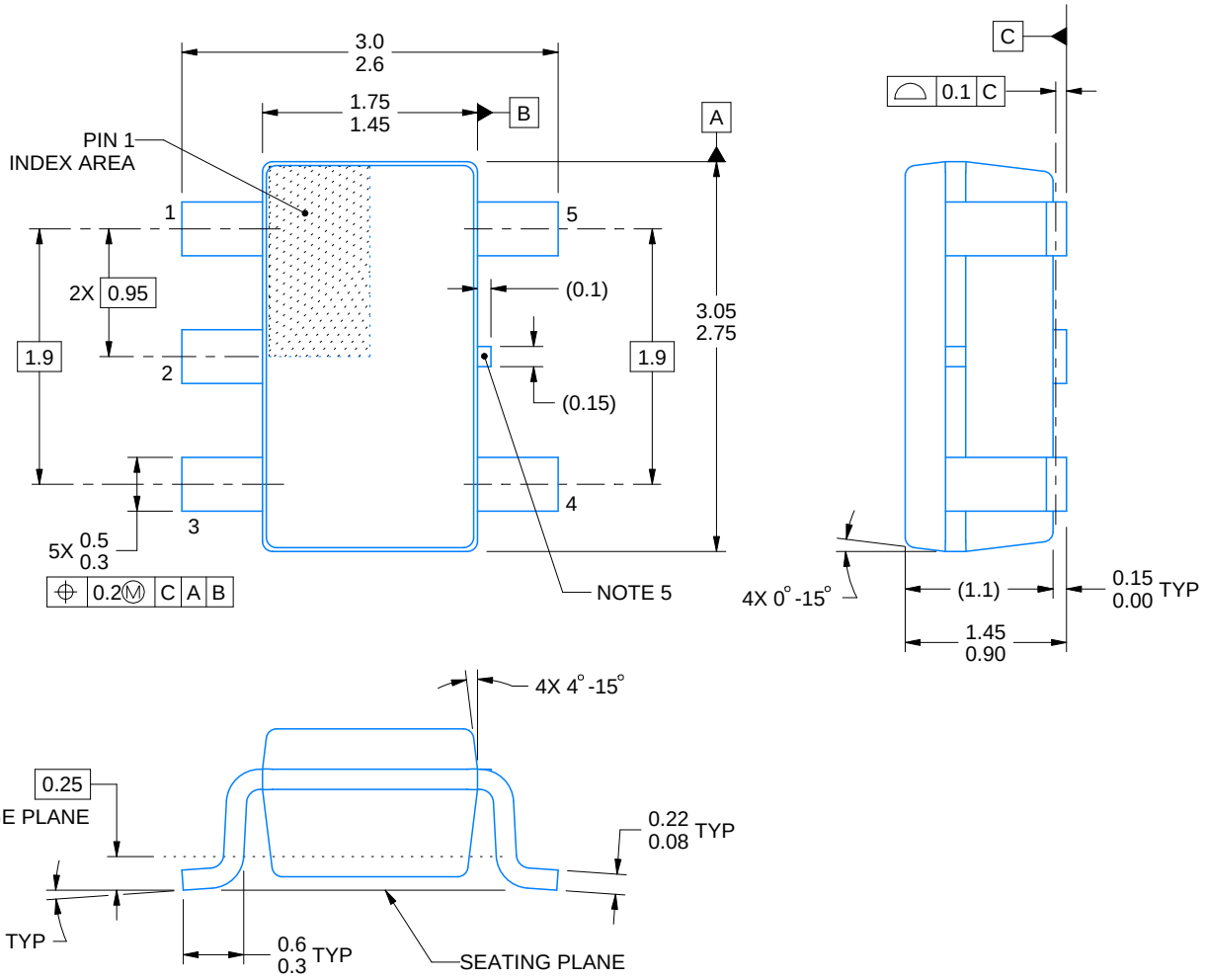
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73219DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73219DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73225DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73225DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73225DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS73225DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73225DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS73230DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73230DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73230DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS73233DBVR1G4	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73233DBVR1G4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73233DBVRM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73233DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS73233DCQR	SOT-223	DCQ	6	2500	366.0	364.0	50.0
TPS73250DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS73250DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73250DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS73250DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

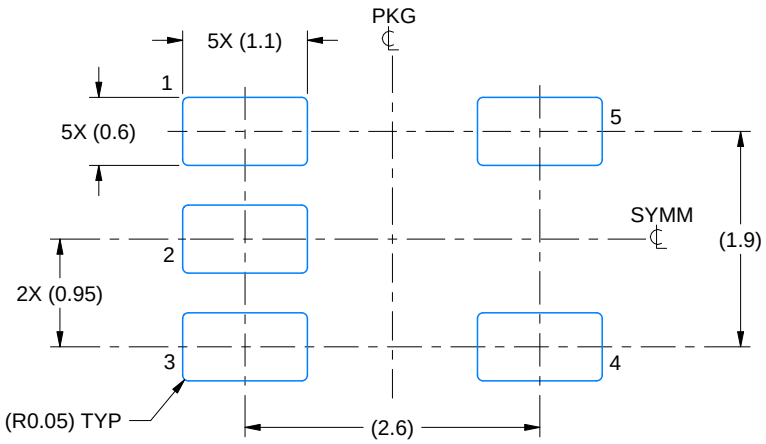
SMALL OUTLINE TRANSISTOR



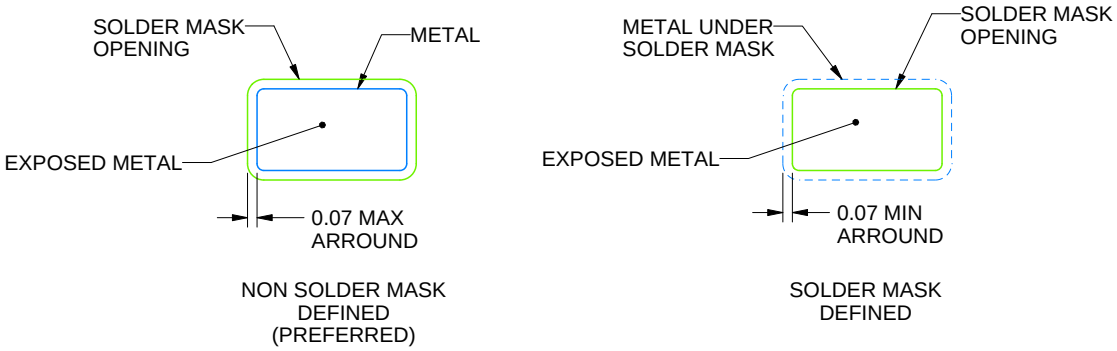
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

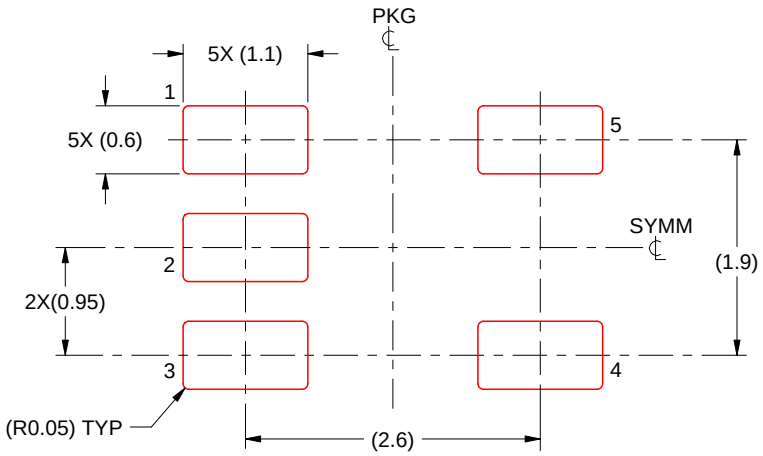


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

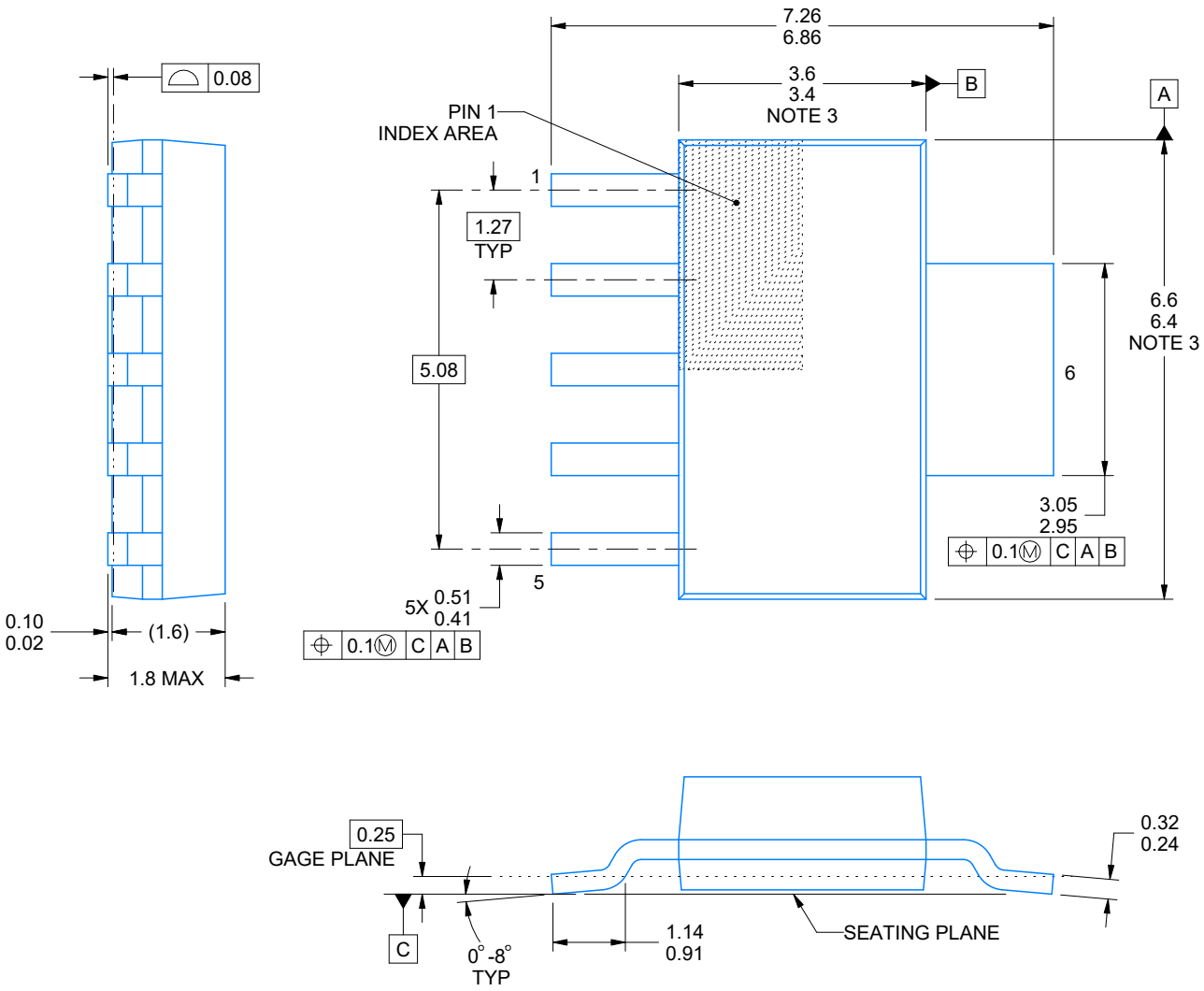
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

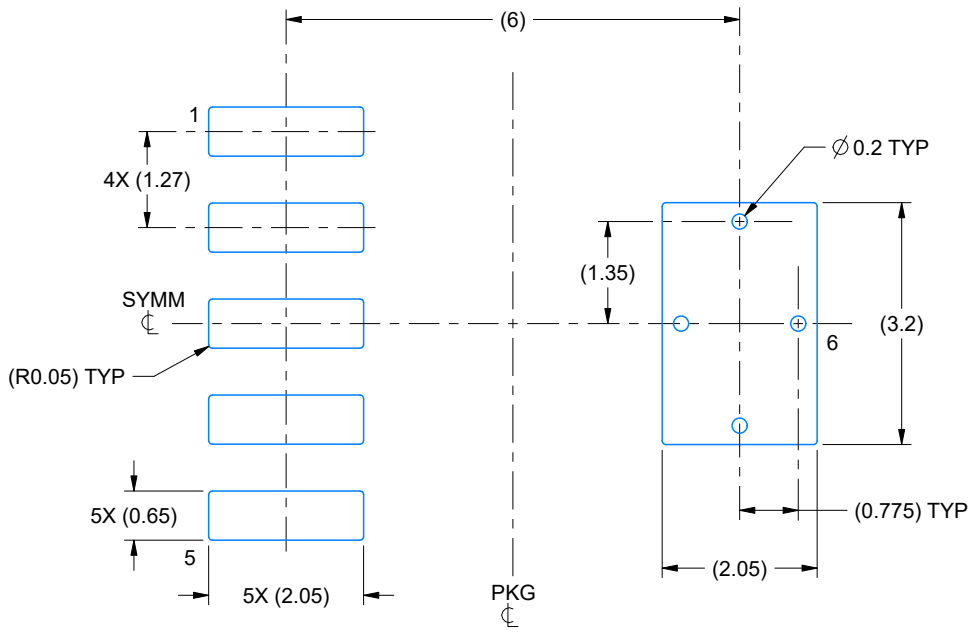
PLASTIC SMALL OUTLINE



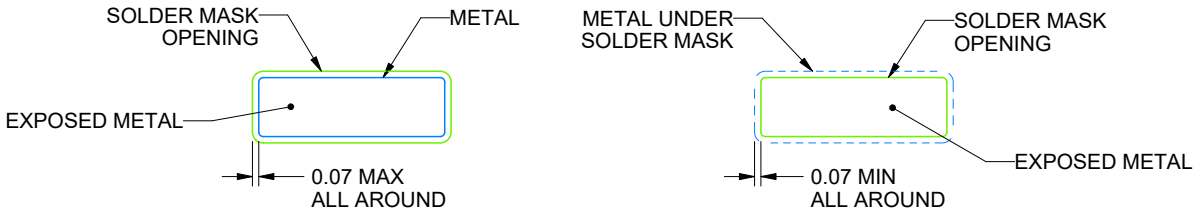
4214845/C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

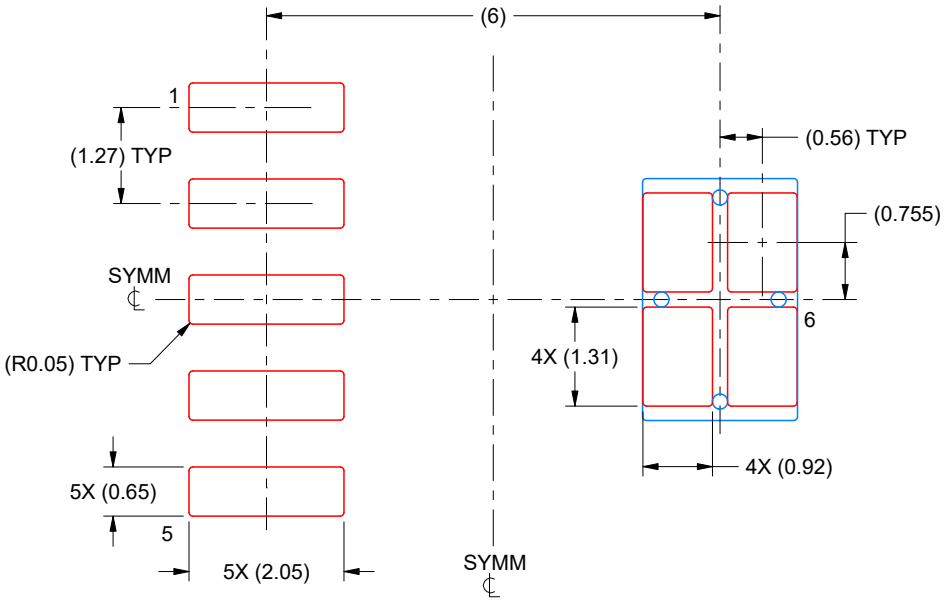


SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

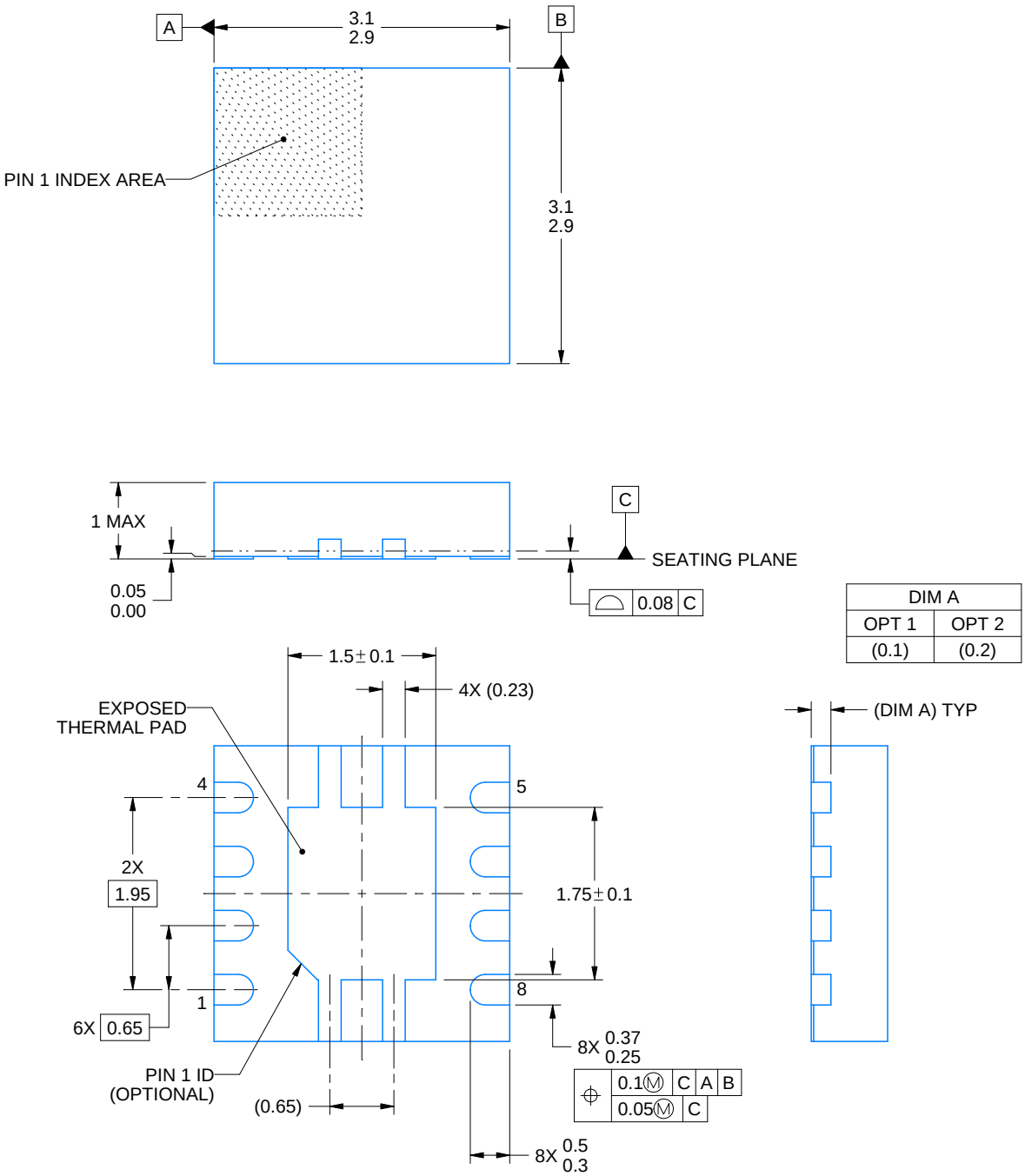
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

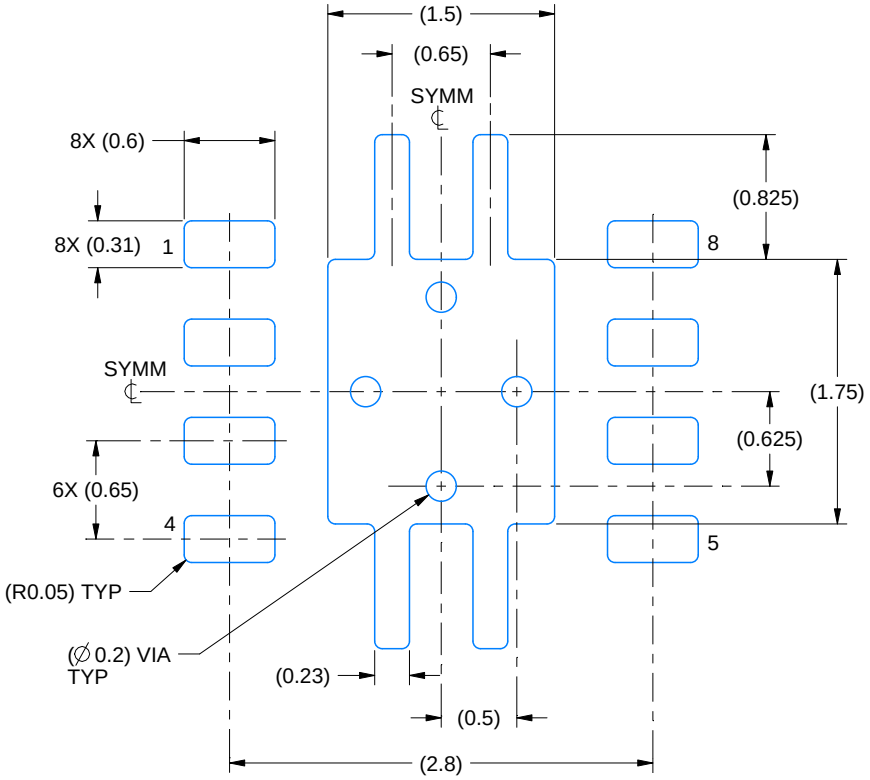
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

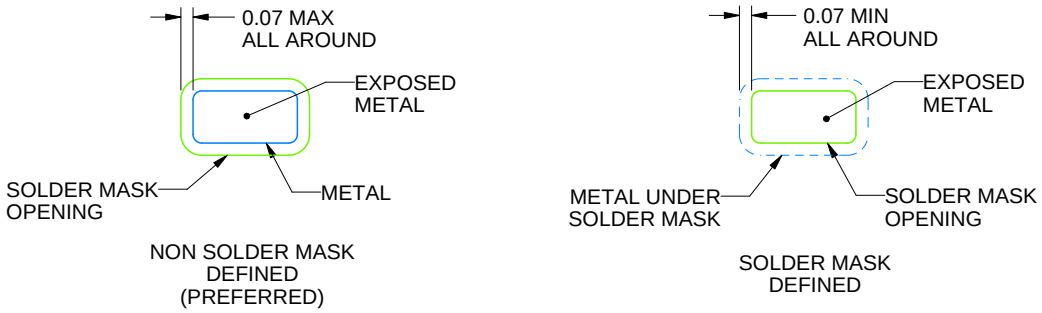
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

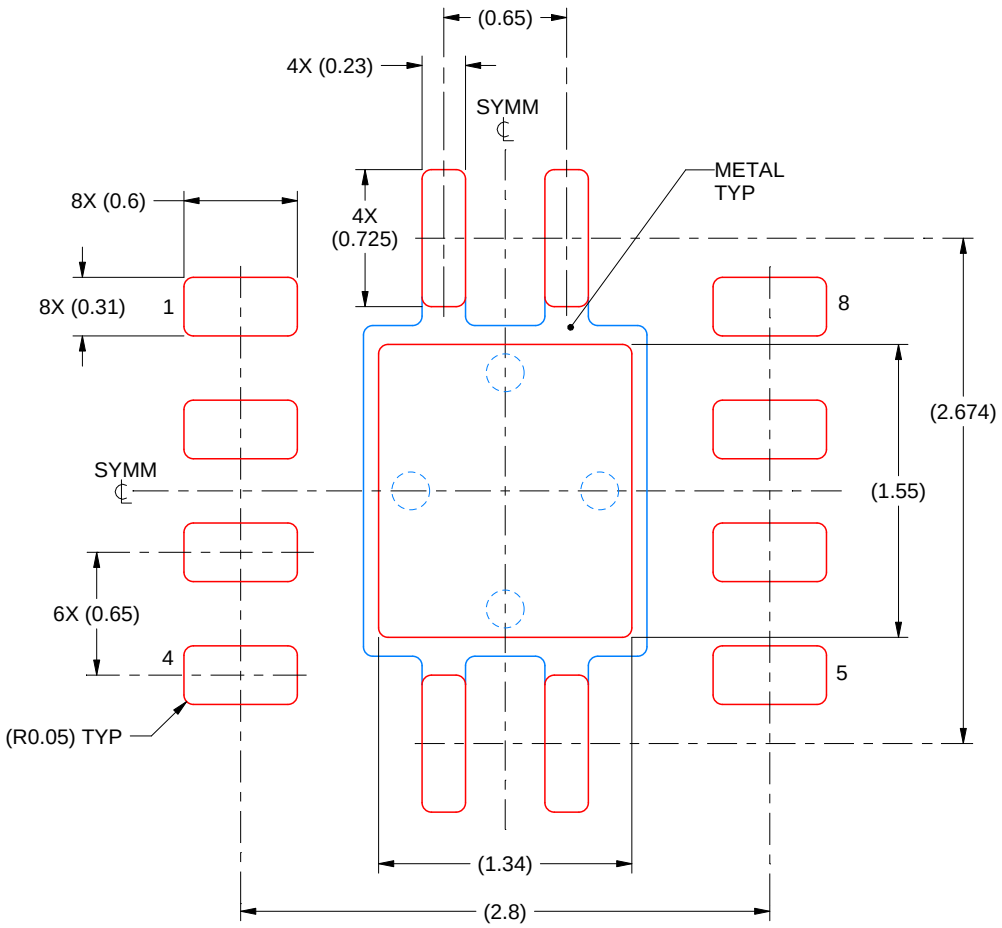


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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