TPS796-Q1 Automotive, Ultra-Low-Noise, High-PSRR, Fast, RF, 1A Low-Dropout Linear Regulator

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- 1A low-dropout regulator with enable
- High PSRR (53dB at 10kHz)
- Low-noise:
  - 54μV_{RMS} (legacy chip)
  - 78μV_{RMS} (new chip)
- Stable with a 1µF ceramic capacitor
- Excellent load, line transient response
- Very low dropout voltage:
  - 220mV (typ) TPS79633-Q1
- SOT-223-6 package

2 Applications

- Medium- and short-range radar
- Automotive head units
- Telematics control units
- Hybrid instrument clusters

3 Description

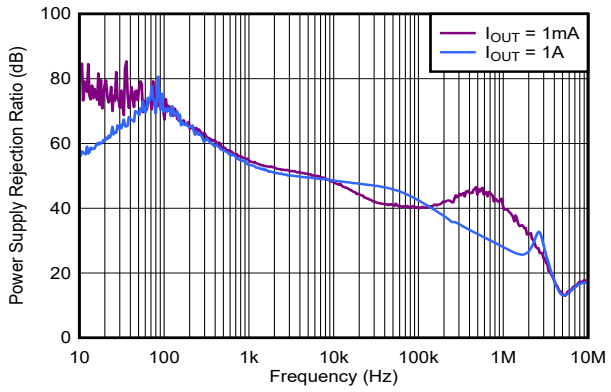
The TPS796-Q1 low-dropout (LDO), low-power, linear voltage regulator features high power-supply rejection ratio (PSRR), ultra-low-noise, fast start-up, and excellent line and load transient responses. This device is stable with a small 1µF ceramic capacitor on the output.

The low output noise and great PSRR performance make the device designed to power-sensitive analog loads. The TPS796-Q1 is a flexible device for post regulation because this device supports an input voltage range from 2.7V to 5.5V.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS796-Q1	DCQ (SOT-223, 6)	6.5mm × 7.06mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



PSRR vs Frequency

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4 Pin Configuration and Functions

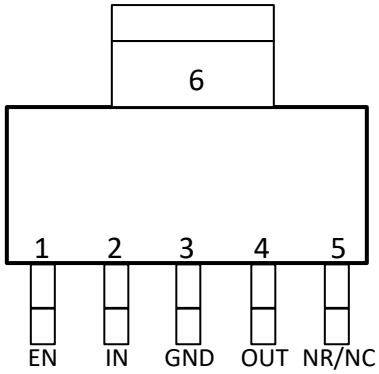


Figure 4-1. DCQ Package, 6-Pin SOT-223 (Top View)

Table 4-1. Pin Functions

PIN			DESCRIPTION
NAME	SOT223 (DCQ)	TYPE	
NR/NC	5	—	Noise-reduction pin (legacy chip). Connecting an external capacitor to this pin bypasses noise generated by the internal band gap, improves power-supply rejection and reduces output noise. No connect pin (new chip). This pin is not internally connected. Connect to GND or leave floating.
EN	1	Input	Enable pin. Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
GND	3, Tab	—	Device GND. Connect GND and TAB to the same ground on the board.
IN	2	Input	Input pin. For best performance, place the nominal recommended value or larger ceramic capacitor from IN to GND; see the *Recommended Operating Conditions* table. Place the input capacitor as close to the input of the device as possible.
OUT	4	Output	Regulated output. A 1µF or greater capacitor is required from OUT to ground for stability. Place the output capacitor as close to output of the device as possible; see the *Recommended Operating Conditions* table.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, V_{IN} (New chip)	–0.3	6.5	V
	Supply, V_{IN} (Legacy chip)	–0.3	6	
	Enable, V_{EN}	–0.3	V_{IN} + 0.3	
	Output, V_{OUT}	–0.3	6	
Current	Output, I_{OUT}	Internally limited		
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage (legacy chip)		2.7		5.5	V
	Input supply voltage (new chip)		2.7		6.0	
C_{IN}	Input capacitor		2.2			µF
C_{OUT}	Output capacitor		1[1]		200	
I_{OUT}	Output current		0		1	A
V_{EN}	Enable voltage (legacy chip)		0		5.5	V
	Enable voltage (new chip)		0		6.0	
F_{EN}	Enable toggle frequency (new chip)				10	kHz
Tj	Junction Temperature		–40		125	°C

(1) The minimum effective capacitance is 0.47 µF.

5.4 Thermal Information

THERMAL METRIC[1]		TPS796-Q1		UNIT
		DCQ (SOT223-6)		
		6 PINS [2]	6 PINS [3]	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.4	71.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70	41.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	8.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	3.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.1	8.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.3	6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Packae Thermal Metrics* application report.
(2) Legacy chip.
(3) New chip.

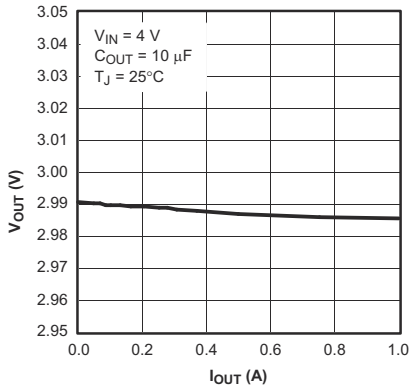
5.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to +125°C), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V (1), I_{OUT} = 1 mA, and C_{OUT} = 10µF and C_{NR} = 0.01µF(Legacy Chip only), unless otherwise noted. All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage	Legacy chip		2.7		5.5	V
		New chip		2.7		6.0	
I_{OUT}	Continuous output current			0		1	A
V_{OUT}	Output accuracy	Fixed V_{OUT} < 5V	0 µA ≤ I_{OUT} ≤ 1 A, $V_{OUT(nom)}$ + 1 V ≤ V_{IN} ≤ 5.5 V (1)	-2.0		2.0	%
$\Delta V_{OUT}/\Delta VIN$	Line regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V			0.05	0.12	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0 µA ≤ I_{OUT} ≤ 1 A			5		mV
V_{DO}	Dropout voltage	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 1A			220	325	mV
I_{CL}	Output current limit	V_{OUT} = 0 (legacy chip)		2.4		4.2	A
I_{CL}	Output current limit	$V_{IN} = V_{OUT(nom)}$ + 1.25 V or 2.0 V (whichever is greater), V_{OUT} = 0.9 x $V_{OUT(nom)}$ (new chip only)		1.04		1.65	A
I_{SC}	Short-circuit current limit	V_{OUT} = 0 (new chip only)			550		mA
I_{GND}	Ground current	0µA ≤ I_{OUT} ≤ 1A (legacy chip)			265	385	µA
I_{GND}	Ground current	0µA ≤ I_{OUT} ≤ 1A (new chip)			700	1100	µA
I_{SHDN}	Shutdown current	V_{EN} = 0 V, 2.7 V ≤ V_{IN} ≤ 5.5 V			0.07	1	µA
PSRR	Power-supply rejection ratio	f = 100 Hz, I_{OUT} = 10mA (legacy chip)			59		dB
		f = 100 Hz, I_{OUT} = 10mA (new chip)			64		
		f = 100 Hz, I_{OUT} = 1A (legacy chip)			54		
		f = 100 Hz, I_{OUT} = 1A (new chip)			74		
		f = 10 kHz, I_{OUT} = 1A (legacy chip)			53		
		f = 10 kHz, I_{OUT} = 1A (new chip)			49		
		f = 100 kHz, I_{OUT} = 1A (legacy chip)			42		
		f = 100 kHz, I_{OUT} = 1A (new chip)			42		
V_n	Output noise voltage	BW = 100Hz to 100kHz, I_{OUT} = 1A	C_{NR} = 0.001 µF		54		μV_{RMS}
			C_{NR} = 0.0047 µF		46		
			C_{NR} = 0.01 µF		41		
			C_{NR} = 0.1 µF		40		
		BW = 10Hz to 100kHz, I_{OUT} = 1A	new chip (10		78		μV_{RMS}
t_{str}	Time, start-up	R_L = 3Ω, C_{OUT} = 1 µF	C_{NR} = 0.001 µF		50		µs
		R_L = 3Ω, C_{OUT} = 1 µF	C_{NR} = 0.0047 µF		75		
		R_L = 3Ω, C_{OUT} = 1 µF	C_{NR} = 0.01 µF		110		
t_{str}	Time, start-up	R_L = 3Ω, C_{OUT} = 1 µF	new chip		550		µs
I_{EN}	Enable pin current	V_{EN} = 0 V		-1		1	µA
$R_{PULLDOWN}$	Pulldown resistance	V_{IN} = 3.3V (new chip only)			100		Ω
V_{UVLO}	UVLO threshold	V_{IN} rising (legacy chip)		2.25		2.65	V
		V_{IN} rising (new chip)		1.28		1.62	
$V_{UVLO(HYST)}$	UVLO hysteresis	V_{IN} hysteresis (legacy chip)			100		mV
		V_{IN} hysteresis (new Chip)			130		
$V_{EN(HI)}$	High-level enable input voltage	2.7V(1) ≤ V_{IN} ≤ 5.5V (legacy chip)		1.7		V_{IN}	V
		2.7V(1) ≤ V_{IN} ≤ 5.5V (new chip)		0.85		V_{IN}	
$V_{EN(LOW)}$	Low-level enable input voltage	2.7V(1) ≤ V_{IN} ≤ 5.5V (legacy chip)				0.7	
		2.7V(1) ≤ V_{IN} ≤ 5.5V (new chip)				0.425	

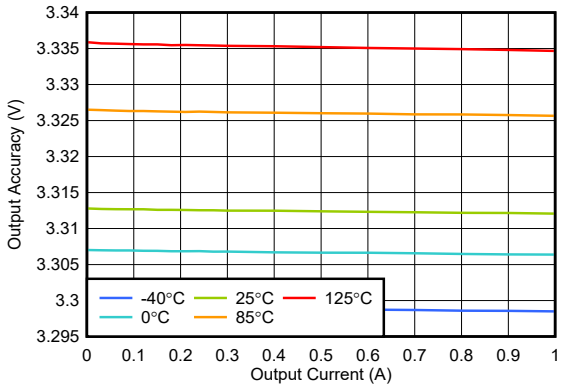
(1) Minimum V_{IN} = V_{OUT} +1V or 2.7V, whichever is greater.

5.6 Typical Characteristics



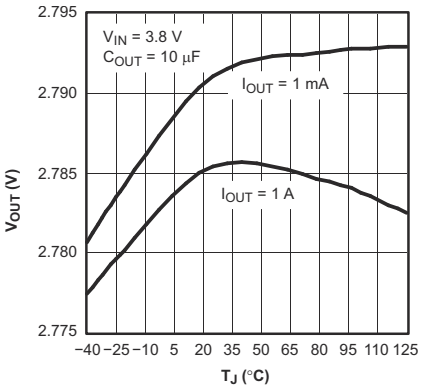
Legacy chip

Figure 5-1. TPS79630-Q1 Output Voltage vs Output Current



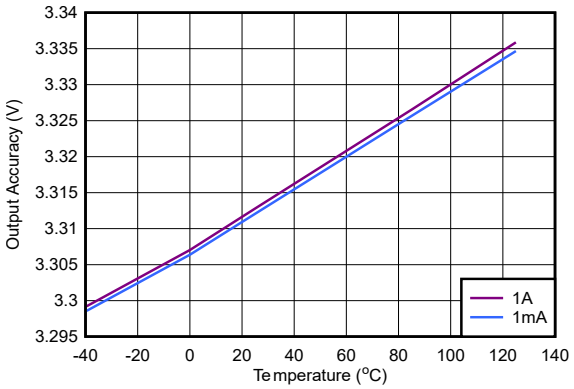
New chip

Figure 5-2. TPS79633-Q1 Output Voltage vs Output Current



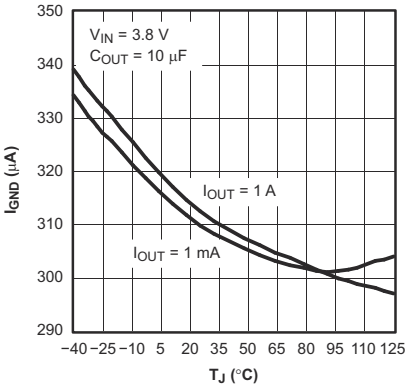
Legacy chip

Figure 5-3. TPS79628-Q1 Output Voltage vs Junction Temperature



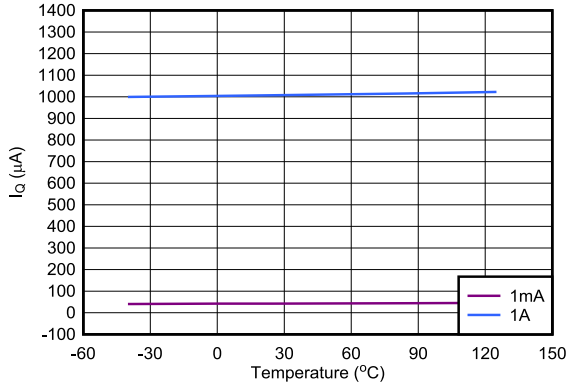
New chip

Figure 5-4. TPS79633-Q1 Output Voltage vs Junction Temperature



Legacy chip

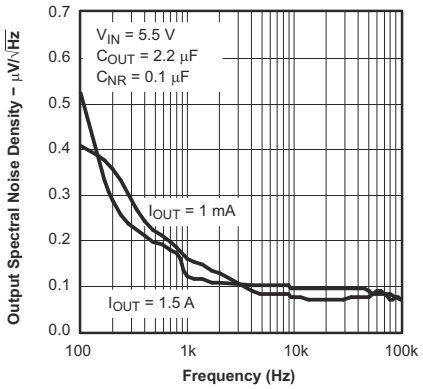
Figure 5-5. TPS79628-Q1 Ground Current vs Junction Temperature



New chip

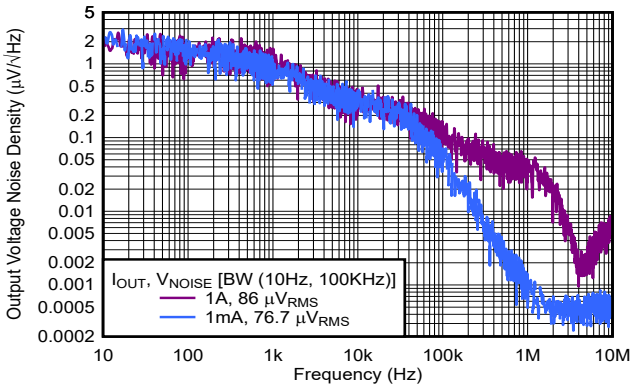
Figure 5-6. TPS79633-Q1 Ground Current vs Junction Temperature

5.6 Typical Characteristics (continued)



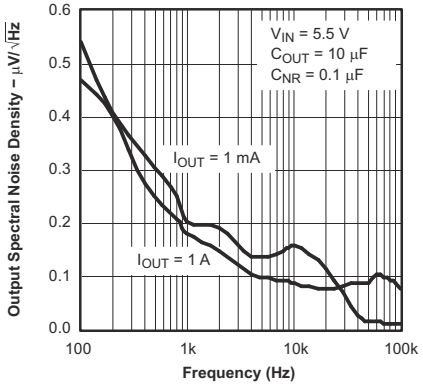
Legacy chip

Figure 5-7. TPS79630-Q1 Output Spectral Noise Density vs Frequency



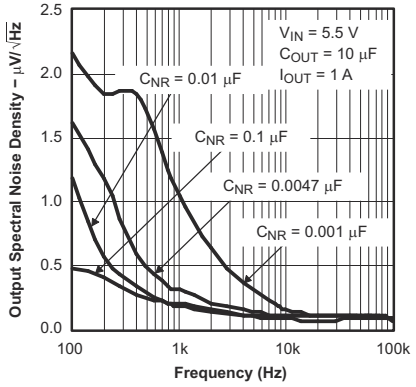
New chip

Figure 5-8. TPS79633-Q1 Output Spectral Noise Density vs Frequency



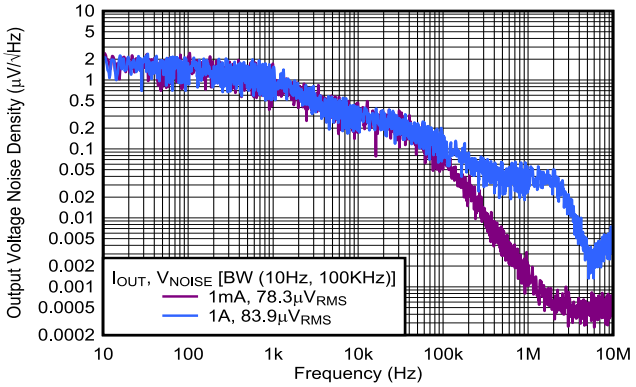
Legacy chip

Figure 5-9. TPS79630-Q1 Output Spectral Noise Density vs Frequency



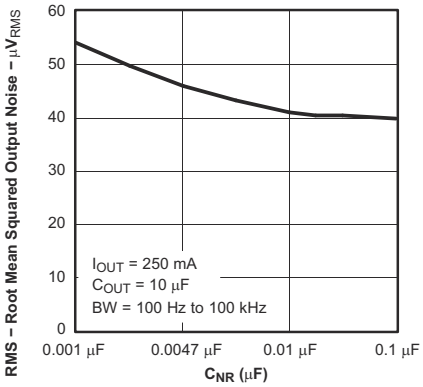
Legacy chip

Figure 5-10. TPS79630-Q1 Output Spectral Noise Density vs Frequency



New chip, C_{OUT} = 10uF

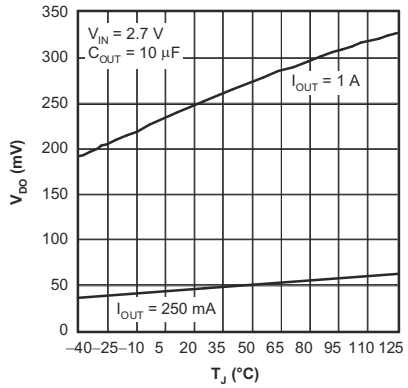
Figure 5-11. TPS79633-Q1 Output Spectral Noise Density vs Frequency



Legacy chip

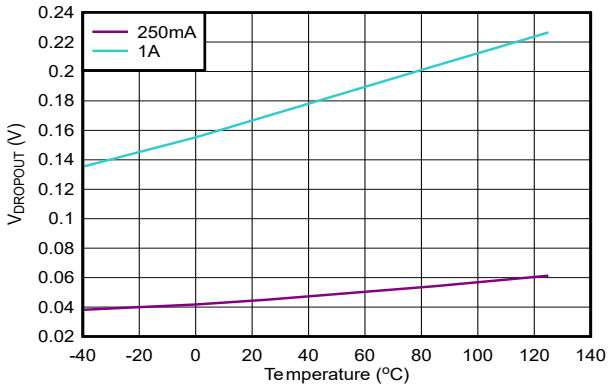
Figure 5-12. TPS79630-Q1 Root Mean Squared Output Noise vs Bypass Capacitance

5.6 Typical Characteristics (continued)



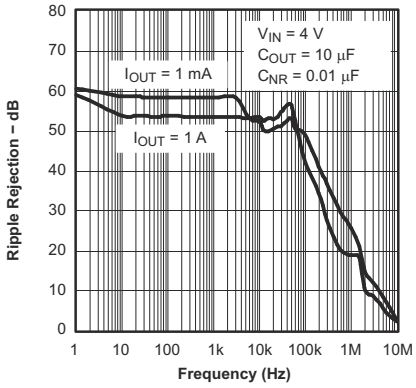
Legacy chip

Figure 5-13. TPS79628-Q1 Dropout Voltage vs Junction Temperature



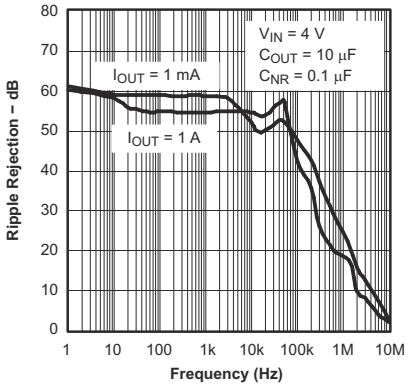
New chip

Figure 5-14. TPS79633-Q1 Dropout Voltage vs Junction Temperature



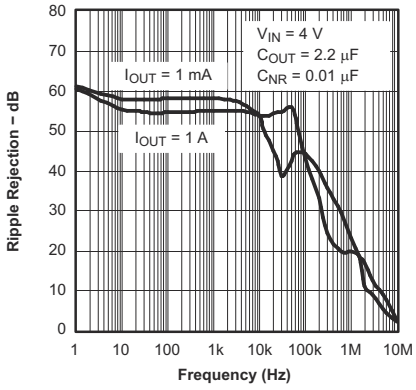
Legacy chip

Figure 5-15. TPS79630-Q1 Ripple Rejection vs Frequency



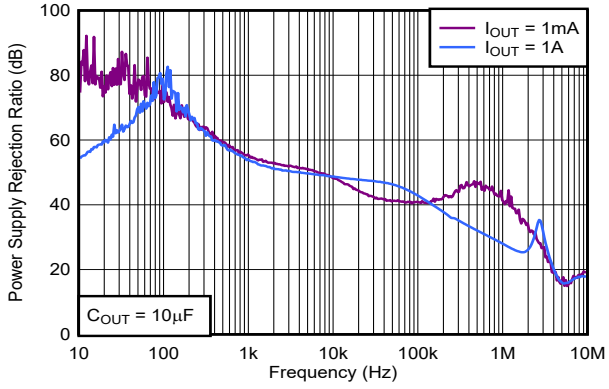
Legacy chip

Figure 5-16. TPS79630-Q1 Ripple Rejection vs Frequency



Legacy chip

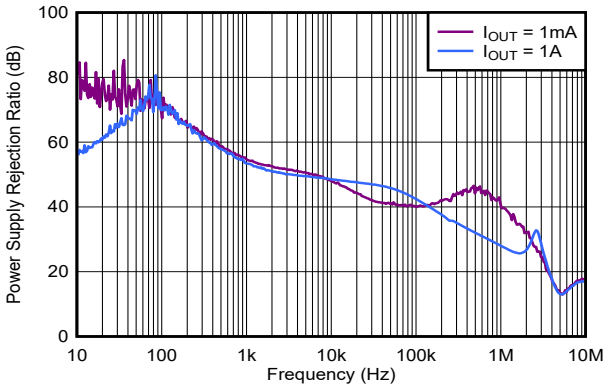
Figure 5-17. TPS79630-Q1 Ripple Rejection vs Frequency



New chip

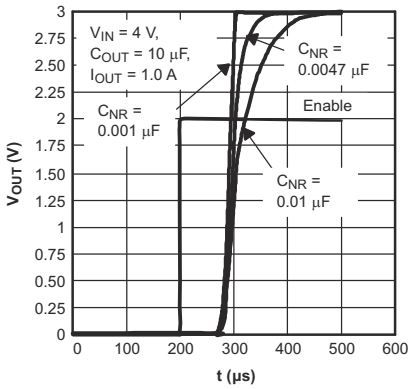
Figure 5-18. TPS79633-Q1 Ripple Rejection vs Frequency

5.6 Typical Characteristics (continued)



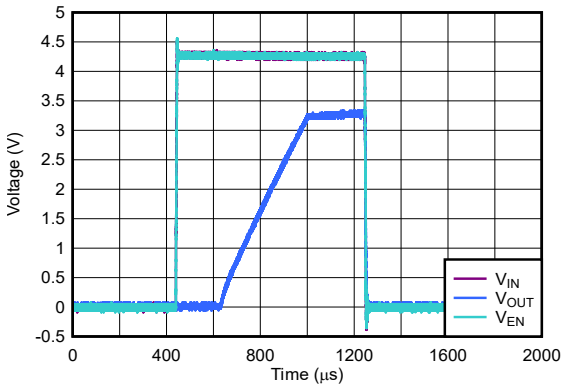
New chip, C_{OUT} = 1uF

Figure 5-19. TPS79633-Q1 Ripple Rejection vs Frequency



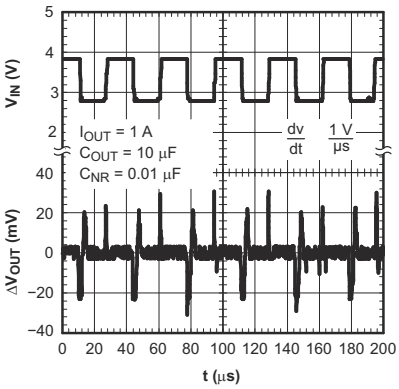
Legacy chip

Figure 5-20. Start-Up Time



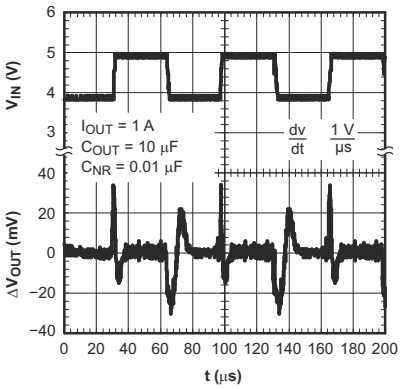
New chip

Figure 5-21. Start-Up Time



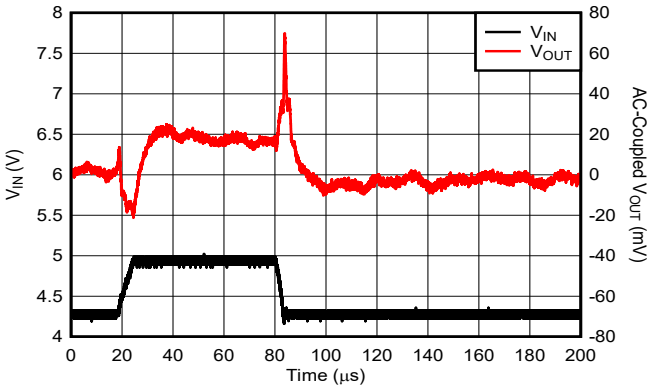
Legacy chip

Figure 5-22. TPS79618-Q1 Line Transient Response



Legacy chip

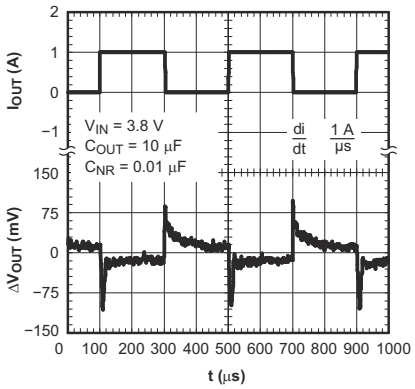
Figure 5-23. TPS79630-Q1 Line Transient Response



New chip

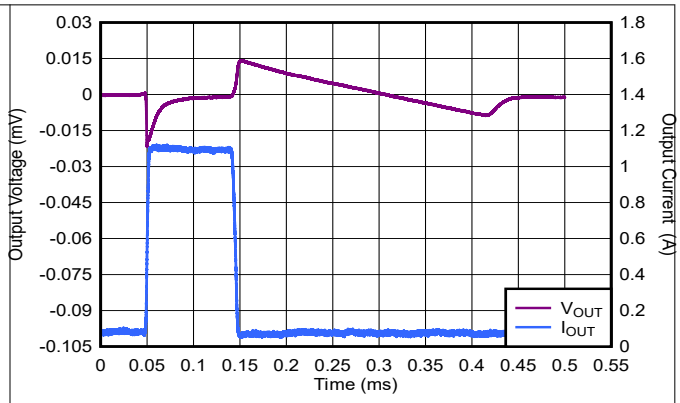
Figure 5-24. TPS79633-Q1 Line Transient Response

5.6 Typical Characteristics (continued)



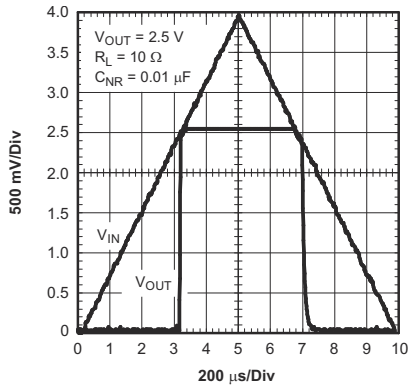
Legacy chip

Figure 5-25. TPS79628-Q1 Load Transient Response



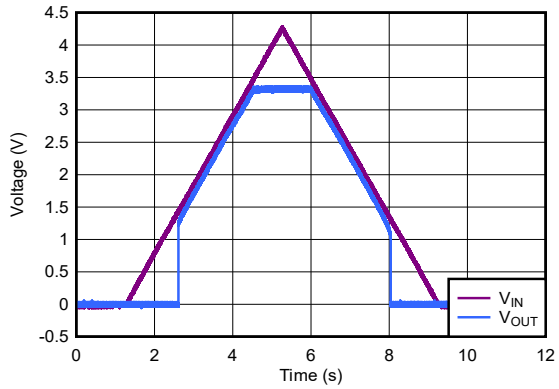
New chip

Figure 5-26. TPS79633-Q1 Load Transient Response



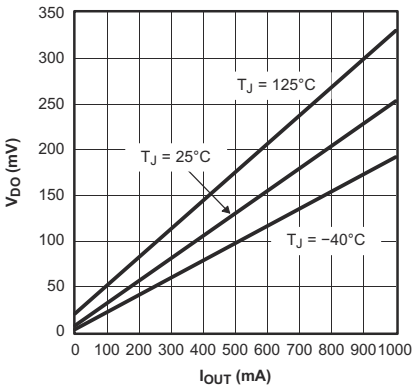
Legacy chip

Figure 5-27. TPS79625-Q1 Power-Up, Power-Down



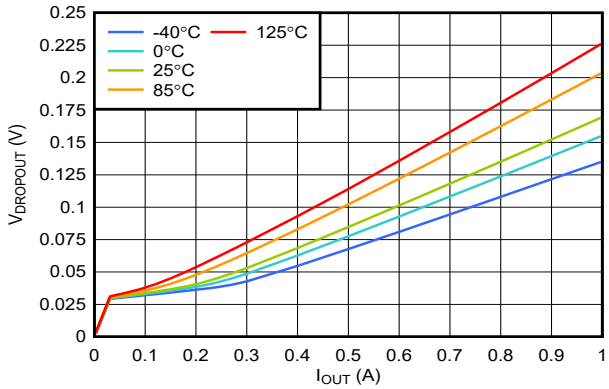
New chip

Figure 5-28. TPS79633-Q1 Power-Up, Power-Down



Legacy chip

Figure 5-29. TPS79630-Q1 Dropout Voltage vs Output Current



New chip

Figure 5-30. TPS79633-Q1 Dropout Voltage vs Output Current

5.6 Typical Characteristics (continued)

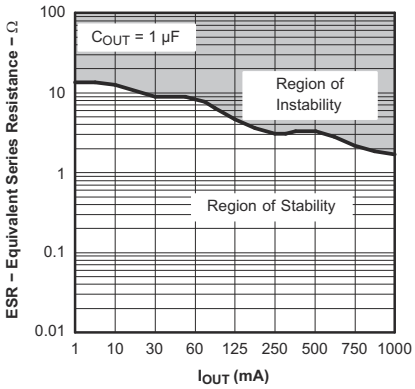


Figure 5-31. TPS79630-Q1 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

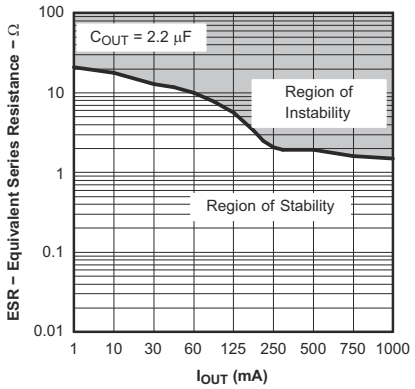


Figure 5-32. TPS79630-Q1 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

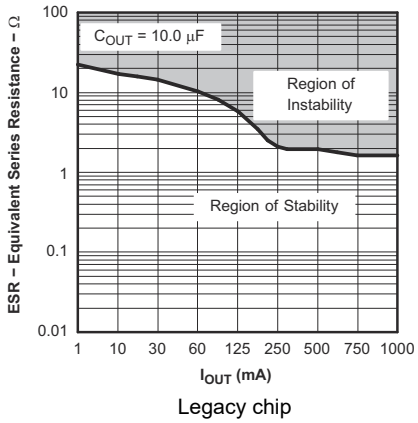


Figure 5-33. TPS79630-Q1 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

6 Detailed Description

6.1 Overview

The TPS796-Q1 is an ultra low-dropout, high PSRR, high-accuracy linear voltage regulator that is optimized for excellent transient performance. These characteristics make the device designed for most automotive applications. This regulator offers foldback current limit, output enable, active discharge, undervoltage lockout (UVLO), and thermal protection.

6.2 Functional Block Diagrams

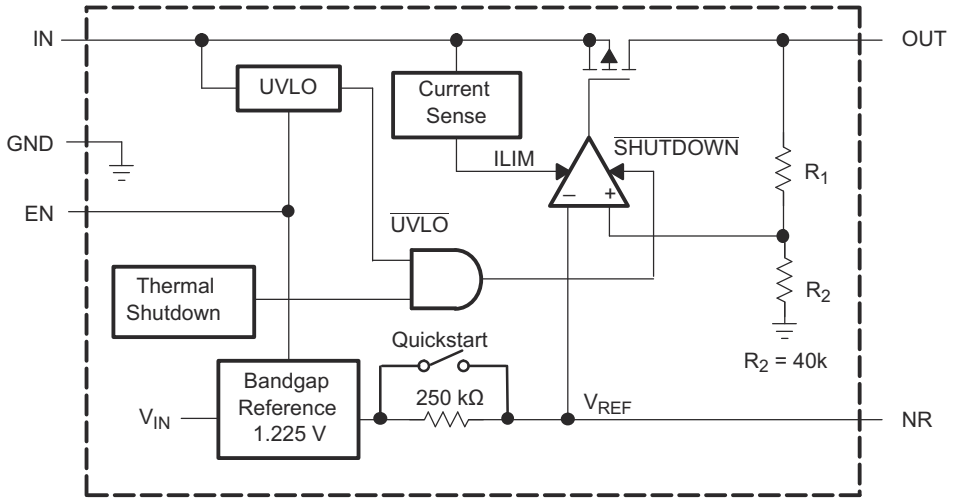


Figure 6-1. Functional Block Diagram (Legacy Chip)

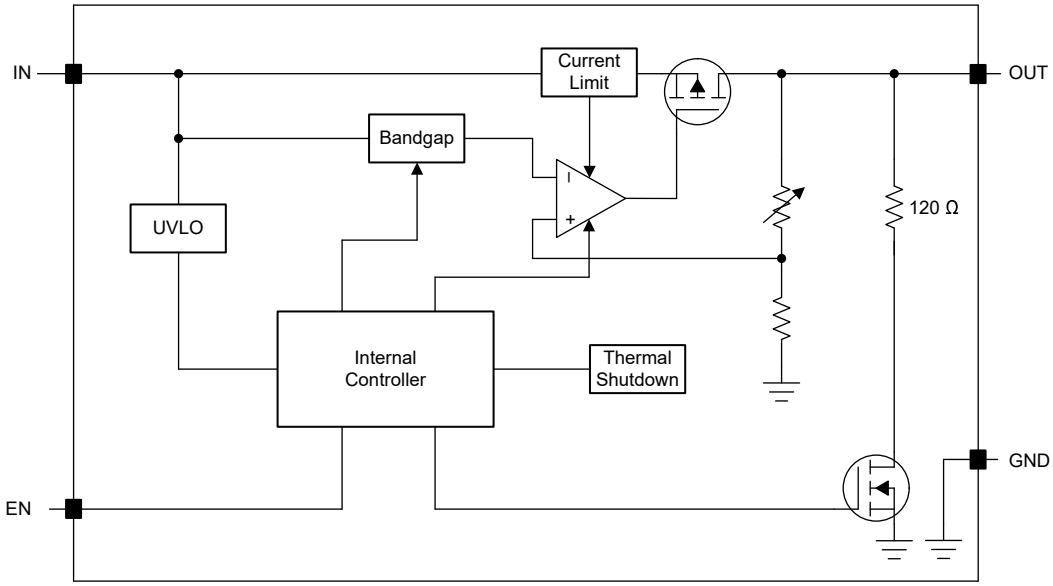


Figure 6-2. Functional Block Diagram (New Chip)

6.3 Feature Description

6.3.1 Undervoltage Lockout (UVLO)

The TPS796-Q1 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage. This circuit verifies that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$.

6.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$. Turn off the device by forcing the EN pin to drop below the maximum EN pin low-level input voltage (see *Electrical Characteristics* table). If shutdown capability is not required, connect EN to IN.

6.3.3 Active Discharge (New Chip)

The device has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin.

Do not rely on the active discharge circuit to discharge the output voltage after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device especially when a large output capacitor is used. Limit reverse current to no more than 5% of the device rated current for a short period of time.

6.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TPS793 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS793 into thermal shutdown degrades device reliability.

6.3.5 Regulator Protection

The TPS796-Q1 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, use external limiting as appropriate.

The legacy chip features internal current limiting and thermal protection. During normal operation, the TPS796-Q1 limits output current to approximately 2.8A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Although current limiting is designed to prevent gross device failure, care must be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately +165°C, thermal-protection circuitry shuts the device down. When the device has cooled down to below approximately +140°C, regulator operation resumes.

The new chip features an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.4 \times VOUT(_{NOM})$.

Figure 6-3 shows a diagram of the foldback current limit.

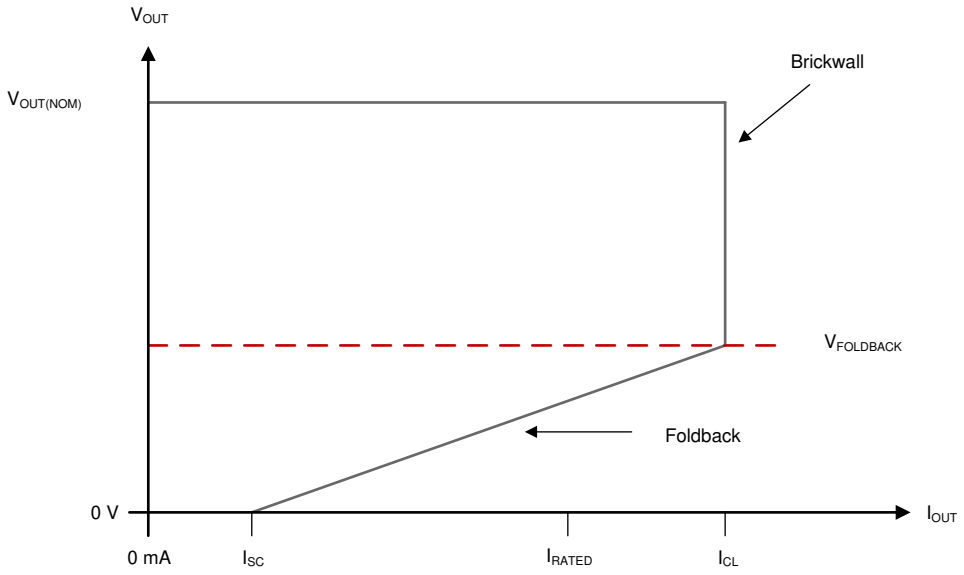


Figure 6-3. Foldback Current Limit

6.4 Device Functional Modes

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage is greater than $V_{EN(min)}$.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass transistor is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

6.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.
- The input voltage is less than $UVLO_{falling}$.

Table 6-1 shows the conditions that lead to the different modes of operation.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{falling}$	$V_{EN} < V_{EN(low)}$	—	$T_J > 165°C$(1)

(1) Approximate value for thermal shutdown.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS796-Q1 low-dropout (LDO) regulator is optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, low output noise, low quiescent current and enable input to reduce supply currents when the regulator is turned off.

A typical application circuit is shown in Figure 7-1 and Figure 7-2.

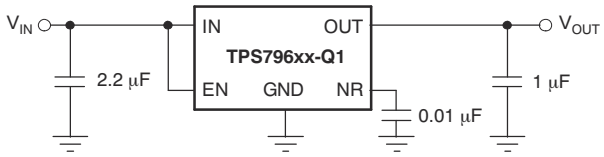


Figure 7-1. Typical Application Circuit (Legacy Chip)

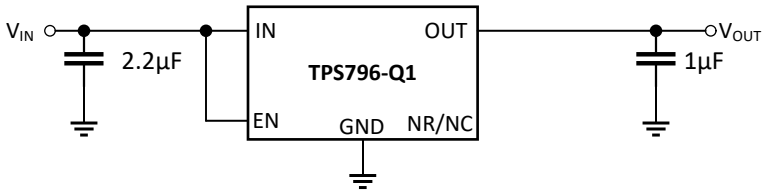


Figure 7-2. Typical Application (New Chip)

7.1.1 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output can overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in Figure 7-3, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

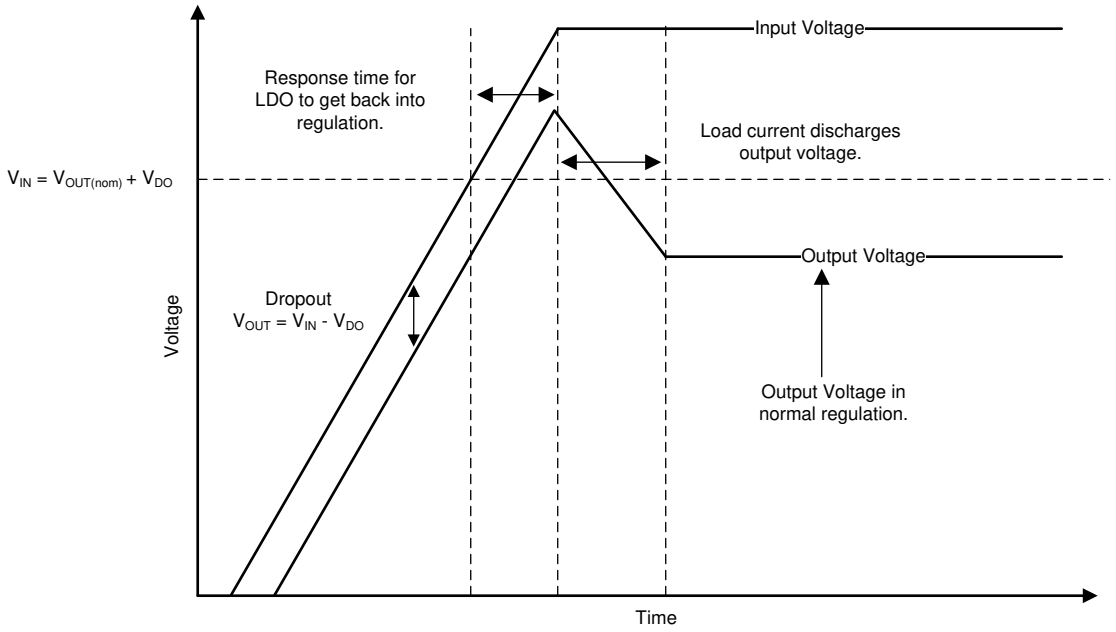


Figure 7-3. Start-Up Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass transistor and bring the gate back to the correct voltage for proper regulation. Figure 7-4 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (V_{GS}) is pulled all the way down to ground to give the pass transistor the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

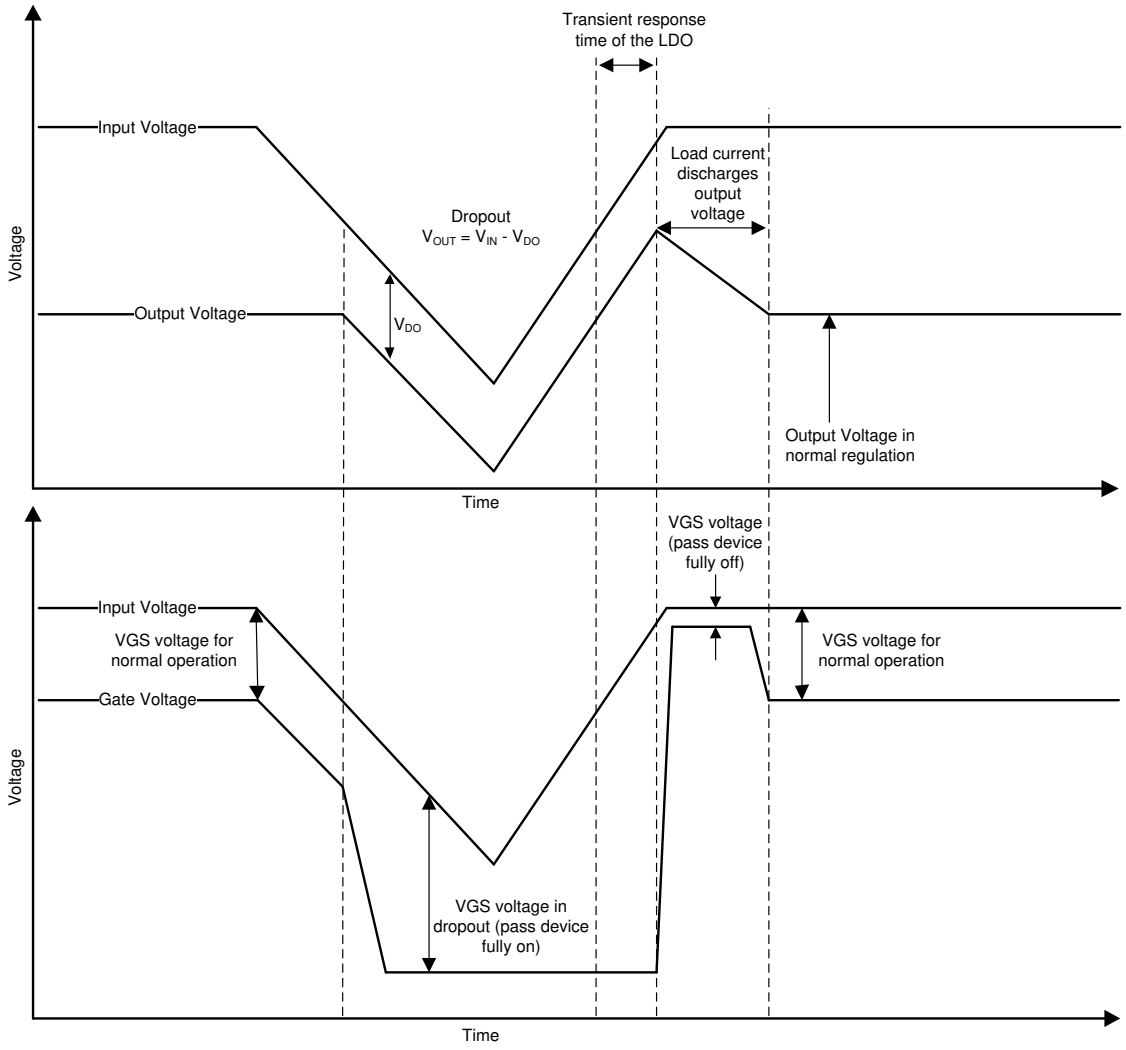


Figure 7-4. Line Transients From Dropout

7.1.2 External Capacitor Requirements

An input capacitor of 1.0µF (new chip) or 2.2µF (legacy chip) or larger ceramic input capacitor, connected between IN and GND, close to the TPS796-Q1, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor can be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

As with most LDO regulators, the TPS796-Q1 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is 1µF. Any 1µF or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS796-Q1 (legacy chip) has an NR pin that is connected to the voltage reference through a 250kΩ internal resistor. The 250kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. For the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor must be no more than 0.1µF to verify that the capacitor is fully charged during the quick-start time provided by the internal switch shown in the *Functional Block Diagrams*.

For example, the TPS796-Q1 exhibits 40μV_{RMS} of output voltage noise using a 0.1μF ceramic bypass capacitor and a 10μF ceramic output capacitor. The output starts up slower as the bypass capacitance increases because of the RC time constant at the bypass pin that is created by the internal 250kΩ resistor and external capacitor.

7.1.3 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements such as PSRR, output noise, and transient response, design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the ground pin of the device.

7.1.4 Regulator Mounting

The tab of the SOT-223-6 package is electrically connected to ground. For best thermal performance, solder the tab of the surface-mount version directly to the printed circuit board (PCB) copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in the *Solder Pad Recommendations for Surface-Mount Devices* application note, available for download from the TI web site (www.ti.com).

7.1.5 Thermal Information

7.1.5.1 Power Dissipation

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 1 calculates P_D:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

Note

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The primary heat conduction path for the package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The power dissipation through the device determines the junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 2. The equation is rearranged for output current in Equation 3.

$$T_J = T_A = (R_{\theta JA} \times P_D) \quad (2)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (3)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the RTE package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

7.1.5.2 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 4 and are given in the *Electrical Characteristics* table.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \quad (4)$$

where:

- P_D is the power dissipated as explained in the *Power Dissipation* section
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

7.2 Typical Application

A typical application circuit is shown in Figure 7-5.

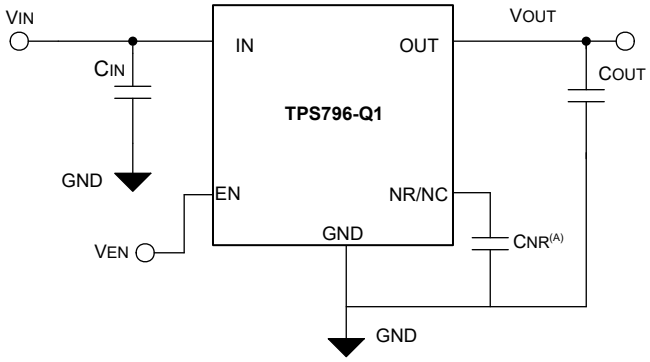


Figure 7-5. Typical Application Circuit

Note

C_{NR} is not required. The TPS796-Q1 (new chip) has an NC (no connect) pin instead; keeping a C_{NR} does not impact device performance.

7.2.1 Design Requirements

Table 7-1 summarizes the design requirement for this application.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input voltage	4.05V
Output voltage	3.3V, ± 2%
Output load	600mA
Maximum ambient temperature	85°C

7.2.2 Detailed Design Procedure

For this design example, the 3.3-V, fixed-version device is selected. The device is powered of a DC/DC converter connected to a battery. A 750-mV headroom between V_{IN} and V_{OUT} is used to keep the device within the dropout voltage specification and to make sure the device stays in regulation under all load and temperature conditions for this design.

7.2.3 Application Curves

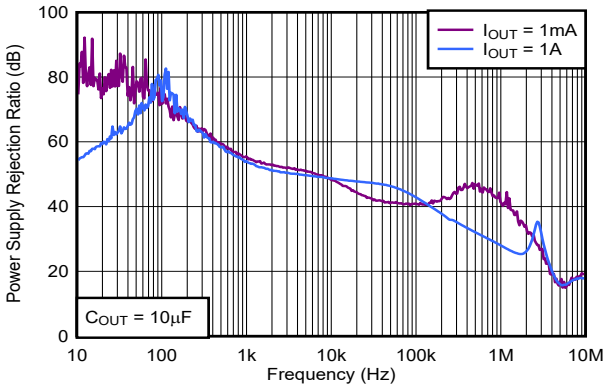


Figure 7-6. PSRR vs Frequency

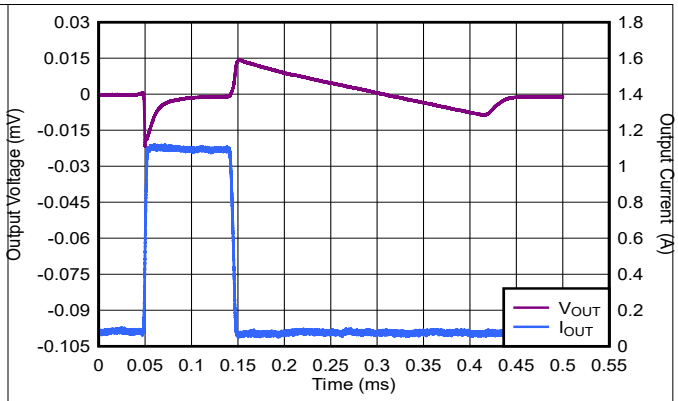


Figure 7-7. Load Transient

7.3 Power Supply Recommendations

The TPS796-Q1 is designed to operate from an input voltage supply range between 2.7 V and 5.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. To avoid negative system performance, do not use vias and long traces to the input and output capacitors.

A low ESL capacitor combined with low trace inductance limits the total inductance present on the output and optimizes the high-frequency PSRR. To improve performance, use a ground reference plane, either embedded in the PCB or placed on the bottom side of the PCB opposite the components. This reference plane serves to verify accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the GND tab. In most applications, this ground plane is necessary to meet thermal requirements.

7.4.2 Layout Examples

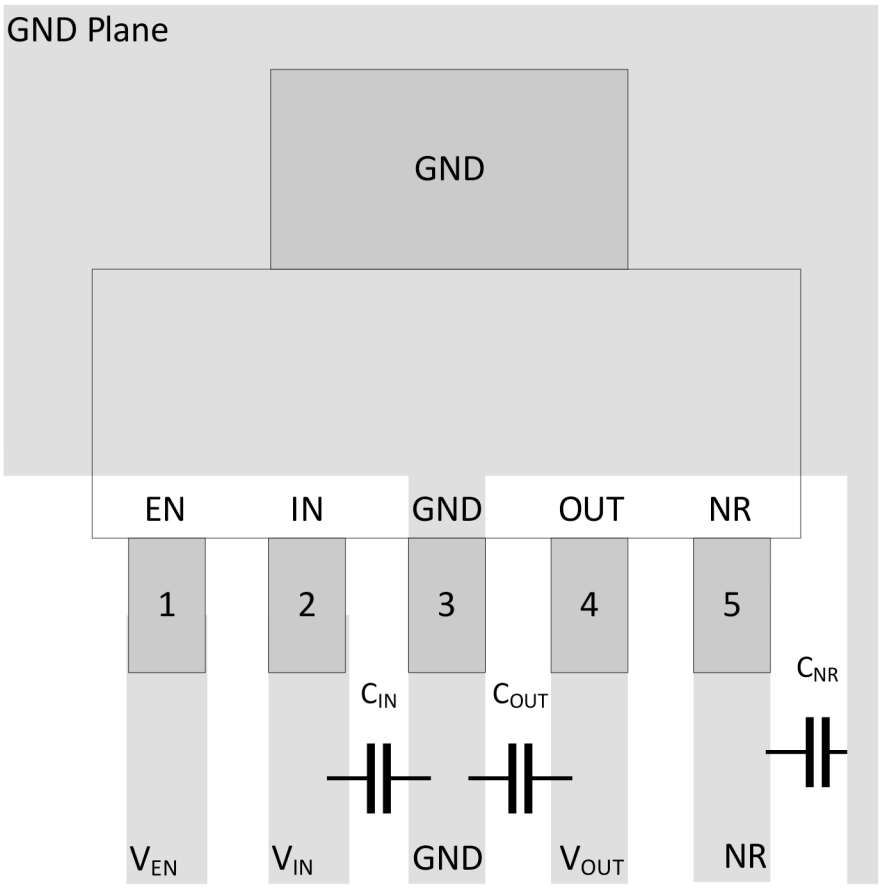


Figure 7-8. TPS796-Q1 Layout Example (Legacy Chip)

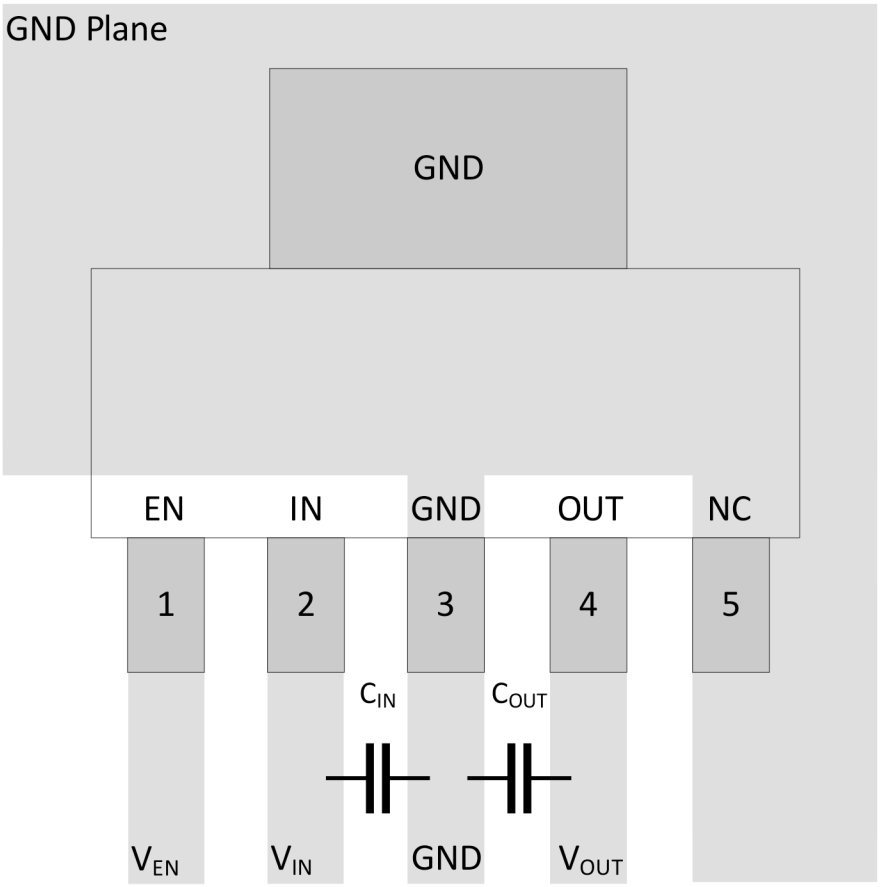


Figure 7-9. TPS796-Q1 Layout Example (New Chip)

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Nomenclature

Table 8-1. Available Options

PRODUCT(1)	DESCRIPTION
TPS79633**Qyyy** *z***M3 Q1**	**Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **yyy** is the package designator. ***z*** is the package quantity **M3** is a suffix designator for the devices that only use the latest manufacturing flow (CSO:RFB). Devices without this suffix ship with the legacy chip (CSO:DLN) or the new chip (CSO:RFB). The reel packaging label provides CSO information to distinguish which chip is used. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2012) to Revision A (June 2025)	Page
• Added device name and *Automotive* to document title	0
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *Device Information*, *ESD Ratings*, *Application and Implementation*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Changed entire document to align with current family format and to identify the features and differences of the legacy chip and new chip	1
• Added new silicon (M3) devices to document	1

- Changed *TPS796xx-Q1* to *TPS796-Q1* and *terminal* to *pin* throughout document....1
- Changed automotive-specific *Features* bullets....1
- Changed *Applications* section....1
- Changed *Terminal Functions* title to *Pin Configuration and Functions* and added Type column to *Pin Functions* table....3
- Added NC pin description to pin 5 for new chip....3
- Added new silicon curves to *Typical Characteristics* section....7
- Added new silicon block diagrams to *Functional Block Diagrams* section....13
- Deleted reference to DRB package....21
- Added *Device Nomenclature* section....25

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79633QDCQRM3Q1	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	S79633Q
TPS79633QDCQRQ1	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	79633Q
TPS79633QDCQRQ1.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	79633Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

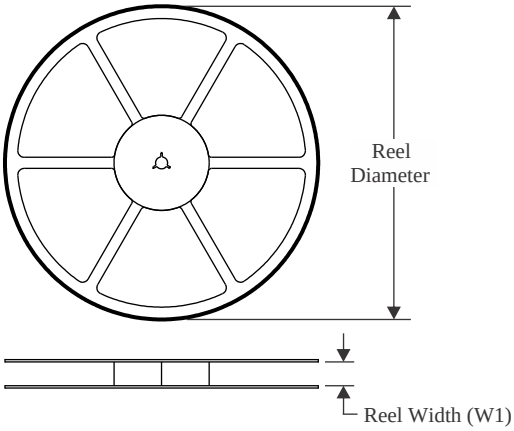
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

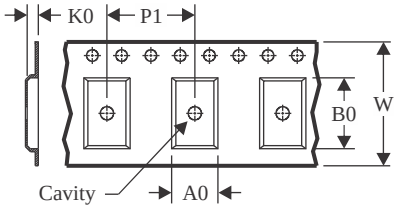
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

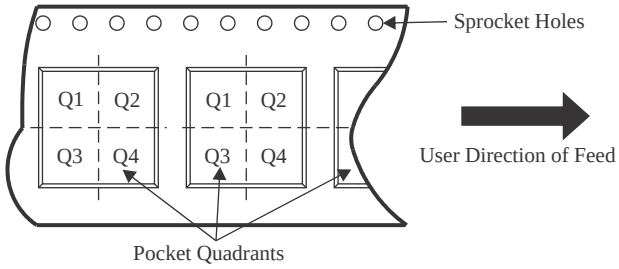


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

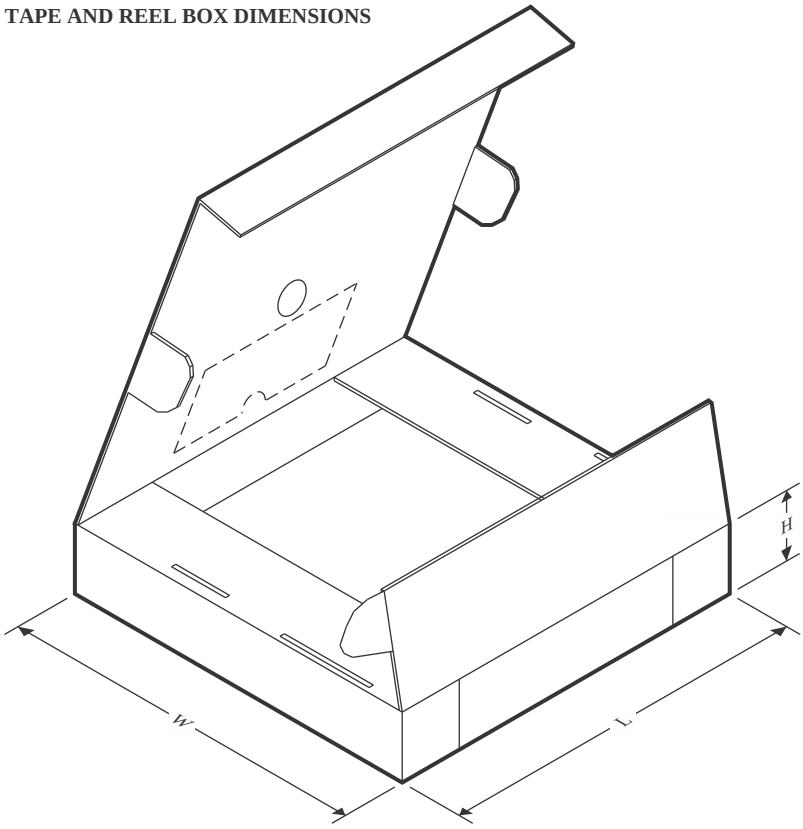
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79633QDCQRM3Q1	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS79633QDCQRQ1	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

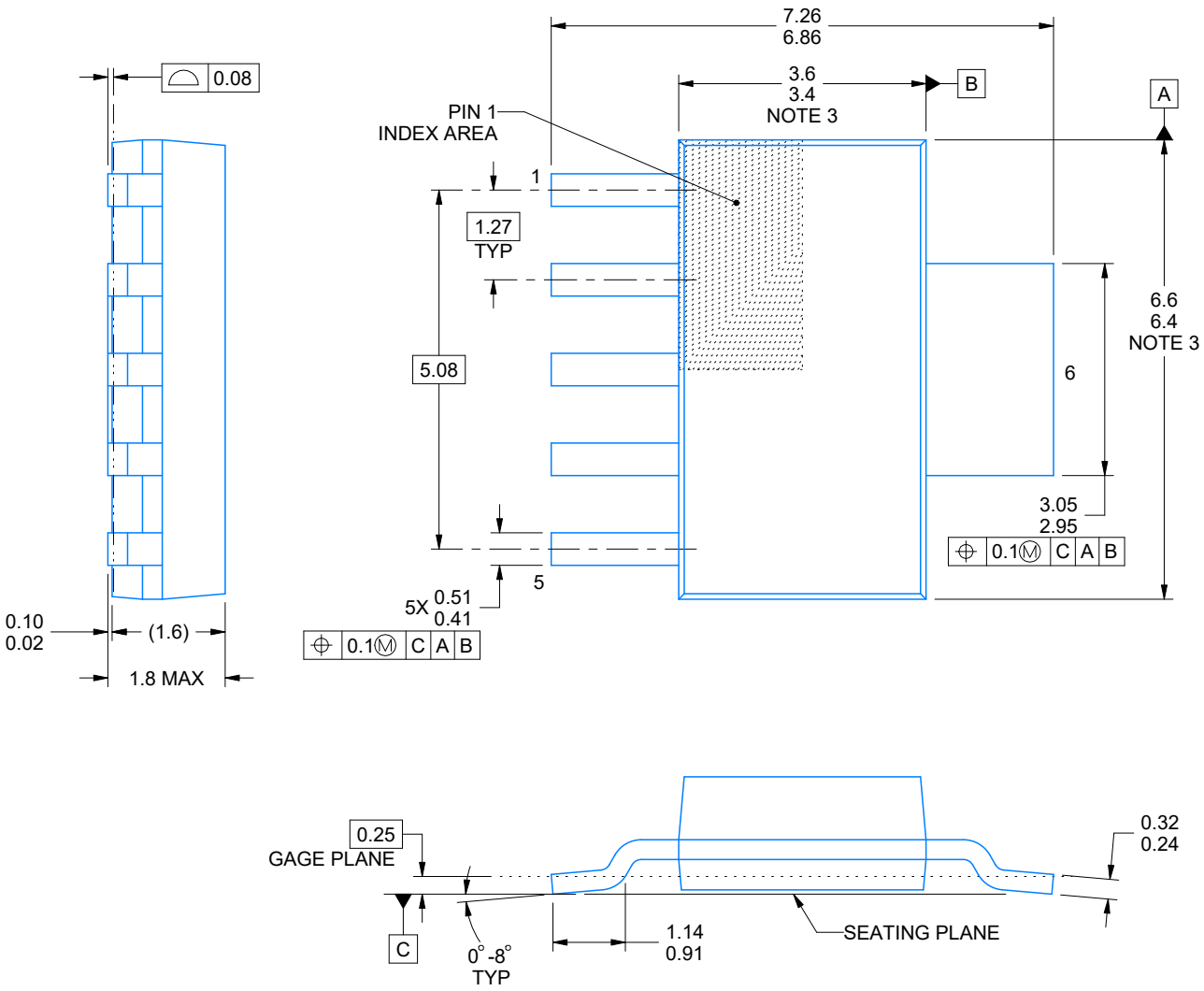
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79633QDCQRM3Q1	SOT-223	DCQ	6	2500	340.0	340.0	38.0
TPS79633QDCQRQ1	SOT-223	DCQ	6	2500	346.0	346.0	29.0

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



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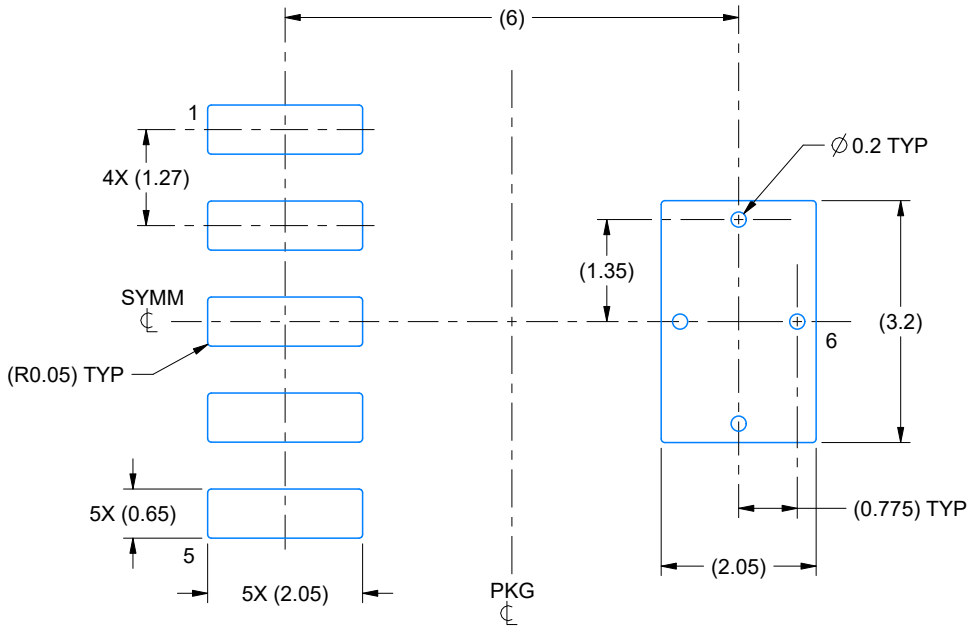
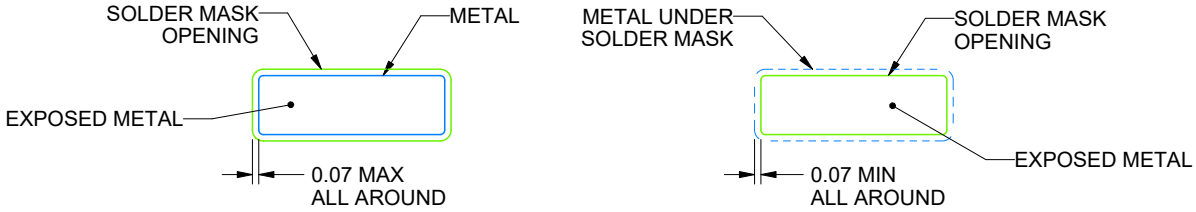
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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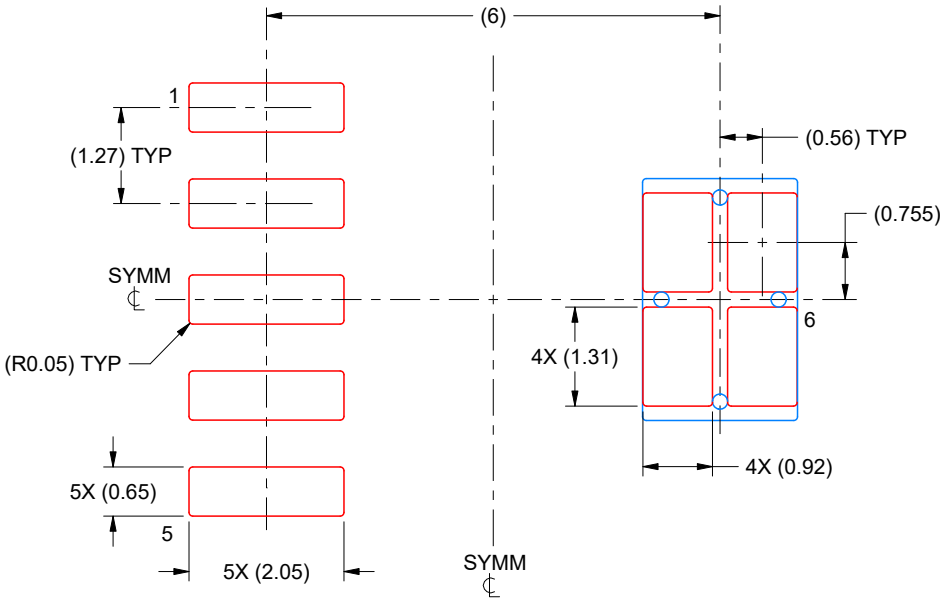
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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