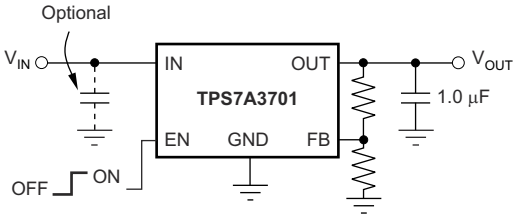
TPS7A37 1% High-Accuracy, 1A, Low-Dropout Regulator With Reverse Current Protection

1 Features

- Stable with 1µF or Larger Ceramic Output Capacitor
- Input Voltage Range: 2.2V to 5.5V
- Ultralow Dropout Voltage:
  - 200mV Maximum at 1A
- Excellent Load Transient Response—Even With Only 1µF Output Capacitor
- NMOS Topology Delivers Low Reverse Leakage Current
- Excellent Accuracy:
  - 0.23% Nominal Accuracy
  - 1% Overall Accuracy Over Line, Over Load, and Over Temperature
- Less Than 20nA typical I_Q in Shutdown Mode
- Thermal Shutdown and Current Limit for Fault Protection

2 Applications

- Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors
- Post-Regulation for Switching Supplies
- Portable and Battery-Powered Equipment



Typical Application Circuit (Adjustable Version)

3 Description

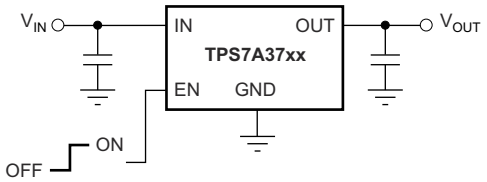
The TPS7A37 family of linear low-dropout (LDO) voltage regulators uses an NMOS pass element in a voltage-follower configuration. This topology is relatively insensitive to output capacitor value and ESR, allowing a wide variety of load configurations. Load transient response is excellent, even with a small 1µF ceramic output capacitor. The NMOS topology also allows very low dropout.

The TPS7A37 family uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 20nA and is designed for portable applications. These devices are protected by thermal shutdown and foldback current limit.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7A37	DRV (WSON, 6)	2.00mm × 2.00mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit (Fixed Version)

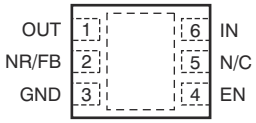
An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions



Power dissipation can limit operating range. Check *Thermal Information* table.

Figure 4-1. DRV Package, 6-Pin WSON (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
EN	4	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the *Shutdown* section under *Applications Information* for more details. EN must not be left floating and can be connected to IN if not used.
FB	2	I	Adjustable voltage version only—this pin is the input to the control loop error amplifier, and is used to set the output voltage of the device.
GND	3, Pad	—	Ground
IN	6	I	Unregulated input supply
N/C	5	—	Not connected
NR/FB	2	—	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
OUT	1	O	Regulator output. A 1.0µF or larger capacitor of any type is required for stability.
PowerPAD	—	—	

(1) I = Input; O = Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6	V
	Enable, V_{EN}	–0.3	6	
	Output, V_{OUT}	–0.3	5.5	
	V_{NR}, V_{FB}	–0.3	6	
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.2		5.5	V
V_{OUT}	Nominal output voltage range	V_{FB}		5.5 - V_{DO}	V
V_{EN}	Enable input voltage	0		V_{IN}	V
I_{OUT}	Output current	0		1	A
C_{IN}	Input capacitor		1		µF
C_{OUT}(1)	Output capacitor	1			µF
C_{NR}	Noise-reduction capacitor		10		nF
R_1(2)	Top resistor of adjustable output resistor divider		$V_{OUT(nom)}$ × 15.833		kΩ
C_{FF}	Feed-forward capacitor		10	100	nF
T_J	Operating junction temperature	–40		125	°C

(1) If the product of C_{OUT} × ESR < 50nF × Ω, the part can ring after a transient.
(2) This nominal value is for the best accuracy.

5.4 Thermal Information

THERMAL METRIC(1)		TPS7A37 New silicon	TPS7A37 Legacy silicon	UNIT
		DRV (WSON)	DRV (WSON)	
		6 PINS	6 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	67.3	67.2	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	100.8	87.6	°C/W

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THERMAL METRIC(1)		TPS7A37 New silicon	TPS7A37 Legacy silicon	UNIT
		DRV (WSON)	DRV (WSON)	
		6 PINS	6 PINS	
$R_{\theta JB}$	Junction-to-board thermal resistance	33.7	36.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.4	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.8	37.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.7	7.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.5 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 1V(1), I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2µF (unless otherwise noted). Typical values are at T_J = 25°C

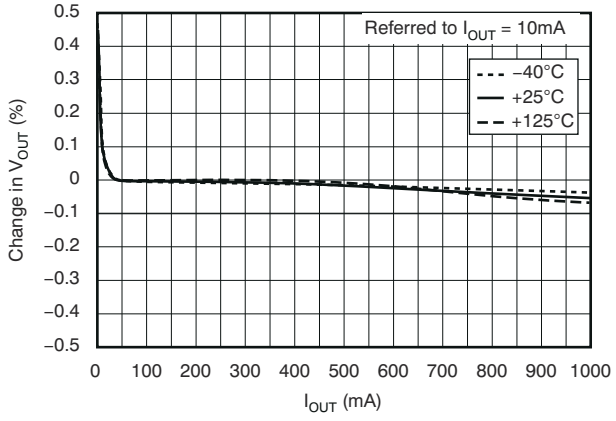
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)(2)		2.2		5.5	V
V_{FB}	Internal reference	T_J = 25°C	1.192	1.204	1.216	V
V_{OUT}	Output voltage range	TPS7A3701(4)	V_{FB}		5.5 - V_{DO}	V
	Accuracy, Nominal	T_J = 25°C		0.23		%
	Accuracy, over V_{IN}, I_{OUT}, and T(3)	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V; 10mA ≤ I_{OUT} ≤ 1A	–1		1	%
$\Delta V_{OUT(\Delta VIN)}$	Line regulation(1)	$V_{OUT(nom)}$ + 0.5V ≤ V_{IN} ≤ 5.5V, legacy silicon		0.01	0.03	%/V
$\Delta V_{OUT(\Delta VIN)}$	Line regulation(1)	$V_{OUT(nom)}$ + 0.5V ≤ V_{IN} ≤ 5.5V, new silicon		0.01	0.07	%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0.1mA ≤ I_{OUT} ≤ 300mA		0.25	0.35	%
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0.1mA ≤ I_{OUT} ≤ 300mA		3	5	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	10 mA ≤ I_{OUT} ≤ 1 A		0.5		%
V_{DO}	Dropout voltage(5) (V_{IN} = $V_{OUT(nom)}$ - 0.1V)	I_{OUT} = 1A		130	200	mV
$Z_{O(DO)}$	Output impedance in dropout	2.2V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$	1.05	1.6	2.2	A
I_{SC}	Short-circuit current	V_{OUT} = 0V		450		mA
I_{REV}	Reverse leakage current(6) (-I_{IN})	V_{EN} ≤ 0.5V, 0V ≤ V_{IN} ≤ V_{OUT}		0.1		µA
I_{GND}	Ground pin current	I_{OUT} = 10mA (I_Q)		400		µA
I_{GND}	Ground pin current	I_{OUT} = 1A, legacy silicon		1300		µA
I_{GND}	Ground pin current	I_{OUT} = 1A, new silicon		880		µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5V		20		nA
I_{FB}	Feedback pin current (TPS7A3701)			0.1	0.6	µA
PSRR	Power-supply rejection ratio (ripple rejection)	f = 100Hz, I_{OUT} = 1A		58		dB
		f = 10kHz, I_{OUT} = 1A		37		
V_N	Output noise voltage, BW = 10Hz to 100kHz	C_{OUT} = 10µF		27 × V_{OUT}		μV_{RMS}
t_{STR}	Startup time	V_{OUT} = 3V, R_L = 30Ω, C_{OUT} = 1µF, legacy silicon		600		µs
t_{STR}	Startup time	V_{OUT} = 3V, R_L = 30Ω, C_{OUT} = 1µF, new silicon		431		µs
$V_{EN(high)}$	EN pin high (enabled)		1.7		V_{IN}	V
$V_{EN(low)}$	EN pin low (shutdown)		0		0.5	V
I_{EN}	Enable pin current (enabled)	V_{EN} = 5.5V		20		nA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		
T_J	Operating junction temperature		–40		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.2V, whichever is greater.
(2) For $V_{OUT(nom)}$ < 1.6V, when V_{IN} ≤ 1.6V, the output locks to V_{IN} and can result in a damaging over-voltage condition on the output. To avoid this situation, disable the device before powering down V_{IN}. (Legacy silicon only)
(3) TPS7A3701 is tested at V_{OUT} = 1.2V.
(4) Tolerance of external resistors not included in this specification.
(5) V_{DO} is not measured for output versions with $V_{OUT(nom)}$ < 2.3V, because minimum V_{IN} = 2.2V.
(6) Fixed-voltage versions only; refer to *Application Information* section for more information.

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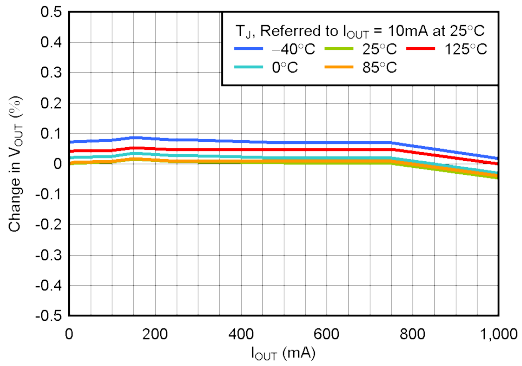
5.6 Typical Characteristics

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2µF, unless otherwise noted.



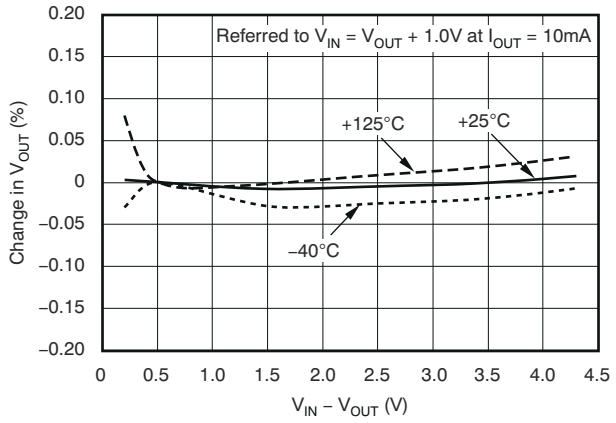
Legacy silicon

Figure 5-1. Load Regulation



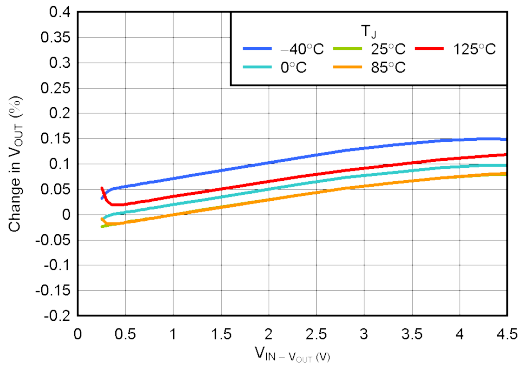
New silicon

Figure 5-2. Load Regulation



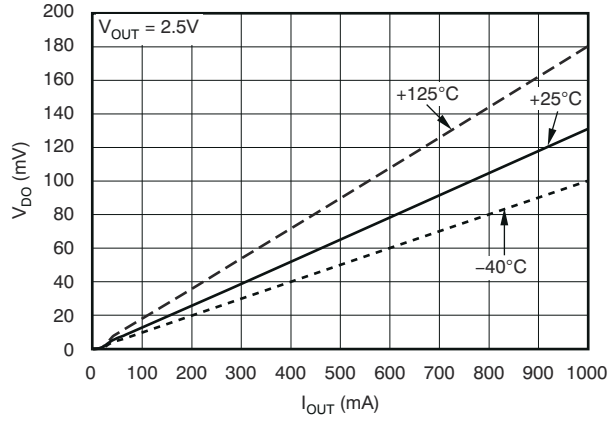
Legacy silicon

Figure 5-3. Line Regulation



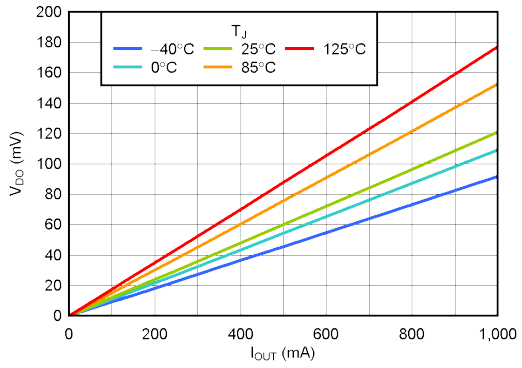
New silicon

Figure 5-4. Line Regulation



Legacy silicon

Figure 5-5. Dropout Voltage vs Output Current



New silicon

Figure 5-6. Dropout Voltage vs Output Current

5.6 Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2µF, unless otherwise noted.

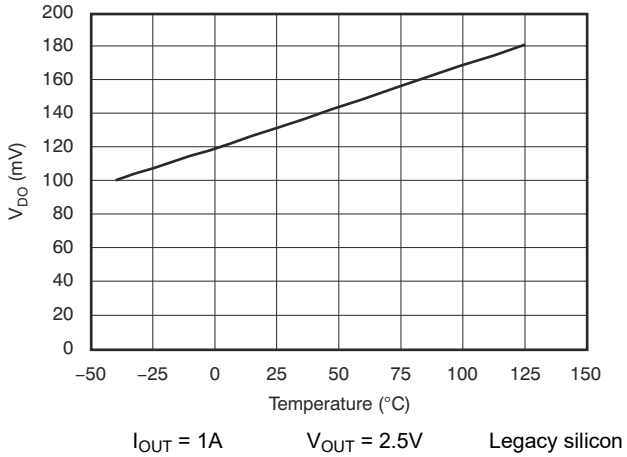


Figure 5-7. Dropout Voltage vs Temperature

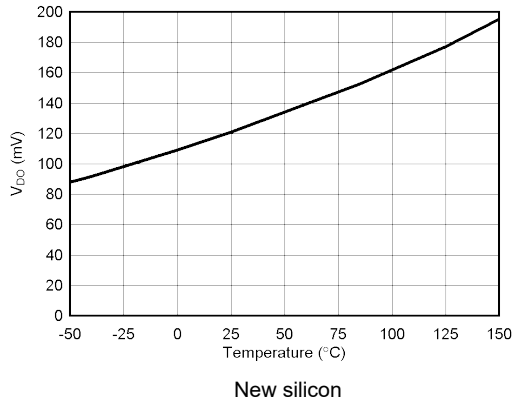


Figure 5-8. Dropout Voltage vs Temperature

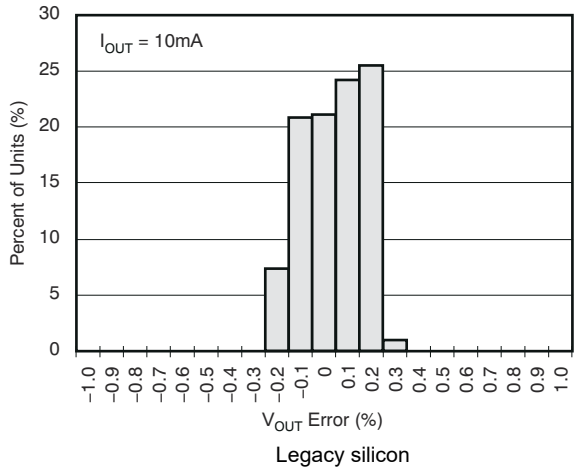


Figure 5-9. Output Voltage Histogram

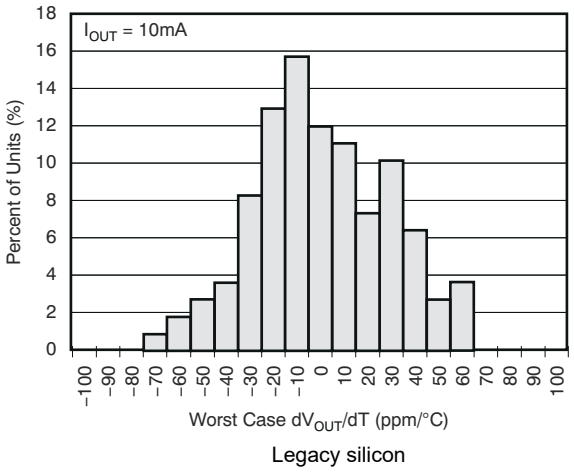


Figure 5-10. Output Voltage Drift Histogram

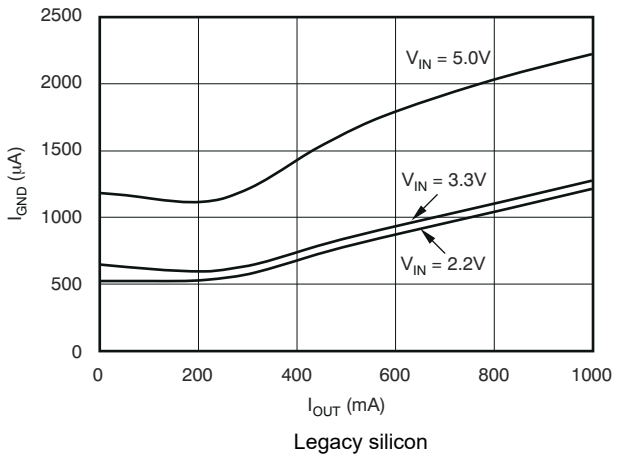


Figure 5-11. Ground Pin Current vs Output Current

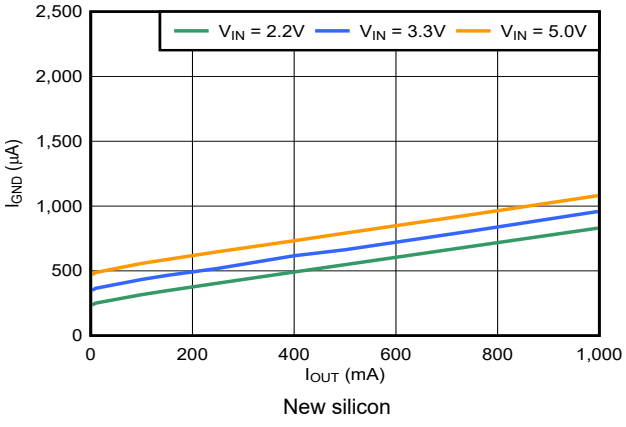
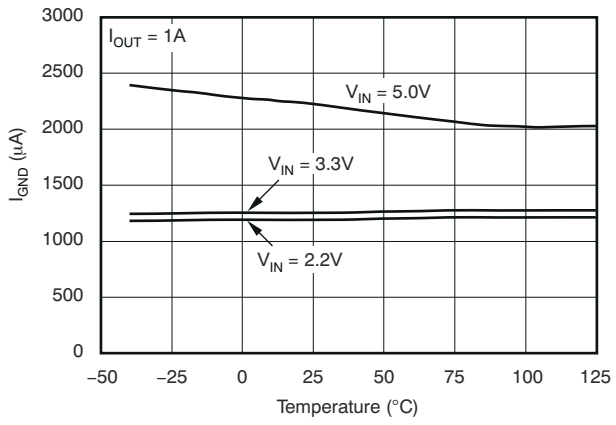


Figure 5-12. Ground Pin Current vs Output Current

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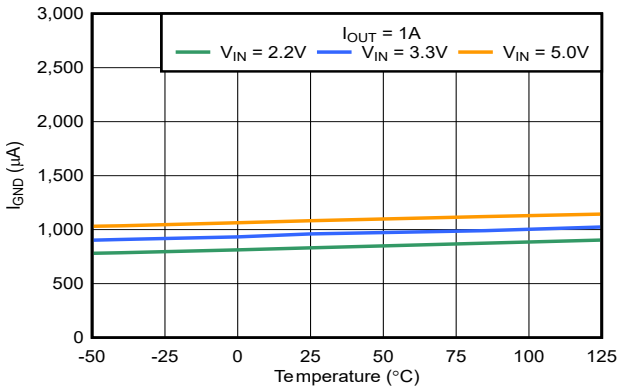
5.6 Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2µF, unless otherwise noted.



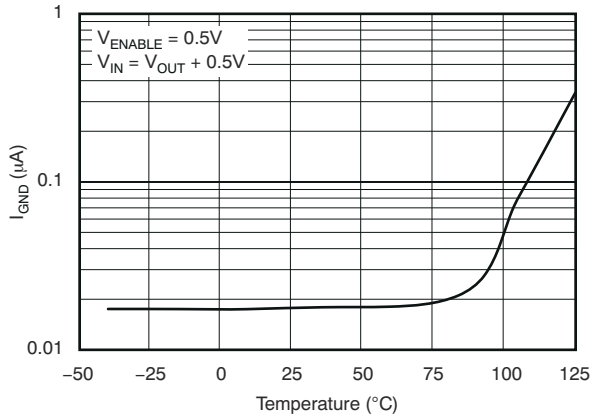
Legacy silicon

Figure 5-13. Ground Pin Current vs Temperature



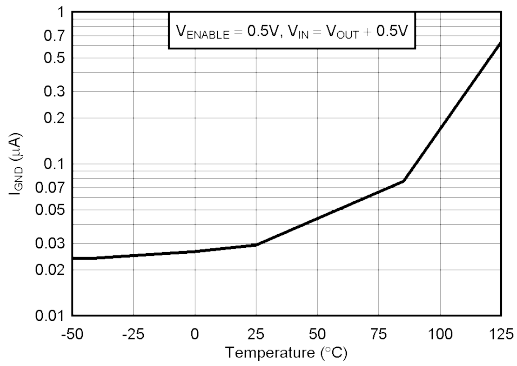
New silicon

Figure 5-14. Ground Pin Current vs Temperature



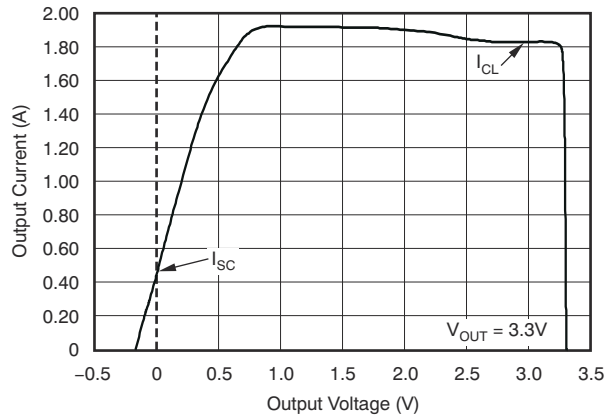
Legacy silicon

Figure 5-15. Ground Pin Current in Shutdown vs Temperature



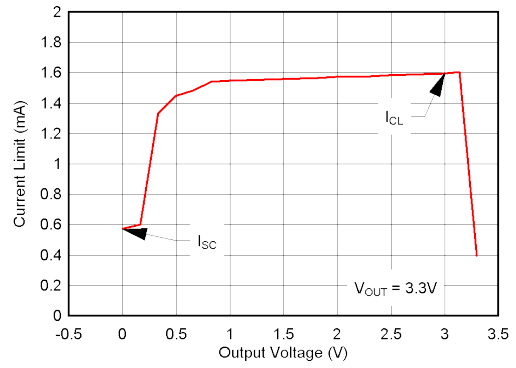
New silicon

Figure 5-16. Ground Pin Current in Shutdown vs Temperature



Legacy silicon

Figure 5-17. Current Limit vs V_{OUT} (Foldback)



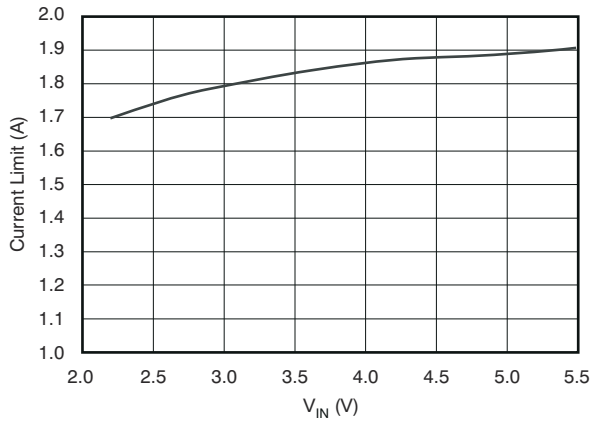
New silicon

Figure 5-18. Current Limit vs V_{OUT} (Foldback)

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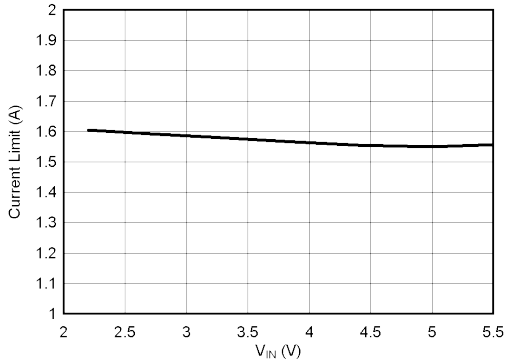
5.6 Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2µF, unless otherwise noted.



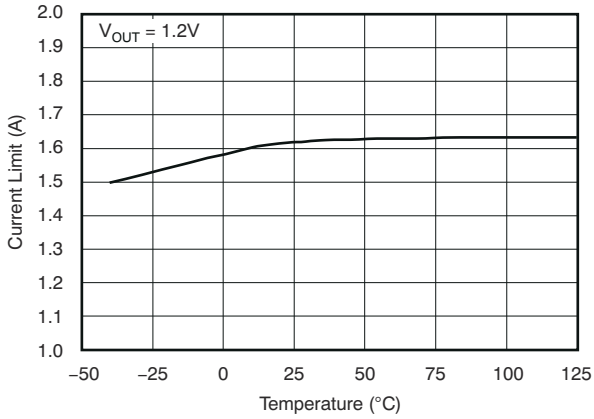
Legacy silicon

Figure 5-19. Current Limit vs V_{IN}



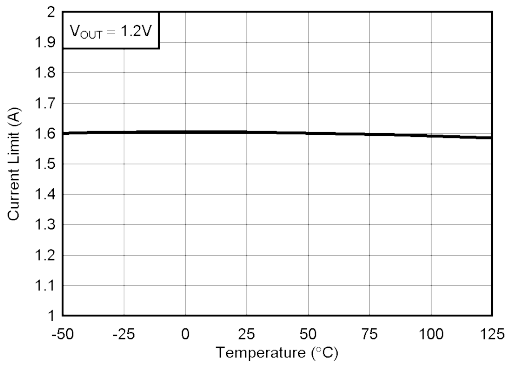
New silicon

Figure 5-20. Current Limit vs V_{IN}



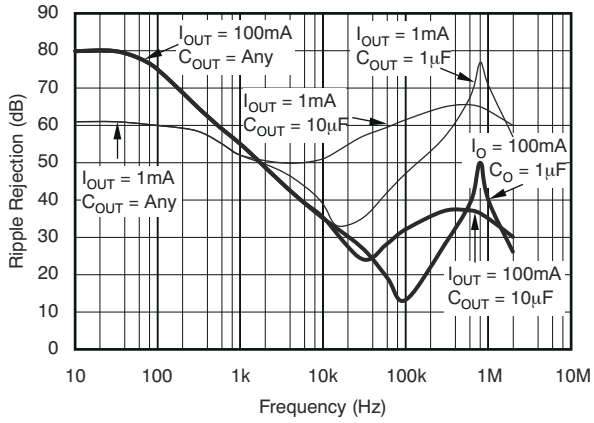
Legacy silicon

Figure 5-21. Current Limit vs Temperature



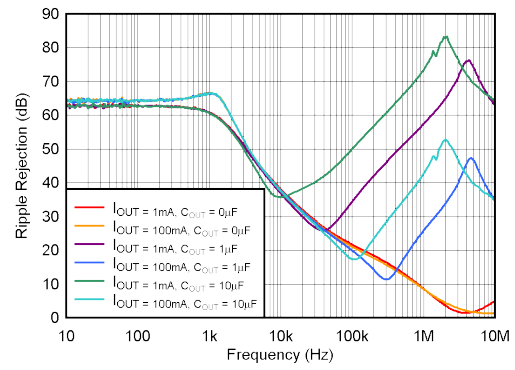
New silicon

Figure 5-22. Current Limit vs Temperature



Legacy silicon

Figure 5-23. PSRR (Ripple Rejection) vs Frequency



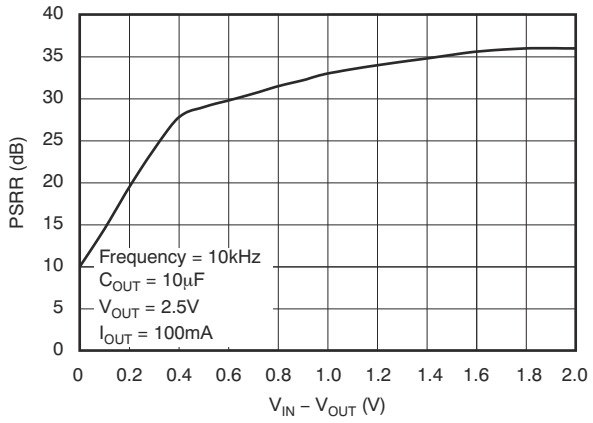
New silicon

Figure 5-24. PSRR (Ripple Rejection) vs Frequency

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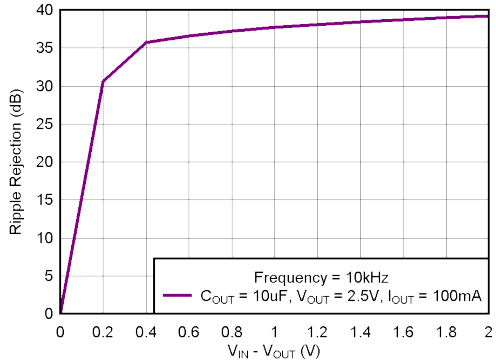
5.6 Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2µF, unless otherwise noted.



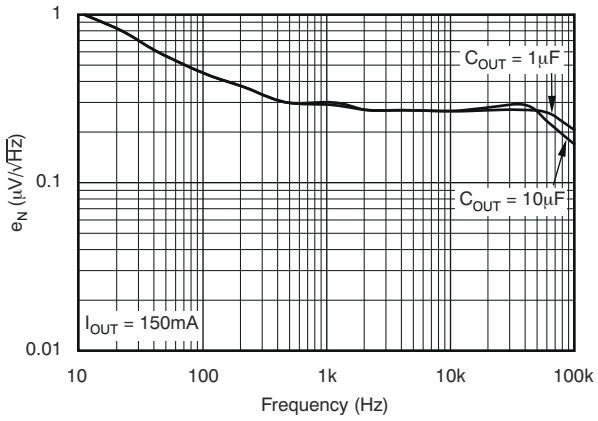
Legacy silicon

Figure 5-25. PSRR (Ripple Rejection) vs V_{IN} – V_{OUT}



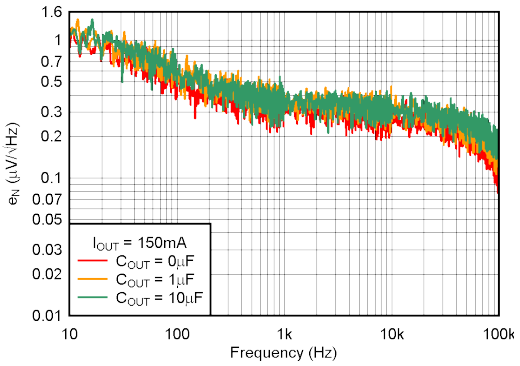
New silicon

Figure 5-26. PSRR (Ripple Rejection) vs (V_{IN} – V_{OUT})



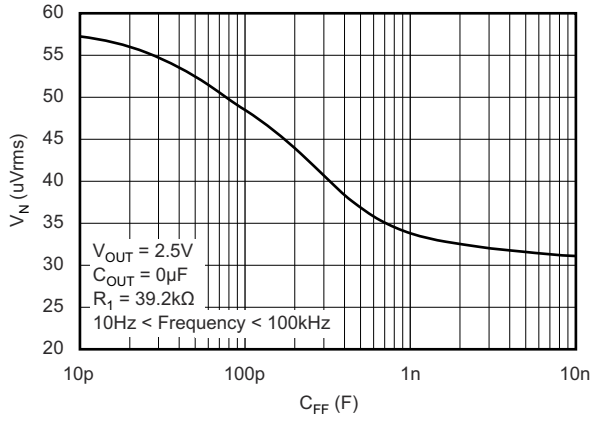
Legacy silicon

Figure 5-27. Noise Spectral Density



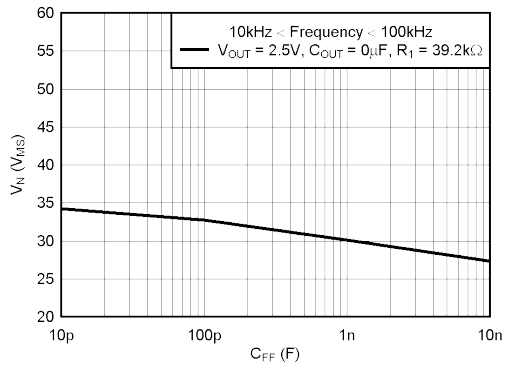
New silicon

Figure 5-28. Noise Spectral Density



Legacy silicon

Figure 5-29. TPS7A3701: RMS Noise Voltage vs C_{FF}



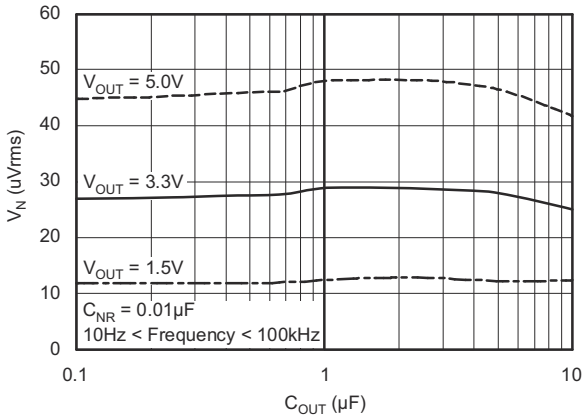
New silicon

Figure 5-30. TPS7A3701 RMS Noise Voltage vs C_{FF}

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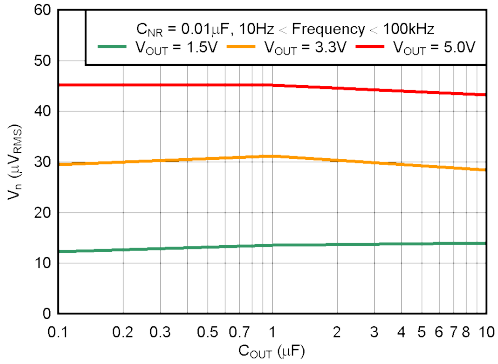
5.6 Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2µF, unless otherwise noted.



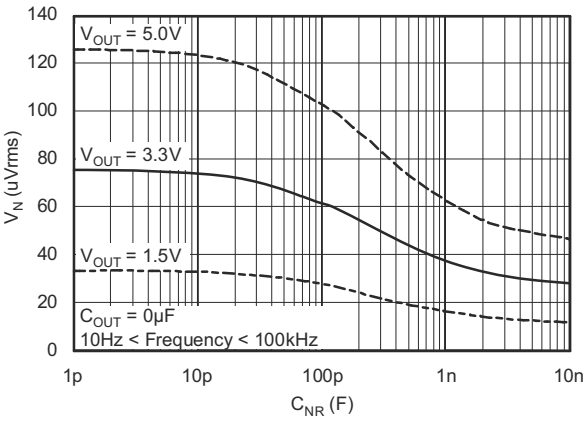
Legacy silicon

Figure 5-31. RMS Noise Voltage vs C_{OUT}



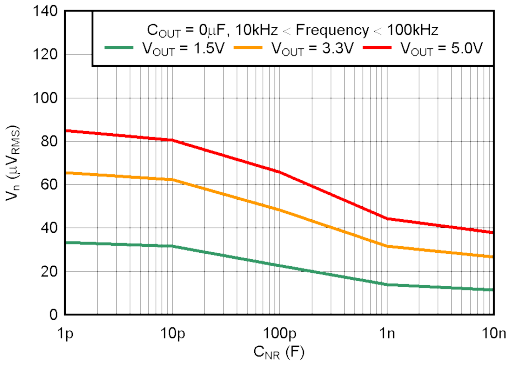
New silicon

Figure 5-32. RMS Noise Voltage vs C_{OUT}



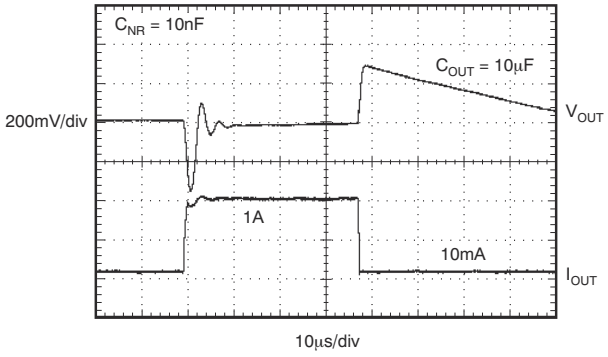
Legacy silicon

Figure 5-33. RMS Noise Voltage vs C_{NR}



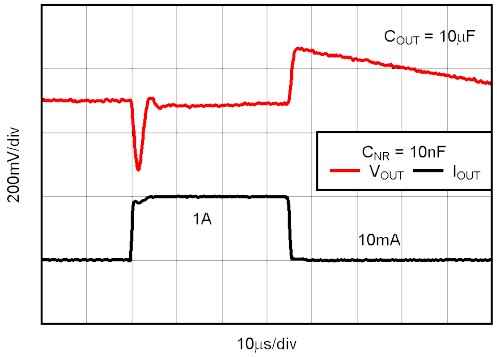
New silicon

Figure 5-34. RMS Noise Voltage vs C_{NR}



V_{OUT} = 3.3V Legacy silicon

Figure 5-35. TPS7A37: Load Transient Response



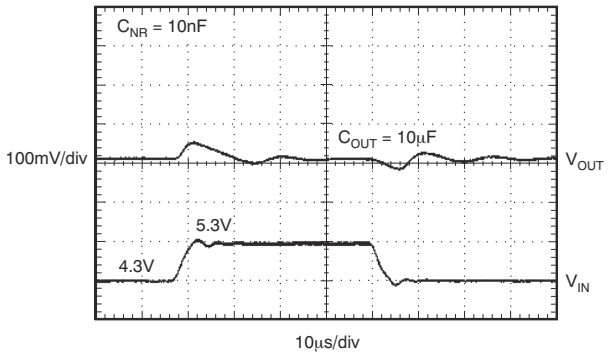
New silicon

Figure 5-36. TPS7A37 Load Transient Response

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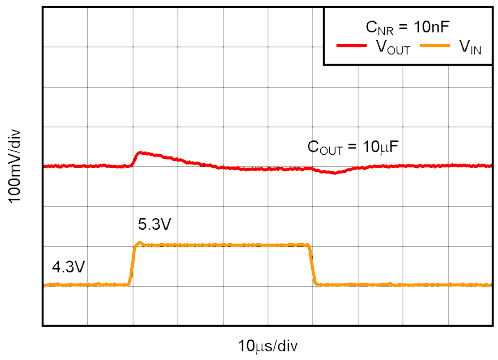
5.6 Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2µF, unless otherwise noted.



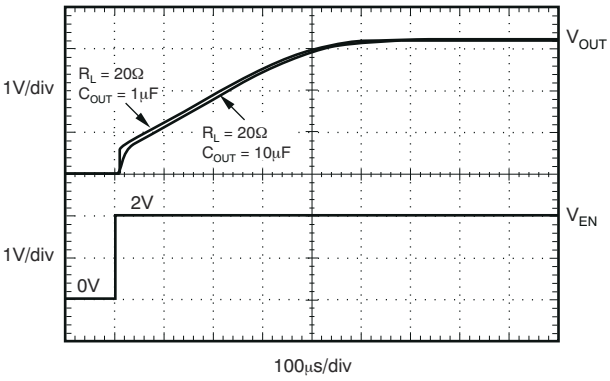
V_{OUT} = 3.3V Legacy silicon

Figure 5-37. TPS7A37: Line Transient Response



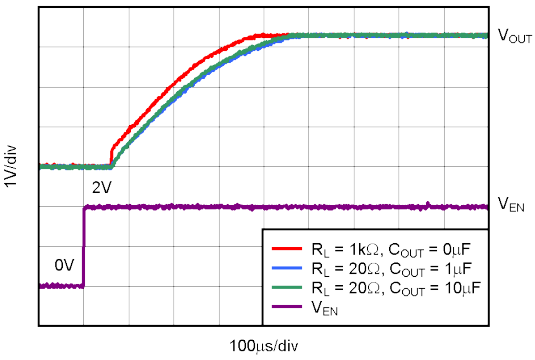
New silicon

Figure 5-38. TPS7A37 Line Transient Response



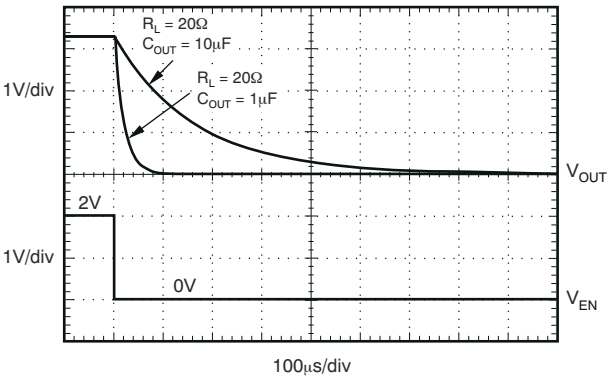
Legacy silicon

Figure 5-39. TPS7A3701: Turn-on Response



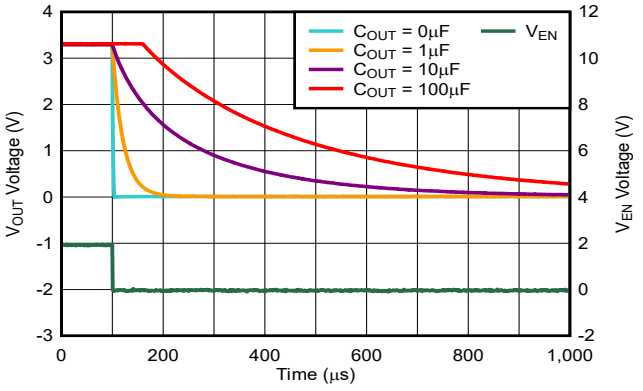
New silicon

Figure 5-40. TPS7A3701 Turn-On Response



Legacy silicon

Figure 5-41. TPS7A3701: Turn-off Response



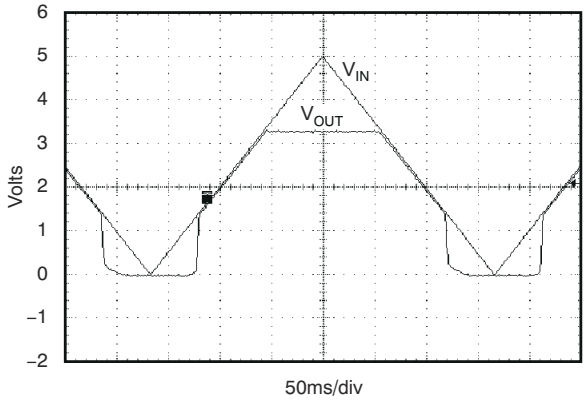
New silicon

Figure 5-42. TPS7A3701 Turn-Off Response

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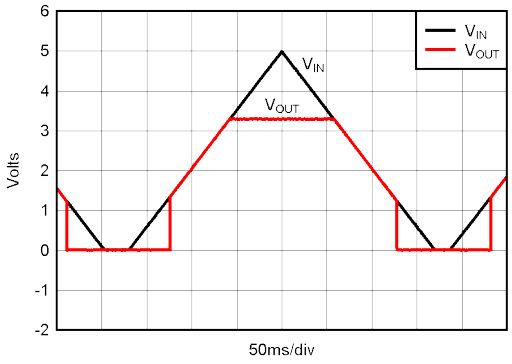
5.6 Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2µF, unless otherwise noted.



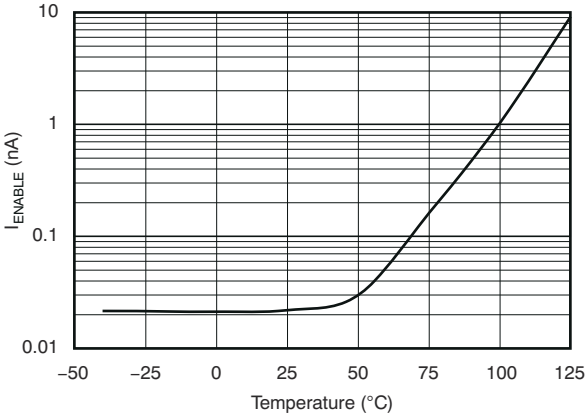
Legacy silicon

Figure 5-43. TPS7A3701: Power-up/Power-down (V_{OUT} = 3.3V)



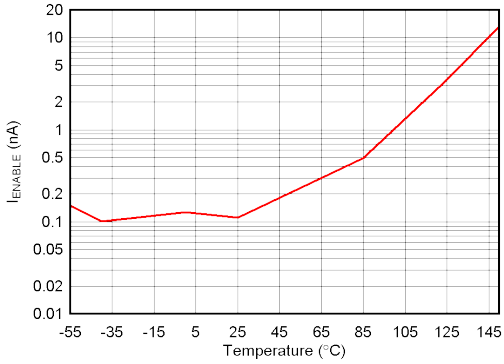
New silicon

Figure 5-44. TPS7A3701, V_{OUT} = 3.3V Power-Up and Power-Down



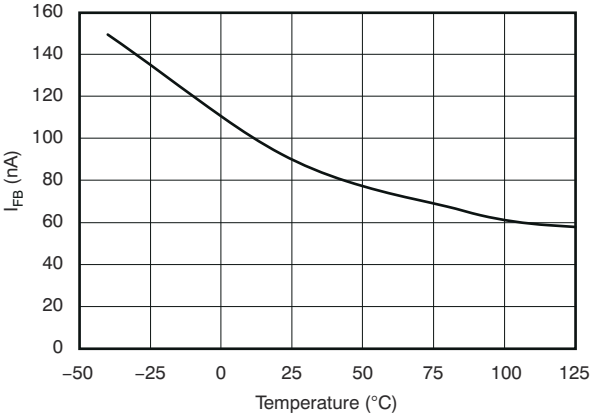
Legacy silicon

Figure 5-45. I_{ENABLE} vs Temperature



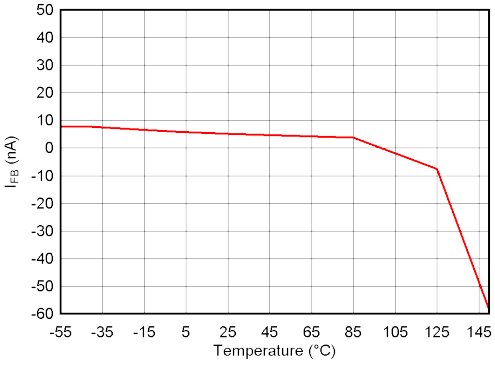
New silicon

Figure 5-46. I_{ENABLE} vs Temperature



Legacy silicon

Figure 5-47. TPS7A3701: I_{FB} vs Temperature



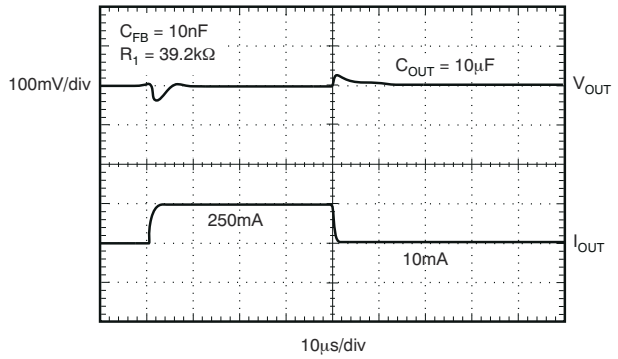
New silicon

Figure 5-48. TPS7A3701I_{FB} vs Temperature

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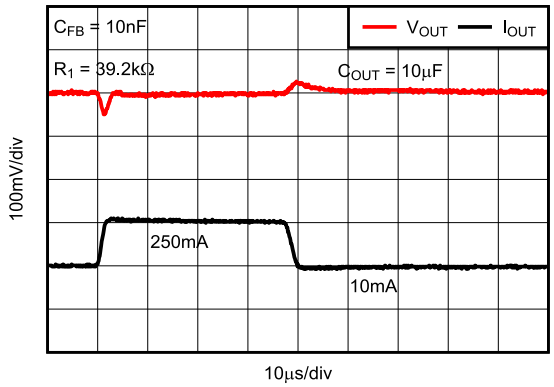
5.6 Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2µF, unless otherwise noted.



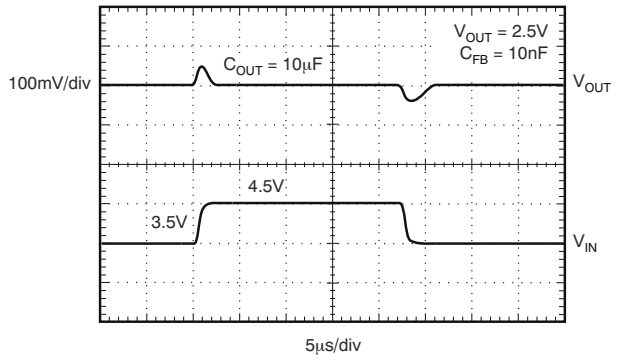
Legacy silicon

Figure 5-49. TPS7A3701: Load Transient, Adjustable Version



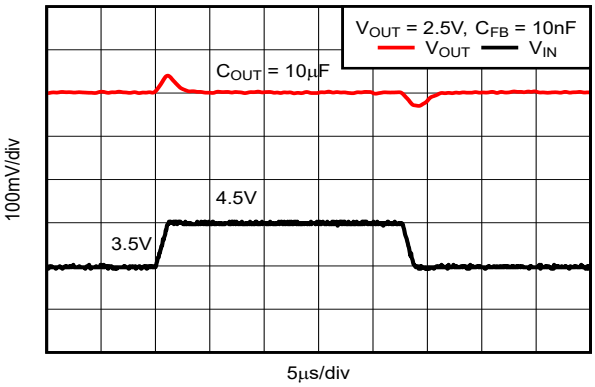
New silicon, C_{OUT} = 10µF tantalum

Figure 5-50. TPS7A3701 Load Transient, Adjustable Version



Legacy silicon

Figure 5-51. TPS7A3701: Line Transient, Adjustable Version



New silicon, C_{OUT} = 10µF tantalum

Figure 5-52. TPS7A3701 Line Transient, Adjustable Version

6 Detailed Description

6.1 Overview

The TPS7A37 belongs to a family of LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance and reverse current protection. These features combined with an enable input make the TPS7A37 designed for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

6.2 Functional Block Diagrams

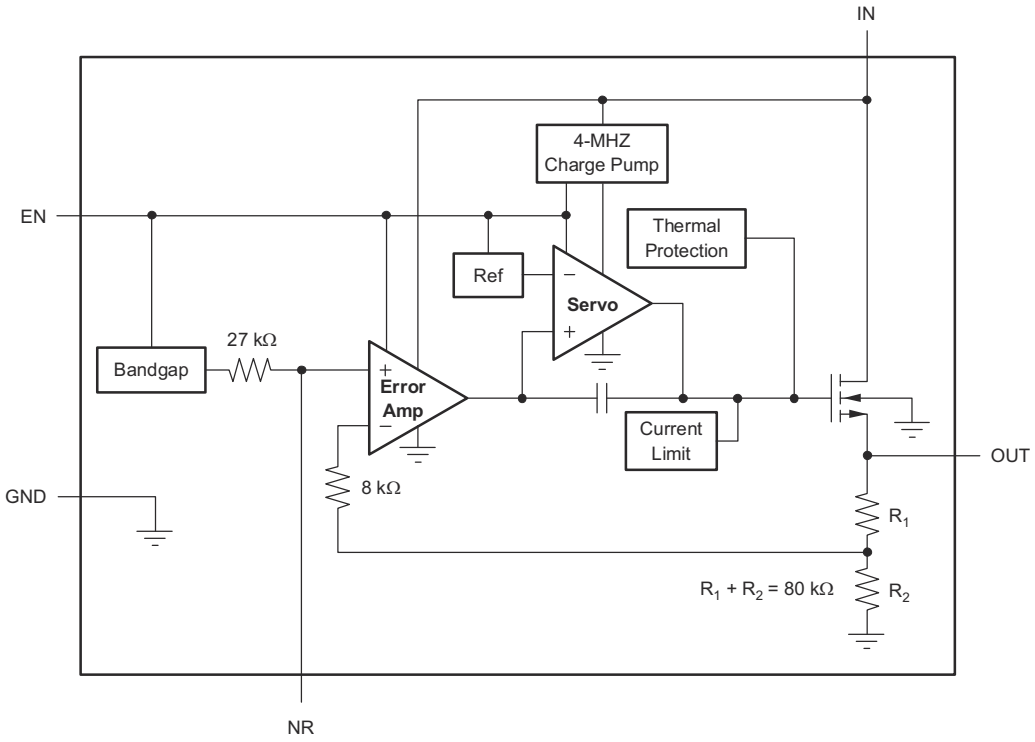
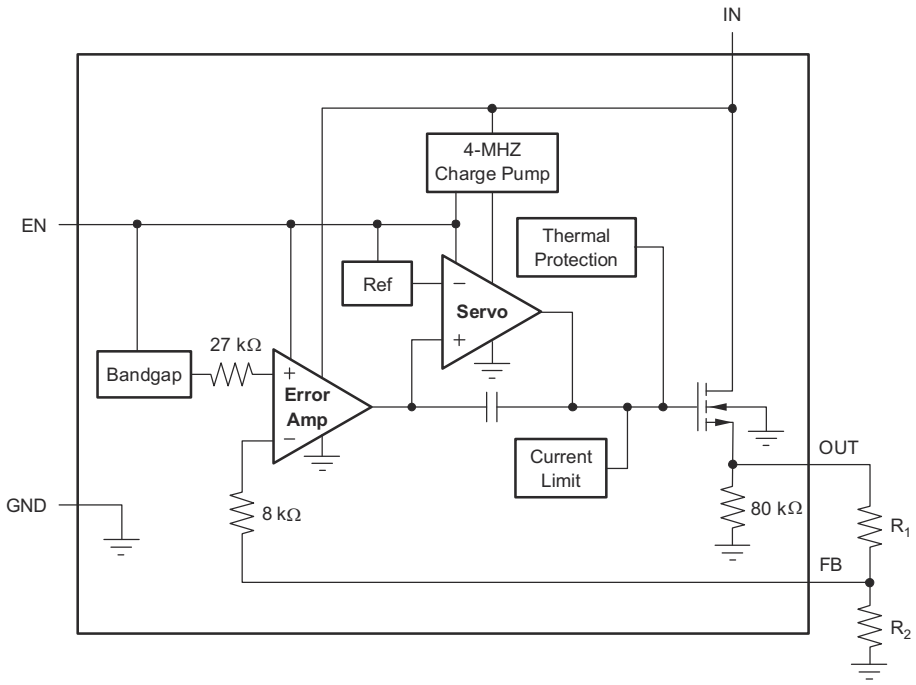


Figure 6-1. Fixed Voltage Version

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Standard 1% Resistor Values for Common Output Voltages

V_O	R_1	R_2
1.2 V	Short	Open
1.5 V	23.2 kΩ	95.3 kΩ
1.8 V	28.0 kΩ	56.2 kΩ
2.5 V	39.2 kΩ	36.5 kΩ
2.8 V	44.2 kΩ	33.2 kΩ
3.0 V	46.4 kΩ	30.9 kΩ
3.3 V	52.3 kΩ	30.1 kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1 \parallel R_2 \cong 19$ kΩ for best accuracy.

Figure 6-2. Adjustable Voltage Version

6.3 Feature Description

6.3.1 Internal Current Limit

The TPS7A37 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5V. See Figure 5-17 in the *Section 5.6* section.

Note from Figure 5-17 that approximately –0.2V of V_{OUT} results in a current limit of 0mA. Therefore, if OUT is forced below –0.2V before EN goes high, the device cannot start up. In applications that work with both a positive and negative voltage supply, the TPS7A37 must be enabled first.

6.3.2 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5V (max) turns the regulator off and drops the GND pin current to approximately 10nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate, and the output ramps back up to a regulated V_{OUT} (see Figure 5-39).

When shutdown capability is not required, EN can be connected to V_{IN}. However, the pass gate is not always discharged using this configuration, and the pass transistor can be left on (enhanced) for a significant time after V_{IN} has been removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power-up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output can overshoot upon power-up.

Note that current limit foldback can prevent device start-up under some conditions. See the *Section 6.3.1* section for more information.

6.3.3 Reverse Current

The NMOS pass element of the TPS7A37 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To verify that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass element can be left on because of stored charge on the gate.

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After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin because of voltage applied on the OUT pin. There is additional current flowing into the OUT pin as a result of the 80kΩ internal resistor divider to ground (see Figure 6-1 and Figure 6-2).

For the TPS7A3701, reverse current can flow when V_{FB} is more than 1.0V above V_{IN}.

6.4 Device Functional Modes

Driving the EN pin over 1.7V turns on the regulator. Driving the EN pin below 0.5V causes the regulator to enter shutdown mode. In shutdown, the current consumption of the device is reduced to 20nA, typically.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability if input impedance is very low, connecting a 0.1µF to 1µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator is good analog design practice. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor can be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS7A37 requires a 1µF output capacitor for stability. The device is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing can occur when C_{OUT} × ESR < 50nΩ-F. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

7.1.2 Output Noise

A precision bandgap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS7A37 and generates approximately $32\mu V_{RMS}$ (10Hz to 100kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of V_{REF} is 1.2V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (2)$$

for the case of no C_{NR}.

An internal 27kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

for C_{NR} = 10nF.

This noise reduction effect is shown as RMS Noise Voltage vs C_{NR} in the *Typical Characteristics* section.

The TPS7A3701 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the feedback pin (FB) reduces output noise and improves load transient performance. This capacitor must be limited to 0.1µF.

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The TPS7A37 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates approximately 250µV of switching noise at approximately 4MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

7.1.3 Dropout Voltage

The TPS7A37 uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS, ON}$ of the NMOS pass element.

For large step changes in load current, the TPS7A37 requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of V_{IN} – V_{OUT} above this line verify normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to dc dropout levels], the TPS7A37 can take a couple of hundred microseconds to return to the specified regulation accuracy.

7.1.4 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without a 1.0µF output capacitor. As with any regulator, the addition of additional capacitance from the OUT pin to ground reduces undershoot magnitude but increases the duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the OUT pin to the FB pin also improves the transient response.

The TPS7A37 does not have active pull-down when the output is over-voltage. This architecture allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This architecture also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal or external load resistance. The rate of decay is given by:

(Fixed voltage version)

$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (4)$$

(Adjustable voltage version)

$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$

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7.2 Typical Applications

7.2.1 Typical Application

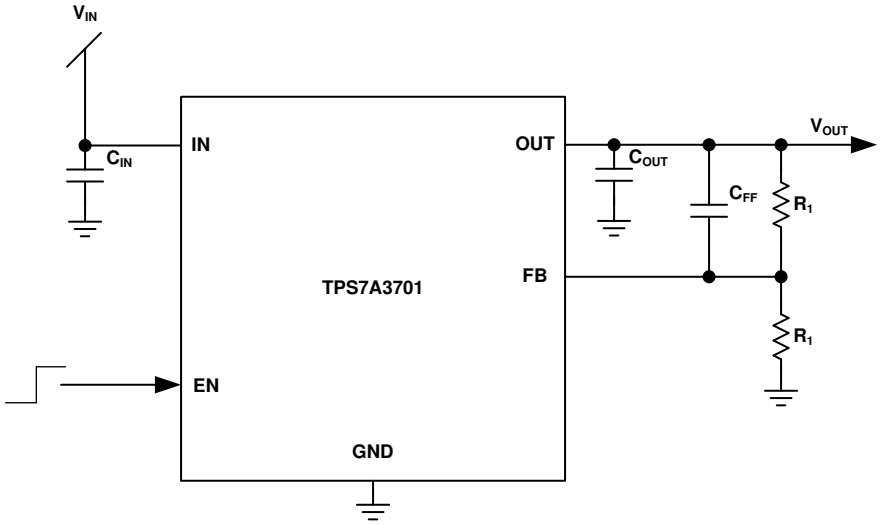


Figure 7-1. Typical Application Schematic

7.2.1.1 Design Requirements

Table 7-1 lists the design parameters.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.6V
Output voltage	3.3V
DC output current	100mA
Peak output current	1A

7.2.1.2 Detailed Design Procedure

Due to the transients in this application input and output capacitors must be used. A C_{IN} = C_{OUT} = 10µF capacitor has been selected.

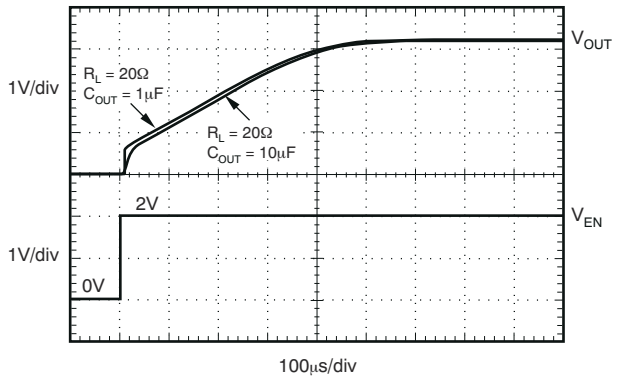
The ESR of the chosen capacitor can be checked by looking the magnitude of the complex impedance over frequency. When |Zc| reaches a minimum the DC ESR is the value of |Zc| at that frequency. The ESR of the chosen capacitor is 10mΩ, which gives us a product of 10mΩ × 10µF = 100nΩ-F > 50nΩ-F, minimizing the ringing during transients.

As the V_{IN} - V_{OUT} change is only 300mV with a 100mA DC current, the expected junction temperature rise over the ambient, on a JEDEC standard board, is 67.2C/W × 0.3V × 0.1A = 2C.

To provide the best accuracy, R1 = 52.3kΩ and R2 = 30.1kΩ, and a 10nF C_{FF} is used to reduce output noise.

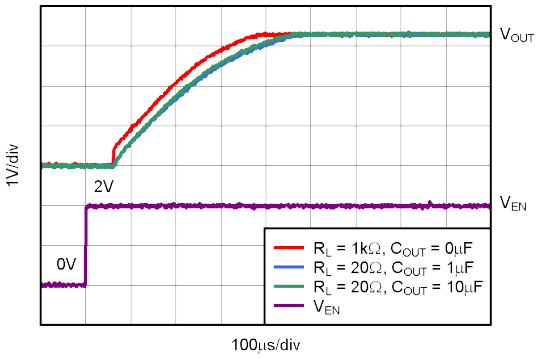
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7.2.1.3 Application Curves



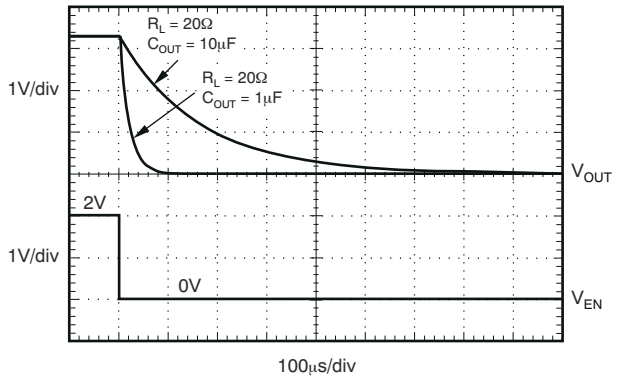
Legacy silicon

Figure 7-2. TPS7A3701: Turn-on Response



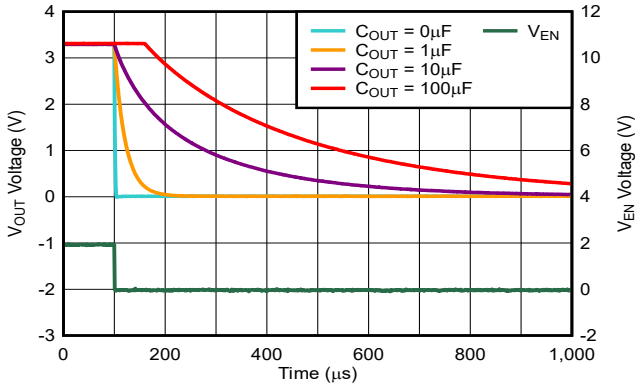
New silicon

Figure 7-3. TPS7A3701 Turn-On Response



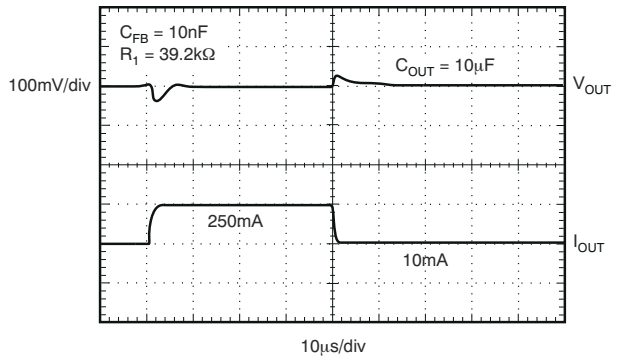
Legacy silicon

Figure 7-4. TPS7A3701: Turn-off Response



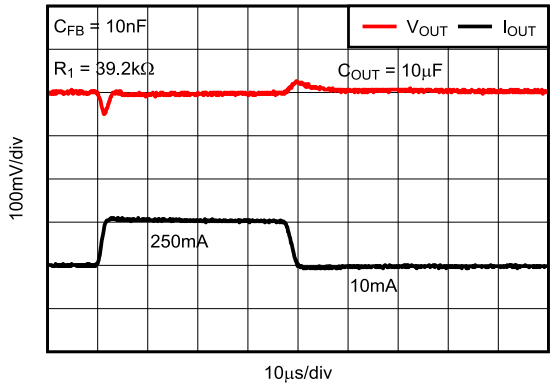
New silicon

Figure 7-5. TPS7A3701 Turn-Off Response



Legacy silicon

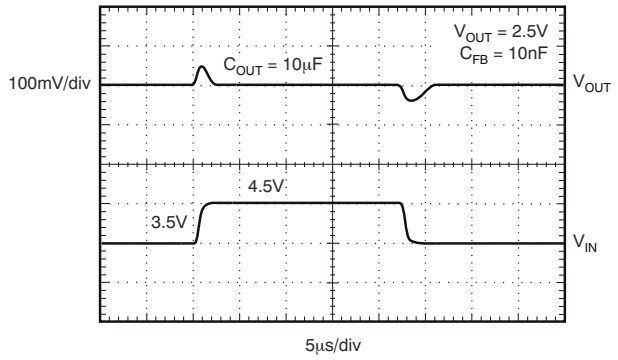
Figure 7-6. TPS7A3701: Load Transient, Adjustable Version



New silicon, C_{OUT} = 10µF tantalum

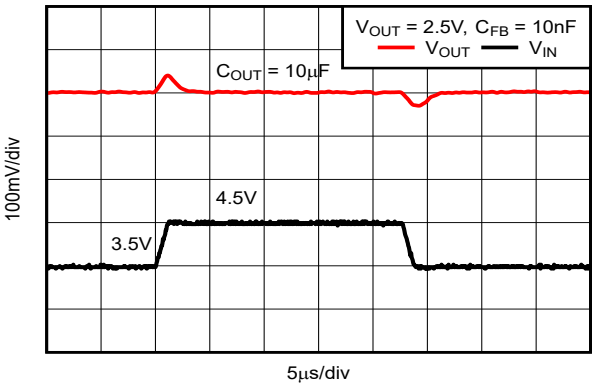
Figure 7-7. TPS7A3701 Load Transient, Adjustable Version

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Legacy silicon

Figure 7-8. TPS7A3701: Line Transient, Adjustable Version



New silicon, C_{OUT} = 10µF tantalum

Figure 7-9. TPS7A3701 Line Transient, Adjustable Version

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7.2.2 Fixed-Voltage Version

Figure 7-10 shows the basic circuit connections for the fixed voltage models.

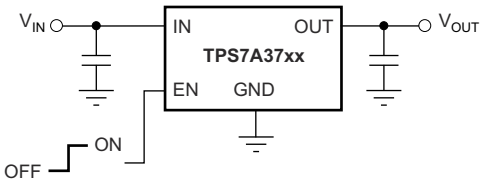


Figure 7-10. Typical Application Circuit for Fixed-Voltage Version

7.2.3 Adjustable Operation

Figure 7-11 gives the connections for the adjustable output version, TPS7A3701 [1].

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 7-11. Sample resistor values for common output voltages are shown in Figure 6-2.

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19kΩ. This 19kΩ, in addition to the internal 8kΩ resistor, presents the same impedance to the error amp as the 27kΩ bandgap reference output. This impedance helps compensate for leakages into the error amp terminals.

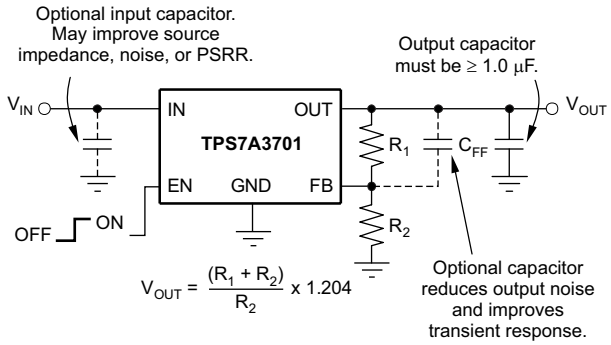


Figure 7-11. Typical Application Circuit for Adjustable-Voltage Version(1)

7.3 Power Supply Recommendations

The input supply for the LDO must be within the recommended operating conditions (that is, between 2.2V to 5.5V). The input voltage must provide adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output transient performance.

7.4 Layout

7.4.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin must be bypassed to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

The GND pin must be tied directly to the PowerPAD under the IC. The PowerPAD must be connected to any internal PCB ground planes using multiple vias directly under the IC.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits can impact system performance negatively, and even cause instability.

[1] Product-preview device.

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7.4.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance (such as PSRR, output noise, and transient response), design the board with ground plane connections for V_{IN} and V_{OUT} capacitors. Furthermore. make sure the ground plane is connected at the GND pin of the device.

7.4.1.2 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the device from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least +35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A37 has been designed to protect against overload conditions. The circuit is not intended to replace proper heatsinking. Continuously running the TPS7A37 into thermal shutdown degrades device reliability.

7.4.1.3 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and verifying reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 6:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{6}$$

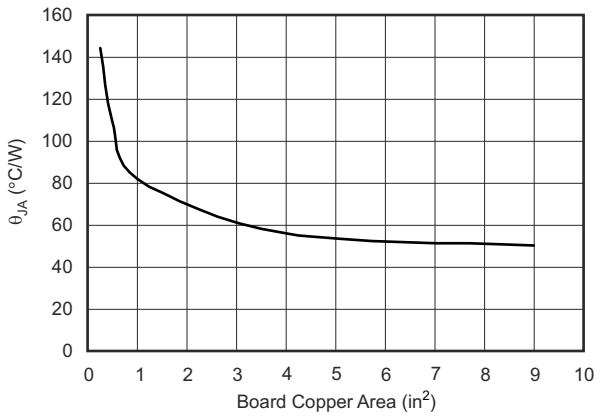
Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the WSON (DRV) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, the pad must be attached to an appropriate amount of copper PCB area to verify the device does not overheat. That tab must be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 7:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \tag{7}$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 7-12.

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θ_{JA} value at board size of 9in^2 (that is, 3in × 3in) is a JEDEC standard.

Figure 7-12. DRV (WSON) Package θ_{JA} vs Board Size

Figure 7-12 shows the variation of θ_{JA} as a function of ground plane copper area in the board. This image is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and must not be used to estimate actual thermal performance in real application environments.

Note

When the device is mounted on an application PCB, use Ψ_{JT} and Ψ_{JB}, as explained in the *Section 7.4.1.4* section.

7.4.1.4 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 8). For backwards compatibility, an older *$\theta_{JC,Top}$* parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{8}$$

Where P_D is the power dissipation shown by Equation 6, T_T is the temperature at the center-top of the IC package, and T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (as Figure 7-14 shows).

Note

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.

By looking at Figure 7-13, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 8 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

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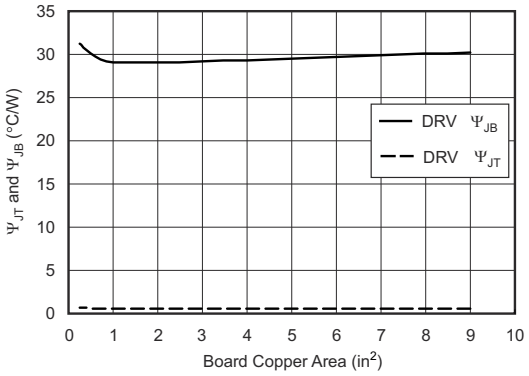
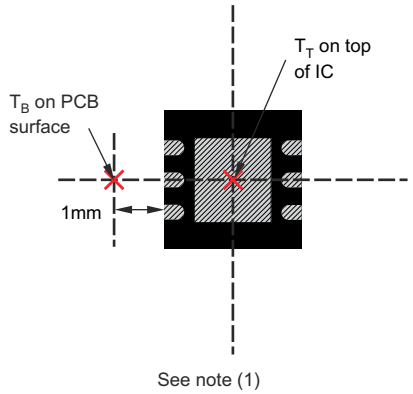


Figure 7-13. DRV (WSON) Package Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, refer to application note SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com. For further information, refer to application note SPRA953, *Semiconductor and IC Package Thermal Metrics*, also available on the TI website.



A. Power dissipation can limit operating range. Check *Thermal Information* table.
B. Example DRV (SON) Package Measurement

Figure 7-14. Measuring Points for T_T and T_B

7.4.2 Layout Example

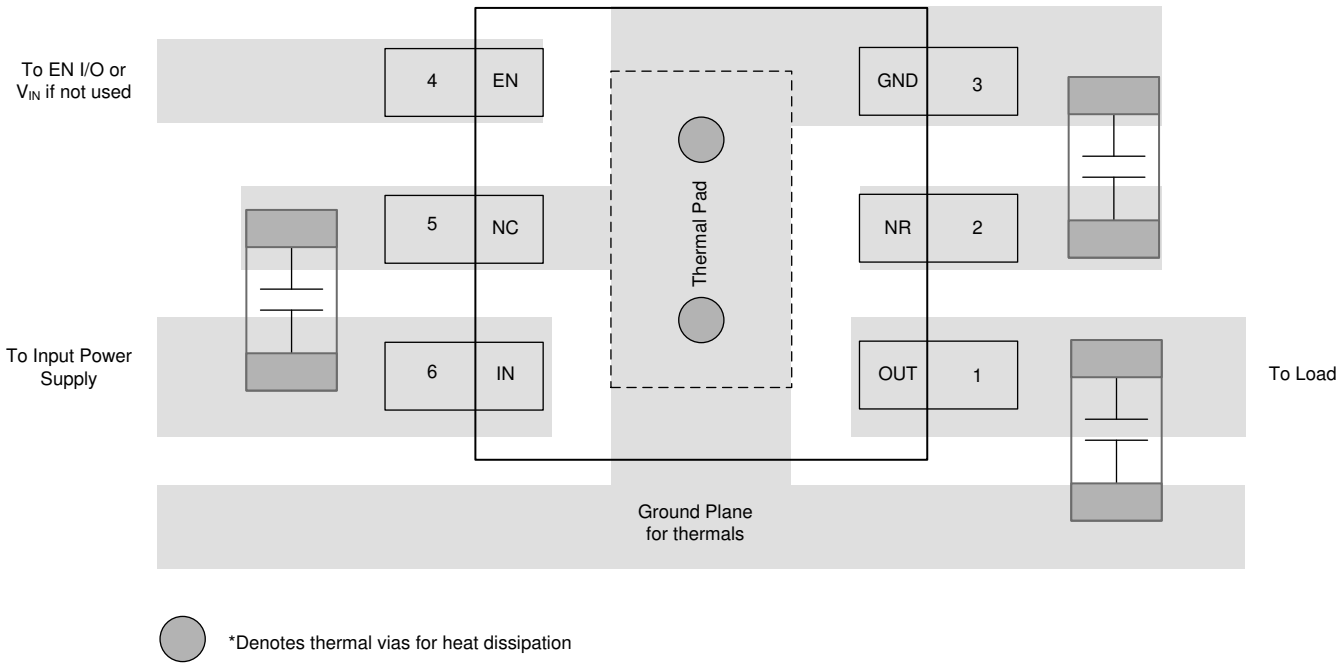


Figure 7-15. Fixed Voltage Layout

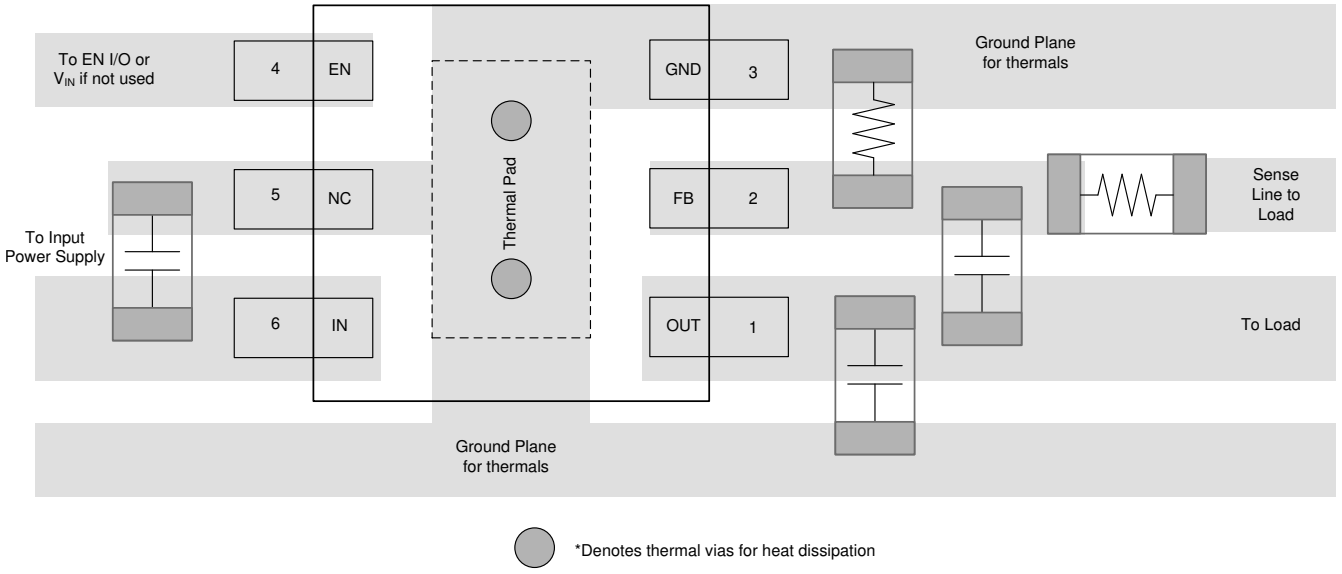


Figure 7-16. Adjustable Voltage Layout

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Available Options

PRODUCT[1]	DESCRIPTION
TPS7A37**xxyyyz(M3)**	**xx** is the nominal output voltage (for example, 25 = 2.5V, 01 = Adjustable[1]). **yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix can ship with the *legacy silicon* (CSO: DLN) or the *new silicon* (CSO: RFB). The reel packaging label provides CSO information to distinguish which silicon is being used. Device performance for new and legacy silicon is denoted throughout the document.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *TPS7A37xxEVM-529 Evaluation Module* user's guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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Changes from Revision B (July 2015) to Revision C (October 2026) **Page**

- Added new silicon thermal results for DRV (WSON) package....4
- Updated internal reference typical value....6
- Added new silicon line regulation....6
- Added new silicon ground current....6
- Added new silicon ground pin current spec....6
- Added new silicon startup time spec....6
- Added *Device Nomenclature* section....29

Changes from Revision A (July 2013) to Revision B (July 2015) **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A3701DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJI
TPS7A3701DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJI
TPS7A3701DRVRM3	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJI
TPS7A3701DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJI
TPS7A3701DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJI
TPS7A3721DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIX
TPS7A3721DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIX
TPS7A3721DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIX
TPS7A3721DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIX
TPS7A3725DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJH
TPS7A3725DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJH
TPS7A3725DRVRM3	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJH
TPS7A3725DRVT	Obsolete	Production	WSON (DRV) | 6	-	-	Call TI	Call TI	-40 to 125	SJH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

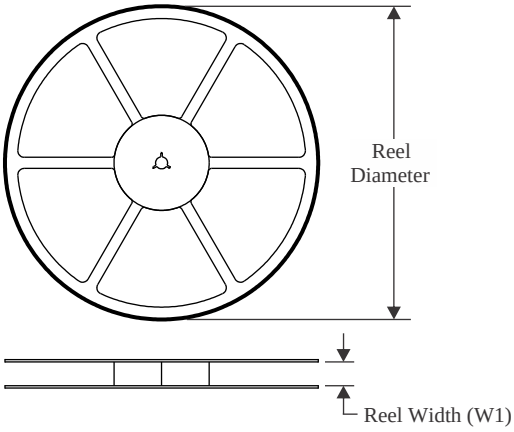
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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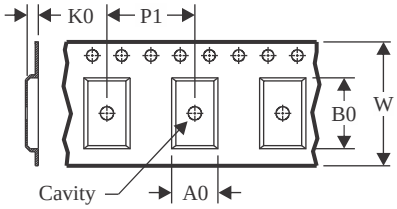
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

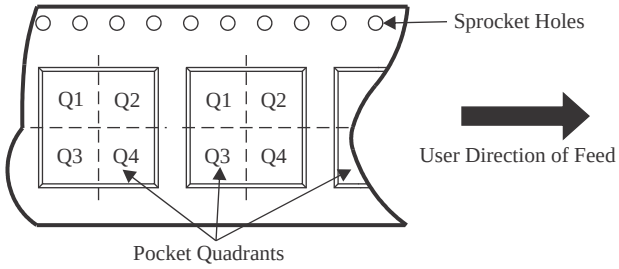


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

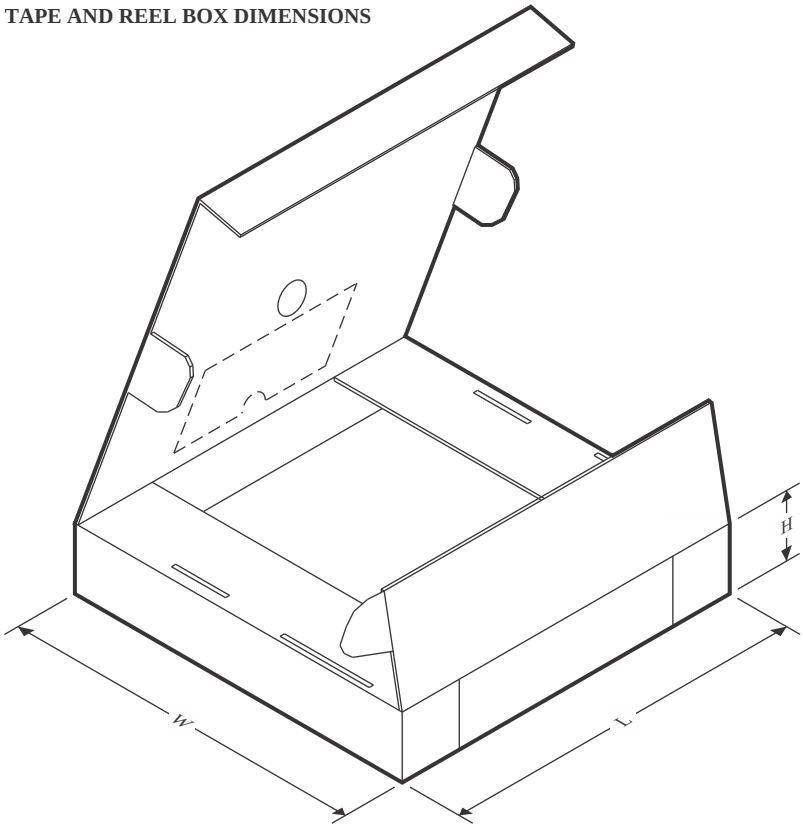
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A3701DRVRM3	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A3721DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS7A3721DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS7A3725DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS7A3725DRVRM3	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

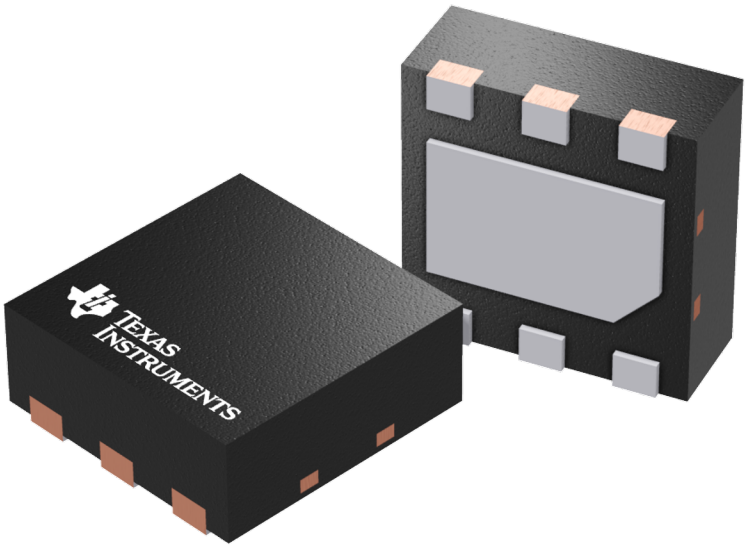


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A3701DRVRM3	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7A3721DRVR	WSON	DRV	6	3000	213.0	191.0	35.0
TPS7A3721DRVT	WSON	DRV	6	250	213.0	191.0	35.0
TPS7A3725DRVR	WSON	DRV	6	3000	213.0	191.0	35.0
TPS7A3725DRVRM3	WSON	DRV	6	3000	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



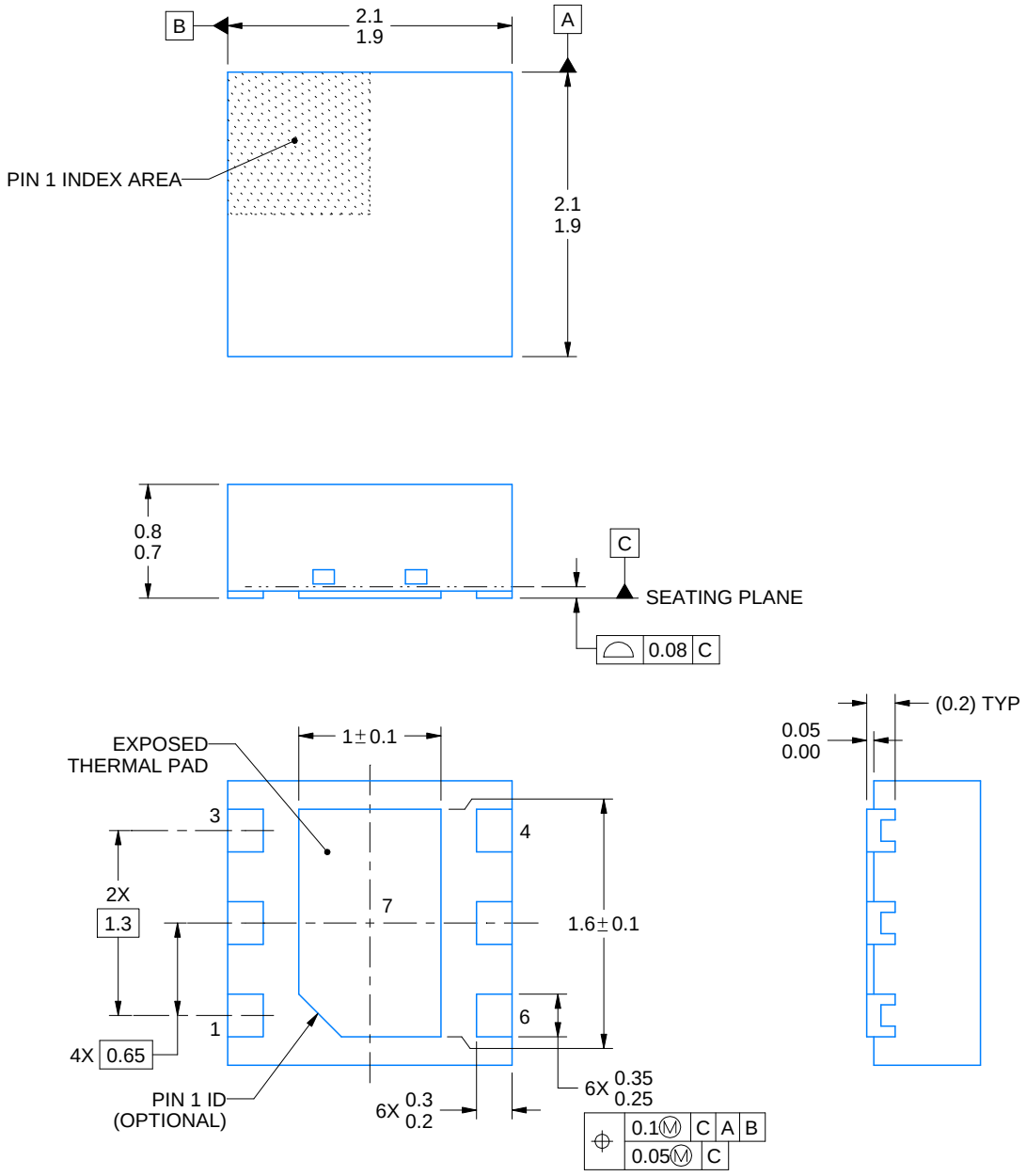
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

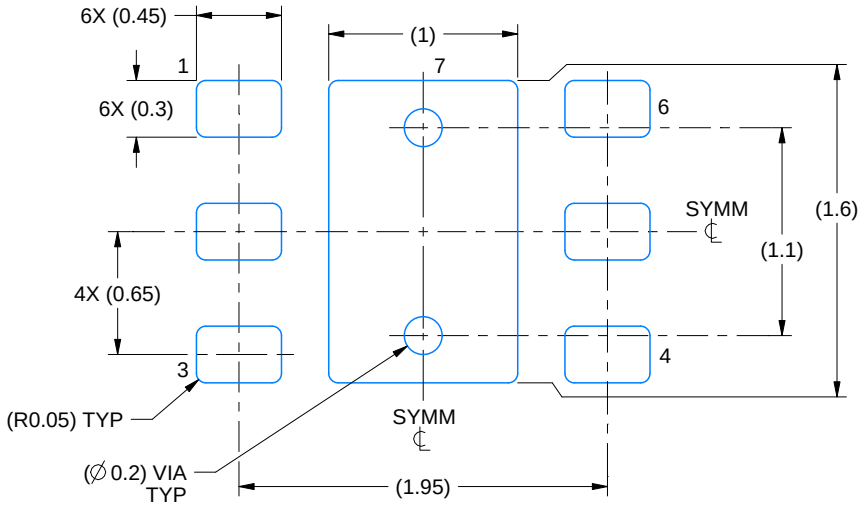
PLASTIC SMALL OUTLINE - NO LEAD



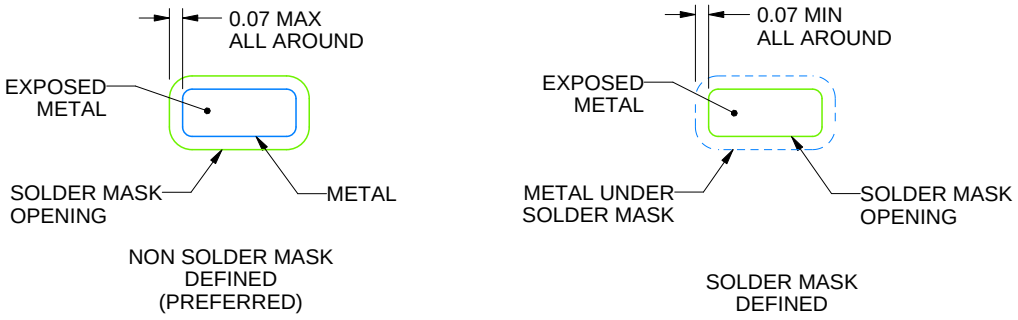
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

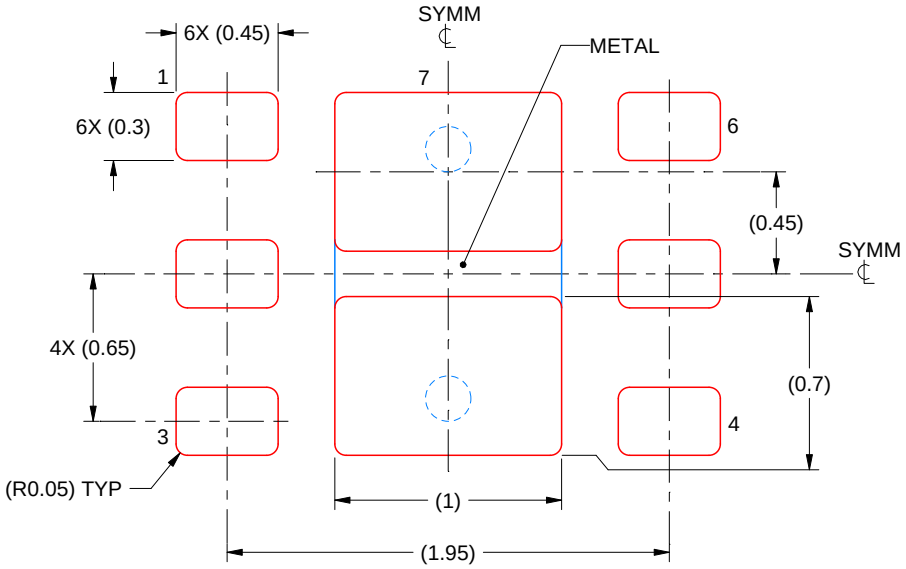


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



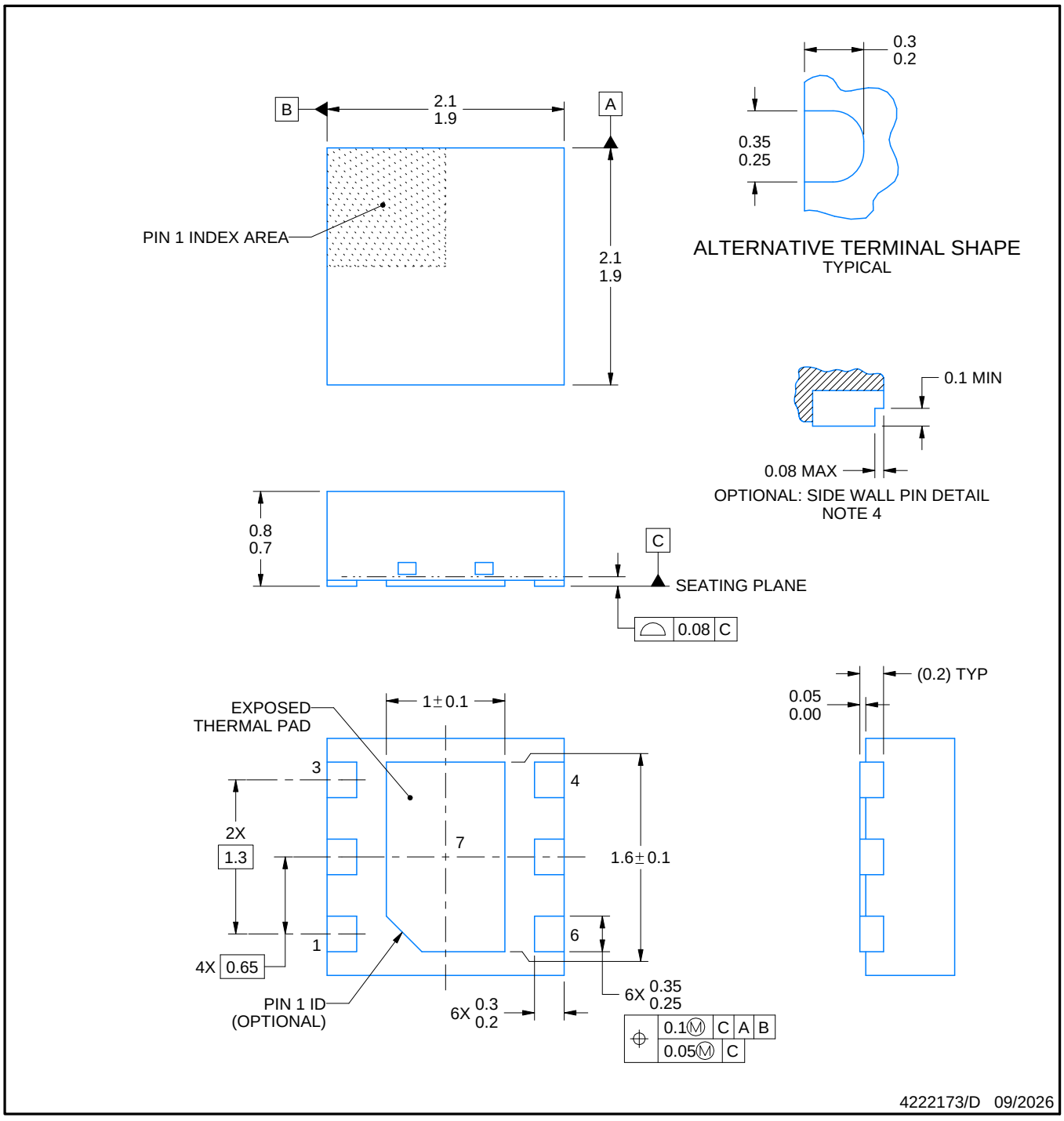
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

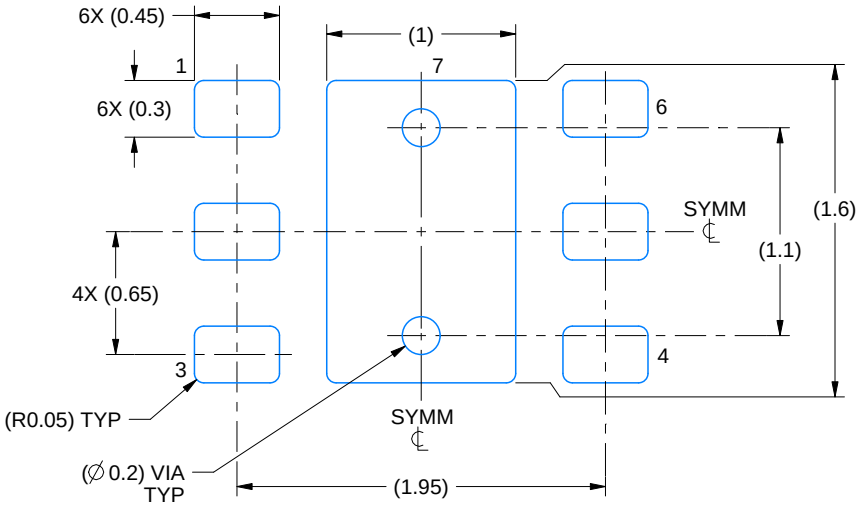
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

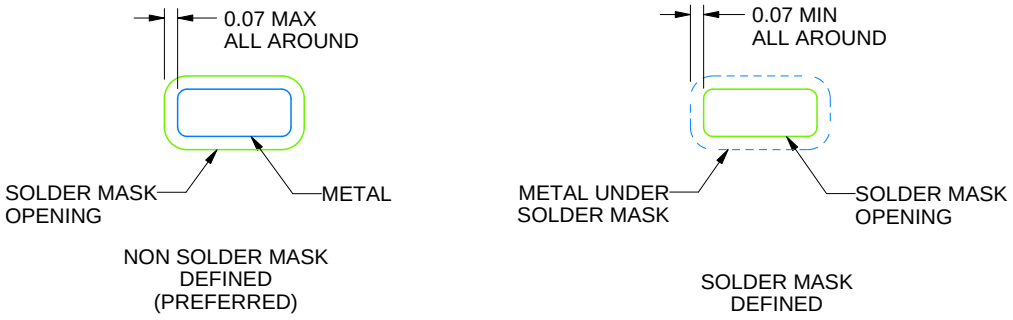


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

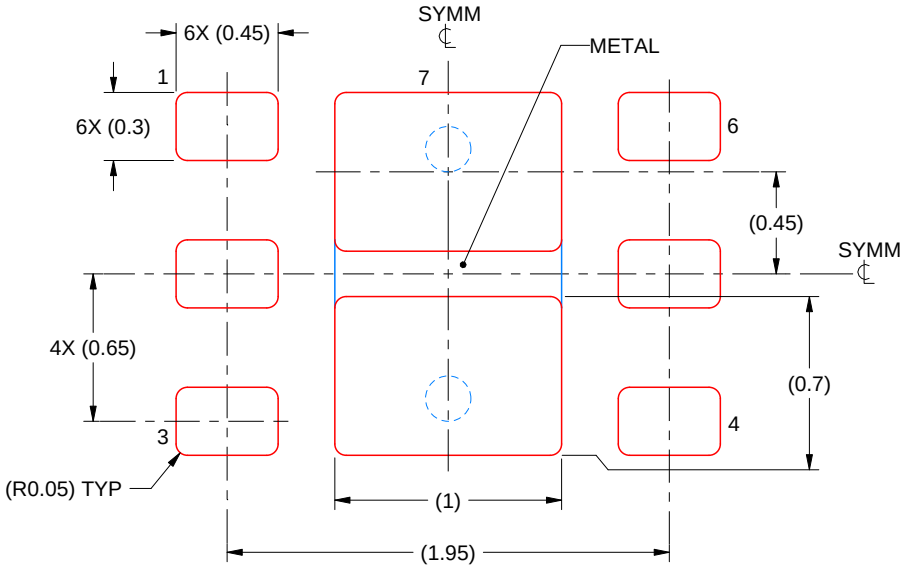


SOLDER MASK DETAILS

4222173/D 09/2026

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/D 09/2026

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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