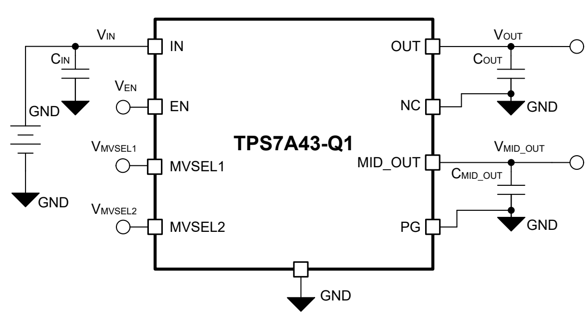
TPS7A43-Q1 Automotive 50mA, 85V, Ultra-Low I_Q, Low-Dropout Voltage Regulator With Power-Good, Precision Enable, and Selectable Mid-Output Rail

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature Grade 1: −40°C to +125°C, T_A
  - Junction temperature: −40°C to +150°C, T_J
- Wide input voltage range: 4V to 85V
  - Supports direct connection to 48V, 24V, or 12V automotive battery
- Wide output voltage range (V_{OUT}):
  - Adjustable: 1.24V to 14.5V
  - Fixed: 3.3V, 5.0V
- Selectable intermediate output (V_{MID_OUT}):
  - 10V, 12V, 15V
- Output current:
  - 50mA (shared between OUT and MID_OUT)
- ±0.8% V_{OUT} accuracy over full temperature range
- Ultra-low I_Q: 5.5µA (typical)
- Precision enable
- Power-good (PG) output
- High PSRR at 100kHz:
  - 73dB (OUT)
  - 47dB (MID_OUT)
- Thermal shutdown and overcurrent protection
- Package:
  - 10-pin HVSSOP (DGQ) [$R_{\theta JA}$ = 51.5°C/W]

2 Applications

- Automotive body motors
- Zone and body domain controller
- Thermal management
- Car access and security systems
- HEV/EV battery-management system (BMS)



Typical Application Circuit

3 Description

The TPS7A43-Q1 is a wide input, low-dropout (LDO) linear voltage regulator with 4V to 85V input voltage range and very-low quiescent current. This device can support a wide range of input voltages and withstand line transient voltages up to 90V (200ms), making the device designed for direct connection to 48V, 24V, or 12V automotive battery. Ultra-low I_Q of 5.5µA typical, 9µA maximum helps meet stringent system requirements and extends battery life in battery-connected applications.

The TPS7A43-Q1 output (OUT) is available in both fixed and adjustable output versions, with regulation from 1.24V to 14.5V and ±0.8% accuracy across temperature. The device is intended for use in an array of automotive applications, including supply for always-on loads like microcontrollers and wake-up functionality for various ICs (for example, CAN). The device is an efficient option to provide power to critical components during system sleep conditions. The TPS7A43-Q1 also features a second intermediate output (MID_OUT) that can be set to 10V, 12V, or 15V using the MVSEL pins. MID_OUT can supply power for LIN or be used to bias amplifiers, minimizing system complexity by eliminating the need for additional regulators.

The TPS7A43-Q1 features a precision enable input that enables or disables the LDO at a fixed and accurate threshold voltage using a resistor divider from the input.

The power-good (PG) output is used to monitor the voltage at the feedback pin to indicate the status of the output voltage. The EN input and PG output can be used for sequencing multiple power sources in the system.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (2)
TPS7A43-Q1	DGQ (HVSSOP, 10)	3.0mm × 4.90mm

(1) For all available packages, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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4 Pin Configuration and Functions

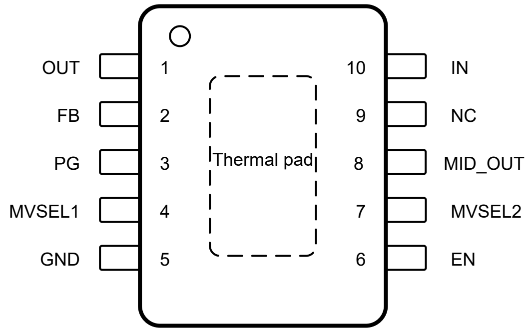

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Figure 4-1. DGQ Package (Adjustable), 10-Pin HVSSOP (Top View)

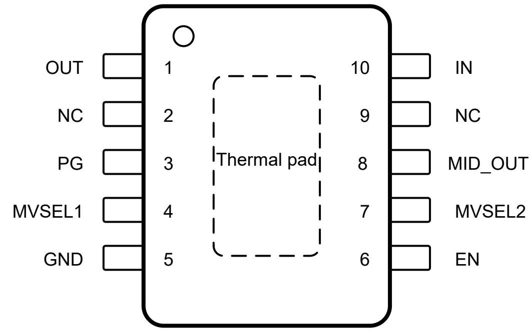

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Figure 4-2. DGQ Package (Fixed), 10-Pin HVSSOP (Top View)

Table 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DGQ (Adjustable)	DGQ (Fixed)		
EN	6	6	Input	Precision enable pin. Driving this pin higher than $V_{EN(HI)}$ enables the device. Driving this pin lower than $V_{EN(LOW)}$ disables the device. Under certain conditions, this pin can be left floating to enable the device; refer to the *Precision Enable* section for details. If this pin is tied to the IN pin, then the input voltage must not exceed 18V; see the *Recommended Operating Conditions* table.
FB	2	—	Input	For adjustable version only. Feedback pin. Input to the control-loop error amplifier for the (OUT) output, which is used to set the output voltage of the device with the use of external resistors. Refer to the *Adjustable Device Feedback Resistors* section for more details. This pin must not be left floating.
GND	5	5	—	Ground pin.
IN	10	10	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground; see the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
MID_OUT	8	8	Output	Regulated MID output pin. A capacitor is required from MID_OUT to ground for stability. Use the minimum recommended value or larger capacitor from MID_OUT to ground; see the*Recommended Operating Conditions* table and the*Input and Output Capacitor Requirements* section. Place the MID output capacitor as close to the MID_OUT and GND pins of the device as possible.
MVSEL1	4	4	Input	MID_OUT voltage-select pin. The MVSEL1 pin and MVSEL2 pin are used to set the MID_OUT voltage; see the *MID_OUT Voltage Setting* section for details on how to set the MID_OUT voltage using these pins. Do not float this pin, instead tie this pin to GND if not used to set V_{MID_OUT}.
MVSEL2	7	7	Input	MID_OUT voltage-select pin. The MVSEL2 pin and MVSEL1 pin are used to set the MID_OUT voltage; see the *MID_OUT Voltage Setting* section for details on how to set the MID_OUT voltage using these pins. Do not float this pin, instead tie this pin to GND if not used to set V_{MID_OUT}.
NC	9	9	—	No internal connection. This pin can be left floating or tied to the GND plane to improve thermal performance. If the application requires high voltage clearance between the IN and MID_OUT pins, this pin must be left floating.
NC	—	2	—	No internal connection. This pin can be left floating or tied to the GND plane to improve thermal performance.

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Table 4-1. Pin Functions (continued)

PIN			TYPE	DESCRIPTION
NAME	DGQ (Adjustable)	DGQ (Fixed)		
OUT	1	1	Output	Regulated output pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor from OUT to ground. Follow the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible.
PG	3	3	Output	Power-good pin. An open-drain output indicates when the output voltage reaches $V_{IT(PG,RISING)}$; see the *Recommended Operating Conditions* table. If not used, this pin can be left floating or tied to the GND plane to improve thermal performance.
Thermal pad	Pad	Pad	—	Exposed pad of the package. Connect this pad to ground or leave floating. Connect the thermal pad to a large-area GND plane for improved thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Voltage[(2)]	IN	–0.3	90[(3)]	V
	OUT (adjustable version)	–0.3	V_{MID} + 0.3[(4)]	
	OUT (fixed version)	–0.3	5.5	
	MID_OUT	–0.3	V_{IN} + 0.3[(5)]	
	FB	–0.3	5.5	
	EN	–0.3	20	
	MVSEL1	–0.3	20	
	MVSEL2	–0.3	20	
	PG	–0.3	20	
Current	Maximum output ($I_{OUT(max)}$)	Internally limited		A
	Maximum MID output ($I_{MID\_OUT(max)}$)	Internally limited		
Temperature	Operating junction, T_J	–50	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the absolute maximum ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional – this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages with respect to GND.
(3) Absolute maximum voltage, withstand 90V for 200ms.
(4) V_{MID_OUT} + 0.3V or 20V (whichever is smaller).
(5) V_{IN} + 0.3V or 20V (whichever is smaller).

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]	±2000	V
		Charged-device model (CDM), per AEC V Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	4		85	V
V_{MID_OUT}	MID output voltage	10		15	V
V_{OUT}	Output voltage (adjustable version)	1.24		$V_{MID\_OUT} - V_{DO(OUT)}$	V
V_{OUT}	Output voltage (fixed version)	1.25		5.5	V
I_{OUT}	Output current	0		$50 - I_{MID\_OUT}$	mA
I_{MID_OUT}	MID rail output current	0		50	mA
V_{MVSEL1}	MID voltage select input voltage 1	0		18	V
V_{MVSEL2}	MID voltage select input voltage 2	0		18	V
V_{EN}	Enable voltage	0		18	V
V_{PG} (1)	Power-good voltage	0		18	V
C_{IN} (2)	Input capacitor		0.1		µF
C_{OUT} (2)	Output capacitor	1	2.2	100	µF
C_{MID_OUT} (2) (3)	MID output capacitor	$3 \times C_{OUT}$			µF
T_A	Ambient temperature range	–40		125	°C
T_J	Operating junction temperature	–40		150	°C

(1) Select pullup resistor to limit PG pin sink current when PG output is driven low. See the *Power Good* section for details.
(2) The capacitance specified in the table is the nominal capacitor value. Assume 50% derating of listed values to arrive at effective capacitance.
(3) Maintain a ratio ≥3:1 between C_{MID_OUT} vs C_{OUT} for stability.

5.4 Thermal Information

THERMAL METRIC(1)		TPS7A43-Q1 HVSSOP (DGQ) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Electrical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = $V_{OUT(nom)}$ + 1.5V or 4V, whichever is greater, FB tied to OUT (adjustable version only), I_{OUT} = 1mA, I_{MID_OUT} = 0mA, V_{EN} = 2V, V_{MVSEL1} = 0.9V, V_{MVSEL2} = 0.9V, C_{IN} = 1µF, C_{MID_OUT} = 4.7µF, and C_{OUT} = 1µF (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage accuracy	Adjustable version, V_{OUT} = V_{FB}		1.23	1.24	1.25	V
ΔV_{OUT}		Fixed output version	T_J = 25°C	–0.5		0.5	%
			T_J = –40°C to +125°C	–0.75		0.75	
			T_J = –40°C to +150°C	–0.8		0.8	
V_{FB}	Feedback voltage	Adjustable version only			1.24		V
$\Delta V_{OUT(\Delta VIN)}$	Line regulation(1)	($V_{OUT(nom)}$ + 1V or 4V) ≤ V_{IN} ≤ 85V		–0.05		0.05	%
		$V_{MID\_OUT(nom)}$ + 1.5V ≤ V_{IN} ≤ 85V		–0.05		0.05	
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	1mA ≤ I_{OUT} ≤ 50mA, I_{MID_OUT} = 0mA		–0.15		0.10	%
ΔV_{MID_OUT}	MID output voltage accuracy	V_{IN} = V_{MID_OUT} + 1.5V	V_{MVSEL1} ≤ $V_{MVSEL1(LOW)}$, V_{MVSEL2} ≤ $V_{MVSEL2(LOW)}$	14.4	15	15.6	V
			V_{MVSEL1} ≤ $V_{MVSEL1(LOW)}$ or V_{MVSEL1} ≥ $V_{MVSEL1(HIGH)}$, V_{MVSEL2} ≥ $V_{MVSEL2(HIGH)}$	11.5	12	12.5	
			V_{MVSEL1} ≥ $V_{MVSEL1(HIGH)}$, V_{MVSEL2} ≤ $V_{MVSEL2(LOW)}$	9.6	10	10.4	
$\Delta V_{MID\_OUT(\Delta VIN)}$	Line regulation of MID output(1)	($V_{MID\_OUT(nom)}$) + 1.5V ≤ V_{IN} ≤ 85V, I_{MID_OUT} = 1mA, I_{OUT} = 0mA		–0.1		0.1	%
$\Delta V_{MID\_OUT(\Delta IOUT)}$	Load regulation of MID output	1mA ≤ I_{MID_OUT} ≤ 50mA V_{IN} = V_{MID_OUT} + 1.5V I_{OUT} = 0mA		–0.2		0.1	%
$V_{UVLO(RISING)}$	UVLO threshold rising	V_{IN} rising, I_{OUT} = 1mA		2	2.2	2.3	V
$V_{DO(OUT)}$	Dropout voltage of V_{IN} to V_{OUT} (2)	I_{OUT} = 50mA				800	mV
$V_{DO(OUT)}$	Dropout voltage of V_{MID_OUT} to V_{OUT} (2)	I_{OUT} = 50mA				200	mV
$V_{DO(MID\_OUT)}$	Dropout voltage of V_{IN} to V_{MID_OUT} (3)	I_{MID_OUT} = 50mA				600	mV
$I_{CL(OUT)}$	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$		100	125	145	mA
$I_{CL(MID\_OUT)}$	MID output current limit	V_{OUT} = 0.9 × $V_{MID\_OUT(nom)}$, V_{IN} = V_{MID_OUT} + 1.5V		118	145	165	mA
I_{GND}	Ground pin current	I_{OUT} = I_{MID_OUT} = 0mA, V_{IN} = V_{MID_OUT} + 1.5V	T_J = 25°C		5.5	7	µA
			T_J = –40°C to +125°C			9	
			T_J = –40°C to +150°C			12	
		I_{OUT} = 50mA, V_{IN} = V_{MID_OUT} + 1.5V			185		
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ $V_{EN(LOW)}$, V_{IN} = $V_{MID\_OUT(nom)}$ + 1.5V I_{OUT} = I_{MID_OUT} = 0mA	T_J = –40°C to +85°C		710	1600	nA
			T_J = –40°C to +125°C			2100	
			T_J = –40°C to +150°C			2500	
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ $V_{EN(LOW)}$, V_{IN} =85V I_{OUT} = I_{MID_OUT} = 0mA	T_J = –40°C to +85°C		710	1900	nA
			T_J = –40°C to +125°C			2500	
			T_J = –40°C to +150°C			2700	
I_{FB}	FB pin current				10		nA
I_{MVSEL1}	MVSEL1 pin current	V_{MVSEL1} = 18V			10		nA
I_{MVSEL2}	MVSEL2 pin current	V_{MVSEL2} = 18V			10		nA

specified at T_J = –40°C to +150°C, V_{IN} = $V_{OUT(nom)}$ + 1.5V or 4V, whichever is greater, FB tied to OUT (adjustable version only), I_{OUT} = 1mA, I_{MID_OUT} = 0mA, V_{EN} = 2V, V_{MVSEL1} = 0.9V, V_{MVSEL2} = 0.9V, C_{IN} = 1µF, C_{MID_OUT} = 4.7µF, and C_{OUT} = 1µF (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{EN}	EN pin current	V_{EN} = 18V			10		nA
$V_{MVSEL1(HIGH)}$	MVSEL1 pin high-level input voltage			0.9			V
$V_{MVSEL1(LOW)}$	MVSEL1 pin low-level input voltage					0.3	V
$V_{MVSEL2(HIGH)}$	MVSEL2 pin high-level input voltage			0.9			V
$V_{MVSEL2(LOW)}$	MVSEL2 pin low-level input voltage					0.3	V
$V_{EN(HI)}$	Enable rising threshold	Device enabled		1.15	1.24	1.35	V
$V_{EN(LOW)}$	Enable falling threshold	Device disabled		1.11	1.19	1.28	V
$V_{EN(HYST)}$	Enable pin hysteresis				50		mV
$V_{IT(PG,RISING)}$	PG pin threshold rising	R_{PULLUP} = 10kΩ, V_{OUT} rising, $V_{IN} \geq V_{UVLO(RISING)}$		88	93	96.5	$\%V_{OUT}$
$V_{HYS(PG)}$	PG pin hysteresis	R_{PULLUP} = 10kΩ, V_{OUT} falling, $V_{IN} \geq V_{UVLO(RISING)}$			3		$\%V_{OUT}$
$V_{IT(PG,FALLING)}$	PG pin threshold falling	R_{PULLUP} = 10kΩ, V_{OUT} falling, $V_{IN} \geq V_{UVLO(RISING)}$		84	90	94.5	$\%V_{OUT}$
$V_{OL(PG)}$	PG pin low level output voltage	$V_{OUT} < V_{IT(PG,FALLING)}$, $I_{PG\text{-}SINK}$ = 500µA				0.4	V
$I_{LKG(PG)}$	PG pin leakage current	$V_{OUT} > V_{IT(PG,RISING)}$, V_{PG} = 18V	T_J = –40°C to +125°C		5	130	nA
			T_J = –40°C to +150°C			190	nA
$PSRR_{(OUT)}$	Power-supply rejection ratio of OUT rail	I_{OUT} = 20mA	f = 10Hz		76		dB
			f = 100Hz		67		dB
			f = 1kHz		82		dB
			f = 100kHz		73		dB
$PSRR_{(MID\_OUT)}$	Power-supply rejection ratio of MID_OUT rail	I_{MID_OUT} = 20mA	f = 10Hz		61		dB
			f = 100Hz		64		dB
			f = 1kHz		55		dB
			f = 100kHz		47		dB
V_n	Output noise voltage	BW = 10Hz to 100kHz, V_{OUT} = 1.24V			124		μV_{RMS}
$T_{SD(shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing			170		°C
$T_{SD(reset)}$	Thermal shutdown reset temperature	Reset, temperature decreasing			155		°C
t_{TSD}	Thermal shutdown response time				60		µs
$t_{TSD(reset)}$	Thermal shutdown reset time				5		ms

(1) Line regulation from input of the LDO to the final output of the LDO.
(2) V_{DO} is measured with V_{IN} = 0.95 × $V_{OUT(nom)}$ for fixed output voltage versions. V_{DO} is not measured for fixed output voltage versions when $V_{OUT} \leq$ 3.1V. For the adjustable output device, V_{DO} is measured with V_{FB} = 0.95 × $V_{FB(nom)}$.
(3) $V_{DO(MID\_OUT)}$ is measured with V_{IN} = 0.95 × $V_{MID\_OUT(nom)}$ for Mid output voltages.

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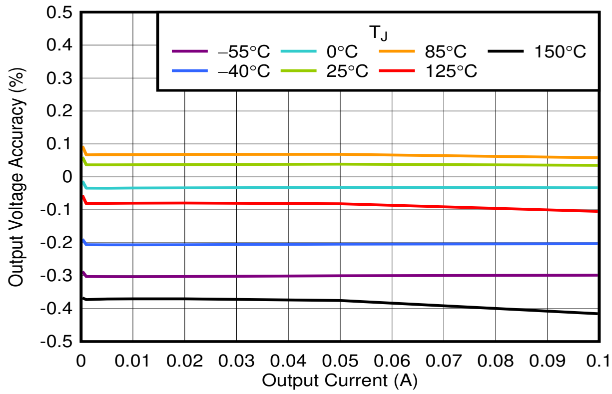
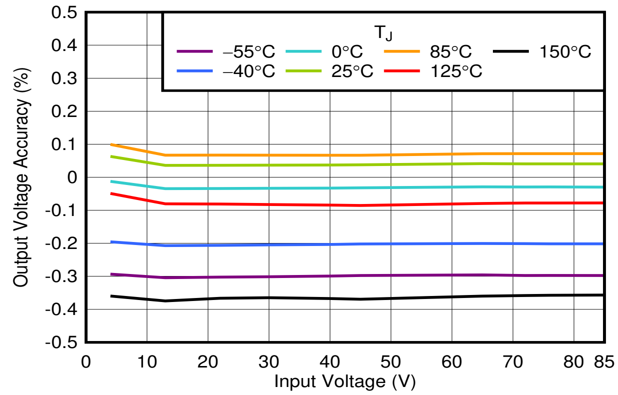
5.6 Typical Characteristics

at operating temperature T_J = 25°C, I_{OUT} = 1mA, I_{MID_OUT} = 0mA, V_{EN} = 2V, V_{MVSEL1} = 0.9V, V_{MVSEL2} = 0.9V, C_{IN} = 1µF, C_{MID_OUT} = 4.7µF, C_{OUT} = 1µF, and V_{IN} = V_{MID_OUT} + 1.5V (unless otherwise noted); typical values are at T_J = 25°C



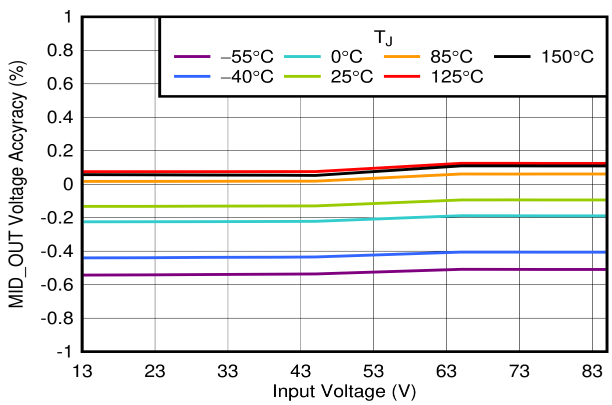
V_{OUT} = 1.24V (adjustable)

Figure 5-1. V_{OUT} Accuracy vs I_{OUT}



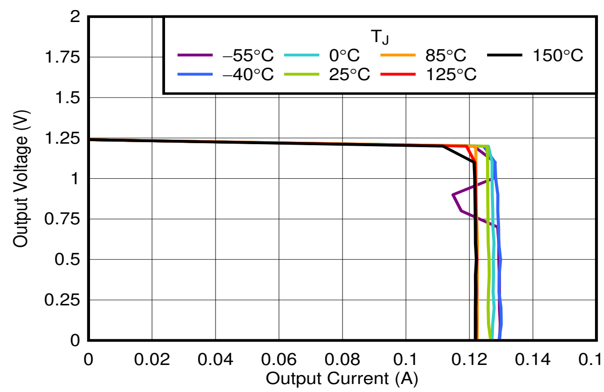
V_{OUT} = 1.24V (adjustable)

Figure 5-2. V_{OUT} Accuracy vs V_{IN}



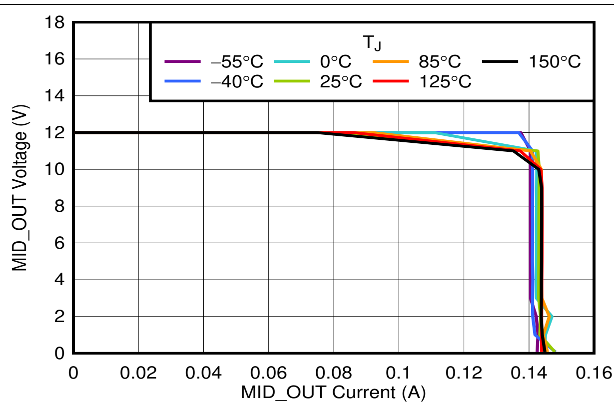
V_{MID_OUT} = 12V

Figure 5-3. V_{MID_OUT} Accuracy vs V_{IN}



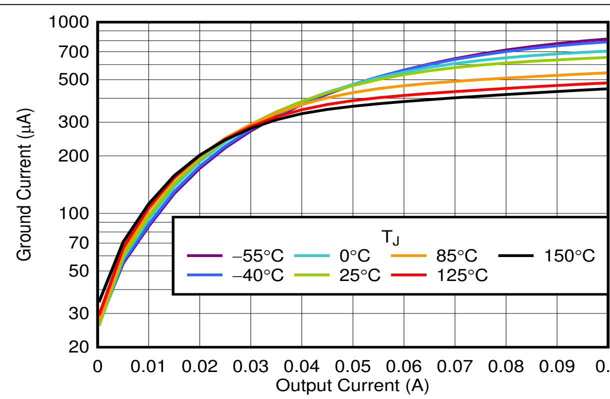
V_{OUT} = 1.24V (adjustable)

Figure 5-4. V_{OUT} vs I_{OUT}



V_{MID_OUT} = 12V

Figure 5-5. V_{MID_OUT} vs I_{MID_OUT}

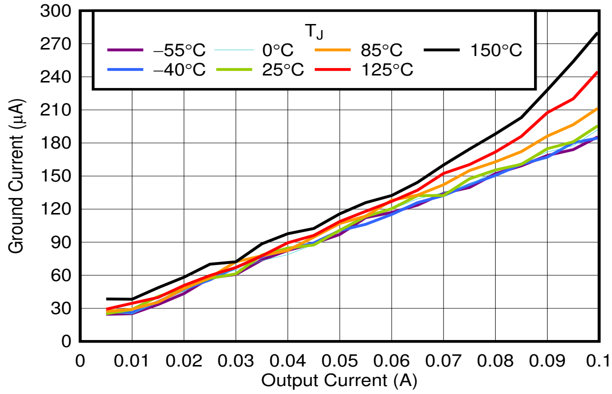


V_{IN} = 11V, V_{OUT} = 1.24V (adjustable)

Figure 5-6. I_{GND} vs I_{OUT} (MID_OUT in Dropout)

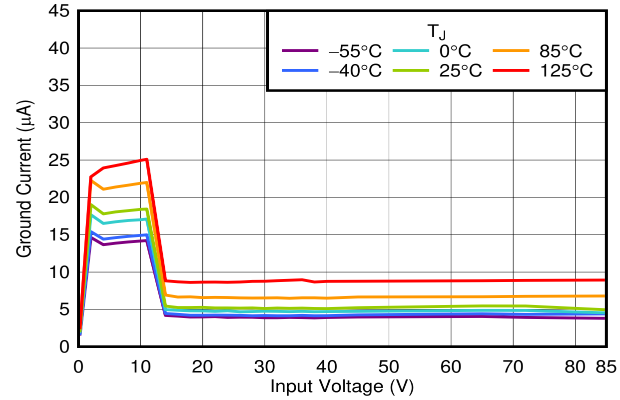
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1mA, I_{MID_OUT} = 0mA, V_{EN} = 2V, V_{MVSEL1} = 0.9V, V_{MVSEL2} = 0.9V, C_{IN} = 1µF, C_{MID_OUT} = 4.7µF, C_{OUT} = 1µF, and V_{IN} = V_{MID_OUT} + 1.5V (unless otherwise noted); typical values are at T_J = 25°C



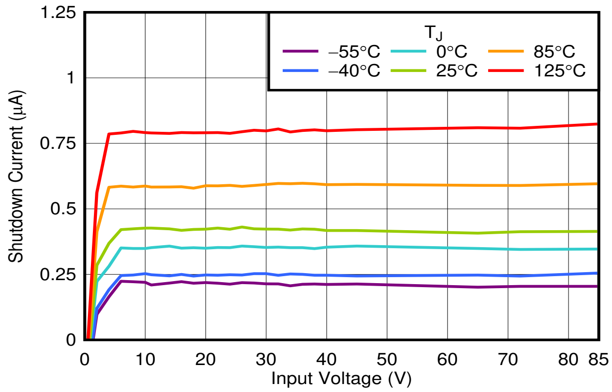
V_{IN} = 16.5V, V_{MID_OUT} = 15V, V_{MVSEL1} = V_{MVSEL2} = 0V, V_{OUT} = 1.24V (adjustable)

Figure 5-7. I_{GND} vs I_{OUT}



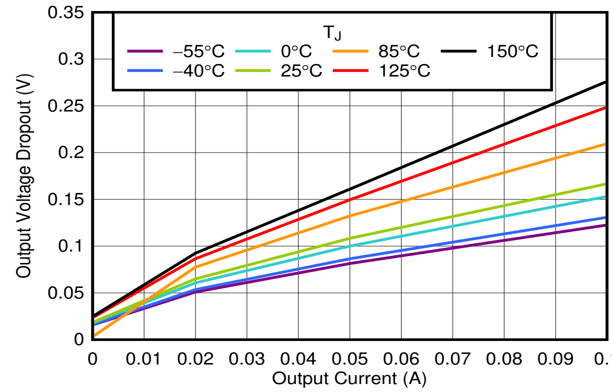
I_{OUT} = 0mA

Figure 5-8. I_{GND} vs V_{IN}



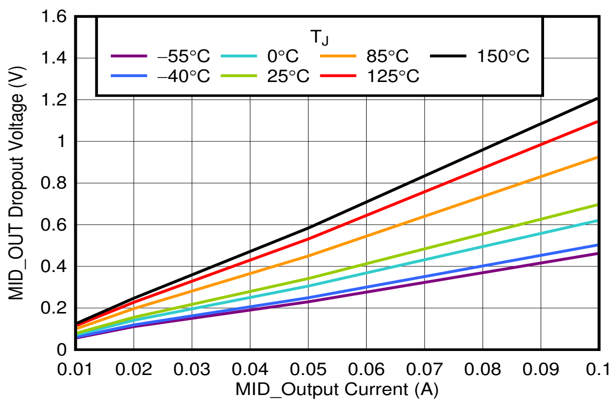
V_{EN} = 1V

Figure 5-9. $I_{SHUTDOWN}$ vs V_{IN}



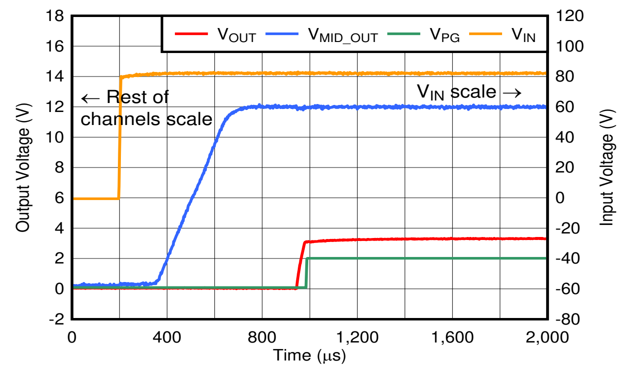
V_{OUT} = 1.24V (adjustable)

Figure 5-10. $V_{DO(OUT)}$ vs I_{OUT}



V_{MID_OUT} = 15V, V_{MVSEL1} = V_{MVSEL2} = 0V, I_{OUT} = 0mA

Figure 5-11. $V_{DO(MID\_OUT)}$ vs I_{MID_OUT}



C_{IN} = 0µF, V_{IN} ramp rate = 10V/µs, V_{OUT} = 3.3V, I_{OUT} = 10mA

Figure 5-12. Fast Start-Up

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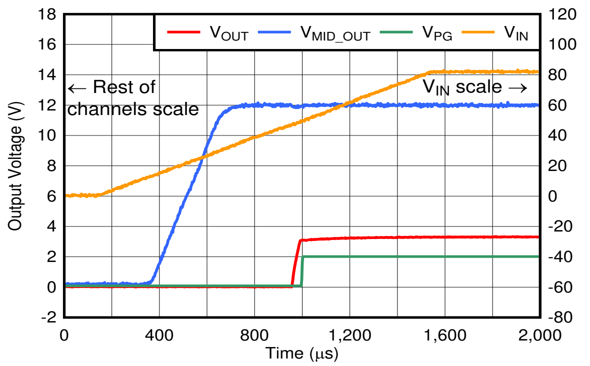
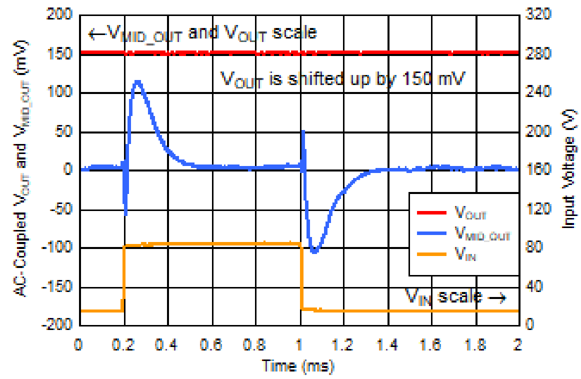
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1mA, I_{MID_OUT} = 0mA, V_{EN} = 2V, V_{MVSEL1} = 0.9V, V_{MVSEL2} = 0.9V, C_{IN} = 1µF, C_{MID_OUT} = 4.7µF, C_{OUT} = 1µF, and V_{IN} = V_{MID_OUT} + 1.5V (unless otherwise noted); typical values are at T_J = 25°C



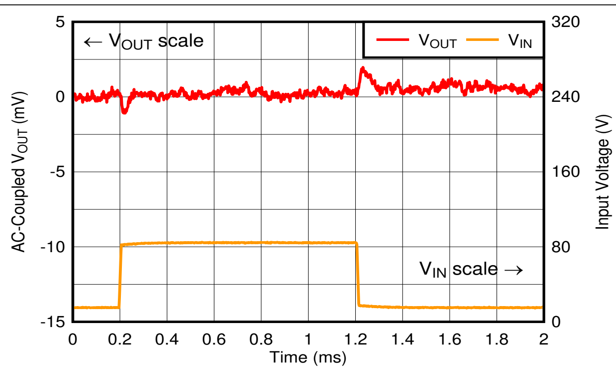
C_{IN} = 0µF, V_{IN} ramp rate = 45V/ms, V_{OUT} = 3.3V, I_{OUT} = 10mA

Figure 5-13. Slow Start-Up



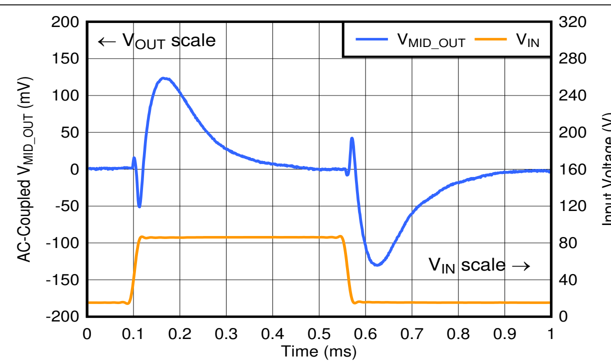
V_{IN} = 15V to 85V, V_{IN} ramp rate = 10V/µs, V_{OUT} = 3.3V, I_{OUT} = 50mA

Figure 5-14. Line Transient



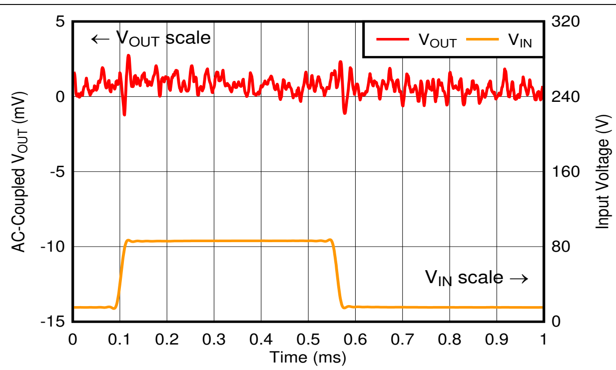
V_{IN} = 15V to 85V, V_{IN} ramp rate = 10V/µs, V_{OUT} = 3.3V, I_{OUT} = 10mA

Figure 5-15. Line Transient



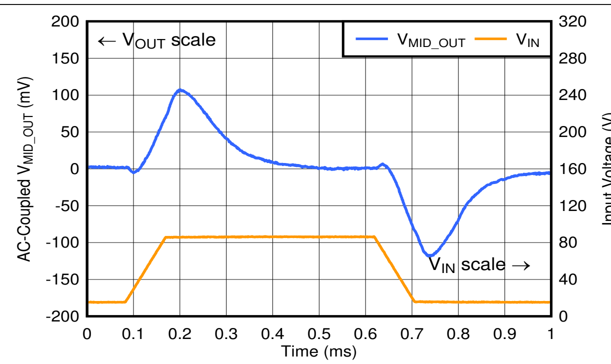
V_{IN} = 15V to 85V, V_{IN} ramp rate = 10V/µs, V_{OUT} = 3.3V, I_{OUT} = 50mA

Figure 5-16. Line Transient



V_{IN} = 15V to 85V, V_{IN} ramp rate = 10V/µs, V_{OUT} = 3.3V, I_{OUT} = 50mA

Figure 5-17. Line Transient

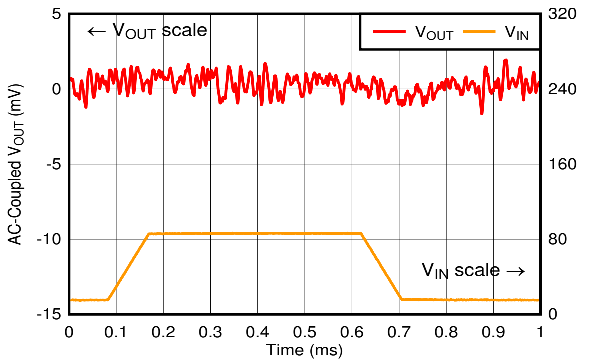


V_{IN} = 4V to 85V, V_{IN} ramp rate = 1V/µs, V_{OUT} = 3.3V, I_{OUT} = 50mA

Figure 5-18. Line Transient (V_{MID_OUT} in Dropout)

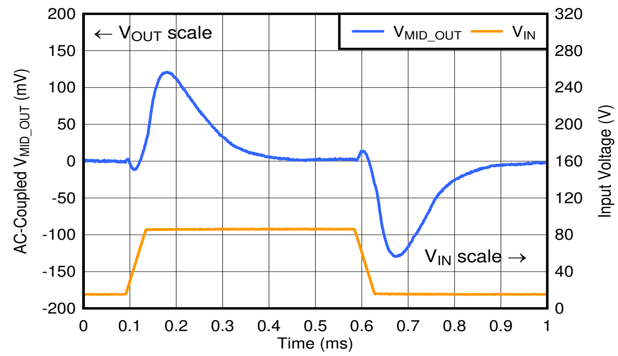
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1mA, I_{MID_OUT} = 0mA, V_{EN} = 2V, V_{MVSEL1} = 0.9V, V_{MVSEL2} = 0.9V, C_{IN} = 1µF, C_{MID_OUT} = 4.7µF, C_{OUT} = 1µF, and V_{IN} = V_{MID_OUT} + 1.5V (unless otherwise noted); typical values are at T_J = 25°C



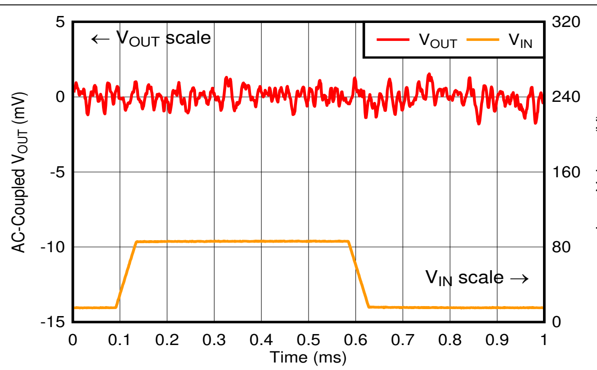
V_{IN} = 4V to 85V, V_{IN} ramp rate = 1V/µs, V_{OUT} = 3.3V, I_{OUT} = 50mA

Figure 5-19. Line Transient (V_{MID_OUT} in Dropout)



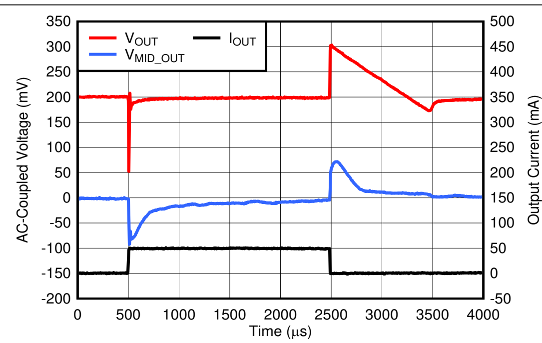
V_{IN} = 4V to 85V, V_{IN} ramp rate = 5V/µs, V_{OUT} = 3.3V, I_{OUT} = 50mA

Figure 5-20. Line Transient (V_{MID_OUT} in Dropout)



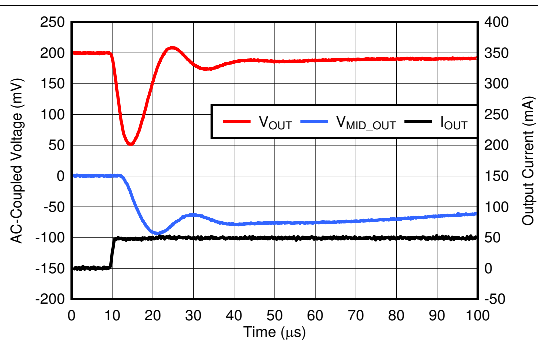
V_{IN} = 4V to 85V, V_{IN} ramp rate = 5V/µs, V_{OUT} = 3.3V, I_{OUT} = 50mA

Figure 5-21. Line Transient (V_{MID_OUT} in Dropout)



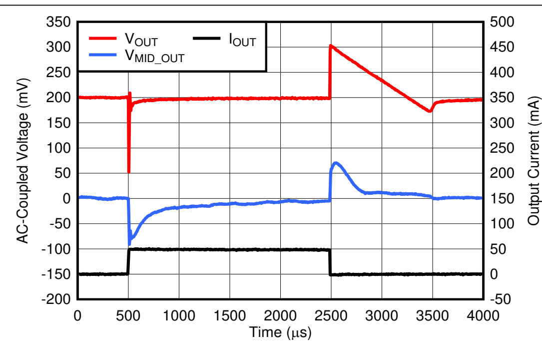
V_{IN} = 65V, V_{OUT} = 3.3V, I_{OUT} = 0mA to 50mA to 0mA, I_{OUT} slew rate = 1A/µs

Figure 5-22. Load Transient



V_{IN} = 65V, V_{OUT} = 3.3V, I_{OUT} = 0mA to 50mA to 0mA, I_{OUT} slew rate = 1A/µs

Figure 5-23. Load Transient (Rising Edge)

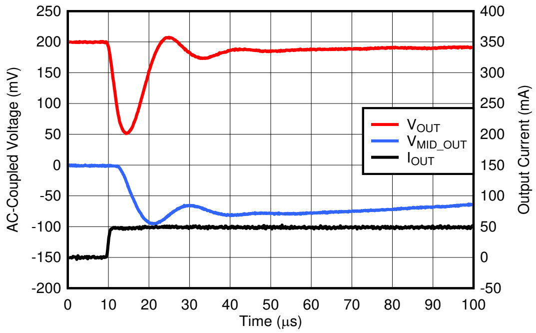


V_{IN} = 65V, V_{OUT} = 3.3V, I_{OUT} = 1mA to 50mA to 1mA, I_{OUT} slew rate = 1A/µs

Figure 5-24. Load Transient

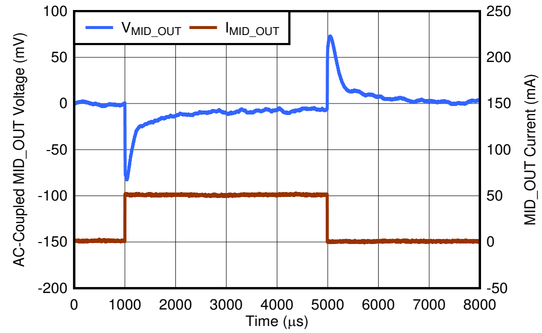
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1mA, I_{MID_OUT} = 0mA, V_{EN} = 2V, V_{MVSEL1} = 0.9V, V_{MVSEL2} = 0.9V, C_{IN} = 1µF, C_{MID_OUT} = 4.7µF, C_{OUT} = 1µF, and V_{IN} = V_{MID_OUT} + 1.5V (unless otherwise noted); typical values are at T_J = 25°C



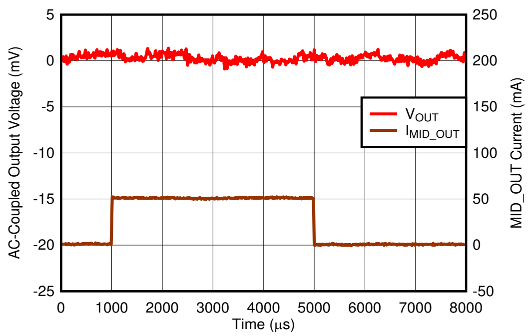
V_{IN} = 65V, V_{OUT} = 3.3V, I_{OUT} = 1mA to 50mA to 1mA, I_{OUT} slew rate = 1A/µs

Figure 5-25. Load Transient (Rising Edge)



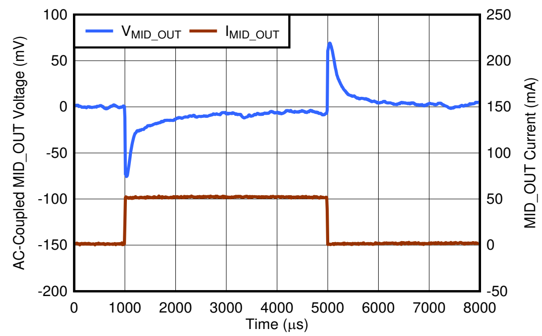
V_{IN} = 65V, V_{MID_OUT} = 12V, I_{MID_OUT} = 0mA to 50mA to 0mA, I_{MID_OUT} slew rate = 1A/µs, I_{OUT} = 0mA

Figure 5-26. Load Transient (MID_OUT)



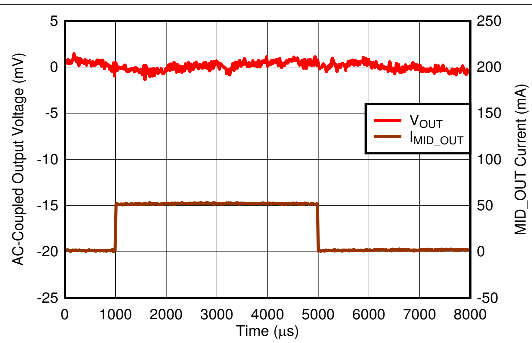
V_{IN} = 65V, V_{OUT} = 3.3V, I_{MID_OUT} = 0mA to 50mA to 0mA, I_{MID_OUT} slew rate = 1A/µs, I_{OUT} = 0mA

Figure 5-27. Load Transient (MID_OUT)



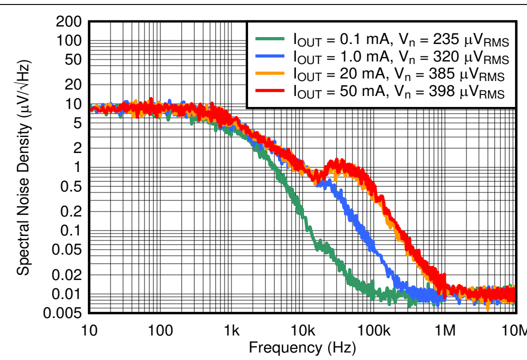
V_{IN} = 65V, V_{MID_OUT} = 12V, I_{MID_OUT} = 1mA to 50mA to 1mA, I_{MID_OUT} slew rate = 1A/µs, I_{OUT} = 0mA

Figure 5-28. Load Transient (MID_OUT)



V_{IN} = 65V, V_{OUT} = 3.3V, I_{MID_OUT} = 1mA to 50mA to 1mA, I_{MID_OUT} slew rate = 1A/µs, I_{OUT} = 0mA

Figure 5-29. Load Transient (MID_OUT)

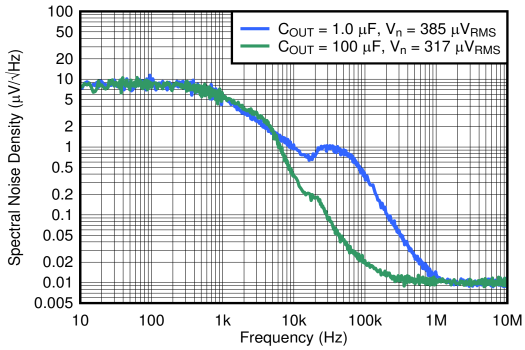


V_{IN} = 13V, V_{OUT} = 3.3V, V_{RMS} bandwidth = 10Hz to 100kHz

Figure 5-30. Spectral Noise Density vs Frequency and I_{OUT}

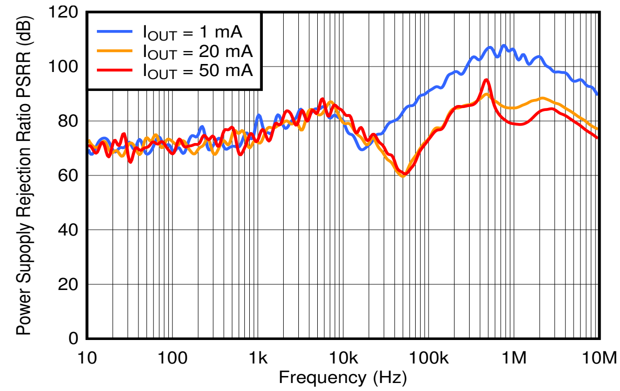
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1mA, I_{MID_OUT} = 0mA, V_{EN} = 2V, V_{MVSEL1} = 0.9V, V_{MVSEL2} = 0.9V, C_{IN} = 1μF, C_{MID_OUT} = 4.7μF, C_{OUT} = 1μF, and V_{IN} = V_{MID_OUT} + 1.5V (unless otherwise noted); typical values are at T_J = 25°C



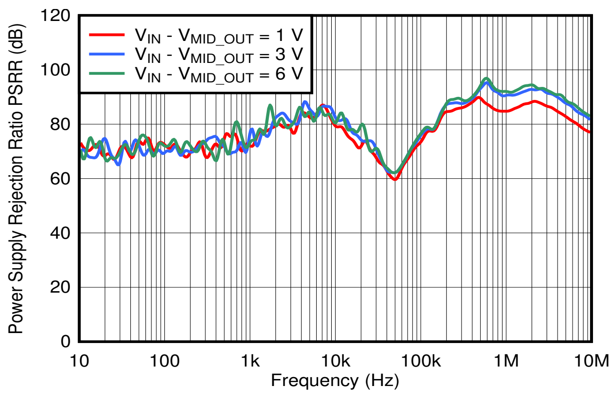
V_{IN} = 13V, V_{OUT} = 3.3V, I_{OUT} = 20mA, V_{RMS} bandwidth = 10Hz to 100kHz

Figure 5-31. Spectral Noise Density vs Frequency and C_{OUT}



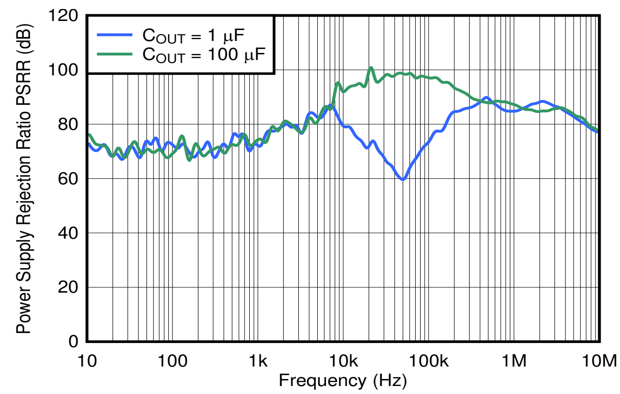
V_{IN} = 13V, C_{IN} = 0μF, V_{OUT} = 3.3V

Figure 5-32. OUT PSRR vs Frequency and I_{OUT}



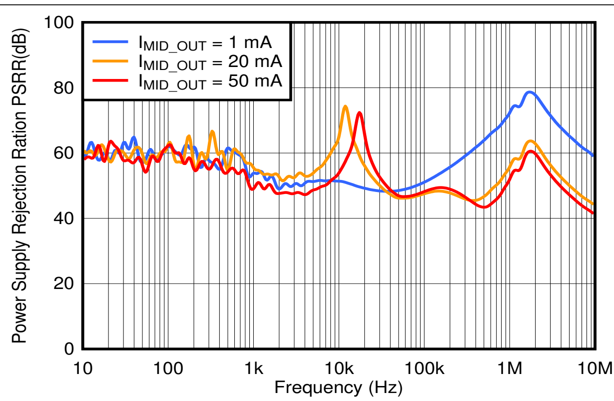
C_{IN} = 0μF, V_{OUT} = 3.3V, I_{OUT} = 20mA

Figure 5-33. OUT PSRR vs Frequency and V_{IN}



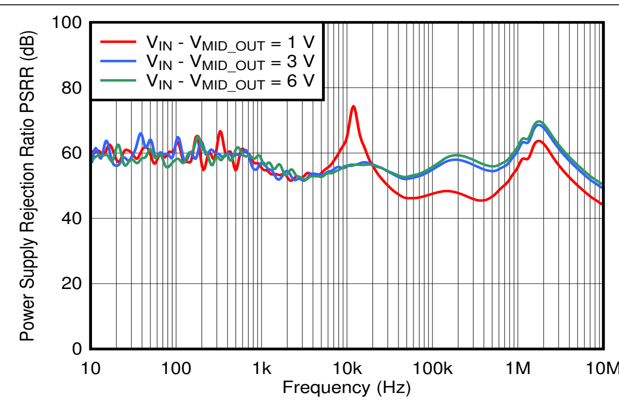
V_{IN} = 13V, C_{IN} = 0μF, V_{OUT} = 3.3V, I_{OUT} = 20mA

Figure 5-34. OUT PSRR vs Frequency and C_{OUT}



V_{IN} = 13V, C_{IN} = 0μF, V_{OUT} = 3.3V, I_{OUT} = 0mA

Figure 5-35. MID_OUT PSRR vs Frequency and I_{MID_OUT}



C_{IN} = 0μF, V_{OUT} = 3.3V, I_{MID_OUT} = 20mA, I_{OUT} = 0mA

Figure 5-36. MID_OUT PSRR vs Frequency and V_{IN}

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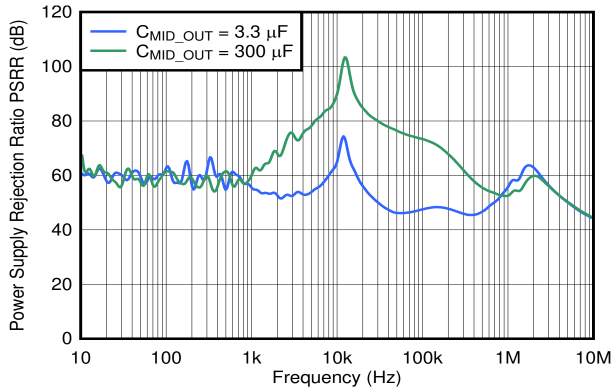
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1mA, I_{MID_OUT} = 0mA, V_{EN} = 2V, V_{MVSEL1} = 0.9V, V_{MVSEL2} = 0.9V, C_{IN} = 1µF, C_{MID_OUT} = 4.7µF, C_{OUT} = 1µF, and V_{IN} = V_{MID_OUT} + 1.5V (unless otherwise noted); typical values are at T_J = 25°C



V_{IN} = 13V, C_{IN} = 0µF, V_{OUT} = 3.3V, I_{MID_OUT} = 20mA, I_{OUT} = 0mA

Figure 5-37. MID_OUT PSRR vs Frequency and C_{MID_OUT}

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6 Detailed Description

6.1 Overview

The TPS7A43-Q1 is an 85V, low quiescent current, low-dropout (LDO) linear regulator. The very low I_Q performance makes the device an excellent choice for battery-powered use cases like 48V automotive applications that are expected to meet increasingly stringent standby-power standards.

The high accuracy over temperature and power-good indication make this device a good choice to meet a broad range of power requirements for microcontrollers and other sensitive loads. The device features a selectable MID_OUT voltage pin which can be used to provide a secondary voltage rail, for example to power LIN or for amplifier bias.

For increased robustness, the TPS7A43-Q1 also incorporates precision enable, output current limit, active discharge, and thermal shutdown protection.

6.2 Functional Block Diagrams

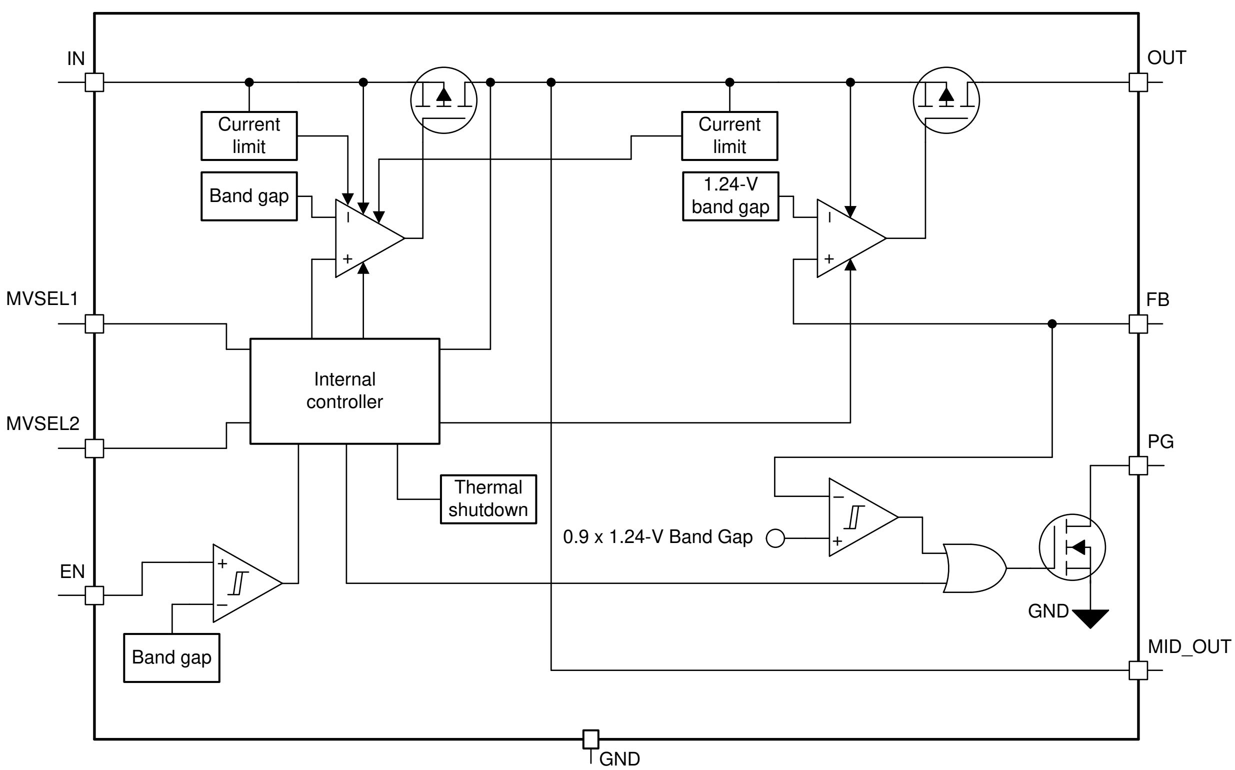

Figure 6-1. Adjustable Version

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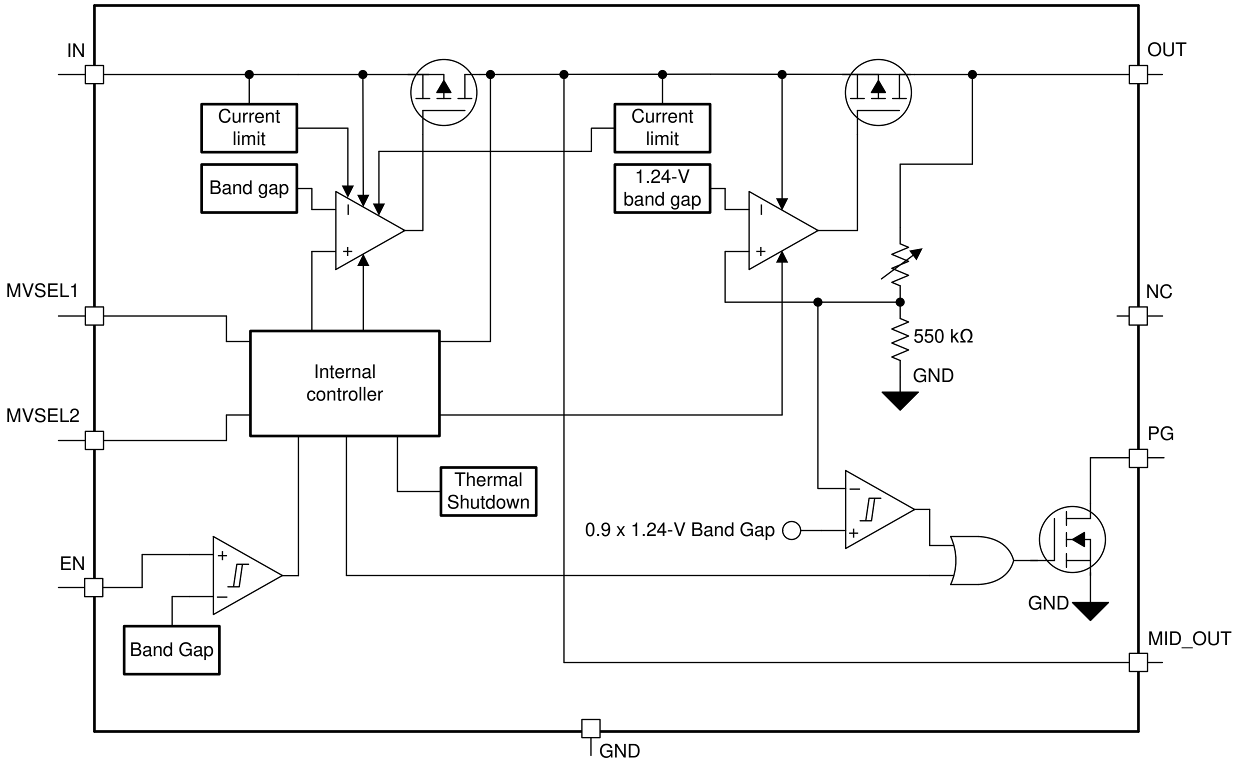

Figure 6-2. Fixed Version

6.3 Feature Description

6.3.1 MID_OUT Voltage Selection

The TPS7A43-Q1 features a MID_OUT voltage pin that provides a secondary output voltage supply in addition to the OUT pin, which is the main output voltage supply. The MID_OUT voltage is set using the MVSEL1 and MVSEL2 pins; see the *MID_OUT Voltage Setting* section for details.

While the MID_OUT rail provides benefits to various applications, the TPS7A43-Q1 can also be used as a single-channel output regulator if desired (only OUT). See the *Use Without MID_OUT* section for more details.

6.3.2 Precision Enable

The TPS7A43-Q1 features a precision enable circuit. The enable pin (EN) is active high. Thus, enable the device by forcing the voltage of the enable pin to exceed the $V_{EN(HI)}$ voltage, and turn off the device by forcing the voltage of the enable pin to drop below the $V_{EN(LOW)}$ voltage; see the *Electrical Characteristics* table.

EN is pulled high by a weak current source (see the *Electrical Characteristics* table). Therefore, EN can be left floating to enable the device. However, care must be taken if floating EN functionality is used, as board-level leakage on the order of tens of nanoamperes can cause the EN pin to be pulled low when EN is left floating.

If this pin is tied to the IN pin, the input voltage must not exceed 18V; see the *Recommended Operating Conditions* table. As shown in Figure 6-3, an external resistor divider circuit can be used to enable the device using the input voltage.

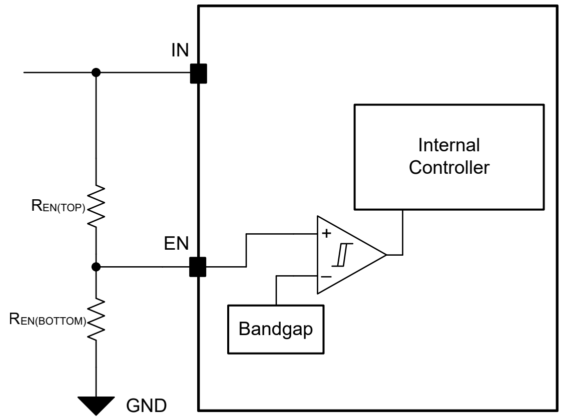

Figure 6-3. Enable the Device Using the Input Voltage

The $V_{EN(HI)}$ (maximum) and $V_{EN(LOW)}$ (minimum) thresholds along with the application input voltage can be used to set the $R_{EN(TOP)}$ to $R_{EN(BOTTOM)}$ resistor divider ratio. See the *Detailed Design Procedure* section for an example. The values of the $R_{EN(BOTTOM)}$ and $R_{EN(TOP)}$ resistors can also be optimized to minimize the leakage current through the divider.

6.3.3 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

6.3.4 Current Limit

The device has internal current limit circuits for both MID_OUT and OUT rails. These circuits protect the regulator during high-current load transient faults or shorting events on either rails. Both current limit circuits are brick-wall schemes with $I_{CL(MID\_OUT)}$ being higher than $I_{CL(OUT)}$. In a high-current load transient fault, the brick-wall scheme limits the output current to the respective current limit ($I_{CL(MID\_OUT)}$ or $I_{CL(OUT)}$), both of which are listed in the *Electrical Characteristics* table.

When the device is in either current limit, the output voltages are not regulated. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in either current limit, the corresponding pass transistor dissipates power. For instance, when the OUT rail is in current limit, the power dissipation can be calculated as [(V_{IN} – V_{OUT}) × $I_{CL(OUT)}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the faulty output current condition continues, the device cycles between current limit and thermal shutdown with approximately a 5ms time constant. For more information on current limits, see the *Know Your Limits* application note.

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Figure 6-4 shows a diagram of the current limit.

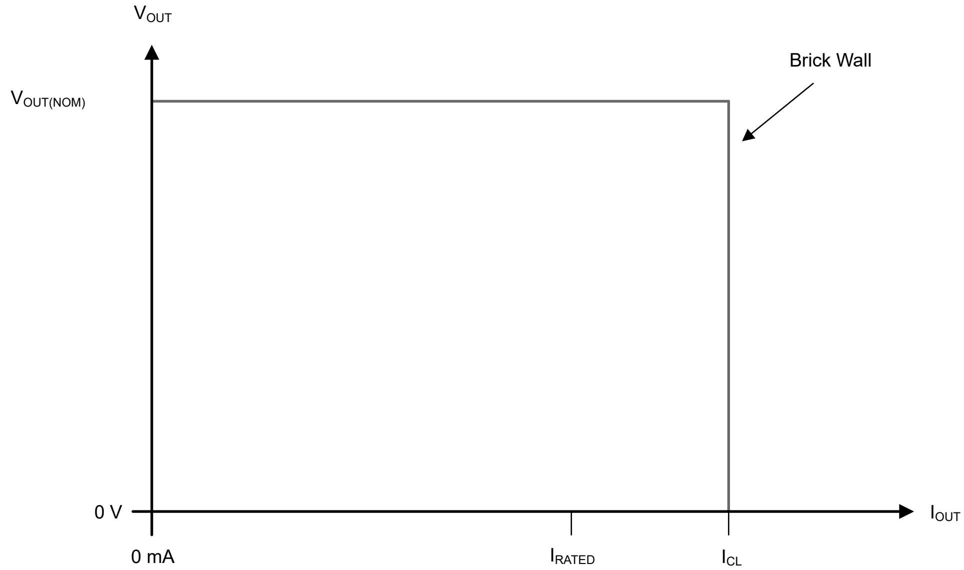

Figure 6-4. Current Limit: Brick-Wall Scheme

6.3.5 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis verifies that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

When the thermal limit is triggered with the load current near the value of the current limit, the output can oscillate prior to the output switching off.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.3.6 Power Good

The power-good (PG) pin is an open-drain output and can be connected to a regulated supply through an external pullup resistor. The maximum pullup voltage is listed as V_{PG} in the *Recommended Operating Conditions* table. For the PG pin to have a valid output, the voltage on the IN pin must be greater than 4V (minimum recommended operating input voltage). If the minimum recommended input voltage is not satisfied, PG behavior is undefined.

When V_{OUT} exceeds $V_{IT(PG,RISING)}$, the PG output is high impedance and the PG pin voltage pulls up to the connected regulated supply. When the regulated output falls below $V_{IT(PG,FALLING)}$, the open-drain output turns on and pulls the PG output low after a short deglitch time. If output voltage monitoring is not needed, the PG pin can be left floating or connected to ground.

The recommended maximum PG pin sink current ($I_{PG\text{-}SINK}$) and the leakage current into the PG pin ($I_{LKG(PG)}$) are listed in the *Electrical Characteristics* table.

The PG pullup voltage (V_{PG_PULLUP}), the desired minimum power-good output voltage ($V_{PG(MIN)}$), and $I_{LKG(PG)}$ limit the maximum PG pin pullup resistor value (R_{PG_PULLUP}). V_{PG_PULLUP}, the PG pin low-level output voltage ($V_{OL(PG)}$), and $I_{PG\text{-}SINK}$ limit the minimum R_{PG_PULLUP}. Maximum and minimum values for R_{PG_PULLUP} can be calculated from the following equations:

$$R_{PG\_PULLUP(MAX)} = (V_{PG\_PULLUP} - V_{PG(MIN)}) / I_{LKG(PG)\_MAX} \tag{2}$$

$$R_{PG\_PULLUP(MIN)} = (V_{PG\_PULLUP} - V_{OL(PG)}) / I_{PG\text{-}SINK} \tag{3}$$

For example, if the PG pin is connected to a pullup resistor with a 3.3V external supply, from the *Electrical Characteristics* table, $R_{PG\_PULLUP(MAX)}$ is 25MΩ. From the *Electrical Characteristics* table, $R_{PG\_PULLUP(MIN)}$ is 6.6kΩ.

Note that $V_{PG(MIN)}$ is a user-defined voltage. For a given application, $V_{PG(MIN)}$ is selected based on the undervoltage threshold that is of interest to monitor.

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6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{EN}	I_{MID_OUT}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{MID\_OUT} < I_{MID\_OUT(max)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation on MID_OUT	$V_{IN(min)} < V_{IN} < V_{MID\_OUT(nom)} + V_{DO(MID\_OUT)}$	$V_{EN} > V_{EN(HI)}$	$I_{MID\_OUT} < I_{MID\_OUT(max)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation on OUT	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO(OUT)}$	$V_{EN} > V_{EN(HI)}$	$I_{MID\_OUT} < I_{MID\_OUT(max)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < 4V$	$V_{EN} < V_{EN(LOW)}$	Not applicable	Not applicable	$T_J > T_{SD(reset)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltages when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage on either rails ($V_{MID\_OUT(nom)} + V_{DO(MID\_OUT)}$ and $V_{OUT(nom)} + V_{DO(OUT)}$)
- The current sourced from either MID_OUT and OUT is less than the respective current limit specified in the *Electrical Characteristics* table for each rail
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$)
- The enable voltage has previously exceeded the $V_{EN(HI)}$ (maximum) threshold and has not yet decreased to less than the $V_{EN(LOW)}$ minimum threshold
- V_{IN} has exceeded 4V if the EN pin is left floating

6.4.3 Dropout Operation

Because the TPS7A43-Q1 has two output rails (MID_OUT and OUT), the device can be in either $V_{DO(MID\_OUT)}$ or $V_{DO(OUT)}$, or in both depending on the input voltage level while all other conditions are met for normal operation. When the input voltage drops to lower than $V_{MID\_OUT(nom)} + V_{DO(MID\_OUT)}$, the device is in $V_{DO(MID\_OUT)}$ dropout. During this rail dropout, V_{MID_OUT} tracks V_{IN} and the transient performance of V_{MID_OUT} becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. The MID_OUT rail line or load transients in the $V_{DO(MID\_OUT)}$ dropout can result in large V_{MID_OUT} deviations. When the device is still in $V_{DO(MID\_OUT)}$ and when V_{IN} is higher than $V_{OUT(nom)} + V_{DO(OUT)}$, V_{OUT} is in regulation and is not in $V_{DO(OUT)}$ dropout. When V_{IN} drops below $V_{OUT(nom)} + V_{DO(OUT)}$, V_{OUT} is no longer in regulation and transient performance becomes significantly degraded.

When the device is in a steady dropout state (when the device is in both $V_{DO(MID\_OUT)}$ and $V_{DO(OUT)}$ dropout, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to $V_{MID\_OUT(nom)} + V_{DO(MID\_OUT)}$ and greater than $V_{OUT(NOM)} + V_{DO}$, the output voltage (OUT) can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.4 Disabled

The outputs of the device can be shutdown by forcing the voltage of the enable pin to less than $V_{EN(LOW)}$ (minimum); see the *Electrical Characteristics* table. When disabled, the pass transistor is turned off and internal circuits are shutdown.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 MID_OUT Voltage Setting

The MID_OUT voltage has three different output voltage levels (10V, 12V, and 15V), as listed in Table 7-1, depending on the MVSEL1 and MVSEL2 pin voltage settings.

Table 7-1. MID_OUT Voltage Setting

SET V_{MVSEL1}	SET V_{MVSEL2}	MID_OUT
$V_{MVSEL1} \le V_{MVSEL1(LOW)}$	$V_{MVSEL2} \le V_{MVSEL2(LOW)}$	15V
$V_{MVSEL1} \le V_{MVSEL1(LOW)}$	$V_{MVSEL2} \ge V_{MVSEL2(HIGH)}$	12V
$V_{MVSEL1} \ge V_{MVSEL1(HIGH)}$	$V_{MVSEL2} \le V_{MVSEL2(LOW)}$	10V
$V_{MVSEL1} \ge V_{MVSEL1(HIGH)}$	$V_{MVSEL2} \ge V_{MVSEL2(HIGH)}$	12V

For adjustable voltage options of the TPS7A43-Q1, and to maintain voltage regulation on the MID_OUT and OUT pins, the input voltage must be kept ≥ MID_OUT + $V_{DO(MID\_OUT)}$. Additionally, to maintain regulation on the OUT pin, the MID_OUT voltage must be set ≥ $V_{OUT(nom)} + V_{DO(OUT)}$.

Set the MVSEL1 and MVSEL2 voltages before enabling the device to set the MID_OUT voltage level; however, the MID_OUT voltage setting can be changed to a different level after the device had powered up. Do not allow these pins to float, instead tie them both to GND if not used to set V_{MID_OUT}. When the device is powered while either of these pins are floating, the MID_OUT voltage is not set properly and can switch levels and cause damage to the device.

7.1.2 Use Without MID_OUT

The MID_OUT rail does not need to be utilized if not required by the user's system. If the TPS7A43-Q1 is used only to drive a load connected to OUT, a capacitor must still be connected from MID_OUT to ground for stability. Follow the recommended capacitor value for C_{MID_OUT} as listed in the *Recommended Operating Conditions* table.

7.1.3 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, $R_{FB(TOP)}$ and $R_{FB(BOTTOM)}$, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_{FB(TOP)} / R_{FB(BOTTOM)}) \tag{4}$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100 times the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_{FB(TOP)} + R_{FB(BOTTOM)} \le V_{OUT} / (I_{FB} \times 100) \tag{5}$$

Figure 7-1 shows a circuit diagram which includes $R_{FB(TOP)}$ and $R_{FB(BOTTOM)}$.

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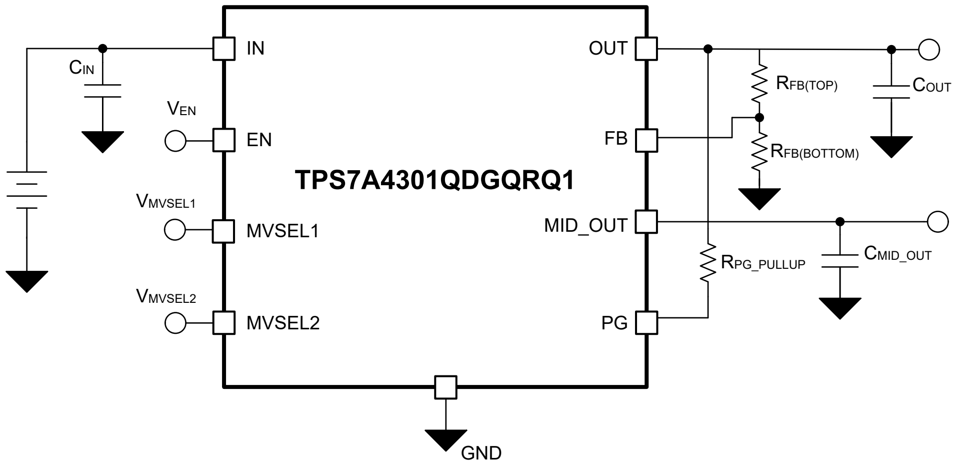

Figure 7-1. Typical Application Circuit for Adjustable Output Version

7.1.4 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a general rule, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table are capacitor values and account for an effective capacitance of approximately 50% of the nominal value.

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7.1.5 Input and Output Capacitor Requirements

An input capacitor is not required for stability except when the device maximum current is sourced from the MID_OUT pin. However, adding an input capacitor is always good analog design practice to counteract reactive input sources and improve transient response, input ripple, and PSRR. Starting with the nominal input capacitor value is required if large, fast transient load or line transients are anticipated on the MID_OUT pin or if the device is located several inches from the input power source.

A minimum of a 3:1 capacitor ratio between C_{MID_OUT} and C_{OUT} is required for proper operation of the TPS7A43-Q1 LDO, and a 4.7µF capacitor can be connected from the MID_OUT pin to GND.

A minimum 1µF output capacitor is required for V_{OUT} stability. A maximum 100µF output capacitor can be used as long as the 3:1 ratio between C_{MID_OUT} and C_{OUT} is maintained. Refer to the *Recommended Operating Conditions* table.

7.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{6}$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{7}$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

7.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). As described in Equation 8 and Equation 9, these parameters provide two methods for calculating the junction temperature (T_J). Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

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$$T_J = T_T + \psi_{JT} \times P_D \quad (8)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (9)$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.2 Typical Application

This section discusses the implementation of the TPS7A43-Q1 in an application for automotive body motors. Figure 7-2 shows a typical circuit diagram for one such application.

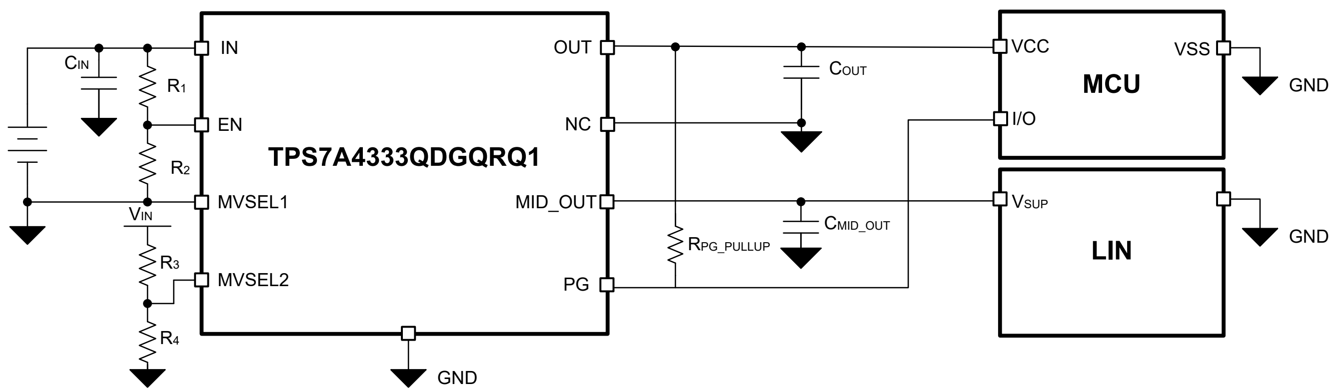


Figure 7-2. Power for Door Modules

7.2.1 Design Requirements

Table 7-2 summarizes the design requirements for an example application for door modules.

Table 7-2. Design Parameters

PARAMETER	DESIGN VALUES
V_{IN}	48V (typical), 85V (transient max)
V_{IN} (system undervoltage)	24V
V_{OUT}	3.3V ± 2%
V_{MVSEL1}	0V
V_{MVSEL2}	≥0.9V
V_{MID_OUT}	12V ± 5%
$I_{(IN)}$ (no load)	< 9μA
I_{OUT} (typical), (max)	20mA, 40mA
I_{MID_OUT} (typical), (max)	1mA, 5mA
T_A	85°C (max)

7.2.2 Detailed Design Procedure

A fixed 3.3V output voltage device is used for this application. The MID_OUT voltage is set to 12V by tying the V_{MVSEL1} pin to GND and setting V_{MVSEL2} to ≥ 0.9V using the R3 and R4 resistor divider. The value of the R3 and R4 divider ratio must verify that V_{MVSEL2} is set to ≥ 0.9V when V_{IN} ≥ 24V. To limit the current burned through this divider to 5µA, R3 can be calculated using Equation 10, and the calculated value then can be rounded to the nearest standard value. When V_{IN} goes all the way up to 85V during a transient, the V_{MSEL2} voltage goes up to 3.188V (which is still lower than the maximum recommended value for this pin, as specified in the *Recommended Operating Conditions* table).

$$R3 = \frac{24V - 0.9V}{5\mu A} = 4.62M\Omega \tag{10}$$

R4 then can be calculated with Equation 11 by using the VMVSEL2 value of the same current value.

$$R4 = \frac{0.9V}{5\mu A} = 180k\Omega \tag{11}$$

The enable precision circuit is used to turn off the device when V_{IN} falls below 24V. The R1 and R2 resistor divider is used to set V_{EN} to lower than $V_{EN(LOW)}$ of 1.11V when V_{IN} ≤ 24V. R1 can be calculated using Equation 12 to limit the burned current through this divider to 5µA, similar to the above divider. For the R1 and R2 values used below, the LDO turns on when V_{EN} surpasses $V_{EN(HI)}$ of 1.15V minimum (V_{IN} = 24.9V), 1.35V maximum (V_{IN} = 29.2V).

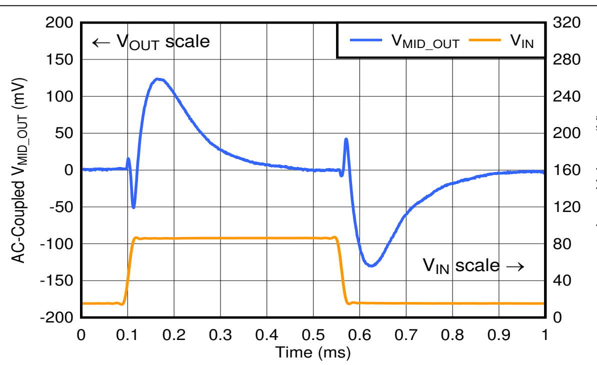
$$R1 = \frac{24V - 1.11V}{5\mu A} = 4.578M\Omega \tag{12}$$

Equation 13 can then be used to calculate R2. The calculated R1 and R2 values can then rounded to the nearest standard values.

$$R2 = \frac{1.11V}{5\mu A} = 222k\Omega \tag{13}$$

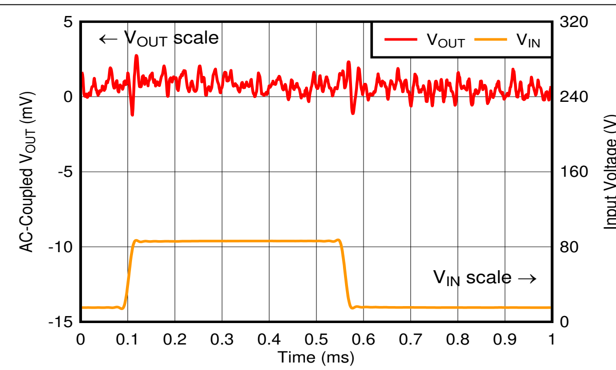
Conversely, if a rising V_{IN} condition to enable the LDO is more important to the system, R1 and R2 can also be selected to target a specific rising voltage threshold. If this is the case, R1 must be selected based on the V_{IN} threshold of interest and $V_{EN(HI)}$ of 1.35V.

7.2.3 Application Curves



V_{IN} = 15V to 85V, V_{IN} ramp rate = 10V/µs, V_{MVSEL1} = 0V, V_{MVSEL2} = 0.9V, I_{OUT} = 50mA, I_{MID_OUT} = open

Figure 7-3. TPS7A43-Q1 Line Transient: 15V to 85V



V_{IN} = 15V to 85V, V_{IN} ramp rate = 10V/µs, V_{MVSEL1} = 0V, V_{MVSEL2} = 0.9V, I_{OUT} = 50mA, I_{MID_OUT} = open

Figure 7-4. TPS7A43-Q1 Line Transient: 15V to 85V (Zoom on V_{OUT})

7.3 Power Supply Recommendations

The device is designed to operate from an input supply voltage range of 4V to 85V. To verify that the output voltages are well regulated and dynamic performance is optimum, the input supply must be at least $V_{MID\_OUT(nom)}$ + 1.5V. Connect a low output impedance power supply directly to the input pin of the TPS7A43-Q1.

7.4 Layout

7.4.1 Layout Guidelines

- Place input and output capacitors as close to the device pins as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device and under the thermal pad to distribute heat.
- Only place tented thermal vias directly beneath the thermal pad of the DGQ package. An untented via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

7.4.2 Layout Examples

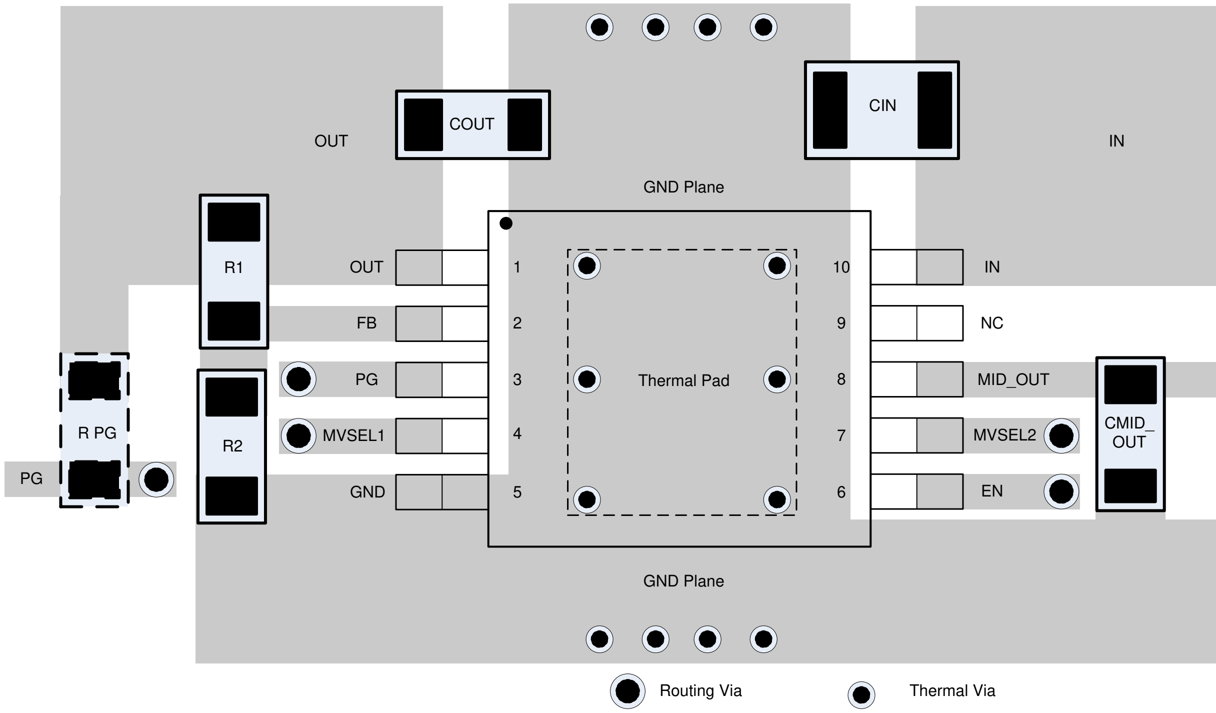


Figure 7-5. Adjustable Version Layout Example

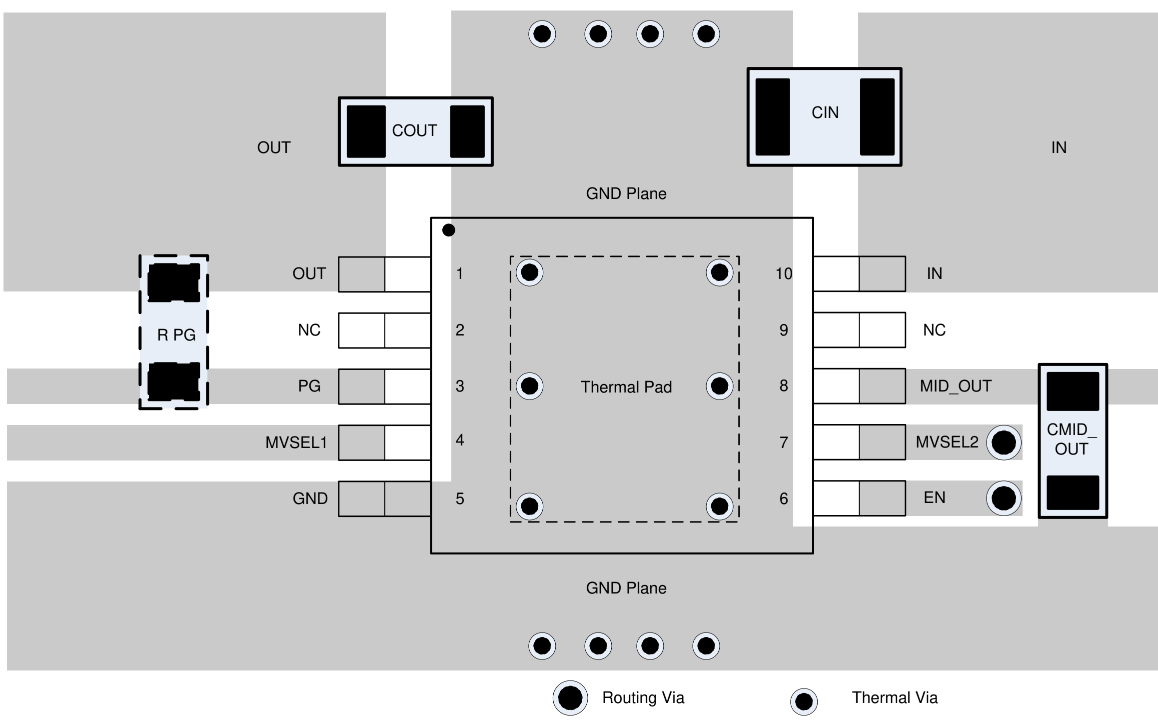


Figure 7-6. Fixed Version Layout Example

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Modules

An evaluation module (EVM) for a similar pin-to-pin device, the TPS7A43, is available to assist in the initial circuit performance evaluation for the TPS7A43-Q1. The *TPS7A43EVM-047 Evaluation Module* user guide can be requested at the Texas Instruments website through the product folders or purchased directly from the TI Store.

8.1.1.2 Spice Models

SPICE models for the TPS7A43-Q1 are available through the product folder under *Tools & software*.

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature (1)

PRODUCT	V_{OUT}
TPS7A43**xx**Q**yyy** **R**Q1	**xx** is the nominal output voltage. For example, 33 = 3.3V, 50 = 5V, 01 = adjustable. **Q** indicates that the device is grade-1 in accordance with the AEC-Q100 standard. **yyy** is the package designator. For example, DGQ = HVSSOP-10. **R** is the designator for large quantity reel packing. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7A43EVM-047 Evaluation Module* user guide
- Texas Instruments, *LDO Basics: Preventing reverse current* blog
- Texas Instruments, *LDO basics: capacitor vs. capacitance* blog

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS7A4301QDGQRQ1	Active	Preproduction	HVSSOP (DGQ) | 10	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS7A4333QDGQRQ1	Active	Preproduction	HVSSOP (DGQ) | 10	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPS7A4350QDGQRQ1	Active	Preproduction	HVSSOP (DGQ) | 10	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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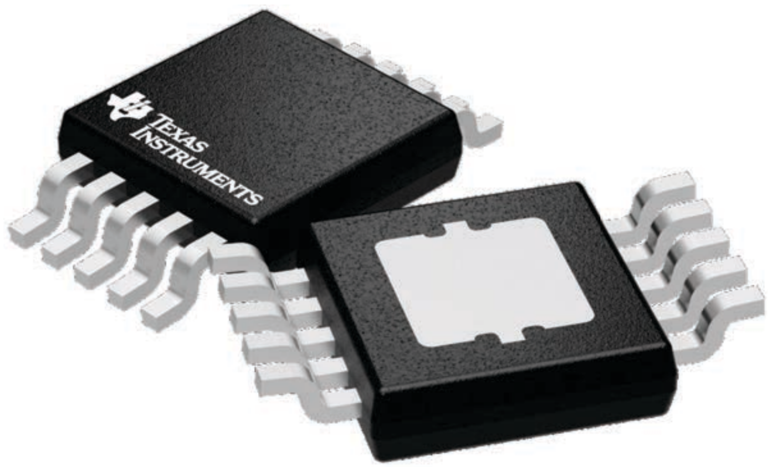
OTHER QUALIFIED VERSIONS OF TPS7A43-Q1 :

- Catalog : TPS7A43

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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