TPS7H1111-SP and TPS7H1111-SEP 1.5-A, Ultra-Low Noise, High PSRR Radiation Hardened Low Dropout (LDO) Linear Regulator

1 Features

- Total ionizing dose (TID) characterized
  - Radiation hardness assurance (RHA) availability of 100 krad(Si) or 50 krad(Si)
- Single-Event Effects (SEE) characterized
  - Single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune up to linear energy transfer (LET) = 75 MeV-cm^2/mg
  - Single-event functional interrupt (SEFI) and single-event transient (SET) characterized up to LET = 75 MeV-cm^2/mg
- Ultra-low noise (10 Hz to 100 kHz):
  - 1.71 μV_{RMS} (typ)
- High power-supply rejection ratio, PSRR (typ):
  - 109 dB at 1 kHz
  - 71 dB at 100 kHz
  - 66 dB at 1 MHz
- Input voltage range from 0.85 V to 7 V
- Bias supply of 2.2 V to 14 V to minimize power dissipation
- Output voltage as low as 0.4 V
- Up to 1.5-A output current
- Excellent output accuracy over line and load:
  - –1.3% to +1.2% across temperature
  - –0.7% to +0.9% at 25°C
- Low-dropout: 215 mV (typ) at 1.5 A
- Programmable soft-start control (SS_SET)
- Open-drain power good (PG) indicator
- Configurable power good threshold (FB_PG)
- Exposed control loop with the external compensation STAB pin
- Internal current limit with configurable behavior
- Current sharing to allow operation of up to 2.9 A
- Military temperature range (–55°C to 125°C)

2 Applications

- Satellite electrical power system (EPS)
- Power for high-speed and high-accuracy circuits
  - Data converters: ADCs and DACs (analog-to-digital and digital-to-analog converters)
  - VCOs (voltage controlled oscillators)
  - PLLs (phase-locked loops)
  - SerDes (serializers and deserializers)
  - Imaging sensors
- Accurate supply for FPGAs (field programmable gate arrays) and DSPs (digital signal processors)
- Radiation-hardened ultra-clean analog supply for space constrained areas

3 Description

The TPS7H1111 is an ultra-low noise, high PSRR, low dropout linear regulator (LDO) optimized for powering radio-frequency (RF) devices in a space environment. It is capable of sourcing up to 1.5 A over a 0.85-V to 7-V input range with a 2.2-V to 14-V bias supply.

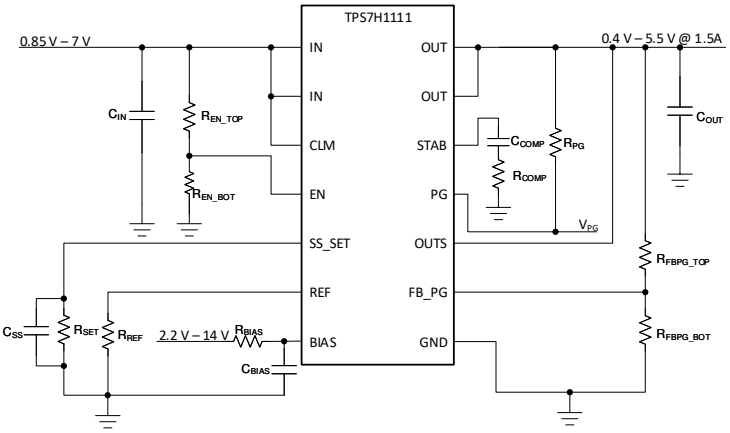
The high performance of the device limits power-supply generated phase noise and clock jitter, making this device ideal for powering high-performance ADCs, DACs, VCOs, PLLs, SerDes, and other RF components in satellites. For digital loads (such as FPGAs and DSPs) requiring low voltage operation, the exceptional accuracy and excellent transient performance ensure optimal system performance.

A standard microcircuit drawing (SMD) is available for the QML variants, 5962R21203. A vendor item drawing (VID) is available for the -SEP variant, V62/23602.

Device Information

PART NUMBER(1)	GRADE	PACKAGE(2)
5962R2120301VXC	QMLV-RHA	14-pin ceramic 8.03 mm × 9.12 mm Mass = 1.23 g
TPS7H1111HBL/EM	Engineering sample	
5962R2120302PYE	QMLP-RHA	28-pin plastic 4.40 mm × 9.70 mm Mass = 198 mg
TPS7H1111MPWPTSEP	SEP	

(1) For additional information view the Device Options Table.
(2) Dimension and mass values are nominal.



Typical Application Circuit

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Device Options Table....3
5 Pin Configuration and Functions....4
6 Specifications....6
6.1 Absolute Maximum Ratings....6
6.2 ESD Ratings....6
6.3 Recommended Operating Conditions....7
6.4 Thermal Information....7
6.5 Electrical Characteristics....8
6.6 Quality Conformance Inspection....11
6.7 Typical Characteristics....12
7 Parameter Measurement Information....25
8 Detailed Description....26
8.1 Overview....26
8.2 Functional Block Diagram....26
8.3 Feature Description....27
8.4 Device Functional Modes....40
9 Application and Implementation....41
9.1 Application Information....41
9.2 Typical Applications....41
9.3 Capacitors Tested....48
9.4 TID Effects....48
9.5 Power Supply Recommendations....50
9.6 Layout....51
10 Device and Documentation Support....53
10.1 Documentation Support....53
10.2 Receiving Notification of Documentation Updates....53
10.3 Support Resources....53
10.4 Trademarks....53
10.5 Electrostatic Discharge Caution....53
10.6 Glossary....53
11 Revision History....53
12 Mechanical, Packaging, and Orderable Information....55

Copyright © 2023 Texas Instruments Incorporated

4 Device Options Table

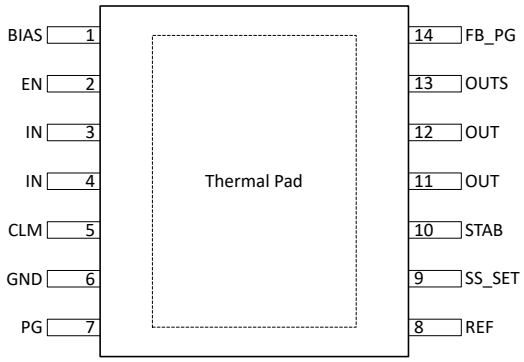
GENERIC PART NUMBER	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER
TPS7H1111-SP	TID of 100 krad(Si) RLAT, DSEE free to 75 MeV-cm^2/mg	QMLV-RHA	14-pin CFP HBL	5962R2120301VXC
		QMLP-RHA	28-pin HTSSOP PWP	5962R2120302PYE
	None	Engineering Model(3)	14-pin CFP HBL	TPS7H1111HBL/EM
TPS7H1111-SEP	TID of 50 krad(Si) RLAT, DSEE free to 43 MeV-cm^2/mg	Space Enhanced Plastic	28-pin HTSSOP PWP	TPS7H1111MPWPTSEP
SN0014HBL	N/A	Mechanical "dummy" package (no die)	14-pin CFP HBL	SN0014HBL

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) For additional information about part grade, view SLYB235.
(3) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (such as no burn-in and only 25°C testing). These units are not suitable for qualification, production, radiation testing, or flight use. Parts are not warranted as to performance over temperature or operating life.

Copyright © 2023 Texas Instruments Incorporated

5 Pin Configuration and Functions

HBL Package
14-Pin CFP
(Top View)



PWP Package
28-Pin HTSSOP
(Top View)

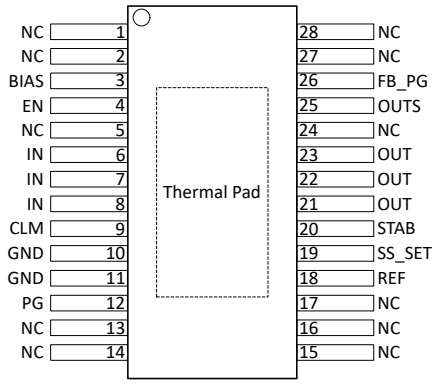


Table 5-1. Pin Functions

PIN			I/O[1]	DESCRIPTION
NAME	HBL (14) NO.	PWP (28) NO.		
BIAS	1	3	I	Bias supply. To support full output current, a separate bias supply is required if the headroom voltage is less than 1.6 V ($V_{headroom} = V_{IN} – V_{OUT} < 1.6$ V). Set the separate bias supply to a voltage at least 1.6 V higher than V_{OUT} for full output current support. A 12-V bias supply will satisfy these conditions (generally a 5-V supply will also suffice). There are no sequencing requirements between V_{BIAS} and V_{IN}. In order to limit noise on BIAS, an RC filter is recommended (typically 10 Ω and 4.7 µF) unless V_{BIAS} is an ultra-clean supply. If a separate bias supply is not used, connect BIAS to V_{IN} (it is also recommended to connect the V_{IN} rail to the BIAS pin through an RC filter).
EN	2	4	I	Enable. Driving this pin to logic high enables the device; driving the pin to logic low disables the device. If enable functionality is not required, connect this pin to IN. Do not float this pin.
IN	3, 4	6, 7, 8	I	Input power. An input capacitor (nominally 10 µF) near this pin is recommended.
CLM	5	9	I	Current limit mode. Connect CLM to V_{IN} for brick-wall current limit mode (when current limit is reached, V_{OUT} is regulated to maintain a constant output current until the fault is removed). Connect CLM to GND for turn-off current limit mode (when current limit is reached, V_{OUT} stops regulating until EN is toggled). Do not change the value of this pin when the device is enabled, and do not float this pin.
GND	6	10, 11	—	Ground.
PG	7	12	O	Power good indicator. This is an open drain pin. Use a pull-up resistor to pull this pin up to V_{OUT} or the desired logic level. It is recommended to pull down PG to ground if unused but it may be left floating.
REF	8	18	I/O	Reference pin. REF outputs a nominal 1.2 V. Place a high accuracy 12.0-kΩ external resistor from REF to GND to set the internal 100-µA current source.
SS_SET	9	19	I/O	Soft-start and voltage set pin. An external capacitor (nominally 4.7-µF ceramic) is used to slow down the output voltage ramp rate during startup along with filtering internal device noise. Capacitor values less than 4.7 µF will result in marginally higher output noise. There is internal fast start circuitry to enable reasonable soft start times. Additionally, a resistor from SS_SET to GND sets the output voltage. During nominal operation, 100 µA is output on this pin and a resistor from SS_SET to GND sets the output voltage.
STAB	10	20	I/O	Stability pin. This is an output from the internal OTA (operational transconductance) error amplifier to aid in measuring or optimizing the control loop. Use a series capacitor (C_{COMP}) and resistor (R_{COMP}) of 4.7 nF and 5 kΩ to compensate the device. For different compensation options, view Section 8.3.8.2. A C0G (NP0) type capacitor capable of withstanding the lower of V_{BIAS} or 7.5 V is recommended (for example, a 25-V rated capacitor).

Copyright © 2023 Texas Instruments Incorporated

Table 5-1. Pin Functions (continued)

PIN			I/O[1]	DESCRIPTION
NAME	HBL (14) NO.	PWP (28) NO.		
OUT	11, 12	21, 22, 23	O	Output power pin. The regulated output voltage. A single 220-µF or two 100-µF tantalum or tantalum polymer capacitors are recommended. See Section 8.3.8.1 for additional information.
OUTS	13	25	I	Output sense pin. This pin is used to sense the output voltage for regulation. Connect OUTS to the OUT pin at the desired point of regulation (remote sense).
FB_PG	14	26	I	Feedback and power good pin. The FB_PG pin enables setting of a configurable power good threshold. This is achieved by feeding the output voltage through a resistor divider to this pin (typical threshold of 300 mV). When the threshold is reached, PG is asserted. Additionally, when the threshold on this pin is reached, start-up is over and the internal fast start circuitry is disabled. If this pin is connected directly to OUT, fast start operation ceases and PG is asserted as soon as V_{OUT} reaches 300 mV (typical).
NC		1, 2, 5, 13, 14, 15, 16, 17, 24, 27, 28	—	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
Thermal pad			—	The ceramic package thermal pad is internally connected to the backside of the die through an electrically conductive path and to the GND pin. It is recommended to connect this metal thermal pad to a large ground plane for effective heat dissipation. The plastic package thermal pad is connected to the backside of the die through an electrically conductive path, it is not internally grounded. Connect the thermal pad to a large ground plane for effective heat dissipation and to provide a connection of the backside of the die to GND for proper operation.
Metal lid	Lid	N/A	—	The lid is internally connected to the thermal pad and GND through the seal ring.

(1) I = Input, O = Output, I/O = Input or Output, — = Other

Copyright © 2023 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	IN	–0.3	7.5	V
	BIAS	–0.3	16	
	EN, PG, FB_PG, OUTS, CLM	–0.3	7.5	
Output voltage	OUT	–0.3	7.5	V
	SS_SET, REF, STAB	–0.3	7.5	
Input current	PG	–0.001	0.01	A
Output current	OUT	–2	2.25	A
Junction temperature	T_J	–55	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Copyright © 2023 Texas Instruments Incorporated

6.3 Recommended Operating Conditions

over operating temperature range, T_J = –55°C to 125°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	IN	0.85		7	V
	BIAS(1)	V_{IN}	V_{OUT} + 1.6 V		
		2.2		14	
	PG	0		7	
	EN	0		7	
	FB_PG	0		6	
	CLM	0		V_{IN}	
Output voltage	OUT(2)			$V_{IN} – V_{DO}$	V
		0.4		5.5	
	SS_SET(2)			$V_{IN} – V_{DO}$	
		0.4		5.5	
Input current	PG	0		0.002	A
Output current	OUT	0		1.5	A
Output bulk capacitance(3)	C_{OUT}	132	200	308	µF
	ESR	7		40	mΩ
	ESL	0.8		2.4	nH
Reference configuration	R_{REF}	11	12	13	kΩ
EN toggle time(4)	t_{EN_LOW}	20			µs
Junction temperature	T_J	–55		125	°C

(1) BIAS has two minimum values, V_{IN} and 2.2 V. BIAS must be set greater than or equal to the larger of these two values. The BIAS max value is always 14 V. For full performance set $V_{BIAS} \geq V_{OUT}$ + 1.6 V. See the *Bias Supply Section* for further details.

(2) OUT and SS_SET have two maximum values, ($V_{IN} – V_{DO}$) and 5.5 V. OUT and SS_SET must be set to less than or equal to the smaller of these two values. The OUT and SS_SET min value is always 0.4 V.

(3) These are the default acceptable output capacitance, equivalent series resistance (ESR), and equivalent series inductance (ESL) values for the bulk capacitance. Other values may be acceptable, such as by modifying the control loop with external compensation using the STAB pin. Tantalum or Tantalum Polymer capacitors are normally used to meet these requirements. Additional ceramic decoupling capacitors are not required, but a single 0.1 µF ceramic capacitor with low ESL near the point of load is acceptable. Additional larger ceramic capacitors are not needed due to the high PSRR and low noise provided by the TPS7H1111 LDO across a wide bandwidth. Therefore, the TPS7H1111 is not designed to support larger ceramic capacitors. See the *Output Capacitance Section* for additional information.

(4) t_{EN_LOW} is the time the EN pin must be driven low before again being driven high for the device to detect a reset. This is generally only applicable when attempting to exit turn-off current limit mode.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7H1111-SP CFP HBL 14 PINS	TPS7H1111-SEP PWP (HTSSOP) 28 PINS	TPS7H1111-SP PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.1	24.7	24.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.3	15.6	15.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	6.6	6.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	0.2	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.1	6.6	6.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	1.0	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Copyright © 2023 Texas Instruments Incorporated

6.5 Electrical Characteristics

Over 0.85 V ≤ V_{IN} ≤ 7 V, V_{BIAS} ≥ V_{OUT} + 1.6 V (V_{IN} ≤ V_{BIAS} ≤ 14 V & V_{BIAS} ≥ 2.2 V), V_{OUT} (target) ≤ V_{IN} – 1.6 V, I_{OUT} = 1 mA, C_{OUT} = 220 µF[1], R_{REF} = 12.0 kΩ, over operating temperature range (T_A = –55°C to 125°C), typical values are at T_A = 25°C, unless otherwise noted; includes RLAT at T_A = 25°C if sub-group number is present for QML RHA and SEP devices[2]

PARAMETER		TEST CONDITIONS		SUB-GROUP[3]	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
V_{DO}	Dropout voltage with V_{BIAS} ≥ V_{OUT} + 1.6 V	0.85 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$	I_{OUT} = 0.1 A	1, 2, 3		17	40	mV
			I_{OUT} = 0.5 A	1, 2, 3		75	150	
			I_{OUT} = 1 A	1, 2, 3		110	280	
			I_{OUT} = 1.5 A	1, 2, 3		215	430	
V_{DO}	Dropout voltage with V_{BIAS} = V_{IN}	2.2 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$	I_{OUT} = 0.1 A	1, 2, 3		785	1100	mV
			I_{OUT} = 0.5 A	1, 2, 3		908	1150	
			I_{OUT} = 1 A	1, 2, 3		1063	1250	
			I_{OUT} = 1.5 A	1, 2, 3		1168	1400	
I_{LIM}	Output current limit	2.5 V ≤ V_{IN} ≤ 7 V V_{OUT} = 0.5 V, V_{CLM} = V_{IN}	T_A = -55°C	3	1.8	1.95	2.1	A
			T_A = 25°C	1	1.75	1.85	2	
			T_A = 125°C	2	1.7	1.8	1.95	
$I_{CLM(LKG)}$	CLM input leakage current	V_{CLM} = 7 V		1, 2, 3		5	150	nA
I_{Q_IN}	Quiescent current	V_{EN} = 7 V, I_{OUT} = 0 A		1, 2, 3		19	27	mA
I_{Q_BIAS}	Bias current with no output load	V_{EN} = 7 V, I_{OUT} = 0 A		1, 2, 3		16	25	
I_{IN_GND}	I_{IN} – I_{OUT} with full output load	V_{EN} = 7 V, I_{OUT} = 1.5 A		1, 2, 3		20	27	mA
I_{BIAS}	Bias current with full output load	V_{EN} = 7 V, I_{OUT} = 1.5 A		1, 2, 3		17	25	
I_{SHDN}	Shutdown current	V_{EN} = 0 V, I_{OUT} = 0 A, V_{OUT} = 0 V		1, 2, 3		20	350	µA
I_{SHDN_BIAS}	Shutdown bias current	V_{EN} = 0 V, I_{OUT} = 0 A, V_{OUT} = 0 V		1, 2, 3		550	1000	
ACCURACY								
V_{ACC}	Output voltage accuracy	1 mA ≤ I_{OUT} ≤ 1.5 A, 2.2 V ≤ V_{BIAS} ≤ 14 V[4], P_D ≤ 4 W[5]	–55°C ≤ T_A ≤ 125°C	1, 2, 3	-1.3%		1.2%	
			T_A = –55°C	3	-1.3%		0.5%	
			T_A = 25°C	1	-0.7%		0.9%	
			T_A = 25°C, post TID[6]	1	-0.7%		1.1%	
			T_A = 125°C	2	-0.7%		1.2%	
I_{SET}	SS_SET pin current to set V_{OUT}	–55°C ≤ T_A ≤ 125°C		1, 2, 3	98.8	99.9	101	µA
		T_A = –55°C		3	98.8	99.4	100.3	
		T_A = 25°C		1	99.0	100	100.9	
		T_A = 125°C		2	99.2	100.2	101	
V_{OS}	Output offset voltage (V_{OUT} – V_{SS_SET})	–55°C ≤ T_A ≤ 125°C		1, 2, 3	–2		0.78	mV
		T_A = -55°C		3	–1.33	–0.2	0.78	
		T_A = 25°C		1	–1.45	–0.25	0.76	
		T_A = 25°C, post TID[6]		1	–1.45		1.5	
		T_A = 125°C		2	–2	–0.5	0.7	
V_{OUT}tempco	V_{OUT} temperature coefficient	T_A from –55°C to 125°C				0.004%		V_{OUT}/°C
		T_A from –55°C to –40°C				0.011%		
		T_A from –40°C to 0°C				0.007%		
		T_A from 0°C to 25°C				0.005%		
		T_A from 25°C to 85°C				0.003%		
		T_A from 85°C to 125°C				0.001%		

Copyright © 2023 Texas Instruments Incorporated

6.5 Electrical Characteristics (continued)

Over 0.85 V ≤ V_{IN} ≤ 7 V, V_{BIAS} ≥ V_{OUT} + 1.6 V (V_{IN} ≤ V_{BIAS} ≤ 14 V & V_{BIAS} ≥ 2.2 V), V_{OUT} (target) ≤ V_{IN} – 1.6 V, I_{OUT} = 1 mA, C_{OUT} = 220 µF(1), R_{REF} = 12.0 kΩ, over operating temperature range (T_A = –55°C to 125°C), typical values are at T_A = 25°C, unless otherwise noted; includes RLAT at T_A = 25°C if sub-group number is present for QML RHA and SEP devices(2)

PARAMETER		TEST CONDITIONS		SUB-GROUP(3)	MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage, ceramic package			1, 2, 3	1.191	1.206	1.220	V
V_{REF}	Reference voltage, plastic package			1, 2, 3	1.190	1.206	1.221	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation, see Figure 7-1	0.85 V ≤ V_{IN} ≤ 7 V, I_{OUT} = 1 mA, V_{BIAS} = 5 V, V_{OUT} = 0.4 V		1, 2, 3		3	200	µV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation, see Figure 7-2	1 mA ≤ I_{OUT} ≤ 1.5 A, V_{BIAS} = 5 V, V_{IN} = 2.5 V, V_{OUT} = 1.8 V		1, 2, 3		500	1000	µV/A
	Current sharing error percentage	$R_{ballast}$ = 5 mΩ, T_A = 25°C	$I_{OUT(TOTAL)}$ = 1.2 A			±1%		
			$I_{OUT(TOTAL)}$ = 2.9 A			±0.1%		
$I_{OUTS(LKG)}$	OUTS leakage current			1, 2, 3		20	200	nA
ENABLE								
$V_{EN(rising)}$	Enable rising threshold (turn-on)			1, 2, 3	0.58	0.60	0.62	V
$V_{EN(falling)}$	Enable falling threshold (turn-off)			1, 2, 3	0.48	0.50	0.52	V
$t_{EN(delay)}$	EN propagation delay	EN high to V_{OUT} = 10 mV		9, 10, 11		90	500	µs
$I_{EN(LKG)}$	Enable input leakage current	V_{EN} = 7 V		1, 2, 3		3	150	nA
$T_{SD(enter)}$	Thermal shutdown enter					160		°C
$T_{SD(exit)}$	Thermal shutdown exit					130		°C
POWER GOOD								
$V_{FB_PG(rising)}$	Power good rising threshold			1, 2, 3	290	306	313	mV
$V_{FB_PG(HYS)}$	Power good hysteresis			1, 2, 3	7	14	19	mV
$I_{FB_PG(LKG)}$	FB_PG input leakage current	V_{FB_PG} = 6 V		1, 2, 3		9	150	nA
$V_{PG(OL)}$	Power good output low	$I_{PG(SINK)}$ = 2 mA		1, 2, 3		113	200	mV
$V_{IN(MIN_PG)}$	Minimum V_{IN} or V_{BIAS} for valid PG (V_{PG} < 0.5 V)	$I_{PG(sink)}$ = 0.6 mA		1, 2, 3		0.6	0.8	V
$I_{PG(LKG)}$	Power good leakage	V_{PG} = 7 V, V_{FB_PG} > $V_{FB_PG(rising\ threshold)}$		1, 2, 3		0.1	2	µA
SOFT START								
$I_{SS_SET(start)}$	SS_SET pin current during startup			1, 2, 3	1.68	2.1	2.52	mA
t_{SS}	Soft-start time	V_{IN} =2.5V, V_{OUT} =1.8V, I_{OUT} = 1 A, $R_{FB_PG(top)}$ = 44.2 kΩ, $R_{FB_PG(bot)}$ = 10 kΩ	C_{SS} = 2.2 µF			1.7		ms
			C_{SS} = 4.7 µF			3.7		ms
			C_{SS} = 10 µF			7.8		ms
NOISE AND PSRR								
PSRR	Power-supply rejection ratio	V_{IN} =2.5V, V_{OUT} =1.8V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω	f_{ripple} = 100 Hz			109		dB
			f_{ripple} = 1 kHz			109		dB
			f_{ripple} = 10 kHz			90		dB
			f_{ripple} = 100 kHz			71		dB
			f_{ripple} = 1 MHz			66		dB
			f_{ripple} = 10 MHz			30		dB

Copyright © 2023 Texas Instruments Incorporated

6.5 Electrical Characteristics (continued)

Over 0.85 V ≤ V_{IN} ≤ 7 V, V_{BIAS} ≥ V_{OUT} + 1.6 V (V_{IN} ≤ V_{BIAS} ≤ 14 V & V_{BIAS} ≥ 2.2 V), V_{OUT} (target) ≤ V_{IN} – 1.6 V, I_{OUT} = 1 mA, C_{OUT} = 220 µF(1), R_{REF} = 12.0 kΩ, over operating temperature range (T_A = –55°C to 125°C), typical values are at T_A = 25°C, unless otherwise noted; includes RLAT at T_A = 25°C if sub-group number is present for QML RHA and SEP devices(2)

PARAMETER		TEST CONDITIONS		SUB-GROUP(3)	MIN	TYP	MAX	UNIT
$PSRR_{BIAS}$	Power-supply rejection ratio, V_{BIAS} to V_{OUT}	V_{IN} = 2.5V, V_{OUT} =1.8V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF, C_{BIAS} = 4.7 µF, R_{BIAS} = 10 Ω	f_{ripple} = 100 Hz			102		dB
			f_{ripple} = 1 kHz			105		
			f_{ripple} = 10 kHz			87		
			f_{ripple} = 100 kHz			97		
			f_{ripple} = 1 MHz			118		
			f_{ripple} = 10 MHz			68		
V_N	Output noise rms voltage (Bandwidth from 10 Hz to 100 kHz)	V_{IN} =2.5V, V_{OUT} = 1.8V, V_{BIAS} = 5 V, I_{OUT} = 1 A	C_{SS} = 2.2 µF			1.73		$µV_{RMS}$
			C_{SS} = 4.7 µF			1.71		
			C_{SS} = 10 µF			1.69		
e_N	Output noise voltage density	V_{IN} =2.5V, V_{OUT} =1.8V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{SS} = 4.7 µF	f = 10 Hz			97		nV/√Hz
			f = 100 Hz			11.2		
			f = 1 kHz			5.4		
			f = 10 kHz			5.6		
			f = 100 kHz			4.9		
			f = 1 MHz			1.6		
			f = 10 MHz			1.7		
STABILITY								
PM	Phase margin	V_{IN} = 2.5 V, V_{OUT} = 1.8 V, I_{OUT} = 1.0 A, C_{OUT} = 2x100 µF(7)				98°		
GM	Gain margin					19		dB

(1) A single 220 µF tantalum capacitor is utilized
(2) See the 5962R21203 SMD for additional information on the QML RHA devices and see the V62/23602 VID for additional information on the SEP devices.
(3) The subgroups are only applicable for QML versions of the device; for subgroup definitions, see Section 6.6.
(4) Additionally, V_{BIAS} ≥ V_{IN} and V_{BIAS} ≥ V_{OUT} + 1.6 V.
(5) P_D is the internal power dissipation. When P_D exceeds 4 W, the current is lowered to avoid excessive local heating (due to tester limitations).
(6) TID = 100 krad(Si) for QMLV and QMLP parts and TID = 50 krad(Si) for SEP parts.
(7) See Section 9.3 for additional information.

Copyright © 2023 Texas Instruments Incorporated

6.6 Quality Conformance Inspection

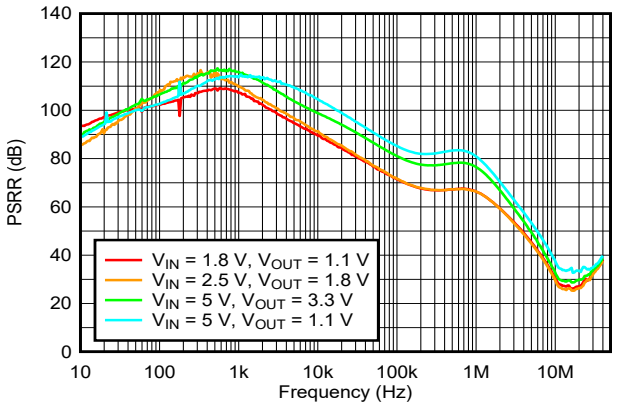
MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMPERATURE (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

Copyright © 2023 Texas Instruments Incorporated

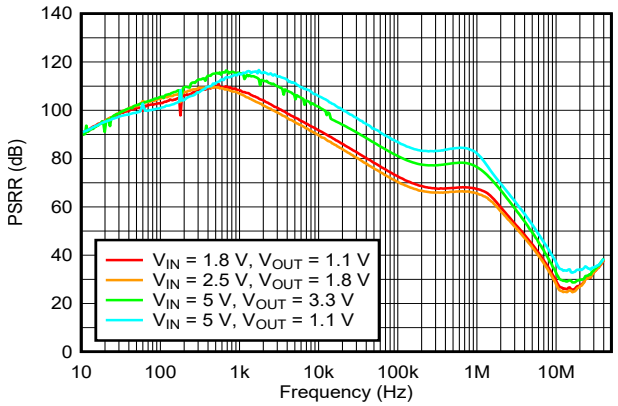
6.7 Typical Characteristics

V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{OUT} = 2 × 100 µF, C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, unless otherwise noted, integrated noise reported with 10-Hz to 100-kHz bandwidth.



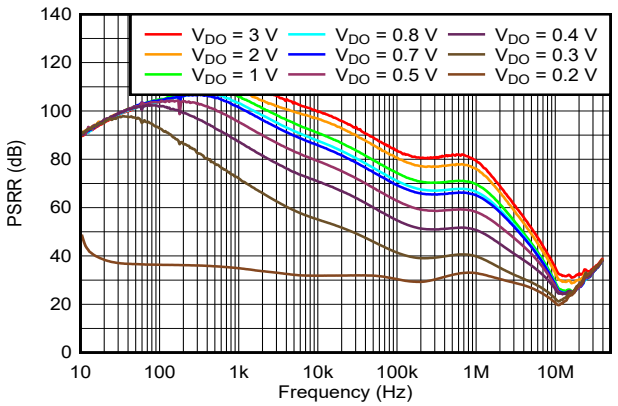
V_{BIAS} = 5 V

Figure 6-1. PSRR vs Frequency (Common Configurations)



V_{BIAS} = 12 V

Figure 6-2. PSRR vs Frequency (Common Configurations)



V_{IN} = V_{OUT} + V_{DO} V_{OUT} = 1.8 V V_{BIAS} = V_{OUT} + 1.6 V

Figure 6-3. PSRR vs Frequency Across Dropout

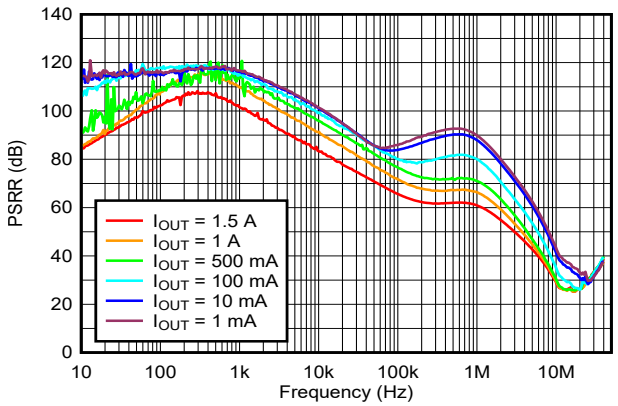
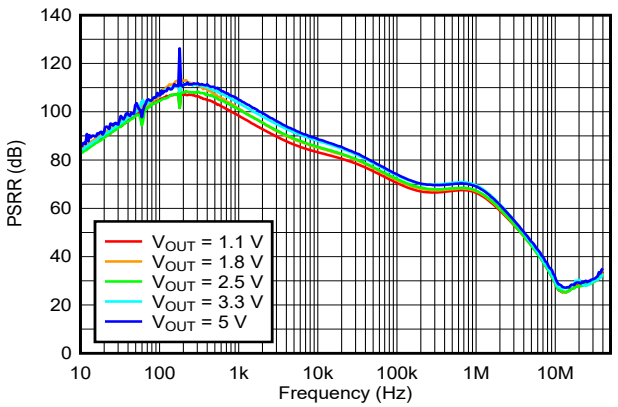
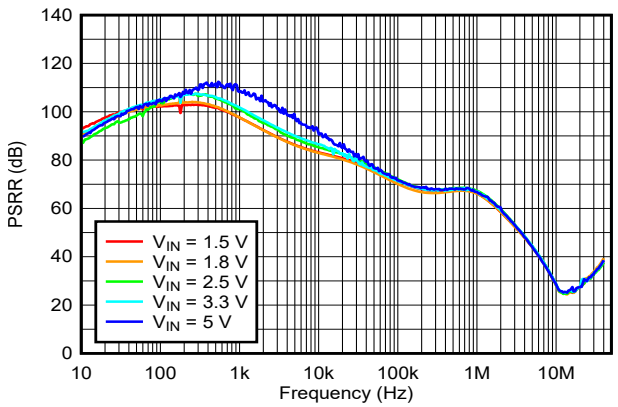


Figure 6-4. PSRR vs Frequency Across Output Current



V_{IN} = V_{OUT} + 0.8 V V_{BIAS} = V_{IN} + 1.6 V

Figure 6-5. PSRR vs Frequency Across Output Voltage



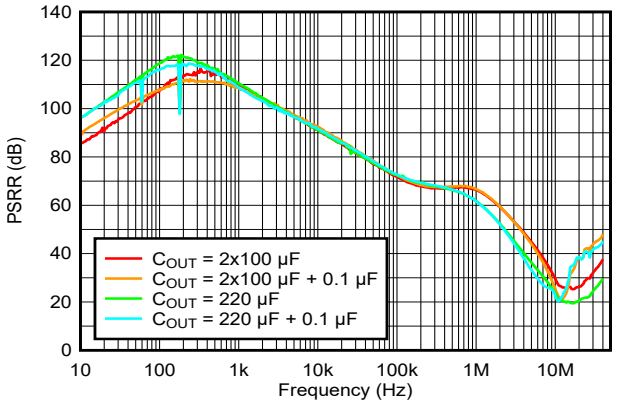
V_{OUT} = V_{IN} – 0.8 V V_{BIAS} = V_{OUT} + 1.6 V

Figure 6-6. PSRR vs Frequency Across Input Voltage

Copyright © 2023 Texas Instruments Incorporated

6.7 Typical Characteristics (continued)

V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{OUT} = 2 × 100 µF, C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, unless otherwise noted, integrated noise reported with 10-Hz to 100-kHz bandwidth.



See Table 9-4 for capacitor part numbers utilized.

Figure 6-7. PSRR vs Frequency Across Output Capacitors

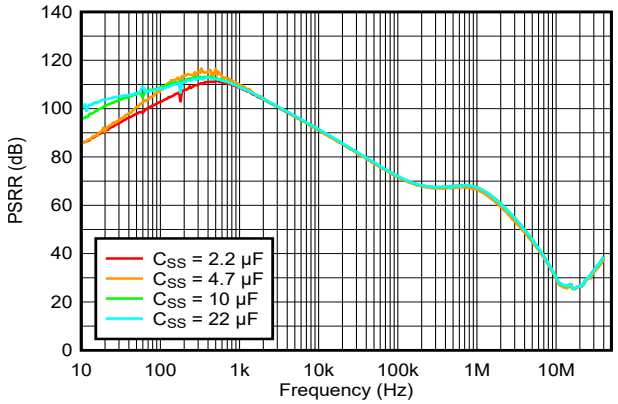


Figure 6-8. PSRR vs Frequency Across Soft Start Capacitance

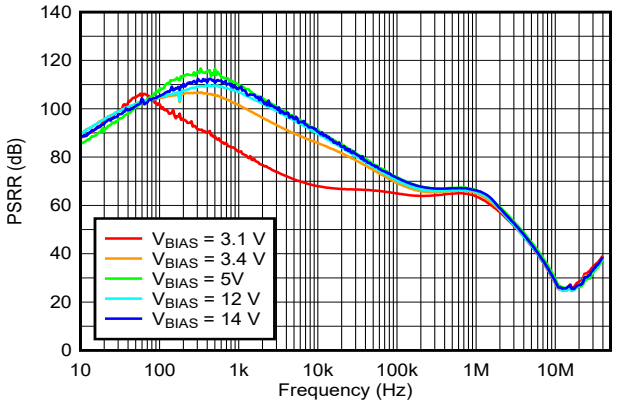
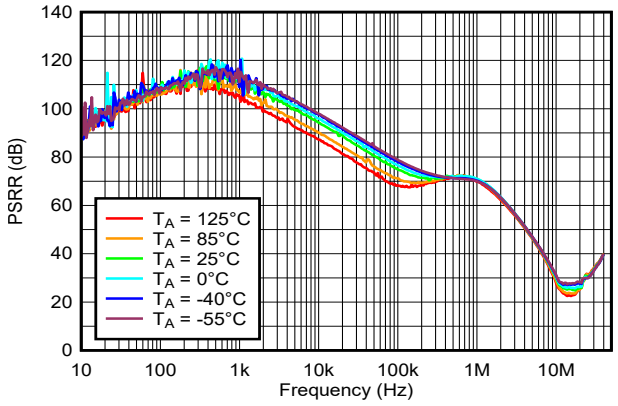
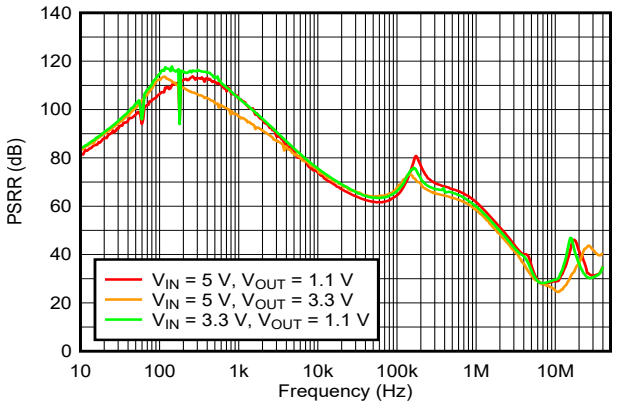


Figure 6-9. PSRR vs Frequency Across Bias Supply



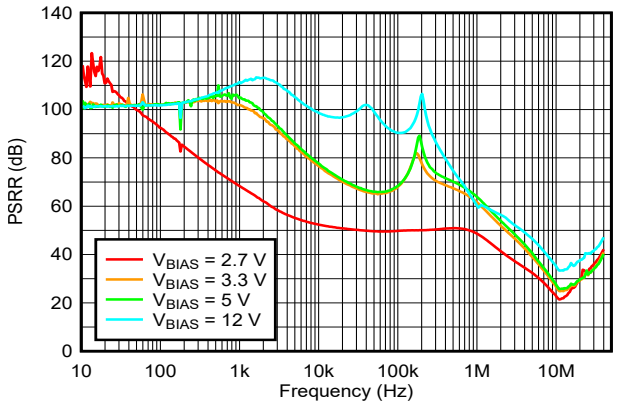
I_{OUT} = 500 mA

Figure 6-10. PSRR vs Frequency Across Temperature



R_{BIAS} = 0 Ω C_{BIAS} = 0 µF

Figure 6-11. PSRR vs Frequency With V_{IN} = V_{BIAS}

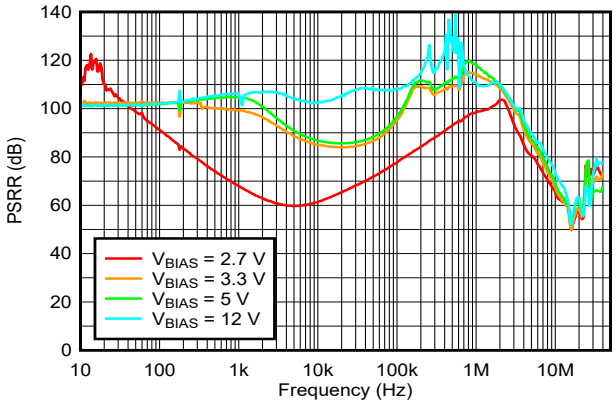


R_{BIAS} = 0 Ω

Figure 6-12. $PSRR_{BIAS}$ vs Frequency Across Bias Voltage Without RC

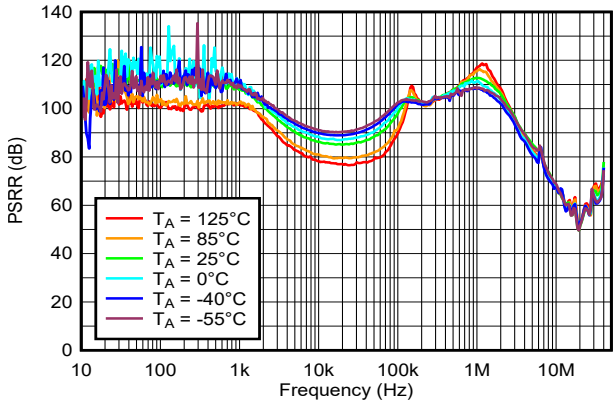
6.7 Typical Characteristics (continued)

V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{OUT} = 2 × 100 µF, C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, unless otherwise noted, integrated noise reported with 10-Hz to 100-kHz bandwidth.



R_{BIAS} = 10 Ω

Figure 6-13. $PSRR_{BIAS}$ vs Frequency Across Bias Voltage With RC



I_{OUT} = 500 mA

Figure 6-14. $PSRR_{BIAS}$ vs Frequency Across Temperature

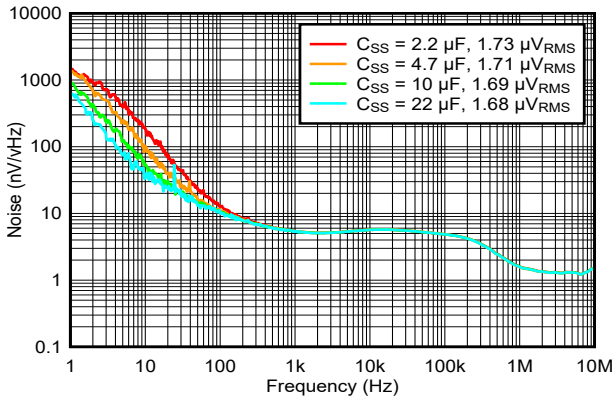


Figure 6-15. Output Noise vs Frequency Across C_{SS} (Noise Spectral Density)

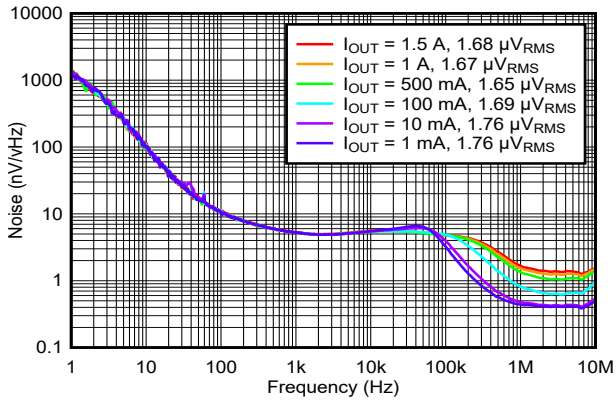
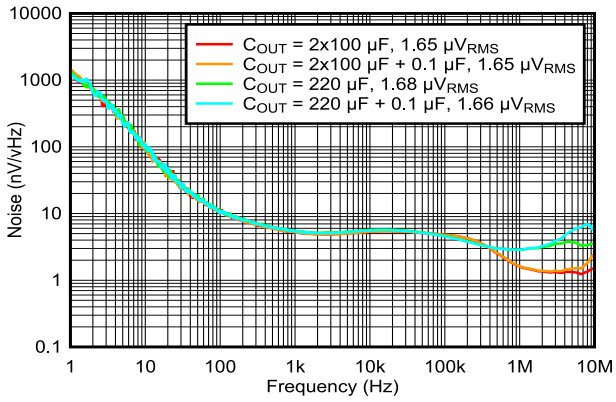
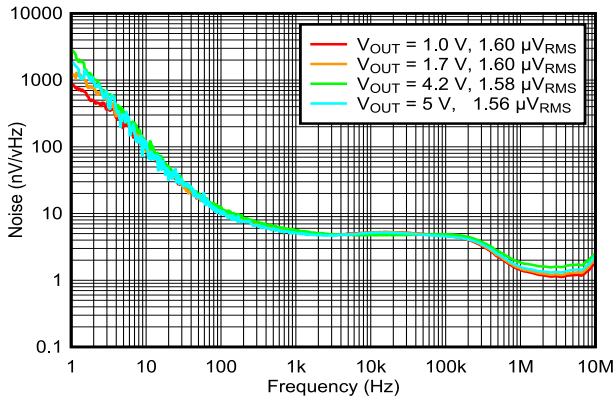


Figure 6-16. Output Noise vs Frequency Across Output Current (Noise Spectral Density)



See Table 9-4 for capacitor part numbers utilized.

Figure 6-17. Output Noise vs Frequency Across Output Capacitor (Noise Spectral Density)



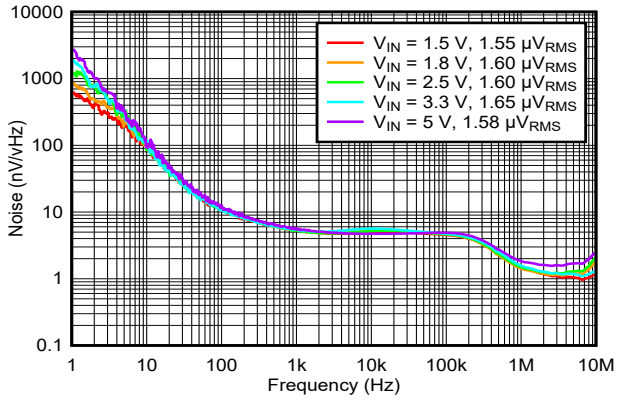
V_{IN} = V_{OUT} + 0.8 V

Figure 6-18. Output Noise vs Frequency Across Output Voltage (Noise Spectral Density)

Copyright © 2023 Texas Instruments Incorporated

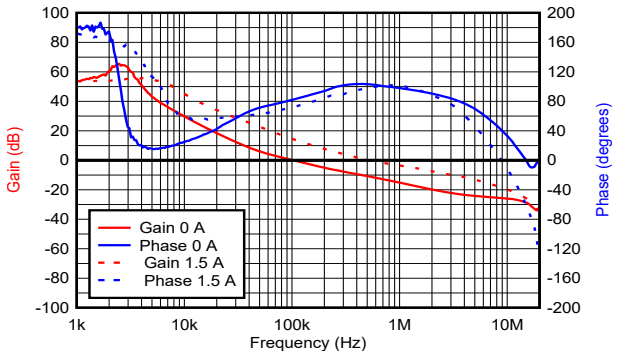
6.7 Typical Characteristics

V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{OUT} = 2 × 100 µF, C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, unless otherwise noted, integrated noise reported with 10-Hz to 100-kHz bandwidth.



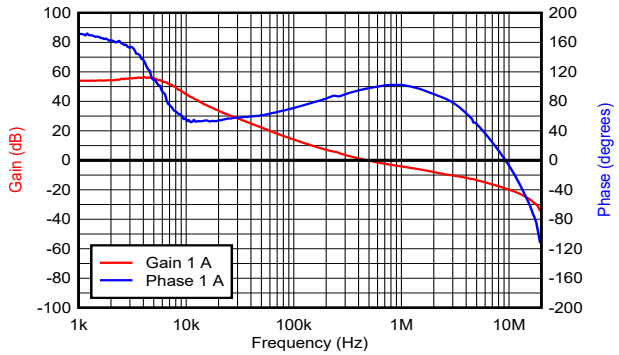
$V_{OUT} = V_{IN} – 0.8$ V

Figure 6-19. Output Noise vs Frequency Across Input Voltage (Noise Spectral Density)



C_{OUT} = 2 × 100 µF. See Table 9-4 for capacitors utilized and information on ceramic and plastic package differences.
I_{OUT} = 0 A: Phase Margin = 83°, Gain Margin = 29 dB
I_{OUT} = 1.5 A: Phase Margin = 99°, Gain Margin = 19 dB

Figure 6-20. Gain and Phase vs Frequency (Bode Plot)

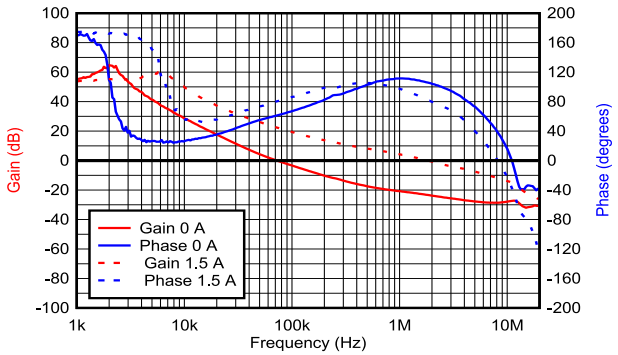


C_{OUT} = 2 × 100 µF. See Table 9-4 for capacitors utilized and information on ceramic and plastic package differences.
Phase Margin = 98°, Gain Margin = 19 dB

Figure 6-21. Gain and Phase vs Frequency (Bode Plot)

6.7 Typical Characteristics (continued)

V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{OUT} = 2 × 100 µF, C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, unless otherwise noted, integrated noise reported with 10-Hz to 100-kHz bandwidth.

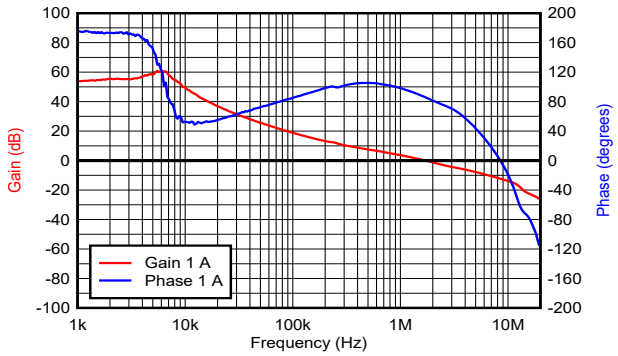


C_{OUT} = 2 × 100 µF + 0.1 µF. See Table 9-4 for capacitors utilized and information on ceramic and plastic package differences.

I_{OUT} = 0 A: Phase Margin = 61°, Gain Margin = 27 dB

I_{OUT} = 1.5 A: Phase Margin = 99°, Gain Margin = 12 dB

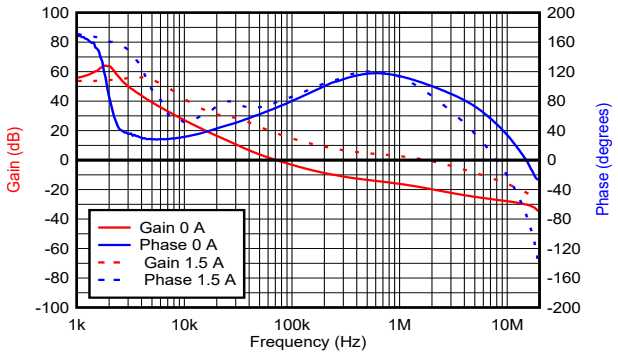
Figure 6-22. Gain and Phase vs Frequency (Bode Plot)



C_{OUT} = 2 × 100 µF + 0.1 µF. See Table 9-4 for capacitors utilized and information on ceramic and plastic package differences.

Phase Margin = 98°, Gain Margin = 13 dB

Figure 6-23. Gain and Phase vs Frequency (Bode Plot)

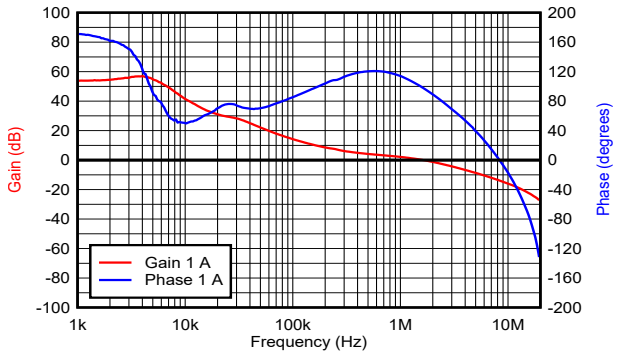


C_{OUT} = 1 × 220 µF. See Table 9-4 for capacitors utilized and information on ceramic and plastic package differences.

I_{OUT} = 0 A: Phase Margin = 71°, Gain Margin = 30 dB

I_{OUT} = 1.5 A: Phase Margin = 91°, Gain Margin = 14 dB

Figure 6-24. Gain and Phase vs Frequency (Bode Plot)



C_{OUT} = 1 × 220 µF. See Table 9-4 for capacitors utilized and information on ceramic and plastic package differences.

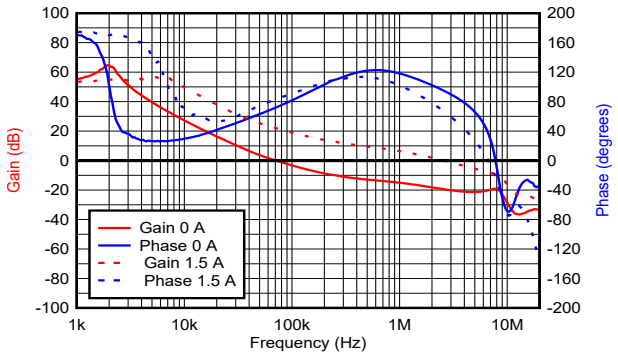
Phase Margin = 98°, Gain Margin = 14 dB

Figure 6-25. Gain and Phase vs Frequency (Bode Plot)

Copyright © 2023 Texas Instruments Incorporated

6.7 Typical Characteristics (continued)

V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{OUT} = 2 × 100 µF, C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, unless otherwise noted, integrated noise reported with 10-Hz to 100-kHz bandwidth.

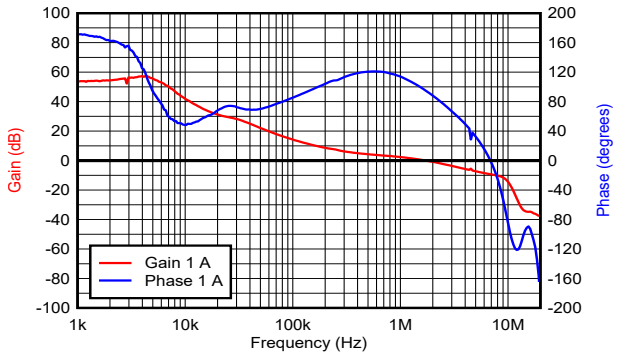


C_{OUT} = 1 × 220 µF + 0.1 µF. See Table 9-4 for capacitors utilized and information on ceramic and plastic package differences.

I_{OUT} = 0 A: Phase Margin = 72°, Gain Margin = 19 dB

I_{OUT} = 1.5 A: Phase Margin = 66°, Gain Margin = 8 dB

Figure 6-26. Gain and Phase vs Frequency (Bode Plot)



C_{OUT} = 1 × 220 µF + 0.1 µF. See Table 9-4 for capacitors utilized and information on ceramic and plastic package differences.

Phase Margin = 94°, Gain Margin = 9 dB

Figure 6-27. Gain and Phase vs Frequency (Bode Plot)

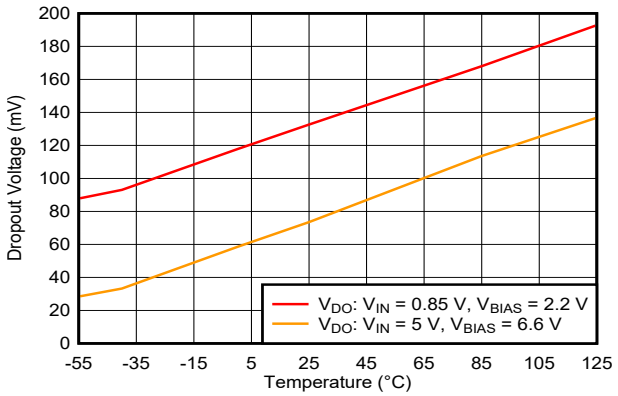
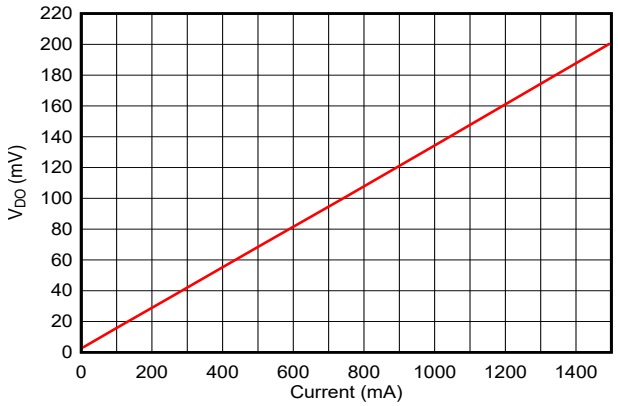


Figure 6-28. Dropout Voltage vs Temperature



V_{IN} = 5 V

V_{BIAS} = V_{IN} + 1.6 V

Figure 6-29. Dropout Voltage vs Current

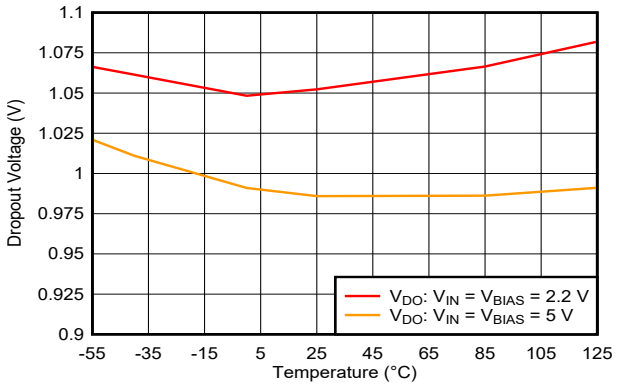


Figure 6-30. Dropout Voltage vs Temperature Without Separate V_{BIAS}

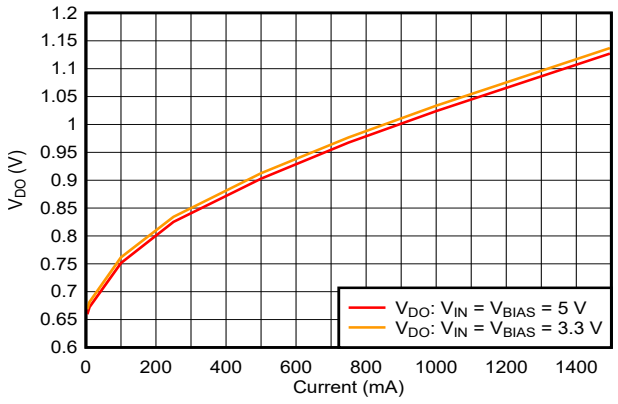
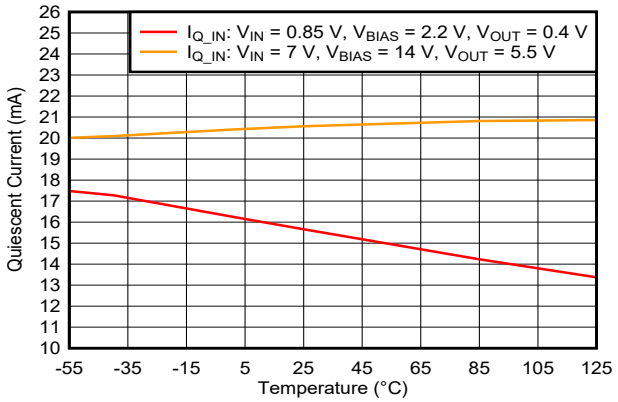


Figure 6-31. Dropout Voltage vs Current Without Separate V_{BIAS}

Copyright © 2023 Texas Instruments Incorporated

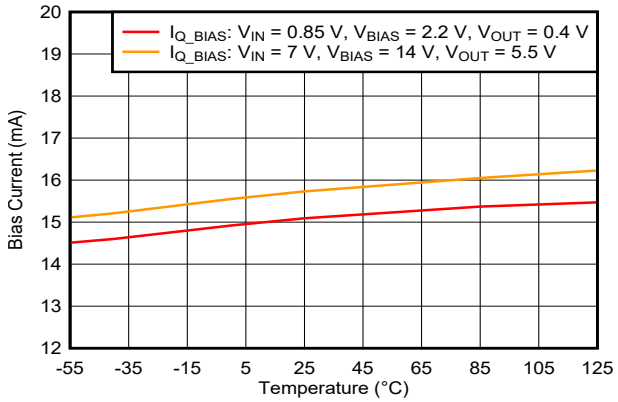
6.7 Typical Characteristics (continued)

V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{OUT} = 2 × 100 µF, C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, unless otherwise noted, integrated noise reported with 10-Hz to 100-kHz bandwidth.



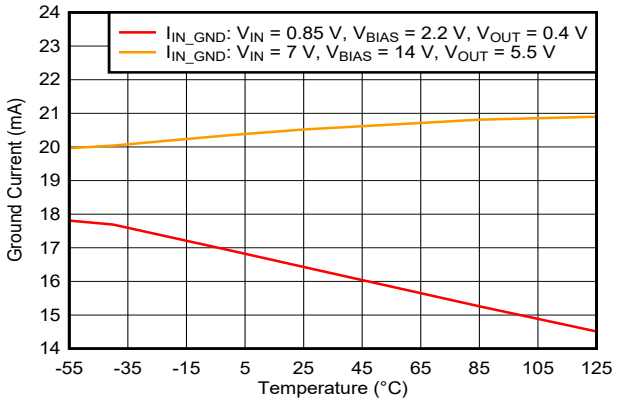
I_{OUT} = 0 A

Figure 6-32. Quiescent Current vs Temperature



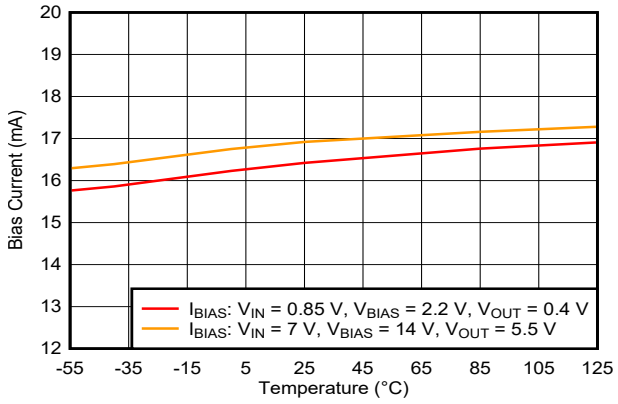
I_{OUT} = 0 A

Figure 6-33. Bias Current vs Temperature



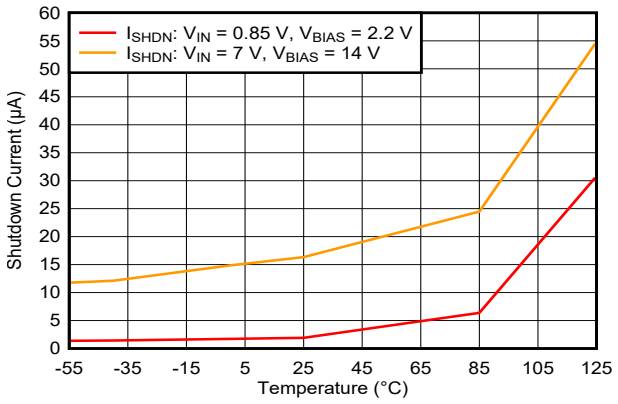
I_{OUT} = 1.5 A

Figure 6-34. Ground Current vs Temperature



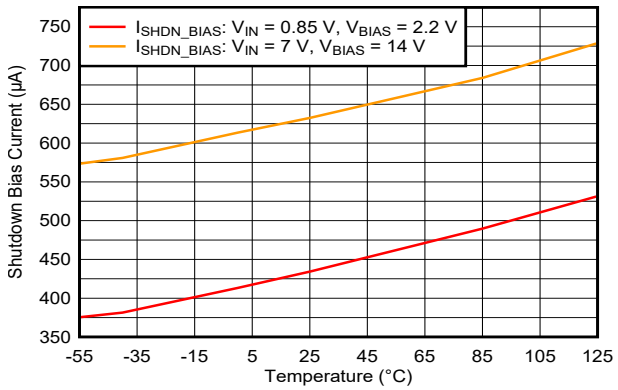
I_{OUT} = 1.5 A

Figure 6-35. Bias Current vs Temperature



V_{EN} = 0 V

Figure 6-36. Shutdown Current vs Temperature



V_{EN} = 0 V

Figure 6-37. Bias Shutdown Current vs Temperature

Copyright © 2023 Texas Instruments Incorporated

6.7 Typical Characteristics (continued)

V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{OUT} = 2 × 100 µF, C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, unless otherwise noted, integrated noise reported with 10-Hz to 100-kHz bandwidth.

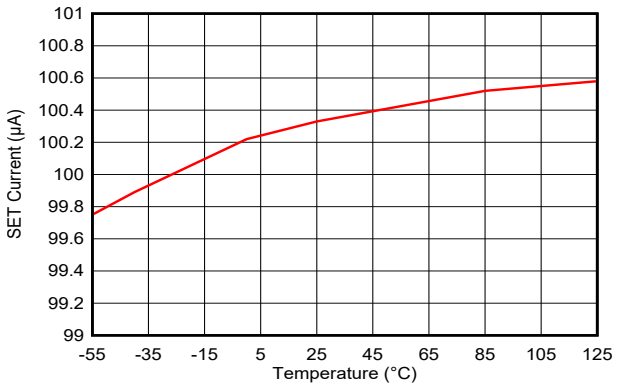
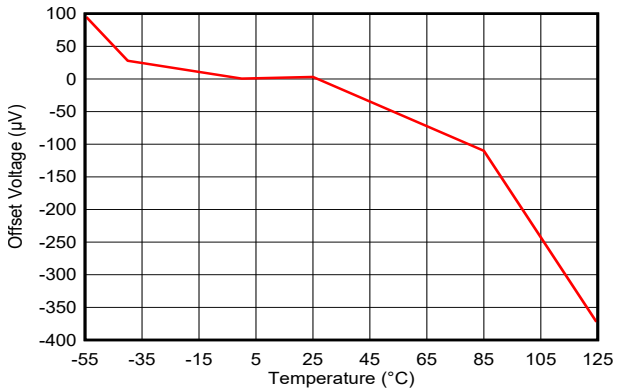


Figure 6-38. SET Pin Current vs Temperature



I_{OUT} = 1 mA

Figure 6-39. Offset Voltage vs Temperature

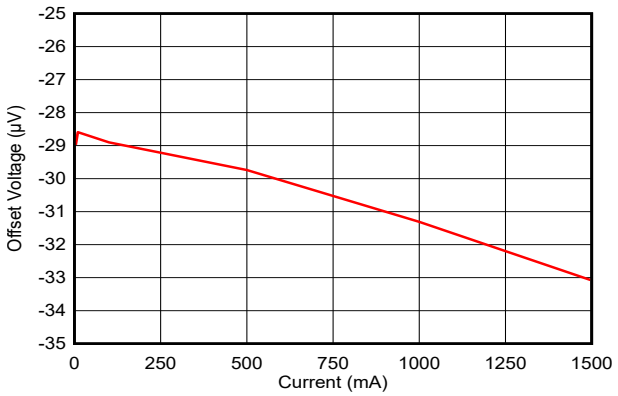


Figure 6-40. Offset Voltage vs Current

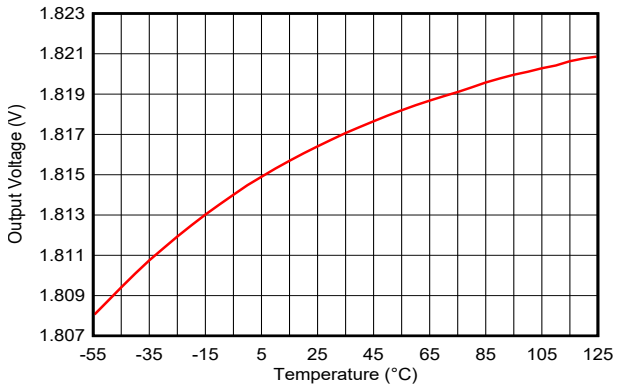
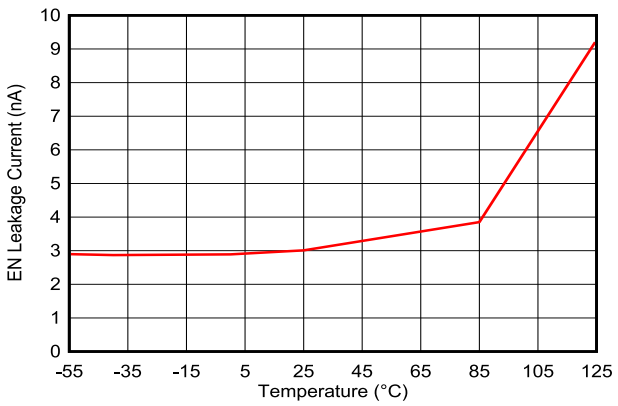
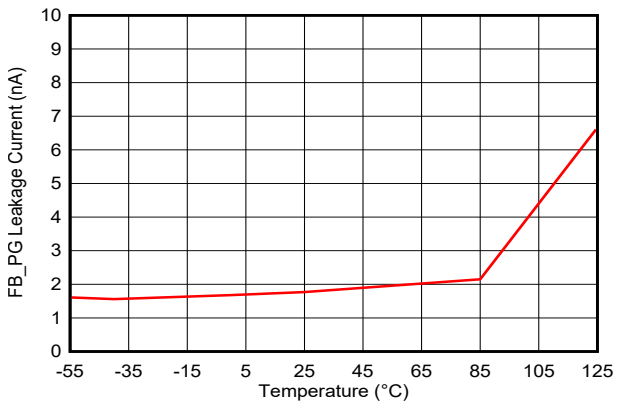


Figure 6-41. Output Voltage vs Temperature



V_{EN} = 7 V V_{IN} = 7 V V_{BIAS} = 14 V

Figure 6-42. Enable Leakage Current vs Temperature



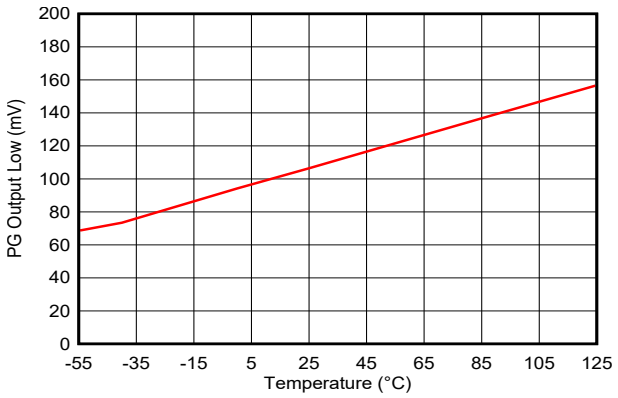
V_{FB_PG} = 6 V V_{IN} = 7 V V_{BIAS} = 14 V
I_{OUT} = 1 mA

Figure 6-43. FB_PG Pin Leakage Current vs Temperature

Copyright © 2023 Texas Instruments Incorporated

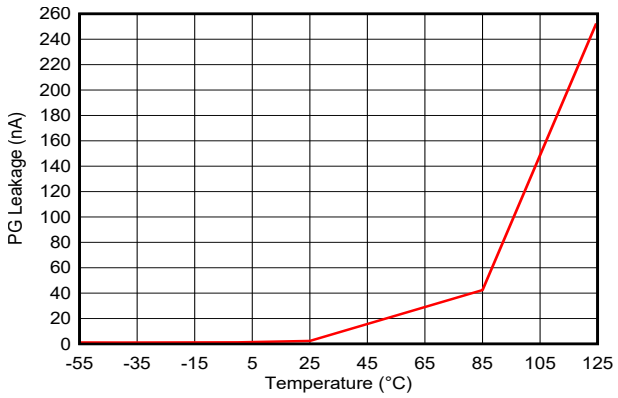
6.7 Typical Characteristics (continued)

V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{OUT} = 2 × 100 µF, C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, unless otherwise noted, integrated noise reported with 10-Hz to 100-kHz bandwidth.



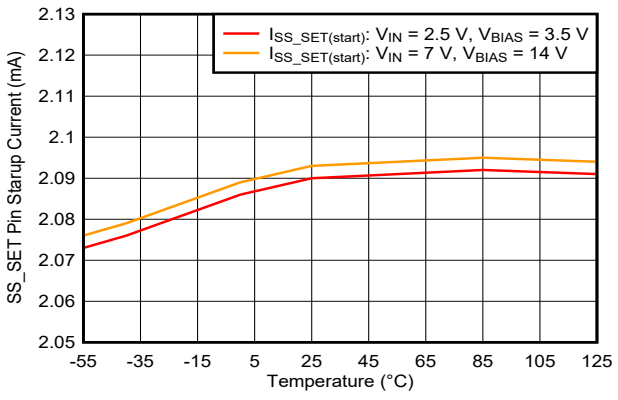
V_{IN} = 0.85 V V_{BIAS} = 2.2 V I_{OUT} = 1 mA
I_{PG} = 2 mA

Figure 6-44. PG Pin Output Low vs Temperature



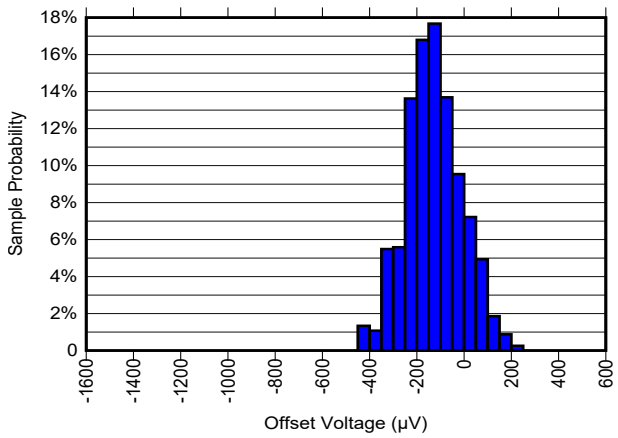
V_{IN} = 7 V V_{BIAS} = 14 V I_{OUT} = 1 mA
V_{PG} = 7 V

Figure 6-45. PG Pin Leakage vs Temperature



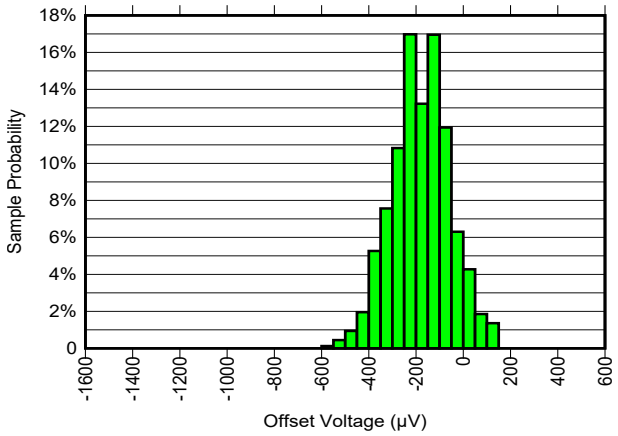
I_{OUT} = 0 mA

Figure 6-46. SS_SET Pin Current During Startup vs Temperature



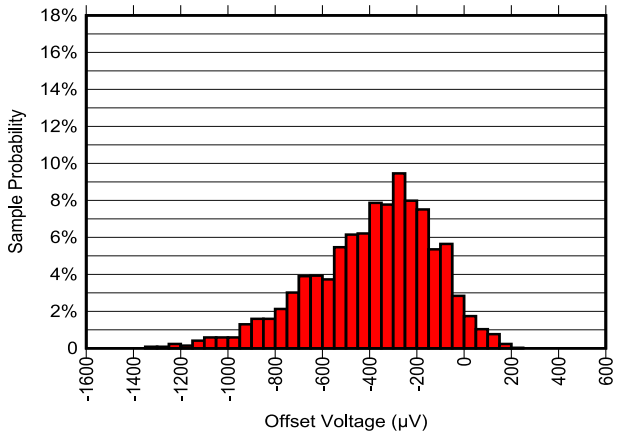
0.85 V ≤ V_{IN} ≤ 7 V, 2.2 V ≤ V_{BIAS} ≤ 14 V, I_{OUT} = 1 mA

Figure 6-47. Output Offset Voltage Distribution at T_A = –55°C



0.85 V ≤ V_{IN} ≤ 7 V, 2.2 V ≤ V_{BIAS} ≤ 14 V, I_{OUT} = 1 mA

Figure 6-48. Output Offset Voltage Distribution at T_A = 25°C



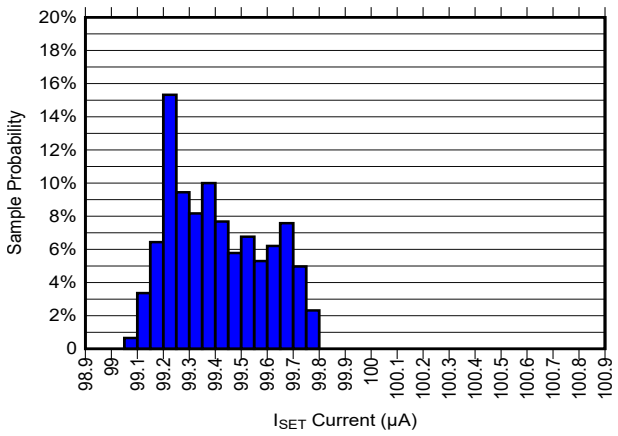
0.85 V ≤ V_{IN} ≤ 7 V, 2.2 V ≤ V_{BIAS} ≤ 14 V, I_{OUT} = 1 mA

Figure 6-49. Output Offset Voltage Distribution at T_A = 125°C

Copyright © 2023 Texas Instruments Incorporated

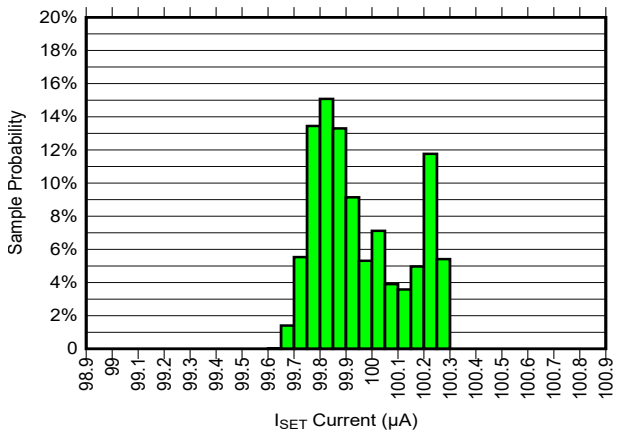
6.7 Typical Characteristics (continued)

V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{OUT} = 2 × 100 µF, C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, unless otherwise noted, integrated noise reported with 10-Hz to 100-kHz bandwidth.



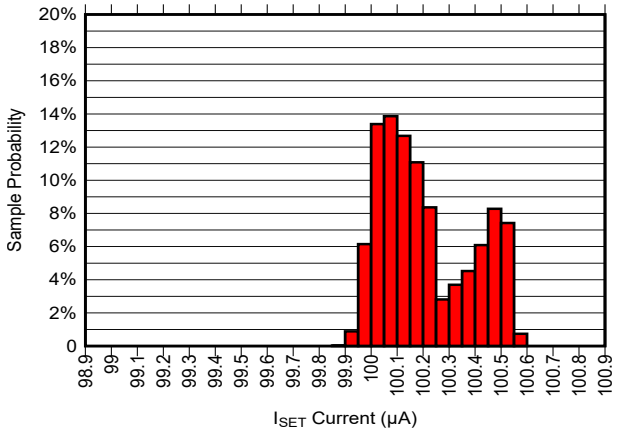
0.85 V ≤ V_{IN} ≤ 7 V, 2.2 V ≤ V_{BIAS} ≤ 14 V, I_{OUT} = 1 mA

Figure 6-50. I_{SET} Current Distribution at T_A = –55°C



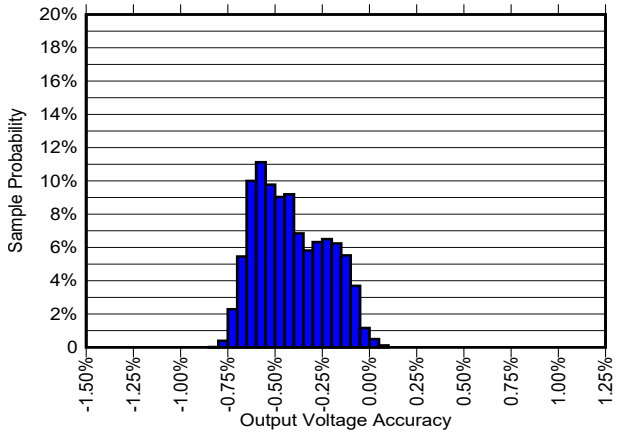
0.85 V ≤ V_{IN} ≤ 7 V, 2.2 V ≤ V_{BIAS} ≤ 14 V, I_{OUT} = 1 mA

Figure 6-51. I_{SET} Current Distribution at T_A = 25°C



0.85 V ≤ V_{IN} ≤ 7 V, 2.2 V ≤ V_{BIAS} ≤ 14 V, I_{OUT} = 1 mA

Figure 6-52. I_{SET} Current Distribution at T_A = 125°C



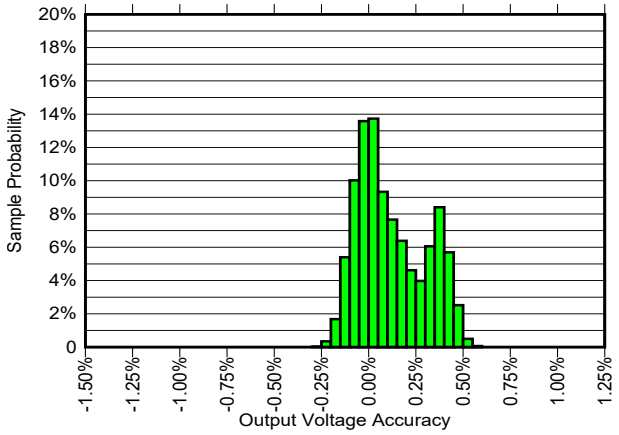
0.85 V ≤ V_{IN} ≤ 7 V, 1 mA ≤ I_{OUT} ≤ 1.5 A, 2.2 V ≤ V_{BIAS} ≤ 14 V, P_D ≤ 4 W

Figure 6-53. Output Voltage Accuracy Distribution at T_A = –55°C

Copyright © 2023 Texas Instruments Incorporated

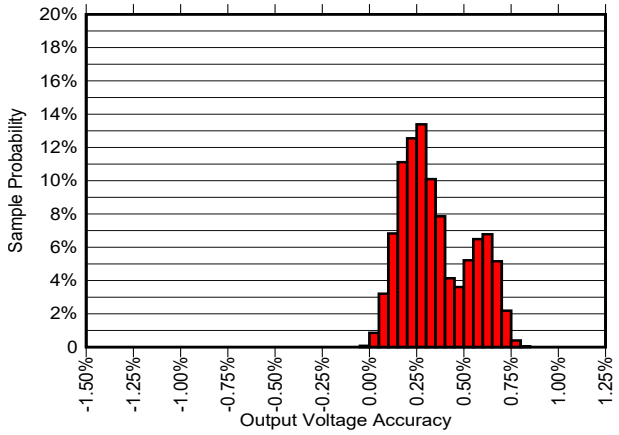
6.7 Typical Characteristics (continued)

V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{OUT} = 2 × 100 µF, C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, unless otherwise noted, integrated noise reported with 10-Hz to 100-kHz bandwidth.



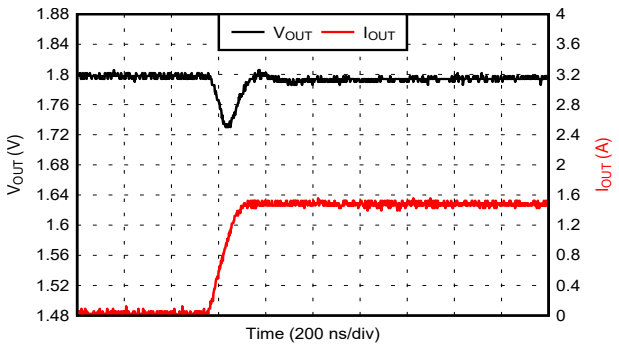
0.85 V ≤ V_{IN} ≤ 7 V, 1 mA ≤ I_{OUT} ≤ 1.5 A, 2.2 V ≤ V_{BIAS} ≤ 14 V, P_D ≤ 4 W

Figure 6-54. Output Voltage Accuracy Distribution at T_A = 25°C



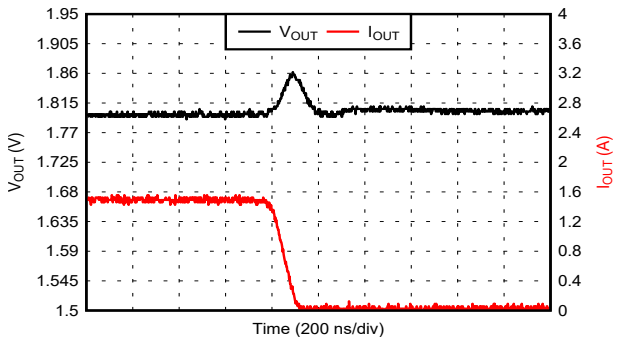
0.85 V ≤ V_{IN} ≤ 7 V, 1 mA ≤ I_{OUT} ≤ 1.5 A, 2.2 V ≤ V_{BIAS} ≤ 14 V, P_D ≤ 4 W

Figure 6-55. Output Voltage Accuracy Distribution at T_A = 125°C



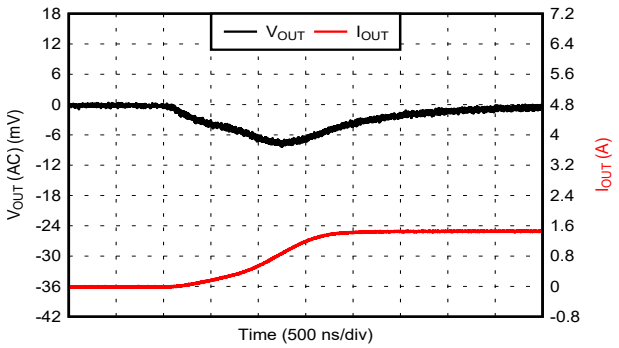
Slew Rate = 10.1 A/µs

Figure 6-56. Load Step: 1 mA to 1.5 A



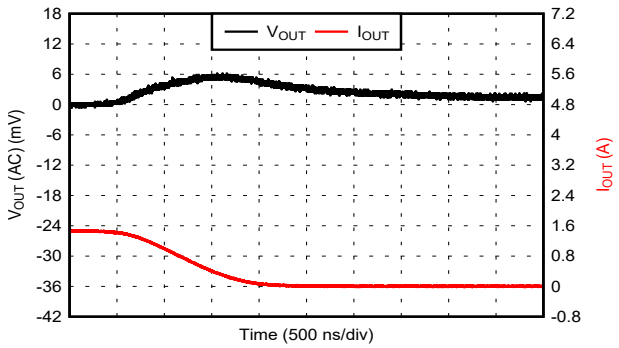
Slew Rate = 13.1 A/µs

Figure 6-57. Load Step: 1.5 A to 1 mA



Slew Rate = 0.9 A/µs

Figure 6-58. Load Step: 1 mA to 1.5 A



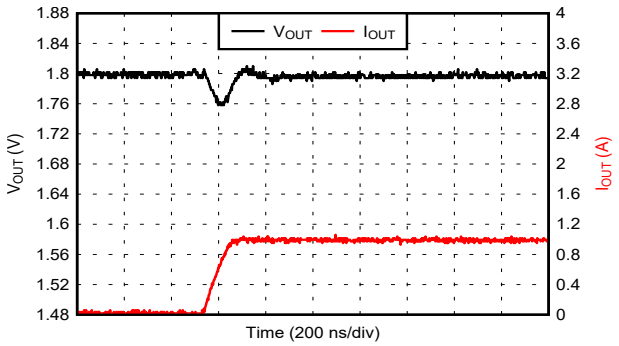
Slew Rate = 1.0 A/µs

Figure 6-59. Load Step: 1.5 A to 1 mA

Copyright © 2023 Texas Instruments Incorporated

6.7 Typical Characteristics (continued)

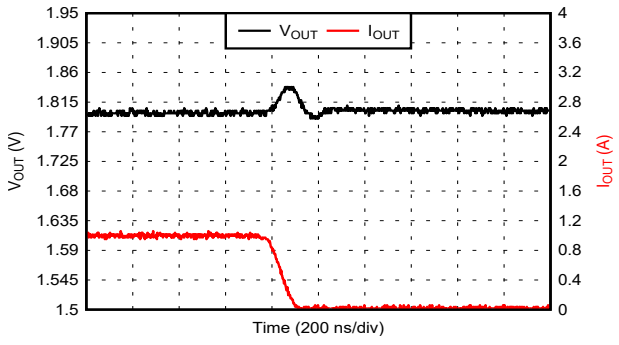
V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{OUT} = 2 × 100 µF, C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, unless otherwise noted, integrated noise reported with 10-Hz to 100-kHz bandwidth.



Slew Rate = 8.5 A/µs

I_{OUT} is only the stepped current, parallel 0.5 A load not shown

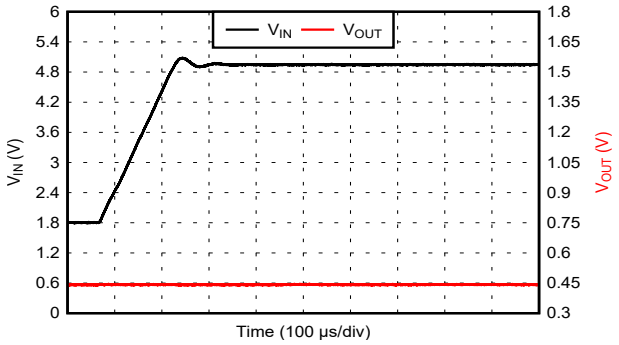
Figure 6-60. Load Step: 0.5 A to 1.5 A



Slew Rate = 8.1 A/µs

I_{OUT} is only the stepped current, parallel 0.5 A load not shown

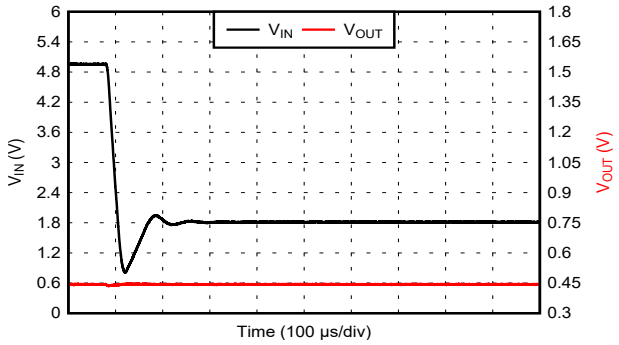
Figure 6-61. Load Step: 1.5 A to 0.5 A



Slew Rate = 20.2 V/ms

V_{OUT} = 0.4 V

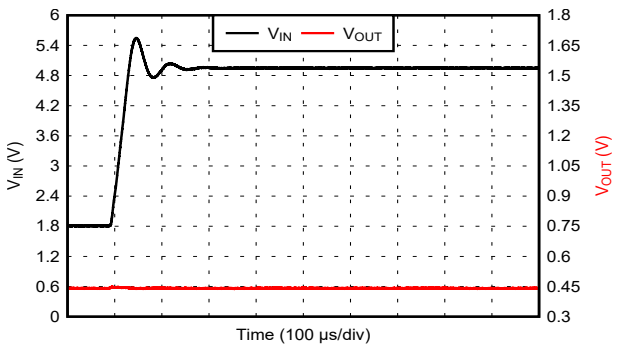
Figure 6-62. Line Step: 1.8 V to 5 V With I_{OUT} = 1.5 A



Slew Rate = 144.8 V/ms

V_{OUT} = 0.4 V

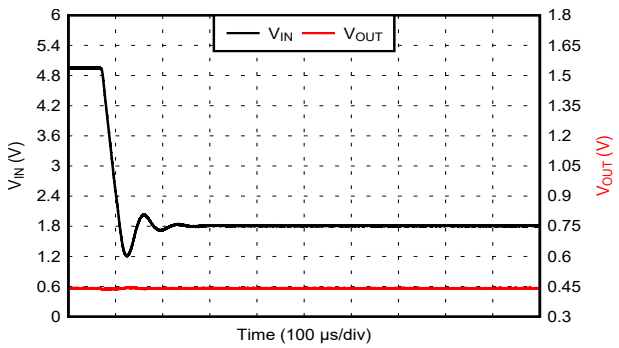
Figure 6-63. Line Step: 5 V to 1.8 V With I_{OUT} = 1.5 A



Slew Rate = 84.0 V/ms

V_{OUT} = 0.4 V

Figure 6-64. Line Step: 1.8 V to 5 V With I_{OUT} = 1 mA



Slew Rate = 85.1 V/ms

V_{OUT} = 0.4 V

Figure 6-65. Line Step: 5 V to 1.8 V With I_{OUT} = 1 mA

Copyright © 2023 Texas Instruments Incorporated

6.7 Typical Characteristics (continued)

V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, C_{OUT} = 2 × 100 µF, C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, unless otherwise noted, integrated noise reported with 10-Hz to 100-kHz bandwidth.

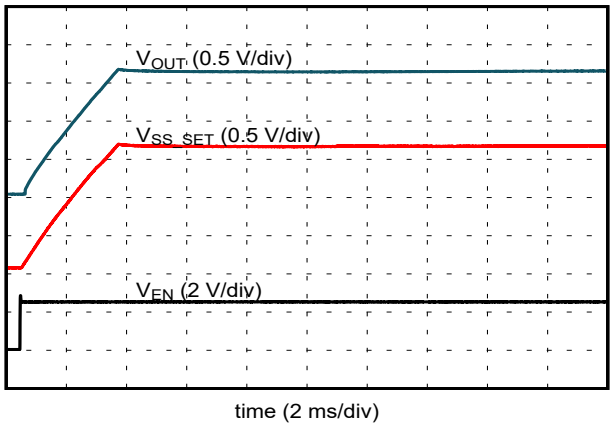
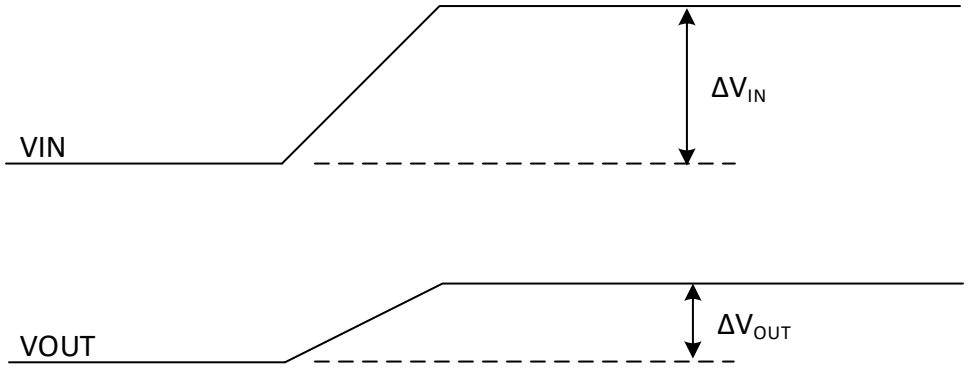


Figure 6-66. Startup Waveform

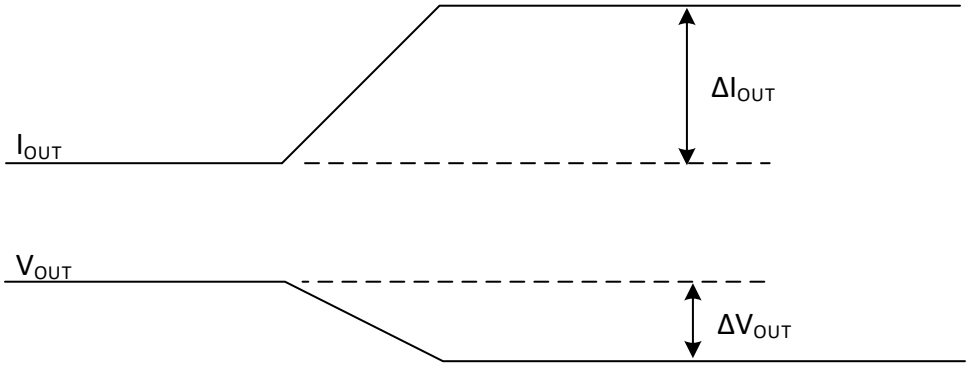
Copyright © 2023 Texas Instruments Incorporated

7 Parameter Measurement Information



A. ΔV_{OUT} / ΔV_{IN} = 3 µV/V (typ). This means for a 1 V change in V_{IN} (ΔV_{IN} = 1 V), there will be a 3 µV change in V_{OUT} (ΔV_{OUT} = 3 µV). Line regulation is a DC parameter; therefore this waveform should only be considered valid after transients die out or for a slow V_{IN} slew rate.

Figure 7-1. Line Regulation



A. ΔV_{OUT} / ΔI_{OUT} = 500 µV/A (typ). This means for a 1 A change in I_{OUT} (ΔI_{OUT} = 1 A), there will be a 500 µV change in V_{OUT} (ΔV_{OUT} = 500 µV). Load regulation is a DC parameter; therefore this waveform should only be considered valid after transients die out or for a slow I_{OUT} slew rate.

Figure 7-2. Load Regulation

Copyright © 2023 Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

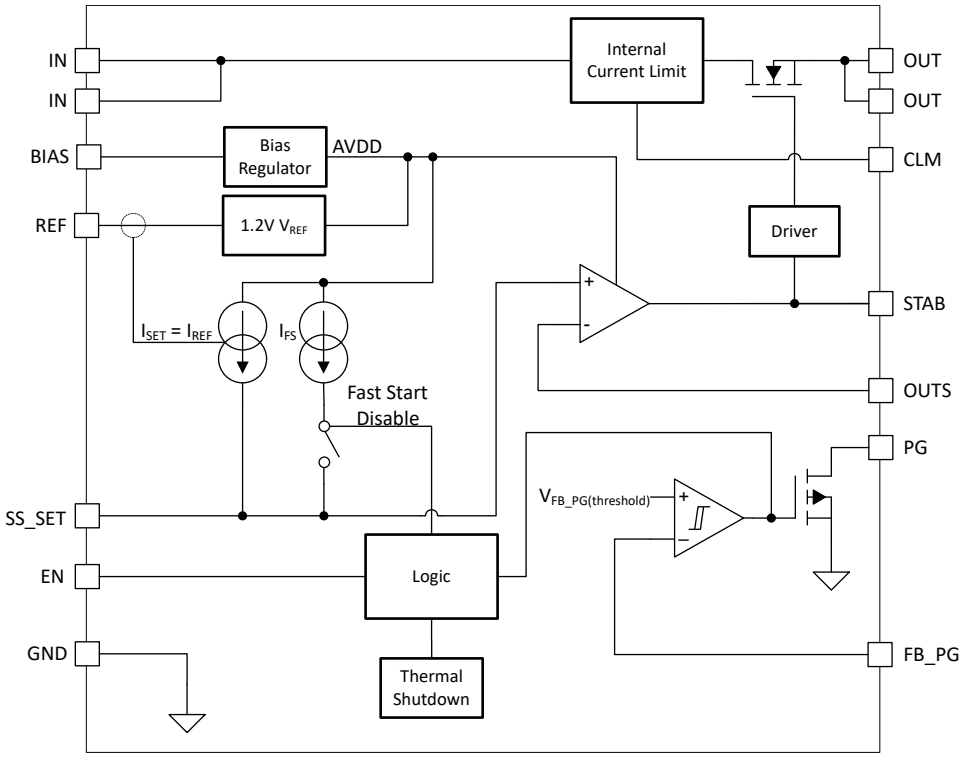
The TPS7H1111 (TPS7H1111-SP and TPS7H1111-SEP) is an ultra-low noise, high PSRR, low dropout linear regulator (LDO) optimized for powering RF devices in space. It uses an NMOS pass element and is capable of sourcing up to 1.5 A over a 0.85-V to 7-V input range. A BIAS pin (2.2 V to 14 V) enables the use of a bias rail to facilitate low V_{IN} to V_{OUT} operation, thus limiting power dissipation. The device creates an ultra-clean output rail and can be configured with minimal external components.

The radiation performance, combined with low-noise and high-PSRR operation, makes the TPS7H1111 ideal for powering noise-sensitive components in satellites. The high performance of the device limits power-supply generated phase noise and clock jitter, making this device ideal for powering high-performance ADCs, DACs, VCOs, PLLs, SerDes, and other RF components.

For digital loads, such as ASICs (application specific integrated circuits), FPGAs, and DSPs, requiring low-input voltage and low-output voltage operation, the exceptional accuracy (+1.2% / –1.3% over line, load, and temperature), remote sensing, excellent transient performance, and soft-start capabilities of the TPS7H1111 ensure optimal system performance.

Additionally, various features are incorporated into the regulator to simplify the electrical system and provide system flexibility. These features include enable functionality (EN), configurable power good output (PG), soft-start control (SS_SET), an internal current limit with configurable behavior (CLM), and external loop compensation (STAB).

8.2 Functional Block Diagram



Copyright © 2023 Texas Instruments Incorporated

8.3 Feature Description

8.3.1 Bias Supply

A bias supply connected to the BIAS pin is required for proper device operation. Depending on the headroom voltage and output current conditions, the bias supply voltage may be the same as the input voltage supply, or it may be a separate higher voltage supply. Note that headroom voltage is defined as the delta between the operating V_{IN} and V_{OUT} conditions ($V_{headroom} = V_{IN} – V_{OUT}$). In all cases, there are no sequencing requirements between V_{BIAS} and V_{IN}.

As described in Table 8-1, if the headroom voltage is greater than or equal to 1.6 V, no separate higher bias supply is required. If the headroom voltage is less than 1.6 V, a separate higher bias supply voltage is required for full performance. In all situations shown in Table 8-1 it is possible to achieve the full 1.5 A of output current with the specified dropout voltage (see the Electrical Characteristics table).

Table 8-1. Bias Rail Requirements for Full Performance Operation

Headroom (V_{IN} - V_{OUT})	Bias Requirement(1)
≥ 1.6 V	Use the same voltage rail as V_{IN} or any $V_{BIAS} \geq V_{IN}$
< 1.6 V	Use a separate voltage rail than V_{IN} where $V_{BIAS} \geq V_{OUT}$ + 1.6 V

(1) In all cases 2.2 V ≤ V_{BIAS} ≤ 14 V

Table 8-2 shows examples of supported V_{BIAS}, V_{IN}, and V_{OUT} combinations that can be achieved with standard voltage rails and result in full 1.5 A output current support. As can be seen, a 12 V bias supply will support all listed standard output voltage rails (generally a 5 V supply will also suffice). Also note that for the conditions where the V_{BIAS} and V_{IN} voltages are the same, a separate supply is not required.

Table 8-2. Bias Rail Standard Rail Examples for Full Performance Operation

V_{BIAS} (V)	V_{IN} (V)	V_{OUT} (V)
12	5	3.3
	5, 3.3	2.5
	5, 3.3, 2.5	1.8
	5, 3.3, 2.5, 1.8	1.1
5	5, 3.3	2.5
	5, 3.3, 2.5	1.8
	5, 3.3, 2.5, 1.8	1.1
3.3	3.3, 2.5, 1.8	1.1

While it is generally recommended to follow the above bias voltage requirements, sometimes it is not feasible (for example, if the headroom is small and a separate bias voltage rail is not available). In this case, it is still possible to operate the TPS7H1111 at the expense of reduced output current (and possibly reduced performance such as PSRR). This condition (where $V_{BIAS} = V_{IN}$ and headroom is small) is specified as *Dropout voltage with* $V_{BIAS} = V_{IN}$ in the Electrical Characteristics table. By meeting the resulting dropout voltage requirements, the part maintains proper operation.

An example of a supported combination that may not result in full performance capabilities is with $V_{BIAS} = V_{IN}$ = 5 V and V_{OUT} = 3.3 V. Assuming the 5 V rail has a 5% tolerance and the 3.3 V output has a specified maximum tolerance of +1.2% tolerance, the worst case headroom is $V_{headroom}$ = 4.75 - 3.34 = 1.41 V. This 1.41 V is less than the 1.6 V recommended. However, as shown in the Electrical Characteristics table, this headroom is greater than the dropout required at the full load current of 1.5 A. Therefore, it is expected that the full current will be supported, but other parameters may not be at full performance (such as PSRR).

Any noise on the bias rail will be attenuated by the $PSRR_{BIAS}$ specification before being coupled to the output. Unless the bias rail is an ultra-clean rail, this noise coupling would be the limiting factor in creating a clean output voltage. Therefore, an RC filter should be used to minimize noise input to the BIAS pin. This is feasible

Copyright © 2023 Texas Instruments Incorporated

due to the low current requirements of the BIAS pin. A 10 Ω and 4.7 µF is generally sufficient to ensure the noise propagated from the BIAS pin to the output voltage is minimized. The selected resistor value must be low enough to ensure the resulting IR drop doesn't cause the bias voltage to become too low for proper operation.

8.3.2 Output Voltage Configuration

The output voltage of the TPS7H1111 is set by placing a resistor, R_{SET}, from the SS_SET pin to GND. During nominal operation, 100 µA is output from the SS_SET pin. By appropriately selecting R_{SET}, the desired output voltage will be generated on the SS_SET pin as calculated in Equation 1. This voltage will be replicated on the output through the internal unity gain error amplifier as shown in Figure 8-1.

$$V_{SS_SET} = I_{SET} \times R_{SET} \quad (1)$$

where

- I_{SET} = 100 µA (typ)
- V_{SS_SET} = set voltage that is configured to the desired output voltage, V_{OUT}

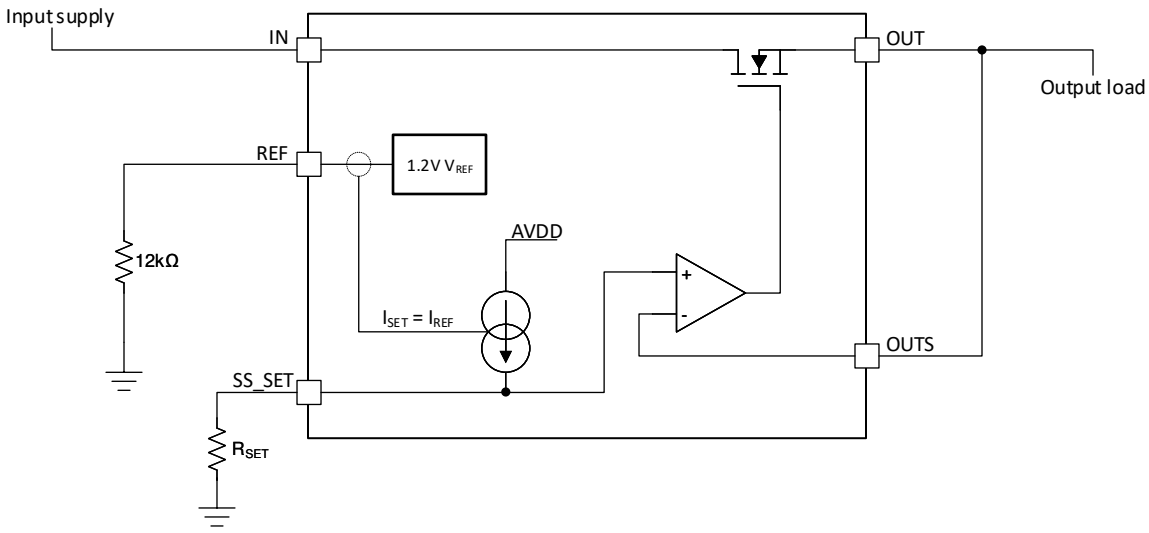


Figure 8-1. Simplified Schematic to Configure Output Voltage

The 100 µA reference current is configured by placing a 12 kΩ resistor from the REF pin to GND. The 1.2 V across the R_{REF} resistor will create an approximate 100 µA reference current. This current is mirrored to the SS_SET pin to create a highly accurate reference current. Generally 0.1% precision resistors are recommended for R_{REF} and R_{SET} to precisely set the currents. If precision 0.1% resistors are utilized, the I_{SS_SET} error due to the R_{REF} resistor will be 0.1%. Additionally, the 0.1% error of the R_{SET} resistor will also contribute to V_{OUT} accuracy error. The TPS7H1111 accuracy specification is +1.2% / –1.3% across line, load, and temperature, but resistor tolerance error must be separately added. Common output voltages and resistor values are shown in Table 8-3.

Copyright © 2023 Texas Instruments Incorporated

Table 8-3. R_{SET} Values for Indicated V_{OUT}

Output Voltage, V_{OUT}	Value for 0.1% Tolerance Resistors
0.4 V	4.02 kΩ
0.7 V	6.98 kΩ
1 V	10 kΩ
1.1 V	11 kΩ
1.2 V	12 kΩ
1.5 V	15 kΩ
1.8 V	18 kΩ
2.5 V	24.9 kΩ
3.3 V	33.2 kΩ
4 V	40.2 kΩ
5 V	49.9 kΩ

Additionally, if greater accuracy is desired, matched resistors may be utilized (which are often available in accuracy ratios better than 0.1%). For example, a nominal 12 kΩ ± 5% resistor could be selected for R_{REF} with a matched resistor so that the that R_{SET} / R_{REF} ratio is 0.01% (or even better). In this case, instead of Equation 1 to calculate the set voltage, use Equation 2.

$$V_{SS_SET} = (1.2 / R_{REF}) \times R_{SET} \quad (2)$$

where

- V_{SS_SET} = set voltage that is set to the desired output voltage, V_{OUT}

Equation 2 allows one to easily calculate errors in the set output voltage due to R_{REF} and R_{SET} resistor mismatch. However, while improved resistor ratios will likely improve the output accuracy, other error sources are still present. These sources include the inherent reference current accuracy itself and error amplifier offset voltage.

The output voltage accuracy, V_{ACC}, specifies a minimum accuracy of –1.3% and maximum accuracy of +1.2% in the Electrical Characteristics table. This specification applies across the complete temperature range of –55°C to 125°C, across all the input voltages (0.85 V ≤ V_{IN} ≤ 7 V and 2.2 V ≤ V_{BIAS} ≤ 14 V), and up to full load (1 mA ≤ I_{OUT} ≤ 1.5 A). A few additional details to the measurement are noted:

- The range of V_{IN}, V_{BIAS}, I_{OUT}, and temperature mean the specification applies across all line, load, and temperature combinations. This is accomplished by testing multiple bias conditions that cover various corners.
- Footnote 4 in the Electrical Characteristics specifies $V_{BIAS} \geq V_{IN}$ *and* $V_{BIAS} \geq V_{OUT} + 1.6$ *V*. This is because not all extreme corners of V_{IN} and V_{BIAS} are feasible (for example, V_{IN} = 7 V and V_{BIAS} = 2.2 V would not make sense).
- Footnote 5 in the Electrical Characteristics specifies that the measurement is done with a power dissipation that is limited to a maximum of 4 W. This is due to tester thermal limitations. On a typical application board with good thermals, there is no inherent limitation.
- The test conditions specify a minimum of 1 mA and not 0 mA for more robust accuracy measurements. However, in a normal application the TPS7H1111 device does not have a minimum load current for stability.
- The post TID specification is measured at room temperature (a MIL standard in order to avoid annealing at high temperatures). The TPS7H1111 is specified post TID to have a minimum accuracy of –0.7% and maximum of +1.1%. This is compared to a pre-TID accuracy of –0.7% and maximum of +0.9%.
- TI does not recommend including the following error terms into the V_{ACC} specification as they are inherently covered in the V_{ACC} parameter itself: I_{SET} current accuracy, V_{OS} (output offset voltage), V_{REF} voltage accuracy, $\Delta V_{OUT}/\Delta V_{IN}$ (line regulation), $\Delta V_{OUT}/\Delta I_{OUT}$ (load regulation), or V_{OUT}tempco.
- The error due to external components, such as R_{REF} and R_{SET} resistor tolerances, may be added to V_{ACC} specifications as this is not included in the parameter.

Copyright © 2023 Texas Instruments Incorporated

For additional information on determining output voltage accuracy, see Section 9.2.1.2.3.

8.3.3 Output Voltage Configuration with a Voltage Source

Since the TPS7H1111 output voltage is equal to the SS_SET voltage (minus any offset error), it is also possible to configure the TPS7H1111 by providing a voltage on SS_SET. As shown in Figure 8-2, a voltage source, V_{SET}, is fed to SS_SET. A DAC can be used as the voltage source to enable a configurable voltage control.

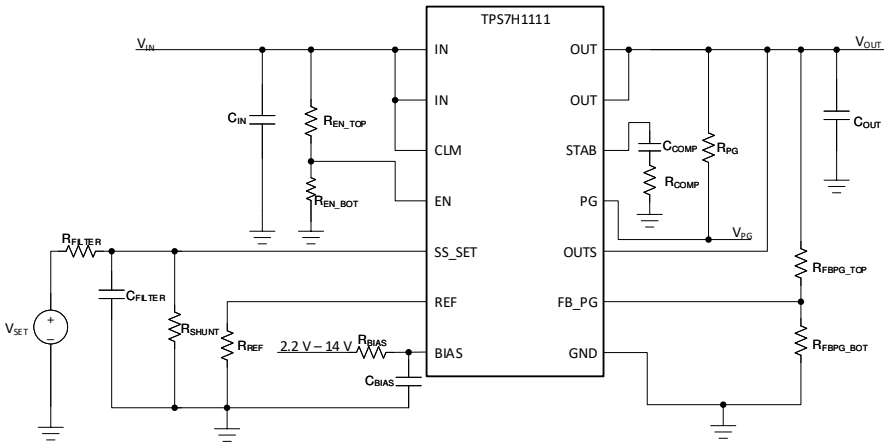


Figure 8-2. Simplified Schematic to Configure Output Voltage with a Voltage Source on SS_SET

A few unique considerations should be taken into account when using this method:

- When a voltage source is provided on SS_SET, instead of relying on the ultra-low noise reference current, the noise of V_{SET} is passed to the output through the unity gain error amplifier. It may be advisable to use an RC filter between V_{SET} and SS_SET as shown to minimize noise.
- Since the TPS7H1111 output voltage directly follows SS_SET, there will be no soft-start during startup. It is recommended to control the V_{SET} voltage slew rate to ensure desired soft-start time. An RC filter between V_{SET} and the SS_SET may help with this slew rate control.
- The SS_SET pin will output a nominal 100 µA during operation and 2.1 mA during "soft-start" (when $V_{FB_PG} < V_{FB_PG(rising)}$). In order to handle this current, a shunt resistor may be required.

8.3.4 Enable

When the enable pin is low, the device will enter shutdown mode and not regulate the output voltage. Normally, an external resistor divider from V_{IN} to GND is used to feed EN. The resistors can be appropriately sized in order to turn on the device when a desired preset input voltage is reached as shown in Equation 3.

$$V_{IN(rising)} = V_{EN(rising)} \times (R_{EN_TOP} + R_{EN_BOT}) / R_{EN_BOT} \quad (3)$$

Similarly, a $V_{IN(falling)}$ voltage can also be calculated using Equation 4. The $V_{IN(rising)}$ and $V_{IN(falling)}$ can be thought of as configurable UVLO (undervoltage-lockout) thresholds.

$$V_{IN(falling)} = V_{EN(falling)} \times (R_{EN_TOP} + R_{EN_BOT}) / R_{EN_BOT} \quad (4)$$

While the TPS7H1111 will turn-on at a V_{EN} of 0.6 V (typ), it is recommended that the final value of V_{EN} is above 0.8 V. This is to ensure appropriate margin above the enable threshold during normal operation to prevent SEFIs during exposure to heavy ions. This recommendation is achieved by satisfying Equation 5.

$$V_{IN(final)} \times R_{EN_BOT} / (R_{EN_TOP} + R_{EN_BOT}) = V_{EN(final)} > 0.8\ V \quad (5)$$

Alternatively, the EN pin may be driven directly from a microcontroller or FPGA. The low voltage threshold of the enable pin aids in support of 1.1-, 1.8-, 2.5-, and 3.3 V logic levels. Similarly it is recommended the final value of V_{EN} is above 0.8 V (this is typically easily achieved with standard logic levels).

Copyright © 2023 Texas Instruments Incorporated

8.3.5 Soft Start and Noise Reduction

In addition to setting the output voltage, the SS_SET pin serves two other important functions: programming the soft start time and creating a noise filter for the internal reference current. In most applications, at least a 4.7 µF capacitor is recommended in order to obtain sufficient low noise performance. Larger value capacitors may be acceptable; however, there are diminishing returns in reduced output noise in capacitor values larger than 4.7µF.

This capacitor also slows down the SS_SET voltage ramp rate, and therefore controls the LDO turn-on time (soft start). However, if the capacitor was only charged by the I_{SET} current (nominally 100 µA), the startup time would be excessive. Therefore, there is an additional fast charge current source (I_{FS} ≈ 2 mA) that is active during startup. Consequently, a 4.7µF capacitor will result in a nominal 3.7 ms soft start time. A simplified diagram of this circuitry is shown in Figure 8-3.

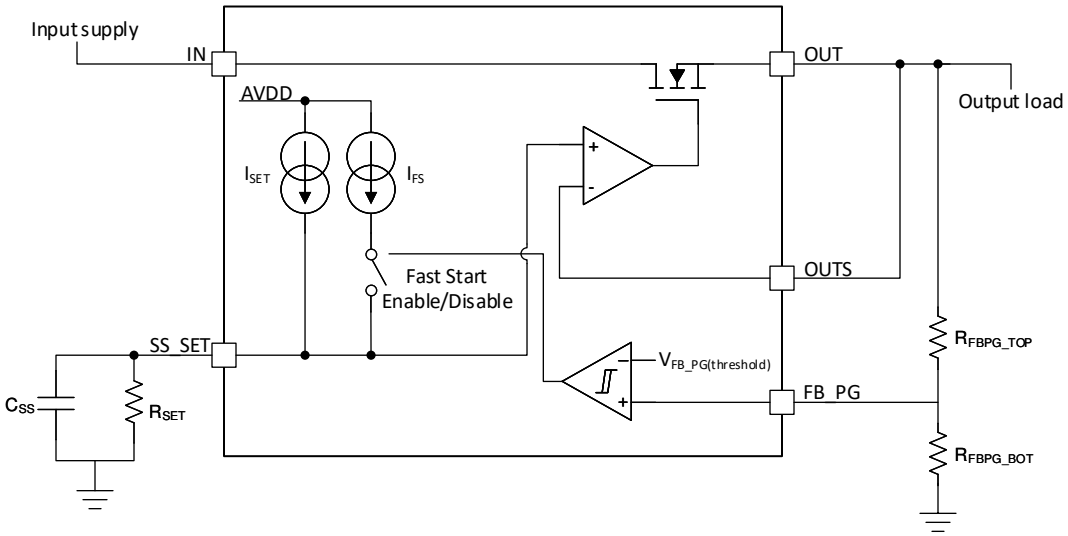


Figure 8-3. Simplified Schematic Showing Startup Circuitry

This fast charge circuitry is active until the FB_PG threshold is reached (typically 300 mV). After the FB_PG threshold has been reached, the fast start current will turn off and the soft start time as shown in Equation 6 will be completed. C_{SS} will continue charging to its final value (as determined by the R_{SET} resistor) with the 100 µA (typ) reference current. An example startup waveform is shown in Figure 8-4. In this waveform it is assumed EN is fed a divided down version of V_{IN}.

$$t_{SS} \approx C_{SS} \times V_{OUT(assert_threshold)} / I_{SS_SET(startup)} \quad (6)$$

where

- t_{SS} = soft start time
- $I_{SS_SET(startup)} = I_{FS} + I_{SET}$ = 2.1 mA (typ)
- $V_{(assert_threshold)}$ = configured value of V_{OUT} for which PG is asserted (typically 90% of $V_{OUT(final)}$, see Section 8.3.6)

Note that the fast charge current (I_{FS}) and set current (I_{SET}) are both active during the soft start time (t_{SS}) and are reported as $I_{SS_SET(start)}$ in the Electrical Characteristics table. This 2.1 mA typical value is valid for a 12 kΩ R_{REF} resistor. As the fast charge current is internally derived from the current through the R_{REF} resistor, values greater than or less than 12 kΩ will cause a decrease or increase of the I_{FS} current respectively.

If the fast start circuitry is not desired, connect the FB_PG pin to V_{OUT}. This will ensure the fast start circuitry is quickly turned-off as the FB_PG threshold is quickly reached. Note that this effects the PG pin behavior as well as described in Section 8.3.6.

Copyright © 2023 Texas Instruments Incorporated

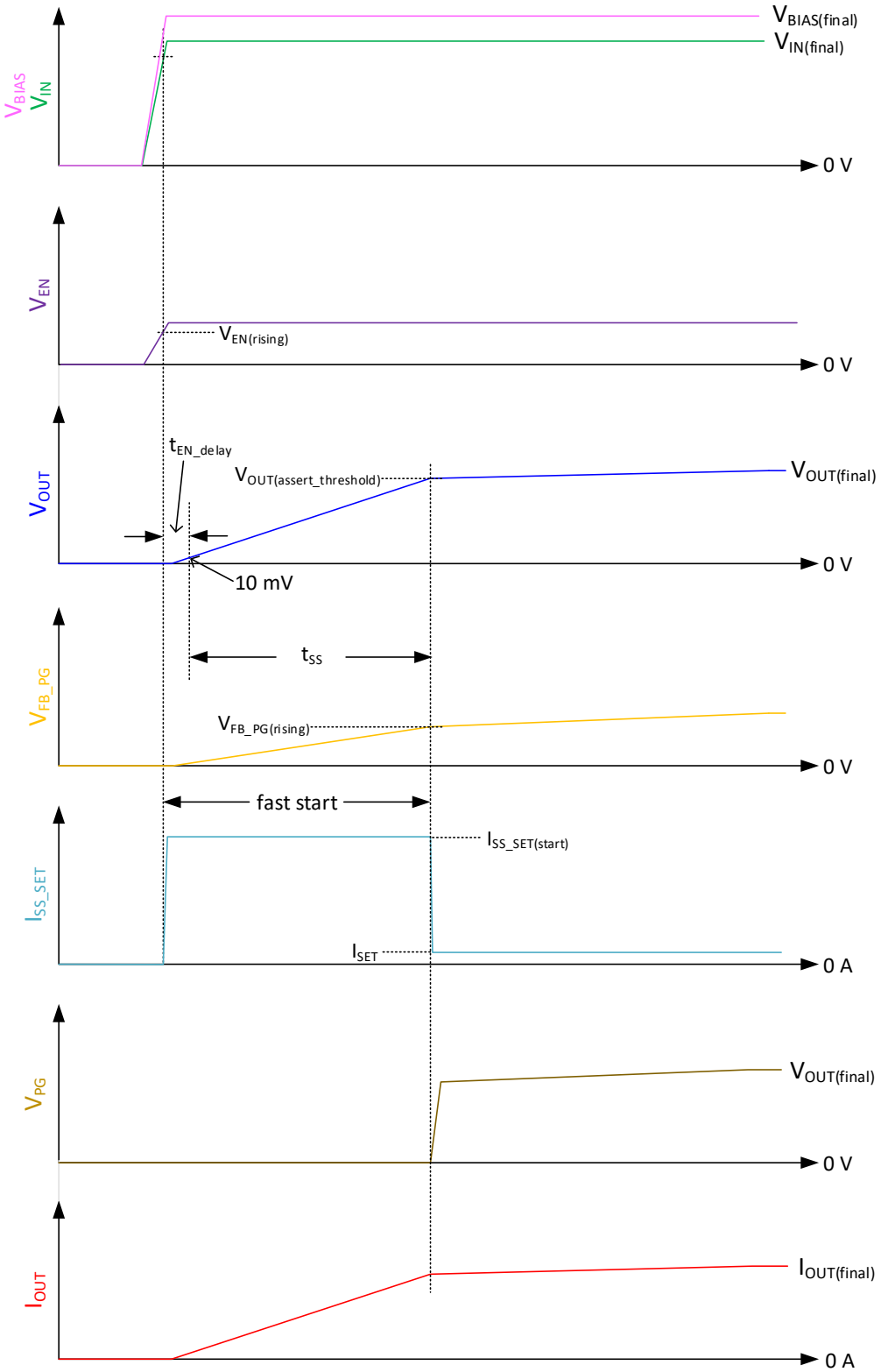


Figure 8-4. Simplified Schematic Showing Startup Waveforms

Copyright © 2023 Texas Instruments Incorporated

8.3.6 Configurable Power Good

The power good indicator pin, PG, is an open drain pin that is asserted when the output voltage reaches the desired value. The PG pin may either be pulled-up through a resistor to V_{OUT}, V_{IN}, or another voltage level less than the recommended maximum of 7 V. Select the resistor size to keep the maximum current sunk by PG to under the recommended operating condition current maximum of 2 mA.

Note that if PG is pulled-up to an external voltage before either V_{IN} or V_{BIAS} are supplied to the device, PG may not be pulled-down due to insufficient drive strength. $V_{IN(MIN_PG)}$ is specified in the Electrical Characteristics table as the minimum value either V_{IN} or V_{BIAS} must reach for PG to have sufficient pull-down strength to pull-down PG to under 0.5 V at less than or equal to 0.6 mA. Once V_{IN} and V_{BIAS} reach their proper final voltages, the PG pin has full drive strength.

By feeding the output voltage through a resistor divider to the FB_PG pin, the PG assertion level can be configured. The FB_PG pin has a typical threshold of 300 mV. When this threshold is reached or exceeded, the PG pin is asserted. Equation 7 shows how to calculate the V_{OUT} value where PG is asserted (it does not take into account the FB_PG pin leakage current which has minimal effect). As described in Section 8.3.5 the fast start circuitry will also turn-off when this level is reached.

$$V_{FB_PG(rising)} = V_{OUT(assert_threshold)} \times R_{FBPG_BOT} / (R_{FBPG_TOP} + R_{FBPG_BOT}) \quad (7)$$

To ensure PG is asserted by the time the final output voltage is reached, the worst case tolerances of output voltage, FB_PG threshold, and resistor tolerance levels must be taken into account. Generally, configuring the resistor divider so $V_{(assert_threshold)}$ is 90% or less than $V_{OUT(final)}$ is sufficient.

The PG deassert threshold can also be calculated using Equation 8.

$$V_{FB_PG(rising)} - V_{FB_PG(hysteresis)} = V_{OUT(deassert_threshold)} \times R_{FBPG_BOT} / (R_{FBPG_TOP} + R_{FBPG_BOT}) \quad (8)$$

If the PG pin is not used, it may be pulled to ground. However, the FB_PG pin must still be properly configured if the fast start circuitry described in Section 8.3.5 is desired.

8.3.7 Current Limit

The internal current limit, I_{LIM}, is the current limit value. There are two types of current limit behavior, depending on the value of the CLM pin. First, when CLM is high, there is brick-wall current limit. When CLM is low, there is turn-off current limit. CLM may be connected directly to V_{IN} or directly to GND to control the current limit operation. Do not change the value of this pin when the device is enabled, and do not float this pin.

Brick-wall current limit, also known as constant current limit, is shown in Figure 8-5. In this mode, once I_{LIM} is reached and the current limit circuitry has time to respond, the TPS7H1111 LDO will enter constant current regulation mode. In other words, the output voltage will drop to whatever value is needed to keep the output current at I_{LIM}. Once the fault is removed the device will resume regulation. Generally, there will be the same soft start time as during initial startup since the SS_SET pin is pulled-low to quickly discharge the C_{SS} capacitor during a fault. However, if the fault is extremely quick, the C_{SS} capacitor may not be fully discharged which would result in a quicker startup time.

Due to the high power dissipation in brick-wall current limit, there is the possibility that the TPS7H1111 will enter thermal shutdown which causes the device to stop regulation until it cools enough to exit thermal shutdown.

Copyright © 2023 Texas Instruments Incorporated

WARNING

The TPS7H1111 is not intended to indefinitely remain in brick-wall current limit mode.

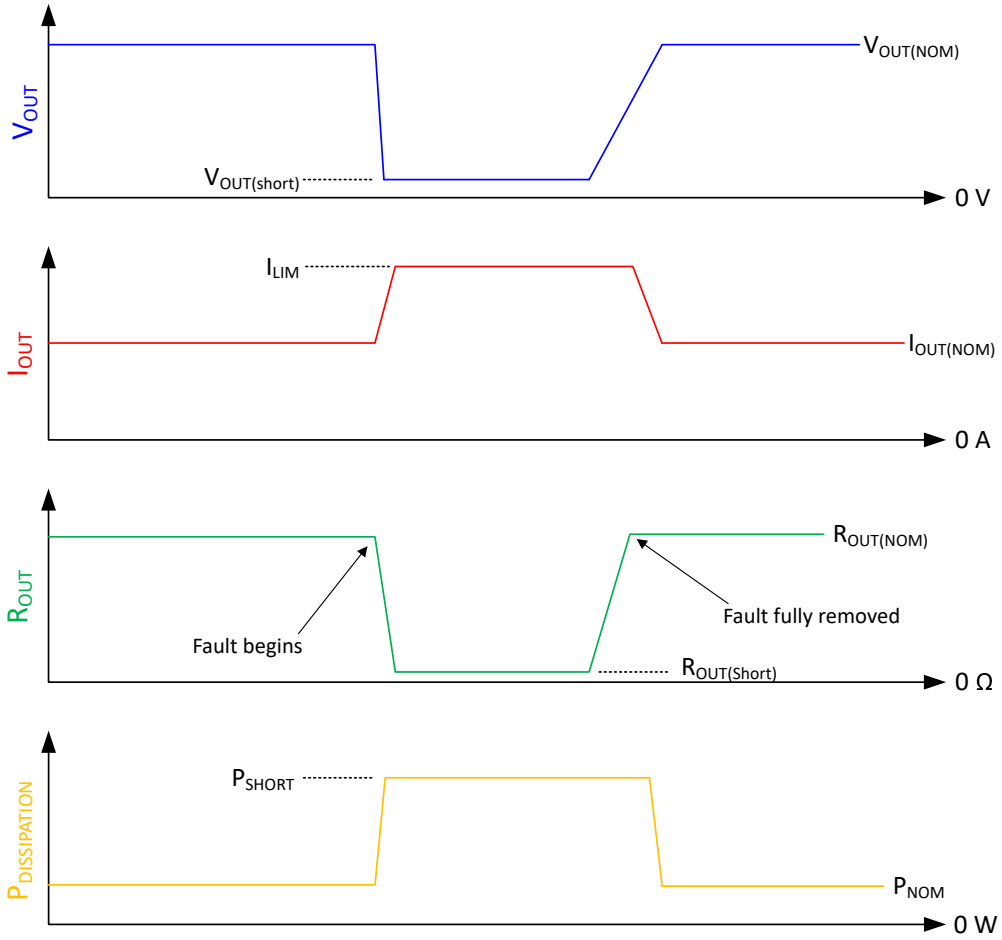


Figure 8-5. Simplified Brick-Wall Current Limit Waveforms (CLM High)

Alternatively, if CLM is low, there is turn-off current limit. The behavior is shown in Figure 8-6. In turn-off current limit, if current limit, I_{LIM}, is reached, the TPS7H1111 LDO will stop regulating (after a brief delay ~28 µs). The LDO will not resume regulation until EN is cycled (brought low then brought high).

The primary advantage of turn-off current limit is that there is no sustained high power dissipation after current limit is reached. However, the main disadvantage is that the device will not automatically resume regulation once the fault is removed. Therefore, an external monitor must determine when a fault has occurred and decide when to toggle the EN pin. This can normally be easily implemented by an existing device (such as an FPGA or microcontroller) monitoring the PG pin. If the monitor detects the PG pin deassert, it can then toggle EN to attempt to resume regulation.

When EN is being toggled from high to low to high, it must be low for at least t_{EN_LOW} (20 µs). Additionally, it is recommended to not toggle EN until SS_SET has discharged to 5% of its nominal value in order to have sufficient soft-start during restart to avoid immediately reentering current limit.

Copyright © 2023 Texas Instruments Incorporated

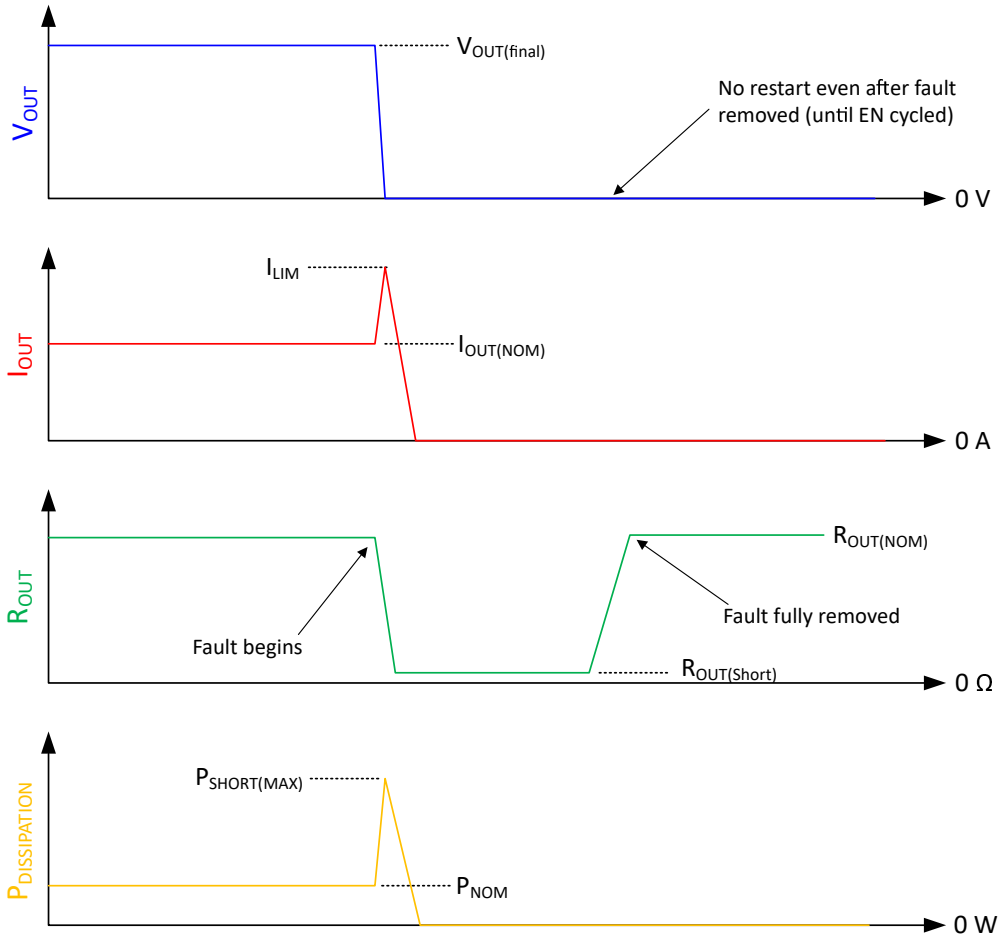


Figure 8-6. Simplified Turn-Off Current Limit Waveforms (CLM Low)

8.3.8 Stability

The default external compensation (C_{COMP} = 4.7 nF, R_{COMP} = 5 kΩ) is sufficient for stability when operating within the Recommended Operating Conditions with the default range of output capacitance and parasitics.

If using the part with different output capacitance than in the Recommended Operating Conditions, different compensation may be required. The main factors affecting stability is the output capacitance, its ESR (equivalent series resistance), and its ESL (equivalent series inductance). See Section 8.3.8.2 for additional information.

Stability may be validated by creating a Bode plot of the control loop. This may be done by injecting a signal into the feedback path. Usually, the signal is injected across a 5 Ω to 50 Ω resistor between OUT and OUTS. Remove this resistor (or use a 0 Ω shunt) when performing other measurements and during nominal operation. A common target for phase margin is 50° and target for gain margin is 6 dB.

8.3.8.1 Output Capacitance

The TPS7H1111 is optimized for a single tantalum output capacitor of 220 µF or two 100 µF capacitors. The complete range of acceptable capacitance, ESR, and ESL are specified in the Recommended Operating Conditions. Make note to verify the selected capacitors meet the requirements across all operating conditions. Additionally, a single 0.1 µF ceramic capacitor can be included. Place the one or more tantalum capacitors near the output of the TPS7H1111 and place the ceramic capacitor near the point of load.

ESR (equivalent series resistance) is an important parasitic element to take into account that varies significantly across frequency for capacitors. ESR values for tantalum capacitors are generally given at 100 kHz, and the values in the Recommended Operating Conditions table approximately correspond to values at 100 kHz. However, in reality the ESR at the loop crossover frequency is primarily what affects the stability of the

Copyright © 2023 Texas Instruments Incorporated

TPS7H1111 control loop. The loop crossover frequency can be higher or lower than 100 kHz. Therefore, the range of ESR values can be considered a good guideline, but additional verification of stability is prudent.

Also note that the capacitance, ESR, and ESL requirements are for the entire bulk capacitance. If 2x100 µF capacitors each with 40 mΩ ESR and 2 nH ESL are used, the resulting capacitance is 200 µF with 20 mΩ ESR and 1 nH ESL. The single ceramic capacitor should not be taken into account when considering these ESR and ESL requirements.

Ceramic capacitors larger than 0.1 µF are generally not allowed due to their lower resonance frequency. This lower resonance frequency is likely within the loop bandwidth of the TPS7H1111 regulator (which can be nearly 10 MHz). Therefore, the low resonance point, combined with the low ESR, negatively impacts the loop bandwidth and device stability. The lower bandwidth negatively affects PSRR, therefore negating any potential benefit of additional ceramic capacitance.

However, if ceramic capacitors above 0.1 µF must be used, it is recommended the ceramic capacitor has a resonance frequency one to two decades above the loop bandwidth. Alternatively additional series resistance can be added to increase the ESR. This prevents a strong resonance point.

TI has measured gain and phase margin of various space grade capacitors to demonstrate good stability margin. See Section 9.3 for additional information.

When capacitors other than the standard bulk capacitance and a single 0.1 µF capacitor are utilized, it is recommended to simulate the capacitors and complete system. It is also suggested to create a Bode plot and perform load steps on the actual system to verify sufficient stability margin.

8.3.8.2 Compensation

It is recommended to compensate the TPS7H1111 by utilizing compensation as shown in Figure 8-7 with C_{COMP} = 4.7 nF and R_{COMP} = 5 kΩ. C_{HF} is not required.

However, if a different control loop response is desired, or if a different output capacitance, ESL, or ESR is used, a different compensation network may be needed. The error amplifier is an OTA (operational transconductance amplifier); therefore, traditional compensation techniques for OTAs may be employed. While TI has found its recommended type I compensation works best, an example of a type II compensation is shown in Figure 8-7.

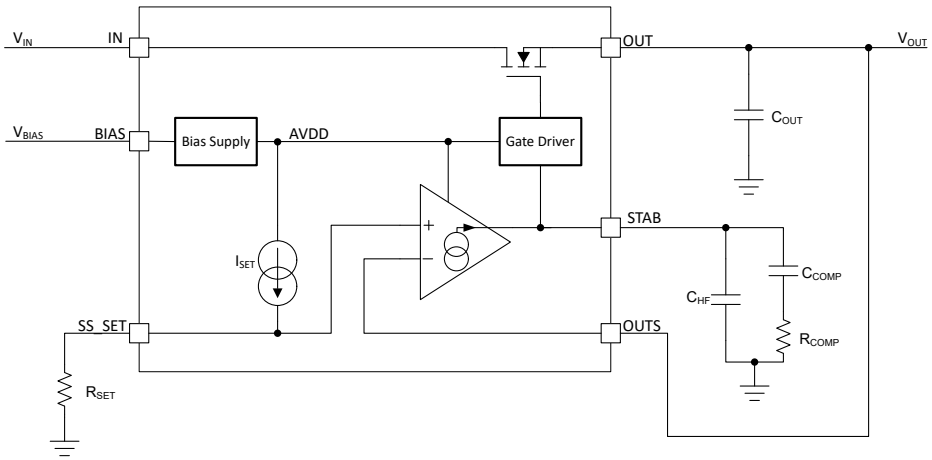


Figure 8-7. General Type II Compensation

Note that unlike in linear regulators that use a resistive voltage divider fed to a feedback pin, a feed forward capacitor (C_{FF}) cannot be used to modify the control loop. For resistive voltage divider LDOs, a feed forward capacitor essentially provides a high frequency short between the output voltage and the feedback pin. However, in the TPS7H1111 architecture, there is no voltage divider and instead the output voltage is fed directly to the negative input terminal of the error amplifier. Since the error amplifier operates in a unity gain configuration, it inherently obtains the potential benefits of reduced noise and increased PSRR that a feed forward capacitor would typically provide.

Copyright © 2023 Texas Instruments Incorporated

8.3.9 Current Sharing

The TPS7H1111 supports paralleling multiple devices in order to increase the output current or spread heat dissipation. While a single device is capable of outputting 1.5 A of current, two devices are capable of outputting slightly less than 3 A. This is because each device will not source exactly 50% of the current. The mismatch in current between the two devices is due to differences in the error amplifier offset, V_{OS}, of each device. Mismatch due to differences in the reference current, I_{SET}, is removed by tying the SS_SET nets together. This is shown in a simplified schematic in Figure 8-8.

Note that an R_{SET} resistance of half the normal value should be used since there is now 200 µA (typ) of current through the resistor. Furthermore, two C_{SS} capacitors should be utilized (or one of twice the normal value) in order to ensure equivalent start-up time. Finally, each device should have its normal output capacitance. When paralleling two devices, this results in twice the capacitance on $V_{OUT(final)}$ when compared with a single device. The output capacitors in Figure 8-8 are placed after the ballast resistor (closest to the load). This placement adds some effective ESR to the capacitors as seen by the TPS7H1111 control loop. It is also acceptable to add the capacitors before the ballast resistors directly at the OUT pins, but this may result in a slightly larger voltage drop during a load step due to the ballast resistor being placed between the output capacitors and the load.

To calculate the mismatch first between two devices, the total output current, I_{OUT}, the set output voltage, V_{SS_SET}, the offset voltage of each device, V_{OS}, and the ballast resistor, $R_{ballast}$, must be known. The ballast resistor may be selected to meet the desired current matching requirements; however, it should be noted that the larger the ballast resistor , the worse the load regulation will be due to IR drops across the ballast resistor. Then, the combined output voltage, $V_{OUT(final)}$, must be calculated as shown in Equation 9. This is the voltage that will be seen at the load.

$$V_{OUT(final)} = [(V_{SS_SET} + V_{OS1}) + (V_{SS_SET} + V_{OS2}) – I_{OUT} \times R_{ballast}] / 2 \quad (9)$$

Next the current in each device is calculated using Equation 10 and Equation 11

$$I_{OUT1} = (V_{SS_SET} + V_{OS1} – V_{OUT(final)}) / R_{ballast} \quad (10)$$

$$I_{OUT2} = (V_{SS_SET} + V_{OS2} – V_{OUT(final)}) / R_{ballast} \quad (11)$$

This calculated current can be compared to the ideal current through each device, $I_{OUT(total)} / 2$.

Copyright © 2023 Texas Instruments Incorporated

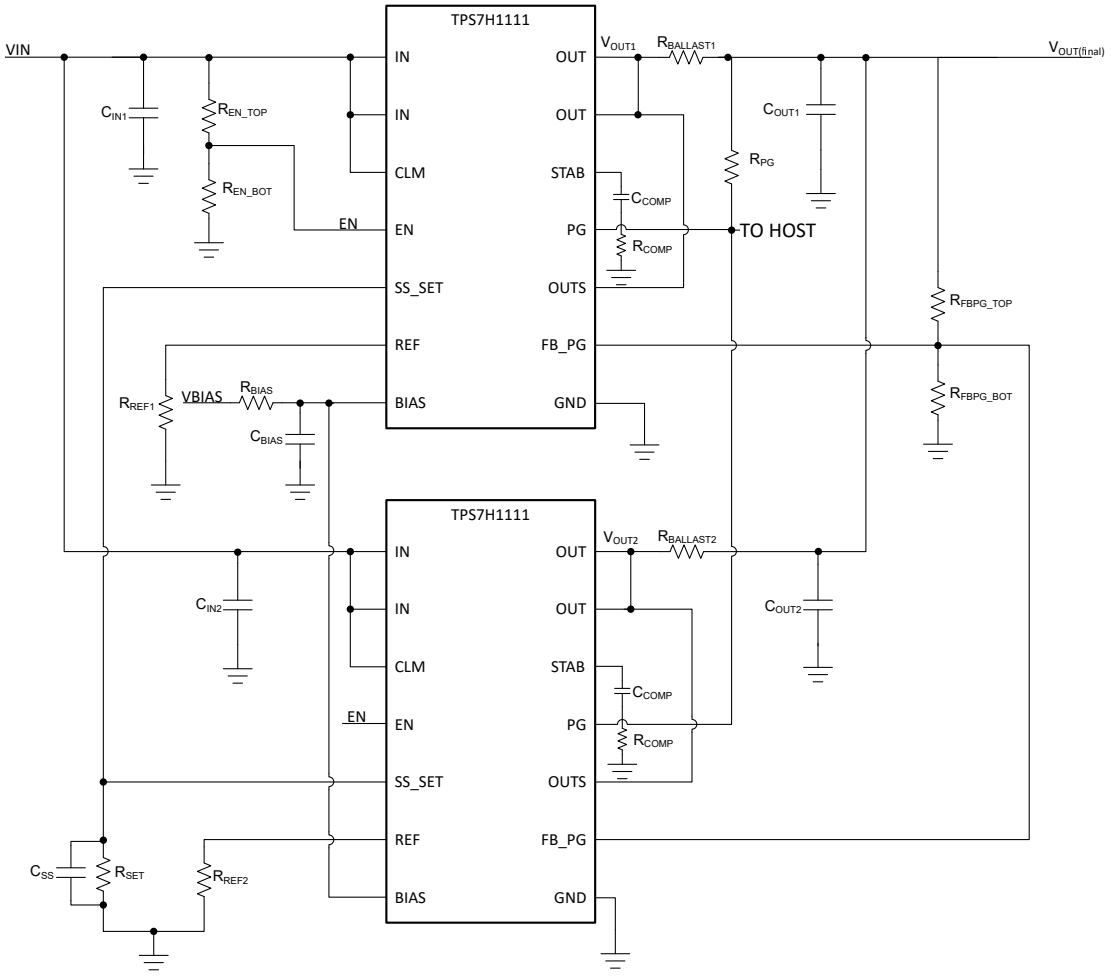


Figure 8-8. Current Sharing Simplified Schematic

Ideally the offset of each device would be measured to determine the exact current sourced by each device. As this is generally infeasible, it is often tempting to use the worst case offset shown in the Electrical Characteristics. This would result in setting V_{OS1} to the maximum specified V_{OS} and V_{OS2} to the minimum specified V_{OS}. However, this may result in an overly pessimistic mismatch. To aid in analysis, histograms of multiple measured units of offset data are provided in Figure 6-47, Figure 6-48, and Figure 6-49. Additionally, measurements have shown better than calculated results as described in Section 9.2.2.

A simplified diagram showing current sharing and the source of error is given in Figure 8-9.

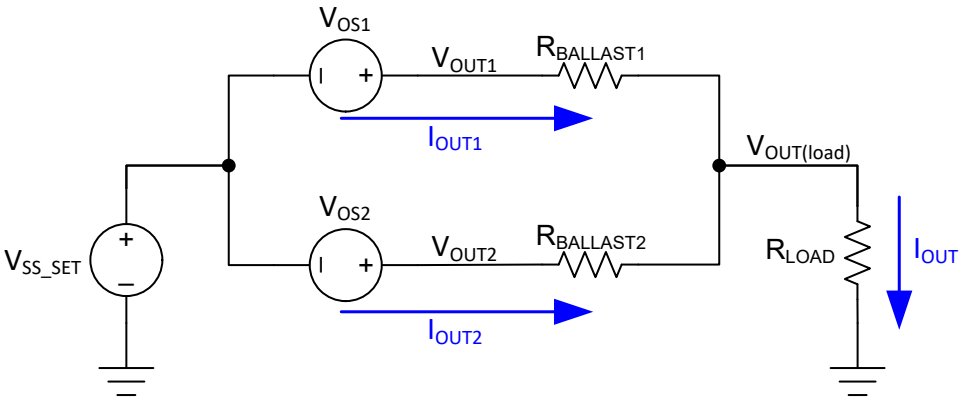


Figure 8-9. Current Sharing Simplified Schematic

Copyright © 2023 Texas Instruments Incorporated

8.3.10 PSRR

The PSRR (power supply rejection ratio) of the TPS7H1111, is the amount it attenuates the input noise at V_{IN}, to the output, V_{OUT}. It is mathematically defined in Equation 12.

$$PSRR = 20 \times \log(V_{IN(AC)} / V_{OUT(AC)}) \quad (12)$$

The input noise is generally dominated by the switching ripple of an upstream converter. This noise occurs at the switching frequency and its harmonics.

The PSRR values are reported under various conditions and at different frequencies in both the Electrical Characteristics and the Typical Characteristics Figure 6-1 through Figure 6-11 . The TPS7H1111 is designed to have excellent PSRR across a wide variety of conditions. In order to further improve PSRR, operating conditions can be fine tuned. In general, the TPS7H1111 PSRR is most improved by the following (in relative order of importance):

- Increased input supply headroom (increased $V_{IN} – V_{OUT}$)
- Increased bias supply headroom (increased $V_{BIAS} – V_{OUT}$)
- Decreased output current
- Larger RC filter on the BIAS rail (only if the bias supply is the main source of noise)

PSRR is only minimally improved on the TPS7H1111 by the following:

- Increased temperature
- Increased soft start capacitance
- Addition of a ferrite bead (see Section 9.2.1.3)
- Increased input voltage
- Increased output voltage

The TPS7H1111 architecture is optimized for high PSRR due to its high loop bandwidth. In order to keep the bandwidth high, the output capacitance should be within the recommended operating conditions. Traditional techniques to improved PSRR by increasing output capacitance are not valid. This is because additional capacitance could reduce the loop bandwidth of the TPS7H1111. This reduced bandwidth will degrade PSRR more than the capacitance helps.

If additional PSRR at high frequency (for example, > 10 MHz) is desired, a ferrite bead may be utilized. The ferrite bead should be placed outside the TPS7H1111 control loop as shown in Section 9.2.1 as to not degrade the loop bandwidth or stability.

In addition to the PSRR from V_{IN} to V_{OUT}, PSRR is specified from V_{BIAS} to V_{OUT} as $PSRR_{BIAS}$. It is defined in Equation 13.

$$PSRR_{BIAS} = 20 \times \log(V_{BIAS(AC)} / V_{OUT(AC)}) \quad (13)$$

Since the BIAS supply is relatively low current, an RC filter can be inserted between the BIAS supply and BIAS pin (typically 10 Ω and 4.7 µF) to increase the $PSRR_{BIAS}$. The RC filter, combined with the internal ripple rejection of the internal bias regulator, provides very high $PSRR_{BIAS}$ as shown in Figure 6-13. Therefore, at typical switching frequencies between 100 kHz and 1 MHz (where high ripple rejection is the most important to filter the input ripple), $PSRR_{BIAS}$ remains very high to avoid becoming a major limiting factor in overall device PSRR. If an RC filter is unable to be utilized, the $PSRR_{BIAS}$ values will be degraded as shown in Figure 6-12.

If the bias supply is exceptionally noisy or if an RC filter is unable to be utilized, it may be beneficial to calculate the total output ripple coming from the input ripple on both the V_{IN} and V_{BIAS} supplies. The total output ripple is the superposition of the V_{IN} ripple attenuated by its PSRR and the V_{BIAS} ripple attenuated by its $PSRR_{BIAS}$ as shown in Equation 14. Note however that each term is frequency dependent.

$$V_{OUT(AC)} = V_{IN(AC)} / (10^{PSRR/20}) + V_{BIAS(AC)} / (10^{PSRR_{BIAS}/20}) \quad (14)$$

Copyright © 2023 Texas Instruments Incorporated

8.3.11 Noise

In addition to the attenuated input noise, the TPS7H1111 (along with all physical devices) creates inherent noise. This noise is superimposed on the output signal. The noise values are also reported under various conditions and at different frequencies in both the Electrical Characteristics and the Typical Characteristics Figure 6-15 through Figure 6-19.

Some of the most problematic noise is the low frequency output noise (also referred to as 1/f noise). This is very difficult to filter out using discrete filters as it would require very large component values. TPS7H1111 is optimized for low noise across the frequency spectrum, particularly at low frequency. Various design techniques are utilized to achieve this such as high loop bandwidth, a unity gain error amplifier, and the use of a reference filter.

The precision current reference, I_{SET}, is filtered by the C_{SS} capacitor. Larger C_{SS} capacitance better filters I_{SET}. However, the noise reduction with larger capacitors primarily reduces the 1/f noise under 200 Hz. The noise reduction is minimal for high frequency noise. Generally a 4.7 µF ceramic capacitor is a reasonable tradeoff between low noise, physical capacitor size, capacitor availability, and device startup time.

The TPS7H1111 has minimal difference in noise across all V_{OUT} and V_{IN} operating conditions. However, at higher output currents the noise is marginally greater at frequencies higher than 100 kHz.

Both PSRR and noise contribute to a clean output voltage. However, depending on the application, either PSRR or noise can be more important, and it is important to optimize for the given application. Generally PSRR is more important if there is substantial noise at V_{IN} (perhaps in the form of a highly noisy switching regulator).

8.3.12 Thermal Shutdown

The TPS7H1111 has thermal shutdown to turn-off the device when the die temperature exceeds $T_{SD(enter)}$. As the die cools below $T_{SD(exit)}$, the device will resume regulation. The typical $T_{SD(enter)}$ of 160°C and $T_{SD(exit)}$ of 130°C provides a large hysteresis (30°C typical). The large hysteresis is intended to allow the device to sufficiently cool before attempting to resume regulation.

8.4 Device Functional Modes

The table below shows the device modes.

Table 8-4. Device Functional Modes

EN PIN	Device Status
High	Regulation mode
Low	Shutdown mode

Copyright © 2023 Texas Instruments Incorporated

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H1111 is a radiation hardened linear regulator optimized for RF applications. It has an output current of up to 1.5 A, and it can be used over an input voltage range of 0.85 V to 7 V with a bias supply voltage range of 2.2 V to 14 V.

9.2 Typical Applications

There are a wide variety of use cases for the TPS7H1111 LDO. The following are discussed in this section:

1. 2.5 V input to 1.8 V output with a configurable turn-on threshold (EN)
2. 2.5 V input to 1.8 V output parallel operation

9.2.1 Application 1: Set Turn-On Threshold with EN

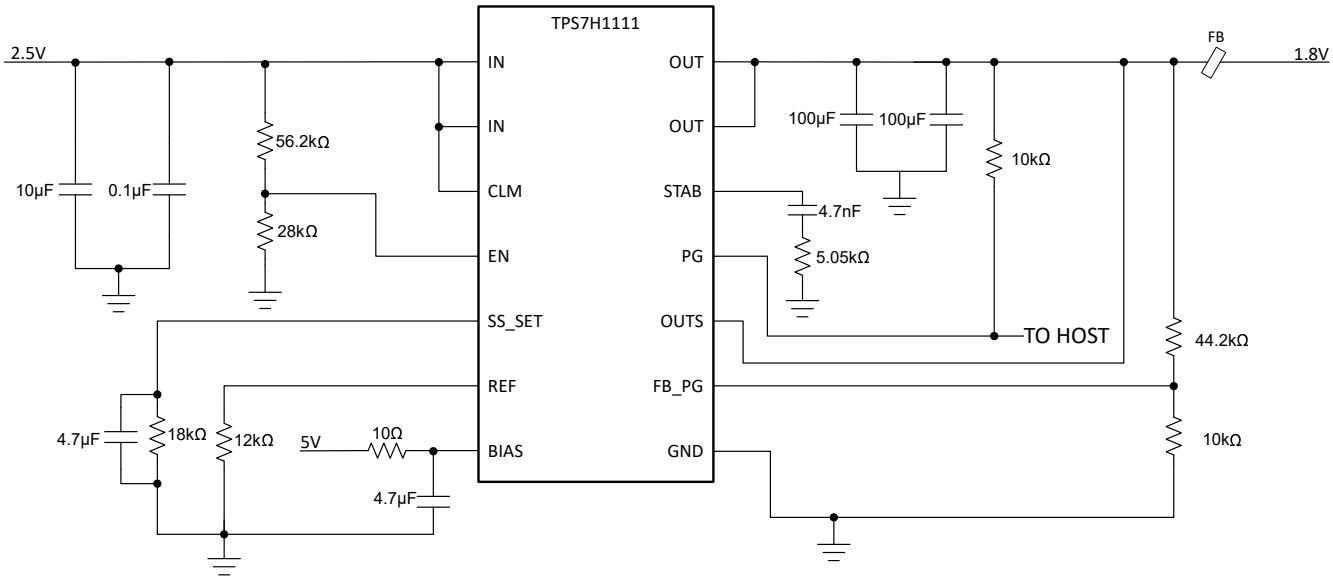


Figure 9-1. Use Case: Set Turn-On Threshold with EN

9.2.1.1 Design Requirements

Table 9-1. Design Parameters

PARAMETER	VALUE
V_{IN}	2.5 V ± 5%
V_{BIAS}	5 V ± 5%
V_{OUT}	1.8 V ± 1.5%
I_{OUT}	1.4 A (typ)
$V_{IN(turn\text{-}on\ threshold)}$	1.8 V (typ)
$V_{OUT(PG\ assertion\ threshold)}$	90% of $V_{OUT(final)}$ (typ), 1.62 V
t_{SS}	3.7 ms (typ)

Copyright © 2023 Texas Instruments Incorporated

Copyright © 2023 Texas Instruments Incorporated

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Bias Supply

A 5 V bias supply was selected for this design. Since V_{BIAS} ≥ V_{OUT} + 1.6 V, there is sufficient bias supply headroom (5 V ≥ 1.8 V + 1.6 V). Additionally, a 10 Ω resistor and 4.7 µF X7R ceramic capacitor were selected to filter the bias supply to ensure bias supply noise is not the limiting factor in overall regulator PSRR.

9.2.1.2.2 Output Voltage Configuration

The output voltage is configured using Equation 1. Therefore, R_{SET} = V_{SS_SET} / I_{SET} = 1.8 V / 100 µA = 18 kΩ. An 18 kΩ 0.1% tolerance resistor is selected. Using a 1% tolerance resistor is also acceptable, but this could contribute 1% error directly to the output voltage. Similarly, a 12 kΩ 0.1% tolerance resistor is selected for R_{REF}.

9.2.1.2.3 Output Voltage Accuracy

To determine the output voltage accuracy, the V_{ACC} specification with in the Section 6.5 table is consulted. V_{ACC} specifies a minimum accuracy of –1.3% and maximum accuracy of +1.2% across temperature. This specification applies across the complete temperature range of –55°C to 125°C, across all the input voltages (0.85 V ≤ V_{IN} ≤ 7 V and 2.2 V ≤ V_{BIAS} ≤ 14 V), and up to full load (1 mA ≤ I_{OUT} ≤ 1.5 A). A few additional details to the measurement are noted in Section 8.3.2. The following sources of error are also added to calculate a system level accuracy:

- Since post TID specifications are measured at room temperature (a MIL standard in order to avoid annealing at high temperatures), the TID drift is not part of the over temperature accuracy specification. The TPS7H1111 is specified post TID to have a minimum accuracy of –0.7% and maximum of +1.1%. This is compared to a pre-TID accuracy of –0.7% and maximum of +0.9%. Therefore, the specification increase due to TID is an additional 0.2% error being added. While the worst case TID drift of a single unit could be used instead, this may be excessively pessimistic as that would require a unit to have an initial room temperature accuracy near the maximum and a drift near the maximum values.
- The external error due to the resistor tolerance of the R_{REF} and R_{SET} resistors need to be added. Since it is assumed the error is uncorrelated, it is decided to add the errors as a sum of squares. For the selected 0.1% tolerance R_{REF} and R_{SET} resistors, the total error is $R_{(error)}$ = sqrt($0.1\%^2$+$0.1\%^2$) = +/– 0.14%.

Equation 15 is used to calculate the system error for output voltage accuracy.

$$System_{(error)} = V_{ACC} + R_{(error)} + TID_{(error)} \quad (15)$$

Therefore, the negative error is $System_{(error)}$ = –1.3% – 0.14% – 0% = –1.44% and the positive error is $System_{(error)}$ = 1.2% + 0.14% + 0.2% = 1.54%. There the total system error due to the TPS7H1111 device, external resistors, and 100 krad(Si) of TID is +1.54%/–1.44%. If the total system error is centered, this comes to ±1.49%.

Lifetime drift data could similarly be added. Group C data may be used to aid this calculation. For this example, it is assumed the lifetime drift is minimal compared to the other sources of error and is therefore not added.

9.2.1.2.4 Enable Threshold

The desired turn-on threshold is 1.8 V. This means that as the V_{IN} rail is turned-on and begins rising, the TPS7H1111 will begin turning-on as soon as V_{IN} reaches 1.8 V. While this is not enough headroom from V_{IN} to V_{OUT} for final regulation, the regulator will begin start-up and V_{IN} will continue to its final voltage of 2.5 V. If desired, a higher voltage turn-on threshold could also be utilized (for example, 2.2 V).

By using Equation 3 and selecting an R_{EN_TOP} value 56.2 kΩ, the R_{EN_BOT} resistor can be calculated as shown in Equation 16.

$$R_{EN_BOT} = V_{EN(rising)} \times R_{EN_TOP} / (V_{IN(rising)} – V_{EN(rising)}) = 0.6\ V \times 56.2\ k\Omega / (1.8\ V – 0.6\ V) = 28.1\ k\Omega \quad (16)$$

A standard value 28 kΩ resistor is selected for R_{EN_BOT}. The worst case (highest) $V_{IN(rising)}$ threshold is calculated using Equation 3 and the max $V_{EN(rising)}$ threshold of 0.62 V. This is determined to be 1.86 V which is

Copyright © 2023 Texas Instruments Incorporated

acceptable. The typical $V_{IN(falling)}$ is then calculated using Equation 4. This is determined to be 1.50 V which is also acceptable.

It is also important to ensure Equation 5 is followed to prevent possible SEFIs. As shown in Equation 17, $V_{EN(final)}$ = 0.83 V which is greater than the recommended 0.8 V.

$$V_{IN(final)} \times R_{EN_BOT} / (R_{EN_TOP} + R_{EN_BOT}) = V_{EN(final)} = 2.5\ V \times 28\ k\Omega / (56.2\ k\Omega + 28\ k\Omega) = 0.83\ V \quad (17)$$

9.2.1.2.5 Soft Start and Noise Reduction

The suggested soft start capacitor is a 4.7 µF ceramic X7R capacitor. This is utilized for this design as it provides a reasonable soft start time of 3.7 ms and great noise filtering. A smaller C_{SS} capacitor could be selected if a slower start-up time is desired; however, a lower value capacitor is not considered in order to maintain great noise filtering of the I_{SET} reference current.

9.2.1.2.6 Configurable Power Good

For this design, it is desired that the power good pin asserts when V_{OUT} reaches 90% of its final value (1.62 V).

By using Equation 7 and selecting an R_{FBPG_BOT} value 10 kΩ, the R_{FBPG_TOP} resistor is calculated as shown in Equation 18.

$$R_{FBPG_TOP} = R_{FBPG_BOT} \times (V_{OUT(assert_threshold)} - V_{FB_PG(rising)})\ ] / V_{FBPG(rising)} = [10\ k\Omega \times (1.62\ V - 0.306\ V)] / 0.306\ V = 42.9\ k\Omega \quad (18)$$

A standard value 44.2 kΩ resistor is selected for R_{FBPG_TOP}. The worst case (highest) $V_{IN(assert_threshold)}$ threshold is then calculated in order to ensure PG is asserted (and the fast charge current is turned-off) before V_{OUT} reaches its desired value. This is determined using Equation 7 along with the maximum $V_{FB_PG(rising)}$ threshold of 313 mV. The $V_{OUT(assert_threshold),\ max}$ value is determined to be 1.70 V. This is 94% of the final V_{OUT} value which is sufficient margin.

Finally, the typical value of the $V_{OUT(deassert_threshold)}$ is calculated to know when PG will deassert. This is determined using Equation 8 along with the $V_{FB_PG(hysteresis)}$ value of 14 mV. The $V_{OUT(deassert_threshold)}$ value is determined to be 1.58 V. This means that if V_{OUT} falls to 88% of its nominal value, the PG pin will deassert.

9.2.1.2.7 Current Limit

The CLM pin is connected directly to V_{IN} for brick-wall current limit mode. If desired, a resistor could also be used to pull-up the CLM pin to V_{IN} (for example, a 10 kΩ resistor).

9.2.1.2.8 Output Capacitor and Ferrite Bead

In accordance with the Recommended Operating Conditions, 200 µF is selected for the output capacitance. Specifically, two 100 µF Tantalum AVX capacitors are utilized (see Section 9.3 for a list of capacitors TI has validated for use with the TPS7H1111-SP).

In this design a ferrite bead was also added for additional high frequency filtering. It is important to keep the OUTS connection before the ferrite bead (to keep the ferrite bead outside the TPS7H1111 control loop). If the ferrite bead was inside the control loop, the additional inductance may cause instability. In general, a ferrite bead is not required for good PSRR performance, but it was added here to determine its affects. Specifically, the KEMET Z1206C800APWST ferrite bead was selected for this design. While not utilized in this design, an additional 0.1 µF capacitor could be placed after the ferrite bead for additional filtering.

9.2.1.3 Application Curve

The PSRR, noise, and a Bode plot measurement is performed both with and without a ferrite bead. The measurements are done for V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, and I_{OUT} = 1 A. It is shown a ferrite bead marginally helps the higher frequency PSRR around 10 MHz. The ferrite bead shows minimal affect on noise and minimal affect on stability.

Copyright © 2023 Texas Instruments Incorporated

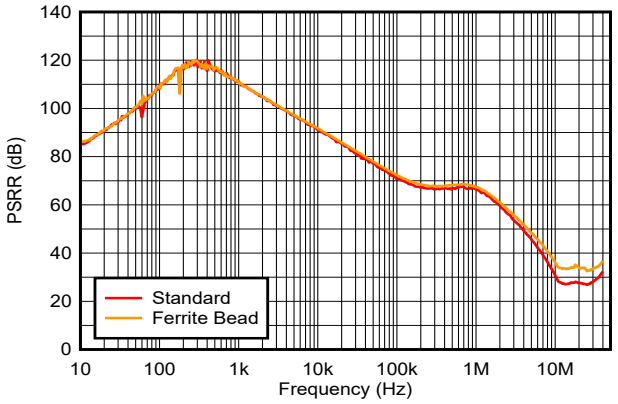


Figure 9-2. PSRR vs. Frequency with Ferrite Bead

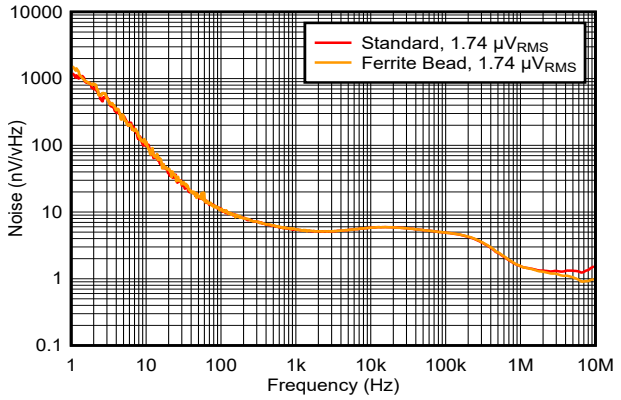
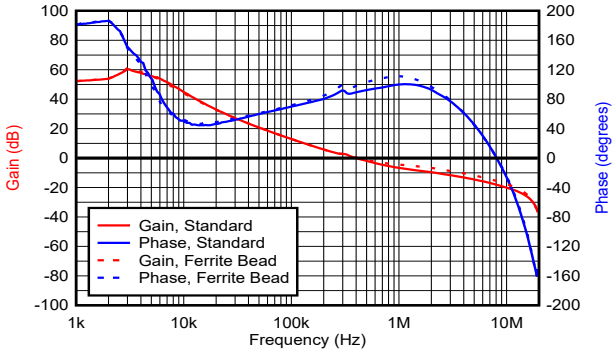


Figure 9-3. Noise vs. Frequency with Ferrite Bead



Standard: Phase Margin = 89°, Gain Margin = 18 dB

Ferrite Bead: Phase Margin = 99°, Gain Margin = 16 dB

Figure 9-4. Bode Plot with Ferrite Bead

9.2.2 Application 2: Parallel Operation

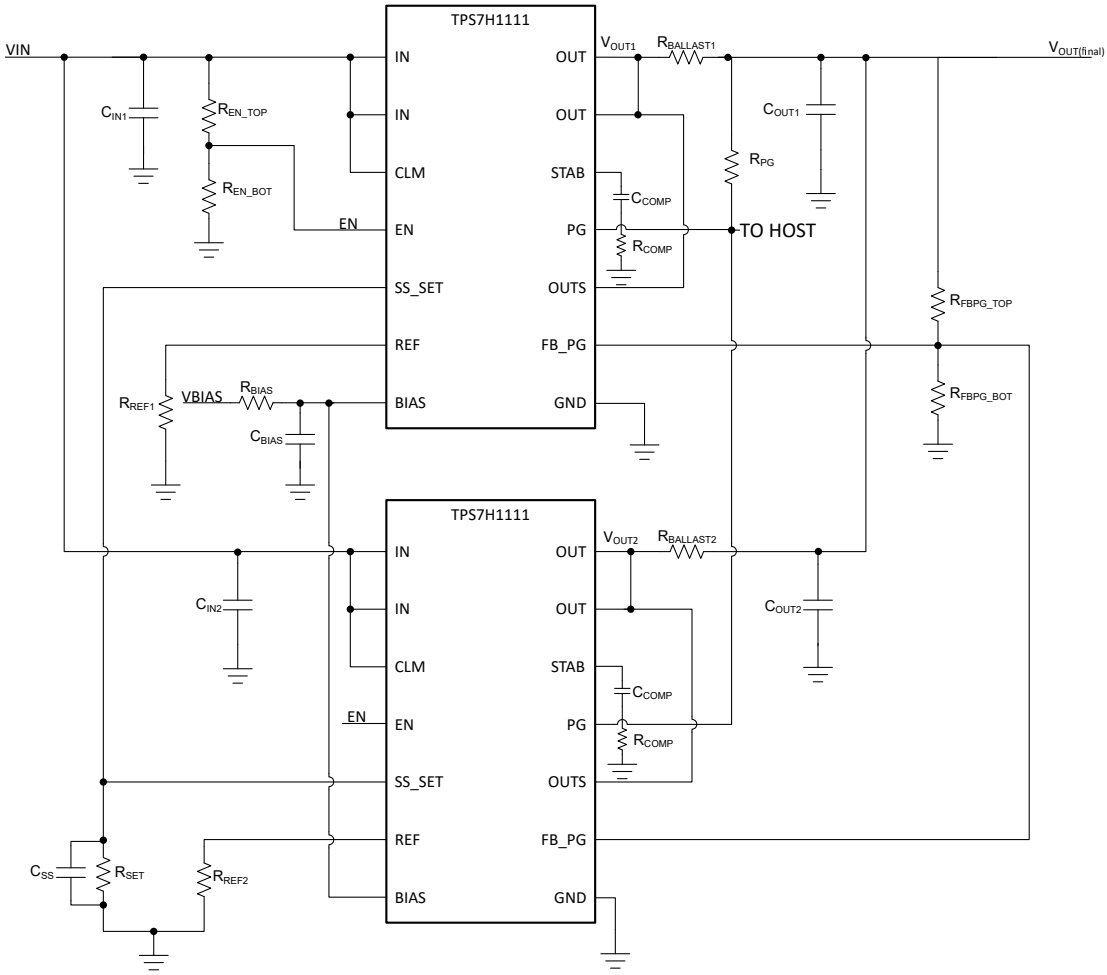


Figure 9-5. Use Case: Parallel Operation

9.2.2.1 Design Requirements

The design requirements shown here are similar to those in Application 1. The main exception is that 2.9 A of output current is desired and a ferrite bead is not utilized. The higher current necessitates the use of paralleled devices.

Table 9-2. Design Parameters

PARAMETER	VALUE
V_{IN}	2.5 V ± 5%
V_{BIAS}	5 V ± 5%
V_{OUT}	1.8 V ± 1.5%
I_{OUT}	2.9 A
$V_{IN(turn\text{-}on\ threshold)}$	1.8 V (typ)
$V_{OUT(PG\ assertion\ threshold)}$	90% of $V_{OUT(final)}$ (typ), 1.62 V
t_{SS}	3.7 ms (typ)

9.2.2.2 Detailed Design Procedure

The design procedure is the same as in Application 1 with the exception of the sections below.

Copyright © 2023 Texas Instruments Incorporated

9.2.2.2.1 Current Sharing

As described in Section 8.3.9, the SS_SET pins are connected together so that each TPS7H1111 internal error amplifier sees the same voltage. A single R_{SET} resistor may be utilized of half the normal value (since there is now 200 µA of current through the resistor). Two C_{SS} capacitors should be utilized (or one of twice the normal value) in order to ensure equivalent start-up time.

A 5 mΩ $R_{ballast}$ resistor was utilized. The board resistance from the output of one device to the common V_{OUT} rail of both devices was assumed to be significantly less than the ballast resistor and was therefore not considered to be a significant factor in calculating the total ballast resistance. This ballast resistor was selected to achieve a reasonable tradeoff between accurate current sharing and minimizing voltage drop across the resistance. If desired, the output voltage of each device could be set marginally higher to account for a voltage drop at a given current.

Section 8.3.9 shows how to calculate the worst current sharing mismatch using the output offset voltage. Additional details are in the following section showing how results are measured better than expected.

9.2.2.3 Application Results

The offset voltage of each device was measured and determined to be –0.1339 mV for the first device and –0.2131 mV for the second device. Equation 10 and Equation 11 are used to calculate the expected error and are recorded in Table 9-3 for different current values. The current is then measured to compare with the expected error value.

Table 9-3. Current Error

$I_{OUT(total)}$	Expected Error	Measured Error
1.156 A	1.37%	1.04%
2.878 A	0.55%	0.07%

As shown in Table 9-3, the measured error is about 1.3x less than expected at 1.156 A and 7.9x less than expected at 2.878 A. This is hypothesized to be at least partially due to the temperature coefficient of V_{OS}. If one device begins sourcing more than half the total current, it will heat up more than the second device. As the device heats, the V_{OS} decreases which causes the device to source less current. This provides a type of negative feedback, therefore ensuring more equal balancing.

Copyright © 2023 Texas Instruments Incorporated

9.3 Capacitors Tested

TI has tested various space grade capacitors and measured the control loop response of the TPS7H1111 system. The effects of different capacitors is clearly shown, but in all cases stability is demonstrated across the current range. The measured gain margin (GM) in decibels and phase margins (PM) in degrees is shown in Table 9-4. Results are taken with V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V at room temperature at the indicated current levels. The Bode plots themselves are shown in Figure 6-20 through Figure 6-27.

Table 9-4. Tested Space Grade Capacitors

Manufacturer	Capacitance	Part Numbers	I_{OUT} = 0 A		I_{OUT} = 1 A		I_{OUT} = 1.5 A	
			PM	GM	PM	GM	PM	GM
Kemet	1x220 µF	T540D227K010AH6710	71	30	98	14	91	14
Kemet	1x220 µF + 0.1 µF(1)	T540D227K010AH6710 + C0603K104K3RML	72	19	94	9	66	8
AVX	2x100 µF	TBME107K020LBLC9045	83	29	98	19	99	19
AVX	2x100 µF + 0.1 µF	TBME107K020LBLC9045 + 300904102104KA	61	27	98	13	99	12

(1) Not recommended for the plastic package due to the lower gain margin.

The values reported above are for the ceramic package TPS7H1111-SP. The plastic package (TPS7H1111-SP and TPS7H1111-SEP) were found to have similar stability responses but with a approximately two decibel lower gain margin. Also note that gain margin decreases at high current and low temperature. Phase margin decreases at low current and high temperature.

9.4 TID Effects

Most specifications listed in the Electrical Characteristics are tested using automated test equipment (ATE). These specifications are therefore easily tested both pre-irradiation and post-irradiation. Additionally, these specifications are generally part of the RLAT (radiation lot acceptance testing) flow. However, some specifications are difficult to measure on the ATE (such as due to high gain or sensitive to parasitics) and are therefore only measured during bench characterization. Typically these specifications are not measured post irradiation.

PSRR, noise, and stability are the key specifications that are not covered using the ATE and therefore not part of the traditional RLAT flow. In order to provide additional information for these key specifications, a one time characterization was performed on three EVMs. These three EVMs were biased and exposed at a high-dose-rate (HDR) to 100 krad(Si).

All PSRR, noise, and stability measurements showed good results under irradiation. The following generalities are made:

- PSRR is measured marginally lower post TID in the 100 Hz to 1 kHz range. Unit 1 shows around 10 dB lower post TID; however, this is thought to be a setup related issue due to difficulty in measuring such high gain. In any event, the PSRR is still extremely high (>95 dB) within this range.
- PSRR is measured marginally lower post TID under 100 Hz and above 1 kHz.
- The noise is measured incrementally higher in the 10 Hz to 10 kHz range.
- The noise is measured about the same below 10 Hz and above 100 kHz.
- The RMS noise is calculated to be an average of 120 nV_{RMS} higher post TID.
- The average phase margin magnitude shift is around 7°. The phase margin remains high for all pre and post measurements.
- The average gain margin magnitude shift is around 2 dB. This change is considered minimal and potentially within measurement error.

The complete data follows. Unless otherwise noted, the EVM conditions are V_{IN} = 2.5 V, V_{OUT} = 1.8 V, V_{BIAS} = 5 V, C_{OUT} = 2x100 µF (see Table 9-4), C_{SS} = 4.7 µF, R_{REF} = 12.0 kΩ, R_{BIAS} = 10 Ω, C_{BIAS} = 4.7 µF, T_A = 25°C, integrated noise reported with 10 Hz to 100 kHz bandwidth.

Copyright © 2023 Texas Instruments Incorporated

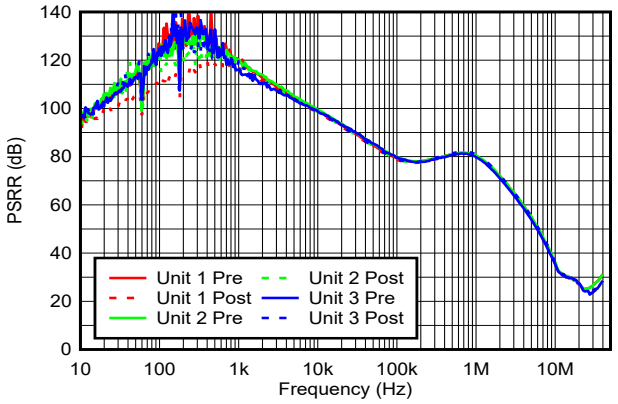


Figure 9-6. PSRR with I_{OUT} = 100 mA

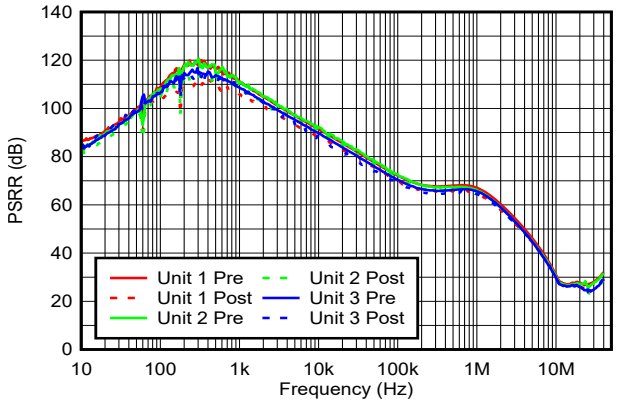


Figure 9-7. PSRR with I_{OUT} = 1 A

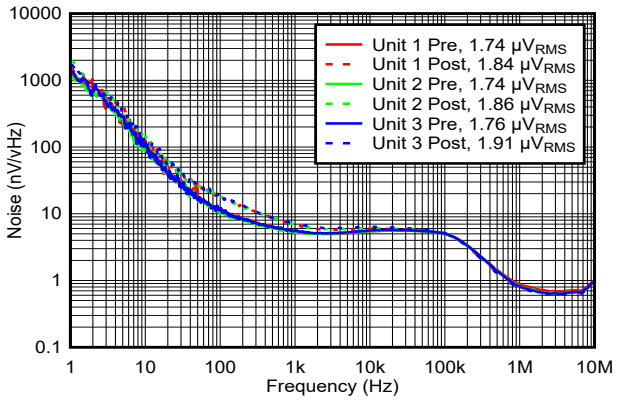


Figure 9-8. Noise Spectral Density with I_{OUT} = 100 mA

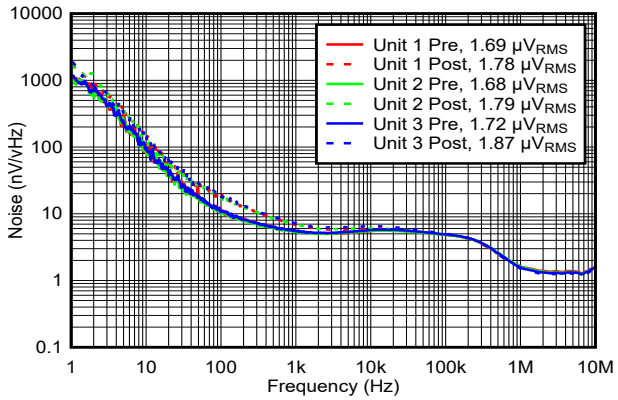
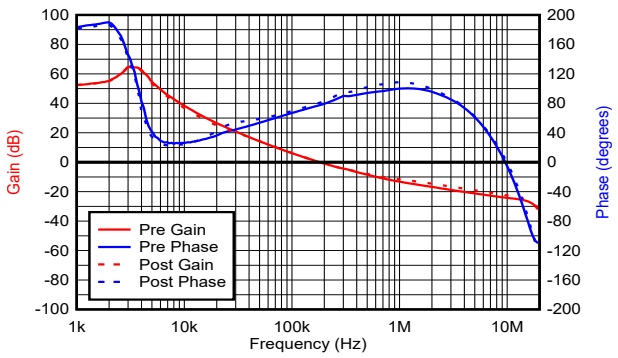


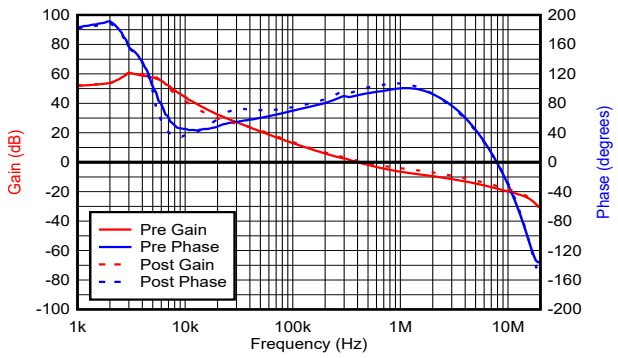
Figure 9-9. Noise Spectral Density with I_{OUT} = 1 A



Pre-Irradiation: Phase Margin = 78°, Gain Margin = 24 dB

Post-Irradiation: Phase Margin = 82°, Gain Margin = 23 dB

Figure 9-10. Bode Plot: Unit 1 with I_{OUT} = 100 mA

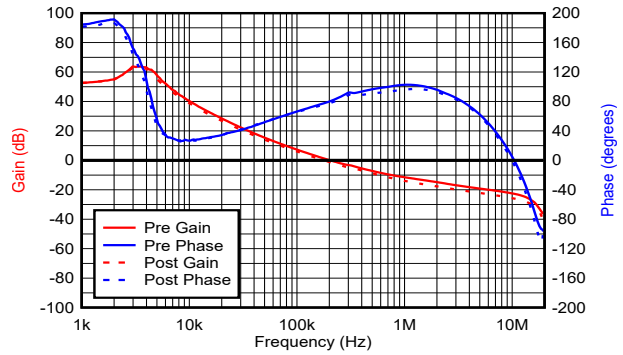


Pre-Irradiation: Phase Margin = 91°, Gain Margin = 18 dB

Post-Irradiation: Phase Margin = 100°, Gain Margin = 16 dB

Figure 9-11. Bode Plot: Unit 1 with I_{OUT} = 1 A

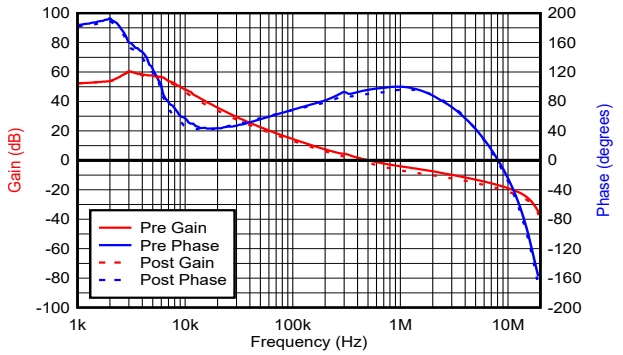
Copyright © 2023 Texas Instruments Incorporated



Pre-Irradiation: Phase Margin = 81°, Gain Margin = 23 dB

Post-Irradiation: Phase Margin = 76°, Gain Margin = 26 dB

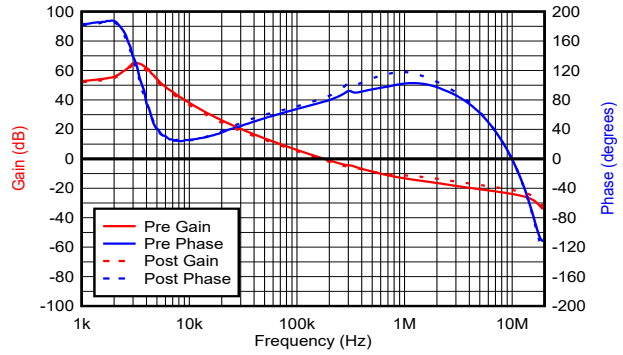
Figure 9-12. Bode Plot: Unit 2 with I_{OUT} = 100 mA



Pre-Irradiation: Phase Margin = 96°, Gain Margin = 17 dB

Post-Irradiation: Phase Margin = 88°, Gain Margin = 19 dB

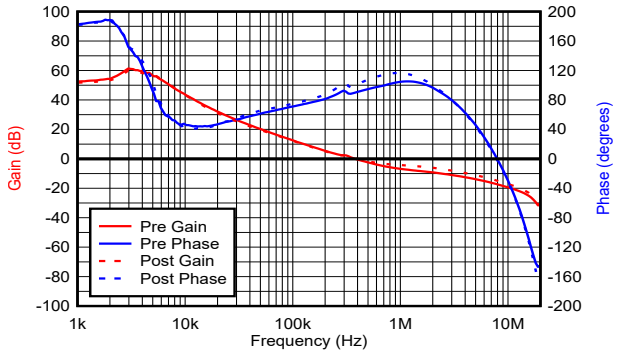
Figure 9-13. Bode Plot: Unit 2 with I_{OUT} = 1 A



Pre-Irradiation: Phase Margin = 78°, Gain Margin = 24 dB

Post-Irradiation: Phase Margin = 81°, Gain Margin = 21 dB

Figure 9-14. Bode Plot: Unit 3 with I_{OUT} = 100 mA



Pre-Irradiation: Phase Margin = 90°, Gain Margin = 18 dB

Post-Irradiation: Phase Margin = 101°, Gain Margin = 15 dB

Figure 9-15. Bode Plot: Unit 3 with I_{OUT} = 1 A

9.5 Power Supply Recommendations

This device is designed to operate with an input voltage supply from 0.85 V to 7 V. The minimum input voltage must provide adequate headroom greater than the dropout voltage for the device to have a regulated output. Additionally, a separate BIAS supply is normally used in order to reduce dropout voltage. The bias supply voltage range is from 2.2 V to 14 V (and at least as high as the input voltage supply); however, for optimal performance, it is recommended $V_{BIAS} \geq V_{OUT}$ + 1.6 V. For additional information view Section 8.3.1.

The internal power dissipation during device regulation, P_D, can be approximated using Equation 19.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_{IN_GND} \times V_{IN} + I_{BIAS} \times V_{BIAS} \quad (19)$$

The TPS7H1111 is a high-PSRR device. In order to obtain the full benefits of the high PSRR from V_{IN} to V_{OUT}, it is important that V_{BIAS} at the BIAS pin input is clean. Any ripple on the BIAS pin will couple from V_{BIAS} to V_{OUT} (reduced by $PSRR_{BIAS}$). The best way to ensure BIAS sees a clean input is to add an RC filter before the BIAS pin. Due to the limited current the BIAS pin consumes, the voltage drop across the resistor is generally acceptable. A suggested value for the RC filter is R = 10 Ω and C = 4.7 µF.

A bulk input capacitor of 10 µF with a 0.1 µF ceramic decoupling capacitor is generally sufficient for good performance. If the input supply is far away from the input of the TPS7H1111, a larger input capacitor such as 47 µF or 100 µF may be beneficial.

The TPS7H1111 is optimized for a single tantalum output capacitor of 220 µF or two 100 µF capacitors. Additionally, a single 0.1 µF ceramic capacitor may be used. Place the tantalum capacitor(s) near the output of the TPS7H1111 and place the ceramic capacitor near the point of load. See Section 8.3.8.1 for additional information.

Copyright © 2023 Texas Instruments Incorporated

9.6 Layout

9.6.1 Layout Guidelines

- Use traces or planes that are sized large enough to handle the input and output current with minimal voltage drop.
- Place the input capacitors close to the IN pins.
  - In some situations, the input capacitor can be placed further aware from the device to minimize magnetic noise coupling.
- Place the bulk output capacitor(s) near the OUT pins.
  - If a ceramic output capacitor is used, place it near the point of load. The TPS7H1111 does not benefit from output decoupling.
- Keep high noise circuits away from SS_SET, REF, and OUTS in order to create a clean V_{OUT} rail.
- Ensure inductance is minimized in the TPS7H1111 feedback loop (which consists going from the OUT to the OUTS pins)

9.6.2 Layout Example

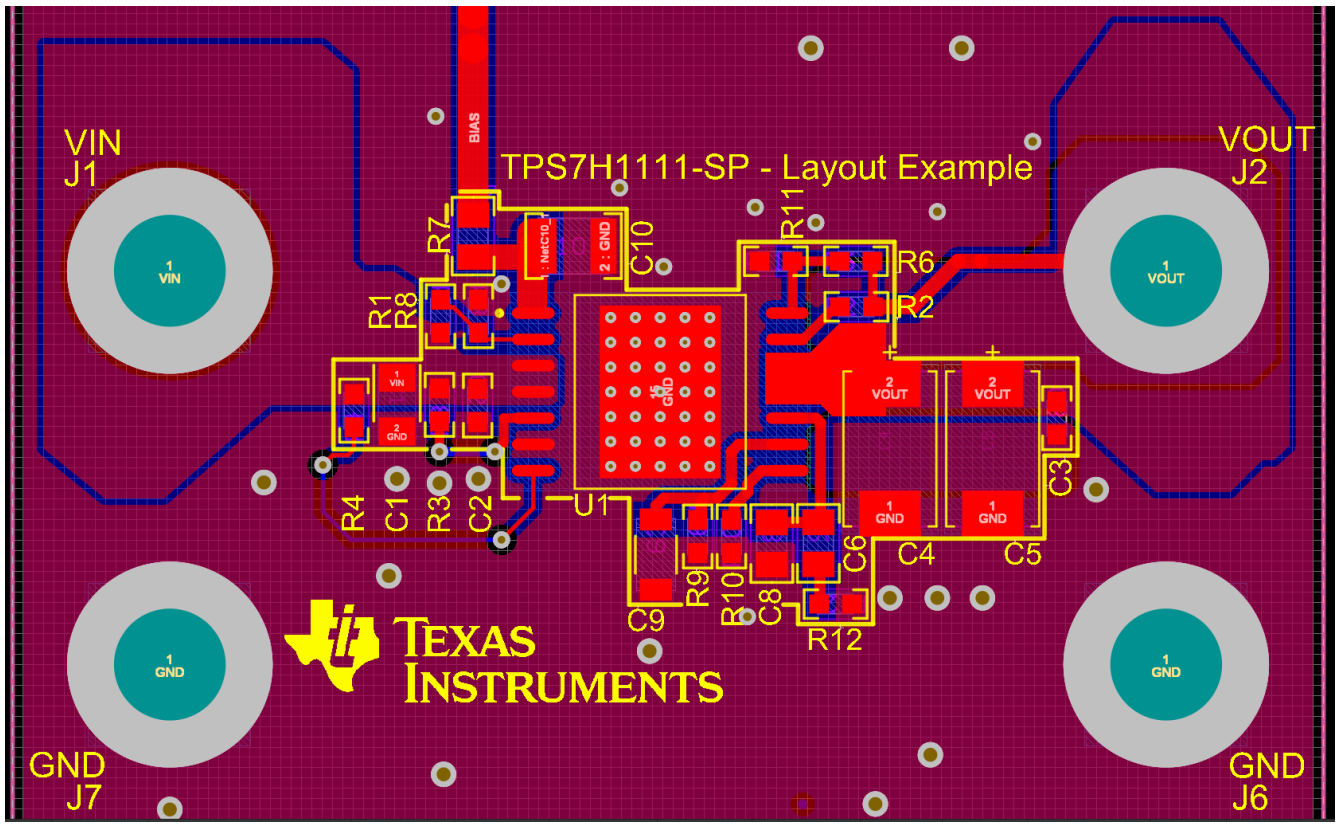


Figure 9-16. Printed Circuit Board Layout Example

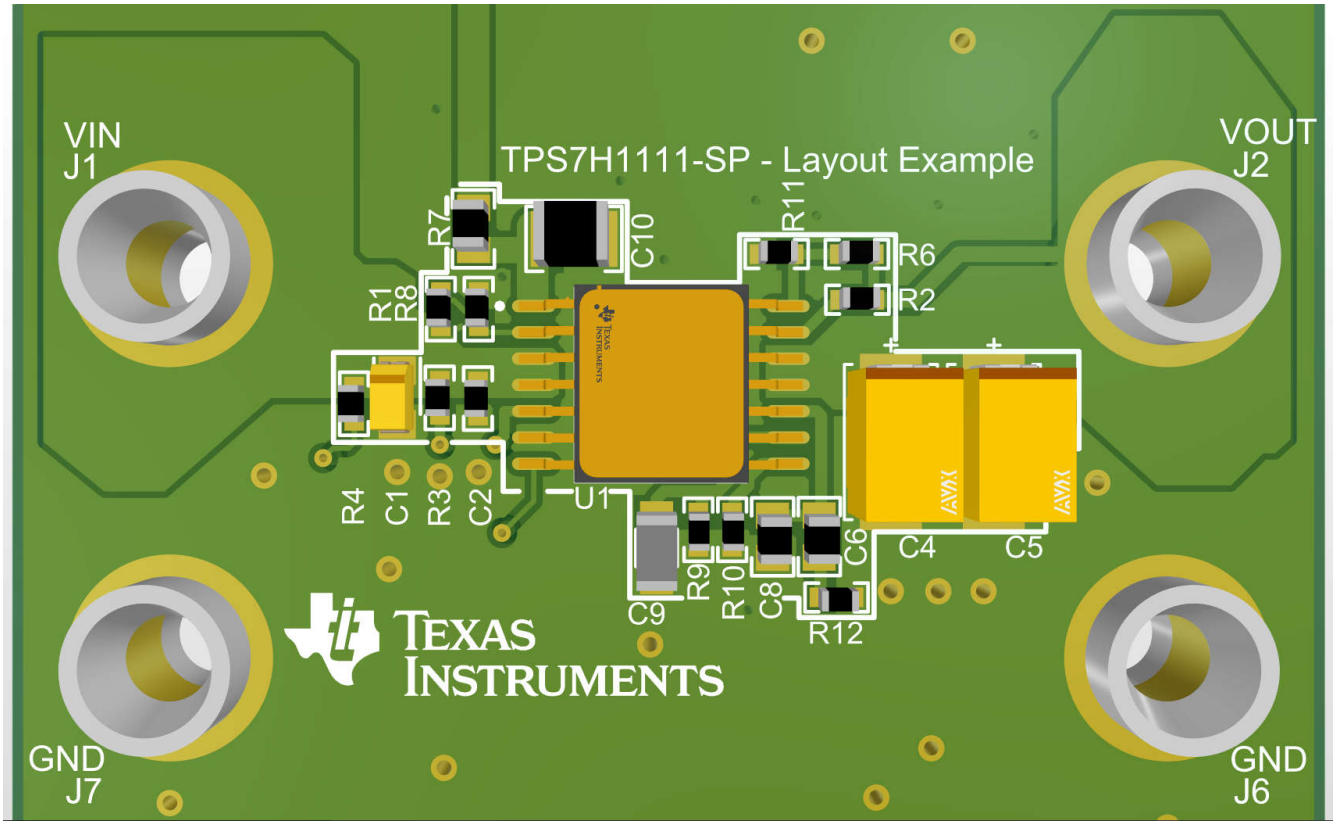


Figure 9-17. Printed Circuit Board Layout Example: 3D View

Copyright © 2023 Texas Instruments Incorporated

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.1.2 Related Documentation

- TPS7H1111-SP Total ionizing dose (TID) Radiation report
- TPS7H1111EVM-CVAL Evaluation Module user's guide
- Standard Microcircuit Drawing, 5962R21203
- Vendor Item Drawing, V62/23602

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2023) to Revision F (December 2023)	Page
• Updated the nominal mass of the plastic package	1
• Changed 5962R2120302PYE status from "Product preview" to "Production data"	1
• Removed known good die and associated die info	1
• Added orderable for "dummy" ceramic package	3
• Added updated thermal information for the TPS7H1111-SP QMLP version	7

Copyright © 2023 Texas Instruments Incorporated

Changes from Revision D (June 2023) to Revision E (August 2023) **Page**

- Corrected Bode plots for figures 7-23, 7-25, and 7-27 in the Typical Characteristics section..... 12

Copyright © 2023 Texas Instruments Incorporated

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2023 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R2120301VXC	Active	Production	CFP (HBL) | 14	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 125	5962R2120301VXC TPS7H1111MHBLV
5962R2120302PYE	Active	Production	HTSSOP (PWP) | 28	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	R2120302P
SN0014HBL	Active	Production	CFP (HBL) | 14	25 | TUBE	-	Call TI	Call TI	25 to 25	SN0014HBL-DC
TPS7H1111HBL/EM	Active	Production	CFP (HBL) | 14	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	25 to 25	TPS7H1111HBL EVAL ONLY
TPS7H1111MPWPTSEP	Active	Production	HTSSOP (PWP) | 28	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H1111PWP
V62/23602-01XE	Active	Production	HTSSOP (PWP) | 28	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	See TPS7H1111MPWPTSEP	7H1111PWP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS7H1111-SEP, TPS7H1111-SP :

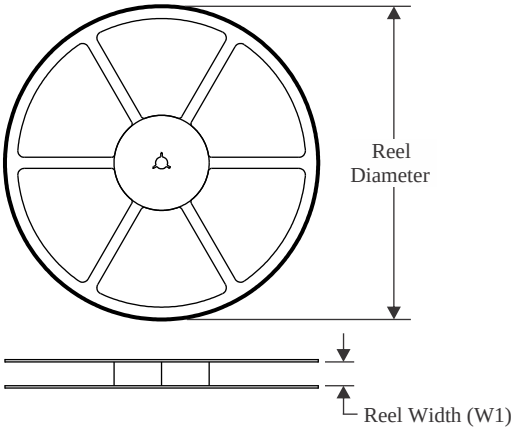
- Catalog : TPS7H1111-SEP
- Space : TPS7H1111-SP

NOTE: Qualified Version Definitions:

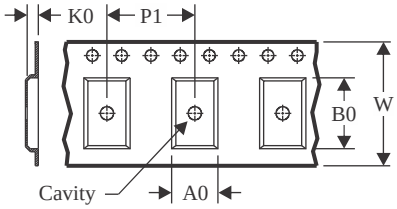
- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

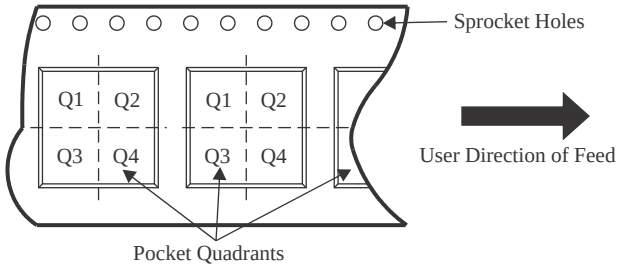


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

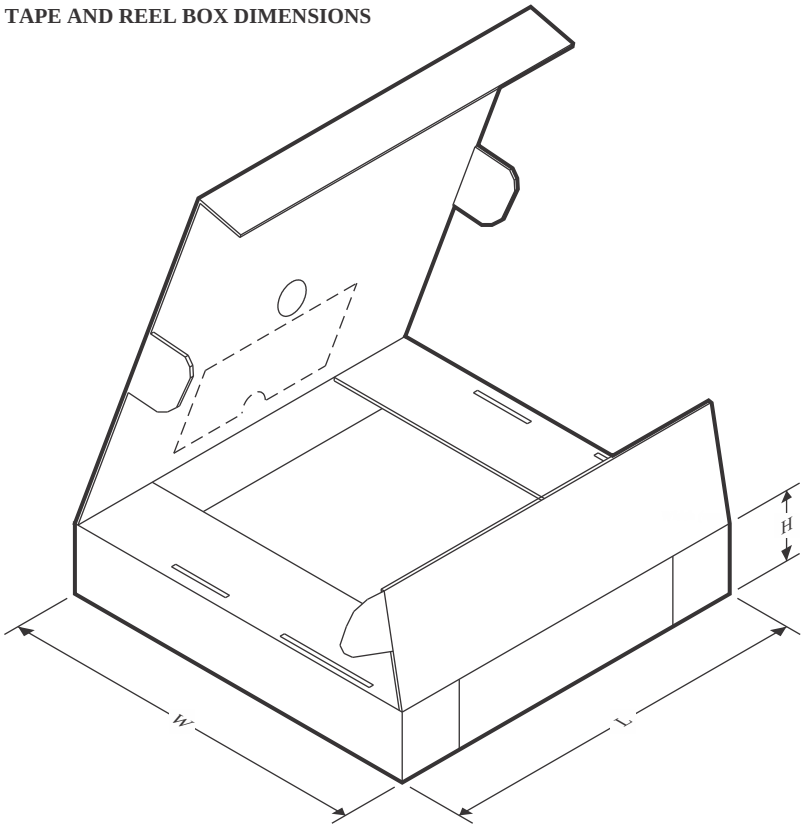
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
5962R2120302PYE	HTSSOP	PWP	28	250	178.0	16.4	6.95	10.0	1.7	8.0	16.0	Q1
TPS7H1111MPWPTSEP	HTSSOP	PWP	28	250	178.0	16.4	6.95	10.0	1.7	8.0	16.0	Q1

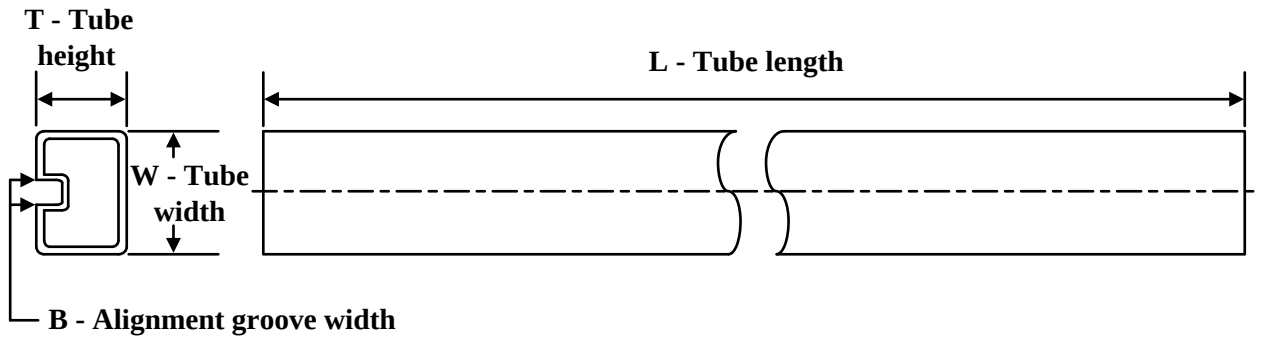
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
5962R2120302PYE	HTSSOP	PWP	28	250	210.0	185.0	35.0
TPS7H1111MPWPTSEP	HTSSOP	PWP	28	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

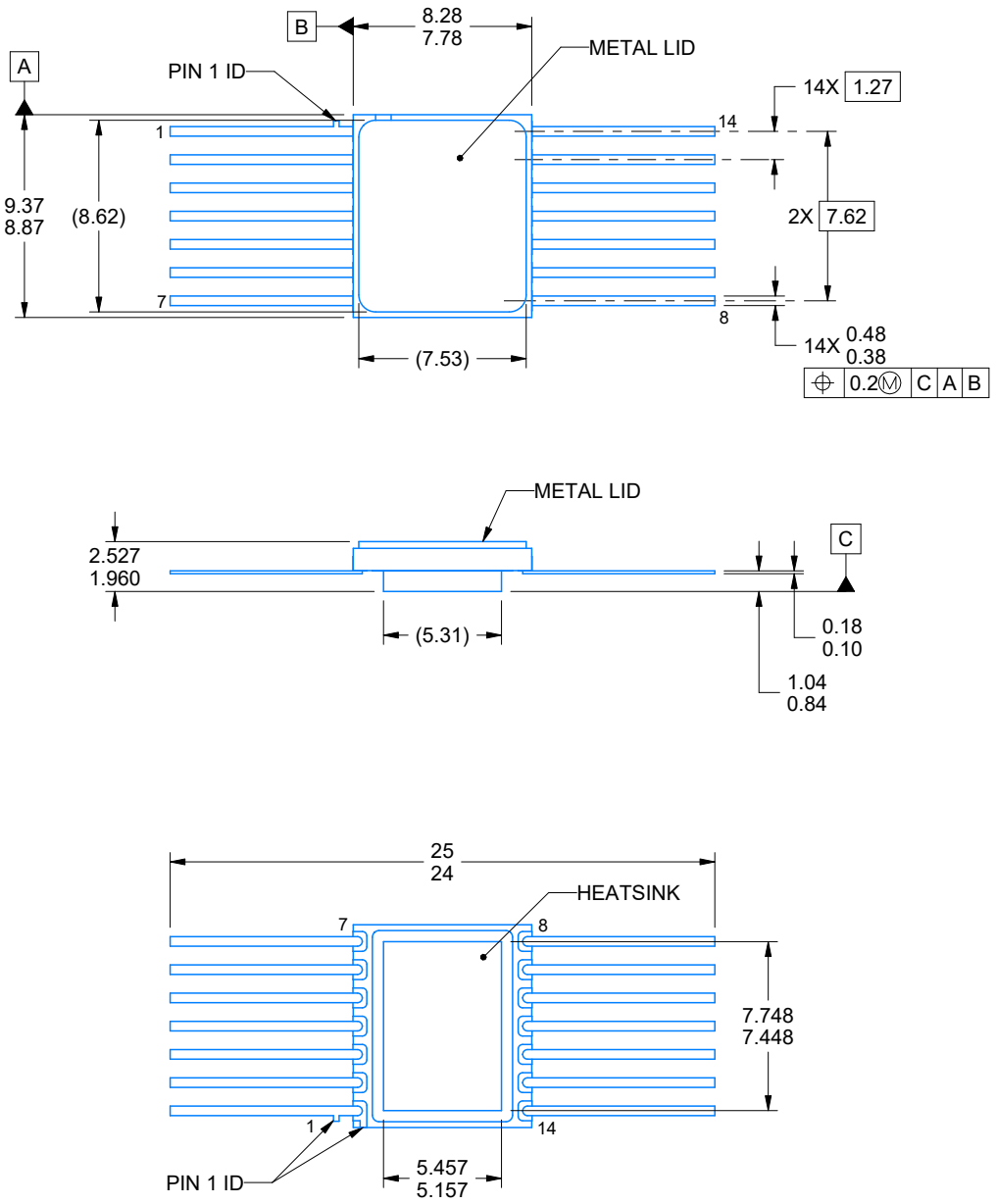
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R2120301VXC	HBL	CFP	14	25	506.98	26.16	6220	NA
TPS7H1111HBL/EM	HBL	CFP	14	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

HBL0014A

CFP - 2.527 mm max height

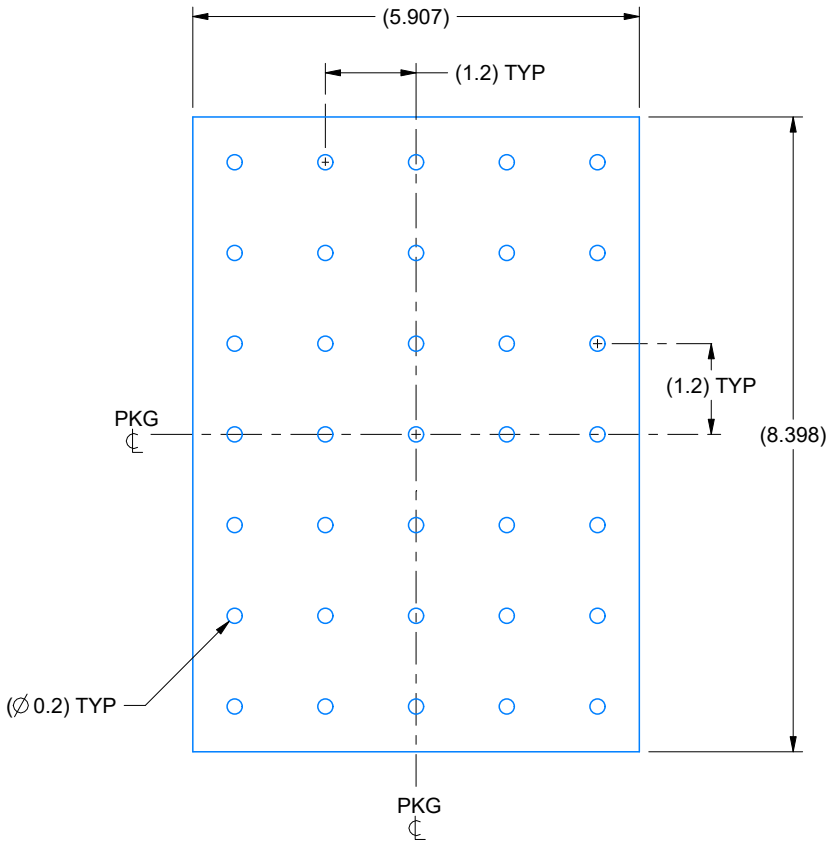
CERAMIC DUAL FLATPACK



4226657/A 03/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid is connected to Heatsink and pin 6
4. The terminals are gold plated.



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

4226657/A 03/2021

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2193915	03/24/2021	R. RAZAK / ANIS FAUZI

GENERIC PACKAGE VIEW

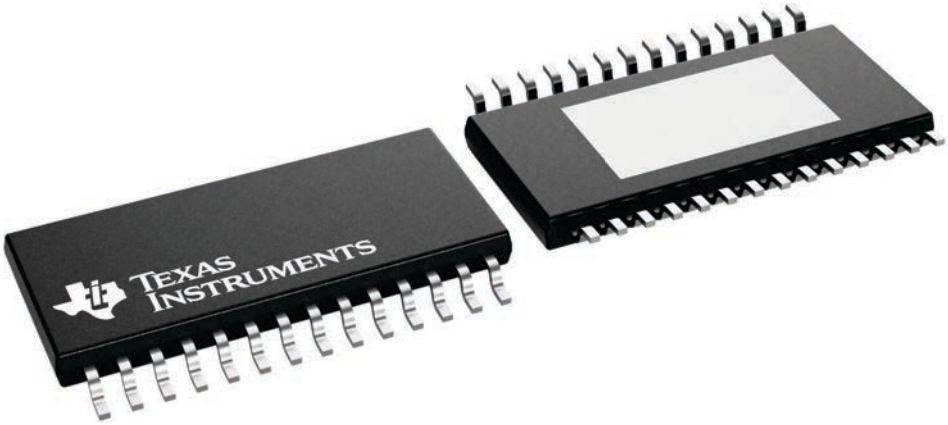
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

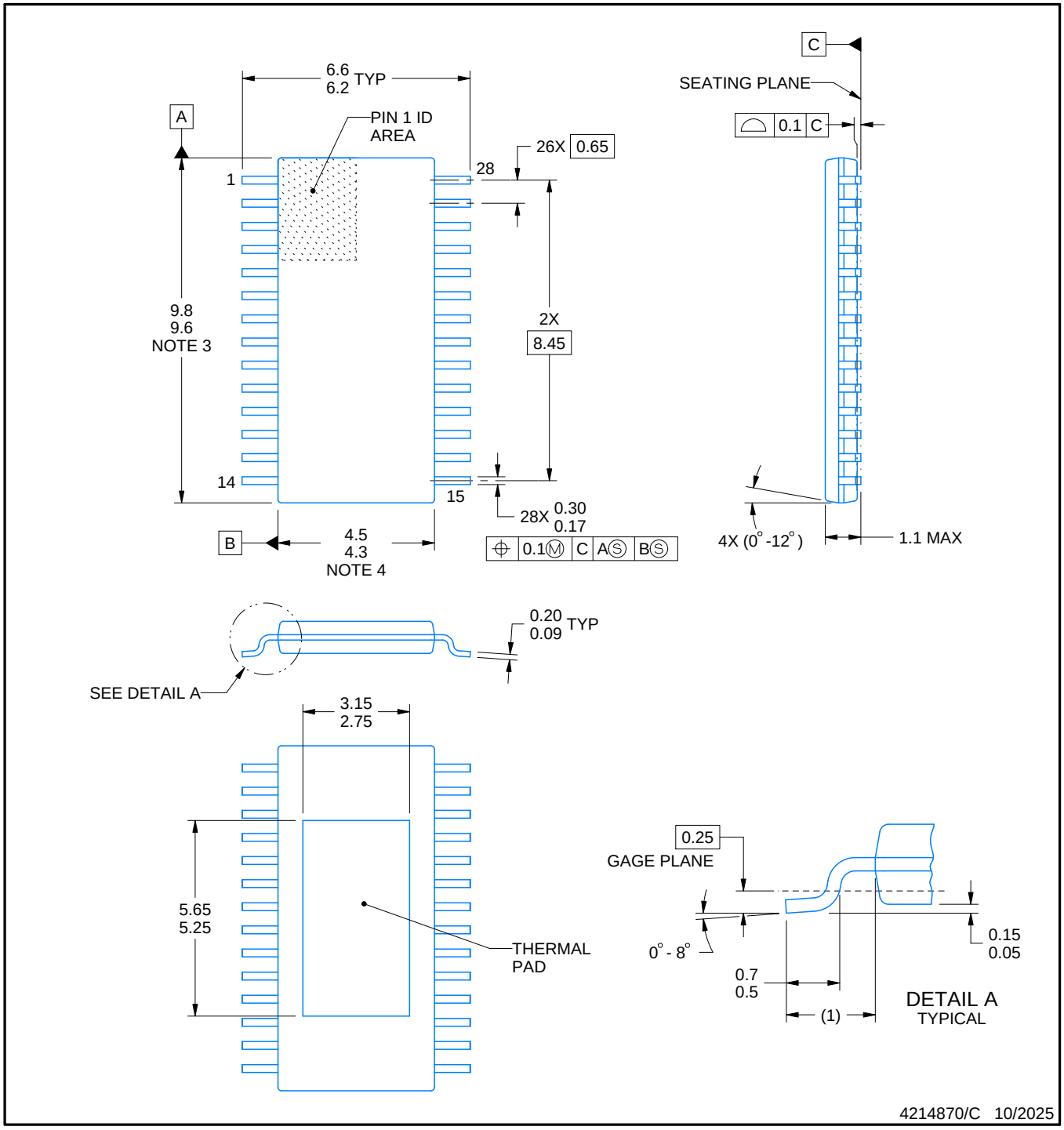


PACKAGE OUTLINE

PWP0028A

PowerPAD™ - 1.1 mm max height

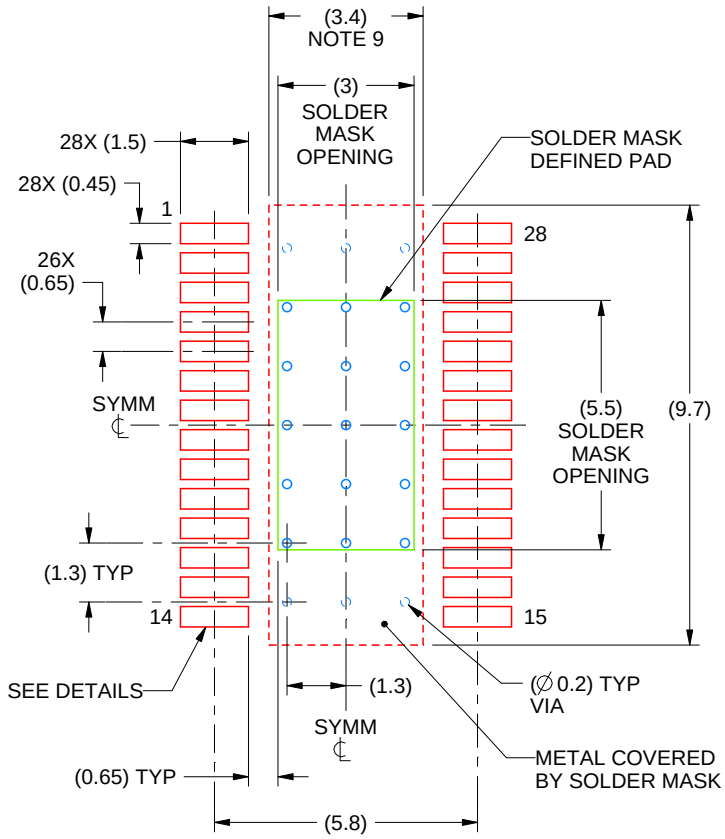
PLASTIC SMALL OUTLINE



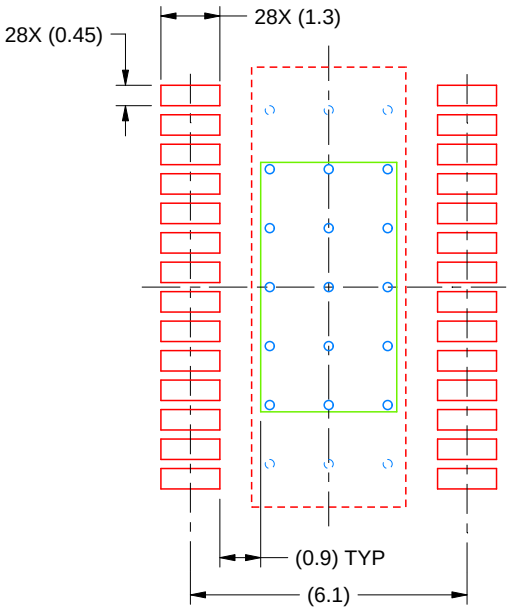
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-153, variation AET.

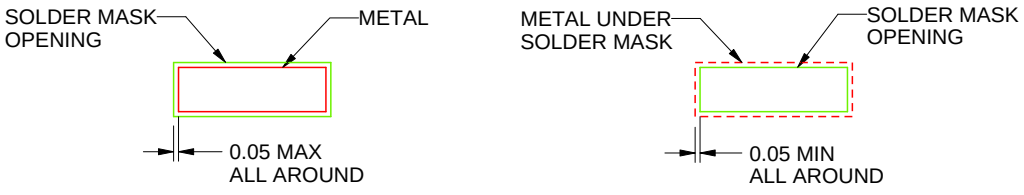


IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE



HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK
DEFINED

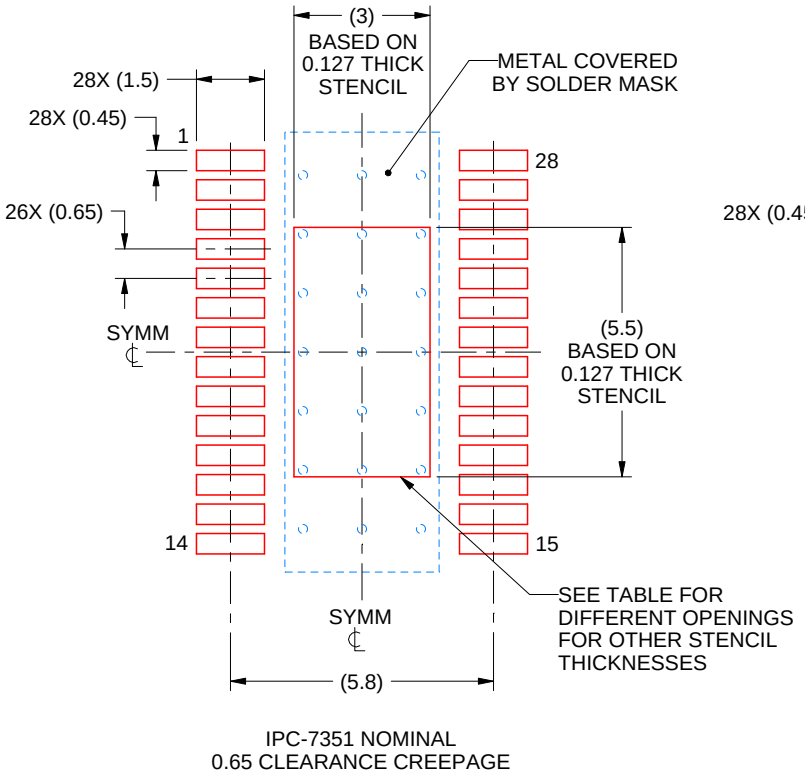
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

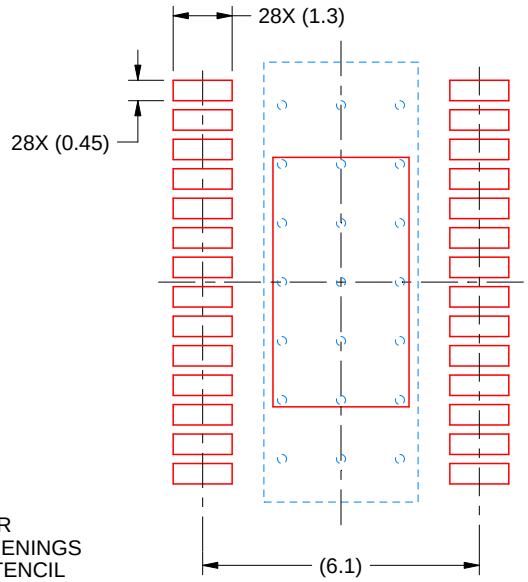
4214870/C 10/2025

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE



HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.55 X 6.37
0.127	3.0 X 5.5 (SHOWN)
0.152	2.88 X 5.16
0.178	2.66 X 4.77

4214870/C 10/2025

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025