TPS7H3014-SP and TPS7H3014-SEP Radiation-Hardened, 14V, 4-Channel Sequencer

1 Features

- Radiation performance:
  - Radiation hardness assurance (RHA) up to a total ionizing dose (TID) of 100 krad(Si) for the QML's and 50 krad(Si) for the SEP
  - Single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune up to linear energy transfer (LET) = 75 MeV-cm^2/mg for the QML's and 43 MeV-cm^2/mg for the SEP
  - Single-event functional interrupt (SEFI) and single-event transient (SET) characterized up to LET = 75 MeV-cm^2/mg for the QML's and 43 MeV-cm^2/mg for the SEP
- Wide supply IN voltage range (V_{IN}): 3V to 14V
- Sequence and monitor up to 4 voltage rails with a single device
  - Daisy chain capability for extended channel count
- Single resistor programmable global timers for:
  - Sequence up and down delay
  - Sequence up time to regulation
- Reverse order sequence down
- Precision threshold voltage and hysteresis current
  - V_{TH_SENSEx} of 599mV ±1% across: voltage, temperature, and radiation (TID)
  - I_{HYS_SENSEx} of 24µA ±3% across: voltage, temperature, and radiation (TID)
- Push-pull outputs with programmable pull-up voltage between 1.6V to 7V
  - Global ENx pull-up domain (V_{PULL_UP1})
  - Common SEQ_DONE and PWRGD pull-up domain (V_{PULL_UP2})
- $\overline{\text{FAULT}}$ open drain output for monitoring of state machine induced faults
- Plastic packages outgas tested per ASTM E595
- Available in military (–55°C to 125°C) temperature range

2 Applications

- Satellite electrical power system (EPS)
- Control sequence and monitoring for complex digital processors such as: FPGAs, SoCs, AFEs, and power systems for space applications

3 Description

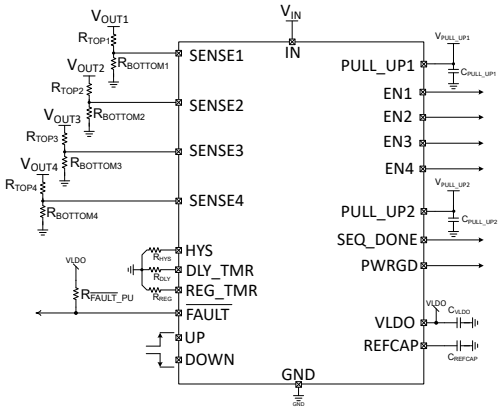
The TPS7H3014 is an integrated, 3V to 14V, four-channel radiation-hardness-assured power-supply sequencer. Channel count can be expanded by connecting multiple devices in a daisy-chain configuration. The device provides sequence up and down control signals for integrated circuits (IC) with active high ("on") inputs. In addition SEQ_DONE and PWRGD flags are provided to monitor the sequence and power status of the monitored power tree.

An accurate 599mV ±1% threshold voltage and a 24µA ±3% hysteresis current provide programmable rise and fall monitoring voltages. The rise and fall delay time is globally programmed via a single resistor. Also, a time-to-regulation timer is provided to track the rising voltage on SENSEx. In addition to these features, a FAULT detection pin is incorporated to monitor internally generated faults and provide increased system level reliability for power sequencing space applications. A standard microcircuit drawing (SMD) is available for the QML variant, 5962R2320101VXC.

Device Information

PART NUMBER(1)	GRADE(2)	PACKAGE(3)
5962R2320101VXC	QMLV-RHA	22-pin ceramic (CFP) 6.21mm x 7.69mm Mass = 415.6mg
TPS7H3014HFT/EM	Engineering sample	
TPS7H3014MPWTSEP	SEP	24-pin Plastic (TSSOP) 4.4mm x 7.8mm Mass = 102.3mg

(1) For additional information view the Device Options table.
(2) For additional information about part grade, view SLYB235.
(3) Dimensions and mass are nominal values.



Typical Application

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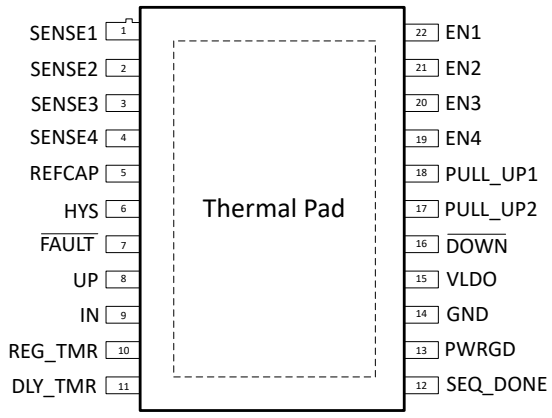
4 Device Options

GENERIC PART NUMBER	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER
TPS7H3014-SP	TID of 100krad(Si) RLAT, DSEE free to 75 MeV-cm^2/mg	QMLV-RHA	22-pin CFP HFT	5962R2320101VXC
	None	Engineering model(3)	22-pin CFP HFT	TPS7H3014HFT/EM
TPS7H3014-SEP	TID of 50 krad(Si) RLAT, DSEE free to 43 MeV-cm^2/mg	Space Enhanced Plastic	24-pin TSSOP PW	TPS7H3014MPWTSEP

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) For additional information about part grade, view SLYB235.
(3) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (such as no burn-in and only 25°C testing). These units are not suitable for qualification, production, radiation testing, or flight use. Parts are not warranted as to performance over temperature or operating life.

5 Pin Configuration and Functions

HFT Package
22-Pin CFP
Top View



PW Package
24-Pin TSSOP
Top View

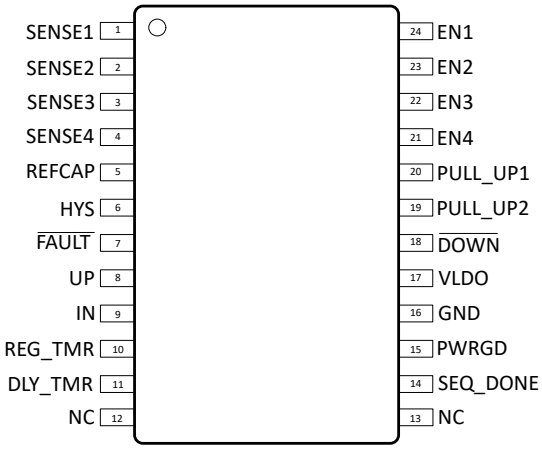


Table 5-1. Pin Functions

PIN			I/O[1]	DESCRIPTION
NAME	HFT (22) NO.	PW (24) NO.		
SENSE1	1	1	I	Non Inverting input of the comparator used to monitor the first rail to be sequenced up/down. Connect an external resistive divider between the rail to be monitored and GND with the middle point tied to the SENSE1, to set the V_{ON} and V_{OFF} voltages. A voltage greater than 599mV (typ.) on this pin is considered as a regulated voltage rail (V_{ON}). The V_{OFF} is set by the I_{HYS} current and the top resistor from the resistive divider. Refer to Top and Bottom Resistive Divider Design Equations.
SENSE2	2	2	I	Non Inverting input of the comparator used to monitor the second rail to be sequenced up/down. Connect an external resistive divider between the rail to be monitored and GND with the middle point tied to the SENSE2, to set the V_{ON} and V_{OFF} voltages. A voltage greater than 599mV (typ.) on this pin is considered as a regulated voltage rail (V_{ON}). The V_{OFF} is set by the I_{HYS} current and the top resistor from the resistive divider. Refer to Top and Bottom Resistive Divider Design Equations.
SENSE3	3	3	I	Non Inverting input of the comparator used to monitor the third rail to be sequenced up/down. Connect an external resistive divider between the rail to be monitored and GND with the middle point tied to the SENSE3, to set the V_{ON} and V_{OFF} voltages. A voltage greater than 599mV (typ.) on this pin is considered as a regulated voltage rail (V_{ON}). The V_{OFF} is set by the I_{HYS} current and the top resistor from the resistive divider. Refer to Top and Bottom Resistive Divider Design Equations.
SENSE4	4	4	I	Non Inverting input of the comparator used to monitor the fourth rail to be sequenced up/down. Connect an external resistive divider between the rail to be monitored and GND with the middle point tied to the SENSE4, to set the V_{ON} and V_{OFF} voltages. A voltage greater than 599mV (typ.) on this pin is considered as a regulated voltage rail (V_{ON}). The V_{OFF} is set by the I_{HYS} current and the top resistor from the resistive divider. Refer to Top and Bottom Resistive Divider Design Equations.
REFCAP	5	5	O	1.2V internal reference. Requires a 470nF external capacitor to GND. Do not load this pin.
HYS	6	6	O	Hysteresis. Connect a 50kΩ resistor between this pin and GND, to program the hysteresis current (typically 24µA) at SENSE1 to SENSE4. Is recommended using a resistor with 0.1% tolerance for accuracy purposes.
$\overline{\text{FAULT}}$	7	7	O	$\overline{\text{FAULT}}$. Open drain output which is forced low by the state machine to indicate an internally generated fault. Is recommended to pull-up this pin to VLDO with a 10kΩ. However a different external voltage source can be used as the pull-up as long as is stable and does not change it value during the operation of the device.

Table 5-1. Pin Functions (continued)

PIN			I/O[1]	DESCRIPTION
NAME	HFT (22) NO.	PW (24) NO.		
UP	8	8	I	Non inverting input of a comparator. A voltage greater than 599mV (typ.) will induce a rising edge and will start a sequence up. This pin can be driven by an external controller, or connected to a main rail trough an external resistive divider with the middle point connected to the UP pin to start the sequence up automatically. An fix hysteresis of 100mV (typ.) is present for noise stability.
IN	9	9	I	Input supply to the device. Input voltage range is from 3V to 14V. Connect at least a 0.1µF capacitor as close as possible to the pin.
REG_TMR	10	10	I/O	Time to regulation timer. Connect a resistor to GND between 10.5kΩ and 1.18MΩ to set the allowed time for a $SENSE_x$ rail to reach the regulation threshold. The delay can be adjusted from 0.25ms to 25ms. Leave this pin floating when is desired to deactivate this feature.
DLY_TMR	11	11	I/O	Delay timer. Connect a resistor to GND between 10.5kΩ and 1.18MΩ to set the sequence up and down delay. The delay can be adjusted from 0.25ms to 25ms. Leave this pin floating when no delay is needed on the system.
SEQ_DONE	12	14	O	Sequence done. Push-Pull output with V_{OH} level set by PULL_UP2 input supply voltage, that indicates when the sequence up or down is completed.
PWRGD	13	15	O	Power Good. Push-Pull output with V_{OH} level set by PULL_UP2, input input supply voltage, that indicates when all rails (SENSE1 to SENSE4) are in regulation.
GND	14	16	—	Ground
VLDO	15	17	O	Output of internal regulator. Requires at least 1µF external capacitor to GND. Allowed loading of this regulator are: $\overline{FAULT}$ pull-up using a 10kΩ or to turn-off unused channels by connecting directly to SENSE2 to SENSE4 as needed.
$\overline{DOWN}$	16	18	I	Non inverting input of a comparator. A voltage lower than 498mV (typ.) will induce a falling edge and will start a sequence down. This pin can be driven by an external controller, or connected to a main rail trough an external resistive divider with the middle point connected to the $\overline{DOWN}$ pin to start the sequence down automatically. An fix hysteresis of 100mV (typ.) is present for noise stability.
PULL_UP2	17	19	I	Input supply voltage to program the pull-up voltage for the push-pull output stage on SEQ_DONE and PWRGD. Connect at least a 1µF capacitor as close as possible to the pin.
PULL_UP1	18	20	I	Input supply voltage to program the global pull-up voltage for the push-pull output stages on EN1 to EN4. Connect at least a 1µF capacitor as close as possible to the pin.
EN4	19	21	O	Enable 4. Push pull output with V_{OH} level set by the PULL_UP1 input supply voltage. Connect to the logical enable signal of the device to control and to be monitor by SENSE4.
EN3	20	22	O	Enable 3. Push pull output with V_{OH} level set by PULL_UP1 input supply voltage. Connect to the logical enable signal of the device to control and to be monitor by SENSE3.
EN2	21	23	O	Enable 2. Push pull output with V_{OH} level set by PULL_UP1 input supply voltage. Connect to the logical enable signal of the device to control and to be monitor by SENSE2.
EN1	22	24	O	Enable 1. Push pull output with V_{OH} level set by PULL_UP1 input supply voltage. Connect to the logical enable signal of the device to control and to be monitor by SENSE1.
NC	—	12, 13	—	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.
Thermal pad		—	—	Internally grounded. It is recommended to connect this metal thermal pad to a large ground plane for effective heat dissipation.
Metal lid	Lid		—	The lid is internally connected to the thermal pad and GND through the seal ring.

(1) I = Input, O = Output, I/O = Input or Output, — = Other

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Input voltage	IN	–0.3	16	V
	UP, $\overline{\text{DOWN}}$	–0.3	7.5	
	SENSE1, SENSE2, SENSE3, SENSE4	–0.3	3.6	
	PULL_UP1, PULL_UP2	–0.3	7.5	
	$\overline{\text{FAULT}}$	–0.3	7.5	
	DLY_TMR, REG_TMR	–0.3	3.6	
Output voltage	VLDO	–0.3	3.6	V
	EN1, EN2, EN3, EN4	–0.3	7.5	
	REFCAP	–0.3	2	
	HYS	–0.3	3.6	
	SEQ_DONE, PWRGD	–0.3	7.5	
Output current	EN1, EN2, EN3, EN4	–20	20	mA
	SEQ_DONE, PWRGD	–20	20	
Junction temperature	T_J	–55	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages values are with respect to GND.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating temperature range, T_A = –55°C to 125°C (unless otherwise noted) (1)

		MIN	NOM	MAX	UNIT
Input voltage	IN	3		14	V
	UP, $\overline{\text{DOWN}}$	0		7	
	SENSE1, SENSE2, SENSE3, SENSE4	0		3.5	
	PULL_UP1, PULL_UP2	1.6		7	
	$\overline{\text{FAULT}}$	0		7	
Output voltage	EN1, EN2, EN3, EN4	0		7	V
	SEQ_DONE, PWRGD	0		7	
Output current	EN1, EN2, EN3, EN4	–10		10	mA
	SEQ_DONE,PWRGD	–10		10	
	$\overline{\text{FAULT}}$	–2			
Junction temperature	T_J	–55		125	°C
Input voltage slew rate	SR_{IN}	0.001		10	V/µs

(1) All voltages values are with respect to GND.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7H3014-SEP	TPS7H3014-SP	UNIT
		PW (TSSOP)	HFT (CFP)	
		24 pins	22 pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66	34.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	7.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.8	17.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16	16.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	8.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	33.3	17	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10.5kΩ, R_{REG_TMR} = 10.5kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, over temperature range (T_A= –55°C to 125°C), unless otherwise noted; includes group E radiation testing at T_A = 25°C for QML RHA devices (1) (2)

PARAMETER		TEST CONDITIONS		SUB-GROUP (3)	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGES AND CURRENTS								
I_{Q_IN}	V_{IN} quiescent current	In Waiting to sequence up and down states with all outputs floating. See State Diagram		1, 2, 3		2.5	4	mA
$UVLO_{RISE}$	V_{IN} rising undervoltage lockout			1, 2, 3	2.72	2.79	2.84	V
$UVLO_{FALL}$	V_{IN} falling udervoltage lockout			1, 2, 3	2.59	2.64	2.69	V
V_{LDO}	Internal linear regulator output voltage	5V ≤ V_{IN} ≤ 14V		1, 2, 3	3.19	3.29	3.38	V
		V_{IN} < 3.24V		1, 2, 3	97%	99%		× V_{IN}
REFCAP	Internal bandgap voltage			1, 2, 3	1.188	1.2	1.212	V
V_{POR_IN}	Power on reset voltage (4)	1.6V ≤ V_{PULL_UPx} ≤ 7V, V_{OL} ≤ 320mV with I_{ENx} = –2mA		1, 2, 3		1.41	2	V
$V_{POR\_PULL\_UPx}$	Power on reset voltage (5)	V_{IN} = 0V, V_{OL} ≤ 320mV with I_{ENx} = –100µA		1, 2, 3		0.89	1.4	V
SENSE1 TO SENSE4, UP AND $\overline{\text{DOWN}}$ COMPARATOR INPUTS								
V_{TH_SENSEx}	Threshold voltage at SENSEx			1, 2, 3	593	599	605	mV
I_{HYS_SENSEx}	SENSEx hysteresis current	V_{SENSEx} = 700mV		1, 2, 3	23.28	24	24.72	µA
I_{LKG_SENSEx}	Input leakage current at SENSEx	V_{SENSEx} = 500mV		1, 2, 3		2	100	nA
V_{TH_UP}	Rising threshold voltage at UP			1, 2, 3	580	598	615	mV
$V_{TH\_\overline{DOWN}}$	Falling threshold voltage at $\overline{\text{DOWN}}$			1, 2, 3	483	498	512	mV
$V_{HYS\_UP\_\overline{DOWN}}$	UP and $\overline{\text{DOWN}}$ hysteresis voltage			1, 2, 3		100		mV
$I_{LKG\_UP\_\overline{DOWN}}$	Input leakage current at UP and $\overline{\text{DOWN}}$	V_{UP} = $V_{\overline{DOWN}}$ = 500mV		1, 2, 3		2	100	nA
V_{TURN_OFF}	Channel 2, 3, 4 turn off voltage			1, 2, 3	87%	89%	91%	× VLDO
EN1 TO EN4, SEQ_DONE AND PWRGD PUSH PULL OUTPUTS								
V_{OL_ENx}	Low-level ENx output voltage	1.6V ≤ V_{PULL_UP1} ≤ 7V	I_{LOAD} = –2mA	1, 2, 3			10%	x V_{PULL_UP1}
			I_{LOAD} = –10mA	1, 2, 3			25%	
V_{OH_ENx}	High-level ENx output voltage	1.6V ≤ V_{PULL_UP1} ≤ 7V	I_{LOAD} = 2mA	1, 2, 3	90%			
			I_{LOAD} = 10mA	1, 2, 3	70%			
$V_{OL\_SEQ\_DONE}$	Low-level SEQ_DONE output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = –2mA	1, 2, 3			10%	x V_{PULL_UP2}
			I_{LOAD} = –10mA	1, 2, 3			25%	
$V_{OH\_SEQ\_DONE}$	High-level SEQ_DONE output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = 2mA	1, 2, 3	90%			
			I_{LOAD} = 10mA	1, 2, 3	70%			
V_{OL_PWRGD}	Low-level PWRGD output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = –2mA	1, 2, 3			10%	
			I_{LOAD} = –10mA	1, 2, 3			25%	
V_{OH_PWRGD}	High-level PWRGD output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = 2mA	1, 2, 3	90%			
			I_{LOAD} = 10mA	1, 2, 3	70%			

6.5 Electrical Characteristics (continued)

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10.5kΩ, R_{REG_TMR} = 10.5kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, over temperature range (T_A= –55°C to 125°C), unless otherwise noted; includes group E radiation testing at T_A = 25°C for QML RHA devices (1) (2)

PARAMETER		TEST CONDITIONS		SUB-GROUP (3)	MIN	TYP	MAX	UNIT
$PULL\_UPx_{LKG}$	PULL_UPx leakage current	V_{PULL_UPx} = 7V		1, 2, 3		48	121	µA
SR_{ENx_RISE}	Enable rising output voltage slew rate	10% to 90% of V_{PULL_UP1}, R_{LOAD} = 50kΩ, C_{LOAD} = 100pF	1.6V ≤ V_{PULL_UP1} ≤ 7V	9, 10, 11	17	125		V/µs
$SR_{SEQ\_DONE\_RISE}$	SEQ_DONE rising output voltage slew rate	10% to 90% of V_{PULL_UP2}, R_{LOAD} = 50kΩ, C_{LOAD} = 100pF	1.6V ≤ V_{PULL_UP2} ≤ 7V	9, 10, 11	17	125		
SR_{PWRGD_RISE}	PWRGD rising output voltage slew rate			9, 10, 11	17	125		
SR_{ENx_FALL}	Enable falling output voltage slew rate	90% to 10% of V_{PULL_UP1}, R_{LOAD} = 50kΩ, C_{LOAD} = 100pF	1.6V ≤ V_{PULL_UP1} ≤ 7V	9, 10, 11	44	126		
$SR_{SEQ\_DONE\_FALL}$	SEQ_DONE falling output voltage slew rate		1.6V ≤ V_{PULL_UP2} ≤ 7V	9, 10, 11	44	126		
SR_{PWRGD_FALL}	PWRGD falling output voltage slew rate			9, 10, 11	44	126		
$R_{ENx\_PULL\_UP}$	EN PMOS source output resistance	I_{LOAD} = 2mA	V_{PULL_UP1} = 1.6V	1, 2, 3		18	40	Ω
			V_{PULL_UP1} = 7V	1, 2, 3		7	20	
$R_{SEQ\_DONE\_PULL\_UP}$	SEQ_DONE PMOS source output resistance	I_{LOAD} = 2mA	V_{PULL_UP2} = 1.6V	1, 2, 3		18	40	
			V_{PULL_UP2} = 7V	1, 2, 3		7	20	
$R_{PWRGD\_PULL\_UP}$	PWRGD PMOS source output resistance	I_{LOAD} = 2mA	V_{PULL_UP2} = 1.6V	1, 2, 3		18	40	
			V_{PULL_UP2} = 7V	1, 2, 3		7	20	
$R_{ENx\_PULL\_DOWN}$	EN NMOS sink output resistance	I_{LOAD} = –2mA, 1.6V ≤ V_{PULL_UP1} ≤ 7V		1, 2, 3		7	28	
$R_{SEQ\_DONE\_PULL\_DOWN}$	SEQ_DONE NMOS sink output resistance	I_{LOAD} = –2mA, 1.6V ≤ V_{PULL_UP1} ≤ 7V		1, 2, 3		7	28	
$R_{PWRGD\_PULL\_DOWN}$	PWRGD NMOS sink output resistance	I_{LOAD} = –2mA, 1.6V ≤ V_{PULL_UP1} ≤ 7V		1, 2, 3		7	28	
$\overline{FAULT}$ OUTPUT								
$R_{\overline{FAULT}\_PULL\_DOWN}$	$\overline{FAULT}$ pull down resistance	$I_{\overline{FAULT}}$ = 100µA		1, 2, 3		131	512	Ω
$I_{LKG\_\overline{FAULT}}$	$\overline{FAULT}$ leakage current	$V_{\overline{FAULT}}$ = 7V		1, 2, 3		23	600	nA
THERMAL PROTECTION								
T_{SD_ENTER}	Thermal shutdown enter temperature					177		°C
T_{SD_EXIT}	Thermal shutdown exit temperature					164		

6.5 Electrical Characteristics (continued)

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10.5kΩ, R_{REG_TMR} = 10.5kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, over temperature range (T_A= –55°C to 125°C), unless otherwise noted; includes group E radiation testing at T_A = 25°C for QML RHA devices (1) (2)

PARAMETER		TEST CONDITIONS	SUB-GROUP (3)	MIN	TYP	MAX	UNIT
DELAY AND TIME TO REGULATION TIMERS							
t_{DLY_TMR}	Delay time	R_{DLY_TMR} = 10.5kΩ	9, 10, 11	0.205	0.268	0.342	ms
		R_{DLY_TMR} = 619kΩ	9, 10, 11	10.77	12.5	14.14	
		R_{DLY_TMR} = 1.18MΩ	9, 10, 11	20	23.37	27.2	
t_{REG_TMR}	Time to regulation	R_{REG_TMR} = 10.5kΩ	9, 10, 11	0.197	0.264	0.34	
		R_{REG_TMR} = 619kΩ	9, 10, 11	10.8	12.4	14.1	
		R_{REG_TMR} = 1.18MΩ	9, 10, 11	20.3	23.63	27.2	

(1) See the 5962R2320101VXC SMD (standard microcircuit drawing) for additional information on the RHA devices.
(2) All voltage values are with respect to GND.
(3) For subgroup definitions, see Quality Conformance Inspection table.
(4) V_{POR_IN} is the minimum V_{IN} voltage for a controlled output state, when 1.6V ≤ V_{PULL_UPx} ≤ 7V. Below V_{POR_IN}, the output cannot be determined.
(5) $V_{POR\_PULL\_UPx}$ is the minimum V_{PULL_UPx} voltage for a controlled output state, when V_{IN} ≤ 3V. Below $V_{POR\_PULL\_UPx}$ the output cannot be determined.

6.6 Timing Requirements

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10.5kΩ, R_{REG_TMR} = 10.5kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, over temperature range (T_A = –55°C to 125°C) unless otherwise noted; includes group E radiation testing at T_A = 25°C for RHA devices (1)

PARAMETER		TEST CONDITIONS	SUB-GROUP (2)	MIN	TYP	MAX	UNIT
$t_{Start\_up\_delay}$	Start-up delay time (3)	V_{REFCAP} ≥ 1.1V, See Figure 7-1	9, 10, 11			2.8	ms
t_{pd_ENx}	ENx propagation delay	DLY_TMR = Open, REG_TMR=Open, See Figure 7-2 and Figure 7-3	9, 10, 11		3.4	6.5	µs
$t_{pd\_SEQ\_DONE}$	SEQ_DONE propagation delay	DLY_TMR = Open, REG_TMR=Open, See Figure 7-4 and Figure 7-5	9, 10, 11		3.4	6.5	
t_{pd_PWRGD}	PWRGD propagation delay	DLY_TMR = Open, REG_TMR=Open, See Figure 7-6 and Figure 7-7	9, 10, 11		3.4	6.5	
$t_{pd\_SM\_FAULT}$	State machine fault propagation delay	In Waiting to Sequence DOWN State from 33% of SENSE1 ↓ to 82% PWRGD ↓ See Figure 7-8 and State Diagram.	9, 10, 11		3.4	4.3	
t_{MIN_UP}	V_{UP} rising minimum time for valid UP	DLY_TMR = Open, See Figure 7-10	9, 10, 11		0.27	0.7	µs
$t_{MIN\_\overline{DOWN}}$	V_{DOWN} rising minimum time for valid DOWN	DLY_TMR = Open, See Figure 7-11	9, 10, 11		0.42	0.9	
$t_{h\_VTH\_RISE}$	Rising theshold on VSENSEx hold time	DLY_TMR = Open, See Figure 7-12	9, 10, 11		0.84	1.6	µs
$t_{h\_VTH\_FALL}$	Falling theshold on VSENSEx hold time	DLY_TMR = Open, See Figure 7-13	9, 10, 11		0.35	1	µs

(1) See the 5962R2320101VXC SMD (standard microcircuit drawing) for additional information on the RHA devices.
(2) For subgroup definitions, see Quality Conformance Inspection table.
(3) During the power-on, V_{IN} must be at or above V_{IN} (MIN) for at least $t_{Start\_up\_delay}$ for all internal references to be within specification.

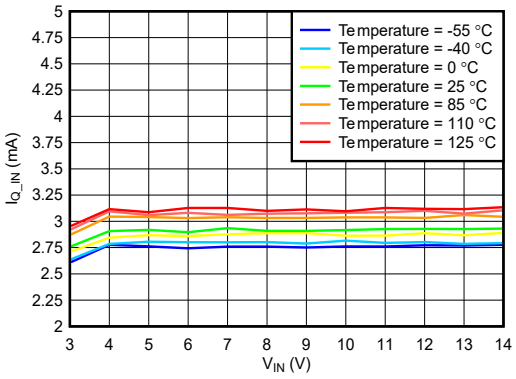
6.7 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

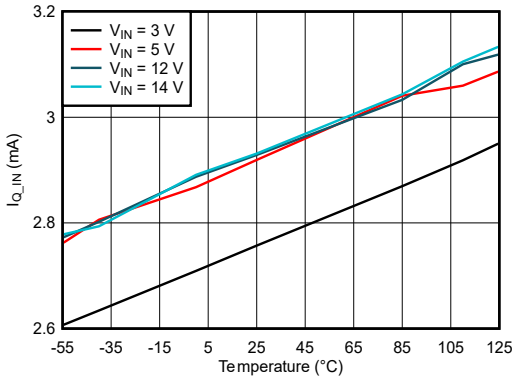
6.8 Typical Characteristics

R_{DLY_TMR} = 10.5kΩ, R_{REG_TMR} = 10.5kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, $V_{\overline{FAULT}}$ = 10kΩ pull-up to VLDO, R_{HYS} = 50kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, unless otherwise noted.



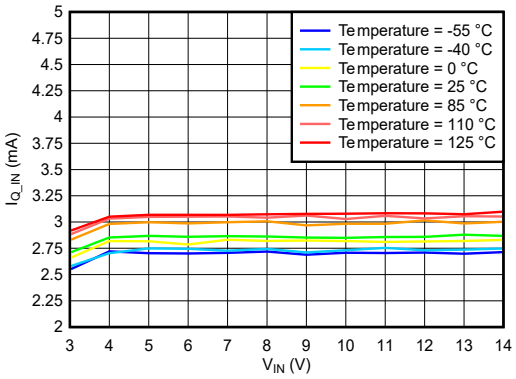
V_{UP} = $V_{\overline{DOWN}}$ = 0V

Figure 6-1. I_{Q_IN} vs V_{IN} Across Temperature in Waiting to Sequence UP State



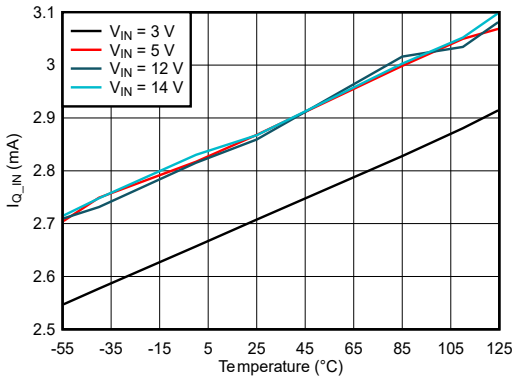
V_{UP} = $V_{\overline{DOWN}}$ = 0V

Figure 6-2. I_{Q_IN} vs Temperature Across V_{IN} in Waiting to Sequence UP State



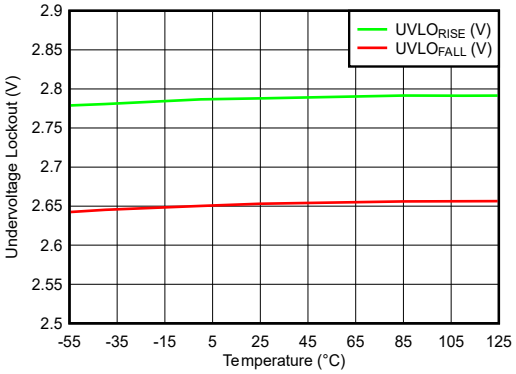
V_{UP} = $V_{\overline{DOWN}}$ = 3.3V

Figure 6-3. I_{Q_IN} vs V_{IN} Across Temperature in Waiting to Sequence DOWN State



V_{UP} = $V_{\overline{DOWN}}$ = 3.3V

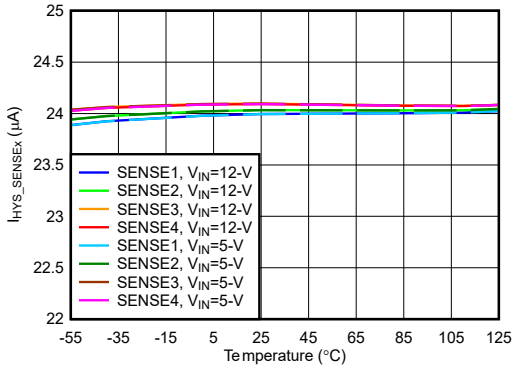
Figure 6-4. I_{Q_IN} vs Temperature Across V_{IN} in Waiting to Sequence DOWN State



R_{DLY_TMR} = Floating
R_{REG_TMR} = 1.18MΩ

V_{UP} = $V_{\overline{DOWN}}$ = 3.3V

Figure 6-5. Undervoltage Lockout vs Temperature



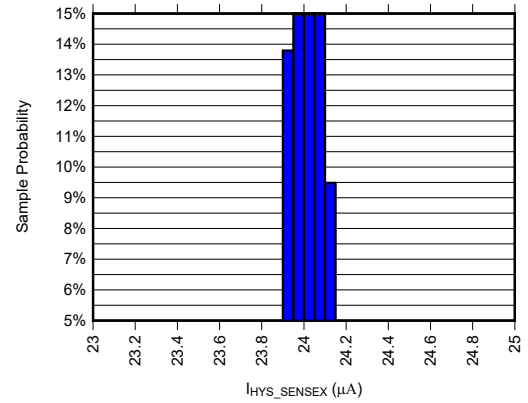
V_{SENSEx} = 700mV

R_{REG_TMR} = Floating

Figure 6-6. I_{HYS_SENSEx} vs Temperature Across V_{IN} and SENSEx Channel

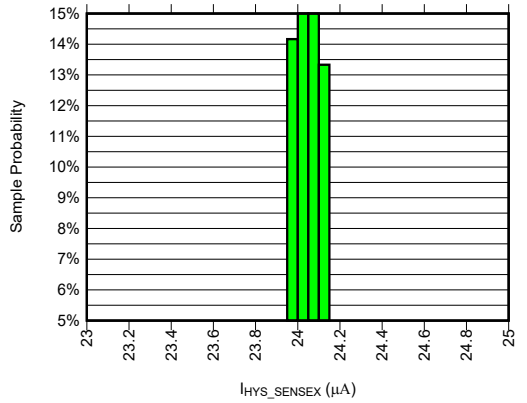
6.8 Typical Characteristics (continued)

R_{DLY_TMR} = 10.5kΩ, R_{REG_TMR} = 10.5kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, $V_{\overline{FAULT}}$ = 10kΩ pull-up to VLDO, R_{HYS} = 50kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, unless otherwise noted.



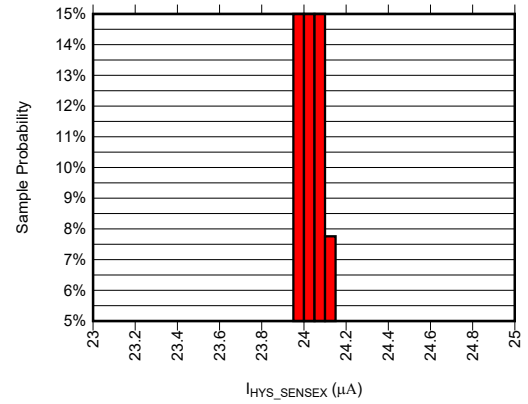
V_{IN} = 3V V_{SENSEx} = 700mV

Figure 6-7. I_{HYS_SENSEx} Current Distribution at Temperature of –55°C



V_{IN} = 3V V_{SENSEx} = 700mV

Figure 6-8. I_{HYS_SENSEx} Current Distribution at Temperature of 25°C



V_{IN} = 3V V_{SENSEx} = 700mV

Figure 6-9. I_{HYS_SENSEx} Current Distribution at Temperature of 125°C

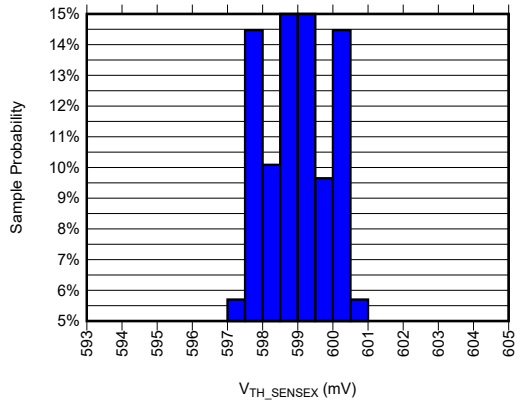


Figure 6-10. V_{TH_SENSEx} Voltage Distribution at Temperature of –55°C

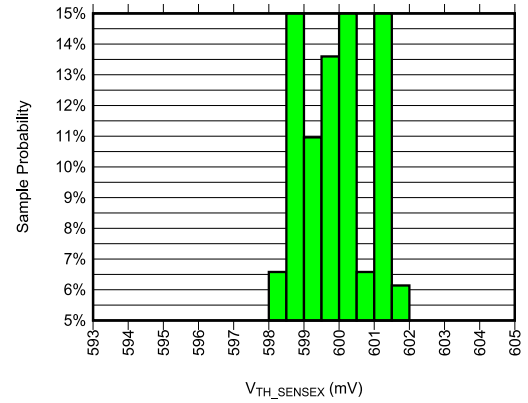


Figure 6-11. V_{TH_SENSEx} Voltage Distribution at Temperature of +25°C

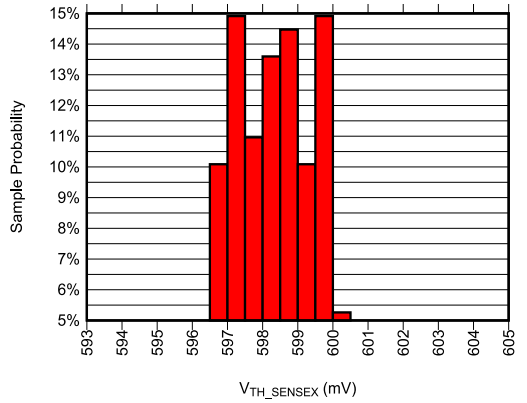
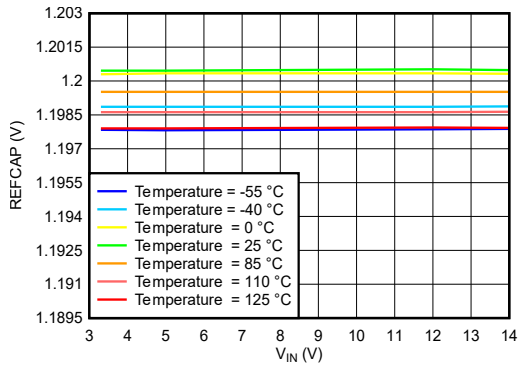


Figure 6-12. V_{TH_SENSEx} Voltage Distribution at Temperature of 125°C

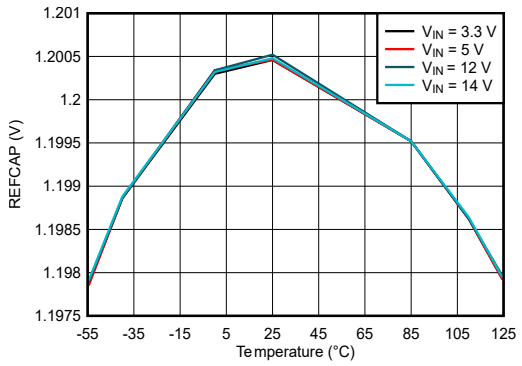
6.8 Typical Characteristics (continued)

R_{DLY_TMR} = 10.5kΩ, R_{REG_TMR} = 10.5kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, $V_{\overline{FAULT}}$ = 10kΩ pull-up to VLDO, R_{HYS} = 50kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, unless otherwise noted.



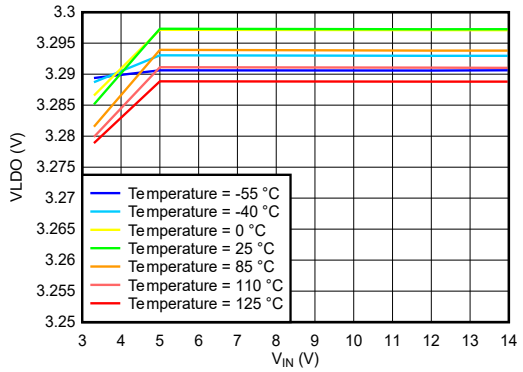
V_{UP} = $V_{\overline{DOWN}}$ = 0V

Figure 6-13. REFCAP vs V_{IN} Across Temperature



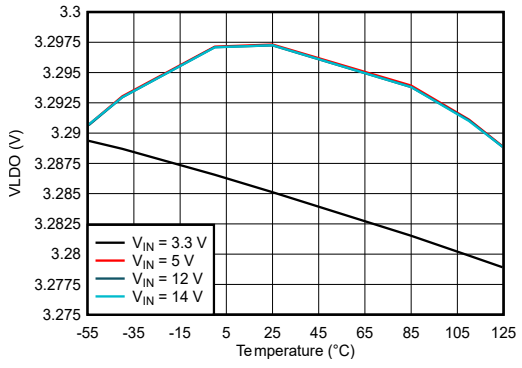
V_{UP} = $V_{\overline{DOWN}}$ = 0V

Figure 6-14. REFCAP vs Temperature Across V_{IN}



V_{UP} = $V_{\overline{DOWN}}$ = 0V

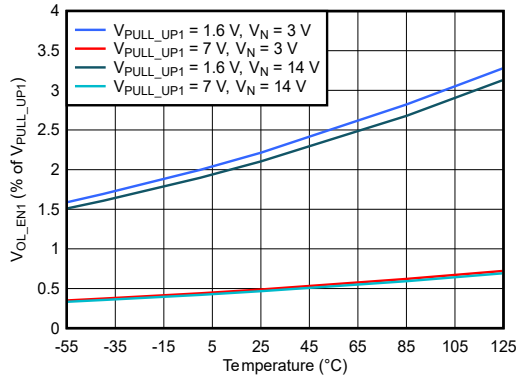
Figure 6-15. VLDO vs V_{IN} Across Temperature



V_{UP} = $V_{\overline{DOWN}}$ = 0V

R_{REG_TMR} = Floating

Figure 6-16. VLDO vs Temperature Across V_{IN}

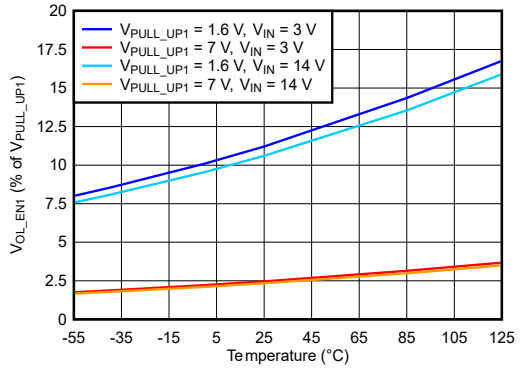


V_{UP} = $V_{\overline{DOWN}}$ = 0V

I_{LOAD} = –2mA

R_{REG_TMR} = Floating

Figure 6-17. V_{OL_EN1} vs Temperature Across V_{PULL_UP1} and V_{IN} at I_{LOAD} = –2mA



V_{UP} = $V_{\overline{DOWN}}$ = 0V

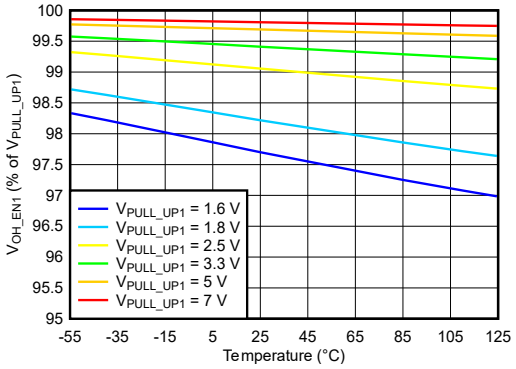
I_{LOAD} = –10mA

R_{REG_TMR} = Floating

Figure 6-18. V_{OL_EN1} vs Temperature Across V_{PULL_UP1} and V_{IN} at I_{LOAD} = –10mA

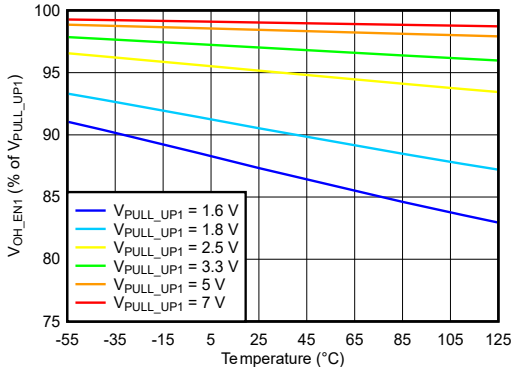
6.8 Typical Characteristics (continued)

R_{DLY_TMR} = 10.5kΩ, R_{REG_TMR} = 10.5kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, $V_{\overline{FAULT}}$ = 10kΩ pull-up to VLDO, R_{HYS} = 50kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, unless otherwise noted.



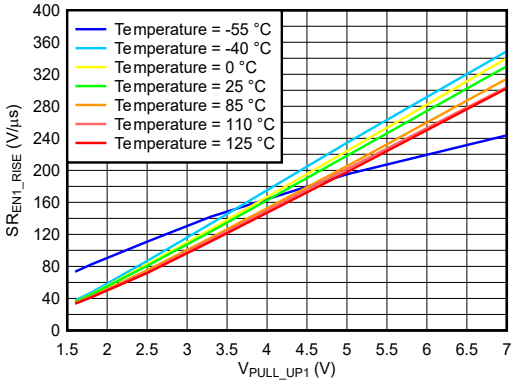
V_{UP} = $V_{\overline{DOWN}}$ = 3.3V
R_{REG_TMR} = Floating
I_{LOAD} = 2mA
V_{IN} = 12V

Figure 6-19. V_{OH_EN1} vs Temperature Across V_{PULL_UP1} at I_{LOAD} = 2mA



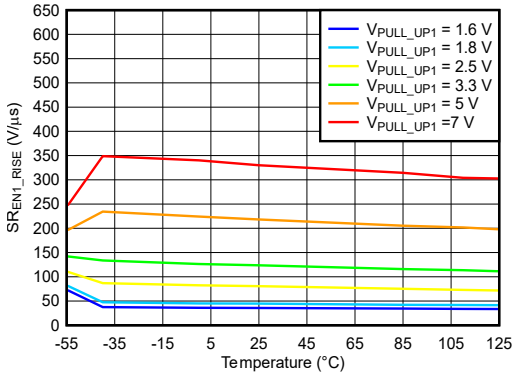
V_{UP} = $V_{\overline{DOWN}}$ = 3.3V
R_{REG_TMR} = Floating
I_{LOAD} = 10mA
V_{IN} = 12V

Figure 6-20. V_{OH_EN1} vs Temperature Across V_{PULL_UP1} at I_{LOAD} = 10mA



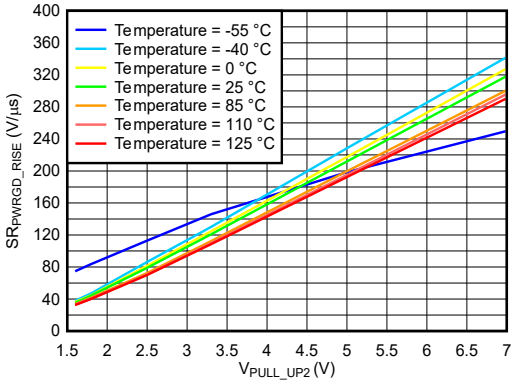
V_{UP} = $V_{\overline{DOWN}}$ = ↑ 3.3V
R_{REG_TMR} = Floating
V_{IN} = 12V

Figure 6-21. SR_{EN1_RISE} vs V_{PULL_UP1} Across Temperature



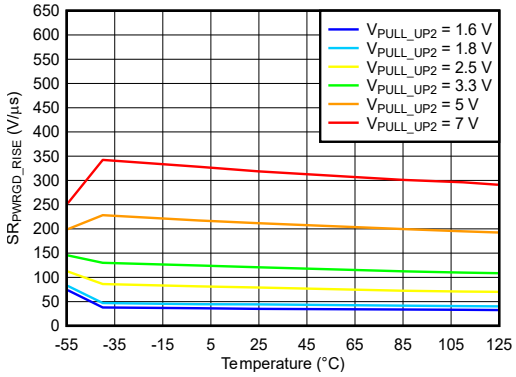
V_{UP} = $V_{\overline{DOWN}}$ = ↑ 3.3V
R_{REG_TMR} = Floating
V_{IN} = 12V

Figure 6-22. SR_{EN1_RISE} vs Temperature Across V_{PULL_UP1}



V_{UP} = $V_{\overline{DOWN}}$ = ↑ 3.3V
R_{REG_TMR} = Floating
V_{IN} = 12V

Figure 6-23. SR_{PWRGD_RISE} vs V_{PULL_UP2} Across Temperature

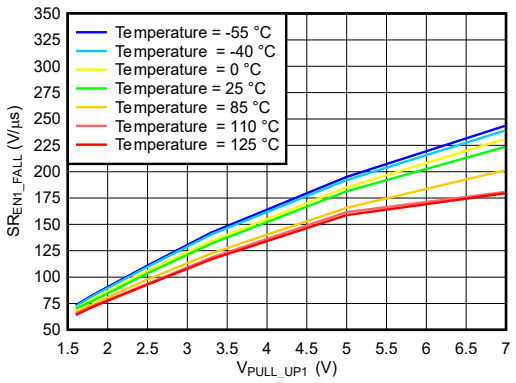


V_{UP} = $V_{\overline{DOWN}}$ = ↑ 3.3V
R_{REG_TMR} = Floating
V_{IN} = 12V

Figure 6-24. SR_{PWRGD_RISE} vs Temperature Across V_{PULL_UP2}

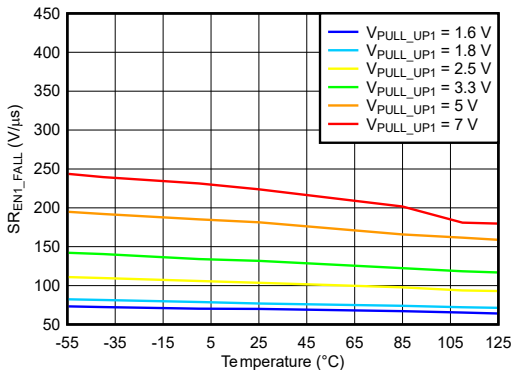
6.8 Typical Characteristics (continued)

R_{DLY_TMR} = 10.5kΩ, R_{REG_TMR} = 10.5kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, $V_{\overline{FAULT}}$ = 10kΩ pull-up to VLDO, R_{HYS} = 50kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, unless otherwise noted.



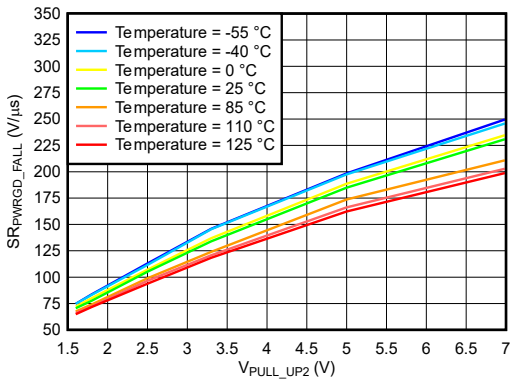
V_{UP} = $V_{\overline{DOWN}}$ = ↓ 0V
R_{REG_TMR} = Floating
V_{IN} = 12V

Figure 6-25. SR_{EN1_FALL} vs V_{PULL_UP1} Across Temperature



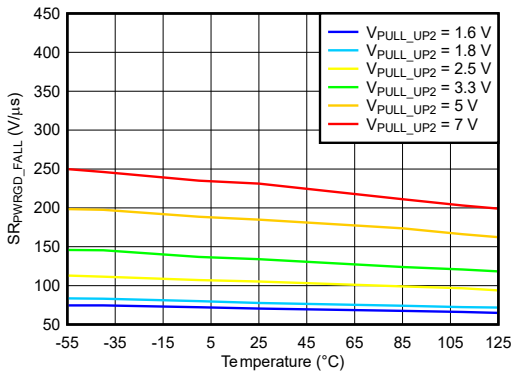
V_{UP} = $V_{\overline{DOWN}}$ = ↓ 0V
R_{REG_TMR} = Floating
V_{IN} = 12V

Figure 6-26. SR_{EN1_FALL} vs Temperature Across V_{PULL_UP1}



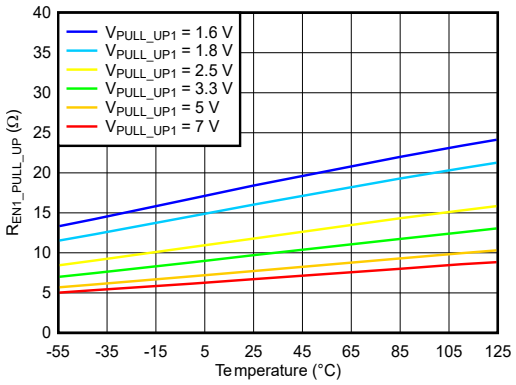
V_{UP} = $V_{\overline{DOWN}}$ = ↓ 0V
R_{REG_TMR} = Floating
V_{IN} = 12V

Figure 6-27. SR_{PWRGD_FALL} vs V_{PULL_UP2} Across Temperature



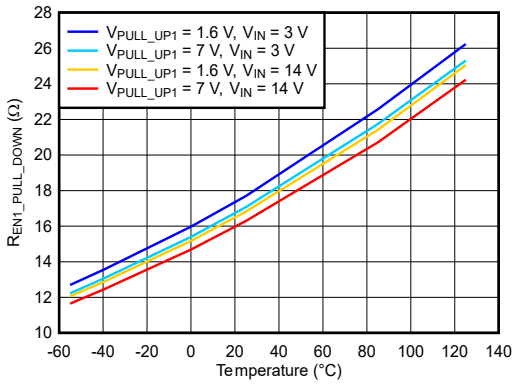
V_{UP} = $V_{\overline{DOWN}}$ = ↓ 0V
R_{REG_TMR} = Floating
V_{IN} = 12V

Figure 6-28. SR_{PWRGD_FALL} vs Temperature Across V_{PULL_UP2}



V_{UP} = $V_{\overline{DOWN}}$ = 3.3V
R_{REG_TMR} = Floating
V_{IN} = 12V
I_{LOAD} = 2mA

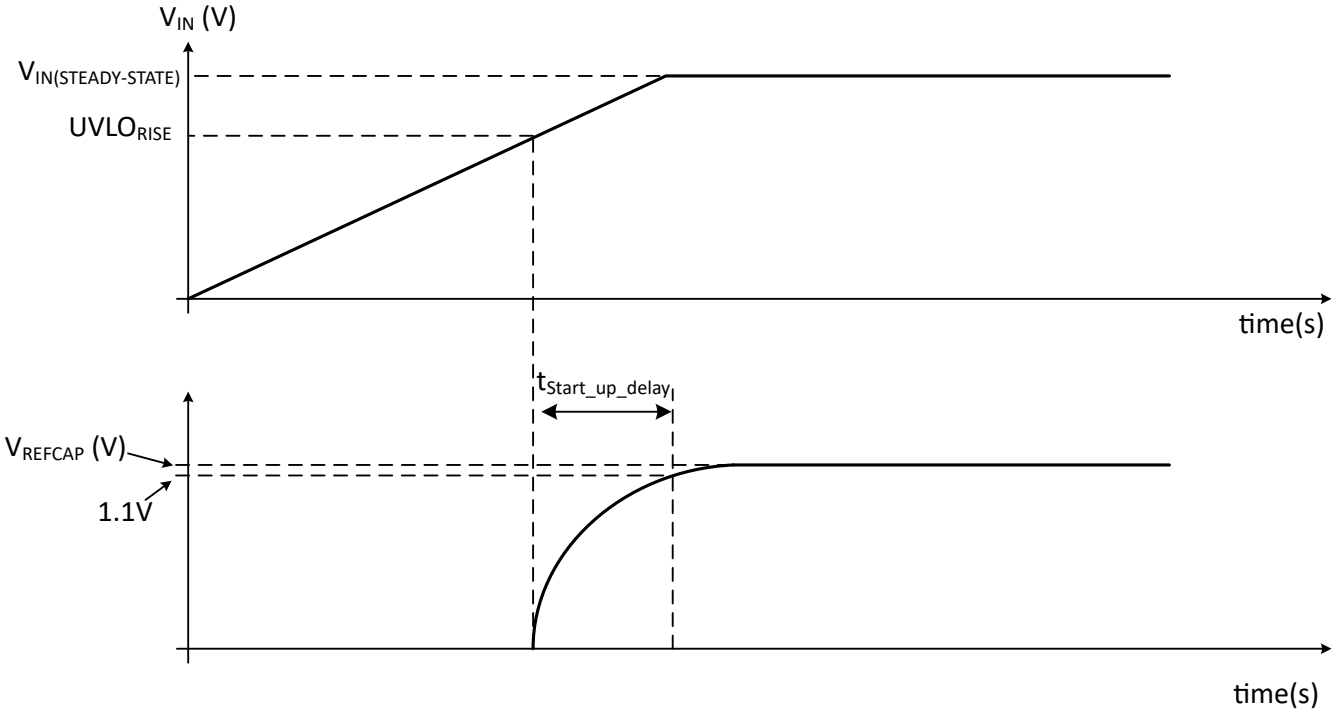
Figure 6-29. $R_{EN1\_PULL\_UP}$ vs Temperature Across V_{PULL_UP1}



V_{UP} = $V_{\overline{DOWN}}$ = 0V
R_{REG_TMR} = Floating
V_{IN} = 12V
I_{LOAD} = –2mA

Figure 6-30. $R_{EN1\_PULL\_DOWN}$ vs Temperature Across V_{PULL_UP1}

7 Parameter Measurement Information



A. $V_{IN(STEADY-STATE)}$ is a valid operating voltage between 3V and 14V

Figure 7-1. $t_{Start\_up\_delay}$ Time Measurement

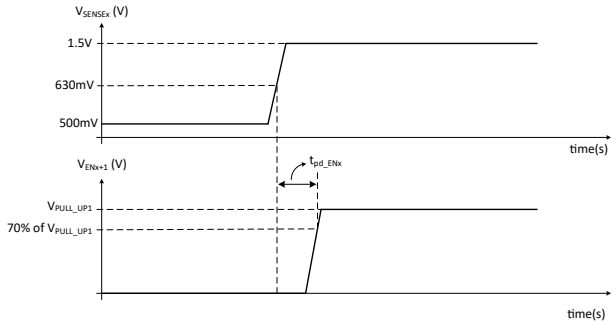


Figure 7-2. ENx Propagation Delay (t_{pd_ENx}) Time Measurement - Rising Voltage

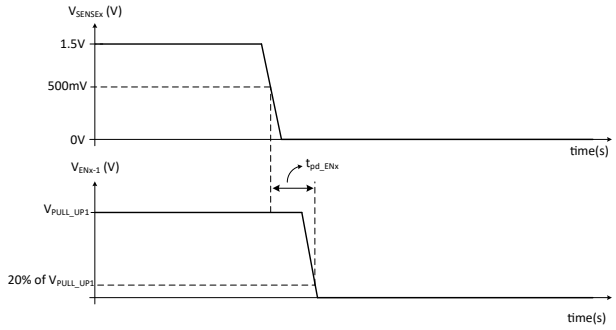


Figure 7-3. ENx Propagation Delay (t_{pd_ENx}) Time Measurement - Falling Voltage

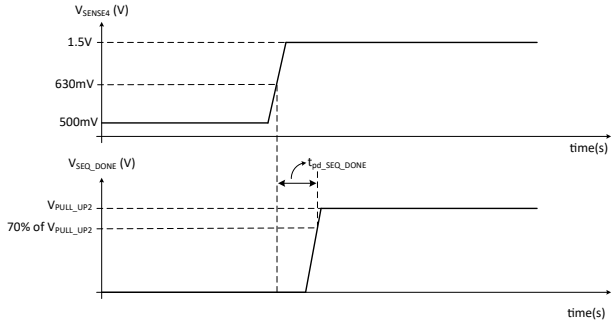


Figure 7-4. SEQ_DONE Propagation Delay ($t_{pd\_SEQ\_DONE}$) Time Measurement - Rising Voltage

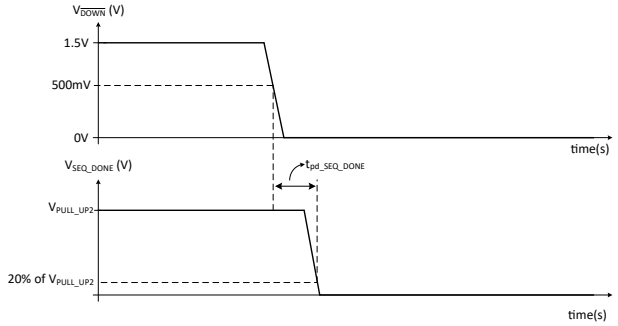


Figure 7-5. SEQ_DONE Propagation Delay ($t_{pd\_SEQ\_DONE}$) Time Measurement - Falling Voltage

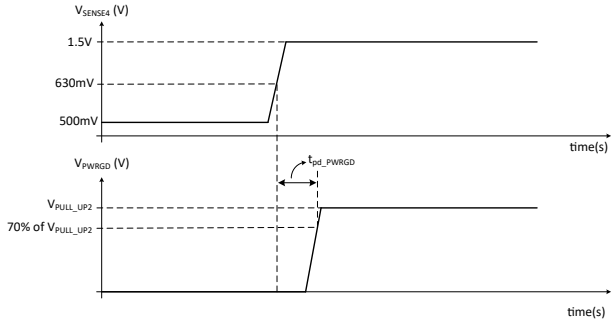


Figure 7-6. PWRGD Propagation Delay (t_{pd_PWRGD}) Time Measurement - Rising Voltage

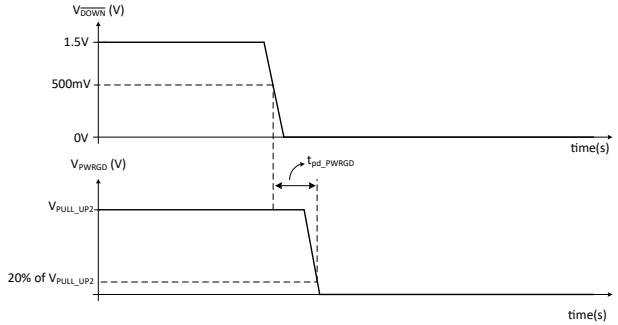
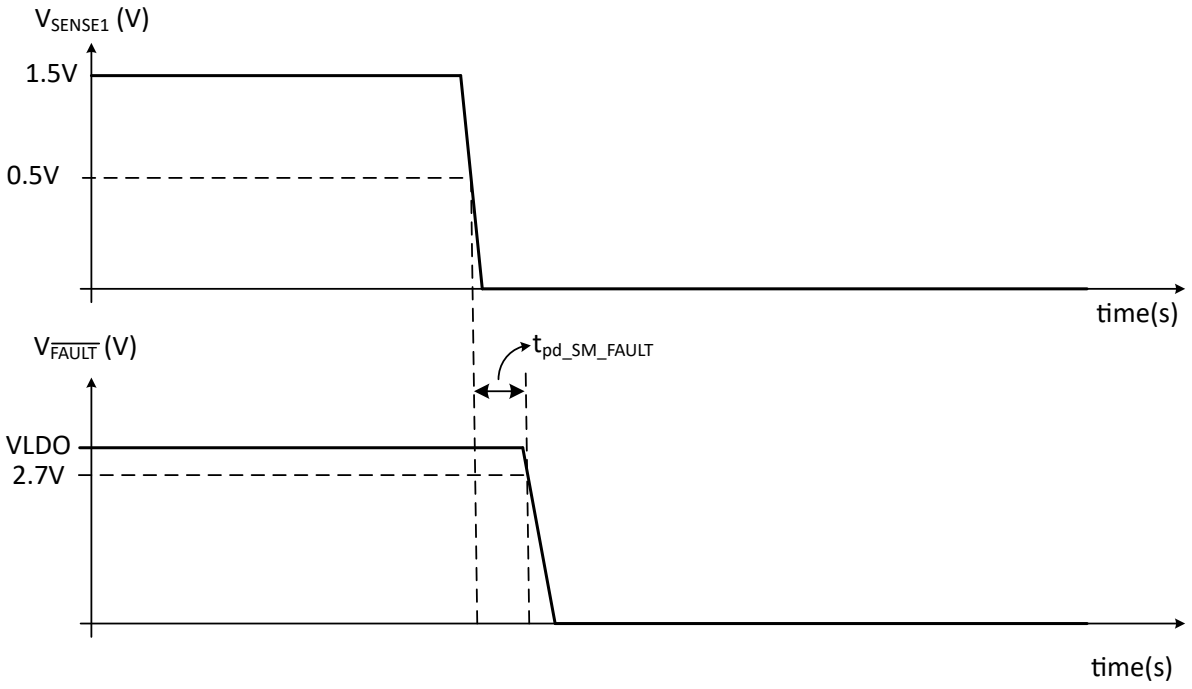


Figure 7-7. PWRGD Propagation Delay (t_{pd_PWRGD}) Time Measurement - Falling Voltage



A. V_{SENSE1} is pulled-low after the state machine is in the waiting to sequence down state.
B. The slew rates are exaggerated for easier visualization.

Figure 7-8. State Machine Detected Fault Propagation Delay ($t_{pd\_SM\_FAULT}$)

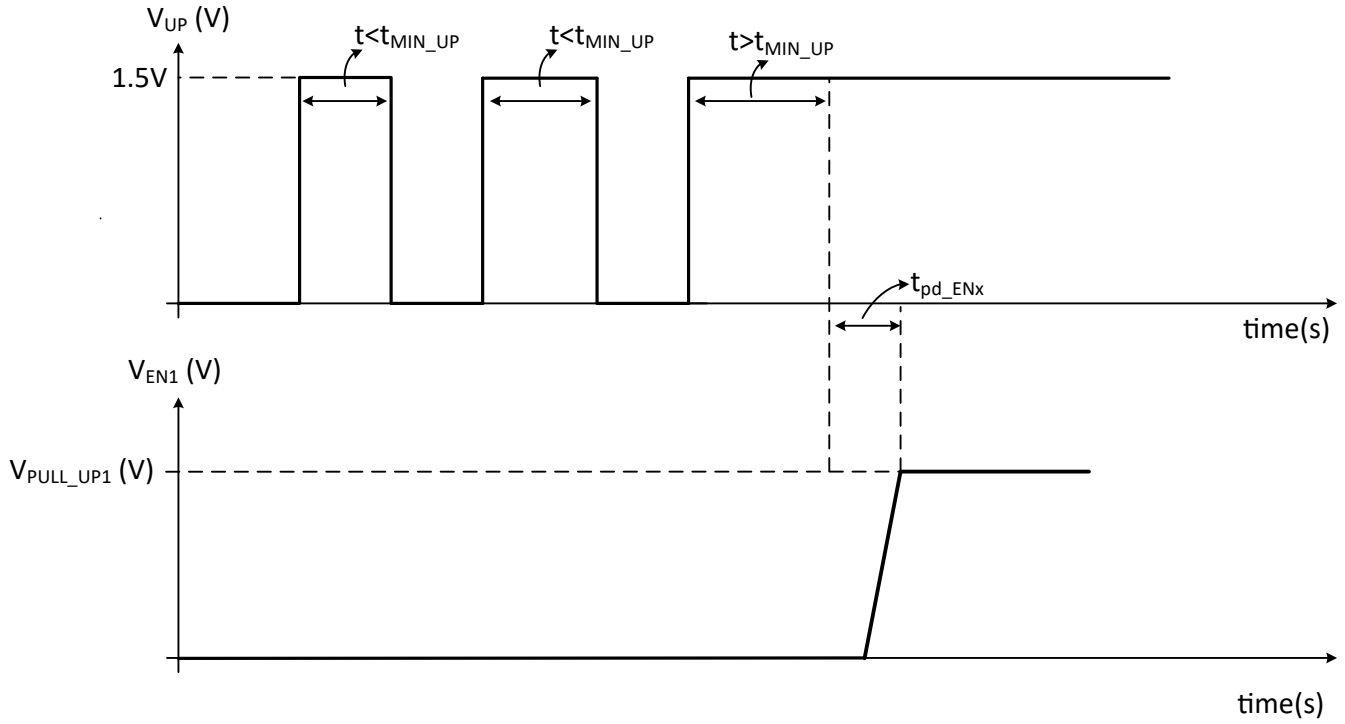


Figure 7-9. Minimum Time for Valid Sequence Up Command (t_{MIN_UP})

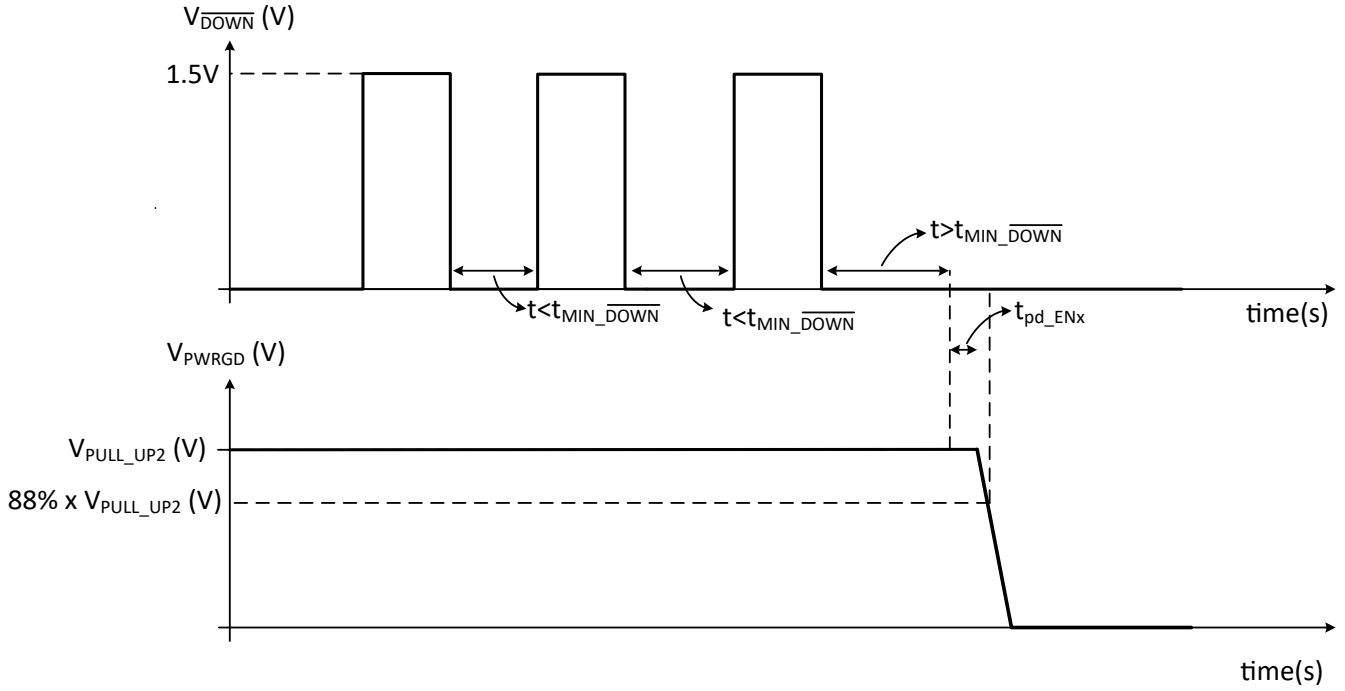


Figure 7-10. Minimum Time for Valid Sequence Down Command ($t_{MIN\_\overline{DOWN}}$)

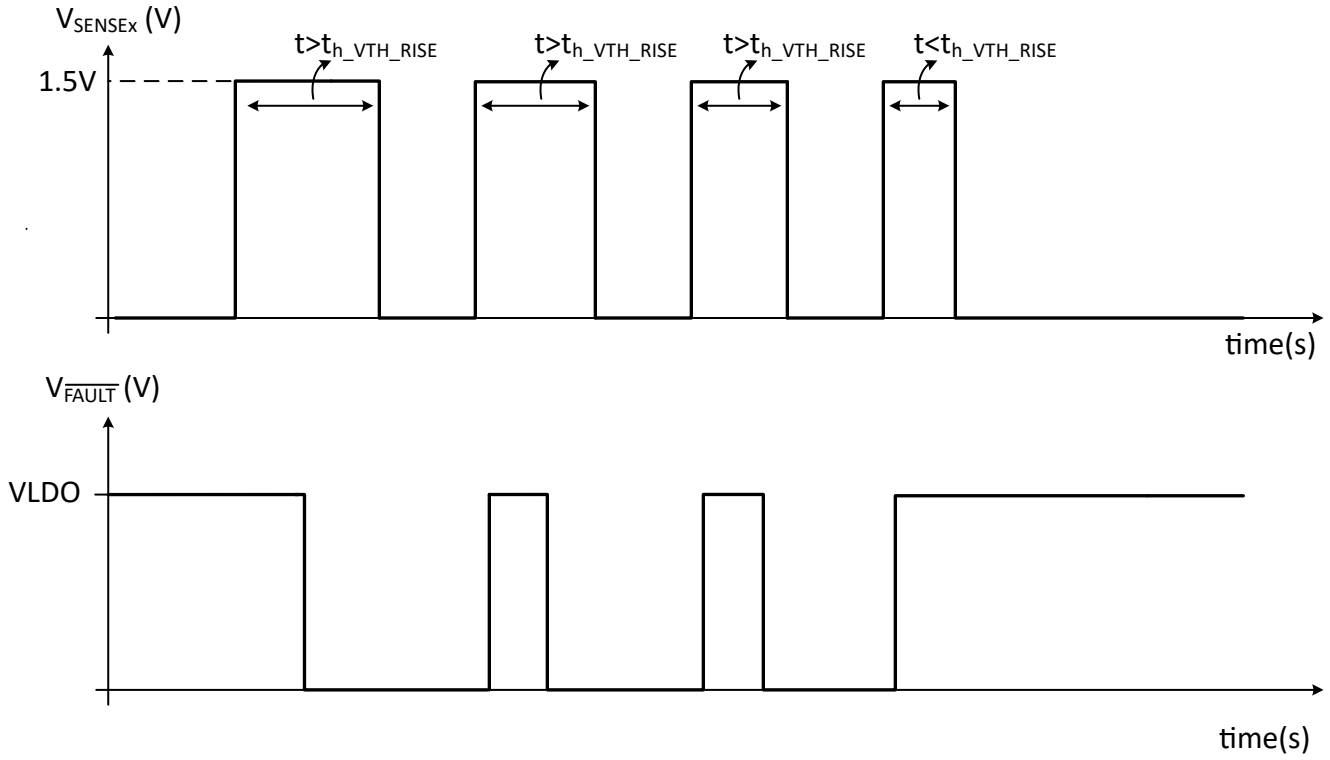


Figure 7-11. Rising Threshold on SENSEx Hold Time ($t_{h\_VTH\_RISE}$)

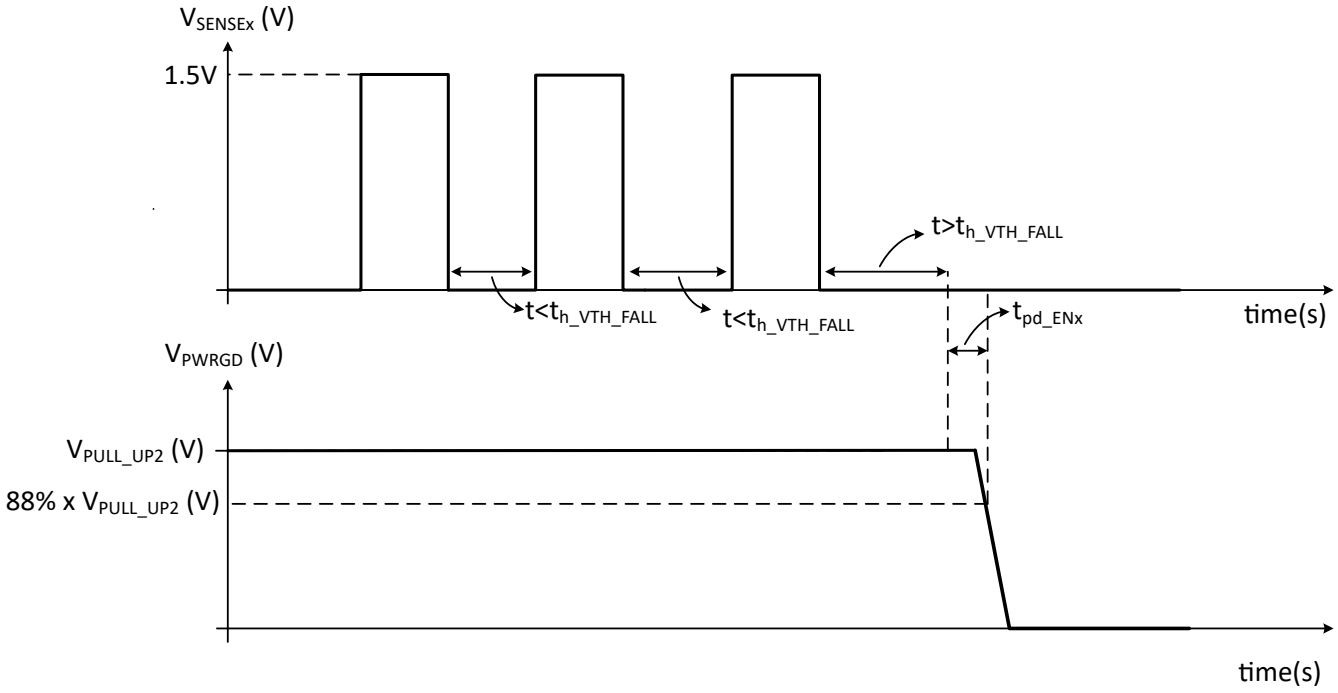


Figure 7-12. Falling Threshold on SENSEx Hold Time ($t_{h\_VTH\_FALL}$)

8 Detailed Description

8.1 Overview

The TPS7H3014 is a four-Channel, 3V to 14V, sequencer and supervisor for space applications. The device is intended to drive devices with enable high logic inputs. The channel count can be incremented as needed for the application by connecting multiple ICs. in a daisy-chain configuration. Each output incorporates a push-pull architecture. The logic high of these outputs are externally provided by the user by supplying a voltage to the PULL-UPx inputs. All ENx push-pull outputs are tied to the PULL_UP1 domain while SEQ_DONE and PWRGD are tied to the PULL_UP2 domain.

The SENSEx inputs are connected to the non-inverting input (undervoltage) of a comparator which is used to determine the on (in regulation) and off (not in regulation) voltage level of the monitored power supply (V_{OUTx}). Each of these inputs feature a threshold level of 599mV (typ) with an accuracy of ±1% across: voltage, temperature, and radiation (TID). The hysteresis voltage threshold level can be adjusted by the user and determined by the R_{TOPx} resistance and the hysteresis current (I_{HYS}). The I_{HYS} becomes active once the rising voltage at SENSEx exceeds the threshold (599mV typ), indicating the monitored voltage rail is in regulation. I_{HYS} is 24µA with an accuracy of ±3% across: voltage, temperature, and radiation (TID).

The device incorporates two timers:

1. **DLY_TMR**: Set the rising and falling ENx delay. Once the $SENSE_{x-1}$ is above the on voltage during a sequence up, the EN_x will be asserted high once the delay set by the user using the DLY_TMR input is expired. The same is true during sequence down, this means that once $SENSE_x$ is below the off voltage the EN_{x-1} will be asserted low once the timer is expired. This timer can be set from 0.25ms to 25ms, by using a 10.5kΩ to a 1.18MΩ, respectively.
2. **REG_TMR**: Set the allowed time that a sensed voltage rail has to be above the on threshold (in regulation). Once the EN_x is asserted high, the $SENSE_x$ has up to the time set by the user, using REG_TMR, to be above 599mV (typ). Otherwise a reverse sequence down from EN_{x-1} is started.

Separate UP and $\overline{\text{DOWN}}$ pins are provided by the device in order to enable daisy-chain configurations. The UP pin has a threshold (V_{TH_UP}) of 599mV (typ), while the $\overline{\text{DOWN}}$ pin has an threshold ($V_{TH\_\overline{DOWN}}$) of 498mV. A fixed hysteresis of 100mV is incorporated in both input comparators for noise stability. These pins are edge sensitive, a rising edge in UP starts the sequence up, while a falling edge in $\overline{\text{DOWN}}$ will start the sequence down.

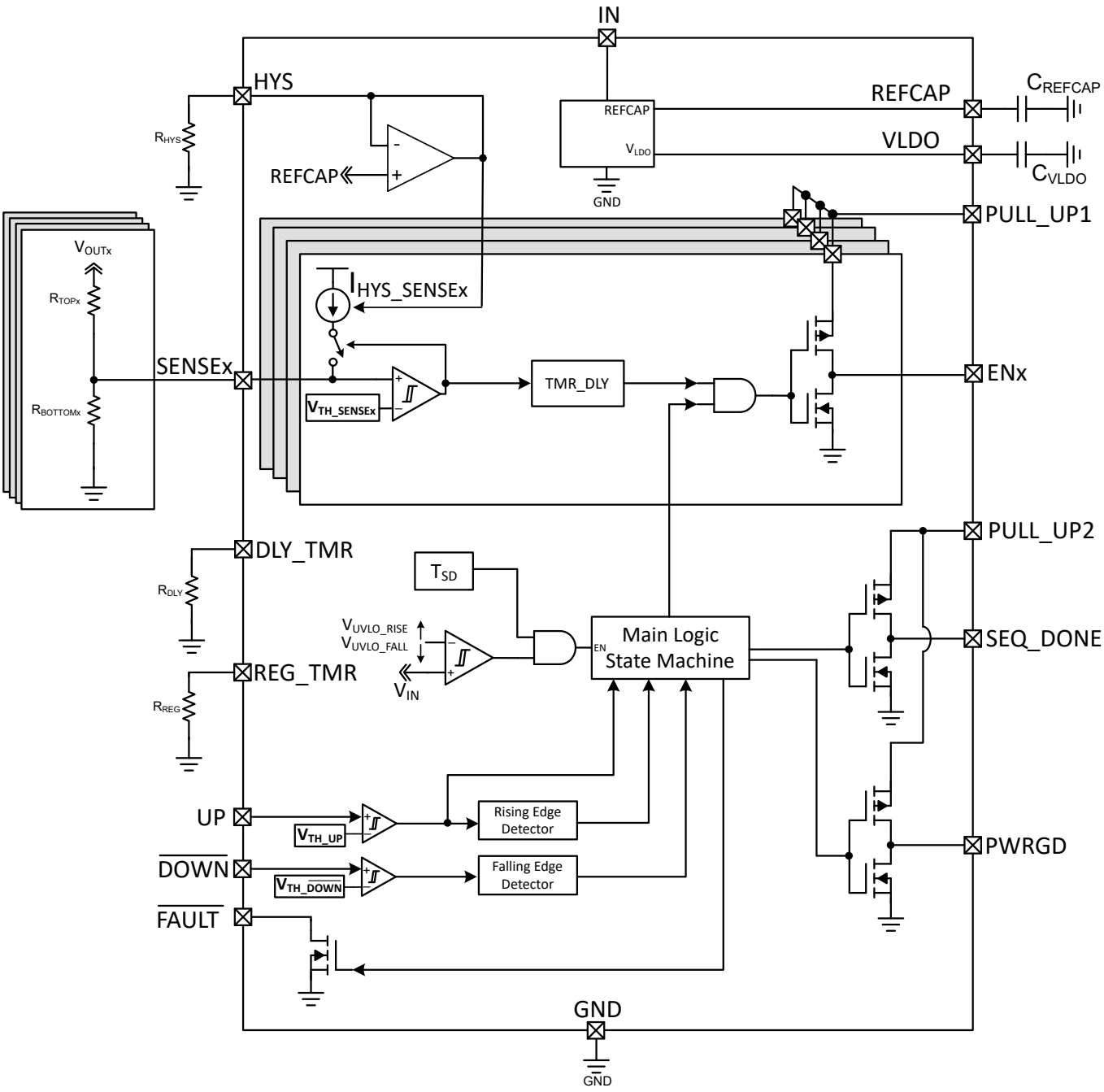
When using a single device and driven externally, both pins (UP and DOWN) are typically tied together. Since UP and $\overline{\text{DOWN}}$ inputs have an accurate threshold, they can be used to initiate the sequence up and down by accurately sensing another rail (using a resistive divider), or they can be externally driven by a controller. Once UP is driven above V_{TH_UP}, the device will start a sequence up by asserting EN1 high after the programmed delay time (DLY_TMR), at which point the SENSE1 will start rising up. If SENSE1 crosses the on voltage before the REG_TMR is expired, then EN2 will be asserted high after the programmed delay. This process continues until the SEQ_DONE and PWRGD are asserted high indicating a complete sequence up and system power good, respectively.

Once the $\overline{\text{DOWN}}$ pin is driven below $V_{TH\_\overline{DOWN}}$, the device will start a sequence down by forcing EN4 low after the programmed delay. At this point, the SENSE4 voltage will start falling until is lower than the set off voltage. Once this happens, EN3 will be asserted low after the programmed delay. This will continue until EN1 is forced low. As the discharge time of the sequenced devices is unknown, the REG_TMR is not active during power down.

During sequence up, SEQ_DONE and PWRGD are asserted high after the last used channel crosses the on voltage threshold and the programmed DLY_TMR is expired (assuming it is active). During sequence down, SEQ_DONE is forced low once V_{OUT1} is below the off voltage and the DLY_TMR is expired. However PWRGD is forced low immediately after the commanded sequence down.

The TPS7H3014 also incorporates a comprehensive FAULT management system described in the State Machine section.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage (IN), VLDO and REFCAP

During steady state operation, the input voltage of the TPS7H3014 must be between 3V and 14V. A minimum bypass capacitance of at least 0.1µF is needed between V_{IN} and GND. The input bypass capacitors should be placed as close to the sequencer IC as possible. Is recommended that V_{IN} slew rate is controlled between 10V/µs to 1mV/µs for proper IC operation.

The voltage applied at V_{IN} serves as the input for the internal regulator that generates the VLDO voltage, typically 3.29V. At input voltages less the 3.29V (typ), the VLDO voltage will follow the voltage at V_{IN}. Recommended capacitance for VLDO is 1µF. Unused SENSE2 to SENSE4 can be tied to VLDO to by-pass the channel delay during sequence up and down. It is recommended to pull-up the $\overline{FAULT}$ pin to VLDO via a 10kΩ resistor, but otherwise it is recommended not to externally load this pin due to limited output current capability. During power up, the user should wait at least the 2.8ms ($t_{Start\_up\_delay}$) after V_{IN} > $UVLO_{RISE}$ before attempting to start a sequence up, this is due to internal time constants in the device.

Each device generates an internal 1.2V bandgap reference that is utilized throughout the various internal control logic blocks. This is the voltage present on the REFCAP pin during steady state operation. This voltage is divided down to produce the reference for the comparator inputs $SENSE_x$ (599mV typ), UP (598mV typ) and $\overline{DOWN}$ (498mV typ). The V_{TH_SENSEx} reference is measured at the EN_x outputs to account for offsets in the error amplifier and maintains regulation within ±1% across: voltage, temperature, and radiation TID (up to 100krad in Silicon). This tight reference tolerance allows the user to monitor voltage rails with high accuracy. A 470nF capacitor to GND is required at the REFCAP pin for proper electrical operation as well as to ensure robust SET performance of the device.

8.3.1.1 Undervoltage Lockout (V_{POR_IN} < V_{IN} < UVLO)

When the voltage on V_{IN} is less than the UVLO (2.79V typ) voltage, but greater than the power-on reset voltage (V_{POR_IN}, 1.41V typ), the output pins (ENx, SEQ_DONE and PWRGD) will be in a logic low state, regardless of the voltage at the inputs of the device, named as:

- $SENSE_x$
- UP
- $\overline{DOWN}$

8.3.1.2 Power-On Reset (V_{IN} < V_{POR_IN})

When the voltage on V_{IN} is lower than the power on reset voltage (V_{POR_IN}), the output signal is undefined and is not to be relied upon for proper device function.

Figure 8-1 shows the ENx outputs relationship to a rising input voltage (V_{IN}). As can be observed, the ENx are undefined when V_{IN} is lower than V_{POR_IN} (typically 1.41V). During this time the outputs can be any value from 0V to V_{IN}. In this case, the input voltages to all undervoltage (UV) input comparators (SENSEx) are below the V_{TH_SENSEx} (599mV). For this reason (in conjunction with waiting for a rising edge on UP), the ENx, SEQ_DONE and $\overline{PWRGD}$ stays low after V_{IN} rises above $UVLO_{RISE}$ (typically 2.79V).

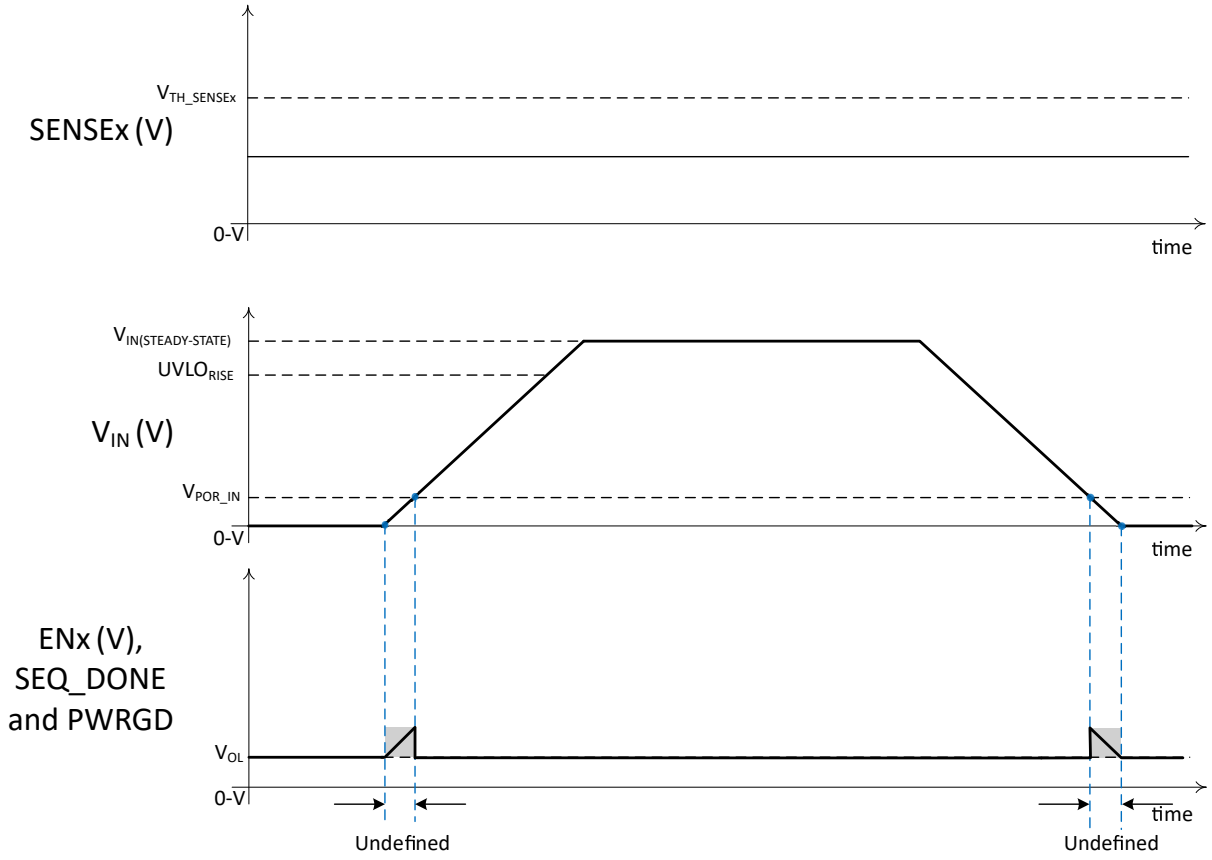


Figure 8-1. Outputs in a Valid Low State After V_{IN} > V_{IN-MIN}

A. This figures assumes:

1. A valid external pull-up voltage is connected to the PULL_UPx inputs (1.6V ≤ V_{PULL_UPx} ≤ 7V).
2. $V_{IN(STEADY-SATE)}$ is a valid V_{IN} voltage between 3V to 14V.
3. $V_{\overline{FAULT}}$ pull up to VLDO.
4. Device is in the: Waiting to Sequence UP State (Refer to State Machine for more details).
5. V_{OL} represents: V_{OL_ENx}, $V_{OL\_SEQ\_DONE}$, and V_{OL_PWRGD}, or the low logic output voltage for all outputs.

8.3.2 SENSEx Inputs

8.3.2.1 V_{TH_SENSEX} and V_{ONx}

The TPS7H3014 sequencer integrates four under-voltage (UV) comparators, with an accurate (±1%) threshold voltage (V_{TH_SENSEx}) of 599mV nominal. V_{TH_SENSEx} is measured at the ENx outputs to account for comparator offsets in the threshold. Maximum flexibility is provided as external resistive dividers can be adjusted to sense any voltage rail (V_{OUTx}). Figure 8-2 shows a conceptual diagram of the comparators connected to the SENSEx inputs. As can be observed, the sensed voltage rail (V_{OUTx}) is attenuated (using an external resistive divider, R_{TOPx} and $R_{BOTTOMx}$) and compared against the V_{TH_SENSEx} voltage. Is recommended to maintain the steady-state SENSEx voltage below 1.6V, in order to maintain the threshold (V_{TH_SENSEx}) accuracy.

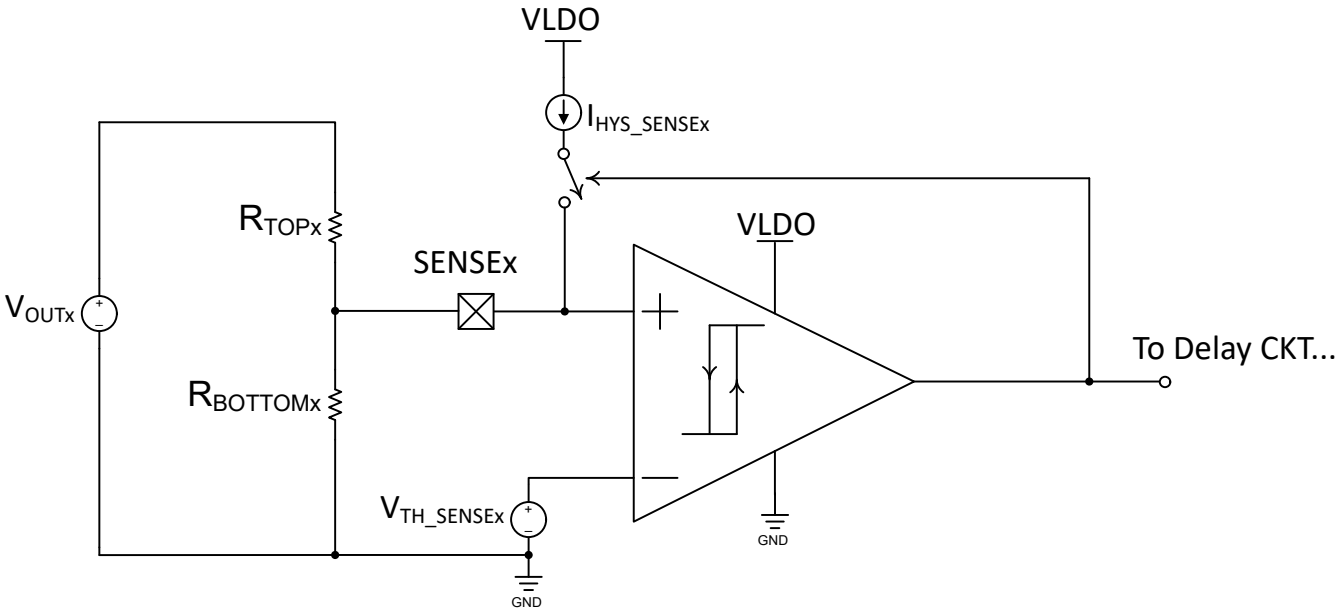


Figure 8-2. SENSEx Comparators Inputs

When the voltage at the monitored rail (V_{OUTx}) is rising, the hysteresis current (I_{HYS}) is not connected to SENSEx input. At this time the SENSEx (attenuated V_{OUTx}) voltage is compared against the SENSEx threshold (V_{TH_SENSEx}). When $V_{SENSEx} > V_{TH\_SENSEx}$ the voltage is considered within regulation limits. We can calculate the on (within regulation) voltage by doing a simple voltage divider as:

$$V_{ONx\_NOMINAL}\ (V) = \left(1 + \frac{R_{TOPx}}{R_{BOTTOMx}}\right) \times V_{TH\_SENSEx} \quad (1)$$

Where:

- V_{TH_SENSEx} is the nominal sense threshold voltage of 599mV.

As with any system, there is some variation (or errors) of the design variables, in this case the top and bottom resistors and the SENSEx threshold voltage. Using the derivative method to calculate the total error (and assuming these variables are uncorrelated) with both resistors having the same tolerance value, the V_{ONx} error can be calculated as:

$$V_{ONx\_ERROR}\ (V) = \pm\sqrt{\frac{V_{TH\_SENSEx}^2 \times \left[\left(2 \times R_{TOL}^2 \times R_{TOPx}^2\right) + \left(V_{TH\_SENSEx\_ACC}^2 \times \left(R_{TOPx} + R_{BOTTOMx}\right)^2\right)\right]}{R_{BOTTOMx}^2}} \quad (2)$$

Where:

- R_{TOL} is the resistors tolerance (same for top and bottom resistors) as numeric value. For example, for 0.1% tolerance resistors, we use 0.001.
- $V_{TH\_SENSEx\_ACC}$ is the SENSEx threshold accuracy as numeric value (in this case 0.01).
- R_{TOPx} and $R_{BOTTOMx}$ are in Ohms (Ω).
- V_{TH_SENSEx} is 0.599 Volts.

Using Equation 1 and Equation 2 we can calculate the on voltage range as:

$$V_{ONx} = V_{ONx\_NOMINAL} \pm V_{ONx\_ERROR} \quad (3)$$

Note

Remember V_{TH_SENSEx} is the reference voltage when accounting for the comparator offsets $V_{TH\_SENSEx} = V_{REF} + V_{OFFSETx}$.

As this device is intended for sequencing of multirail systems, the ENx to SENSEx order is defined in ascending channel number (EN1 to EN4) for sequence up, and descending (EN4 to EN1) for sequence down. When a channel of the sequencer is not needed (unused) the channel can be connected to VLDO to skip the channel during sequence up/down. Is recommended to connect all disabled channels to VLDO, but an external voltage greater than 91% of VLDO (max) will disabled the channel (the voltage at SENSEx cannot exceed 3.5V). Only channels 2 through 4 can be disabled. It is recommended to disabled channels starting from high (channel #4) to low (channel #2). The channels are disabled starting from the lowest channel count and higher. This means that if channel #2 is disabled, by definition channels #3 and #4 will also be disabled. It is mandatory to connect all disabled channels to VLDO (or a voltage greater than 91% of VLDO).

Note

The channels to be disabled must be valid at power up and not be dynamically changed during the sequence up and down.

Any voltage at SENSE 2 to SENSE4 > V_{TURN_OFF} [91% of VLDO(max)] will disable (or turn-off) the channel. This will disable the delay (set by TMR_DLY) for those channels during sequence up and down.

Although it is not required, in noisy applications it is good analog design practice to place a small bypass capacitor at the SENSEx inputs in order to reduce sensitivity to transient voltages on the monitored signal.

8.3.2.2 I_{HYS_SENSEx} and V_{OFFx}

The TPS7H3014 has a built-in hysteresis current of 24µA with an accuracy of ±3% (with R_{HYS} = 50kΩ). The hysteresis current is equivalent to REFCAP/R_{HYS}. A tolerance of 0.1% for the R_{HYS} is recommended as it ultimately affects the hysteresis current accuracy.

Note

A resistor of R_{HYS}=49.9kΩ can be used instead of 50kΩ. In this case the nominal I_{HYS_SENSEx} current will be 24.05µA instead of 24µA.

This current is mirrored internally across all SENSEx inputs. This hysteresis current becomes active when the SENSEx voltage is greater than the threshold voltage (599mV ±1%), same as V_{OUTx} > V_{ONx} (Refer to Equation 3 and Figure 8-2). This current (I_{HYS}) multiplied by the R_{TOPx} resistance induces a voltage (V_{HYSx}) that is added to the SENSEx node, effectively boosting (incrementing) the node voltage. During sequence down, or an undervoltage event when the V_{OUTx} is decrementing, it will need to drop below the V_{OFF} voltage in order to be considered as an out of regulation (or fault). The hysteresis voltage is defined as:

$$V_{HYSx\_NOMINAL}\ (V) = I_{HYS\_SENSEx} \times R_{TOPx} \quad (4)$$

Where:

- I_{HYS_SENSEx} = 24 × 10^{-6} Amps (or 24µA)

- R_{TOPx} units are in Ohms (Ω)

The "off" voltage (or out of regulation) voltage can be calculated as:

$$V_{OFFx\_NOMINAL}\ (V) = V_{ONx\_NOMINAL} - V_{HYSx\_NOMINAL} \quad (5)$$

Using Equation 1 and Equation 5

$$V_{OFFx\_NOMINAL}\left(V\right) = \left[\left(1 + \frac{R_{TOPx}}{R_{BOTTOMx}}\right) \times V_{TH\_SENSEx}\right] - \left(I_{HYS\_SENSEx} \times R_{TOPx}\right) \quad (6)$$

Where:

- V_{TH_SENSEx} is the nominal sense threshold voltage of 0.599V
- I_{HYS_SENSEx} = 24 × 10^{-6} Amps (or 24µA)
- R_{TOPx} and $R_{BOTTOMx}$ units are in Ohms (Ω)

The V_{OFF} error (using the derivative method and assuming all variables are uncorrelated) can be calculated as:

$$V_{OFFx\_ERROR}\left(V\right) = \pm\sqrt{\frac{A + B + C + D}{R_{BOTTOMx}^{2}}} \quad (7)$$

Where the equation terms are:

$$A = I_{HYS\_SENSEx}^{2} \times I_{HYS\_SENSEx\_ACC}^{2} \times R_{TOPx}^{2} \times R_{BOTTOMx}^{2} \quad (8)$$

$$B = R_{TOL}^{2} \times R_{TOPx}^{2} \times V_{TH\_SENSEx}^{2} \quad (9)$$

$$C = R_{TOL}^{2} \times R_{TOPx}^{2} \times \left[\left(I_{HYS\_SENSEx} \times R_{BOTTOMx}\right) - V_{TH\_SENSEx}\right]^{2} \quad (10)$$

$$D = V_{TH\_SENSEx}^{2} \times V_{TH\_SENSEx\_ACC}^{2} \times \left(R_{TOPx} + R_{BOTTOMx}\right)^{2} \quad (11)$$

Where:

- R_{TOL} is the resistors tolerance (same for top and bottom resistors) as numeric value. For example, for 0.1% tolerance resistors, we use 0.001.
- $V_{TH\_SENSEx\_ACC}$ is the SENSEx threshold accuracy as numeric value (in this case 0.01).
- $I_{HYS\_SENSEx\_ACC}$ is the hysteresis current accuracy as numeric value (in this case 0.03)
- V_{TH_SENSEx} is the nominal sense threshold voltage of 0.599V
- I_{HYS_SENSEx} = 24 × 10^{-6} Amps (or 24µA)
- R_{TOPx} and $R_{BOTTOMx}$ units are in Ohms (Ω)

$$V_{OFFx} = V_{OFFx\_NOMINAL} \pm V_{OFFx\_ERROR} \quad (12)$$

Using Equation 6 and Equation 7 we can calculate the off voltage range as:

Figure 8-3, shows a conceptual diagram of the rising and falling voltage, it also shows the errors on this voltage due to V_{TH} accuracy, I_{HYS} accuracy, and the resistive divider tolerances. At the system level, these errors have to be taken into account for a robust design.

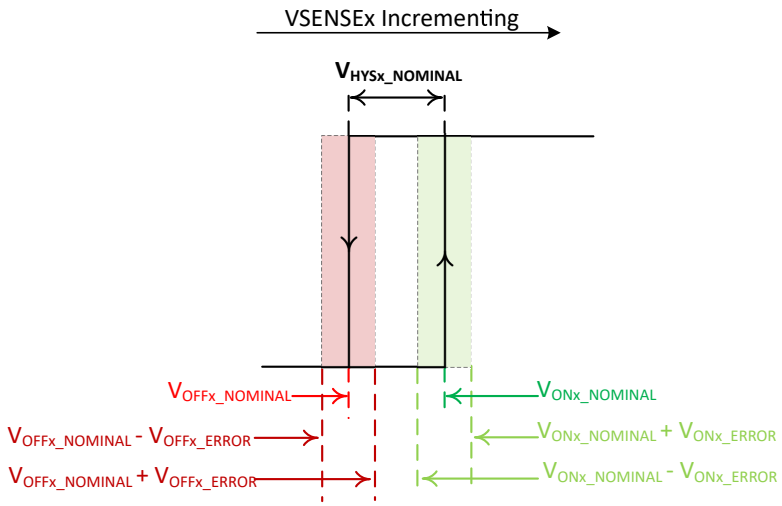


Figure 8-3. Rising and Falling Thresholds Voltages for the SENSE$_x$ Comparators

8.3.2.3 Top and Bottom Resistive Divider Design Equations

At the system level the designer knows (or selects) the V_{ONx} and V_{OFFx} levels. Usually these voltages are selected as percentages of the nominal rail voltage (V_{OUTx}) being monitored. Knowing this information, we can calculate the resistive divider components values (R_{TOPx} and $R_{BOTTOMx}$) for the desired target levels. Using Equation 4 and Equation 5 we can calculate the top resistor as:

$$R_{TOPx} = \frac{V_{ONx} - V_{OFFx}}{I_{HYS\_SENSEx}} \quad (13)$$

From Equation 1 we can calculate the bottom resistor as:

$$R_{BOTTOMx} = \frac{R_{TOPx} \times V_{TH\_SENSEx}}{V_{ONx} - V_{TH\_SENSEx}} \quad (14)$$

It's important to notice that the larger the separation between V_{ONx} and V_{OFFx} (referred as V_{HYSx}), the bigger the error in the off voltage. Figure 8-4 shows a plot of the error in the V_{OFFx} for different hysteresis voltages (V_{HYSx} = V_{ONx} – V_{OFFx}). The plot is created for three different V_{ON} voltages (or percentages of the nominal output voltage: 90, 95, and 97%) and two different output voltages (0.8V and 28V). As can be observed, the output voltage has very little impact on the off voltage error (differences cannot be appreciated on the plot). The error (in percent) can go from approximately 1% (at V_{HYS} = 3%) to around 2.6% (at V_{HYS} = 80%).

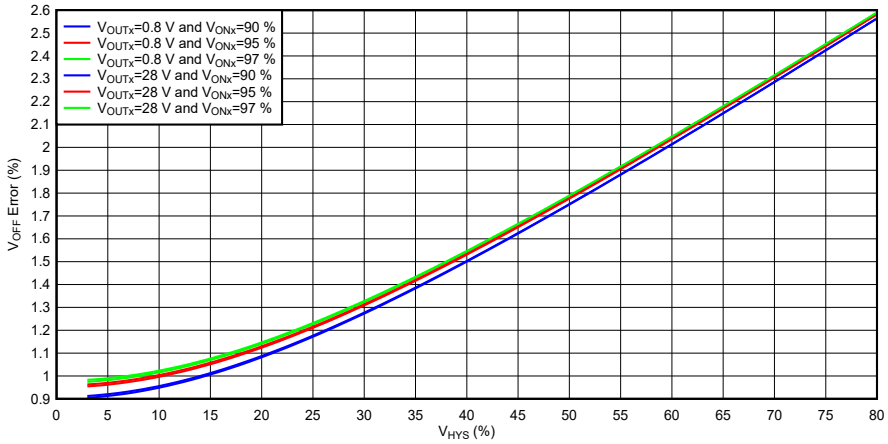


Figure 8-4. V_{OFFx} Error vs V_{HYS}

A. This plot does not includes the error on the V_{OFFx} due to the difference between the calculated top and bottom resistors using Equation 13 and Equation 14 and the actual resistance values that a designer can procure.
B. The resistor tolerance used for the calculation is 0.1%, V_{TH_SENSEx} accuracy is 1%, and the I_{HYS_SENSEx} accuracy is 3%.
C. In this plot the V_{HYS} (%) represents the separation as percentages of the nominal output voltage (V_{OUTx}).
D. In this plot, the V_{OFF} error in % is normalized with respect to the full-scale voltage (or V_{OUTx}).

8.3.3 Output Stages (ENx,SEQ_DONE,PWRGD,PULL_UP1 and PULL_UP2)

The output stage's (EN1 to EN4), SEQ_DONE and PWRGD are of push-pull, active high type. The pull-up voltage for the push-pull outputs is externally provided by the user. PULL_UP1 (input) is the pull-up voltage domain for all ENx outputs (EN1 to EN4), while PULL_UP2 (input) is the pull-up voltage domain for the SEQ_DONE and PWRGD outputs.

Note

There are no sequencing requirements for IN, PULL_UP1, and PULL_UP2; however, all must be biased before commanding a sequence up and down.

Note

TI recommends to decouple PULL_UPx inputs with a 1µF ceramic capacitor as close to the pins as possible. This is to ensure clean voltages signals at the outputs (ENx, PWRGD, and SEQ_DONE).

Each output stage consists of a PMOS/NMOS (CMOS) pair. Each leg has an output resistance of typically 7Ω for V_{PULL_UPx} > 3.3V. PULL_UP1 and PULL_UP2, have a voltage range of 1.6V to 7V, and can be independently biased or tied to the same voltage rail, however both most be biased. The output resistance of the PMOS leg has a PULL_UPx voltage dependency. The lower the PULL_UPx voltage, the higher the PMOS resistance.

When V_{IN} < V_{POR_IN} and V_{PULL_UPx} > $V_{POR\_PULL\_UPx}$ (1.4V maximum) the output will be in a known pull-down state. At this condition the outputs have reduced sinking capabilities with V_{OL} ≤ 320mV when the device is sinking 100µA of current into the outputs:

- ENx
- PWRGD
- SEQ_DONE

Once the input voltage range is withing the recommended input voltage range of 3V to 14V, the output will have the full strength capabilities of ±10mA, per output.

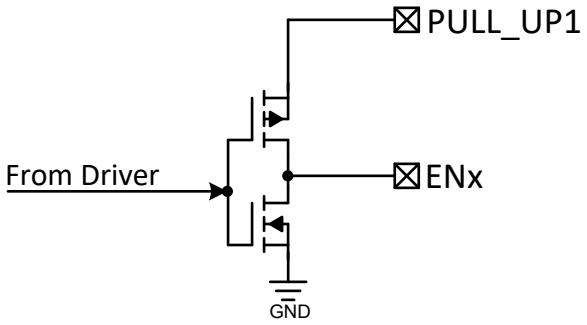


Figure 8-5. ENx Push-Pull Output Stages

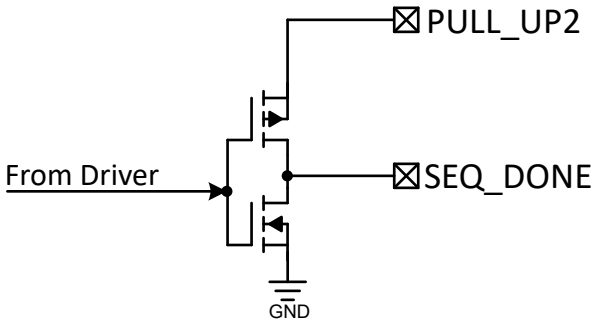


Figure 8-6. SEQ_DONE Push-Pull Output Stage

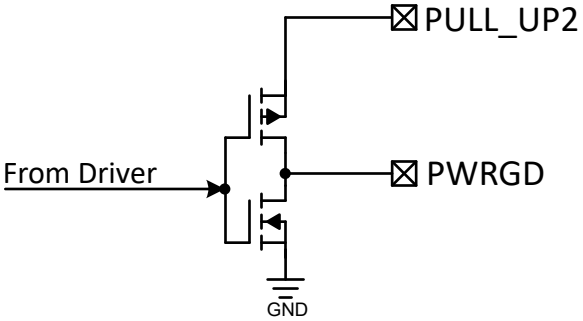


Figure 8-7. PWRGD Push-Pull Output Stage

8.3.4 User-Programmable TIMERS

The TPS7H3014 has two global (or common to all SENSEx channels) adjustable timers:

- DLY_TMR
- REG_TMR

Both timers are programmed via a single resistor from the DLY_TMR and REG_TMR pin to GND. The resistors are used to program the internal oscillator frequency of the timers. Leaving the DLY_TMR or the REG_TMR pin floating will disable the timer, respectively. Disabling the timers results in a reduced current consumption on the device (I_{Q_IN}). The range for both timers is 250µs to 25ms.

Note

Timers conditions must be valid at power up and must not be dynamically changed.

Figure 8-8 shows a sequence up and down assuming no faults and UP/DOWN pins tied together. The DLY_TMR is shown in orange and the REG_TMR time is shown with arrows (starting from ENx going high).

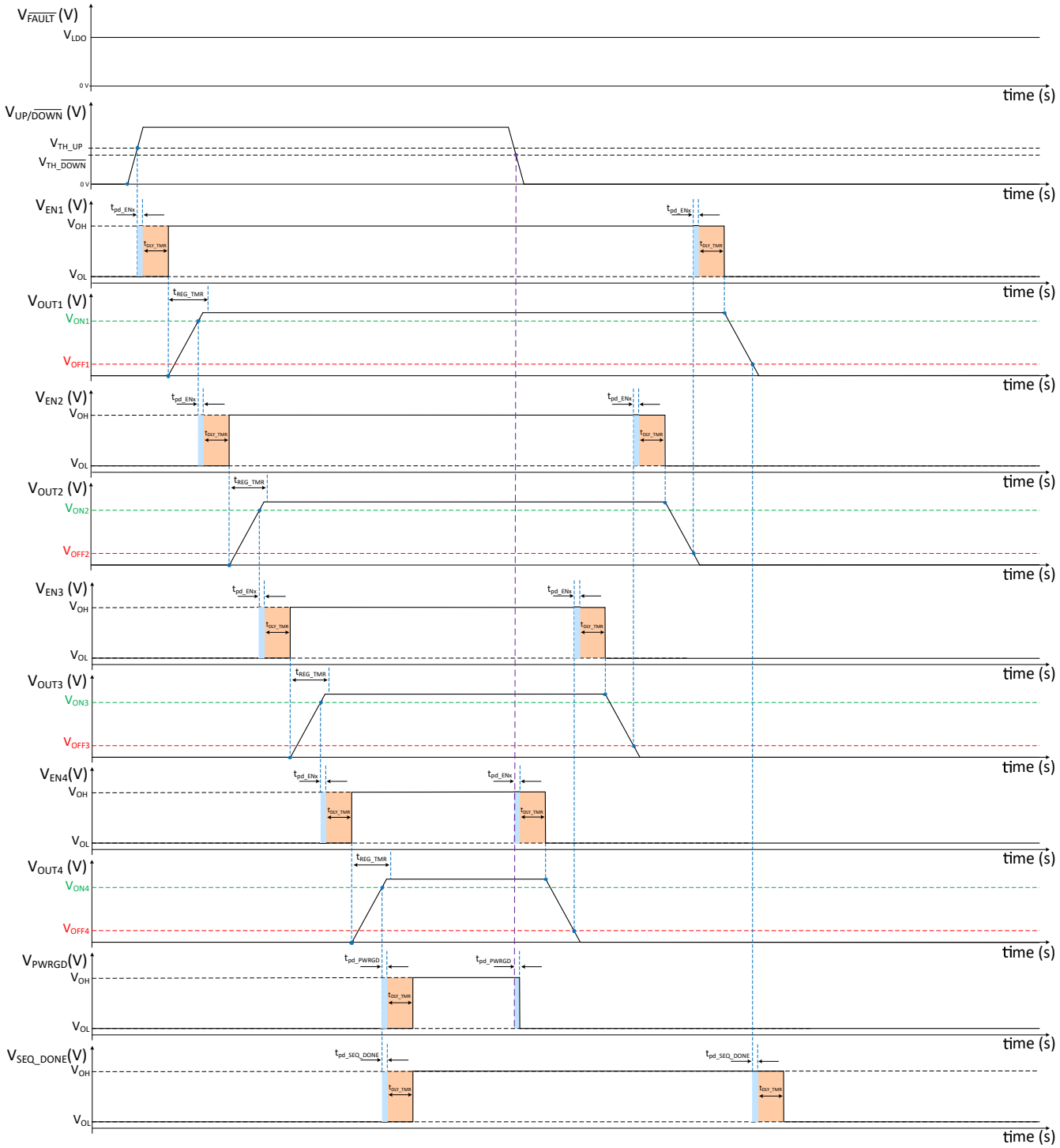


Figure 8-8. Sequence UP and DOWN

A. It's important to notice the t_{pd_ENx}, t_{pd_PWRGD}, and $t_{pD\_SEQ\_DONE}$ in blue. This is a propagation delay in the outputs (ENx,PWRGD and SEQ_DONE). If no DLY_TMR (floating) is used, the output signals will change to the valid state after this delay. When using the DLY_TMR, then this time has to be added to the programmed timer time.

B. The REG_TMR is only valid during sequence up.

8.3.4.1 DLY_TMR

The TPS7H3014 includes an adjustable time delay. A single resistor connected between the DLY_TMR pin and GND will program the delay. Possible resistor (R_{DLY}) values are between 10.5kΩ and 1.18MΩ for a 268µs to 23.63ms delay, respectively. During sequence up, this delay holds the EN_{x+1}, SEQ_DONE, and PWRGD low after the monitored voltage crosses the "on" voltage ($V_{OUTx} > V_{ONx}$) for the user programmed time. During sequence down, the $EN_{x–1}$ and SEQ_DONE are held high for the programmed delay time after the monitored voltage crosses the "off" voltage ($V_{OUTx} < V_{OFFx}$).

Note

During sequence down, PWRGD goes low immediately after the $V_{\overline{DOWN}} < V_{TH\_\overline{DOWN}}$.

If no delay is preferred for the system, the pin (DLY_TMR) can be left floating. When no delay is preferred, an inherent propagation delay of 6.5µs (max) will be observed during sequence up, between V_{OUTx} crossing the V_{ONx} and EN_{x+1} going high. The propagation delay is also observed during sequence down when V_{OUTx} cross the V_{OFFx} and the $EN_{x–1}$ is forced low. SEQ_DONE and PWRGD also have this propagation delay during $V_{OUT4} > V_{ON4}$ during sequence up. During sequence down, SEQ_DONE will go low after the propagation delay when $V_{OUT1} < V_{OFF1}$ and PWRGD will go low after the propagation delay when the sequence down is commanded. Figure 8-8 shows the propagation delay in blue (t_{pd_ENx}, $t_{pd\_SEQ\_DONE}$, t_{pd_PWRGD}) and the programmed delay (t_{DLY_TMR}) in orange. The DLY_TMR resistor can be selected using Equation 15 or Equation 16. Figure 8-9 and Figure 8-10 shows the linear trend between the DLY_TMR resistor and the delay time.

For t_{DLY_TMR} between 0.268ms and 12.5ms use:

$$R_{DLY\_TMR}(k\Omega) = \left[49.75 \times t_{DLY\_TMR}(ms)\right] - 2.832 \quad (15)$$

For t_{DLY_TMR} greater than 12.5ms use:

$$R_{DLY\_TMR}(k\Omega) = \left[51.61 \times t_{DLY\_TMR}(ms)\right] - 26.12 \quad (16)$$

Table 8-1 shows nominal resistors value for different delay times.

Table 8-1. Typical DLY_TMR Resistors

t_{DLY_TMR} (ms)	R_{DLY_TMR} (kΩ)
0.268	10.5
12.5	619
23.37	1180

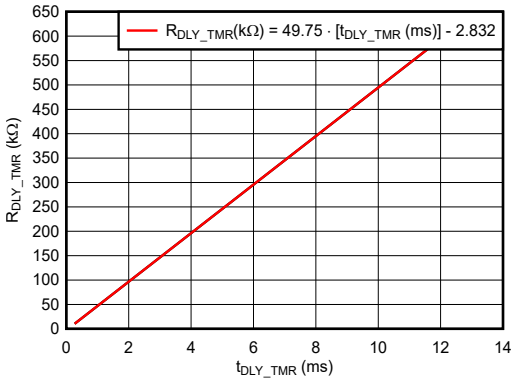


Figure 8-9. R_{DLY_TMR} vs t_{DLY_TMR} From 0.268ms to 12.5ms

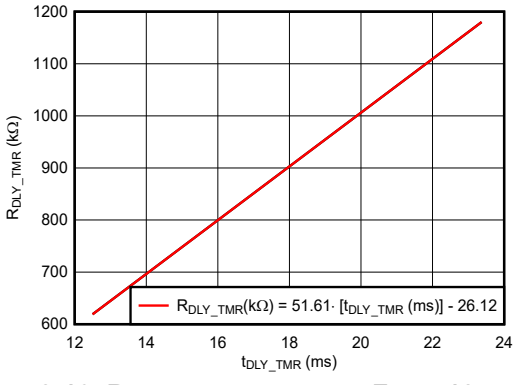


Figure 8-10. R_{DLY_TMR} vs t_{DLY_TMR} From 12.5ms to 23.37ms

8.3.4.2 REG_TMR

The REG_TMR (for regulation timer) is an adjustable time monitor that monitors the time it takes to V_{OUTx} > V_{ONx}. The user can program the REG_TMR using a single resistor between REG_TMR and GND. The range of the resistor (R_{REG}) is between 10.5kΩ to 1.18MΩ, for a 264µs to 23.63ms, respectively. If the user does not want the REG_TMR to be active, the pin can be left floating. In this case, V_{OUTx} has infinite time to cross the V_{ONx} voltage. The REG_TMR is only active during the sequence up.

Note

If the REG_TMR is left floating and the V_{ONx} voltage is never crossed, the state machine will stay waiting indefinitely.

If active, the REG_TMR will monitor the time a V_{OUTx} takes to cross the V_{ONx} voltage once the ENx signal is forced high. In the case the REG_TMR is expired and V_{OUTx} has not crossed the V_{ONx} voltage, a reverse sequence down from the previously sequenced rail will be started as described in the State Machine section. Figure 8-8 shows the REG_TMR active during sequence up, from the time ENx is forced high (V_{OUTx} starts rising). In this case, V_{OUTx} always crosses V_{ON} before the timer is expired. The REG_TMR resistor can be selected using Equation 17 and Equation 18. Figure 8-11 or Figure 8-12 shows the linear trend between the REG_TMR resistor and the regulation time allowed for the rail to be in regulation (V_{OUTx} > V_{ONx}).

For t_{DLY_TMR} between 0.264ms and 12.4ms use:

$$R_{DLY\_TMR}(k\Omega) = \left[50.14 \times t_{DLY\_TMR}\,(ms)\right] - 2.737 \quad (17)$$

For t_{DLY_TMR} greater than 12.4ms use:

$$R_{DLY\_TMR}(k\Omega) = \left[49.96 \times t_{DLY\_TMR}\,(ms)\right] - 0.4479 \quad (18)$$

Table 8-2 shows typical resistor values for different allowed regulation times.

Table 8-2. Typical REG_TMR Resistors

t_{REG_TMR} (ms)	R_{REG_TMR} (kΩ)
0.264	10.5
12.4	619
23.63	1180

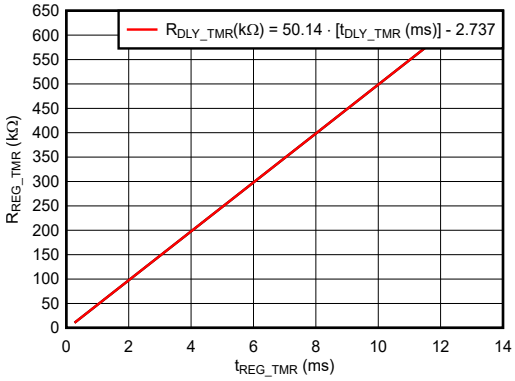


Figure 8-11. R_{REG_TMR} vs t_{REG_TMR} From 0.264ms to 12.4ms

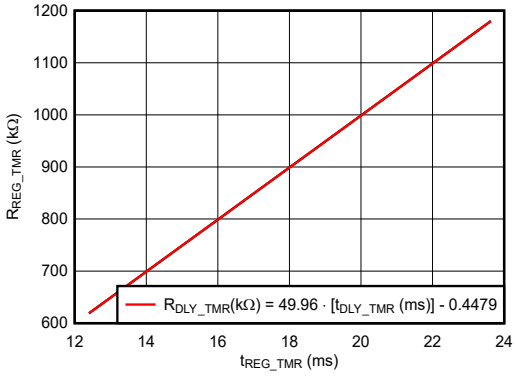


Figure 8-12. R_{REG_TMR} vs t_{REG_TMR} From 12.4ms to 23.63ms

8.3.5 UP and $\overline{DOWN}$

The UP and $\overline{DOWN}$ pins are the inputs that initiate a sequence up or down. Both pins incorporate an accurate comparator with a threshold voltage of V_{TH_UP} = 599mV (for UP) and $V_{TH\_\overline{DOWN}}$ = 498mV (for $\overline{DOWN}$) with an accuracy of ±3% for both inputs.

A fixed hysteresis of 100mV is incorporated in both comparators for noise stability. The edges on these pins are used to initiate the command as:

- Rising edge on UP starts a sequence up.
- Falling edge on $\overline{DOWN}$ starts a sequence down.

The UP voltage is also used in the state machine as a latch method to prevent oscillations during a FAULT. In order to move away from the Fault state, the UP voltage has to be logic low. As UP is a comparator with 100mV of hysteresis, depending on whether the V_{UP} have been previously above the V_{TH_UP}, the logic low level is:

- V_{TH_UP} ≤ 599mV (typ) if UP has not previously been above V_{TH_UP}.
- V_{UP_TH} (typically 600mV) – 100mV ≤ 500mV (typ) if UP has previously crossed V_{UP_TH}.

These inputs can be driven externally by a house-keeping controller or via a resistive divider connected to a voltage source.

As these inputs are edge sensitive, is important to have a stable input voltage ($UVLO_{RISE}$ < V_{IN} < 14V) for at least 2.8ms ($t_{Start\_up\_delay}$) before sending the sequence up command. This is due to internal time constants in the device. During sequence down, it's important to maintain a stable input voltage until the SEQ_DONE flag is set low to allow all rails to be properly sequenced down.

As both the UP and $\overline{DOWN}$ pins have accurate undervoltage comparators, the user can program the voltage at which the system will automatically start the sequence up and down when monitoring a main power rail (V_{MAIN}) via a resistive divider. However, in this case it is important to make sure the rising and falling edge are sent when V_{IN} is stable, as mentioned before. A capacitor can be added from UP to GND to delay the signal when the slew rate at V_{MAIN} is fast.

Usually the designer knows the voltages at which it's desired to start the sequence up (referred to as V_{UP_IDEAL}) and down (referred to as $V_{\overline{DOWN}\_IDEAL}$). With that information we can calculate the resistive divider values using Equation 19 and Equation 20. Usually the top resistor is fixed to a 10kΩ value.

$$R_{BOTTOM\_UP} = R_{TOP\_UP} \times \frac{V_{TH\_UP}}{V_{UP\_IDEAL} - V_{TH\_UP}} \tag{19}$$

$$R_{BOTTOM\_\overline{DOWN}} = R_{TOP\_\overline{DOWN}} \times \frac{V_{TH\_\overline{DOWN}}}{V_{\overline{DOWN}\_IDEAL} - V_{TH\_\overline{DOWN}}} \tag{20}$$

where:

- V_{TH_UP}= 598mV (typical)
- $V_{TH\_\overline{DOWN}}$ = 498mV (typical)

Once the designer knows the actual (real) resistive divider values, Equation 21 and Equation 22 can be used to calculate the sequence up and down nominal voltages as:

$$V_{UP\_NOMINAL}\ (V) = \left(1 + \frac{R_{TOP\_UP}}{R_{BOTTOM\_UP}}\right) \times V_{TH\_UP} \tag{21}$$

$$V_{\overline{DOWN}\_NOMINAL}\ (V) = \left(1 + \frac{R_{TOP\_\overline{DOWN}}}{R_{BOTTOM\_\overline{DOWN}}}\right) \times V_{TH\_\overline{DOWN}} \tag{22}$$

If desired, to select the capacitance (C_{DELAY}) for the UP pin we can use Equation 23.

$$C_{DELAY}\left(F\right) > \frac{t_{DELAY}(s)}{R_{TH}\left(\Omega\right) \times \ln\left(-\frac{V_{TH}(V)}{V(t) - V_{TH}(V)}\right)} \quad (23)$$

where:

- t_{DELAY} (s) is the desired delay time in seconds (at least 2.8ms after V_{IN} > $UVLO_{RISE}$).
- R_{TH} is the Thévenin equivalent resistance. In this case the parallel between R_{TOP} and R_{BOTTOM} in ohms.
  - $$R_{TH}\left(\Omega\right) = \frac{R_{TOP}\,(\Omega) \times R_{BOTTOM}(\Omega)}{R_{TOP}\,(\Omega) + R_{BOTTOM}(\Omega)} \quad (24)$$
- V_{TH} is the Thévenin equivalent voltage. In this case the voltage at V_{UP} during steady state operation in volts.
  - $$V_{TH}\left(V\right) = \left(\frac{R_{BOTTOM}(\Omega)}{R_{TOP}\,(\Omega) + R_{BOTTOM}(\Omega)}\right) \times V_{MAIN}\left(V\right) \quad (25)$$
- V(t) is the voltage at UP (V_{UP}) which will start the sequence up. In this case 598mV ±3%, in volts.

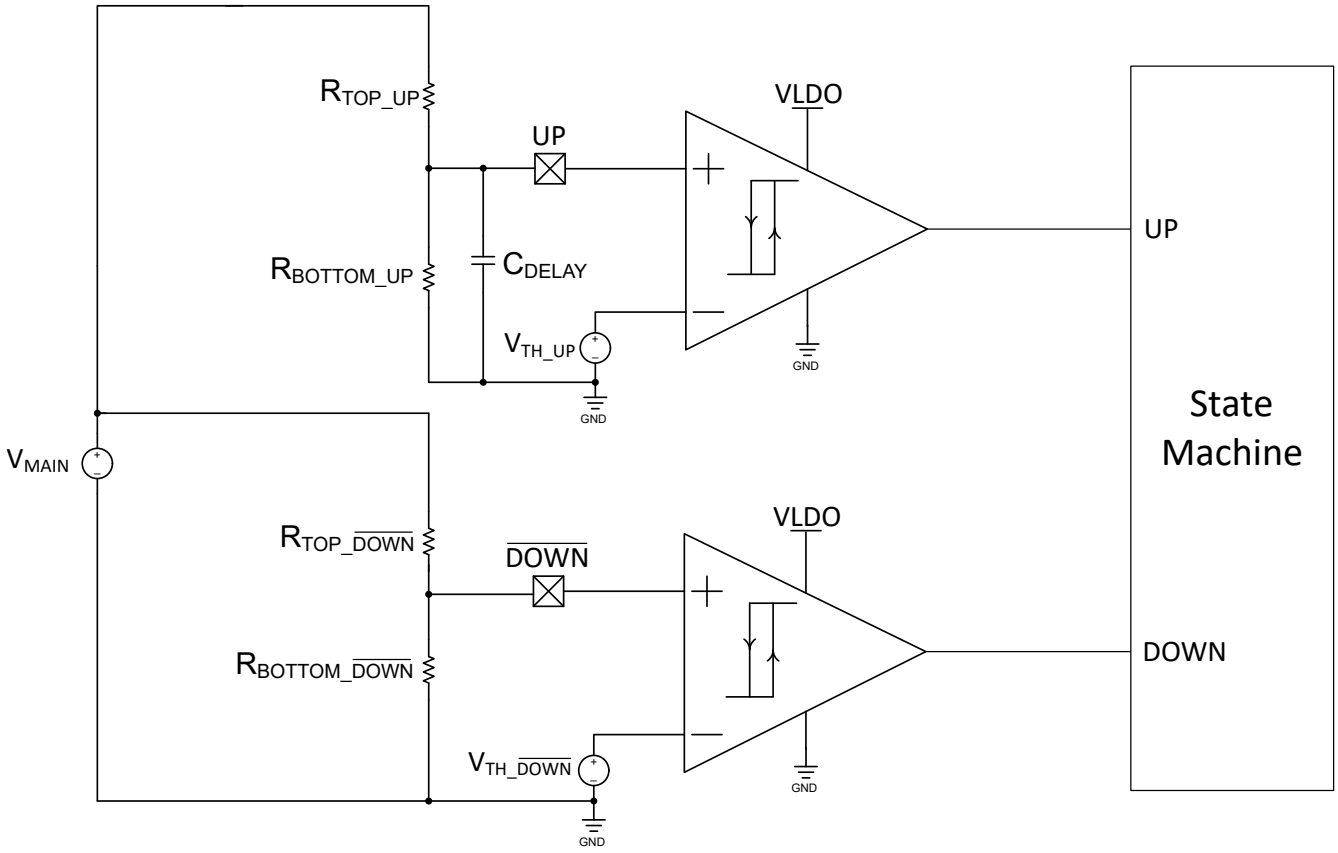


Figure 8-13. Monitor a Main Rail to Automatically Start the Sequence UP and $\overline{\text{DOWN}}$

8.3.6 FAULT

The $\overline{\text{FAULT}}$ pin is an open-drain output that the user can use to monitor if an internal fault has been induced by the state machine. Is recommended to pull this pin to the VLDO output via a 10kΩ resistor. Another voltage source can be used if needed, but is important that this voltage is stable and greater than 1V at all times. The maximum voltage at this pin is 7V. For proper operation this voltage must be stable before attempting a sequence up/down and must never go below 1V during the device operation. The open-drain FET is forced low when the internal state machine of the sequencer detects a fault as described in State Machine .

8.3.7 State Machine

The TPS7H3014 incorporates a comprehensive state machine engine. Three possible outcomes are possible depending on the detected inputs states.

1. A reverse sequence down from previously deemed-good (forced high) ENx signals, is started if:
   - V_{OUTx} fails to reach the V_{ONx} voltage during sequence up within the time establish by the REG_TMR, when ENx is high.
   - Any V_{OUTx} crosses the V_{OFFx} after previously crossing the V_{ONx} and the V_{OUTx+1} has not yet crossed the V_{ONx+1}.
   - The users command a sequence down in the middle of a sequence up.
2. All outputs (ENx, SEQ_DONE and PWRGD) are forced low if an out-of-order is detected, this means:
   - A previously deemed-good rail V_{OUTx} drops below V_{OFFx} when at least the V_{OUTx+1} is already in regulation (deemed-good).
   - Any $V_{OUTx} > V_{ONx}$ when EN_X is not high. **Valid only during sequence up**.

   Note

   It is typical in sequencers to set V_{ONx} as some percentage of the nominal voltage to be monitored (E.g. $V_{ONx} = 0.8 \times V_{OUTx}$). There is a period of time during sequence down at which the $V_{OUTx} \geq V_{ONx}$. As the discharge rate of the rail (V_{OUTx}) is unknown to the TPS7H3014, this feature is only valid during sequence up.
3. A sequence up from previously forced low ENx signals, after the DLY_TMR is expired is started if:
   - The users command a sequence up in the middle of a sequence down.

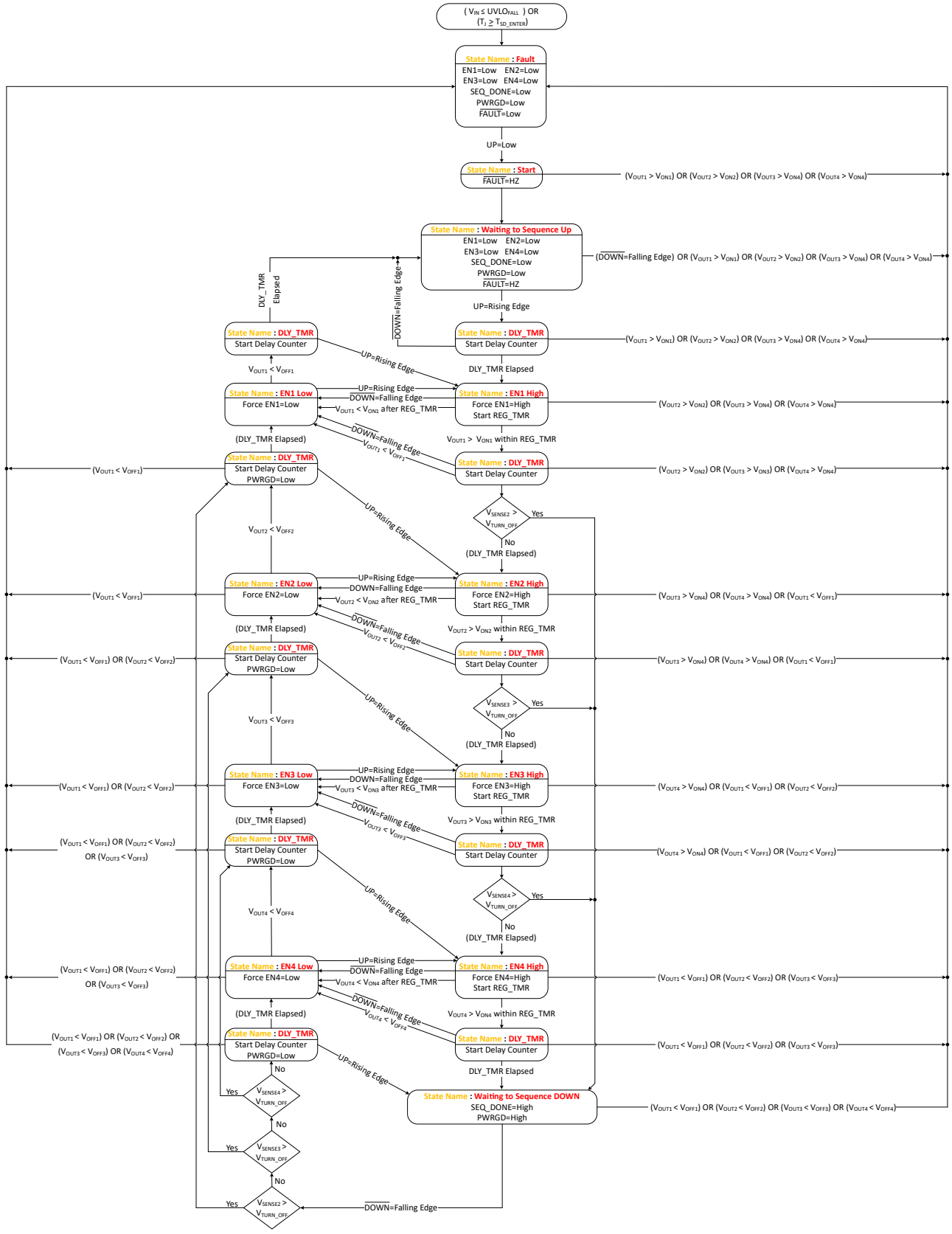


Figure 8-14. TPS7H3014 State Machine Diagram

8.4 Daisy Chain

The TPS7H3014 incorporates four input channels to sequence/monitor up to four voltage rails. However, in the case where more than four channels are needed in the application, multiple devices can be daisy chained as needed. The daisy chain configuration is shown in Figure 8-15. In this case, only two devices are shown, however multiple IC can be configured as needed by the application.

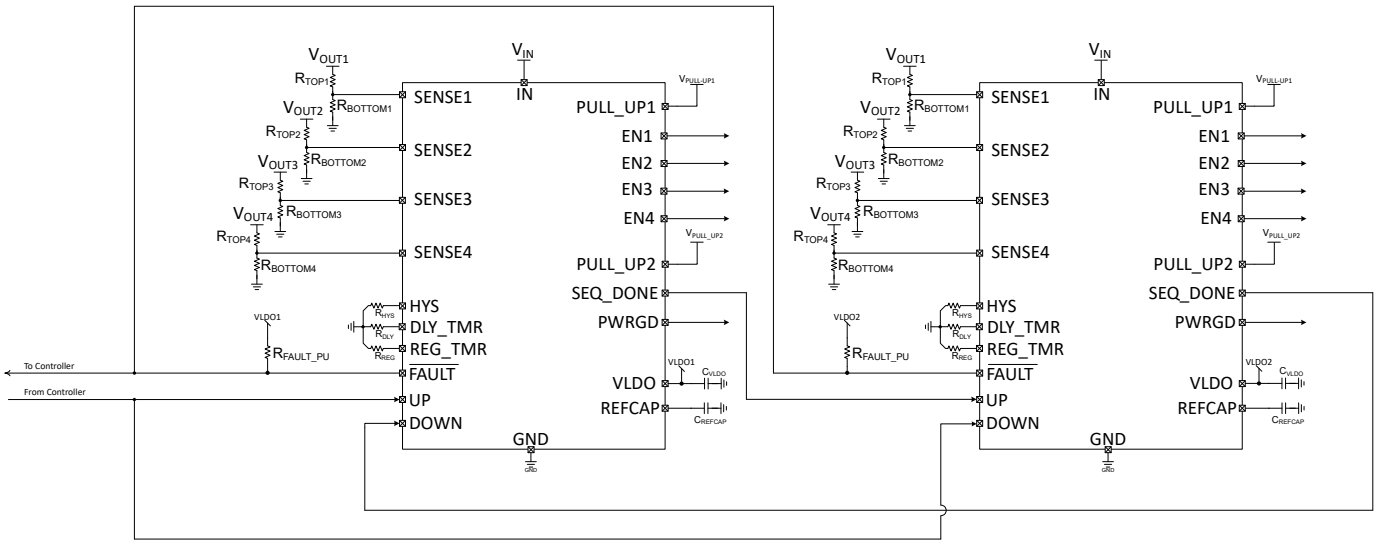


Figure 8-15. Daisy Chain Configuration

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H3014 is a radiation hardened 4-channel sequencer. It can be used to sequence FPGAs, ASICs, AFEs, and various power systems

9.2 Typical Application

9.2.1 Self Contained – Sequence UP and DOWN

In many modern systems (or sub-systems), multiple voltage rails are often needed (we refer to this as the power tree). Often these power trees have a specified sequencing up order and reverse sequence down needed to guarantee reliable system operation. Is not uncommon for these systems to also have timing specifications which cannot be infringed for correct operation. In this example, four voltage rails are sequenced and monitored via the ENx outputs and SENSEx inputs, respectively. Detailed design procedure and component selection is provided below. The design is summarized in Figure 9-1.

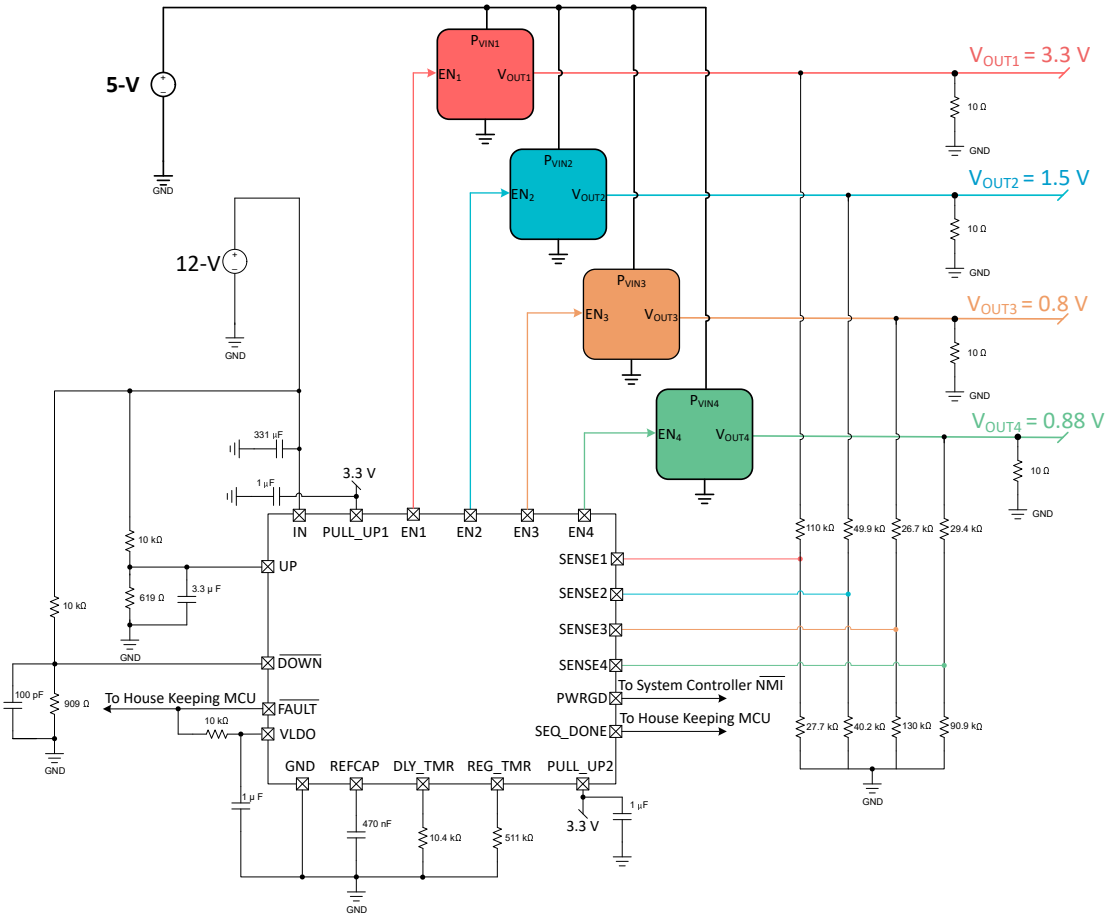


Figure 9-1. Self Contained Sequence UP/DOWN Design for a Four Voltage Rail Power Tree

9.2.1.1 Design Requirements

This design requires voltage sequencing of four voltage rails. The nominal TPS7H3014 input voltage is 12V and the sequencer is set to start the sequence up and down automatically when the voltage reaches the desired target voltage levels. All the voltage regulators are powered by a nominal 5V voltage rail. The system housekeeping microcontroller can monitor a fault via the voltage at the $\overline{\text{FAULT}}$ pin, which is pulled-up to VLDO. The PWRGD is the flag to be connected to the non-maskable interrupt of the system if it exists, or monitored by the MCU to know the status of the power tree. The SEQ_DONE can also be monitored to know if the sequence up/down are completed. All design conditions are defined in Table 9-1.

Table 9-1. Design Conditions

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
System nominal voltage	Monitor the 12V input voltage and start the sequence up when the voltage is greater than 10.7V (88%) for at least 3.7ms. When the voltage decrements below 6V (or 50%) a sequence down is started.	The TPS7H3014 can monitor a voltage and start a sequence up and down automatically via a resistive divider. The internal reference in UP and $\overline{\text{DOWN}}$ have an accuracy of 3%. For minimal error, it is recommended to use 0.1% tolerance resistors.
V_{OUT1}	3.3V nominal with: V_{ON} = 90% and V_{OFF} = 10%	V_{ON} = 2.978V ±29.97mV V_{OFF} = 0.338V ±84.61mV Using 0.1% tolerance resistors
V_{OUT2}	0.8V nominal with: V_{ON} = 90% and V_{OFF} = 10%	V_{ON} = 0.722V ±7.22 mV V_{OFF} = 0.081V ±20.54mV Using 0.1% tolerance resistors
V_{OUT3}	1.5V nominal with: V_{ON} = 90% and V_{OFF} = 10%	V_{ON} = 1.343V ±13.47mV V_{OFF} = 0.145V ±38.35mV Using 0.1% tolerance resistors
V_{OUT4}	0.88V nominal with: V_{ON} = 90% and V_{OFF} = 10%	V_{ON} = 0.793V ±7.93mV V_{OFF} = 0.087V ±22.6mV Using 0.1% tolerance resistors
ENx delay during sequence up and down	Delay of 0.268ms nominal	R_{DLY_TMR} = 10.4kΩ
Allowed time for a rail to reach the V_{ONx}	Allow 10.3ms (nominal) for the rail to reach the V_{ONx}	R_{REG_TMR} = 511kΩ

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Input Power Supplies and Decoupling Capacitors

The TPS7H3014 has three input power supplies:

1. IN, the input supply to provide power to the TPS7H3014 IC. It is recommended to decouple this power supply with at least 1µF as close to the pin as possible. In this application, V_{IN} = 12V.
2. PULL_UP1, which is the input supply to program the output voltage high (V_{OH}) of all the enable outputs (ENx). These outputs are connected to the regulator enable inputs to control the sequence up and down. It is recommended to decouple this power supply with at least 1µF as close to the pin as possible. In this application, the V_{PULL_UP1} = 3.3V. This is a typical voltage used in electronic systems and satisfies the logic inputs of most regulators in the market.
3. PULL_UP2, which is the input supply to program the output voltage high (V_{OH}) of PWRGD and SEQ_DONE outputs. These outputs are typically connected to the system controller (typically an FPGA or ASIC) and/or to the house-keeping controller. In daisy chain configurations, SEQ_DONE is connected to UP of subsequent TPS7H3014 I.C. as shown in Figure 8-15. It is recommended to decouple this power supply with at least 1µF as close to the pin as possible. In this application, the V_{PULL_UP1} = 3.3V. This is a typical voltage of controller I/Os.

The TPS7H3014 also has two regulated voltage outputs that need to be decoupled for good electrical and radiation performance. These are:

1. REFCAP, the 1.2V reference, used internally in the device to generate all ratiometric voltage reference such as:
   - V_{TH_SENSEx}
   - I_{HYS_SENSEx}
   - V_{TH_UP}
   - $V_{TH\_\overline{DOWN}}$

   Decouple this reference with a 470nF ceramic capacitor as close to the pin as possible. Do not load this pin externally.
2. VLDO, this is the output of the internal regulator used to provide power to the internal circuits on the TPS7H3014. Is recommended to decouple this regulator with at least 1µF as close to the pin as possible. The valid loading of this regulator is:
   - To turn-off channels 2–4 as needed.
   - To pull-up the $\overline{FAULT}$ open-drain output.

9.2.1.2.2 UP and $\overline{DOWN}$ Thresholds

In this application the UP and $\overline{DOWN}$ pins are used to monitored the input voltage supply of 12V. A sequence up is started when the rail voltage is greater than 10.7 (typ) and down when the voltage is lower than 6V (typ). As the TPS7H3014 has an internal time constant ($t_{Start\_up\_delay}$) of 2.8ms (max), a delay capacitor of 3.3µF is added to UP pin. This capacitor is added to introduce a delay in the UP pin when V_{IN} is rising. This capacitor adds a second condition to start the sequence up, if V_{IN} ≥ 10.7V (typ) for at least 2.8ms then the sequence up is commanded.

Fixing the upper resistor for the resistive divider in UP and $\overline{DOWN}$, we can calculate the bottom resistor per our design requirements. The upper resistor is fixed to 10kΩ for both cases. Using the equations in Equation 19 and Equation 20, the bottom resistors for up and down are calculated as:

$$R_{BOTTOM\_UP} = 10\ k\Omega \times \frac{0.598\ V}{10.7\ V - 0.589\ V} \cong 594\ \Omega \tag{26}$$

$$R_{BOTTOM\_\overline{DOWN}} = 10\ k\Omega \times \frac{0.498\ V}{6\ V - 0.498\ V} \cong 905\ \Omega \tag{27}$$

Now that the reference resistors are calculated, we can select the actual (or real) resistors. In this case 0.1% tolerance resistors are used to select the closest value as:

- R_{BOTTOM_UP} = 619Ω
- $R_{BOTTOM\_\overline{DOWN}}$ = 909Ω

With the actual resistor values, we can back-calculate the nominal voltage to start the sequence up and down using Equation 21 and Equation 22 as:

$$V_{UP\_NOMINAL}(V) = \left(1 + \frac{10\ k\Omega}{619\ \Omega}\right) \times 12\ V \cong 10.66\ V \tag{28}$$

$$V_{\overline{DOWN}\_NOMINAL}(V) = \left(1 + \frac{10\ k\Omega}{909\ \Omega}\right) \times 12\ V \cong 5.97\ V \tag{29}$$

The delay capacitor is calculated using Equation 23, Equation 24, and Equation 25 as:

$$R_{TH}(\Omega) = \frac{10\ k\Omega \times 619\ \Omega}{10\ k\Omega + 619\ \Omega} = 582.9\ \Omega \tag{30}$$

$$V_{TH}(\Omega) = \left(\frac{619\ \Omega}{10\ k\Omega + 619\ \Omega}\right) \times 12\ V = 0.7\ V \tag{31}$$

$$C_{DELAY}(F) \geq \frac{0.0028\ s}{582.9\ \Omega \times \ln\left(-\frac{0.7\ V}{0.598\ V - 0.7\ V}\right)} = 2.49\ \mu F \tag{32}$$

The delay capacitor is selected as 3.3µF.

9.2.1.2.3 SENSEx Thresholds

The SENSEx inputs are used to monitor the voltage rails to be sequenced up and down. For this design the output voltages to be sequenced and monitored are:

1. V_{OUT1} = 3.3V
2. V_{OUT2} = 0.8V
3. V_{OUT3} = 1.5V
4. V_{OUT4} = 0.88V

The V_{ON} and V_{OFF} are selected to be 90% and 10% of the nominal voltage rail, for all the rails. Using Equation 13 and Equation 14 we can calculate the top and bottom reference resistors and select the closest resistor values using 0.1% resistor values. Table 9-2 shows the reference (or calculated) top and bottom resistors. Table 9-3 shows the selected resistors for the application.

Table 9-2. SENSEx Reference Nominal Resistors

Channel #	V_{ON} (V)	V_{OFF} (V)	R_{TOP} (kΩ)(1)	R_{BOTTOM} (kΩ)(1)
1	2.970	0.330	110.0	27.8
2	1.350	0.150	50.0	39.9
3	0.720	0.080	26.7	132.0
4	0.792	0.088	29.3	91.0

(1) Values are rounded to one decimal place.

An example of how the top and bottom resistors for channel 1 (or SENSE1) were calculated are shown below:

$$\frac{2.970\ \text{V} - 0.330\ \text{V}}{24\ \mu\text{A}} = 110\ \text{k}\Omega \tag{33}$$

$$\frac{110\ \text{k}\Omega \times 0.599\ \text{V}}{2.970\ \text{V} - 0.599\ \text{V}} = 39.88\ \text{k}\Omega \tag{34}$$

Table 9-3. SENSEx Selected Resistors Using 0.1 % Tolerance Resistors

Channel #	R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)
1	110	27.7
2	49.9	40.2
3	26.7	130
4	29.4	90.9

Now that the actual resistors are known, we can calculate the actual on and off nominal voltages and the error voltages by using Equation 1, Equation 2, Equation 3, Equation 6, Equation 7, and Equation 12. Using the errors, we can calculate the upper and lower voltages and normalize the values with respect to the nominal output voltage.

Table 9-4. V_{ON} Nominal Values With Statistics in Volts and Percentage

Channel #	$V_{ON\_NOMINAL}$ (V)(1)	$V_{ON\_NOMINAL}$ (%)(1) (4)	V_{ON_ERROR} (mV)(1)	V_{ON_LSL} (V)(1) (2)	V_{ON_LSL} (%)(1) (2) (4)	V_{ON_USL} (V)(1) (3)	V_{ON_USL} (%)(1) (3) (4)
1	2.978	90.232	29.966	2.948	89.325	3.008	91.141
2	1.343	89.502	13.466	1.329	88.605	1.356	90.400
3	0.722	90.253	7.222	0.715	89.350	0.729	91.156
4	0.793	90.084	7.932	0.785	89.182	0.801	90.985

(1) Values are rounded to three decimal places.
(2) LSL stands for lower specification limit or the min.
(3) USL stands for upper specification limit or the max.
(4) Values are normalized to the nominal output voltage for that rail.

Table 9-5. V_{OFF} Nominal Values with Statistics in Volts and Percentage

Channel #	$V_{OFF\_NOMINAL}$ (V)(1)	$V_{OFF\_NOMINAL}$ (%)(1) (4)	V_{OFF_ERROR} (mV)(1)	V_{OFF_LSL} (V)(1) (2)	V_{OFF_LSL} (%)(1) (2) (4)	V_{OFF_USL} (V)(1) (3)	V_{OFF_USL} (%)(1) (3) (4)
1	0.338	10.233	84.613	0.253	7.669	0.422	12.797
2	0.145	9.662	38.354	0.107	7.105	0.183	12.219
3	0.081	10.153	20.535	0.061	7.586	0.102	12.720
4	0.087	9.902	22.604	0.065	7.333	0.110	12.470

(1) Values are rounded to three decimal places.
(2) LSL stands for lower specification limit.
(3) USL stands for upper specification limit.
(4) Values are normalized to the nominal output voltage for that rail.

9.2.1.3 Application Curves

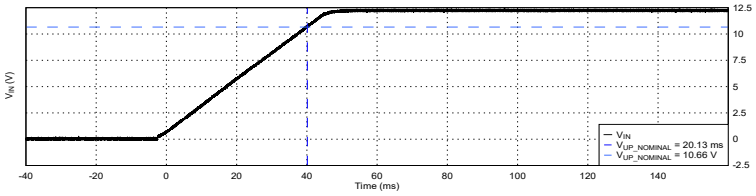


Figure 9-2. V_{IN} vs Time During Sequence UP

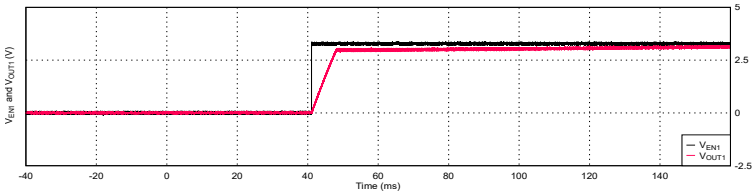


Figure 9-3. EN1 and V_{OUT1} vs Time During Sequence UP

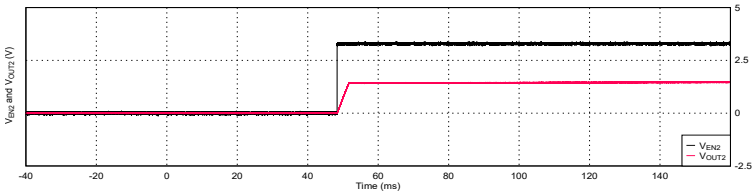


Figure 9-4. EN2 and V_{OUT2} vs Time During Sequence UP

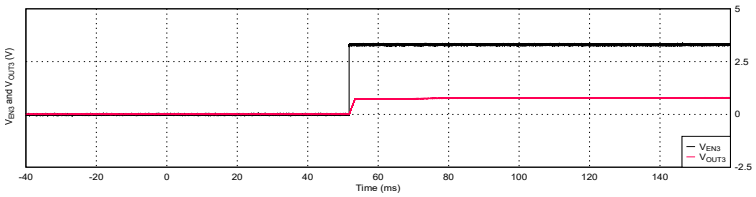


Figure 9-5. EN3 and V_{OUT3} vs Time During Sequence UP

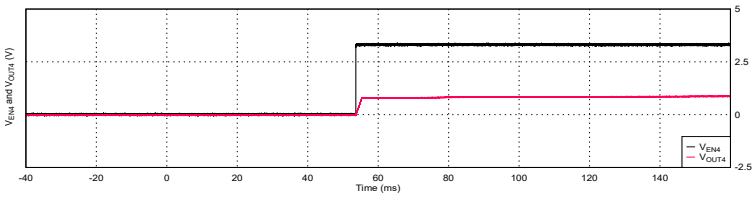


Figure 9-6. EN4 and V_{OUT4} vs Time During Sequence UP

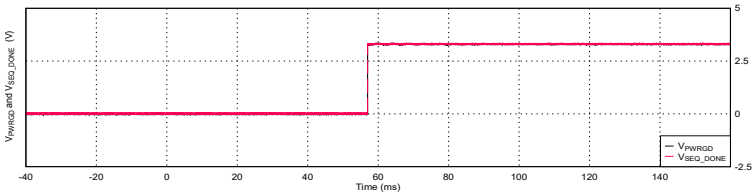


Figure 9-7. PWRGD and SEQ_DONE vs Time During Sequence UP

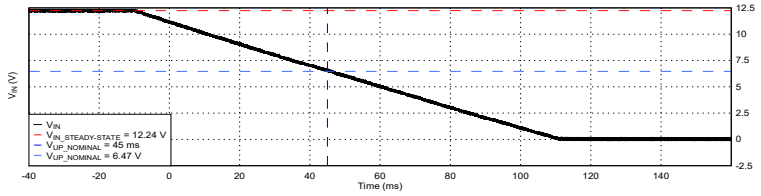


Figure 9-8. V_{IN} vs Time During Sequence DOWN

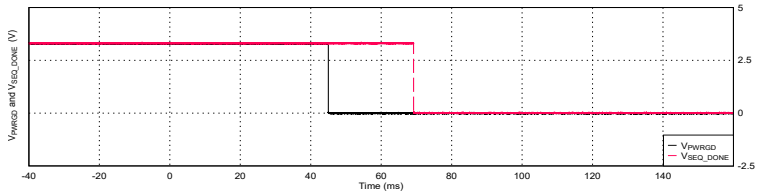


Figure 9-9. PWRGD and SEQ_DONE vs Time During Sequence DOWN

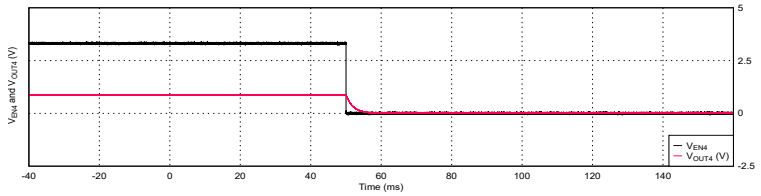


Figure 9-10. EN4 and V_{OUT4} vs Time During Sequence DOWN

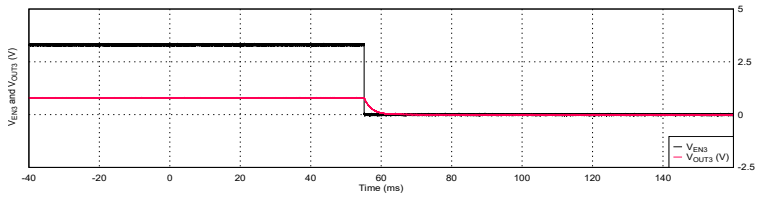


Figure 9-11. EN3 and V_{OUT3} vs Time During Sequence DOWN

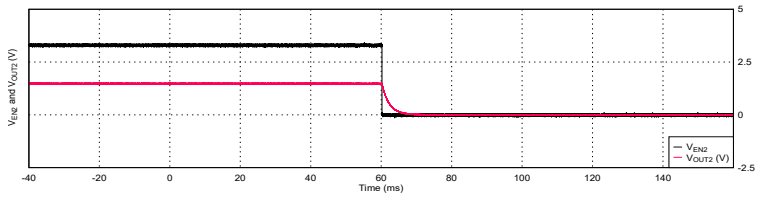


Figure 9-12. EN2 and V_{OUT2} vs Time During Sequence DOWN

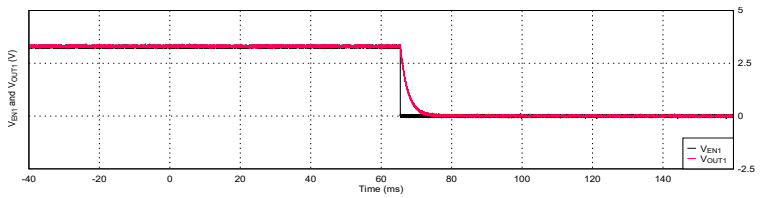


Figure 9-13. EN1 and V_{OUT1} vs Time During Sequence DOWN

9.2.2 Sequencing of Negative Voltage Rails

It is possible to sequence negative voltage rails using the TPS7H3014 with the support of some external circuitry such as:

1. Stable positive voltage reference.
2. Comparator with hysteresis.

Figure 9-14, shows the typical connections to sense a negative voltage rail. When $-V_{OUTx}$ is at zero volts (initial state), the voltage at the inverting input of the external comparator is given by Equation 35. The resistive divider is selected such that the initial voltage at the non-inverting input of the comparator is greater than the reference voltage by a desired factor. This factor depends on the desired threshold at which the negative voltage must be considered to be in regulation.

When the negative voltage rail ($-V_{OUTx}$) is turned-on the voltage at the non-inverting inputs starts decrementing until $-V_{OUTx}$ reaches steady-state. When the voltage at the non-inverting input is lower than the reference voltage the output of the comparators is forced high (the high value is determined by the positive bias of the comparator, V_+).

As the TPS7H3014 implements the hysteresis via a current, when the output of the external comparator is high, a typical 24µA ($I_{HYS\_SESNSEx}$) are sunk into the output of the comparator. The selected comparator needs to be able to withstand this current sinking while maintaining a constant output.

R_x, R_y and R_h resistors attenuate the V_+ voltage to provide the thresholds that ultimately determines when the $-V_{OUTx}$ is considered to in or out of regulation. For more details refer to TIDU020 and Section 9.2.2.1.

$$V_{INVERTING\_INPUT}\left(V\right) = \left(\frac{R_{TOP}(\Omega)}{R_{TOP}(\Omega) + R_{BOTTOM}(\Omega)}\right) \times V_{OFFSET}\left(V\right) \quad (35)$$

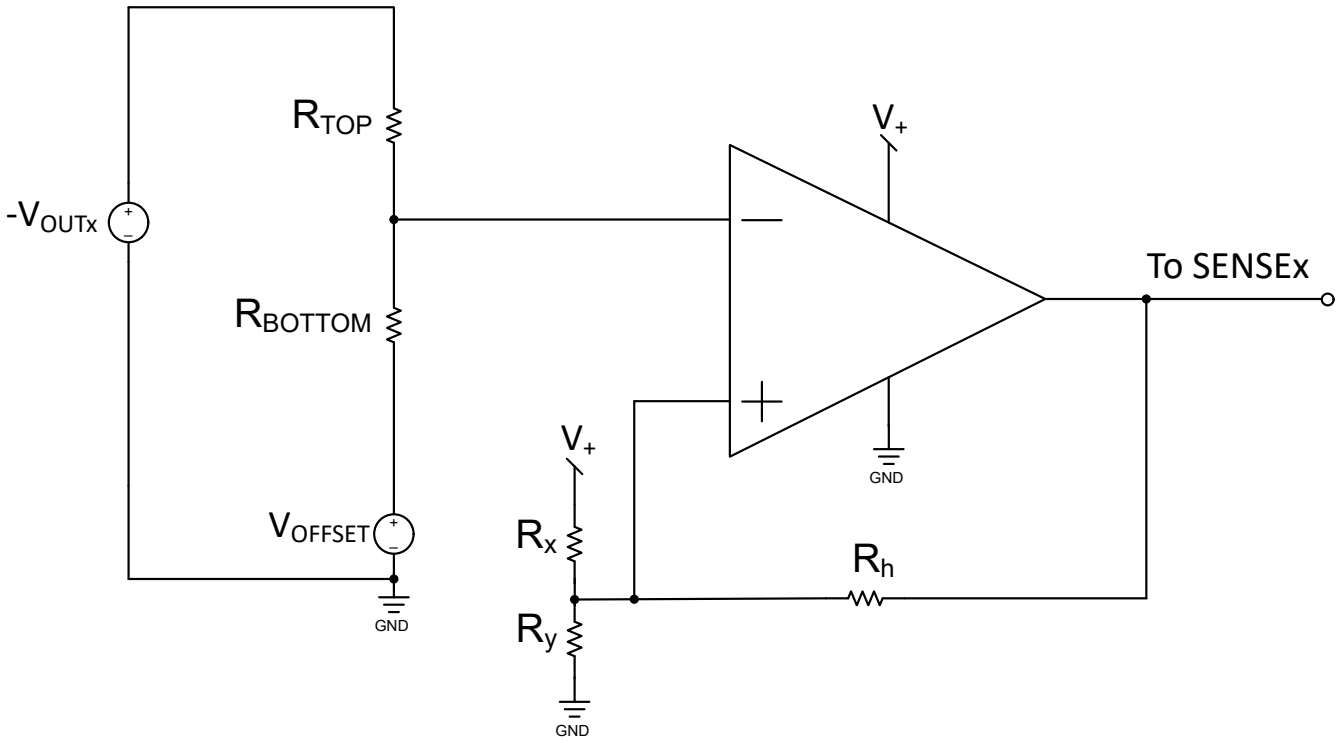


Figure 9-14. Sensing Negative Rails Using External Circuitry

Note

- When using external components to sense negative voltage rail the rising and falling threshold accuracy are dependent upon the external circuitry selected.
- The high voltage of the comparator most be below V_{TURN_OFF}, otherwise the channel is internally disabled. An resistive divider can be used to attenuate the output of the comparator if needed.

9.2.2.1 Negative Voltage Design Equations

For the purpose of this discussion the following assumptions are made:

1. V_+ is provide from 2.5V stable reference voltage.
2. The output stage of the comparator is push-pull.
3. The negative voltage to be sequenced is –1.8V at steady-state.

The first step in the design is to select the voltages (or percent of the steady-state voltage) at which the negative rail is considered to be:

- In regulation
  - The –1.8V rail is considered to be in regulation when it is > to 97% of the final value. In this case 1.746V. We refer to this as the on voltage (V_{ON})
- Not in regulation.
  - The –1.8V rail is considered not be in regulation when it is < to 95% of the final value. In this case 1.71V. We refer to this as the off voltage (V_{OFF})

With this information we can calculate the hysteresis voltage as:

$$V_{hys}(V) = V_{ON}(V) - V_{OFF}(V) = 1.746V - 1.71V = 0.036V \quad (36)$$

The second step is determine the R_x, R_y and R_h resistors values used to generate the hysteresis reference voltages. These voltages are called V_L and V_H. We select V_L to be an attenuated value from the 2.5V reference. In this example we select V_L as 0.6V. V_H is calculated as:

$$V_H(V) = V_L(V) + V_{hys}(V) = 0.6V + 0.036V = 0.636V \quad (37)$$

With this information we can calculate the resistor ratio as:

$$\frac{R_h}{R_x} = \frac{V_L(V)}{V_{hys}(V)} = \frac{0.6}{0.036} = 16.67 \quad (38)$$

$$\frac{R_y}{R_x} = \frac{V_L(V)}{V_+(V) - V_H(V)} = \frac{0.6}{2.5 - 0.636} = 0.32 \quad (39)$$

The R_x value selected is 10kΩ and R_y and R_h are calculated using Equation 38 and Equation 39. Using 0.1% tolerance resistors the selected values are:

- R_y = 3.2kΩ
- R_h = 165kΩ

As the actual resistors are known, we can calculate the actual V_L and V_H to be:

- V_{H_REAL} = 0.633V
- V_{L_REAL} = 0.597V

Finally we want to calculate the resistors for R_{TOP} and R_{BOTTOM} per Figure 9-14. For this we can calculate an equivalent voltage at the inverting input when the $–V_{OUTx}$ must be considered to be on regulation as:

$$-V_{OUT\_EQ}(V) = V_{OFFSET}(V) - V_{ON}(V) = 2.5V - 1.746V = -0.754V \quad (40)$$

Using this equivalent voltage and V_{L_REAL} we can calculate the ratio of the bottom to top resistor as:

$$\frac{R_{BOTTOM}}{R_{TOP}} = \frac{V_{L\_REAL}(V)}{|-V_{OUT\_EQ}(V)| - V_{L\_REAL}(V)} = \frac{0.597}{0.754 - 0.597} = 3.8 \quad (41)$$

Using 0.1 % tolerance resistors and fixing R_{TOP} to 10kΩ, R_{BOTTOM} is selected as 38.2kΩ.

Now that all the final components are selected, we can calculate the real (or expected) on and off voltages as V_{ON} = 1.746V and V_{OFF} = 1.701V

9.3 Externally Induced System RESET

In applications when it is necessary to propagate an externally detected fault into the TPS7H3014, an external FET can be connected from SENSE1 to GND. If SENSE1 is pulled to zero by turning on the FET connected to this pin, the internal state machine forces all outputs low. The FET off leakage ultimately affects the V_{OUT1} on and off accuracy. For this reason, it is important to choose a FET with minimal leakage. For more details, refer to section 3.6 (Externally Induced System RESET) in the TPS7H3014EVM-CVAL EVM User Guide.

9.4 Power Supply Recommendations

The TPS7H3014 is designed to operate from an input supply (V_{IN}) with a voltage range between 3V to 14V. It is recommended to add at least one 1µF ceramic capacitor from V_{IN} to GND as close to the pin as possible.

The PULL_UP1 and PULL_UP2 are also considered power inputs in this case for the push-pull outputs. The voltage range on these inputs are 1.6V to 7V. For these inputs, it is also recommend to add at least one 1µF ceramic capacitor from PULL_UP1 to GND and from PULL_UP2 to GND. This capacitor must be placed as close to the pins as possible.

9.5 Layout

9.5.1 Layout Guidelines

- Make sure that the connection to the V_{IN} pin is low impedance. Place a greater than 1µF ceramic capacitor as near as possible to the V_{IN} pin.
- Make sure that the connection to the V_{PULL_UP1} and V_{PULL_UP2} pins are low impedance. Place a greater than 1µF ceramic capacitor as near as possible to the pins.
- If needed, place a small capacitor between the SENSEx pins and GND to reduce the sensitivity to transient voltages on the monitored signal.

9.5.2 Layout Example

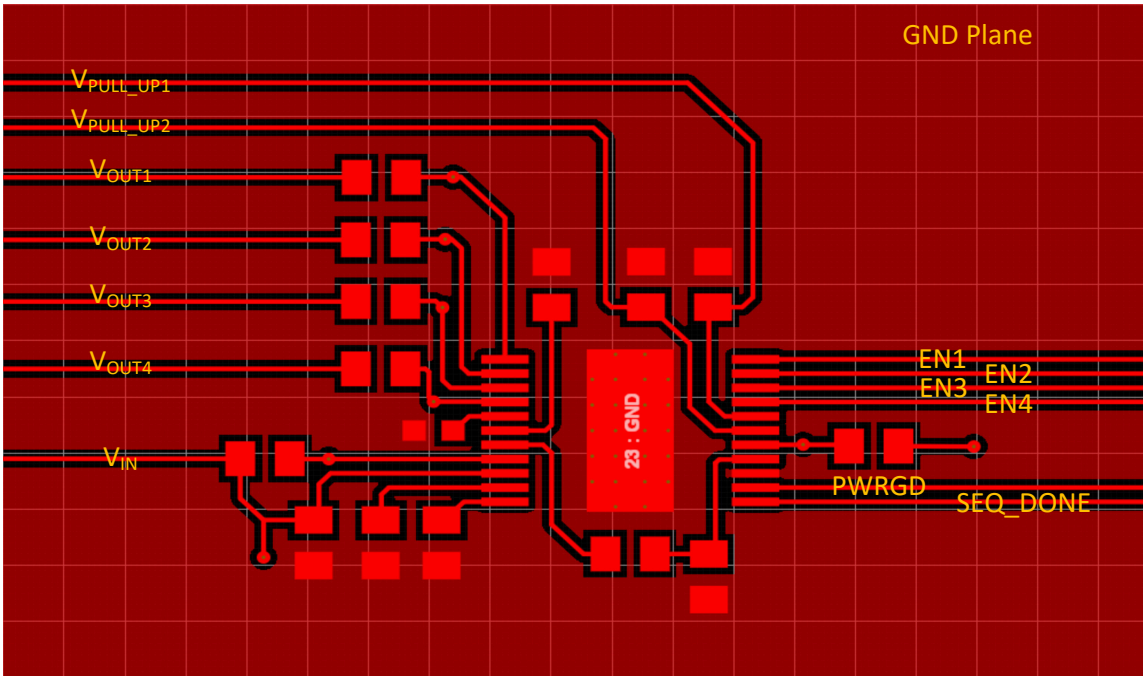


Figure 9-15. Printed Circuit Board Layout Example: Top Layer

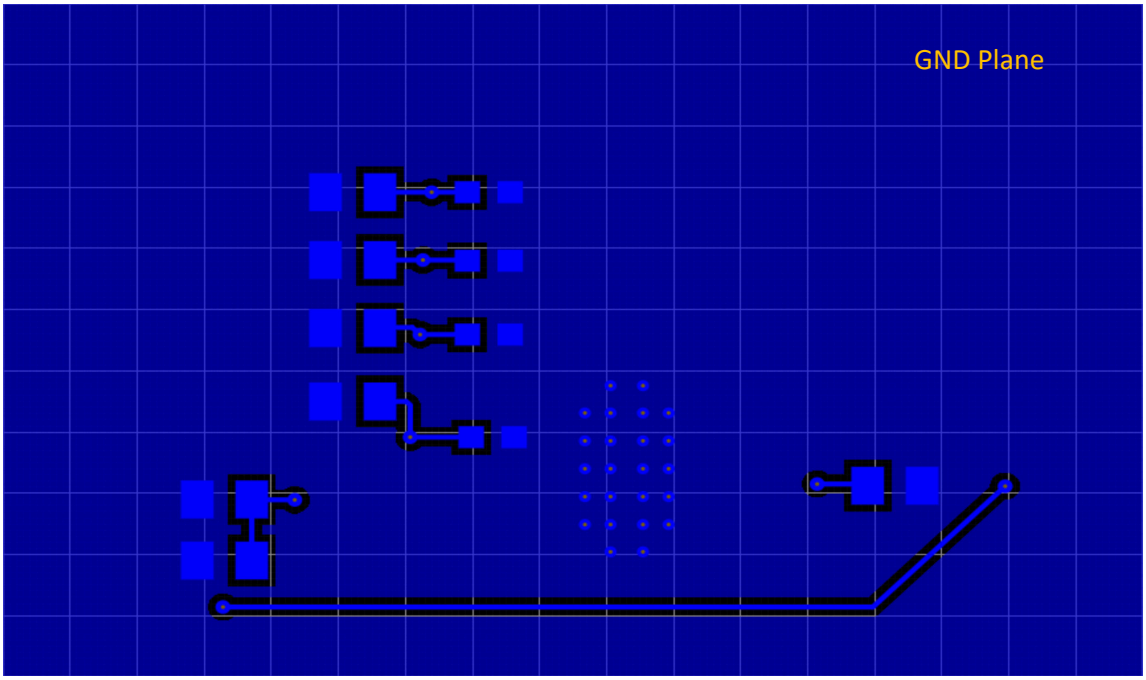


Figure 9-16. Printed Circuit Board Layout Example: Bottom Layer

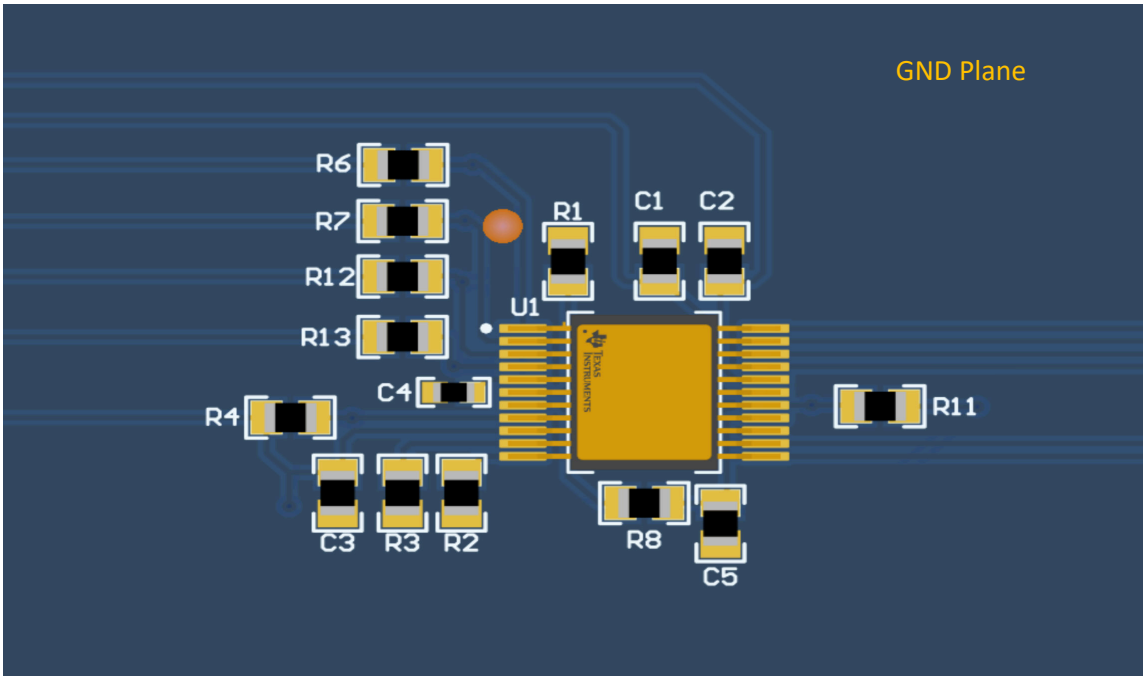


Figure 9-17. Printed Circuit Board Layout Example: Top Layer 3D View

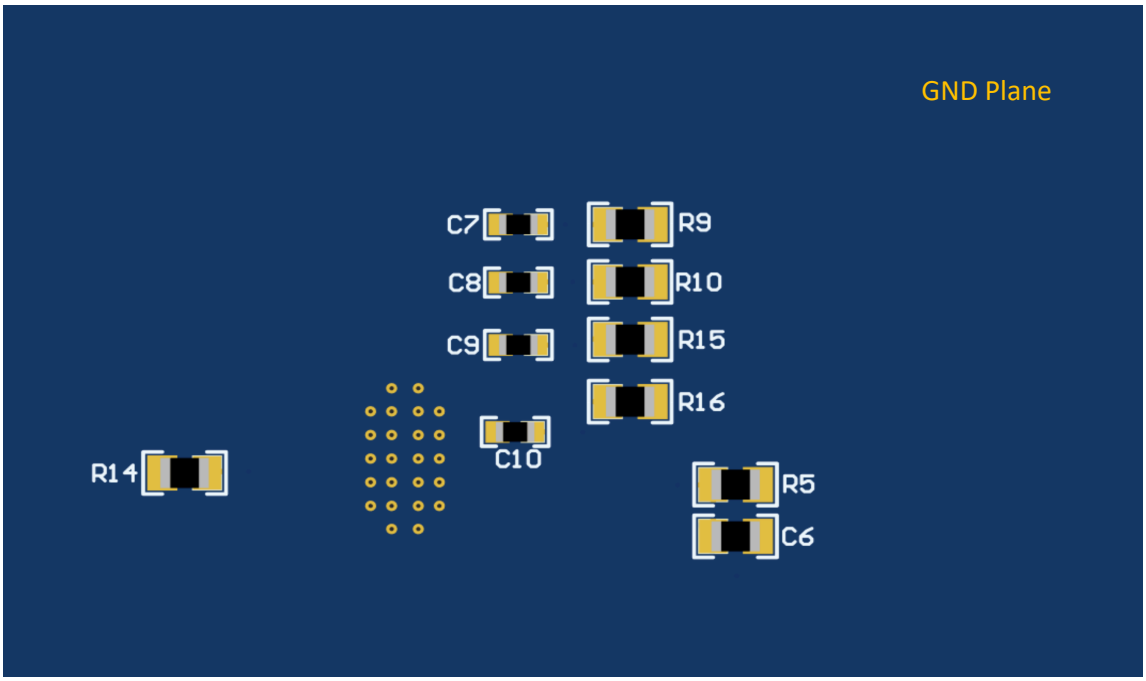


Figure 9-18. Printed Circuit Board Layout Example: Bottom Layer 3D View

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

The following related documents are available for download at www.ti.com:

- *TPS7H3014EVM-CVAL EVM User Guide*, SLVUCT9
- *TPS7H3014EVM EVM Evaluation Module (EVM) User Guide*, SLVUD73
- *TPS7H3014-SP Total Ionizing Dose (TID)*, SLVK170
- *TPS7H3014-SEP Total Ionizing Dose (TID)*, SLVK200
- *TPS7H3014-SP Neutron Displacement Damage (NDD) Characterization Report*, SLVK171
- *TPS7H3014-SEP Neutron Displacement Damage (NDD) Characterization Report*, SLVK202
- *TPS7H3014-SP Single-Event Effects (SEE) Report*, SLVK172
- *TPS7H3014-SEP Single-Event Effects (SEE) Report*, SLVK198
- Standard Microcircuit Drawing
- Vendor Item Drawing
- *Comparator with Hysteresis Reference Design*, TIDU020
- *IQ vs Accuracy Tradeoff In Designing Resistor Divider Input To A Voltage Supervisor*, SLVA450

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2025) to Revision D (July 2025)	Page
• Added comment that explains that is mandatory to connect to VLDO all channels to be disabled (or unused)	25
• Remove $\overline{\text{DOWN}}$ = Falling Edge from the faults conditions in the Start State and fix typo	37
• Fixed typo on V_{OUTx} labels	40
• Added SEP related documentation	52

Changes from Revision B (June 2024) to Revision C (April 2025)	Page
• Added the SEP orderable as product preview	3

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R2320101VXC	Active	Production	CFP (HFT) | 22	25 | TUBE	Yes	NIAU	N/A for Pkg Type	-55 to 125	5962R2320101VXC TPS7H3014MHFTV
TPS7H3014HFT/EM	Active	Production	CFP (HFT) | 22	25 | TUBE	Yes	NIAU	N/A for Pkg Type	25 to 25	TPS7H3014HFTEM EVAL ONLY
TPS7H3014MPWTSEP	Active	Production	TSSOP (PW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H3014PW
V62/25644-01XE	Active	Production	TSSOP (PW) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H3014PW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS7H3014-SEP, TPS7H3014-SP :

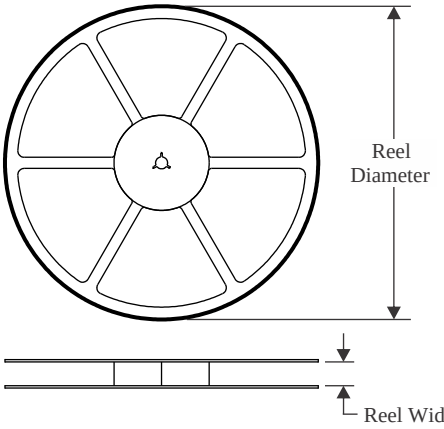
- Catalog : TPS7H3014-SEP
- Space : TPS7H3014-SP

NOTE: Qualified Version Definitions:

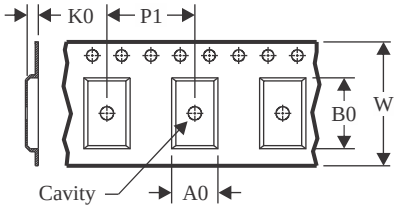
- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

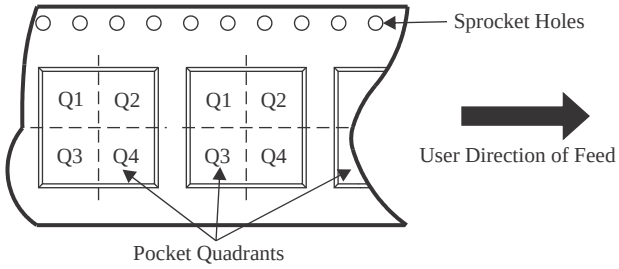


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

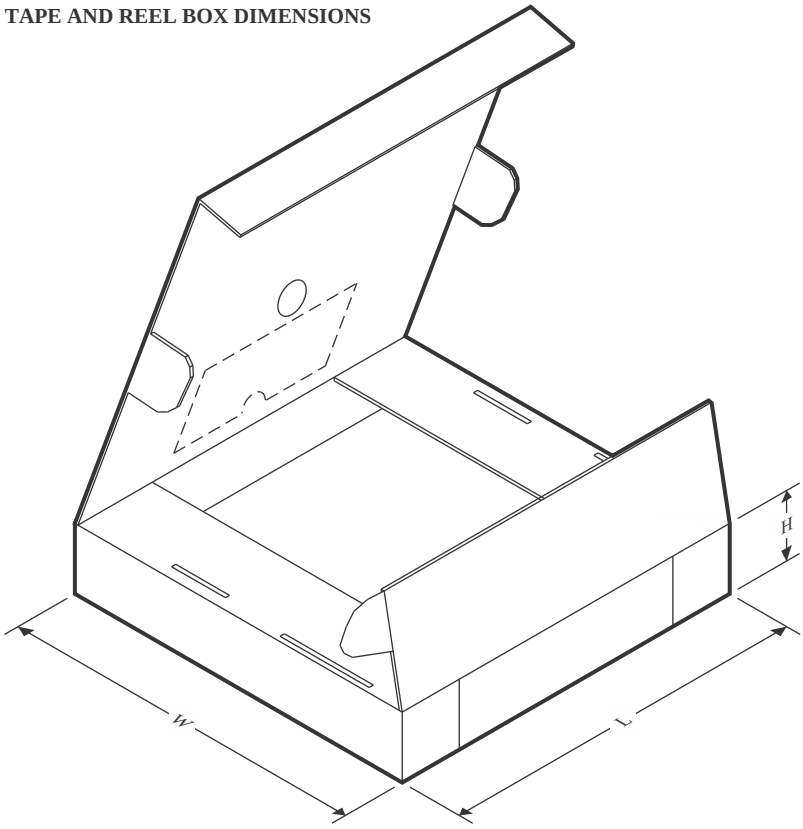
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7H3014MPWTSEP	TSSOP	PW	24	250	178.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

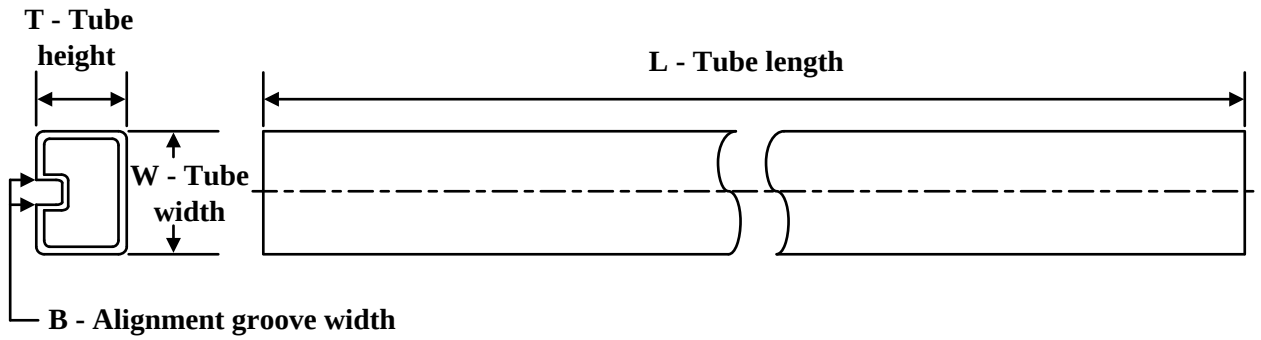
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7H3014MPWTSEP	TSSOP	PW	24	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

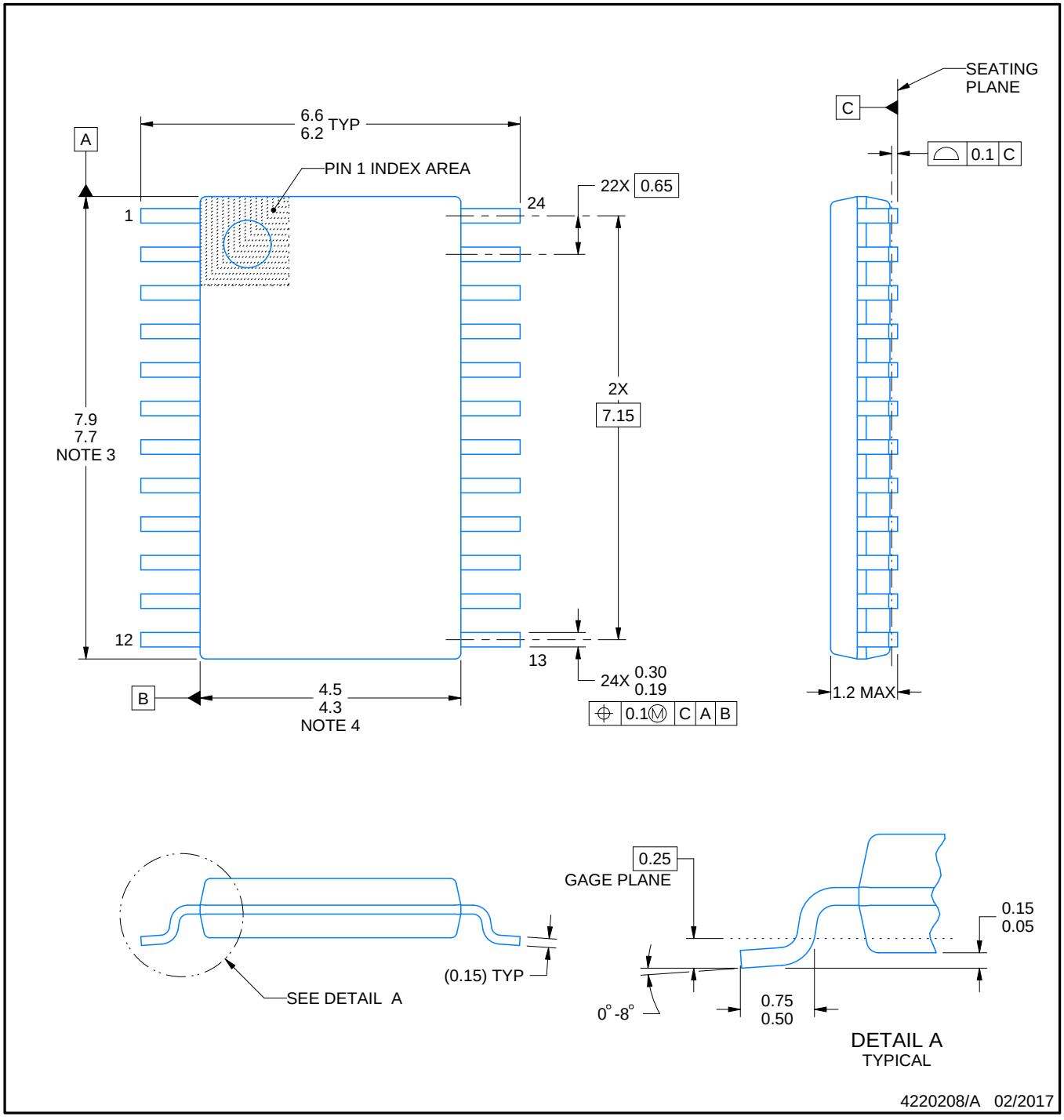
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R2320101VXC	HFT	CFP	22	25	506.98	32.77	9910	NA
TPS7H3014HFT/EM	HFT	CFP	22	25	506.98	32.77	9910	NA

PACKAGE OUTLINE

PW0024A

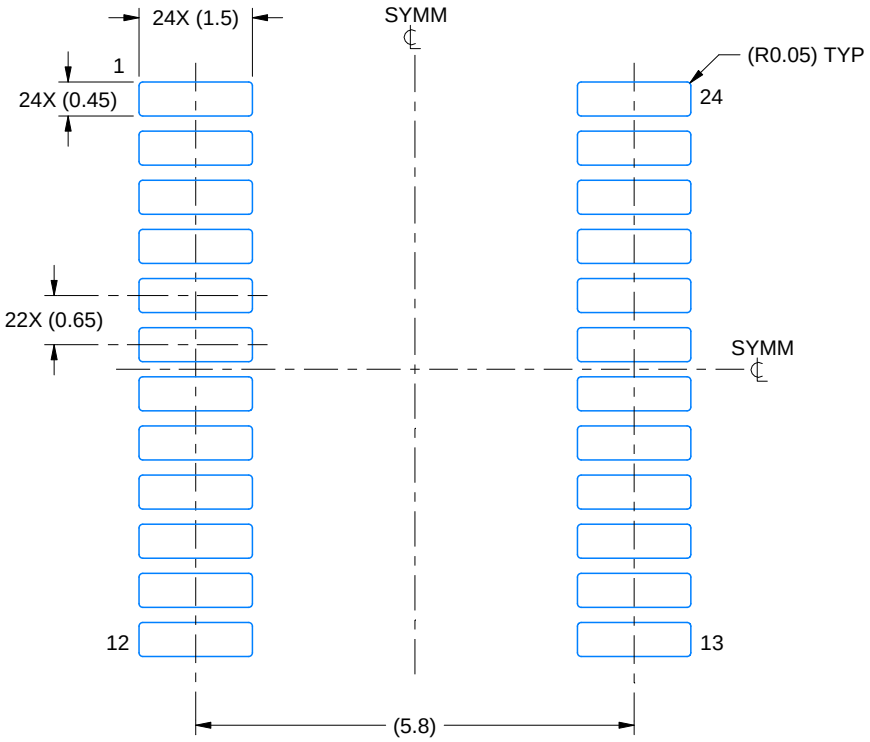
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

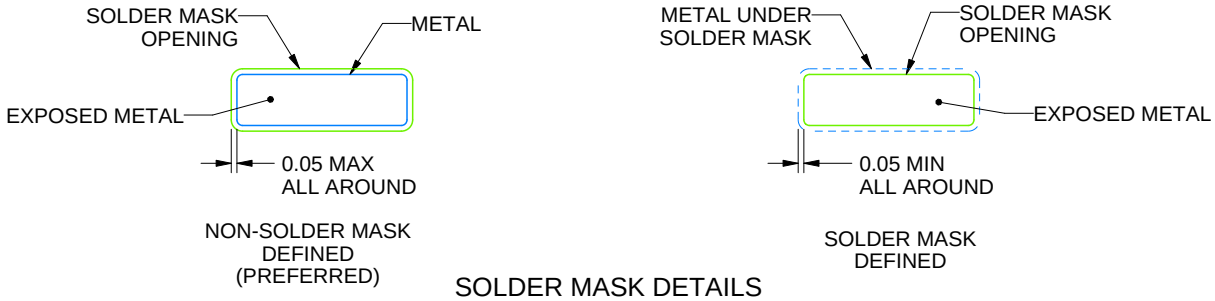


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

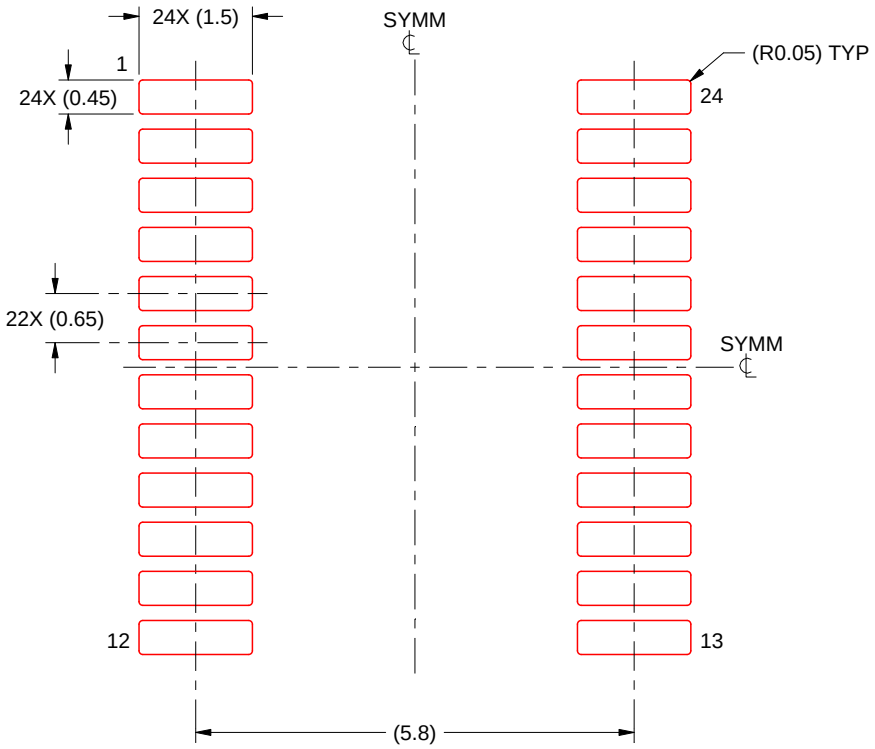


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

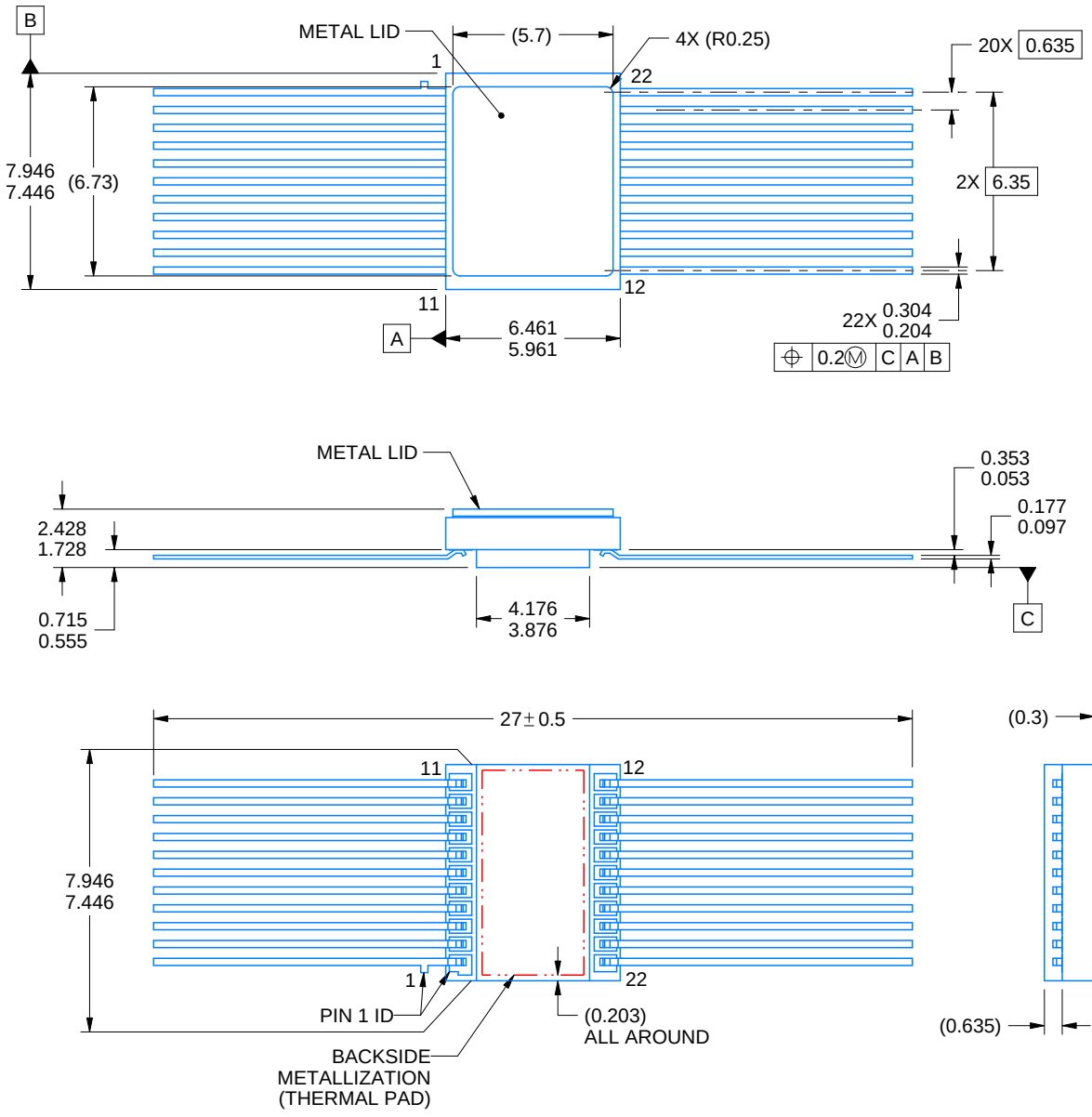
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

HFT0022A

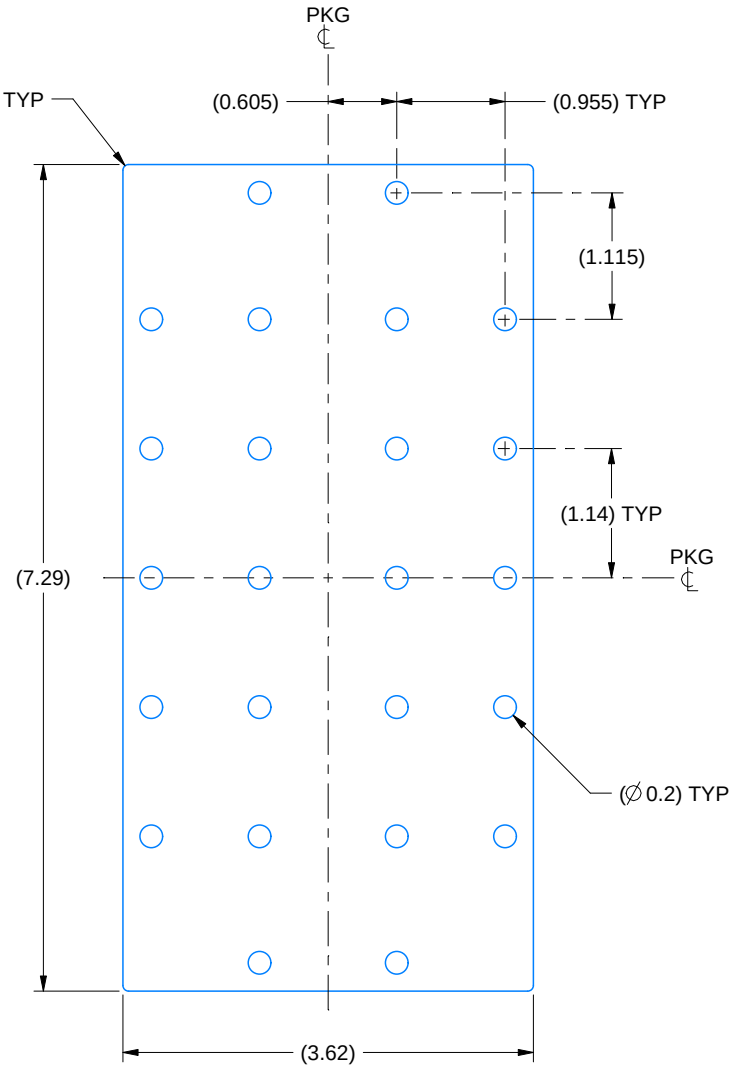
CFP - 2.428mm max height

CERAMIC FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.
5. Metal lid is connected to backside metalization



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

4225791/C 01/2021

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2186323	03/13/2020	R. RAZAK / ANIS FAUZI
B	ADD LAND PATTERN VIEW / SHEET	2190485	10/22/2020	R. RAZAK / ANIS FAUZI
C	UPDATE TOTAL LEAD LENGTH TO 27± 0.5	2192775	01/28/2021	R. RAZAK / ANIS FAUZI

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Last updated 10/2025