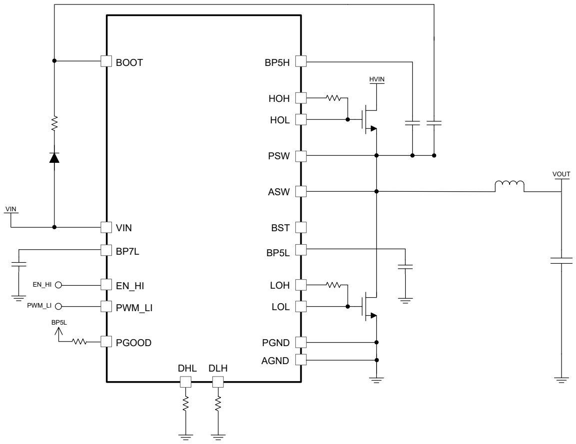
TPS7H60x5-SP and TPS7H60x5-SEP Radiation-Hardness-Assured Half Bridge GaN FET Gate Drivers

1 Features

- Radiation performance:
  - Radiation-hardness-assurance (RHA) up to total ionizing dose (TID) of 100krad(Si)
  - Single-event transient (SET), single-event burnout (SEB), and single-event gate rupture (SEGR) immune to linear energy transfer (LET) = 75MeV-cm^2/mg
  - Single-event transient (SET) and single-event functional interrupt (SEFI) characterized up to LET = 75MeV-cm^2/mg
- 1.3A peak source, 2.5A peak sink current
- Two operational modes:
  - Single PWM input with adjustable dead time
  - Two independent inputs
- Selectable input interlock protection in independent input mode
- Split outputs for adjustable turn-on and turn-off times
- 30ns typical propagation delay in independent input mode
- 5.5ns typical delay matching
- Plastic packages outgas tested per ASTM E595
- Available in military temperature range (–55°C to 125°C)

2 Applications

- Space satellite power supplies
- Motor drives
- Reaction wheels
- Communications payload
- Optical imaging payload
- Satellite electrical power system



Simplified Application Diagram

3 Description

The TPS7H60x5 series of radiation-hardness-assured (RHA) gallium nitride (GaN) field effect transistor (FET) gate drivers is designed for high frequency, high efficiency, and high current applications. The series consists of the TPS7H6005 (200V rating), the TPS7H6015 (60V rating), and the TPS7H6025 (22V rating). Each of these devices has a 56-pin HTSSOP plastic package and availability in both the QMLP and Space Enhanced Plastic (SEP) grades. The drivers feature adjustable dead time capability, small 30ns propagation delay, and 5.5ns high-side and low-side matching. These parts also include internal high-side and low-side LDOs, which ensure a drive voltage of 5V regardless of supply voltage. The TPS7H60x5 drivers all have split-gate outputs, providing flexibility to adjust the turn-on and turn-off strength of the outputs independently.

The TPS7H60x5 drivers feature two control input modes: independent input mode (IIM) and PWM mode. In IIM each of the outputs is controlled by a dedicated input. In PWM mode, two complementary outputs signals are generated from a single input and the user can adjust the dead time for each edge.

The gate drivers also offer user configurable input interlock in independent input mode as anti-shoot through protection. Input interlock disallows turn-on of both outputs when both inputs are on simultaneously. The user has the option to enable or disable this protection in independent input mode, which allows the driver to be used in a number of different converter configurations. The drivers can also be utilized for both half-bridge and dual-low side converter applications.

Device Information

PART NUMBER[1]	GRADE	BODY SIZE[2]
5962R2220104PYE	QMLP-RHA	56-pin plastic 6.1mm × 14.0mm Mass = 119mg[3]
TPS7H6005MDCATSEP	SEP	
5962R2220105PYE	QMLP-RHA	
TPS7H6015MDCATSEP	SEP	
5962R2220106PYE	QMLP-RHA	
TPS7H6025MDCATSEP	SEP	

(1) For additional information view the *Device Options* table.
(2) The body size (length × width) is a nominal value and does not include pins.
(3) Mass is a nominal value.

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4 Device Comparison Table

DEVICE	ABSOLUTE MAXIMUM VOLTAGE(1)	RECOMMENDED OPERATING VOLTAGE(1)
TPS7H6005	200V	150V
TPS7H6015	60V	45V
TPS7H6025	22V	14V

(1) This represents the "SW to GND" voltage rating of the devices as shown in the *Specifications* section.

5 Device Options Table

GENERIC PART NUMBER	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER
TPS7H6005-SP	TID up to 100krad(Si) RLAT and DSEE free up to LET = 75MeV-cm^2/mg	QMLP-RHA	56-pin TSSOP DCA	5962R2220104PYE
TPS7H6005-SEP	TID up to 50krad(Si) RLAT and DSEE free up to LET = 43MeV-cm^2/mg	Space Enhanced Plastic		TPS7H6005MDCATSEP
TPS7H6015-SP	TID up to 100krad(Si) RLAT and DSEE free up to LET = 75MeV-cm^2/mg	QMLP-RHA		5962R2220105PYE
TPS7H6015-SEP	TID up to 50krad(Si) RLAT and DSEE free up to LET = 43MeV-cm^2/mg	Space Enhanced Plastic		TPS7H6015MDCATSEP
TPS7H6025-SP	TID up to 100krad(Si) RLAT and DSEE free up to LET = 75MeV-cm^2/mg	QMLP-RHA		5962R2220106PYE
TPS7H6025-SEP	TID up to 50krad(Si) RLAT and DSEE free up to LET = 43MeV-cm^2/mg	Space Enhanced Plastic		TPS7H6025MDCATSEP

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID and SEE radiation reports for the device.
(2) For additional information about part grade, view SLYB235.

6 Pin Configuration and Functions

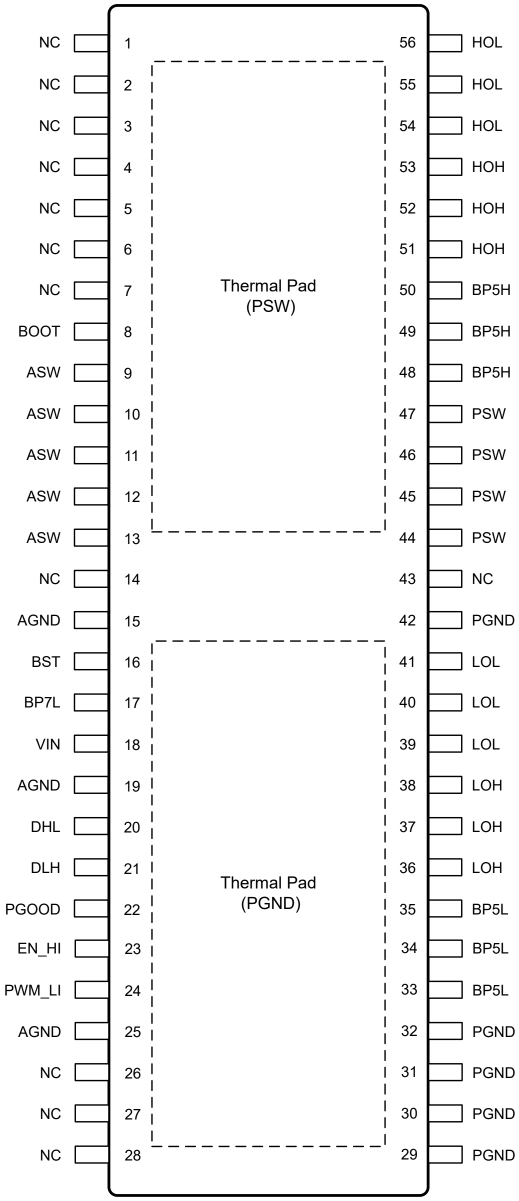


Figure 6-1. DCA Package
56-Pin TSSOP
(Top View)

Table 6-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NUMBER	NAME		
8	BOOT	I	Input voltage supply of the high-side linear regulator. The external bootstrap capacitor is placed between BOOT and ASW. The cathode of the external bootstrap diode is connected to this pin. A Zener diode clamp may be needed between BOOT and ASW in order to not exceed the absolute maximum electrical rating.
9–13	ASW	—	High-side driver signal return. ASW(9) is internally connected to PSW and the high-side thermal pad. Connect ASW(10-13) to ASW externally.

Table 6-1. Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NUMBER	NAME		
16	BST	O	For bootstrap charging that utilizes the internal bootstrap switch, this pin serves as the bootstrap diode anode connection point. The external high-side bootstrap capacitor can be charged through this pin using the input voltage applied to VIN, internal bootstrap switch, and external bootstrap diode(s).
17	BP7L	O	Low-side 7V linear regulator output. A minimum of 1µF capacitance is required from BP7L to AGND.
18	VIN	I	Gate driver input voltage supply. Input voltage range is from 10V to 14V. This pin serves as the input to the low-side linear regulators and the internal bootstrap switch. For bootstrap charging directly from the input voltage, VIN also serves as the bootstrap diode anode connection point.
15, 19, 25	AGND	—	Low-side driver signal return. AGND(15) and AGND(19) are internally connected to PGND and the low-side thermal pad. Connect AGND(25) to AGND externally.
20	DHL	I	High-side to low-side dead time set. In PWM mode, a resistor from DHL to AGND sets the dead time between the high-side turn-off and low-side turn-on. In independent input mode (IIM), DHL is used to configure the input interlock protection of the driver. DHL is connected to BP5L in IIM with interlock enabled. A resistor valued between 100kΩ and 220kΩ is connected from DHL to AGND for IIM with interlock disabled.
21	DLH	I	Low-side to high-side dead time set. In PWM mode, a resistor from DLH to AGND sets the dead time between the low-side turn-off and high-side turn-on. In independent input mode (IIM), DLH is used to configure the input interlock protection of the driver. A resistor valued between 100kΩ and 220kΩ is connected from DLH to AGND for IIM with interlock enabled. DLH is connected to BP5L in IIM with interlock disabled.
22	PGOOD	O	Power good pin. Asserts low when any of the low-side internal linear regulators or VIN goes into undervoltage lockout. Requires a 10kΩ pull-up resistor to BP5L.
23	EN_HI	I	Enable input or high-side driver control input. In PWM mode this is used as an enable pin. In independent input mode (IIM) this serves as the control input for the high-side driver.
24	PWM_LI	I	PWM input or low-side driver control input. In PWM mode this is used as the PWM input to the gate driver. In independent input mode (IIM) this serves as the control input for the low-side driver.
29–32, 42	PGND	—	Low-side power ground. Connect to the source of the low-side GaN FET. Internally connected to AGND and low-side thermal pad. Connect to AGND at printed circuit board level.
33–35	BP5L	O	Low-side 5V linear regulator output. A minimum of 1µF capacitance is required from BP5L to PGND.
36–38	LOH	O	Low-side driver source current output. Connect to the gate of low-side GaN FET with short, low inductance path. A resistor between LOH and the gate of the GaN FET can be used to adjust the turn-on speed.
39–41	LOL	O	Low-side driver sink current output. Connect to the gate of the low-side GaN FET with short, low inductance path. A resistor between LOL and the gate of the GaN FET can be used to adjust the turn-off speed.
44–47	PSW	—	Switch node connection. Connect to the source of the high-side GaN FET. Internally connected to ASW and high-side thermal pad. Connect to ASW at printed circuit board level.
48–50	BP5H	O	High-side 5V linear regulator output. A minimum of 1µF capacitance is required from BP5H to PSW.
51–53	HOH	O	High-side driver source current output. Connect to the gate of the high-side GaN FET with short, low inductance path. A resistor between HOH and the gate of the GaN FET can be used to adjust the turn-on speed.
54–56	HOL	O	High-side driver sink current output. Connect to the gate of the high-side GaN FET with short, low inductance path. A resistor between HOL and the gate of the GaN FET can be used to adjust the turn-off speed.

Table 6-1. Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NUMBER	NAME		
1–7, 14, 26–28, 43	NC	—	No connect. These pins are not connected internally. Pins 1-7 and 26-28 can be left unconnected or connected to the respective reference voltage (ASW or AGND) in order to avoid floating metal and prevent charge buildup. For pins 14 and 43, these are recommended to be left unconnected in order to meet the requirements of IEC-60664 for creepage and clearance. Ultimately, the connections of pins 14 and 43 are left to the discretion of the user based on the specific creepage and clearance guidelines that are selected for the design.
—	PSW PAD	—	High-side thermal pad. Internally connected to ASW(9) and PSW. Should be connected to ASW pins.
—	PGND PAD	—	Low-side thermal pad. Internally connected to AGND(15), AGND(19) and PGND. Should be connected to AGND pins.

(1) I = Input, O = Output, I/O = Input or Output, — = Other

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature (unless otherwise noted)(1)

	MIN	MAX	UNIT
VIN to AGND	–0.3	16	V
BP7L to AGND	–0.3	8	V
BP5L to AGND	–0.3	7	V
BP5H to SW	–0.3	7	V
BOOT to SW	–0.3	V_{SW} + 16	V
EN_HI	–0.3	16	V
PWM_LI	–0.3	16	V
DHL, DLH	–0.3	V_{BP5L} + 0.3	V
LOH, LOL	–0.3	V_{BP5L} + 0.3	V
HOH, HOL	V_{SW} – 0.3	V_{BP5H} + 0.3	V
PGOOD	–0.3	V_{BP5L} + 0.3	V
SW to AGND (TPS7H6005)	–10	200	V
SW to AGND (TPS7H6015)	–10	60	V
SW to AGND (TPS7H6025)	–10	22	V
BOOT to AGND (TPS7H6005)	0	216	V
BOOT to AGND (TPS7H6015)	0	76	V
BOOT to AGND (TPS7H6025)	0	38	V
BST to AGND	–0.3	16	V
BST current (3µs transient pulse, non-repetitive)		4	A
Junction temperature, T_J	–55	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
VIN to AGND	10		14	V
EN_HI	0		14	V
PWM_LI	0		14	V
BOOT to SW	V_{SW} + 8		V_{SW} + 14	V
SW (TPS7H6005)	–10		150	V
SW (TPS7H6015)	–10		45	V
SW (TPS7H6025)	–10		14	V
SW slew rate			100	V/ns
VIN slew rate			0.03	V/µs
PWM_LI, EN_HI slew rate	2			V/µs
Operating junction temperature	–55		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS7H60x5	UNIT
		HTSSOP	
		56 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	5.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

Specifications are over ambient temperature operating range T_A = –55°C to 125°C, VIN = 10V to 14V, V_{BP5L} = V_{BP5H} = 5V, and no load on LOH, LOL, HOH, and HOL (unless otherwise noted).

PARAMETER		TEST CONDITIONS		SUBGROUP[1]	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS								
I_{QLS}	Low-side quiescent current	VIN = 12V, BOOT = 10V	MODE = PWM, EN = 0V	1, 2, 3		5	6.8	mA
			MODE = IIM, LI = HI = 0V	1, 2, 3		5	8	
I_{QHS}	High-side quiescent current	VIN = 12V, BOOT = 10V	MODE = PWM, EN = 0V	1, 2, 3		4	6.3	mA
			MODE = IIM, LI = HI = 0V	1, 2, 3		4	6.3	
I_{QBG}	BOOT to AGND quiescent current (TPS7H6005)	SW = 100V, BOOT = 110V				20		µA
I_{QBG}	BOOT to AGND quiescent current (TPS7H6015)	SW = 28V, BOOT = 38V				15		µA
I_{QBG}	BOOT to AGND quiescent current (TPS7H6025)	SW = 12V, BOOT = 22V				10		µA
I_{OP_BG}	BOOT to AGND operating current (TPS7H6005)	SW = 100V, BOOT = 110V				20		µA
I_{OP_BG}	BOOT to AGND operating current (TPS7H6015)	SW = 28V, BOOT = 38V				15		µA
I_{OP_BG}	BOOT to AGND operating current (TPS7H6025)	SW = 12V, BOOT = 22V				10		µA
I_{OP_LS}	Low-side operating current	MODE = PWM, no load for LOL and LOH	f = 500kHz	1, 2, 3		6	9	mA
			f = 1MHz	1, 2, 3		8	11	
			f = 2MHz	1, 2, 3		12	16	
			f = 5MHz	1, 2, 3		20	30	
		MODE = IIM, no load for LOL and LOH	f = 500kHz	1, 2, 3		6	9	
			f = 1MHz	1, 2, 3		8	12	
			f = 2MHz	1, 2, 3		11	17	
			f = 5MHz	1, 2, 3		20	30	
I_{OP_HS}	High-side operating current	MODE = PWM, no load for HOL and HOH	f = 500kHz	1, 2, 3		5	6.5	mA
			f = 1MHz	1, 2, 3		5.3	8	
			f = 2MHz	1, 2, 3		7	10.5	
			f = 5MHz	1, 2, 3		13	19	
		MODE = IIM, no load for HOL and HOH	f = 500kHz	1, 2, 3		4.5	6.5	
			f = 1MHz	1, 2, 3		5.3	8	
			f = 2MHz	1, 2, 3		7	10.5	
			f = 5MHz	1, 2, 3		11.7	15	
LOW-SIDE TO HIGH-SIDE CAPACITANCE								
	Low-side to high-side capacitance	Low-side pins shorted together and high-side pins shorted together				6		pF
GATE DRIVER								
V_{OL}	Low-level output voltage	I_{OL} = 100mA		1, 2, 3		0.07	0.15	V
BP5x – V_{OH}	High-level output voltage	I_{OH} = 100mA		1, 2, 3		0.13	0.3	V
I_{OH}	Peak source current	HOH, LOH = 0V, BP5x = 5V		1, 2, 3	0.7	1.3	2.3	A
I_{OL}	Peak sink current	HOL, LOL = 5V, BP5x = 5V		1, 2, 3	1.6	2.5	4.6	A
INTERNAL REGULATORS								
V_{BP5L}	Low-side 5V regulator output voltage	C_{BP5L} = 1µF		1, 2, 3	4.75	5.0	5.175	V
	Required BP5L output capacitor [2]			1, 2, 3	1			µF
V_{BP5H}	High-side 5V regulator output voltage	C_{BP5H} = 1µF		1, 2, 3	4.75	5.0	5.175	V
	Required BP5H output capacitor [2]				1			µF

7.5 Electrical Characteristics (continued)

Specifications are over ambient temperature operating range T_A = –55°C to 125°C, VIN = 10V to 14V, $V_{BP5L} = V_{BP5H}$ = 5V, and no load on LOH, LOL, HOH, and HOL (unless otherwise noted).

PARAMETER		TEST CONDITIONS		SUBGROUP(1)	MIN	TYP	MAX	UNIT
V_{BP7L}	7V regulator output voltage			1, 2, 3	6.65	7	7.35	V
	Required BP7L output capacitor (2)				1			µF
UNDERVOLTAGE PROTECTION								
$BP5H_R$	BP5H UVLO rising threshold	C_{BP5H} = 1µF		1, 2, 3	4.0	4.25	4.5	V
$BP5H_F$	BP5H UVLO falling threshold	C_{BP5H} = 1µF		1, 2, 3	3.8	4.05	4.3	V
$BP5H_H$	BP5H UVLO hysteresis	C_{BP5H} = 1µF				0.2		V
$BP5L_R$	BP5L UVLO rising threshold	C_{BP5L} = 1µF		1, 2, 3	4.0	4.25	4.5	V
$BP5L_F$	BP5L UVLO falling threshold	C_{BP5L} = 1µF		1, 2, 3	3.8	4.05	4.3	V
$BP5L_H$	BP5L UVLO hysteresis	C_{BP5L} = 1µF				0.2		V
$BP7L_R$	BP7L UVLO rising threshold	C_{BP7L} = 1µF		1, 2, 3	6.2	6.5	6.8	V
$BP7L_F$	BP7L UVLO falling threshold	C_{BP7L} = 1µF		1, 2, 3	5.9	6.2	6.5	V
$BP7L_H$	BP7L UVLO hysteresis	C_{BP7L} = 1µF				0.3		V
VIN_R	VIN UVLO rising threshold			1, 2, 3	8.0	8.6	9.0	V
VIN_F	VIN UVLO falling threshold			1, 2, 3	7.5	8.1	8.5	V
VIN_H	VIN UVLO hysteresis					0.5		V
$BOOT_R$	BOOT UVLO rising threshold			1, 2, 3	6.6	7.1	7.4	V
$BOOT_F$	BOOT UVLO falling threshold			1, 2, 3	6.2	6.65	7	V
$BOOT_H$	BOOT UVLO hysteresis					0.45		V
INPUT PINS								
V_{IR}	Input rising edge threshold			1, 2, 3	1.80		2.65	V
V_{IF}	Input falling edge threshold			1, 2, 3	1.15		1.85	V
V_{IHYS}	Input hysteresis					0.8		V
R_{PD}	Input pull-down resistance	V = 2.15V applied at input (EN_HI or PWM_LI)		1, 2, 3	100		400	kΩ
PROGRAMMBLE DEAD TIME								
T_{DLH}	LO off to HO on dead time	MODE = PWM, LO falling to HO rising (90% to 10%), f ≤ 2MHz	RLH = 3.32kΩ	9, 10 , 11	0	4.5	10	ns
			RLH = 11.8kΩ	9, 10 , 11	8	12	15.5	
			RLH = 21kΩ	9, 10 , 11	15.5	21	24	
			RLH = 52.3kΩ	9, 10 , 11	36	50	59	
			RLH = 105kΩ	9, 10 , 11	74	97	113.5	
T_{DHL}	HO off to LO on dead time	MODE = PWM, HO falling to LO rising (90% to 10%), f ≤ 2MHz	RHL = 7.87kΩ	9, 10 , 11	0	5	10	ns
			RHL = 13.3kΩ	9, 10 , 11	6	10.5	15	
			RHL = 23.7kΩ	9, 10 , 11	16	21	24.5	
			RHL = 57.6kΩ	9, 10 , 11	44	53	61	
			RHL = 113kΩ	9, 10 , 11	81	105	125	
BOOTSTRAP DIODE SWITCH								
R_{BST_SW}	Bootstrap diode switch resistance	I_{BST_SW} = 100mA		1, 2, 3		0.43		Ω
	Bootstrap diode switch parallel resistance	I_{BST_RP} = 1mA		1, 2, 3	0.8	1	1.2	kΩ
POWER GOOD								
	Logic-low output	I_{FLT} = 1mA		1, 2, 3			0.4	V
	PGOOD internal resistance	BP5L = 5V, BP7L = 7V, VIN = 12V		1, 2, 3	0.7	1	1.9	MΩ
	Minimum BP5L voltage for valid PGOOD output			1, 2, 3		2	2.85	V

(1) Subgroups are applicable for QML parts. For subgroup definitions, see *Quality Conformance Inspection*.
(2) Specified by design; not tested in production.

7.6 Switching Characteristics

Specifications are over ambient temperature operating range T_A = –55°C to 125°C, VIN = 10V to 14V, V_{BP5L} = V_{BP5H} = 5V, and no load on LOH, LOL, HOH, and HOL (unless otherwise noted).

PARAMETER		TEST CONDITIONS		SUBGROUP[1]	MIN	TYP	MAX	UNIT
t_{LPHL}	LO turnoff propagation delay	MODE = PWM	PWM rising to LOL falling	9, 10, 11		30	48	ns
		MODE = IIM	LI falling to LOL falling	9, 10, 11		27	38	
t_{LPLH}	LO turnon propagation delay	MODE = IIM	LI rising to LOH rising	9, 10, 11		24	38	ns
t_{HPHL}	HO turnoff propagation delay	MODE = PWM	PWM falling to HOL falling	9, 10, 11		35	50	ns
		MODE = IIM	HI falling to HOL falling	9, 10, 11		30	40	
t_{HPLH}	HO turnon propagation delay	MODE = IIM	HI rising to HOH rising	9, 10, 11		26	40	ns
t_{MON}	Delay matching LO on and HO off[3]	MODE = IIM		9, 10, 11		5.5	12	ns
t_{MOFF}	Delay matching LO off and HO on[3]	MODE = IIM		9, 10, 11		1.5	4	ns
t_{HRC}	HO rise time	C_L = 1000pF	10% to 90%	9, 10, 11		3.5	7.5	ns
t_{LRC}	LO rise time		10% to 90%	9, 10, 11		3	7.5	
t_{HFC}	HO fall time		90% to 10%	9, 10, 11		4	5.5	
t_{LFC}	LO fall time		90% to 10%	9, 10, 11		3	5.5	
t_{PW_IIM}	Minimum input pulse width (turn-on)	MODE = IIM		9, 10, 11		5	8	ns
$t_{PW\_IIM\_OFF}$	Minimum input pulse width (turn-off)	MODE = IIM		9, 10, 11		8	12	ns
t_{PW_PWM}	Minimum required input pulse width for targeted dead time [2]	MODE = PWM, DT reduction ≤ 2ns	RLH = 11.9kΩ, RHL = 13.3kΩ			22		ns
		MODE = PWM, DT reduction ≤ 3ns	RLH = 21 kΩ, RHL = 23.7kΩ			30		

(1) Subgroups are applicable for QML parts. For subgroup definitions, see the Quality Conformance Inspection table.
(2) Specified by design; not tested in production.
(3) Specification limits for this parameter are represented as an absolute value.

7.7 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

7.8 Typical Characteristics

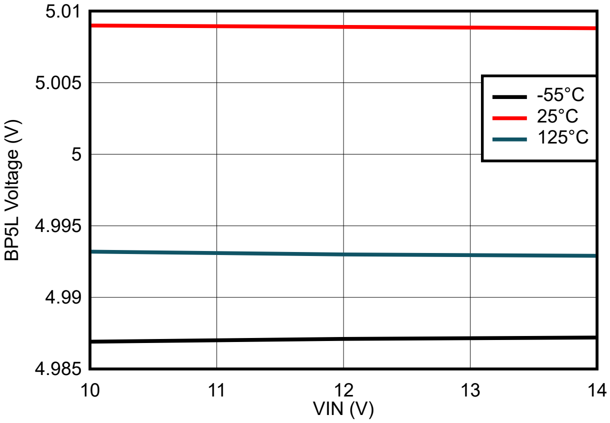


Figure 7-1. BP5L Output Voltage vs VIN Voltage

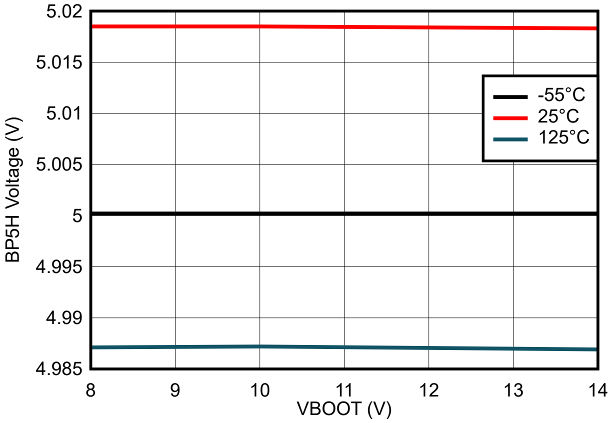


Figure 7-2. BP5H Output Voltage vs BOOT Voltage

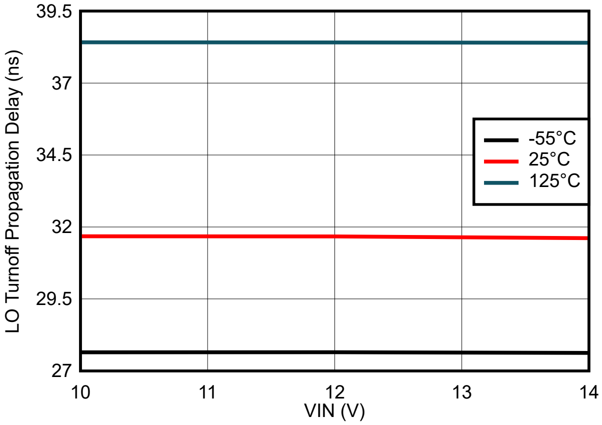


Figure 7-3. LO Turnoff Propagation Delay vs VIN Voltage (PWM)

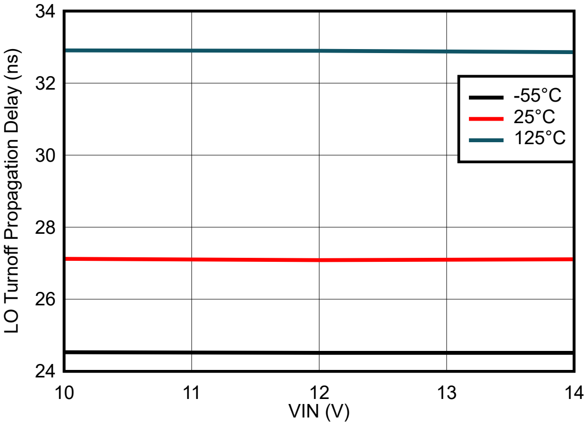


Figure 7-4. LO Turnoff Propagation Delay vs VIN Voltage (IIM)

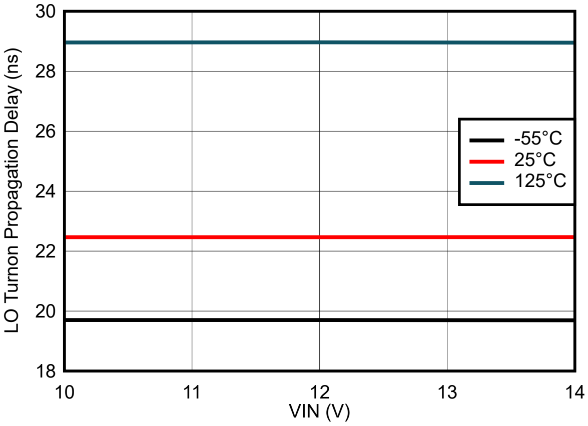


Figure 7-5. LO Turnon Propagation Delay vs VIN Voltage (IIM)

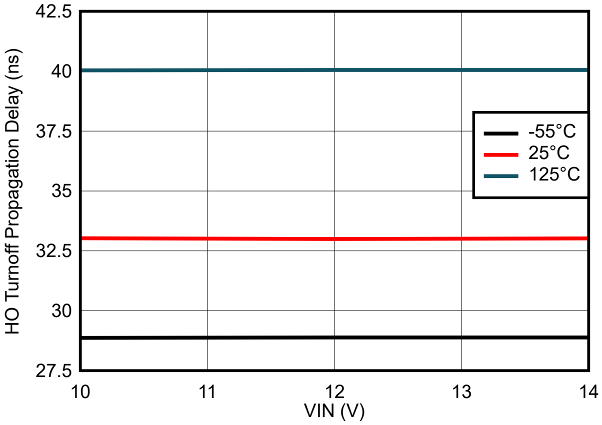


Figure 7-6. HO Turnoff Propagation Delay vs VIN Voltage (PWM)

7.8 Typical Characteristics (continued)

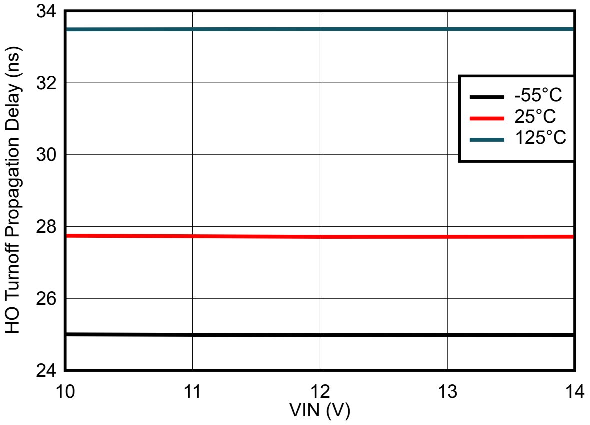


Figure 7-7. HO Turnoff Propagation Delay vs VIN Voltage (IIM)

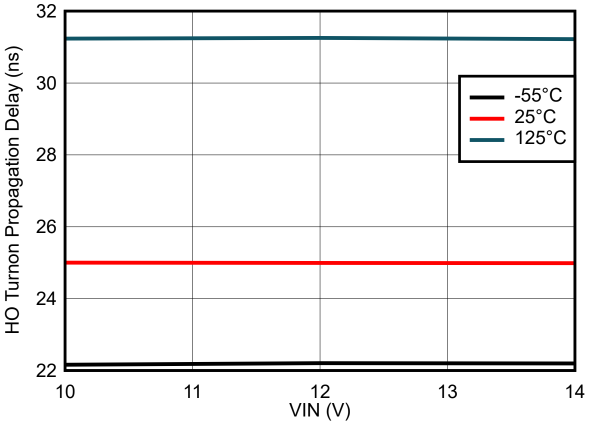


Figure 7-8. HO Turnon Propagation Delay vs VIN Voltage (IIM)

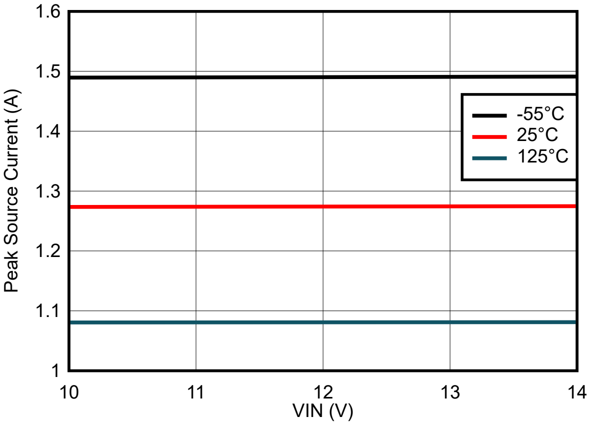


Figure 7-9. Peak Source Current vs VIN Voltage

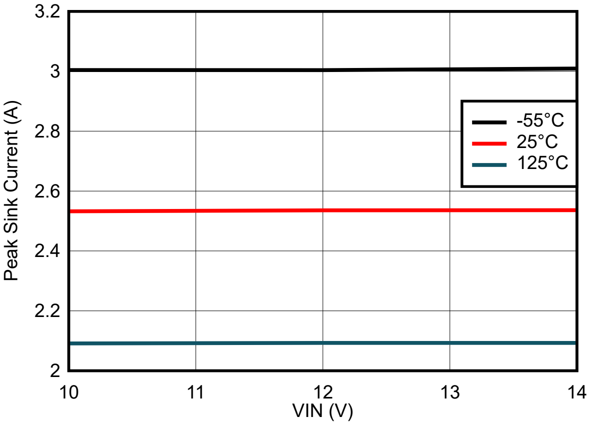


Figure 7-10. Peak Sink Current vs VIN Voltage

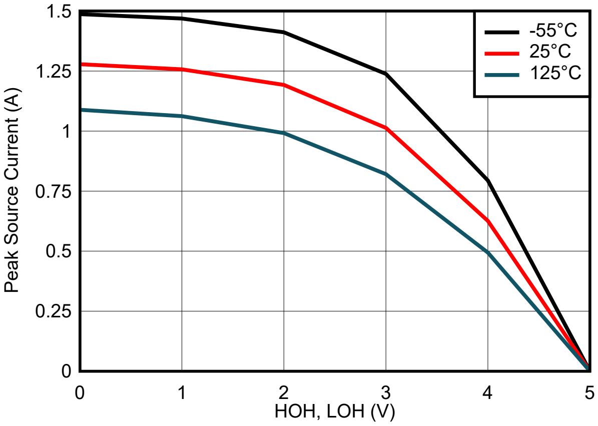


Figure 7-11. Peak Source Current vs Output Voltage

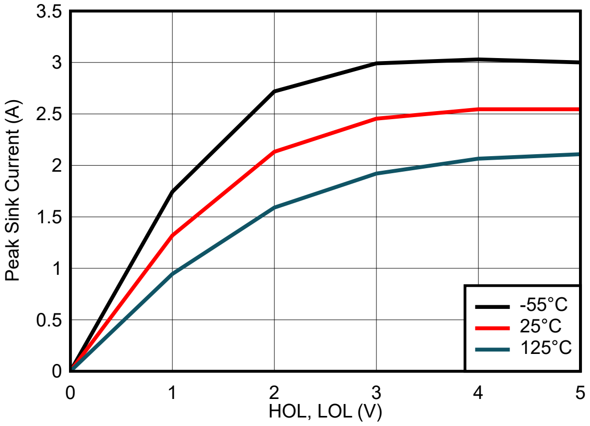


Figure 7-12. Peak Sink Current vs Output Voltage

7.8 Typical Characteristics (continued)

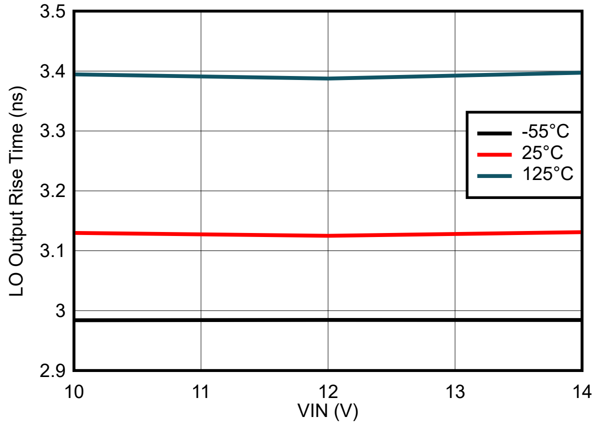


Figure 7-13. LO Output Rise Time vs VIN Voltage

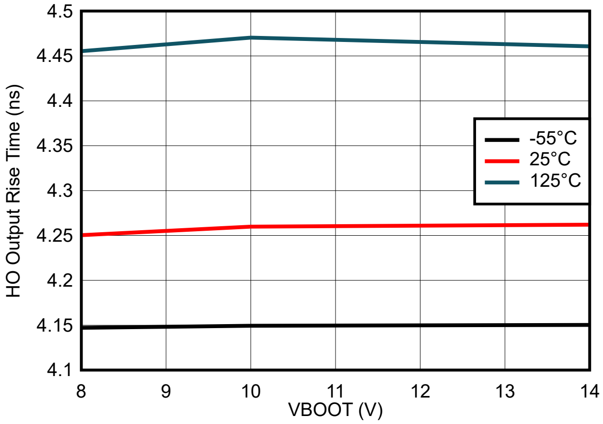


Figure 7-14. HO Output Rise Time vs BOOT Voltage

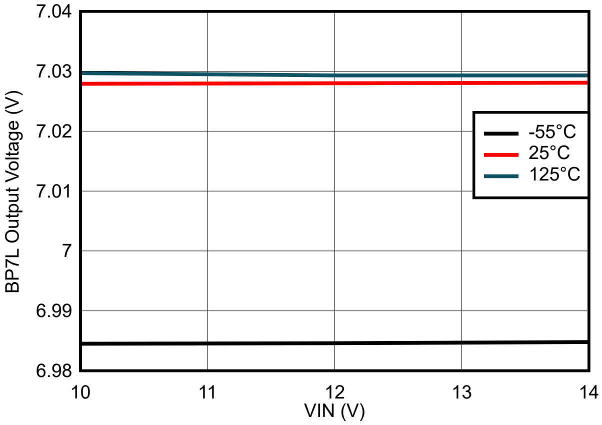


Figure 7-15. BP7L Output Voltage vs VIN Voltage

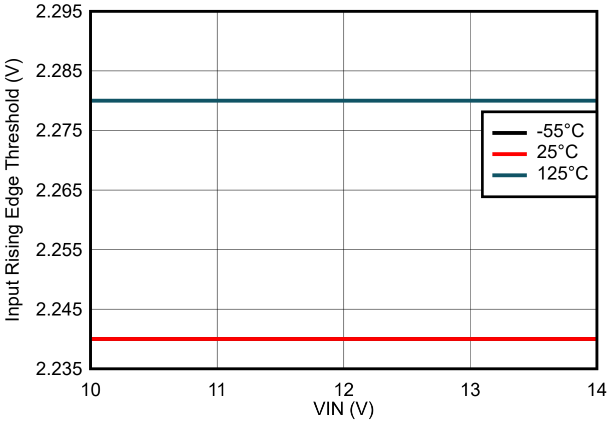


Figure 7-16. Input Rising Edge Threshold vs VIN Voltage

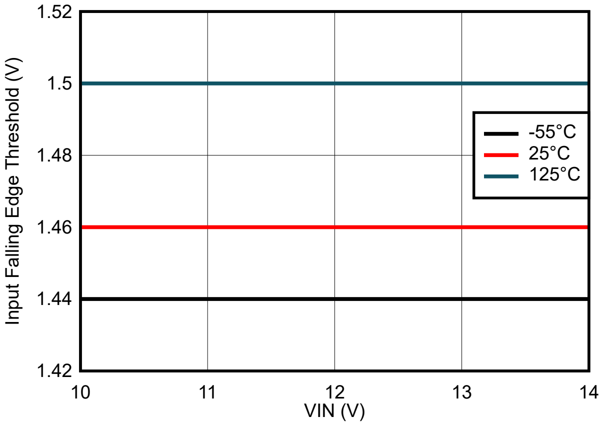


Figure 7-17. Input Falling Edge Threshold vs VIN Voltage

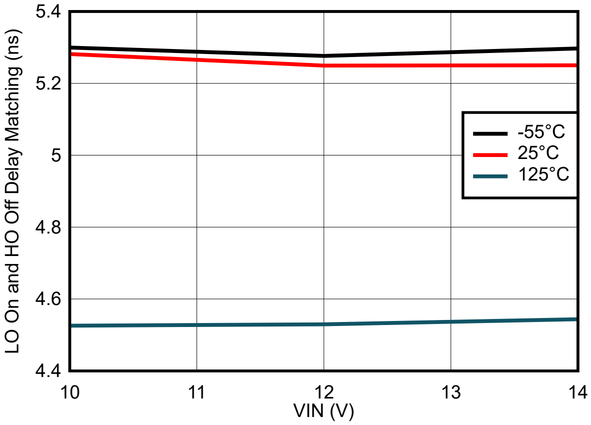


Figure 7-18. LO On and HO Off Delay Matching vs VIN Voltage

7.8 Typical Characteristics (continued)

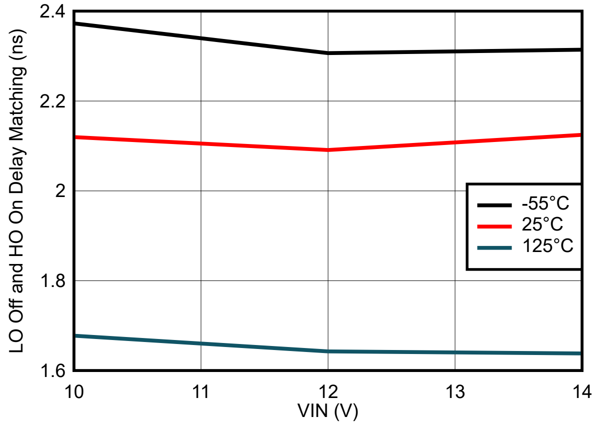


Figure 7-19. LO Off and HO On Delay Matching vs VIN Voltage

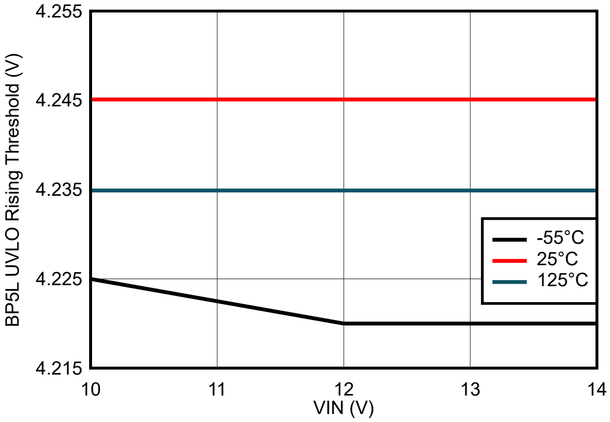


Figure 7-20. BP5L UVLO Rising Threshold vs VIN Voltage

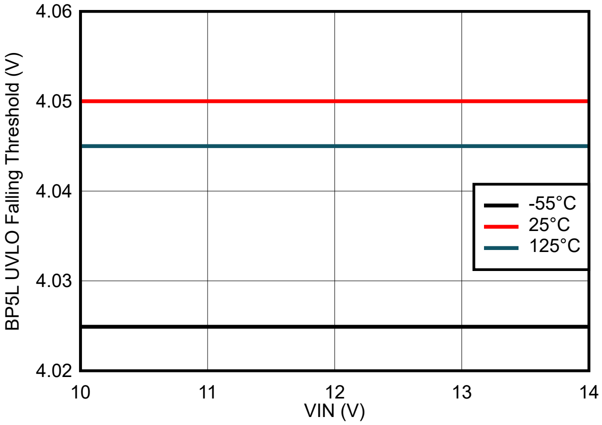


Figure 7-21. BP5L UVLO Falling Threshold vs VIN Voltage

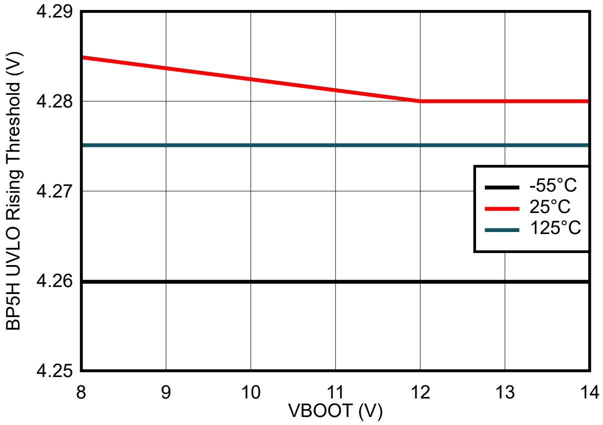


Figure 7-22. BP5H UVLO Rising Threshold vs BOOT Voltage

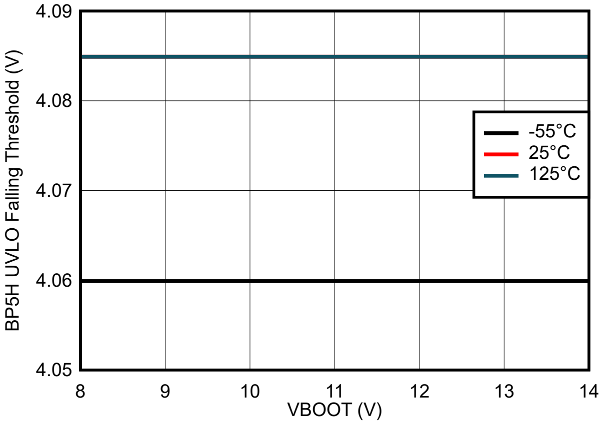


Figure 7-23. BP5H UVLO Falling Threshold vs BOOT Voltage

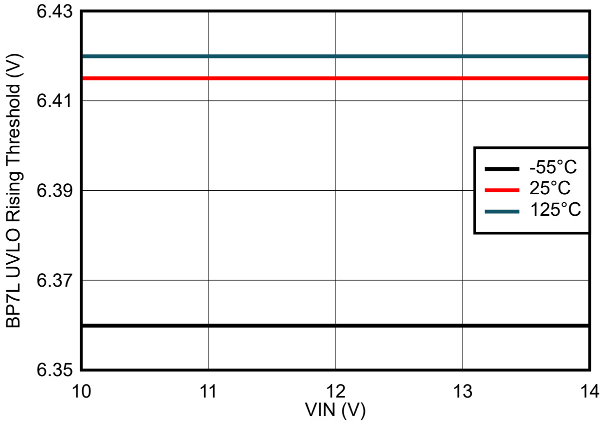


Figure 7-24. BP7L UVLO Rising Threshold vs VIN Voltage

7.8 Typical Characteristics (continued)

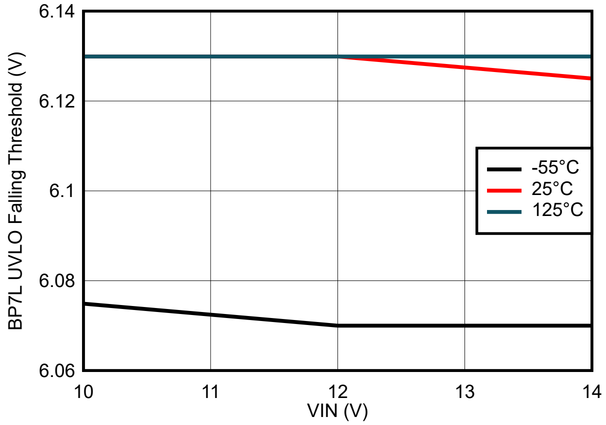


Figure 7-25. BP7L UVLO Falling Threshold vs VIN Voltage

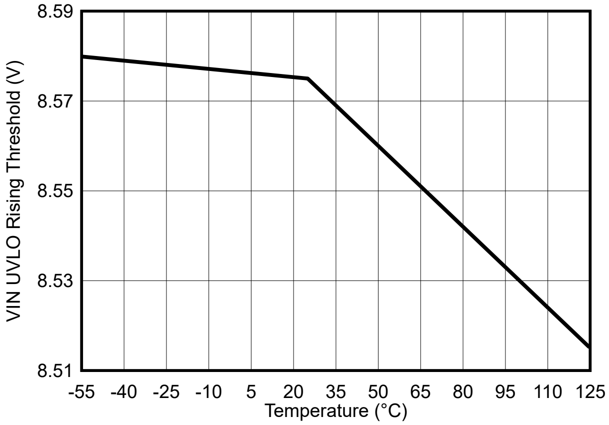


Figure 7-26. VIN UVLO Rising Threshold vs Temperature

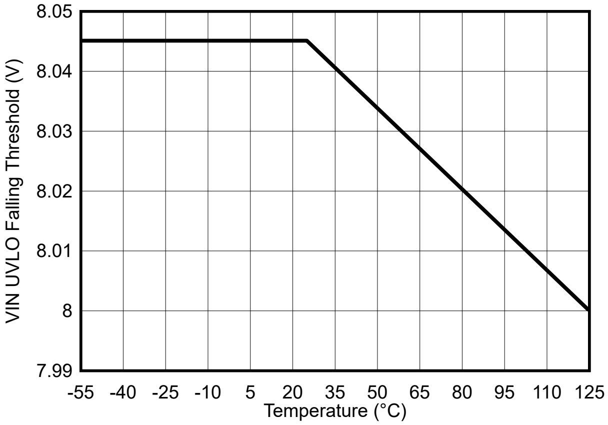


Figure 7-27. VIN UVLO Falling Threshold vs Temperature

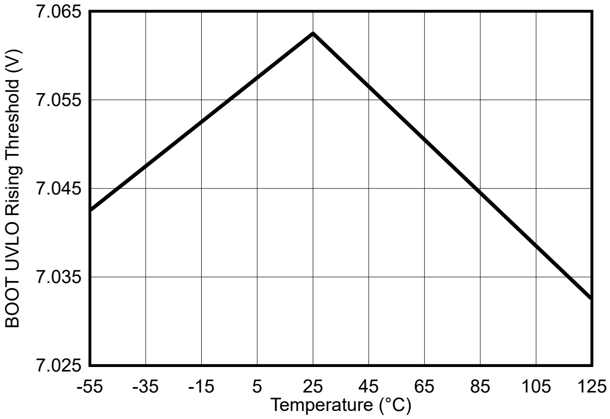


Figure 7-28. BOOT UVLO Rising Threshold vs Temperature

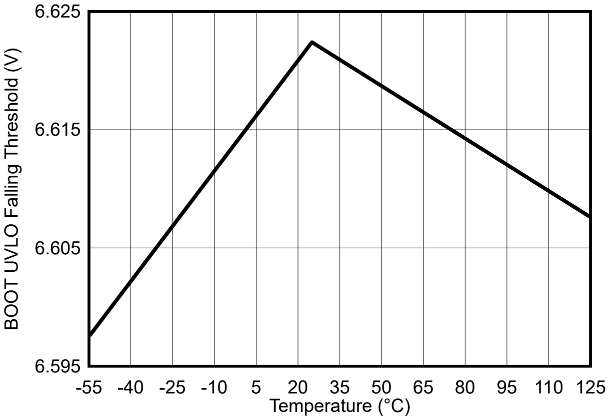
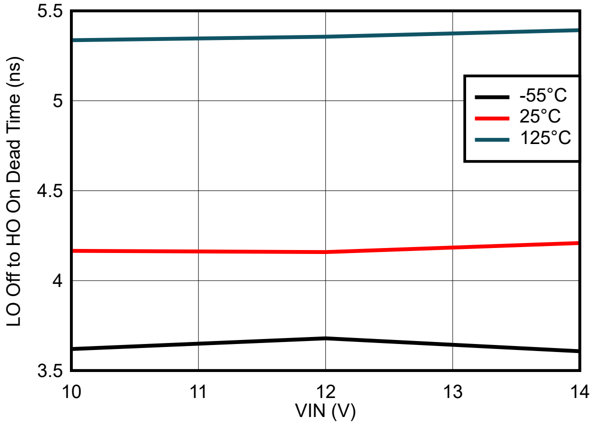


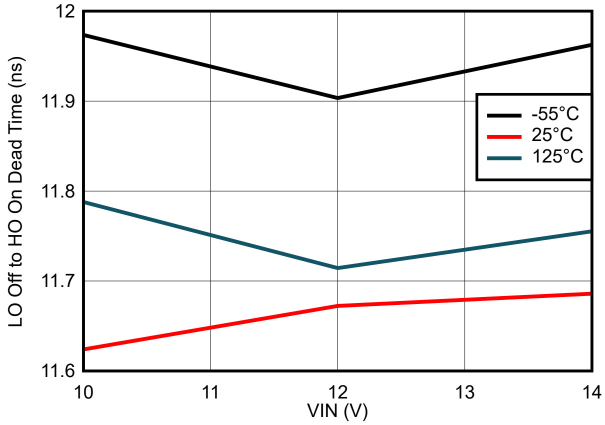
Figure 7-29. BOOT UVLO Falling Threshold vs Temperature



RLH = 3.32kΩ

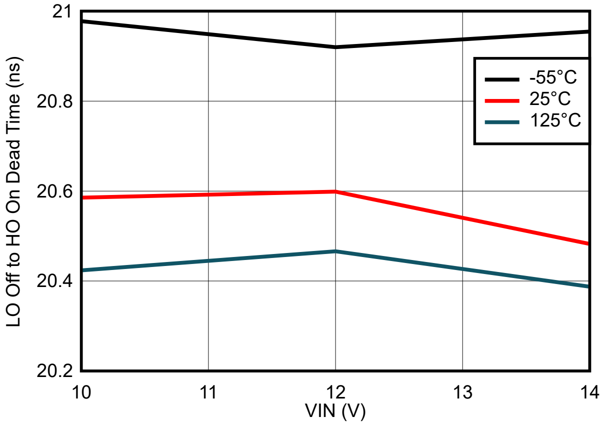
Figure 7-30. LO Off to HO On Dead Time vs VIN Voltage

7.8 Typical Characteristics (continued)



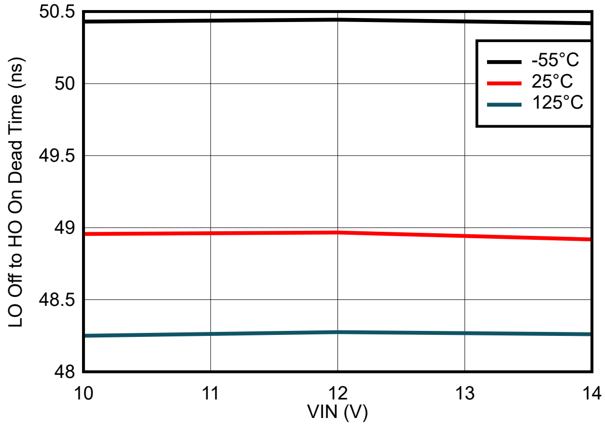
RLH = 11.8kΩ

Figure 7-31. LO Off to HO On Dead Time vs VIN Voltage



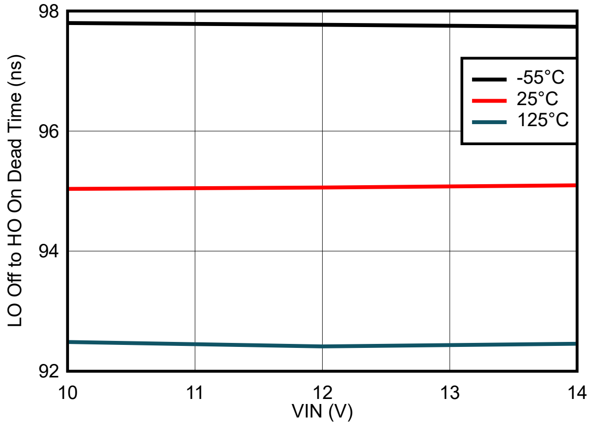
RLH = 21kΩ

Figure 7-32. LO Off to HO On Dead Time vs VIN Voltage



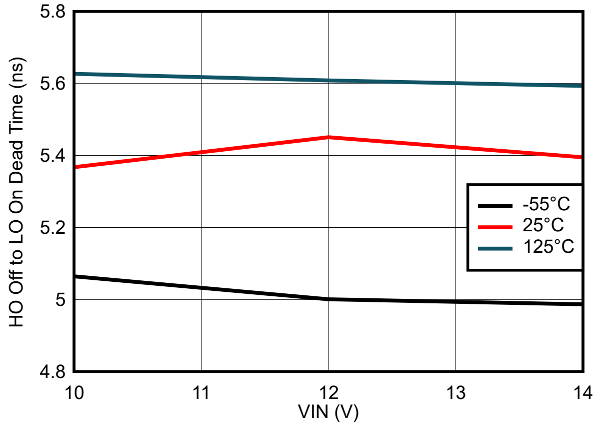
RLH = 52.3kΩ

Figure 7-33. LO Off to HO On Dead Time vs VIN Voltage



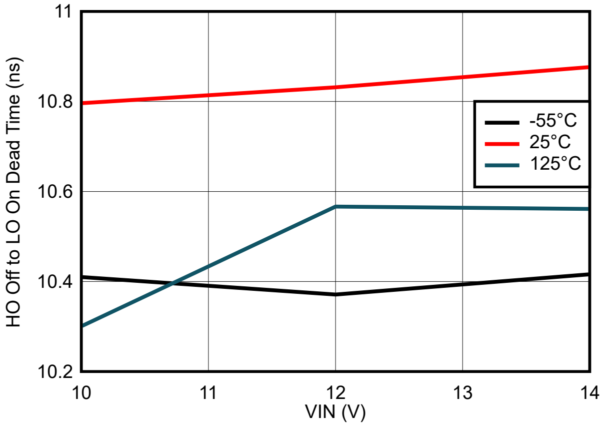
RLH = 105kΩ

Figure 7-34. LO Off to HO On Dead Time vs VIN Voltage



RLH = 7.87kΩ

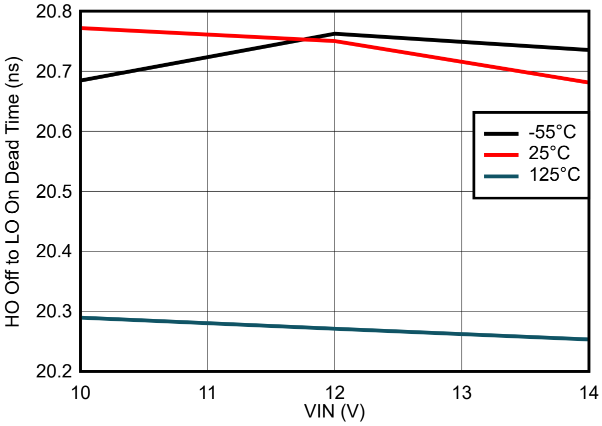
Figure 7-35. HO Off to LO On Dead Time vs VIN Voltage



RLH = 13.3kΩ

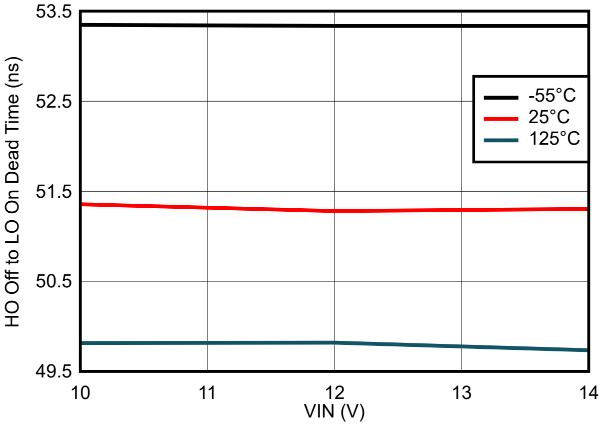
Figure 7-36. HO Off to LO On Dead Time vs VIN Voltage

7.8 Typical Characteristics (continued)



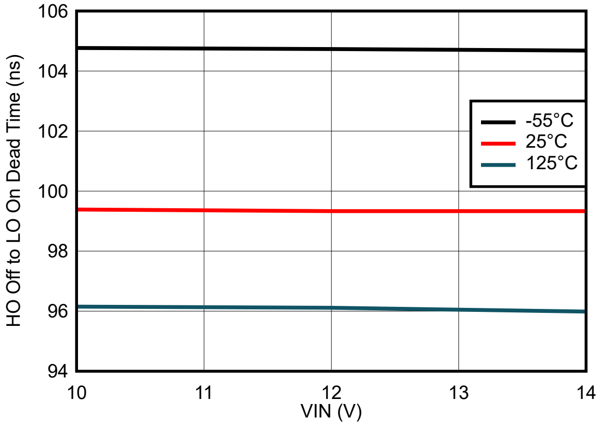
RLH = 23.7kΩ

Figure 7-37. HO Off to LO On Dead Time vs VIN Voltage



RLH = 57.6kΩ

Figure 7-38. HO Off to LO On Dead Time vs VIN Voltage



RLH = 113kΩ

Figure 7-39. HO Off to LO On Dead Time vs VIN Voltage

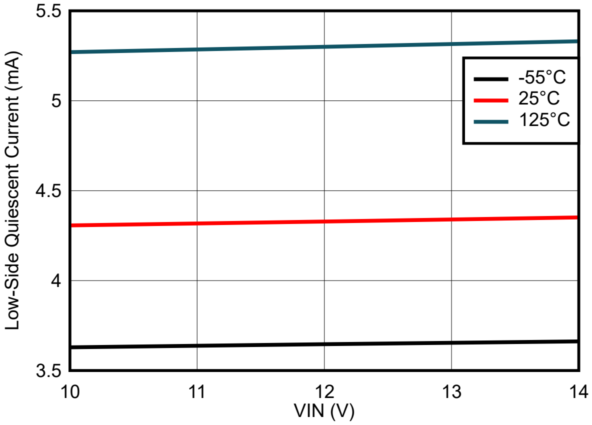


Figure 7-40. Low-Side Quiescent Current vs VIN Voltage

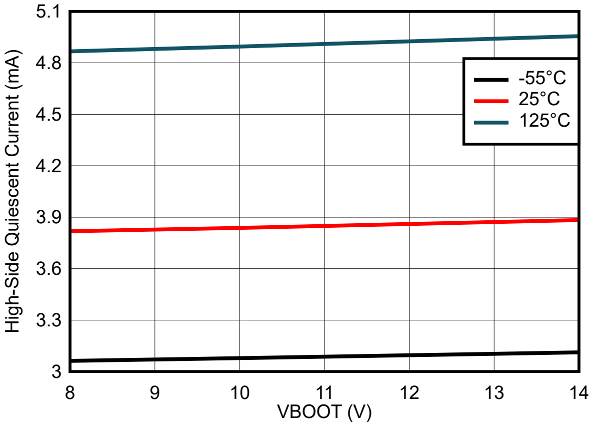
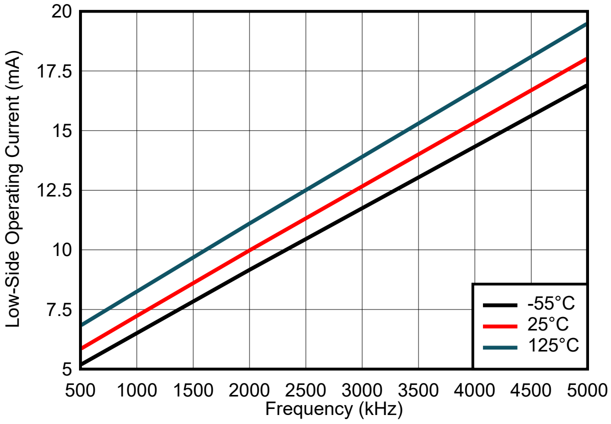


Figure 7-41. High-Side Quiescent Current vs BOOT Voltage



VIN = 12V

Figure 7-42. Low-Side Operating Current vs Frequency (IIM)

7.8 Typical Characteristics (continued)

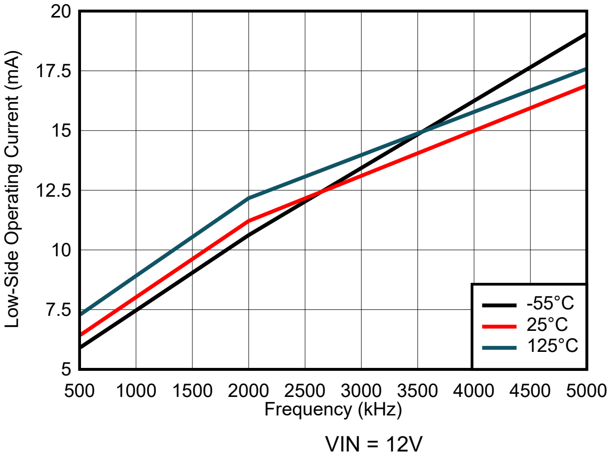


Figure 7-43. Low-Side Operating Current vs Frequency (PWM)

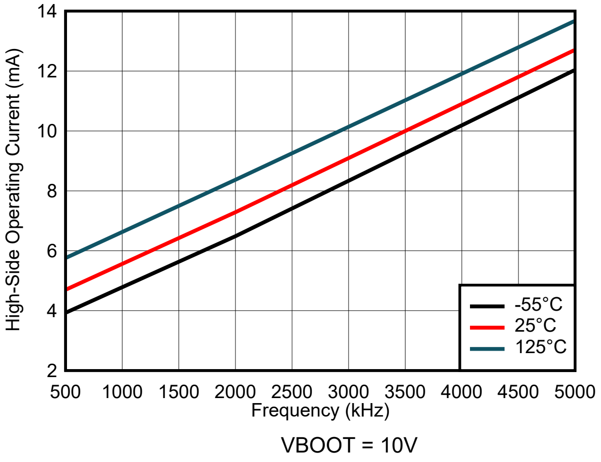


Figure 7-44. High-Side Operating Current vs Frequency (IIM)

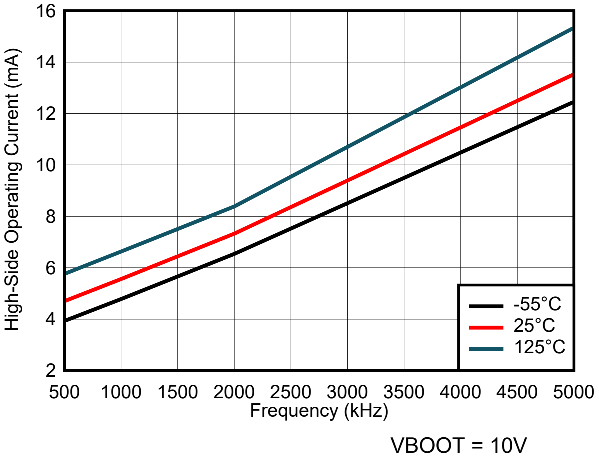


Figure 7-45. High-Side Operating Current vs Frequency (PWM)

8 Detailed Description

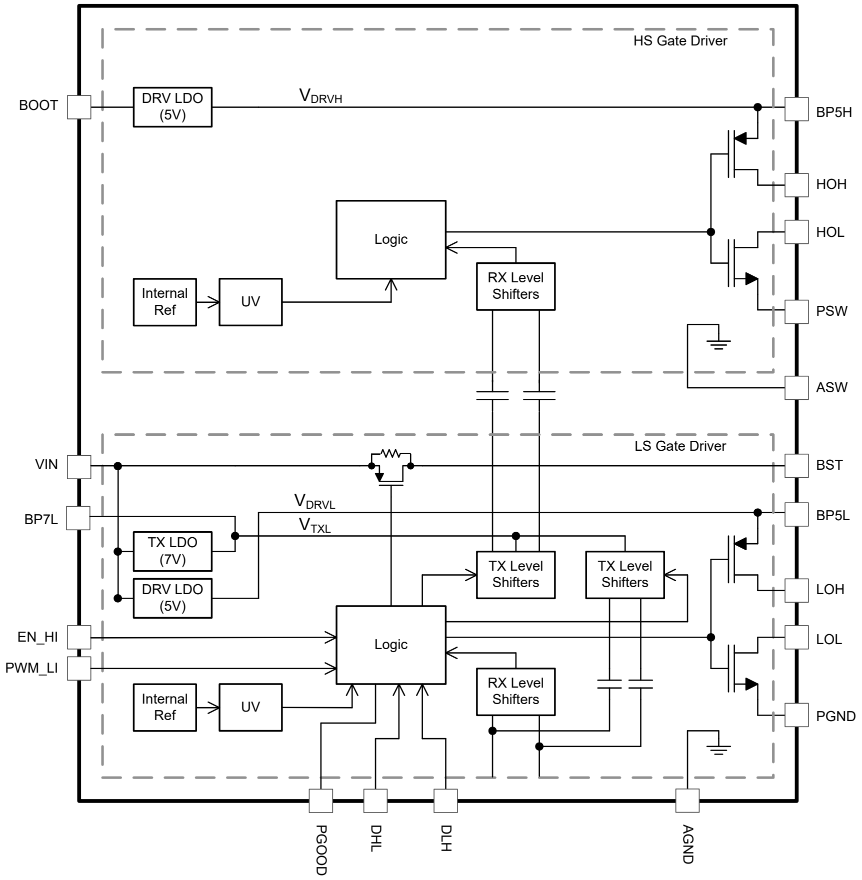
8.1 Overview

The TPS7H60x5 series of radiation-hardness-assured (RHA) half-bridge gate drivers are intended for use with enhancement mode GaN FETs. The series consists of the TPS7H6005 (200V driver), TPS7H6015 (60V driver), and the TPS7H6025 (22V driver). Each driver in the series has a 56-pin HTSSOP package and is available in both QMLP and SEP device grades. The drivers can be utilized in high frequency, high efficiency GaN based power converter designs. Each driver is designed to have a propagation delay of 30ns (typical) as well as 5.5ns (typical) high-side to low-side delay matching.

The drivers contain high-side and low-side internal linear regulators. These ensure that the gate voltages are maintained at 5V in order to prevent any damage of the GaN devices that are being driven. Split outputs on the high-side and low-side drivers provide the user the flexibility to independently adjust the turn-on and turn-off times of the GaN FETs. An external bootstrap diode is required for the gate drivers and as such, the user has the ability to optimize the diode based on the application. The drivers contain an internal switch in series with the bootstrap diode that can be used to prevent overcharging of the bootstrap capacitor and decreases reverse recovery losses in the diode.

The gate drivers have two modes of operation: PWM mode and independent input mode (IIM). The dual mode operation allows for each gate driver to be used with a wide number of PWM controllers to enable both synchronous rectifier control and GaN FET compatibility. The user also has the option to enable input interlock protection in IIM, allowing for anti-shoot through protection in synchronous buck and half-bridge topologies. This protection can also be disabled in IIM if desired, which allows the drivers to be utilized in two-switch forward converters and dual single ended applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage

During steady state operation, the input voltage of the TPS7H60x5 must be between 10V and 14V. This voltage serves as the input to the two low-side linear regulators, BP5L and BP7L. The external high-side bootstrap capacitor is also charged from VIN (see *Bootstrap Charging*). For best performance, add a bypass capacitor from VIN to AGND. Place this bypass capacitor as close to the gate driver as possible. This bypass capacitor is typically at least ten times greater than the value selected for the bootstrap capacitor.

8.3.2 Linear Regulator Operation

The TPS7H60x5 contains three internal linear regulators: BP5L, BP7L, and BP5H. BP5L and BP7L are included on the low side of the driver. These linear regulators provide 5V and 7V, respectively, as the nominal output voltages. BP5L is used to power the low-side logic circuitry as well as the low-side gate drive voltage. The BP5L regulator has an accuracy of 5V +3.5%/-5% to provide the proper voltage for driving GaN FETs. A minimum capacitor of 1μF is required from the BP5L pin to PGND. BP7L powers the low-side transmitters within the driver. A minimum capacitor of 1μF is also required from the BP7L pin to AGND.

On the high side, the voltage on BOOT serves as the input to the high side linear regulator BP5H. Similar to BP5L on the low-side, this regulator is used to power the high-side logic circuitry while providing the 5V +3.5%/-5% high-side gate voltage to the external FET. A minimum capacitor of 1μF is required from BP5H to PSW. The recommendation for all internal linear regulators is that these not be externally loaded other than where indicated within this document.

8.3.3 Bootstrap Operation

To generate the power for the high-side gate driver circuitry when used in a half-bridge configuration, the gate driver requires the use of a bootstrap circuit. The selection of the TPS7H60x5 bootstrap components is critical for proper gate driver operation. There are also various methods for bootstrap capacitor charging that can be utilized for this device.

8.3.3.1 Bootstrap Charging

The TPS7H60x5 provides the user several options for charging the bootstrap capacitor. The flexibility is to allow for operation with a wide range of PWM controllers, and also to allow the user to select an option with trade-offs that are most desirable for the specific application. In both instances, a bootstrap resistor is recommended to limit the bootstrap current during initial startup. The bootstrap resistor and capacitor need to be chosen such that sufficient time is allowed for the re-charge of the capacitor for the specific application.

The first option is to allow for charging of the bootstrap capacitor through the internal bootstrap switch of the driver. This switch is internally connected between VIN and BST pins and the bootstrap diode is connected externally between BST (anode) and BOOT (cathode). The bootstrap switch is only on when the low side driver output is on. By disallowing bootstrap charging during the converter dead times, the maximum voltage across the bootstrap capacitor can be reduced. The internal bootstrap switch has a parallel resistance of 1kΩ that allows for slow charging the bootstrap capacitor at start-up before low-side FET turn-on.

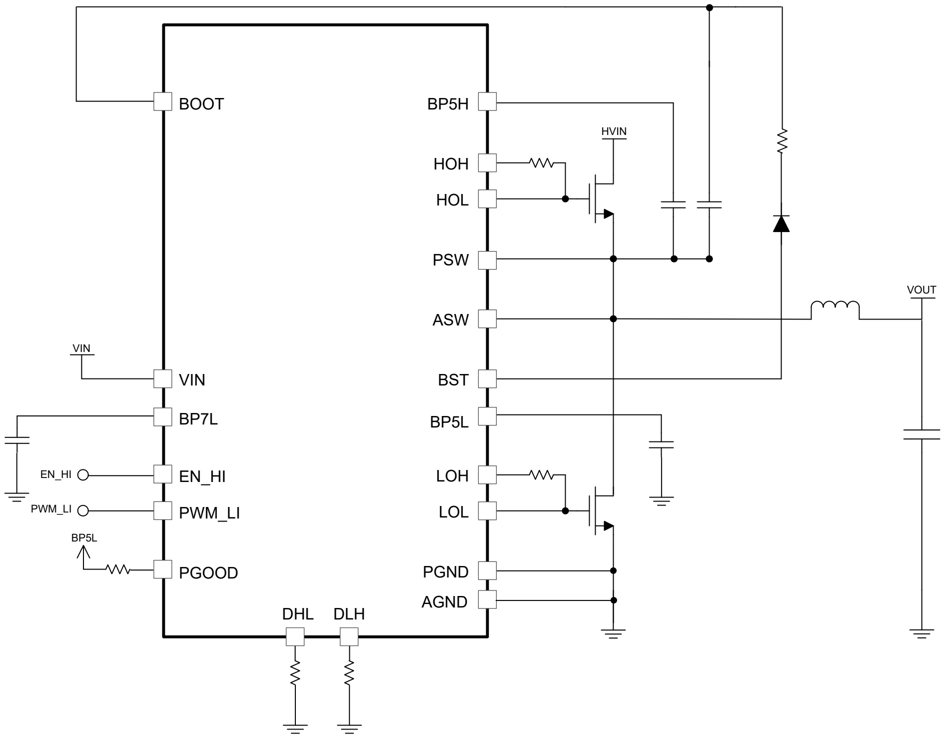


Figure 8-1. Internal Switch Bootstrap Charging Configuration

Another option is to charge the bootstrap capacitor directly from VIN. This is a more conventional method used with half-bridge drivers. This option can be considered in a number of use cases, but is particularly helpful in instances where the low-side FET turn-on is not immediate. This is the case when using the TPS7H60x5 with one of the three controllers in the TPS7H500x-SP family that have integrated synchronous rectification outputs. The synchronous rectification outputs are disabled during soft-start, and as such, when implementing a synchronous buck topology the bootstrap capacitor cannot be charged through the internal bootstrap switch of the driver. The bootstrap switch does have the parallel resistor for slow-charging, but sequencing and/or startup requirements for the converter can potentially dictate that the charging need to occur more rapidly. When using the direct VIN charging, the options for preventing overcharging of the bootstrap capacitor are to add a resistor in series with the bootstrap capacitor, to add a Zener diode in parallel with the bootstrap capacitor, or a combination of both. A consideration that must be made if using the Zener diode is that has an associated leakage current during normal operation, which contributes to the overall converter losses.

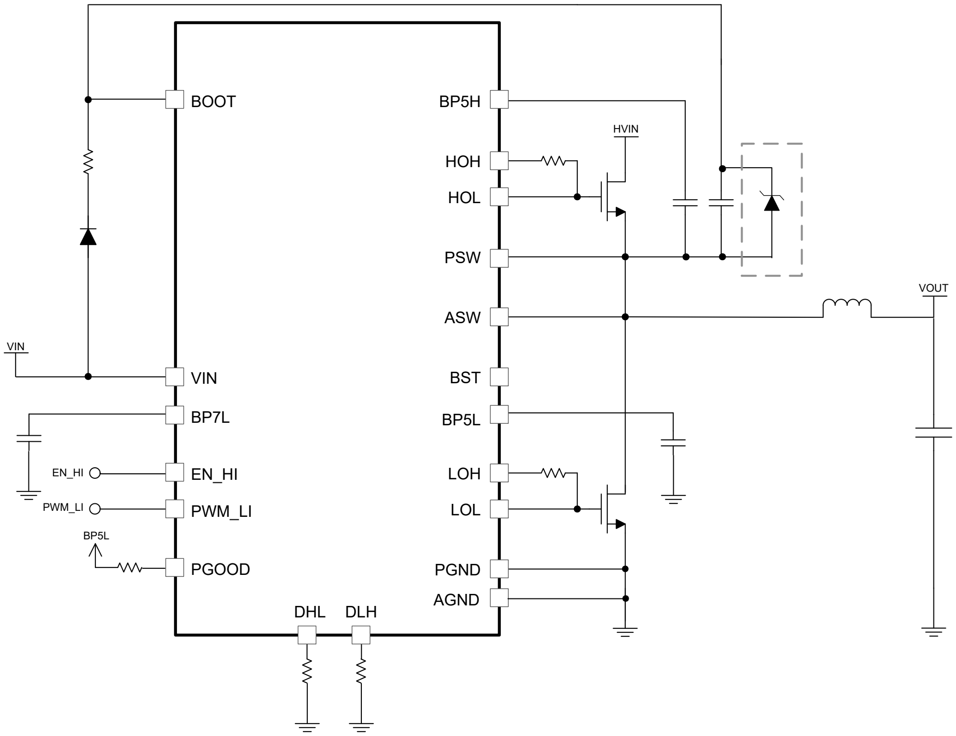


Figure 8-2. Direct VIN Bootstrap Charging Configuration

Lastly, a dual-charging option can be considered, which is a combination of the bootstrap switch and direct VIN charging methods. This method offers the benefit of circumventing any potential bootstrap charging issues during startup due to the low-side FET not turning on, while also taking advantage of the reduction of bootstrap voltage during normal operation offered by the internal switch. The series resistor used with the bootstrap diode in the direct VIN charging path must be higher than the resistance of the internal bootstrap switch to make sure that the charging is via the bootstrap switch during normal operation. This higher resistor value also effectively reduces the Zener current during normal operation. The trade-off for this configuration is the additional part count.

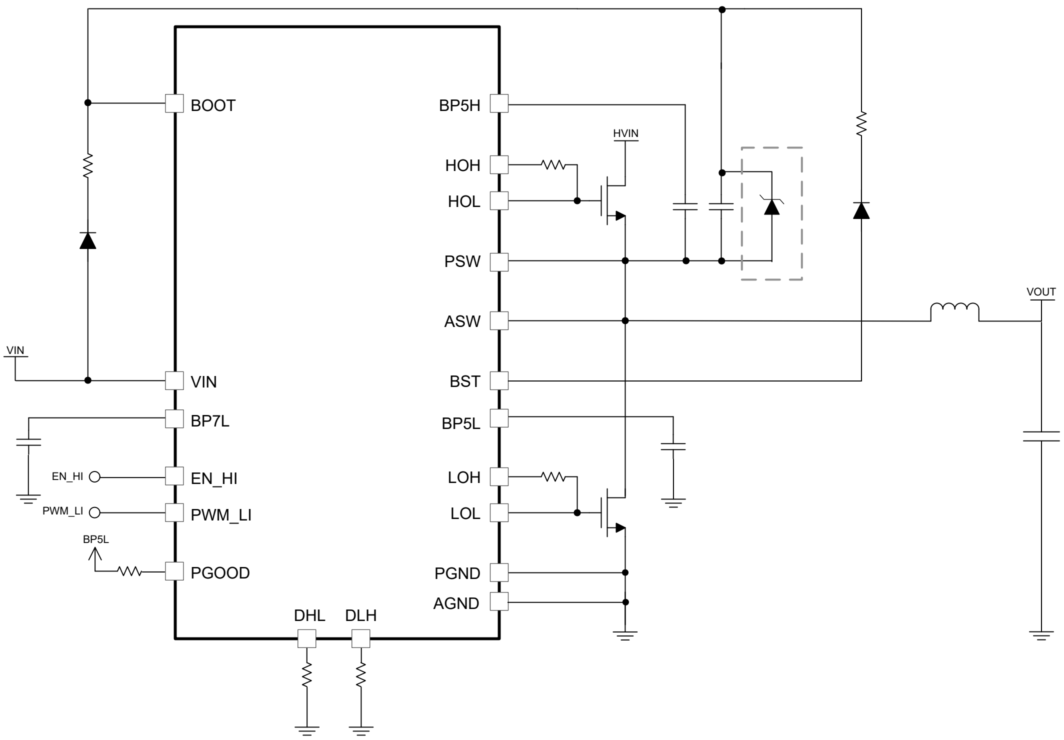


Figure 8-3. Dual Bootstrap Charging Configuration

8.3.3.2 Bootstrap Capacitor

The external bootstrap capacitor that is required for the driver is connected between BOOT and ASW. The bootstrap capacitor voltage serves as the input to the high-side linear regulator BP5H that provides the gate drive voltage for the high-side GaN FET. A general guideline for bootstrap capacitor selection is that its value should be at least 10× greater than the gate capacitance of the high-side GaN FET that is being driven:

$$C_{BOOT} \geq 10 \times C_g \tag{1}$$

where:

- C_g is the gate capacitance for the high-side GaN FET

A more detailed calculation of the minimum bootstrap capacitance needed can be found using Equation 2:

$$C_{BOOT} \geq \frac{Q_{total}}{\Delta V_{BOOT}} \tag{2}$$

$$Q_{total} = Q_g + I_{QBG} \times \frac{D_{MAX}}{f_{SW}} + \frac{I_{QHS}}{f_{SW}} \tag{3}$$

where:

- Q_g is the total gate charge for the high-side GaN FET
- I_{QBG} is the BOOT to AGND quiescent current
- D_{MAX} is the maximum duty cycle
- I_{QHS} is the high-side quiescent current
- f_{SW} is the switching frequency

and ΔV_{BOOT} is the maximum allowable drop on BOOT for proper operation:

$$\Delta V_{BOOT} = VIN - (n \times V_F) - V_{BOOT\_UVLO} \tag{4}$$

where:

- VIN is the gate driver input voltage
- n is the number of external bootstrap diodes placed in series
- V_F is the forward voltage drop of the bootstrap diode
- V_{BOOT_UVLO} is the falling undervoltage lockout threshold of BOOT (6.65V typical)

Using a sufficiently sized capacitor, low frequency motor driver applications can be supported using the TPS7H60x5 devices. Selection of a bootstrap capacitor with low ESR and ESL is recommended. The voltage rating of the bootstrap capacitor should have sufficient margin above the maximum expected bootstrap voltage.

8.3.3.3 Bootstrap Diode

Regardless of the method of charging the bootstrap capacitor, the TPS7H60x5 requires an external bootstrap diode rated to withstand the input voltage that is applied to the converter power stage in the half-bridge configuration. Care must be taken when selecting the external bootstrap diode. The bootstrap diode needs to be capable of handling peak transient currents that occur during the startup period. Fast recovery diodes should be used in the bootstrap circuit. The user needs to examine the I-V characteristics of the selected diode to verify that the forward voltage under the intended operating conditions does not become too large to trigger the undervoltage lockout of the BP5H regulator. Overall, the user needs to meet the conditions of Equation 5:

$$\mathrm{VIN} - (\mathrm{n} \times \mathrm{V_F}) \geq \mathrm{V_{BOOT\_UVLO}} \tag{5}$$

where:

- VIN is the gate driver input voltage
- n is the number of external bootstrap diodes placed in series
- V_F is the forward voltage drop of the bootstrap diode
- V_{BOOT_UVLO} is the falling undervoltage lockout threshold of BOOT (6.65V typical)

8.3.3.4 Bootstrap Resistor

The bootstrap resistor is used to (1) limit the peak current during gate driver startup and (2) control the slew rate (dv/dt) at BOOT. The peak current through the bootstrap diode, and through the BST switch if utilized, can become excessively high during the initial charging period. Furthermore, excessive slew rates at BOOT can cause a slight overshoot of the BP5H voltage during startup. To mitigate these issues a bootstrap resistor of at least 2Ω is recommended.

While the bootstrap resistor does alleviate peak current and slew rate issues, this resistor in conjunction with the bootstrap capacitor introduces a time constant τ:

$$\tau = \frac{\mathrm{R_{BOOT}} \times \mathrm{C_{BOOT}}}{\mathrm{D}} \tag{6}$$

where:

- R_{BOOT} is the value of the bootstrap resistor in ohms
- C_{BOOT} is the value of bootstrap capacitor in Farads
- D is the duty cycle of the switching converter

The time required to charge and refresh the charge of the bootstrap capacitor needs to be checked against the time constant. Lastly, the resistor can experience high power dissipation during the initial charging period. Select a resistor that can handle the energy during this charging period:

$$\mathrm{E} = \frac{1}{2} \times \mathrm{C_{BOOT}} \times \mathrm{V_{BOOT}^2} \tag{7}$$

where:

- C_{BOOT} is the value of bootstrap capacitor in Farads
- V_{BOOT} is the final voltage of the bootstrap capacitor

8.3.4 High-Side Driver Startup

For proper startup up of the high side, the BOOT to SW voltage must be greater than the BOOT UVLO rising threshold value of 6.4V (typical). In half-bridge converter configurations that have a pre-bias voltage present at the output, the bootstrap capacitor may not be able to adequately charge from VIN until the output voltage is sufficiently discharged. This same behavior can be seen during a brownout of VIN in which the input voltage temporarily decreases below the VIN UVLO falling threshold. Upon recovery, the low-side driver will attempt to begin normal operation, but the turn-on of the high-side driver will be delayed due to the output voltage that is present on the converter. This is a problem that is inherent in half-bridge gate drivers. Discharge circuits at the converter output can help alleviate the problem by forcing the output to a low voltage, only after which gate drive startup is attempted.

8.3.5 Inputs and Outputs

The input pins of the TPS7H60x5 are PWM_LI and EN_HI. Each of these pins has an internal pull-down resistance of approximately 200kΩ (typical). The functions of these pins vary depending on the selected mode of operation of the gate driver as described in *Device Functional Modes*. In PWM mode, PWM_LI serves as the input pin for the single PWM control signal into the driver and EN_HI is an enable pin for the driver. In independent input mode, PWM_LI serves as the low-side input and EN_HI serves as the high-side input. The inputs are capable of withstanding voltages up to 14V, which allows them to be directly connected to the outputs of an analog PWM controller with a power supply voltage less than or equal to 14V. If operating in independent input mode and either of the two input channels PWM_LI or EN_HI is not used, it is recommended to connect the input to AGND. Given that the inputs are edge-triggered, it is recommended to use input signals with slew rates faster than 2V/µs for expected operation.

The TPS7H60x5 contains split outputs on both the high-side and low-side. The high-side consists of outputs HOH and HOL, which are the source and sink outputs, respectively. Likewise, the low-side has source output LOH and sink output LOL. These split outputs offer the flexibility to adjust the turn-on and turn-off speed independently by placing additional impedance to either the turn-on or turn-off path of the GaN device that is being driven. These outputs are capable of sourcing 1.3A and sinking 2.5A, typical.

8.3.6 Dead Time

When operating in PWM mode, resistors to AGND are required on both DLH and DHL to program the dead time. The DHL resistor sets the dead time between high-side output (HO) turn-off to low-side (LO) output turn-on. Likewise, the resistor on DLH sets the dead-time between low-side (LO) turn-off to high-side (HO) turn-on. The resistor can be used to set the dead time from a minimum value of roughly 5ns up to 100ns. The resistor must be populated on both pins to operate the device in this mode.

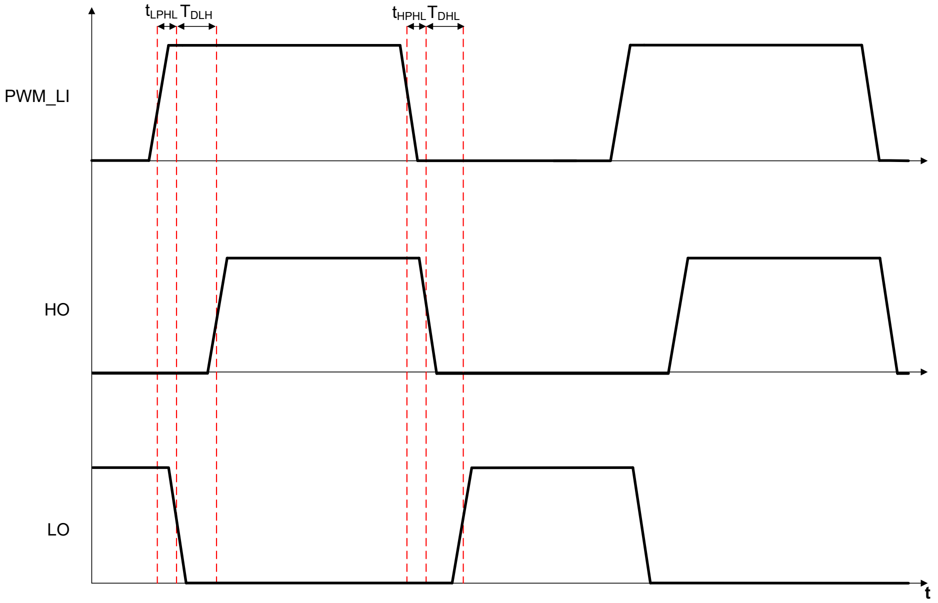


Figure 8-4. Timing Waveforms in PWM Mode Showing Dead Time

The resistors required to program for a desired dead times are calculated from

$$\mathrm{RHL} = 1.077 \times \mathrm{T_{DHL}} + 1.812 \quad (8)$$

where:

- T_{DHL} is the desired "HO off to LO on" dead time in ns
- RHL is in kΩ

$$\mathrm{RLH} = 1.064 \times \mathrm{T_{DLH}} - 0.630 \quad (9)$$

where:

- T_{DLH} is the desired "LO off to HO on" dead time in ns
- RLH is in kΩ

Carefully select dead time to prevent cross-conduction between the high-side and low-side switches, while also minimizing losses during this period. The resistors selected for RHL and RLH are recommended to have a tolerance of 1% or better.

8.3.7 Input Interlock Protection

The TPS7H60x5 can be configured to have input interlock protection in independent input mode (IIM). To activate the input interlock protection in IIM, DHL must be connected to 5V while DLH has a resistor (valued between 100kΩ and 220kΩ) connected between the pin and AGND. This protection is intended to improve the robustness and reliability of the power stage with which the driver is being used by preventing shoot-through of the GaN FETs in a half-bridge configuration. In any instance when the protection is enabled and both inputs are logic high, the internal logic turns both of the outputs off. Both outputs remain off until one of the inputs goes low, in which case the outputs follow the input logic. There is no fixed time deglitching for this feature in order to not impact the propagation delay and dead time of the driver. Small filters at the inputs of the driver can be utilized to improve robustness in noise prone applications.

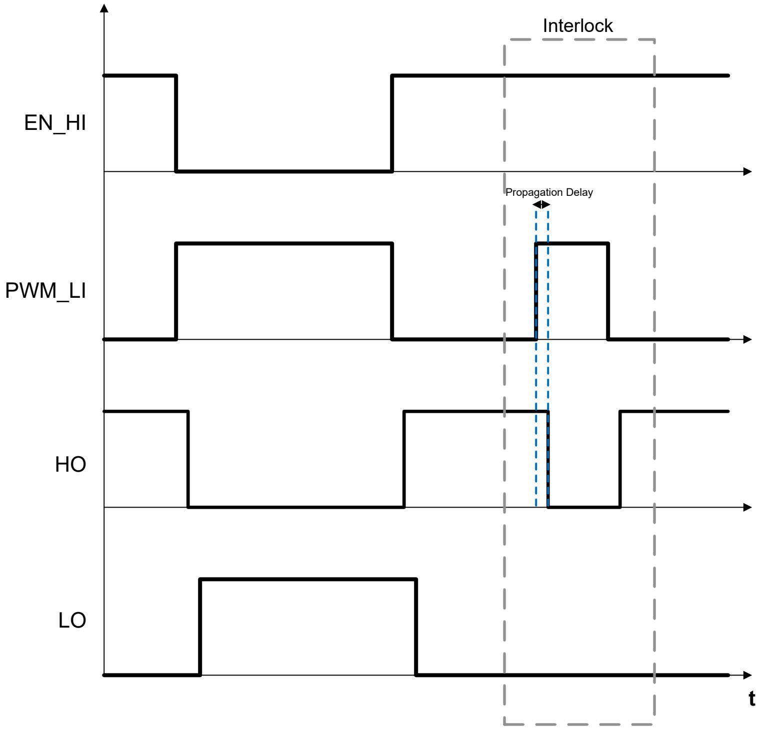


Figure 8-5. Input Interlock Protection in Independent Input Mode

8.3.8 Undervoltage Lockout and Power Good (PGOOD)

The TPS7H60x5 has undervoltage lockout (UVLO) on BP5L, BP7L, BP5H, BOOT, and VIN. When the output voltage on any of the low-side linear regulators or VIN falls below the UVLO threshold (4.05V for the BP5L linear regulator, 6.2V for the BP7L linear regulator, and 8.1V for VIN), the PWM inputs are ignored to prevent the GaN FETs from partial turn-on. In this scenario, the UVLO actively pulls LO and HO low. When the low-side regulators and VIN are each above the respective UVLO threshold but one of the high-side UVLOs is triggered (4.05V for BP5H and/or 6.65V for BOOT), then only HO is pulled low.

The gate driver also has a power good (PGOOD) pin, which indicates when any of the low-side linear regulators have entered undervoltage lockout. The pin enters the logic-high state when all low-side regulators and VIN each have surpassed the respective rising UVLO threshold. The pin goes, or remains, logic-low if any one of these linear regulators or VIN falls below the corresponding falling UVLO threshold. The PGOOD pin has an internal pull-down resistance of 1MΩ when the pin is in the logic-high state. A pull-up of 10kΩ connected from PGOOD to BP5L is recommended.

8.3.9 Negative SW Voltage Transients

Though enhancement mode GaN FETs do not contain a body diode like silicon FETs, the devices are capable of reverse conduction due to the symmetrical device structure. During the reverse conduction periods, the source-drain voltage of the GaN FET is typically higher than what is encountered with a traditional silicon FET, largely depending on the type of GaN device that is being used. As such, the switch node pins of the driver (ASW and PSW, collectively referred to as SW) have a negative voltage present. This negative transient can lead to an excessive bootstrap voltage, since BOOT is always referenced to SW. Furthermore, the printed circuit board layout and device parasitic inductances can further intensify the negative voltage transients. Operating at a bootstrap voltage above the absolute maximum of 16V can be detrimental to the gate driver, so care must be taken to make sure that the maximum BOOT to SW voltage differential is not exceeded. Generally, BOOT follows SW instantaneously so that the BOOT to SW voltage does not overshoot significantly. However, an external Zener diode can be used between BOOT and SW to clamp the bootstrap voltage to acceptable values during operation.

8.3.10 Level Shifter

The TX and RX level shifters interface between the inputs on the low-side to the high-side driver stage which is referenced to the high voltage switch node (ASW). The level shifters allow control of the HO output. The level shifters in both the high-side and low-side signal paths are identical and provide excellent delay matching (5.5ns typical).

8.4 Device Functional Modes

The mode of operation for the TPS7H60x5 is determined by the state of the DHL and DLH pins. The configuration of these pins should not be changed during device operation. There are two different operational modes: PWM and independent input mode. In PWM mode, the EN_HI pin is used to enable the device and a single PWM input signal is required on PWM_LI and the TPS7H6005 generates the complementary output signals on LO and HO. Since the primary application of this mode is a synchronous buck converter, HO will generate the main output and LO will generate the synchronous rectification output. Resistors are connected from DHL to AGND and DLH to AGND in order to program the dead time between the high-side and low-side outputs. For acceptable resistor values (TBD) to use in PWM mode, refer to *Dead Time* section.

In independent input mode (IIM), separate PWM input signals are required on PWM_LI and EN_HI. The corresponding outputs of the TPS7H60x5 are driven directly from these inputs. In IIM with interlock disabled, DLH is tied to BP5L and DHL has a resistor connected to AGND. For operation in IIM with interlock enabled, connect a resistor between DLH and AGND while connecting DHL to BP5L. For both operating mode options in IIM, resistors used must be valued between 100kΩ and 220kΩ.

Table 8-1 shows the configuration for each operating mode. Note that these are the only valid operating modes for the driver, and the connections for DLH and DHL must adhere to one of these configurations for proper operation.

Table 8-1. TPS7H60x5 Operating Mode Selection

Operating Mode	DLH	DHL
PWM	Resistor to AGND	Resistor to AGND
Independent input mode - input interlock disabled	BP5L	Resistor to AGND (100kΩ to 220kΩ)
Independent input mode - input interlock enabled	Resistor to AGND (100kΩ to 220kΩ)	BP5L

Table 8-2 shows the truth table for each functional mode of the TPS7H60x5.

Table 8-2. TPS7H60x5 Truth Table

Inputs		PWM Mode		IIM - Interlock Disabled		IIM - Interlock Enabled	
EN_HI	PWM_LI	HO	LO	HO	LO	HO	LO
0	0	0	0	0	0	0	0
0	1	0	0	0	1	0	1
1	0	0	1	1	0	1	0
1	1	1	0	1	1	0	0

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H60x5 series consists of half-bridge gate drivers designed for the optimal control of GaN FETs in a space environment. Each enables high-frequency, high-efficiency space grade converter design while offering superb robustness against radiation induced effects. The drivers contain integrated 5V linear regulators for the gate voltage on both the low side and the high side, ensuring enhanced reliability for the GaN FETs that are being driven. The primary use case for the drivers is in half-bridge configurations, such as synchronous buck or full-bridge topologies. However, the driver can easily be utilized in other common converter topologies such as the push-pull, active clamp forward, or two-switch forward (with external circuit additions).

The TPS7H60x5 has several features that allows for operation with both legacy radiation hardened PWM controllers and newer devices like the TPS7H5001-SP or TPS7H5005-SEP as part of a GaN centric converter design. The input pins of the driver can accept signals up to 14V, allowing it to interface directly with the older PWM controllers with high output voltages. The device also offers two distinct operating modes: PWM mode and independent input mode (IIM). In PWM mode the gate driver requires only a single input, while generating the primary and synchronous rectification outputs needed to control a synchronous buck converter. The dead time between the generated signals can be programmed via the gate driver. IIM allows for independent signals to control the low side and the high side, or if desired, can be used to operate the device in a dual low side configuration. In IIM, interlock protection can be turned on or off, depending on the specific user needs.

Furthermore, the device offers undervoltage lockout protection for both its internal regulators and the VIN and BOOT voltages. An optional bootstrap switch is integrated into the driver, which allows for charging the bootstrap diode through VIN, and remains turns on only when the low-side output is on. The combination of features and radiation performance for the TPS7H60x5 make it ideal for use in space-grade converter designs.

9.2 Typical Application

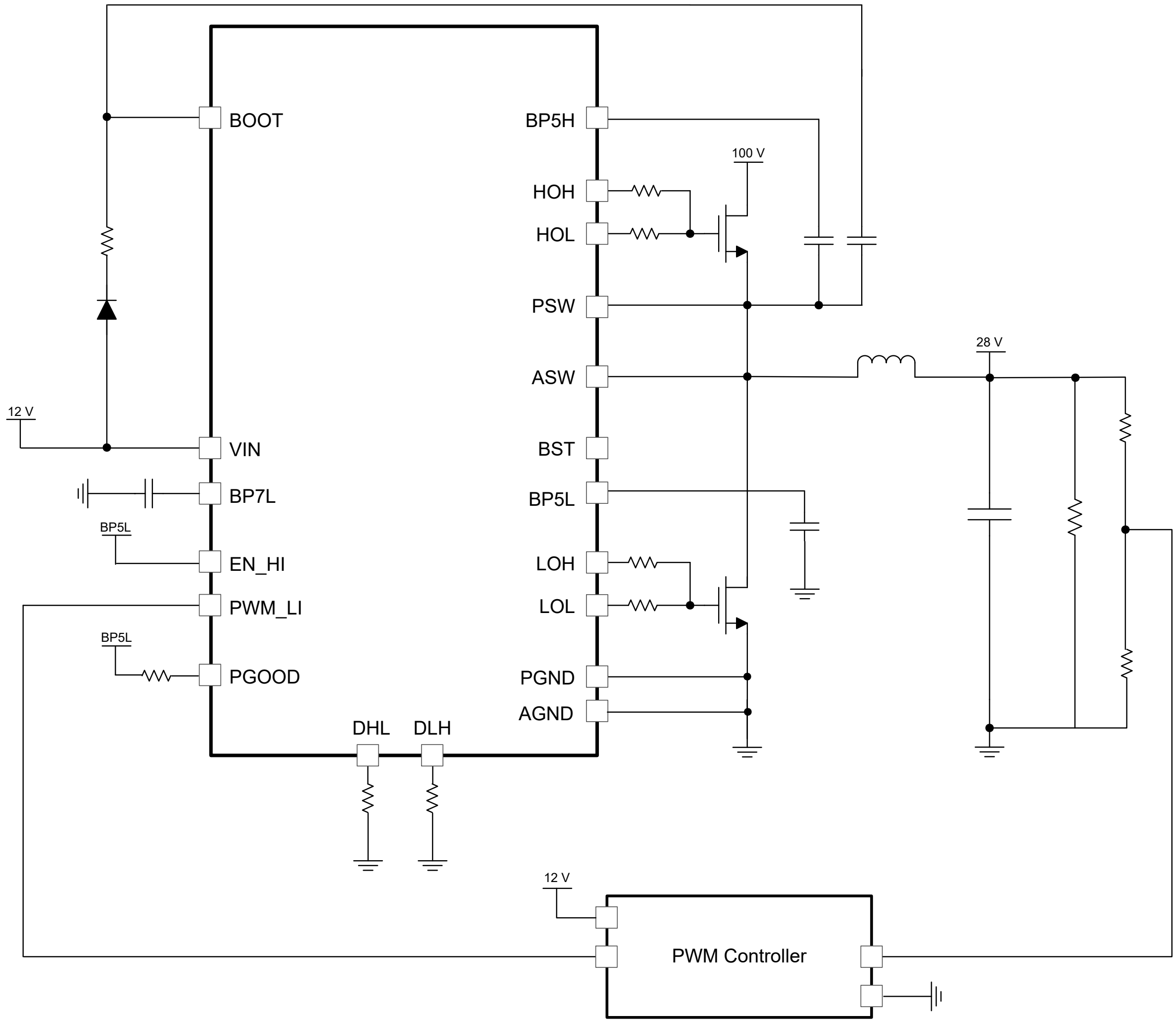


Figure 9-1. Typical Application Utilizing TPS7H6005 in Synchronous Buck Converter

9.2.1 Design Requirements

The example provided is to demonstrate the usage of TPS7H6005 in a high voltage synchronous buck converter. The design example is intended to detail component selection and configuration related to the TPS7H6005. For this particular application, the gate driver is operating in PWM mode.

Table 9-1. Design Parameters

PARAMETER	VALUE
Power stage input supply voltage	100V
Output voltage	28V
Output current	10A
Switching frequency	500kHz
Gate driver input voltage	12V
Duty cycle	28% nominal, ~35% maximum
Inductor	15µH
GaN FET	EPC2307 (evaluation only)
Operating mode	PWM

Note that the selected GaN FET is for laboratory evaluation of the driver. TI recommends selecting a GaN FET that satisfies both the electrical and radiation requirements of the design.

9.2.2 Detailed Design Procedure

9.2.2.1 Bootstrap and Bypass Capacitors

The external bootstrap capacitor needs to maintain operation above the BOOT UVLO falling threshold during normal operation. As a best design practice, size the capacitor to allow for substantial margin this threshold. The first step in determining the bootstrap capacitor value is calculating for ΔV_{BOOT}. This is the maximum allowable drop on the bootstrap capacitor:

$$\Delta V_{BOOT} \approx VIN - (n \times V_F) - V_{BOOT\_UVLO} = 12V - (1 \times 0.9V) - 6.65V = 4.35V \quad (10)$$

where:

- n is the number of bootstrap diodes used in series
- V_F is the voltage drop of the bootstrap diode chosen
- V_{BOOT_UVLO} is the BOOT UVLO falling threshold voltage

To maintain significant margin and account for any additional voltage drop across the bootstrap resistor used and also for load transients, the capacitor is calculated for ΔV_{BOOT} of 1.5V. Referring to *Bootstrap Capacitor*, the value of Q_{total} needs to first be determined, and then C_{BOOT} can subsequently be calculated:

$$Q_{total} = Q_g + I_{QBG} \times \frac{D_{MAX}}{f_{SW}} + \frac{I_{QHS}}{f_{SW}} = 10.6nC + 20\mu A \times \frac{0.35}{500kHz} + \frac{4mA}{500kHz} = 18.6nC \quad (11)$$

$$C_{BOOT} \geq \frac{Q_{total}}{\Delta V_{BOOT}} = \frac{18.6nC}{1.5V} = 12.4nF \quad (12)$$

A minimum value of 12.4nF is needed for the design. However, given the potential for capacitance changes with temperature and applied voltage, as well as unexpected circuit behavior such as load transients that impact the bootstrap charging time, a 100nF X7R capacitor is selected.

The VIN capacitor selected must be larger than the bootstrap capacitor. The general recommendation is that this capacitor is at least ten times the bootstrap capacitor value, which gives 1µF capacitor in this instance. For the evaluation setup, a 2.2µF and 1µF capacitor were used at VIN, both ceramic X7R type capacitors. The recommendation is to place these capacitors and the bootstrap capacitors as close the respective pins as possible. Select capacitors with voltage ratings that are sufficiently larger than the maximum applied voltage (that is, greater than two times if possible).

Lastly, as detailed in *Linear Regulator Operation*, select high-quality 1µF X7R ceramic capacitors for use at BP5H, BP5L, and BP7L outputs. Place these capacitors in close proximity to the respective pins.

9.2.2.2 Bootstrap Diode

The bootstrap diode needs to have sufficient voltage rating to block the power stage input voltage of the power converter for the synchronous buck application. Depending on the type of diode selected, series diodes are required if the power stage input voltage is high. As mentioned in *Bootstrap Diode*, the diode also needs to be able to handle the peak current during the gate driver startup, and exhibit a low forward voltage drop, low junction capacitance, and fast recovery time. Particularly at higher frequencies, a Schottky diode may be required. A 150V, 1A rated Schottky diode with 110pF junction capacitance is selected for the evaluation setup. Note that the diode selected for use in the evaluation is for laboratory testing only, and TI recommends selection of a diode that meets all of the system performance and radiation needs.

9.2.2.3 BP5x Overshoot and Undershoot

Although the TPS7H6005 has internal high-side and low-side linear regulators (BP5H and BP5L, respectively) to provide a gate drive voltage with excellent DC accuracy, parasitic inductances and capacitances from both the

PCB layout and GaN FET can lead to transient ringing on the gate drive waveform during switching. This ringing can result in voltage peaks that are higher than the regulated BP5x voltage, and potentially exceed the absolute maximum VGS ratings of the selected GaN FET. Note that there is also potential for violating the minimum VGS ratings during turn-off, depending on the severity of the oscillations on the gate voltage waveform. To mitigate the amplitude of the oscillations and avoid excessive ringing, the driver needs to be in close proximity to the GaN FETs that are being driven, and gate resistors can be used. The *Gate Resistor* section provides more details about the gate resistor selection. See the *Layout Guidelines* section for recommendations on how to optimize the gate driver layout.

9.2.2.4 Gate Resistor

The TPS7H6005 has split outputs, allowing for resistors to be placed in series with the gate of the GaN FET in both the turn-on and turn-off paths. These gate resistors serve to dampen ringing at the gate of the device that is caused by parasitic capacitances and inductances. Ringing and noise can also be presented due to the high voltage and current switching in the gate drive power loop. This is particularly important for GaN devices which have low values for the absolute maximum gate voltages. Furthermore, the gate resistors can also be used to tune the drive strength of the drive. This is done by limiting the peak current capability of the driver. For this design, 2Ω resistors are used for both the turn-on and turn-off gate paths. From these values, the high-side peak pull-up current can be calculated as shown in :

$$I_{OHH} = \mathrm{MIN}\left(1.3\mathrm{A}, \frac{V_{BP5H}}{R_{HOH} + R_{GATE\_ON} + R_{GFET(int)}}\right) \tag{13}$$

where:

- V_{BP5H} is the output voltage of the high side linear regulator
- R_{HOH} is the internal high-side pull-up resistance (1.3Ω calculated from the high-level output voltage specification)
- R_{GATE_ON} is the gate resistor value used in the turn-on path
- $R_{GFET(int)}$ is the internal gate resistance of the GaN FET being driven (typically available from the GaN FET manufacturer)

Note that as indicated in the *Specifications* section, the peak source current the driver is capable of providing is approximately 1.3A (typical), so I_{OHH} is limited by this value. In this instance:

$$I_{OHH} = \frac{V_{BP5H}}{R_{HOH} + R_{GATE\_ON} + R_{GFET(int)}} = \frac{5\mathrm{V}}{1.3\Omega + 2\Omega + 0.4\Omega} \approx 1.3\mathrm{A} \tag{14}$$

Likewise, for the peak high-side sink current:

$$I_{OLH} = \mathrm{MIN}\left(2.5\mathrm{A}, \frac{V_{BP5H}}{R_{HOL} + R_{GATE\_OFF} + R_{GFET(int)}}\right) \tag{15}$$

where:

- R_{HOL} is the internal high-side pull-down resistance (0.7Ω calculated from the low-level output voltage specification)
- R_{GATE_OFF} is the gate resistor value used in the turn-off path

As such, the peak sink current can be calculated as:

$$I_{OLH} = \frac{V_{BP5H}}{R_{HOL} + R_{GATE\_OFF} + R_{GFET(int)}} = \frac{5\mathrm{V}}{0.7\Omega + 2\Omega + 0.4\Omega} = 1.6\mathrm{A} \tag{16}$$

The equations for the low-side peak source and sink current are provided, but note that in this instance these are identical to the high-side values calculated.

$$I_{OHL} = \mathrm{MIN}\left(1.3\mathrm{A}, \frac{V_{BP5L}}{R_{LOH} + R_{GATE\_ON} + R_{GFET(int)}}\right) = \frac{5\mathrm{V}}{1.3\Omega + 2\Omega + 0.4\Omega} \approx 1.3\mathrm{A} \tag{17}$$

$$I_{OLL} = MIN\left(2.5A, \frac{V_{BP5L}}{R_{LOL} + R_{GATE\_OFF} + R_{GFET(int)}}\right) = \frac{5V}{0.7\Omega + 2\Omega + 0.4\Omega} = 1.6A \tag{18}$$

The selection of the external gate resistor typically requires tuning and is an iterative process. The best practice is to evaluate the value of the gate resistors on the specific PCB design to verify the intended impact and adjust as needed.

9.2.2.5 Dead Time Resistor

When configured in PWM mode, the gate drive allows for the programming of two separate dead times:

- between LO off and HO on using RLH
- between HO off and LO on using RHL

The dead time values selected are critical as these directly impact that losses that occur in the converter during these periods. The dead time is carefully chosen to avoid cross-conduction between the high-side FET and low-side FET, while also minimizing the third-quadrant conduction time for the GaN FETs. For this particular application, a dead time of approximately 25ns was targeted for both T_{DLH} and T_{DHL}.

$$RHL = 1.077 \times T_{DHL} + 1.812 = (1.077 \times 25ns) + 1.812 = 28.74k\Omega \tag{19}$$

$$RLH = 1.064 \times T_{DLH} - 0.630 = (1.064 \times 25ns) - 0.630 = 25.97k\Omega \tag{20}$$

A resistor value of 30kΩ was used for both RHL and RLH.

9.2.2.6 Gate Driver Losses

Gate drive devices such as the TPS7H6005 have several different components that comprise the power losses. The quiescent power losses P_{QC}can be determined using Equation 21 :

$$P_{QC} = (VIN \times I_{QLS}) + (V_{BOOT} \times I_{QHS}) = (12V \times 5mA) + (10V \ \times 4mA) = 100mW \tag{21}$$

where:

- I_{QLS} is the low-side quiescent current (selected for PWM mode in this design)
- I_{QHS} is the high-side quiescent current (selected for PWM mode in this design)
- V_{BOOT} is the voltage at BOOT with respect to ASW

Leakage current power losses P_{BG} can be calculated using Equation 22:

$$P_{BG} = V_{BG} \times I_{QBG} \times D_{MAX} = 110V \ \times 20\mu A \times 0.35 = 0.77mW \tag{22}$$

where:

- V_{BG} is the voltage between BOOT and AGND
- I_{QBG} is the BOOT to AGND leakage current

There are losses that occur within the driver due to the charging and discharging of the GaN FET gate charge. To determine these, first calculate P_{GATE} as:

$$P_{GATE} = V_{BP5x} \times Q_G \times f_{SW} = 5V \ \times 10.6nC \times 500kHz = 26.5mW \tag{23}$$

This loss is actually distributed amongst the resistances in the gate driver loop, which includes the driver, the gate resistances and the GaN FET. The power dissipated within the TPS7H6005 for both turn-on and turn-off can be calculated:

$$P_{DRV\_ON\_HS} = \frac{1}{2} \times \frac{R_{HOH} \times P_{GATE}}{R_{HOH} + R_{GATE} + R_{GFET(int)}} \tag{24}$$

$$P_{DRV\_OFF\_HS} = \frac{1}{2} \times \frac{R_{HOL} \times P_{GATE}}{R_{HOL} + R_{GATE} + R_{GFET(int)}} \tag{25}$$

$$P_{DRV\_ON\_LS} = \frac{1}{2} \times \frac{R_{LOH} \times P_{GATE}}{R_{LOH} + R_{GATE} + R_{GFET(int)}} \tag{26}$$

$$P_{DRV\_OFF\_LS} = \frac{1}{2} \times \frac{R_{LOL} \times P_{GATE}}{R_{LOL} + R_{GATE} + R_{GFET(int)}} \tag{27}$$

In this instance, the high-side and low-side losses are the same:

$$P_{DRV\_ON\_HS} = P_{DRV\_ON\_LS} = \frac{1}{2} \times \frac{R_{xOH} \times P_{GATE}}{R_{xOH} + R_{GATE} + R_{GFET(int)}} = \frac{1}{2} \times \frac{1.3\Omega \times 26.5mW}{1.3\Omega + 2\Omega + 0.4\Omega} = 4.7mW \tag{28}$$

$$P_{DRV\_OFF\_HS} = P_{DRV\_OFF\_LS} = \frac{1}{2} \times \frac{R_{xOL} \times P_{GATE}}{R_{xOL} + R_{GATE} + R_{GFET(int)}} = \frac{1}{2} \times \frac{0.7\Omega \times 26.5mW}{0.7\Omega + 2\Omega + 0.4\Omega} = 3mW \tag{29}$$

Finally, the P_{GATE} losses within the driver can be found:

$$P_{DRV\_HS} = P_{DRV\_ON\_HS} + P_{DRV\_OFF\_HS} = 4.7mW + 3mW = 7.7mW \tag{30}$$

$$P_{DRV\_LS} = P_{DRV\_ON\_LS} + P_{DRV\_OFF\_LS} = 4.7mW + 0.8mW = 7.7mW \tag{31}$$

$$P_{DRV} = P_{DRV\_HS} + P_{DRV\_LS} = 7.7mW + 7.7mW = 15.4mW \tag{32}$$

There is also a component of power consumption associated with the operating current of the driver, which is specified at no-load and frequency dependent. These can be approximated using the operating current parameters in the *Specifications* section:

$$P_{OP\_PWM} = \left(VIN \times I_{OP\_PWM\_LS}\right) + \left(V_{BOOT} \times I_{OP\_PWM\_HS}\right) = (12V \times 6mA) + (10V \times 5mA) = 122mW \tag{33}$$

where:

- $I_{OP\_PWM\_LS}$ is the low-side operating current (selected for PWM mode at 500kHz)
- $I_{OP\_PWM\_HS}$ is the high-side operating current (selected for PWM mode at 500kHz)

9.2.3 Application Curves

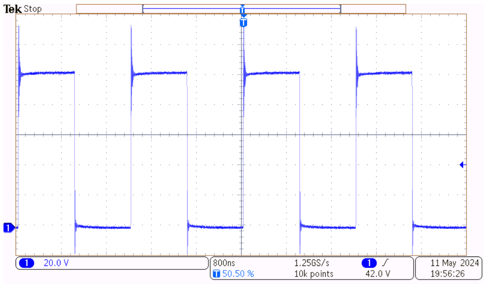


Figure 9-2. 100V, 500kHz Switch Node Signal From TPS7H6005EVM

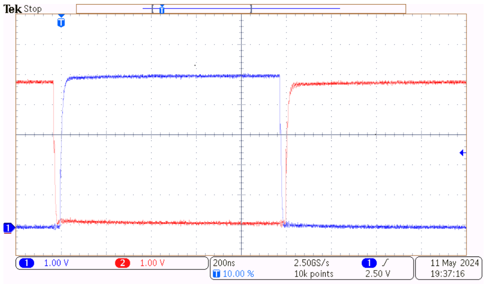


Figure 9-3. 500kHz HO (blue) and LO (red) Gate Driver Outputs in PWM Mode From TPS7H6005EVM

9.3 Power Supply Recommendations

The recommended bias supply voltage range for TPS7H60x5 is from 10V to 14V. The input voltage supply for the driver should be well regulated and properly bypassed for best electrical performance. The BOOT voltage which supplies the high-side driver should be between 8V to 14V. It is imperative to minimize the voltage drop along the bootstrap charging path so that the high-side driver does not inadvertently enter into undervoltage lockout at any time during normal operation.

A local bypass capacitor must be placed between the VIN and AGND pins. Likewise, the bootstrap capacitor should be placed between the BOOT and ASW pins, and must also be in close proximity to the device. This capacitor must be located as close as possible to the device. TI recommends a low-ESR, low-ESL, ceramic, surface-mount capacitors (X7R or better) for the connections at VIN and BOOT.

9.4 Layout

9.4.1 Layout Guidelines

Small gate capacitance and Miller capacitance enable enhancement mode GaN FETs to operate with fast switching speed. The induced high dv/dt and di/dt, coupled with a low gate threshold voltage and limited headroom of enhancement mode GaN FETs gate voltage, make the circuit layout crucial to the optimum performance. Following are some recommendations:

1. Place the GaN FETs as close as possible to the gate driver. The main priority of the layout is to decrease overall loop inductance and to minimize noise coupling issues by confining the peak currents that charge and discharge the GaN FET gates to a minimal physical area on the printed circuit board.
2. Minimize the loop area of the bootstrap charging path as it can contain high peak currents. Given that the TPS7H60x5 has multiple bootstrap charging options, and that the charging takes place on a cycle-by-cycle basis, place both the bootstrap capacitor and diode to facilitate a small loop area for the chosen charging method.
3. Place all bypass capacitors (VIN to AGND, BP5L to AGND, BP5H to ASW, BOOT to ASW) as close to the device and respective pins as possible. Capacitors with low ESR and ESL are recommended. If possible, place these capacitors on the same side of the printed circuit board as the gate driver.
4. Separate power traces and signal traces and minimize any overlap of the signals on different printed circuit board layers.
5. The parasitic inductance in series with the source of the high-side FET and the low-side FET can impose excessive negative voltage transients on the driver during switching. Use short, low-inductance paths to connect PSW to the high-side FET source and PGND to the low-side FET source.
6. To prevent excessive ringing on the input power bus, good decoupling practices are required by placing low-ESR capacitors adjacent to the GaN FETs.

9.4.2 Layout Examples

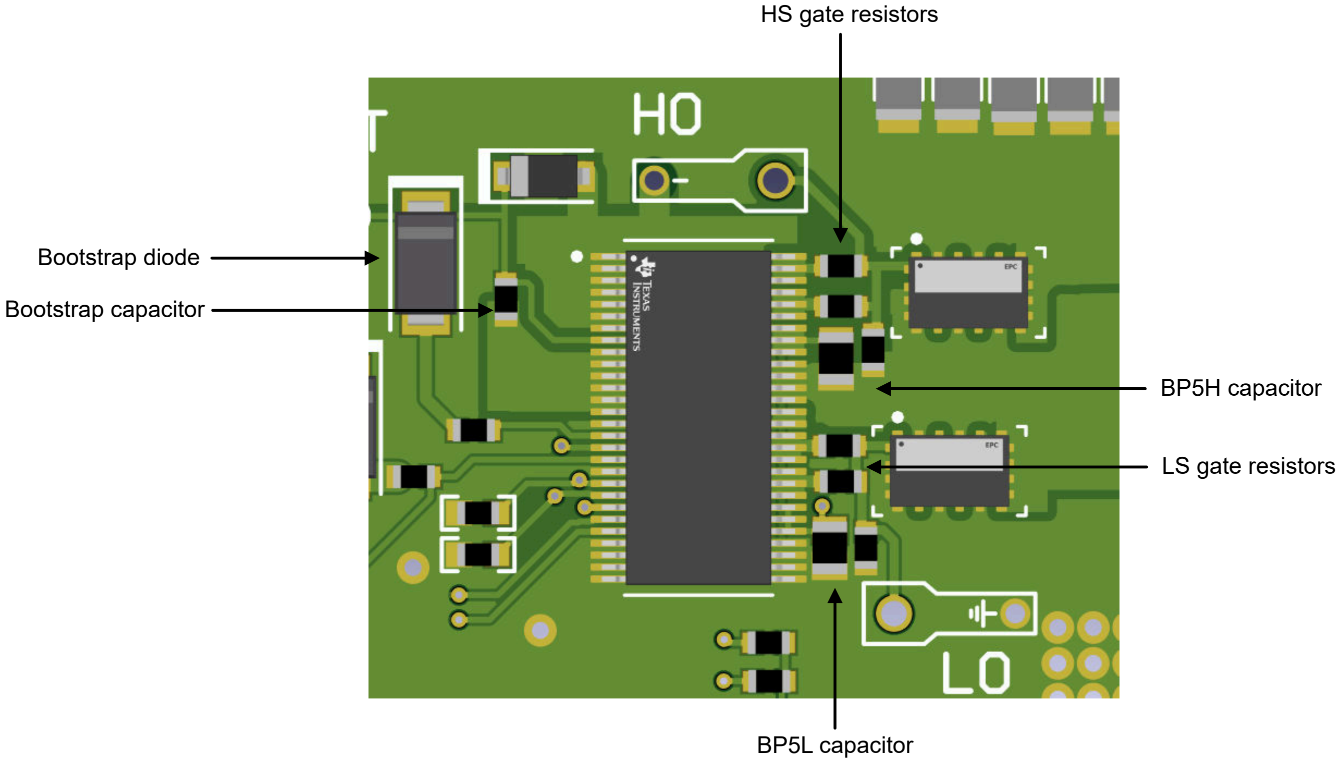


Figure 9-4. 3D View From TPS7H6005EVM

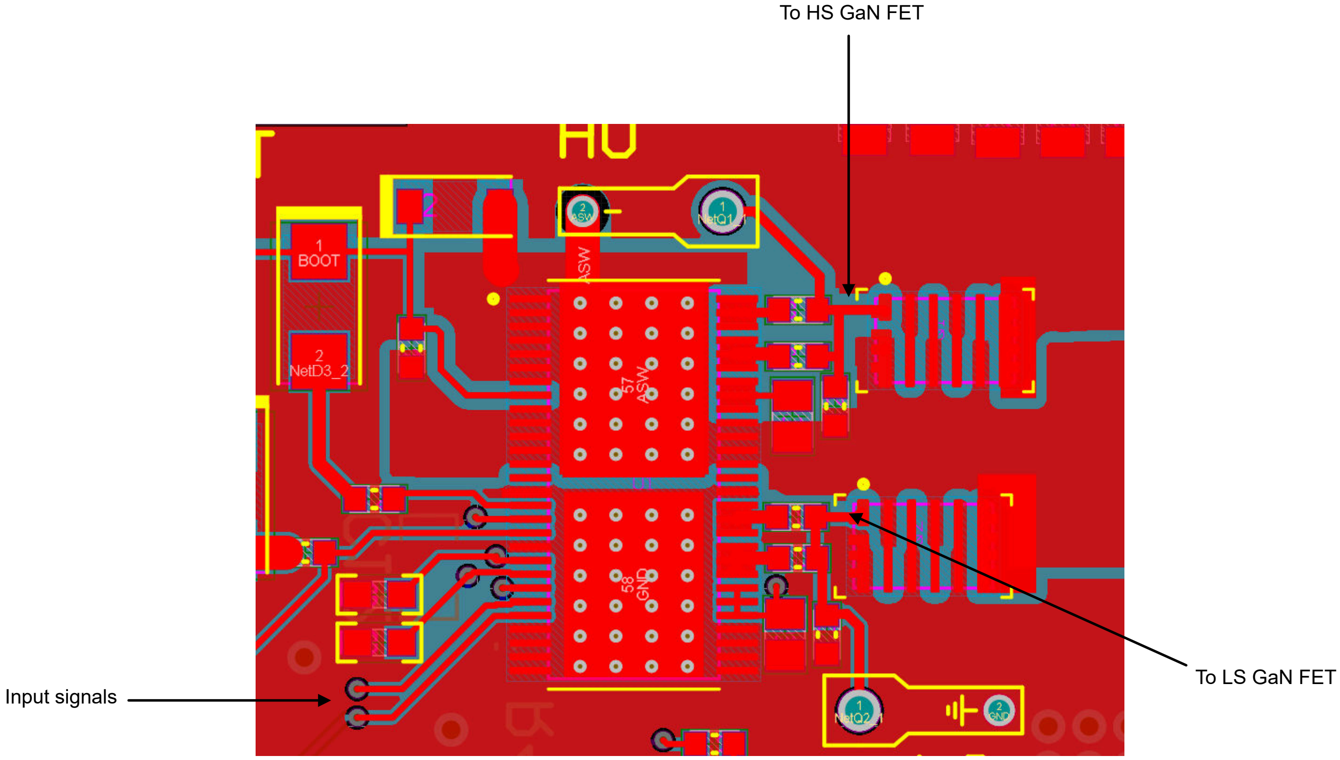


Figure 9-5. Layout Example From TPS7H6005EVM

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7H6005EVM Evaluation Module user's guide*
- Texas Instruments, *TPS7H60x5-SEP Single Event Effects radiation report*
- Texas Instruments, *TPS7H60x5-SP Single Event Effects radiation report*
- Texas Instruments, *TPS7H60x5-SEP Total Ionizing Dose (TID) radiation report*
- Texas Instruments, *TPS7H6005-SP Total Ionizing Dose (TID) radiation report*
- Texas Instruments, *TPS7H60x5 Neutron Displacement Damage radiation report*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2025) to Revision C (April 2025) — Page

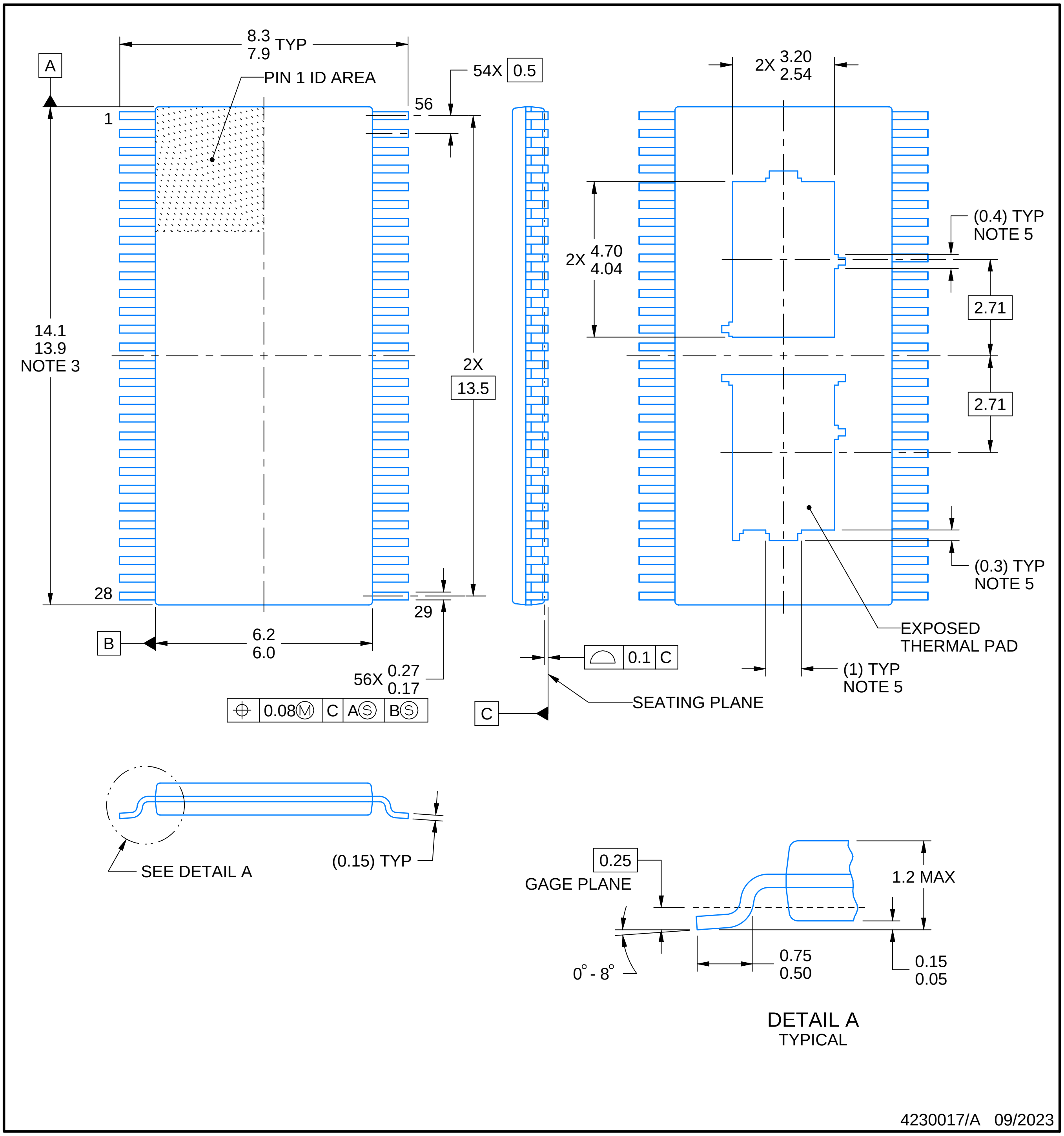
- Changed TPS7H6005-SP, TPS7H6015-SP, and TPS7H6025-SP devices From: *Product Preview* To: *Production Data* 1
- Updated rating for Electrostatic discharge human-body model (HBM) from ±1000V to ±2000V.......... 8
- Updated rating for Electrostatic discharge charged-device model (CDM) from ±250V to ±500V.......... 8

Changes from Revision A (December 2024) to Revision B (February 2024) — Page

- Changed TPS7H6015-SEP and TPS7H6025-SEP devices From: *Advance Information* To: *Production Data* . 1

12 Mechanical, Packaging, and Orderable Information

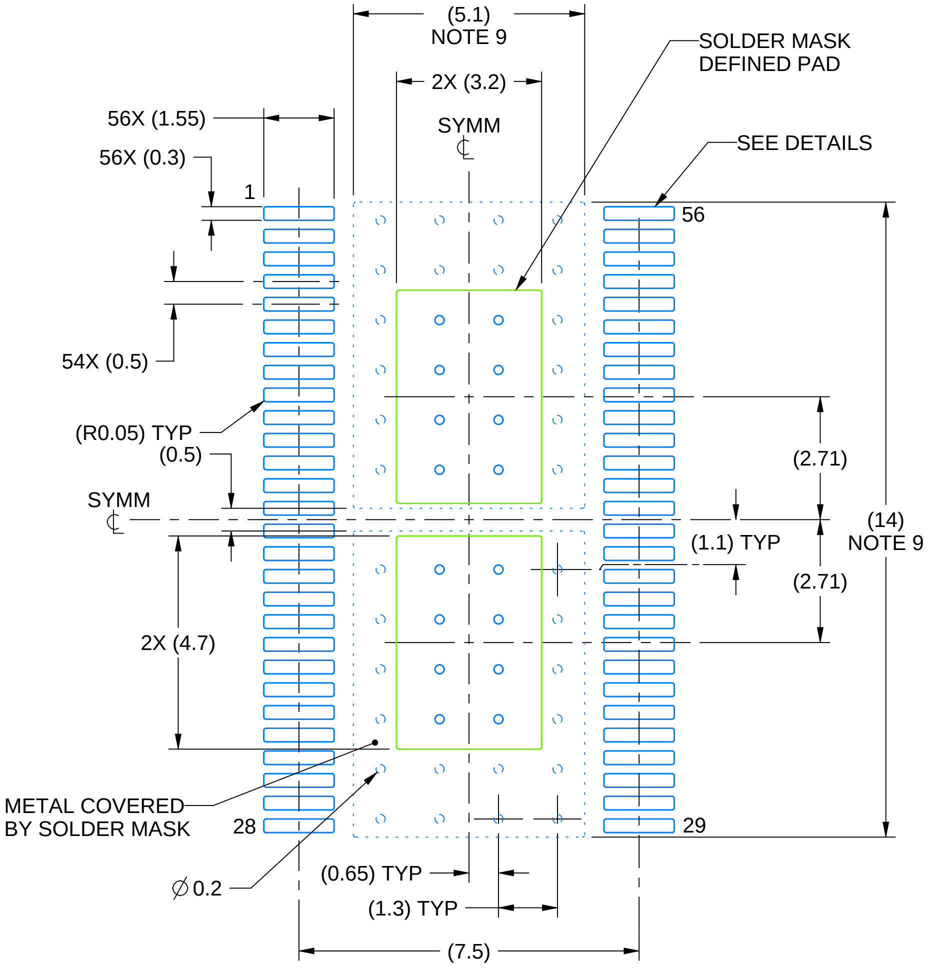
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



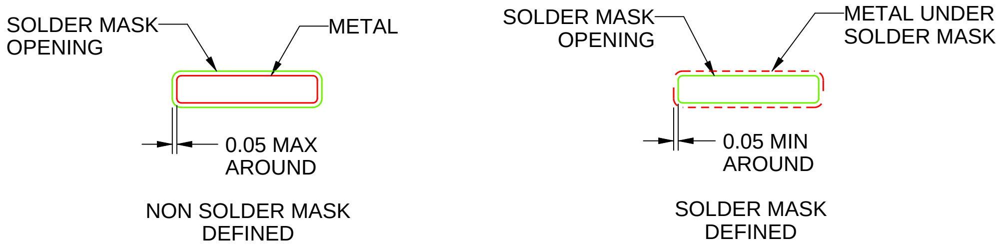
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not present.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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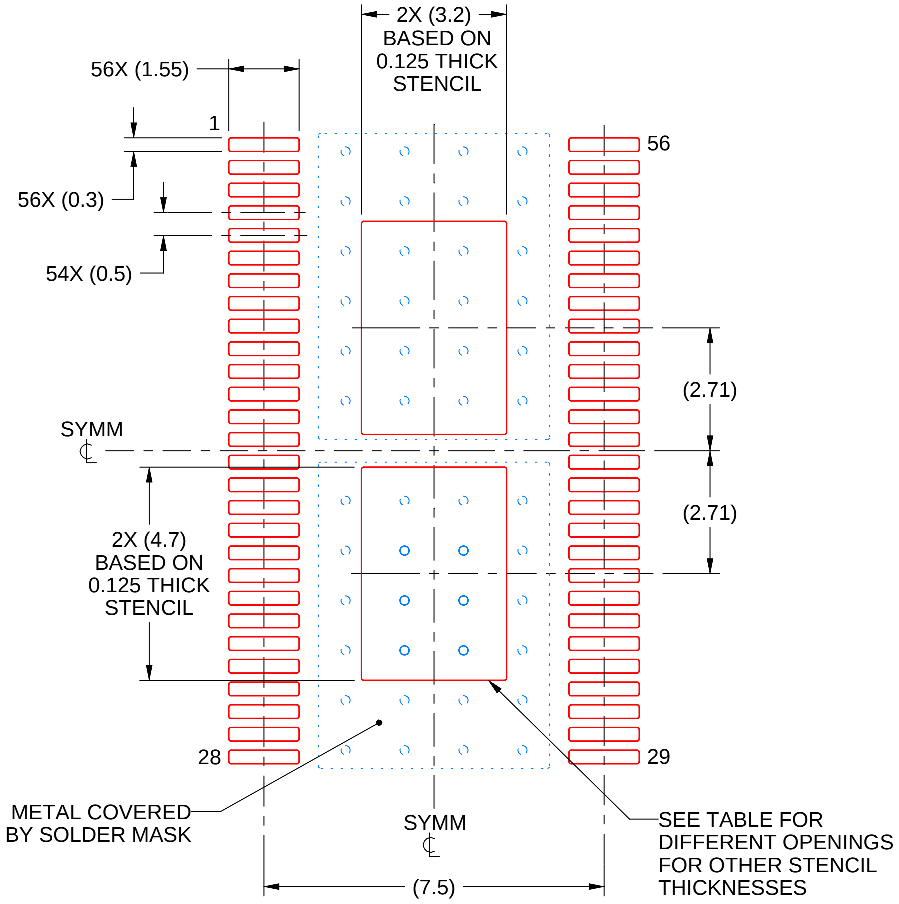
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.58 X 5.25
0.125	3.20 X 4.70 (SHOWN)
0.15	2.92 X 4.29
0.175	2.70 X 3.97

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R2220104PYE	Active	Production	HTSSOP (DCA) | 56	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	R2220104PYE
5962R2220105PYE	Active	Production	HTSSOP (DCA) | 56	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	R2220105PYE
5962R2220106PYE	Active	Production	HTSSOP (DCA) | 56	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	R2220106PYE
TPS7H6005MDCATSEP	Active	Production	HTSSOP (DCA) | 56	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H6005DCA
TPS7H6015MDCATSEP	Active	Production	HTSSOP (DCA) | 56	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H6015DCA
TPS7H6025MDCATSEP	Active	Production	HTSSOP (DCA) | 56	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H6025DCA
V62/24632-01XE	Active	Production	HTSSOP (DCA) | 56	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H6005DCA
V62/24632-02XE	Active	Production	HTSSOP (DCA) | 56	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H6015DCA
V62/24632-03XE	Active	Production	HTSSOP (DCA) | 56	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H6025DCA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS7H6005-SEP, TPS7H6005-SP, TPS7H6015-SEP, TPS7H6015-SP, TPS7H6025-SEP, TPS7H6025-SP :

- Catalog : TPS7H6005-SEP, TPS7H6015-SEP, TPS7H6025-SEP

- Space : TPS7H6005-SP, TPS7H6015-SP, TPS7H6025-SP

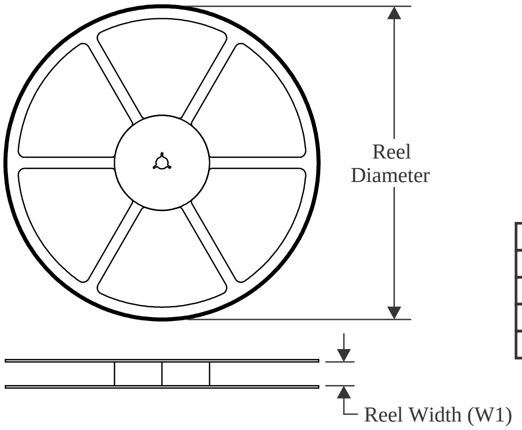
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

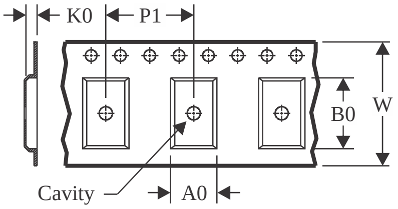
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

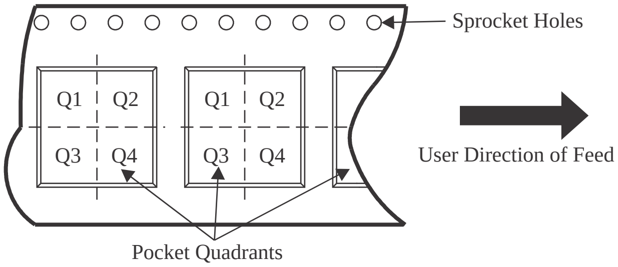


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

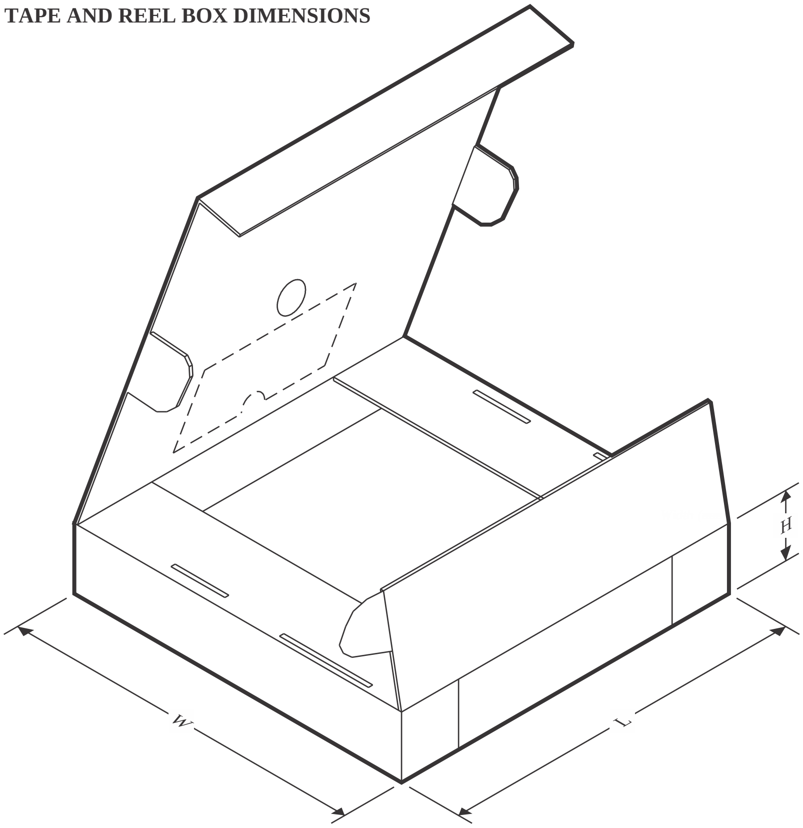
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
5962R2220104PYE	HTSSOP	DCA	56	250	178.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1
5962R2220105PYE	HTSSOP	DCA	56	250	178.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1
5962R2220106PYE	HTSSOP	DCA	56	250	178.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1
TPS7H6005MDCATSEP	HTSSOP	DCA	56	250	178.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1
TPS7H6015MDCATSEP	HTSSOP	DCA	56	250	178.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1
TPS7H6025MDCATSEP	HTSSOP	DCA	56	250	178.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
5962R2220104PYE	HTSSOP	DCA	56	250	223.0	191.0	55.0
5962R2220105PYE	HTSSOP	DCA	56	250	223.0	191.0	55.0
5962R2220106PYE	HTSSOP	DCA	56	250	223.0	191.0	55.0
TPS7H6005MDCATSEP	HTSSOP	DCA	56	250	223.0	191.0	55.0
TPS7H6015MDCATSEP	HTSSOP	DCA	56	250	223.0	191.0	55.0
TPS7H6025MDCATSEP	HTSSOP	DCA	56	250	223.0	191.0	55.0

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