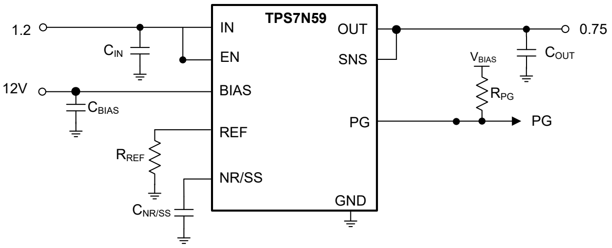
TPS7N59 10A, Low-V_{IN}, Low-Noise, High-Accuracy, Ultra-Low Dropout (LDO) Voltage Regulator

1 Features

- Input voltage range: 0.7V to 6.0V
- Output voltage noise: 2.5µV_{RMS}
- 1% (max) accuracy over line, load, and temperature
- Low dropout: 150mV (typ) at 10A
- Power-supply rejection ratio (10A):
  - 84dB at 1kHz
  - 64dB at 10kHz
  - 49dB at 100kHz
  - 30dB at 1MHz
- Excellent load transient response:
  - ±20mV with a 10mA to 10A load step
- Adjustable output voltage range: 0.5V to 5.2V
- Adjustable soft-start inrush control
- BIAS rail: 3V to 12V external rail
- Open-drain, power-good (PG) output
- Package: 4mm × 4mm, 24-pin WQFN
  - EVM $R_{\theta JA}$: 14.3°C/W

2 Applications

- Hardware accelerator & GPU card/module
- Optical & copper CPE
- High performance computing
- Ultrasound scanners
- Lab and field instrumentation
- Sensor, imaging, and radar



Typical Application Circuit

3 Description

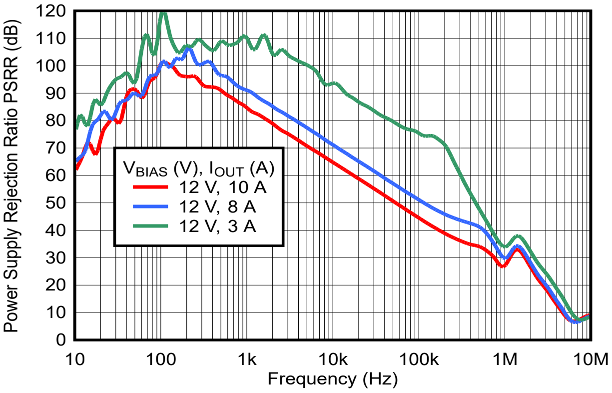
The TPS7N59 is a low-noise (2.5µV_{RMS}), ultra-low-dropout linear regulator (LDO) capable of sourcing 10A with only 150mV of dropout, independently of the output voltage. The device output voltage is adjustable from 0.5V to 5.2V using a single external resistor. The combination of low noise, high PSRR (30 dB at 1MHz), and high output-current capability makes the TPS7N59 designed for powering noise-sensitive components (such as RF amplifiers, radar sensors, SERDES and analog chipsets) found in radar power, communication, and imaging applications.

Digital loads [such as application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and digital signal processors (DSPs)] requiring low-input, low-output (LILO) voltage operation also benefit from the exceptional accuracy (1% over load, line, and temperature), remote sensing, excellent transient performance, and soft-start capabilities to provide good system performance. The versatility, performance, and small footprint solution make this LDO an excellent choice for high-current analog loads such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and imaging sensors as well as digital loads such as serializer/deserializers (SerDes), FPGAs, and DSPs.

Package Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE
TPS7N59	RTW (WQFN, 24)	4.00mm × 4.00mm

(1) For more information, see Section 10.



PSRR vs I_{OUT}, 1.15V_{IN}, 0.75V_{OUT}

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4 Pin Configuration and Functions

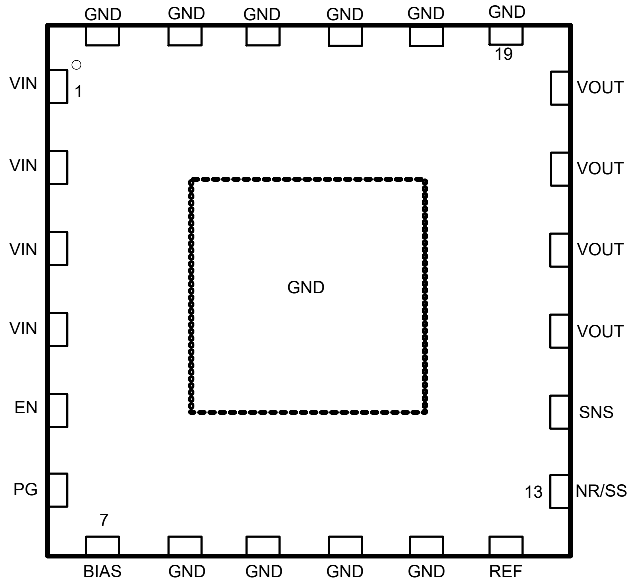


Figure 4-1. RTW Package, 24-Pin WQFN (Top View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BIAS	7	I	BIAS supply voltage pin.
EN	5	I	Enable pin. See the *Precision Enable and UVLO* section for additional information.
GND	8, 9, 10, 11, 19, 20, 21, 22, 23, 24	GND	Ground pin. See the *Layout Guidelines* section for additional information.
IN	1, 2, 3, 4	I	Input supply voltage pin. See the *Input and Output Capacitor Requirements (C_{IN} and C_{OUT})* section for more details.
NR/SS	13	I/O	Noise-reduction pin. See the *Programmable Soft-Start* and *Soft-Start, Noise Reduction (NR/SS Pin), and Power-Good (PG Pin)* sections for additional information.
OUT	15, 16, 17, 18	O	Regulated output pin. See the *Output Voltage Setting and Regulation* and *Input and Output Capacitor Requirements (C_{IN} and C_{OUT})* sections for more details.
PG	6	O	Open-drain, power-good indicator pin for the low-dropout regulator (LDO) output voltage. See the *Power-Good Pin (PG Pin)* section for additional information.
REF	12	I/O	Reference pin. See the *Output Voltage Setting and Regulation* section for additional information.
SNS	14	I	Output sense pin. See the *Output Voltage Setting and Regulation* section for additional information.
Thermal Pad	—	GND	Connect the pad to GND for best possible thermal performance. See the *Layout* section for more information.

(1) I = input, O = output, I/O = input or output, G = ground.

ADVANCE INFORMATION

5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range and all voltages with respect to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	BIAS	–0.3	13.2	V
	IN, PG, EN	–0.3	6.5	
	REF, SNS	–0.3	6	
	OUT	–0.3	V_{IN} + 0.3 (2)	
Current	OUT	Internally limited		A
	PG (sink current into the device)		5	mA
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The absolute maximum rating is V_{IN} + 0.3V or 6.0V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range	0.7		6	V
V_{EN}	Enable supply voltage range	0		6	V
V_{REF}	Reference voltage range	0.5		5.3	V
V_{OUT}	Output voltage range	0.5		5.2	V
V_{BIAS}	Bias voltage range	3		12.6	V
I_{OUT}	Output current	0		10	A
C_{IN}	Input capacitor	4.7	10	1000	µF
C_{OUT}	Output capacitor (1)	22	22	3000	µF
C_{OUT_ESL}	Output capacitor ESR	2		20	mΩ
Z_{OUT_ESL}	Total impedance ESL	0.2		1	nH
C_{BIAS}	Bias pin capacitor	0	1	100	µF
C_{REF}	Reference noise-reduction capacitor	0.1	4.7	10	µF
R_{PG}	Power-good pull-up resistance	10		100	kΩ
T_J	Junction temperature	–40		125	°C

(1) Effective output capacitance of 15µF minimum is required for stability. The effective output capacitance accounts for tolerance, temperature, voltage, and any other factors that affect the value.

5.4 Thermal Information

THERMAL METRIC (1)		TPS7N59		UNIT
		RTW (WQFN) (2)	RTW (WQFN) (3)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36	14.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.4	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.4	–	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.4	5.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Using New Thermal Metric application note.
(2) Evaluated using JEDEC standard (2s2p).
(3) Evaluated using EVM.

5.5 Electrical Characteristics

over operating temperature range (T_J = –40°C to +125°C), $V_{OUT(NOM)}$ = 0.5V, $V_{IN(NOM)} = V_{OUT(NOM)}$ + 0.4V, $V_{BIAS} = V_{OUT(NOM)}$ + 3.2V, I_{OUT} = 0A, V_{EN} = 1.8V, C_{IN} = 10µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, $C_{NR/SS}$ = 100nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO(IN)}$	Input supply UVLO	V_{IN} rising V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6V		0.67	0.7	V
$V_{HYS(UVLO\_IN)}$	Input supply UVLO hysteresis	V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6V		50		mV
$V_{UVLO(BIAS)}$ – V_{REF}	BIAS UVLO relative to V_{REF}	V_{BIAS} rising, 1.4V ≤ V_{REF} ≤ 5.2V		2.1	2.95	V
$V_{HYS(UVLO\_BIAS - REF)}$	BIAS UVLO relative to V_{REF} hysteresis	1.4V ≤ V_{REF} ≤ 5.2V		240		mV
$I_{NR/SS}$	NR/SS fast start-up charging current	$V_{NR/SS}$ = GND, V_{IN} = 1.1V		0.2		mA
V_{OUT}	Output voltage accuracy [1]	0.5V ≤ $V_{OUT(NOM)}$ ≤ 5.2V[1] [2], 0.9V ≤ V_{IN} ≤ 6V V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6V 0A ≤ I_{OUT} ≤ 10A	–1		1	%
I_{REF}	REF current pin	0.5V ≤ $V_{OUT(NOM)}$ ≤ 5.2V[1] [2], 0.9V ≤ V_{IN} ≤ 6V V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6V 0A ≤ I_{OUT} ≤ 10A	49.5	50	50.5	µA
V_{OS}	Output offset voltage ($V_{NR/SS}$- V_{OUT})	0.5V ≤ $V_{OUT(NOM)}$ ≤ 5.2V[1] [2], 0.9V ≤ V_{IN} ≤ 6V V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6V 0A ≤ I_{OUT} ≤ 10A	–3		3	mV
		$V_{OUT(NOM)}$ = 0.5V[1] [2], V_{IN} = 0.9V V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6V I_{OUT} = 0A	–1		1	
$\Delta I_{REF(\Delta VBIAS)}$	Line regulation: ΔI_{REF}	V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6V, V_{IN} = 0.7V, V_{OUT} = 0.5V, I_{OUT} = 0A		0.15		nA/V
$\Delta V_{OS(\Delta VBIAS)}$	Line regulation: ΔV_{OS}	V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6V, V_{IN} = 0.7V, V_{OUT} = 0.5V, I_{OUT} = 0A		0.06		µV/V
$\Delta I_{REF(\Delta VIN)}$	Line regulation: ΔI_{REF}	0.7V ≤ V_{IN} ≤ 6V, V_{OUT} = 0.5V, I_{OUT} = 0A, V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6V		0.03		nA/V
$\Delta V_{OS(\Delta VIN)}$	Line regulation: ΔV_{OS}	0.7V ≤ V_{IN} ≤ 6V, V_{OUT} = 0.5V, I_{OUT} = 0A, V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6V		0.01		µV/V
$\Delta V_{OS(\Delta IOUT)}$	Load regulation: ΔV_{OS}	V_{IN} = 0.9V, V_{OUT} = 0.5V, 0A ≤ I_{OUT} ≤ 10A, [2] V_{BIAS} = V_{OUT} + 3.2V		5		µV/A
	Change in I_{REF} vs V_{REF}	0.5V ≤ V_{REF} ≤ 5.2V, V_{IN} = 6V, I_{OUT} = 0A, V_{BIAS} = V_{OUT} + 3.2V		4.4		nA
	Change in V_{OS} vs V_{REF}			0.25		mV
V_{DO}	Dropout voltage [3]	0.72V ≤ V_{IN} ≤ 5.3V, I_{OUT} = 10A, V_{BIAS} = V_{OUT} + 3.2V, –40°C ≤ T_J ≤ +125°C		150	220	mV
I_{LIM}	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(NOM)}$, $V_{OUT(NOM)}$ = 5.2V, V_{IN} = $V_{OUT(NOM)}$ + 400mV, V_{BIAS} = V_{OUT} + 3.2V	10.5	11.6	12.8	A
I_{SC}	Short circuit current limit	R_{LOAD} = 10mΩ, under foldback operation		9.9		A
I_{BIAS}	BIAS pin current	V_{IN} = 6V, I_{OUT} = 0A, V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6V V_{OUT} = 5.2V	1	1.5	2	mA
I_{GND}	GND pin current	V_{IN} = 6V, I_{OUT} = 0A, V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6V V_{OUT} = 5.2V	3.5	5	6.5	mA
I_{SDN}	Shutdown GND pin current	PG = (open), V_{IN} = 6V, V_{EN} = 0.4V, V_{BIAS} = 12.6V		150	450	µA
I_{EN}	EN pin current	V_{IN} = 6V, 0V ≤ V_{EN} ≤ 6V	-5		5	µA
$V_{IH(EN)}$	EN trip point rising (turn-on)	V_{IN} = 1.1V V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6	0.62	0.65	0.68	V
$V_{HYS(EN)}$	EN trip point hysteresis	V_{IN} = 1.1V V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 12.6		40		mV
$V_{IT(PG)}$	PG pin threshold	For PG transitioning low with falling V_{OUT}, V_{IN} = 1.1V, V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1mA (current into device)	87	90	93	%
$V_{HYS(PG)}$	PG pin hysteresis	V_{IN} = 1.1V, V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1mA (current into device)		2		%
$V_{OL(PG)}$	PG pin low-level output voltage	V_{IN} = 1.1V, V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1mA (current into device)			0.4	V
$I_{LKG(PG)}$	PG pin leakage current	V_{PG} = 6V, V_{OUT} > $V_{IT(PG)}$, V_{IN} = 1.1V			1	µA

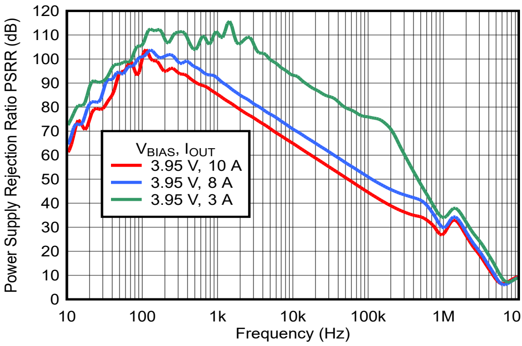
over operating temperature range (T_J = –40°C to +125°C), $V_{OUT(NOM)}$ = 0.5V, $V_{IN(NOM)}$ = $V_{OUT(NOM)}$ + 0.4V, V_{BIAS} = $V_{OUT(NOM)}$ + 3.2V, I_{OUT} = 0A, V_{EN} = 1.8V, C_{IN} = 10µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, $C_{NR/SS}$ = 100nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power-supply ripple rejection	f = 1MHz, V_{IN} = 1.1V, $V_{OUT(NOM)}$ = 0.75V, V_{BIAS} = V_{OUT} + 3.2V, I_{OUT} = 10A, $C_{NR/SS}$ = 4.7 µF		40		dB
V_n	Output noise voltage	BW = 10Hz to 100kHz, V_{IN} = 0.9V, V_{OUT} =0.5V, I_{OUT} = 10A, $C_{NR/SS}$ = 4.7µF, V_{BIAS} = V_{OUT} + 3.2V		2.5		μV_{RMS}
	Noise spectral density	f = 100Hz, V_{IN} = 0.9V, V_{OUT} = 0.5V, I_{OUT} = 10A, $C_{NR/SS}$ = 4.7µF, V_{BIAS} = V_{OUT} + 3.2V		18		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
	Noise spectral density	f = 1kHz, V_{IN} = 0.9V, V_{OUT} = 0.5V, I_{OUT} = 10A, $C_{NR/SS}$ = 4.7µF, V_{BIAS} = V_{OUT} + 3.2V		7.3		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
	Noise spectral density	f = 10kHz, V_{IN} = 0.9V, V_{OUT} = 0.5V, I_{OUT} = 10A, $C_{NR/SS}$ = 4.7µF, V_{BIAS} = V_{OUT} + 3.2V		5.4		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
R_{DIS}	Output pin active discharge resistance	V_{IN} = 1.1V, V_{BIAS} = 0V, V_{EN} = 0V		110		Ω
R_{NR/SS_DIS}	NR/SS pin active discharge resistance	V_{IN} = 1.1V, V_{BIAS} = 0V, V_{EN} = 0V		100		Ω
$T_{SD(shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
$T_{SD(reset)}$	Thermal shutdown reset temperature	Reset, temperature decreasing		150		°C

(1) Max power dissipation of 4W.
(2) Limited by pulse max power dissipation. For $V_{OUT(NOM)}$ > 0.5V , I_{OUT} = 10A, $V_{IN(NOM)}$ = $V_{OUT(NOM)}$ + 0.4V
(3) V_{REF} = V_{IN}, V_{SNS} = 97% × $V_{REF.}$

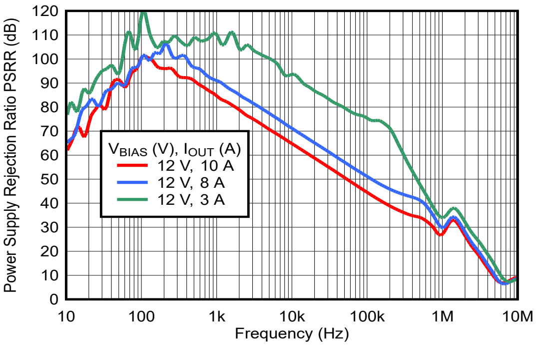
5.6 Typical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, C_{IN} = 10μF, C_{OUT} = 22μF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



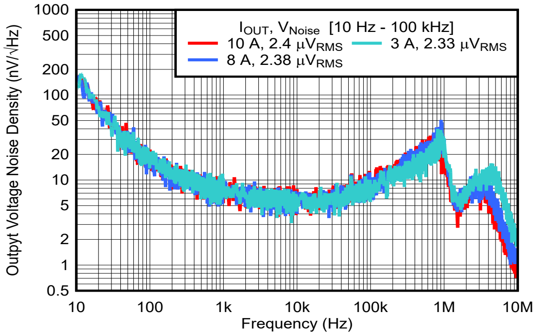
$C_{NR/SS}$ = 4.7μF, C_{OUT} = 22μF, V_{IN} = 1.15V, V_{OUT} = 0.75V

Figure 5-1. PSRR vs Frequency and I_{OUT}



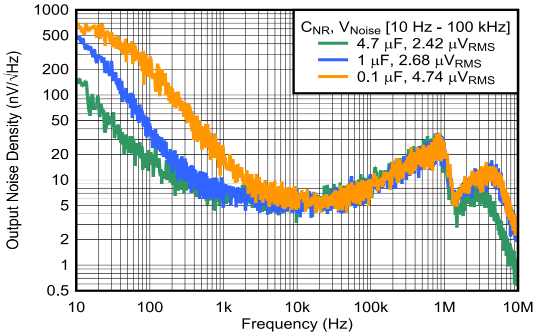
$C_{NR/SS}$ = 4.7μF, C_{OUT} = 22μF, V_{IN} = 1.15V, V_{OUT} = 0.75V

Figure 5-2. PSRR vs Frequency and I_{OUT}



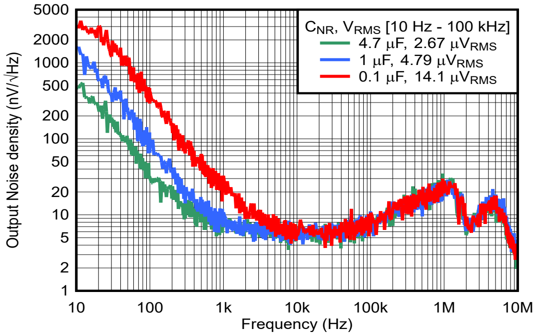
$C_{NR/SS}$ = 4.7μF, C_{IN} = 10μF, C_{OUT} = 22μF, V_{IN} = 1.15V, V_{OUT} = 0.75V

Figure 5-3. Output Voltage Noise Density vs Frequency and I_{OUT}



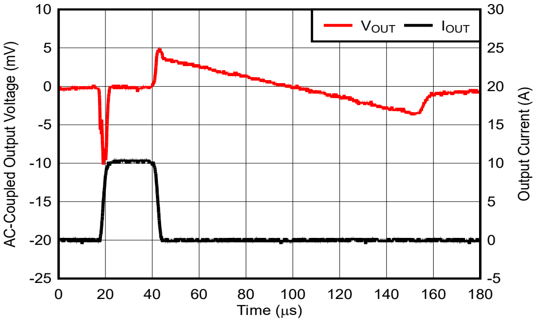
$C_{NR/SS}$ = 4.7μF, C_{IN} = 10μF, C_{OUT} = 22μF, V_{IN} = 1.15V, V_{OUT} = 0.75V, I_{OUT} = 10A

Figure 5-4. Output Voltage Noise Density vs Frequency and $C_{NR/SS}$



$C_{NR/SS}$ = 4.7μF, C_{IN} = 10μF, C_{OUT} = 22μF, V_{OUT} = 5V, I_{OUT} = 10A

Figure 5-5. Output Voltage Noise Density vs Frequency and $C_{NR/SS}$

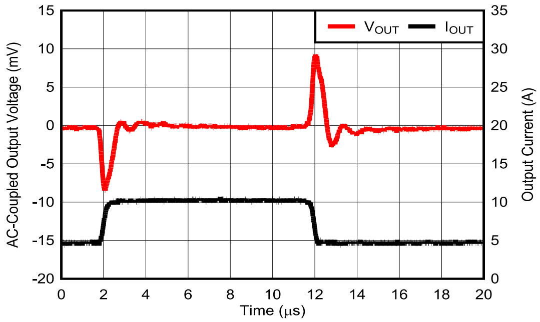


$C_{NR/SS}$ = 4.7μF, C_{IN} = 10μF, C_{OUT} = 22μF, V_{IN} = 1.15V, V_{OUT} = 0.75V, Slew Rate = 1A/μs

Figure 5-6. Load Transient for V_{OUT} = 0.75V, I_{OUT} = 0A to 10A

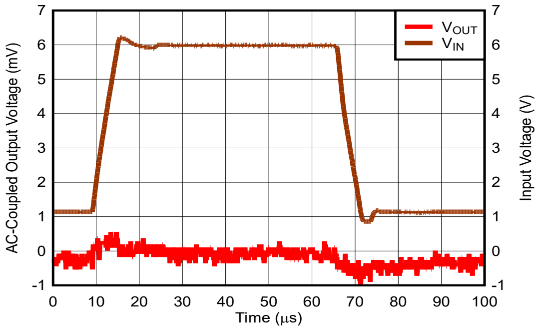
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, C_{IN} = 10µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



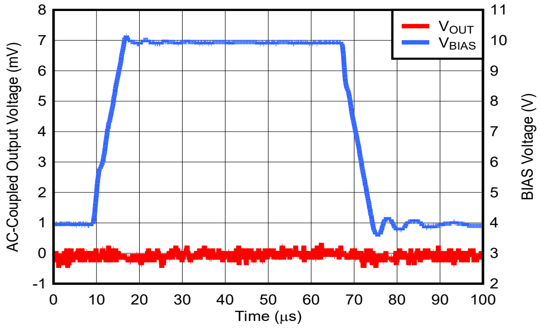
$C_{NR/SS}$ = 4.7µF, C_{IN} = 10µF, C_{OUT} = 22µF,
V_{IN} = 1.15V, V_{OUT} = 0.75V, Slew Rate = 5A/µs

Figure 5-7. Load Transient for V_{OUT} = 0.75V, I_{OUT} = 5A to 10A



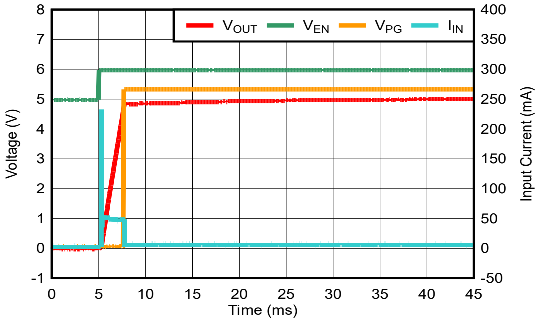
$C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF,
V_{IN} = 1.15V, V_{OUT} = 0.75V

Figure 5-8. Line Transient for V_{OUT} = 0.75V



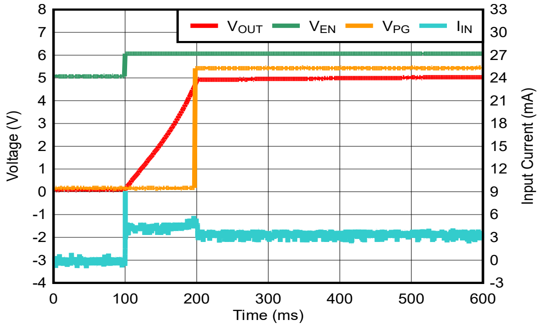
$C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF,
V_{IN} = 1.15V, V_{OUT} = 0.75V

Figure 5-9. Line Transient with V_{BIAS} for V_{OUT} = 0.75V



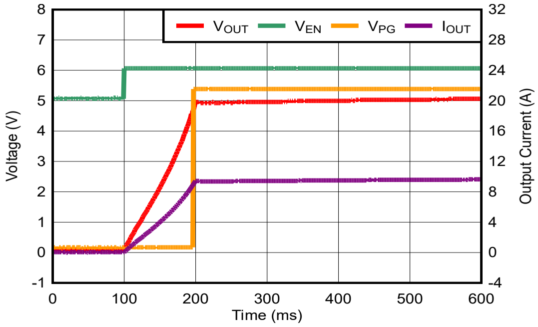
$C_{NR/SS}$ = 0.1µF, C_{IN} = 10µF, C_{OUT} = 22µF,
, V_{OUT} = 5V

Figure 5-10. Inrush Current during startup



$C_{NR/SS}$ = 4.7µF, C_{IN} = 10µF, C_{OUT} = 22µF,
, V_{OUT} = 5V

Figure 5-11. Inrush Current during startup

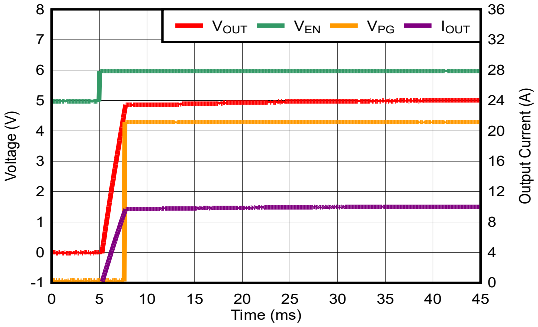


$C_{NR/SS}$ = 4.7µF, C_{IN} = 10µF, C_{OUT} = 22µF,
, V_{OUT} = 5V, I_{OUT} = 10A

Figure 5-12. Startup

5.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4V$, $V_{EN} = 1.8V$, $C_{IN} = 10\mu F$, $C_{OUT} = 22\mu F$, $C_{BIAS} = 0nF$, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



$C_{NR/SS} = 0.1\mu F$, $C_{IN} = 10\mu F$, $C_{OUT} = 22\mu F$,
, $V_{OUT} = 5V$, $I_{OUT} = 10A$

Figure 5-13. Startup

6 Detailed Description

6.1 Overview

The TPS7N59 is a low-noise (2.5µV_{RMS} over 10Hz to 100kHz bandwidth),high-accuracy (1%), ultra-low-dropout (LDO) linear voltage regulator with an input range of 0.7V to 6.0V and an output voltage range from 0.5V to 5.2V. This device uses remarkable circuitry to achieve wide bandwidth and high loop gain, resulting in ultra-high PSRR even with very low operational headroom [V_{OpHr} = (V_{IN} – V_{OUT})]. At a high level, the device has two main primary features (the current reference and the unity-gain LDO buffer) and a few secondary features (such as the adjustable soft-start inrush control, precision enable and PG pin).

The current reference is controlled by the REF pin. This pin sets the output voltage with a single resistor, the pin sets the start-up time and filters the noise generated by the reference and external R_{REF}

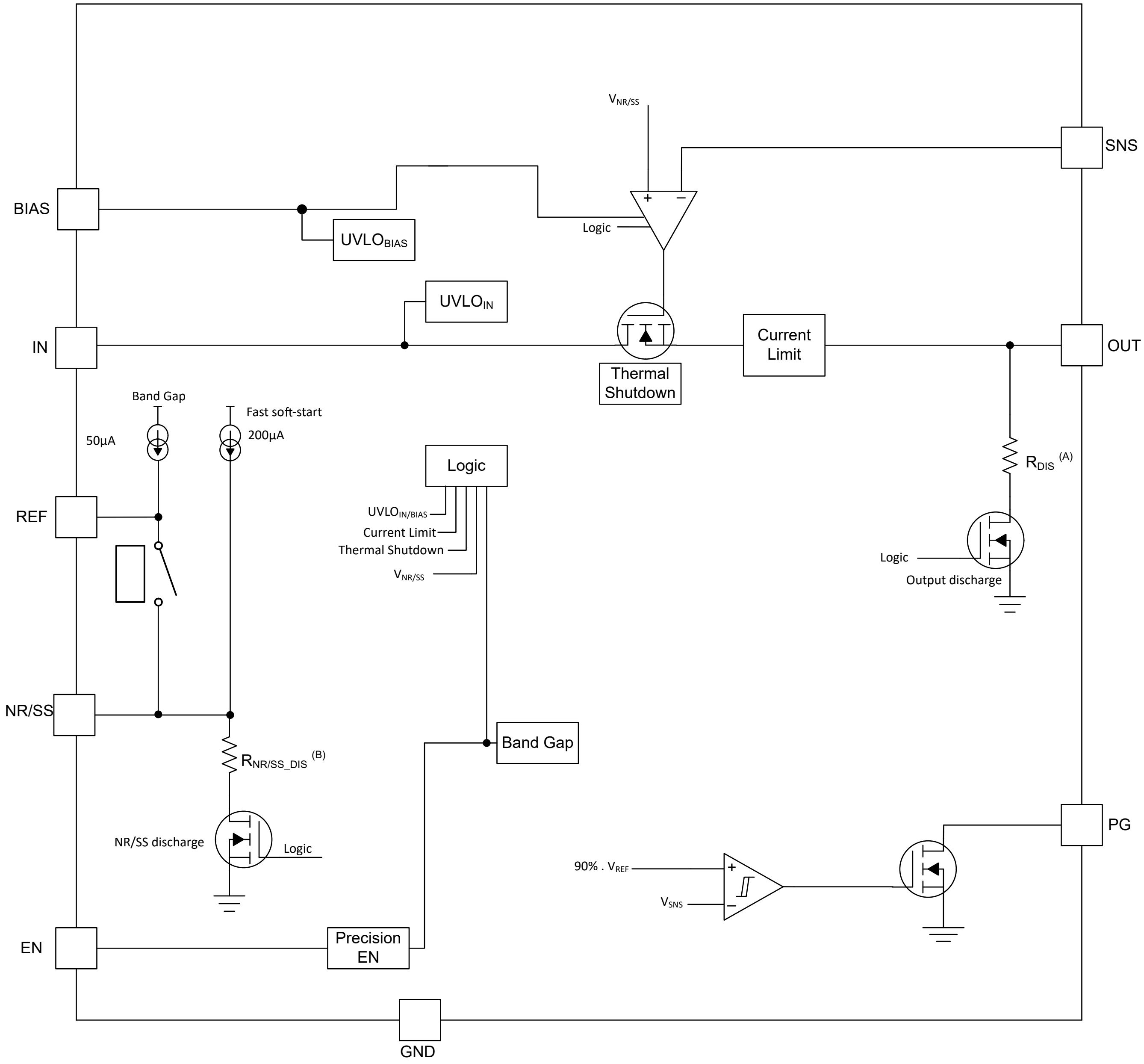
The unity-gain configuration sets the output voltage. The low noise does not increase with output voltage and provides wideband PSRR. As such, the SNS pin is only used for remote sensing of the load.

The low-noise current reference, 50µA typical, is used in conjunction with an external resistor (R_{REF}) to set the output voltage. This process allows the output voltage range to be set from 0.5V to 5.2V. To achieve low noise and allow for a soft-start inrush, an external capacitor, C_{REF} (typically 4.7µF), is placed in parallel with the R_{REF} resistor attenuating the band-gap noise. The R_{REF} resistor sets the output voltage. This unity-gain LDO provides ultra-high PSRR over a wide frequency range without compromising load and line transients.

The EN pin sets the precision enable feature; a resistor divider on this pin selects the optimal input voltage at which the device starts. There are three independent undervoltage lockout (UVLO) voltages in this device: the internal fixed UVLO thresholds for the IN and BIAS rails, and the externally adjustable UVLO threshold using the EN pin.

This regulator offers current limit, thermal protection, is fully specified from –40°C to +125°C, and is offered in a 24-pin WQFN, 4mm × 4mm thermally efficient package.

6.2 Functional Block Diagram



A. See the R_{DIS} (the output pin active discharge resistance) value in the *Electrical Characteristics* table.

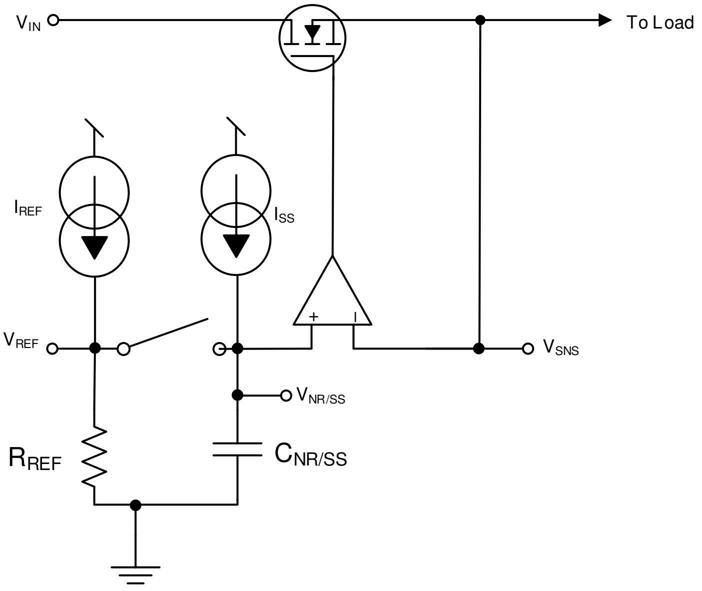
B. See the R_{NR/SS_DIS} (the NR/SS pin active discharge resistance) value in the *Electrical Characteristics* table.

6.3 Feature Description

6.3.1 Output Voltage Setting and Regulation

The simplified regulation circuit is shown in Figure 6-1, in which the input signal (V_{REF}) is generated by the internal current source (I_{REF}) and the external resistor (R_{REF}). The LDO output voltage is programmed by the V_{REF} voltage because the error amplifier is always operating in unity-gain configuration. The V_{REF} reference voltage is generated by an internal low-noise current source driving the R_{REF} resistor and is designed to have very low bandwidth at the input to the error amplifier through the use of a low-pass filter (C_{REF} || R_{REF}).

The unity-gain configuration is achieved by connecting SNS to OUT. For best performance, minimize trace inductance on the output and connect C_{OUT} as closely to the output as possible.



$V_{OUT} = I_{REF} \times R_{REF}$.

Figure 6-1. Simplified Regulation Circuit

This unity-gain configuration, along with the highly accurate I_{REF} reference current, enables the device to achieve excellent output voltage accuracy. The low dropout voltage (V_{DO}) enables reduced thermal dissipation and achieves robust performance. This combination of features make this device an excellent voltage source for powering sensitive analog low-voltage (≤ 5.5V) devices.

6.3.2 Low-Noise, Ultra-High Power-Supply Rejection Ratio (PSRR)

The device architecture features a highly accurate, high-precision, low-noise current reference followed by a state-of-the-art, complementary metal oxide semiconductor (CMOS) error amplifier ($6nV/\sqrt{Hz}$ at 10kHz noise for $V_{OUT} \geq 0.5V$). Unlike previous-generation LDOs, the unity-gain configuration of this device provides low noise over the entire output voltage range.

6.3.3 Programmable Soft-Start

The device features a programmable, monotonic, current-controlled, soft-start circuit that uses the C_{REF} capacitor to minimize inrush current into the output capacitor and load during start-up. This circuitry can also reduce the start-up time for some applications that require the output voltage to reach at least 90% of the set value for fast system start up.

6.3.4 Precision Enable and UVLO

Depending on the circuit implementation, up to three independent undervoltage lockout (UVLO) voltage circuits can be active. An internally set UVLO on the input supply (IN pin) and the bias supply (BIAS pin) automatically disables the LDO when the input voltage reaches the minimum threshold. A precision EN function (EN pin) can also be used as a user-programmable UVLO.

1. The internal input supply voltage UVLO circuit prevents the regulator from turning on when the input voltage is not high enough, see the *Electrical Characteristics* table for more details.
2. The internal bias supply voltage UVLO circuit prevents the regulator from turning on when the bias voltage is not high enough, see the *Electrical Characteristics* table for more details.
3. The precision enable circuit allows a simple sequencing of multiple power supplies with a resistor divider from another supply. This enable circuit can be used to set an external UVLO voltage at which the device is enabled using a resistor divider on the EN pin; see the *Precision Enable (External UVLO)* section for more details.

6.3.5 Power-Good Pin (PG Pin)

The PG pin is an output indicating if the LDO is ready to provide power. This pin is implemented using an open-drain architecture. During the start-up phase, the PG voltage threshold is set by the REF voltage when the fast soft-start is ongoing and is set by the NR/SS voltage when the fast soft-start is completed and the switch between REF and NR/SS is closed.

As shown in the *Functional Block Diagram*, the PG pin is implemented by comparing the SNS pin voltage to an internal reference voltage and, as such, is considered a voltage indicator reflecting the output voltage status.

6.3.6 Active Discharge

To quickly discharge internal nodes, the device incorporates two internal pulldown metal-oxide semiconductor field effect transistors (MOSFETs). The first pulldown MOSFET connects a resistor (R_{DIS}) from OUT to ground when the device is disabled to actively discharge the output capacitor. The second pulldown MOSFET connects a resistor from REF (R_{REF_DIS}) to ground when the device is disabled and discharges the REF capacitor. Both pulldown MOSFETs are activated by any of the following events:

- Driving the EN pin below the $V_{EN(LOW)}$ threshold
- The IN pin voltage falling below the undervoltage lockout $V_{UVLO(IN)}$ threshold
- The BIAS pin voltage falling below the undervoltage lockout $V_{UVLO(BIAS)}$ threshold

Note

A brownout event on BIAS during a low-input, low-output (LILO) operation (< $1.1V_{IN}$) can result in incomplete C_{REF} discharge. Consider the time constant on both the REF and OUT pins for a proper system shutdown procedure.

6.3.7 Thermal Shutdown Protection (T_{SD})

A thermal shutdown protection circuit disables the LDO when the pass transistor junction temperature (T_J) rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis verifies that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical). The thermal time constant of the semiconductor die is fairly short, thus the device can cycle off and on when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes. For reliable operation, limit the junction temperature to the maximum listed in the *Electrical Characteristics* table. Operation above this maximum temperature causes the device to exceed the operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The bias voltage is greater than the nominal output voltage plus 3.2V ($V_{OUT(nom)} + 3.2V$)
- The output current is less than the current limit ($I_{OUT} < I_{LIM}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$)
- The voltage on the EN pin has previously exceeded the $V_{IH(EN)}$ threshold voltage and has not yet decreased to less than the enable falling threshold

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} \geq V_{OUT(nom)} + V_{DO}$ and $V_{IN} \geq V_{UVLO(IN)}$	$V_{BIAS} \geq V_{OUT} + 3.2V$	$V_{EN} \geq V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{BIAS} < V_{OUT} + 3.2V$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{EN} < V_{IL(EN)}$	-	$T_J \geq T_{SD}$ for shutdown

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage minus V_{DO}. In dropout operation, the transient performance is significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

Note

Unlike traditional n-type field effect transistor (NMOS) LDOs with two supply rails, BIAS and IN, the TPS7N59 cannot enter an OUT-to-BIAS dropout mode. For proper operation, a minimum of V_{BIAS} = V_{REF}+ 3.2V is recommended to keep a voltage above UVLO(BIAS).

For additional information, see the *Undervoltage Lockout (UVLO) Operation* section.

6.4.3 Disabled

The output can be shutdown by forcing the voltage of the EN pin to less than the $V_{IH(EN)}$ threshold (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and both the NR/SS pin and OUT pin voltages are actively discharged to ground by internal discharge circuits to ground when the IN pin voltage is higher than or equal to a diode-drop voltage.

6.4.4 Current-Limit Operation

If the output current is greater than or equal to the minimum current limit ($I_{LIM(Min)}$), then the device operates in current-limit mode. Current limit is a foldback implementation.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

7.1.1 Precision Enable (External UVLO)

The precision enable circuit (EN pin) turns the device on and off. This circuit can be used to set an external undervoltage lockout (UVLO) voltage, as shown in Figure 7-1, to turn on and off the device using a resistor divider between IN (or BIAS), EN, and GND.

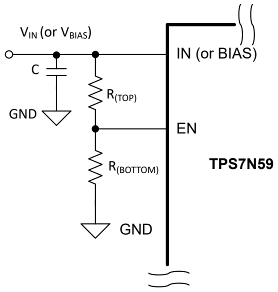


Figure 7-1. Precision EN Used as an External UVLO

This external UVLO design is used to prevent the device from turning on when the input supply voltage is not high enough and can place the device in dropout operation. This design also allows simple sequencing of multiple power supplies with a resistor divider from another supply. Another benefit from using a resistor divider to enable or disable the device is that the EN pin is never left floating because this pin does not have an internal pulldown resistor. However, a Zener diode can be needed between the EN pin and ground to comply with the absolute maximum ratings on this pin.

Use Equation 1 and Equation 2 to determine the correct resistor values.

$$V_{ON} = V_{OFF} \times [(V_{IH(EN)} + V_{HYS(EN)}) / V_{EN}] \quad (1)$$

$$R_{(TOP)} = R_{(BOTTOM)} \times (V_{OFF} / V_{IH(EN)} - 1) \quad (2)$$

where:

- V_{OFF} is the input or bias voltage where the regulator turns off
- V_{ON} is the input or bias voltage where the regulator turns on

Note

For the EN pin input current, I_{EN}, effects are ignored.

7.1.2 Undervoltage Lockout (UVLO) Operation

The TPS7N59 uses an undervoltage lockout (UVLO) circuit for both input and bias voltage. This circuit disables the output until all voltages are greater than the rising UVLO voltages.

7.1.2.1 IN Pin UVLO

The IN pin UVLO (UVLO(IN)) circuit makes sure that the device remains disabled before the input supply reaches the minimum operational voltage range, and that the device shuts down when the input supply falls too low.

The UVLO(IN) circuit has a minimum response time of several microseconds to fully assert. During this time, a downward line transient below approximately 0.67V causes the input supply UVLO(IN) to assert for a short time. However, the UVLO(IN) circuit does not have enough stored energy to fully discharge the internal circuits inside the device and can result in incomplete discharge of OUT and NR/SS capacitors.

Note

The effect of the downward line transient can trigger the overshoot prevention circuit and can be easily mitigated by using the design proposed in the *Precision Enable (External UVLO)* section.

7.1.2.2 BIAS UVLO

The BIAS pin UVLO (UVLO(BIAS)) circuit makes sure that the device remains disabled before the input supply reaches the minimum operational voltage range, and that the device shuts down when the input supply falls too low.

The UVLO(BIAS) circuit has a minimum response time of several microseconds to fully assert. During this time, a downward line transient below approximately V_{REF} + 2.1V causes the input supply UVLO(BIAS) to assert for a short time. However, the UVLO(BIAS) circuit does not have enough stored energy to fully discharge the internal circuits inside of the device and can result in incomplete discharge of the OUT and NR/SS capacitors.

Note

The effect of the downward line transient can trigger the overshoot prevention circuit and can be easily mitigated by using the design proposed in the *Precision Enable (External UVLO)* section.

7.1.2.3 Typical UVLO Operation

Figure 7-2 illustrates the UVLO (IN or BIAS) circuit response to various input voltage events. The diagram can be separated into the following regions:

- Region A: The device does not turn on until the input reaches the UVLO rising threshold.
- Region B: Normal operation with a regulated output.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output can fall out of regulation but the device is still enabled.
- Region D: Normal operation with a regulated output.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached by the input voltage and a normal start up then follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0V. The output falls because of the load and active discharge circuit.

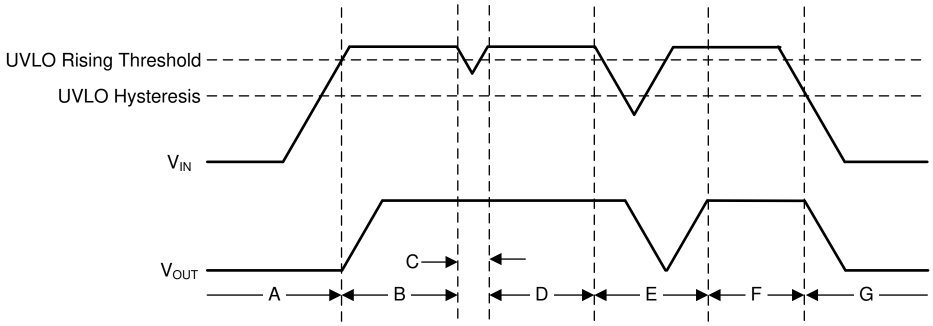


Figure 7-2. Typical UVLO Operation

7.1.3 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the minimum voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$) that is required for regulation. When V_{IN} drops to or below the set V_{DO} for the given load current, the device functions as a resistive switch and does not regulate output voltage. When the device is operating in dropout, the output voltage tracks the input voltage and the dropout voltage (V_{DO}) is proportional to the output current because the device is operating as a resistive switch. Operating the device at or near dropout significantly degrades the device transient performance and PSRR. Maintaining sufficient V_{OpHr} significantly improves the device transient performance and PSRR.

Note

If the minimum BIAS rail is set 3.2V above the REF pin voltage, the pass transistor has enough BIAS-to-OUT headroom, thus leaving only the IN-to-OUT dropout conditions to be considered. For other operating conditions, see the *Undervoltage Lockout (UVLO) Operation* section.

7.1.4 Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The TPS7N59 is designed and characterized for operation with ceramic capacitors of 22µF or greater (15µF or greater of actual capacitance) at the output and 10µF or greater (5µF or greater of actual capacitance) at the input. Use at least a 10µF capacitor at the input to minimize input impedance. Place the input and output capacitors as near as practical to the respective input and output pins to minimize trace parasitics. If the trace inductance from the input supply to the TPS7N59 is high, a fast current transient can cause V_{IN} to ring above the absolute maximum voltage rating and damage the device. This situation can be mitigated by adding additional input capacitors to dampen the ringing, thereby keeping any voltage spike below the device absolute maximum ratings.

Note

Because of the wide bandwidth, the LDO error amplifier can react faster than the output capacitor. In such a case, the load behavior appears directly on the LDO supply, potentially dragging the supply down. To avoid such behaviors, minimize both ESR and ESL present on the output; see the *Recommended Operating Conditions* table.

7.1.5 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) and low equivalent series inductance (ESL) ceramic capacitors at the input, output, and noise-reduction pins. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature and supply voltage. The use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. Make sure to derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for a capacitance derating of approximately 50%, but at high V_{IN} and V_{OUT}

conditions (V_{IN} = 5.5V to V_{OUT} = 5.0V) and temperature extremes, the derating can be greater than 50%, and must be taken into consideration. Place capacitors as close as possible to the corresponding pin and make the capacitor GND connection as close as possible to the device GND pin to shorten transient currents on the return path. Using a larger input capacitor or a bank of capacitors with various values is always good design practice to counteract input trace inductance, improve transient response

7.1.6 Soft-Start, Noise Reduction (NR/SS Pin), and Power-Good (PG Pin)

The NR/SS pin has the dual function of controlling the soft-start time and reducing the noise generated by the internal band-gap reference and the external resistor R_{REF}. The NR/SS capacitor ($C_{NR/SS}$) reduces the output noise to very low levels and sets the output ramp rate to limit inrush current.

The device features a programmable, monotonic, voltage-controlled, soft-start circuit that is set to work with an external capacitor ($C_{NR/SS}$). In addition to the soft-start feature, the $C_{NR/SS}$ capacitor also lowers the output voltage noise of the LDO. The soft-start feature can be used to eliminate power-up initialization problems. The controlled output voltage ramp also reduces peak inrush current during start up, minimizing start-up transients to the input power bus.

To achieve a monotonic start up, the device output voltage tracks the $V_{NR/SS}$ reference voltage until this reference reaches the set value (the set output voltage). The $V_{NR/SS}$ reference voltage is set by the R_{REF} resistor and, during start up, the device uses a fast charging current (I_{FAST_SS}), as shown in Figure 7-3, to charge the $C_{NR/SS}$ capacitor.

Note

Any leakage on the NR/SS and REF pins directly impacts the accuracy of the reference voltage.

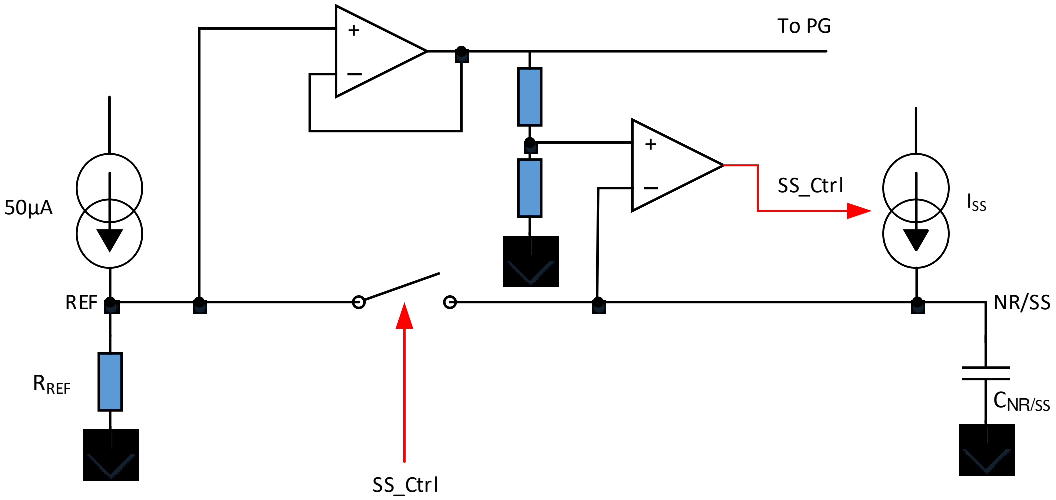


Figure 7-3. Simplified Soft-Start Circuit

The 200µA (typical) $I_{NR/SS}$ current quickly charges $C_{NR/SS}$ until the voltage reaches approximately 97% of the set output voltage, then the I_{SS} current turns off, the switch between REF and NR/SS closes, and only the I_{REF} current continues to charge $C_{NR/SS}$ to the set output voltage level.

Note

The discharge pulldown resistor on NR/SS (see the *Functional Block Diagram*) is engaged when any of the GND referenced UVLOs have been tripped, or when any faults occur (overtemp, PORs, IREF bad, or OTP error) and the NRSS pin is above 50mV.

The soft-start ramp time depends on the fast start-up ($I_{NR/SS}$) charging current, the reference current (I_{REF}), $C_{NR/SS}$ capacitor value, and the targeted output voltage ($V_{OUT(target)}$). *Equation 3* calculates the soft-start ramp time.

$$\text{Soft-start time } (t_{SS}) = (V_{OUT(target)} \times C_{NR/SS}) / (I_{SS}) \quad (3)$$

The I_{SS} current is provided in the *Typical Characteristics* section and has a value of 200µA (typical). The I_{REF} current has a value of 50µA (typical). The remaining 3% of the start-up time is determined by the $R_{REF} \times C_{NR/SS}$ time constant. Figure 7-4 shows the PG threshold at start up.

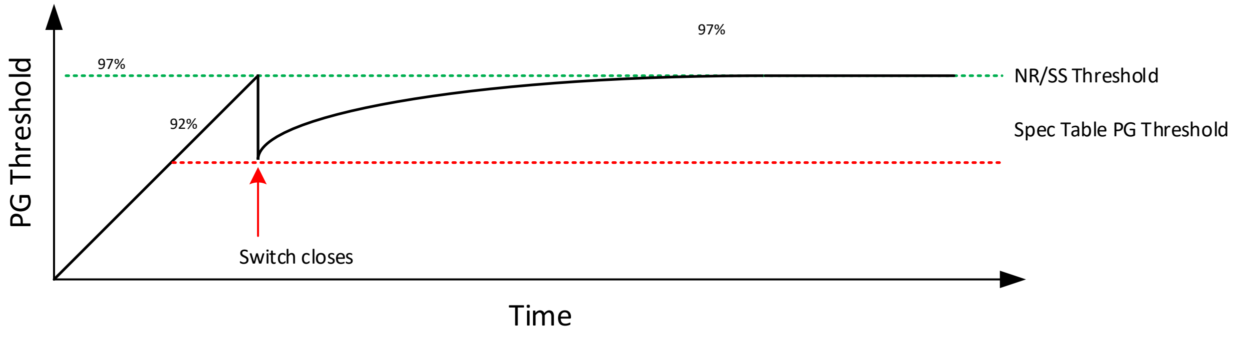


Figure 7-4. PG Threshold During Start-Up

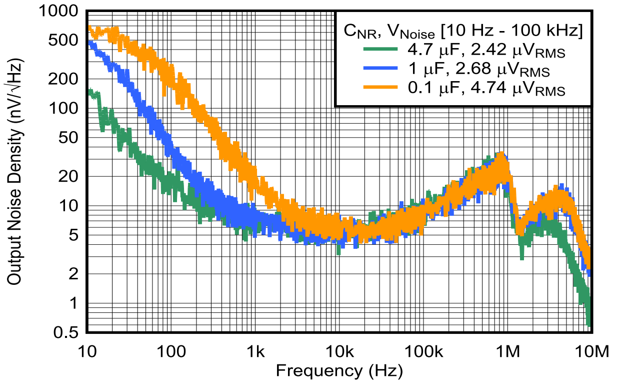
The output voltage noise can be lowered significantly by increasing the $C_{NR/SS}$ capacitor. The $C_{NR/SS}$ capacitor and R_{REF} resistor form a low-pass filter (LPF) that reduces noise from the V_{REF} voltage reference, thereby lowering the device noise floor. The LPF is a single-pole filter and Equation 4 calculates the LPF cutoff frequency. Increasing the $C_{NR/SS}$ capacitor can significantly lower output voltage noise, however, doing so lengthens start-up time. For low-noise applications, use a 4.7µF $C_{NR/SS}$ for best noise and start-up time trade off.

$$\text{Cutoff Frequency } (f_{cutoff}) = 1 / (2 \times \pi \times R_{REF} \times C_{NR/SS}) \quad (4)$$

Note

Current limit can be entered during start up with a small $C_{NR/SS}$ and large C_{OUT} because V_{OUT} no longer tracks the soft-start ramp.

Figure 7-5 show the impact of the $C_{NR/SS}$ capacitor on the LDO output voltage noise.



C_{IN} = 10µF, C_{OUT} = 22µF, V_{IN} = 1.15V, V_{OUT} = 0.75V, I_{OUT} = 10A, V_{BIAS} = 12V

Figure 7-5. Output Voltage Noise Density vs $C_{NR/SS}$

7.1.7 Optimizing Noise and PSRR

Noise can be generally defined as any unwanted signal combining with the desired signal (such as the regulated LDO output) that results in degraded power-supply source quality. Noise can be easily noticed in audio as a hissing or popping sound. Extrinsic and intrinsic are the two basic groups that noise can be categorized into. Noise produced from an external circuit or natural phenomena such as 50 to 60 hertz power-line noise (spikes), along with the harmonics, is an excellent representative of extrinsic noise. Intrinsic noise is produced by components within the device circuitry such as resistors and transistors. For this device, the two dominating sources of intrinsic noise are the error amplifier and the internal reference voltage (V_{REF}). Another term that sometimes combines with extrinsic noise is PSRR, which refers to the ability of the circuit or device to reject or filter out input supply noise and is expressed as a ratio of output voltage noise ripple to input voltage noise ripple.

Optimize the device intrinsic noise and PSRR by carefully selecting:

- $C_{NR/SS}$ for the low-frequency range up to the device bandwidth
- C_{OUT} for the high-frequency range close to and higher than the device bandwidth
- Operating headroom, V_{IN} – V_{OUT} (V_{OpHr}), mainly for the low-frequency range up to the device bandwidth, but also for higher frequencies to a less effect

The device noise performance can be significantly improved by using a larger $C_{NR/SS}$ capacitor to filter out noise coupling from the input into the device V_{REF} reference. This coupling is especially apparent from low frequencies up to the device bandwidth. The low-pass filter formed by $C_{NR/SS}$ and R_{REF} can be designed to target low-frequency noise originating in the input supply. One downside of a larger $C_{NR/SS}$ capacitor is a longer start-up time. The device unity-gain configuration eliminates the noise performance degradation that other LDOs suffer from because of the feedback network. Furthermore, increasing the device load current has little to no effect on the device noise performance.

Further improvement to the device noise at a higher frequency range than the device bandwidth can be achieved by using a larger C_{OUT} capacitor. However, a larger C_{OUT} increases inrush current and slows down the device transient response.

7.1.8 Adjustable Operation

As shown in Figure 7-6, the output voltage of the device can be set using a single external resistor (R_{REF}).

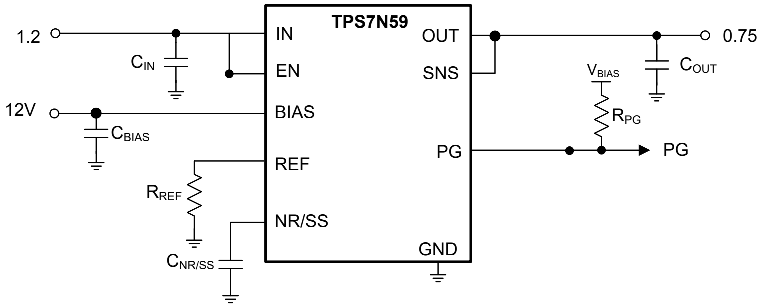


Figure 7-6. Typical Circuit

Use Equation 5 to calculate the R_{REF} value needed for the desirable output voltage.

$$V_{OUT} = I_{REF(NOM)} \times R_{REF} \quad (5)$$

Table 7-1 shows the recommended R_{REF} resistor values to achieve several common rails using a standard 1%-tolerance resistor.

Table 7-1. Recommended R_{REF} Values

TARGETED OUTPUT VOLTAGE (V)	R_{REF} (kΩ)[1]	CALCULATED OUTPUT VOLTAGE (V)
0.5	10.0	0.500
0.6	12.1	0.605
0.7	14.0	0.700
0.8	16.2	0.810
0.9	18.2	0.910
1.0	20.0	1.000
1.2	24.3	1.215
1.5	30.1	1.505
2.5	49.9	2.495
3.0	60.4	3.020
3.3	66.5	3.325
3.6	71.5	3.575
4.7	95.3	4.765
5.0	100.0	5.000

(1) 1% resistors.

7.1.9 Load Transient Response

The load-step transient response is the LDO output voltage response to load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions shown in Figure 7-7 are broken down in this section. Regions A, E, and H are where the output voltage is in steady-state regulation.

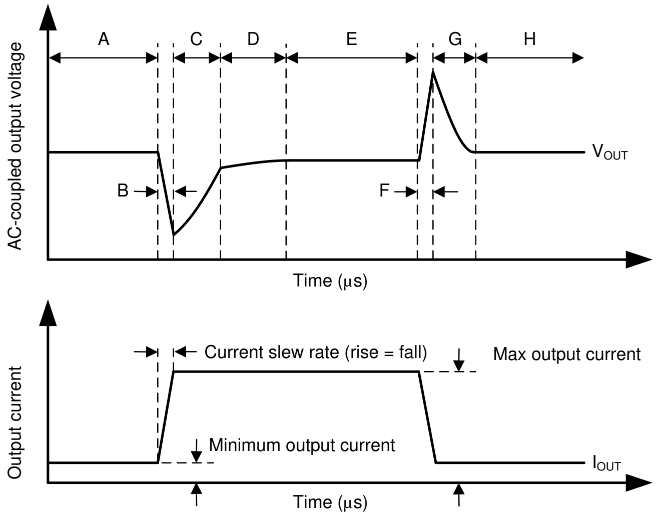


Figure 7-7. Load Transient Waveform

During transitions from a light load to a heavy load:

- The initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load:

- The initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

Transitions between current levels changes the internal power dissipation because the device is a high-current device (region D). The change in power dissipation changes the die temperature during these transitions, and leads to a slightly different voltage level. This temperature-dependent output voltage level shows up in the various load transient responses.

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

Note

The TPS7N59, with the high bandwidth, can react faster than the output capacitors. Make sure that there is sufficient capacitance at the input of the LDO.

7.1.10 Sequencing

There is no sequencing requirement between IN, BIAS, and EN.

As with devices having an internal MUX, a false PG can be triggered during shutdown if the BIAS rail is faster than the IN rail to discharge.

As shown in Figure 7-8, when the bias rail decreases below $V_{UVLO(BIAS)}$, the internal MUX between IN and BIAS switches over and the LDO is fully powered from the IN rail.

When the BIAS rail goes below UVLO(BIAS) with the IN rail greater than 1.1V, the LDO can restart because IN is still a valid condition for operations.

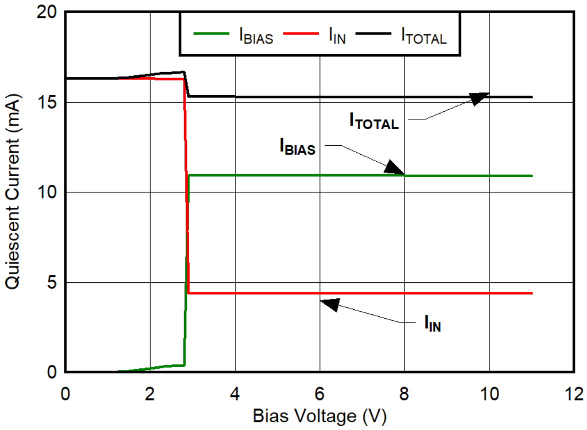


Figure 7-8. Total Quiescent Current vs BIAS

7.1.11 Power-Good Functionality

As described in the *Functional Block Diagram*, the PG pin is a open-drain MOSFET driven by a Schmitt trigger. The Schmitt trigger compares the SNS pin voltage to a preselected voltage equal to 90% that of the reference voltage.

As mentioned in the *Recommended Operating Conditions* table, the pullup resistance must be between 10kΩ and 100kΩ for best performance. If the PG functionality is not desired, the PG pin can either be left floating or connected to GND.

There are two UVLO circuits present on the BIAS rail, one referenced to GND ($V_{UVLO(BIAS)}$) and one referenced to V_{REF} ($V_{UVLO(BIAS)} – V_{REF}$). A false PG event can occur as a result of logic priorities.

To eliminate any false PG events, consider setting V_{BIAS} 3.2V above V_{OUT}.

Table 7-2 describes the various UVLO behaviors.

Table 7-2. UVLO Triggered PG Events

V_{REF}	$V_{UVLO(BIAS)} – V_{REF}$ RISING	$V_{UVLO(BIAS)} – V_{REF}$ FALLING
0.5V	2.1 + 0.5 = 2.6V	1.86 + 0.5 = 2.36V
0.7V	2.1 + 0.7 = 2.8V	1.86 + 0.7 = 2.56V
1.4V	2.1 + 1.4 = 3.5V	1.86 + 1.4 = 3.26V
5.2V	2.1 + 5.2 = 7.3V	1.86 + 5.2 = 7.06V

7.1.12 Current Mode Margining

Output voltage margining is a technique that allows a circuit to be evaluated for how well changes are tolerated in the power supply. This test is typically performed by adjusting the supply voltage to a fixed percentage above and below the nominal output voltage.

This section discusses the implementation of a voltage margining application using the TPS7N59. A margining target of ±2.5% is used to demonstrate the chosen implementation.

Figure 7-9 shows a simplified visualization of the TPS7N59 REF pin with a current DAC.

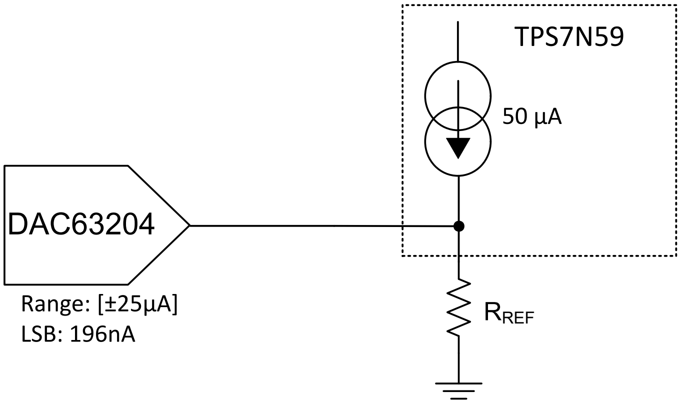


Figure 7-9. Simplified Margining Schematic

Table 7-3 summarizes the design requirements.

Table 7-3. Design Requirement

PARAMETER	Design Values
V_{IN}	2.5V
V_{OUT}	1.8V nominal with ±2.5% margining
$C_{NR/SS}$	4.7µF
R_{REF}	36kΩ
DAC I_{OUT} range	±25µA

In this example, the output voltage is set to a nominal 1.8V using 36kΩ at the REF pin to GND. Equation 6 calculates the R_{REF} resistor value.

$$R_{REF} = V_{OUT} / I_{REF} \tag{6}$$

The DAC63204, a 4-channel, 12-bit voltage and current output DAC with I^2C, is selected and programmed into the current-output mode with an output range set to ±25µA. In conjunction with the 8-bit current DAC resolution, this output range allows a minimum step size (or LSB) of approximately 196nA. Into the 36kΩ resistor, the LSB translates into a 7mV voltage resolution or 0.38% of the nominal 1.8V targeted voltage. To achieve the full ±2.5% swing around the nominal voltage, the DAC63204 must source or sink ±1.25 µA.

The current flowing through R_{REF} changes to 51.25µA and 48.75µA and adjusts the output voltage to 1.845V and 1.75V, respectively.

Figure 7-10 and Figure 7-11 show the current margining results.

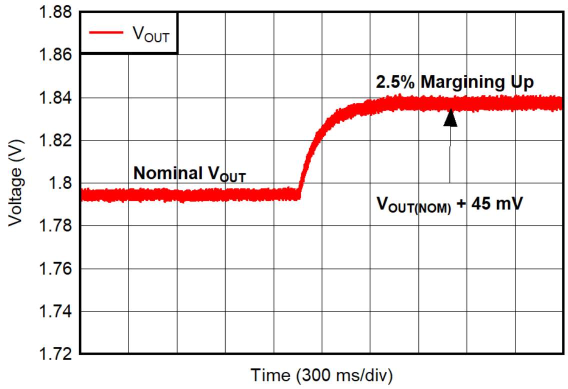


Figure 7-10. Margining Up

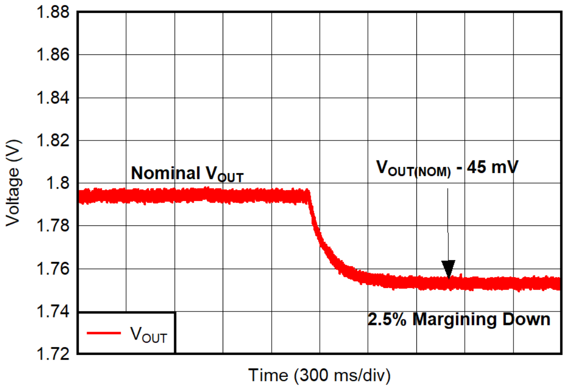


Figure 7-11. Margining Down

When implementing voltage margining with this LDO, a time constant is associated with the response. This RC time constant is a result of the parallel combination of R_{REF} and $C_{NR/SS}$, see Figure 7-9. This RC effect is illustrated in Figure 7-10 and Figure 7-11.

Equation 7 calculates the time constant for this implementation:

$$\tau = R_{REF} \times C_{NR/SS} \tag{7}$$

where:

- R_{REF} is 36kΩ
- $C_{NR/SS}$ is 4.7μF
- τ = 169ms

7.1.13 Voltage Mode Margining

Output voltage margining is a technique that allows a circuit to be evaluated for how well changes are tolerated in the power supply. This test is typically performed by adjusting the supply voltage to a fixed percentage above and below the nominal output voltage.

This section discusses the implementation of a voltage mode margining application using the TPS7N59. A margining target of ±5% is used to demonstrate the chosen implementation.

Figure 7-12 shows a simplified visualization of the TPS7N59 REF pin with a voltage DAC.

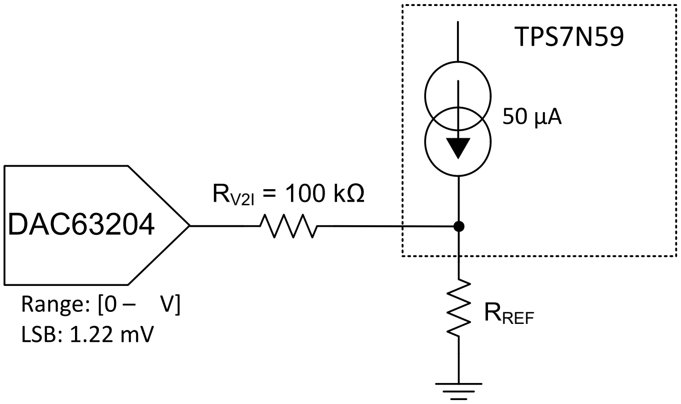


Figure 7-12. Simplified Voltage Mode Margining Schematic

Table 7-3 summarizes the design requirements.

Table 7-4. Design Requirement

PARAMETER	DESIGN VALUES
V_{IN}	2.5V
V_{OUT}	1.8V nominal with ±5% margining
$C_{NR/SS}$	4.7μF
R_{REF}	36kΩ
DAC V_{OUT} range	1.432V to 2.108V

In this example, the output voltage is set to a nominal 1.8V using a 36kΩ resistor at the REF pin to GND. Equation 8 calculates the value for the R_{REF} resistor.

$$R_{REF} = V_{OUT} / I_{REF} \quad (8)$$

The DAC63204, a 4-channel, 12-bit voltage and current output DAC with I^2C, is selected and programmed into the voltage-output mode with an output range set between 1.432V and 2.108V. In conjunction with the 12-bit voltage DAC resolution, this output range allows a minimum step size (or LSB) of approximately 1.22mV or 122μA when the voltage-to-input (V2I) conversion or R_{V2I} (100kΩ) is taken into consideration. Into the 36kΩ resistor, this LSB translates into a 0.44mV voltage resolution or approximately 0.025% of the nominal 1.8V targeted voltage. To achieve the full ±5% swing around the nominal voltage, the DAC63204 must source 3.1μA or sink 3.7μA.

The current flowing through R_{REF} changes to 53.1μA and 46.3μA, thus adjusting the output voltage to 1.88V and 1.7V respectively.

Section 7.1.13 and Figure 7-14 show the voltage margining results.

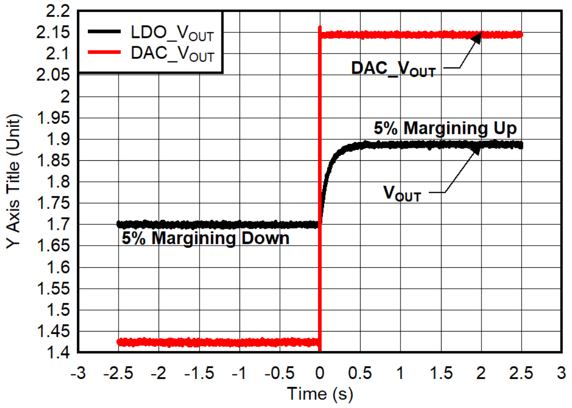


Figure 7-13. Margining From –5% to +5%

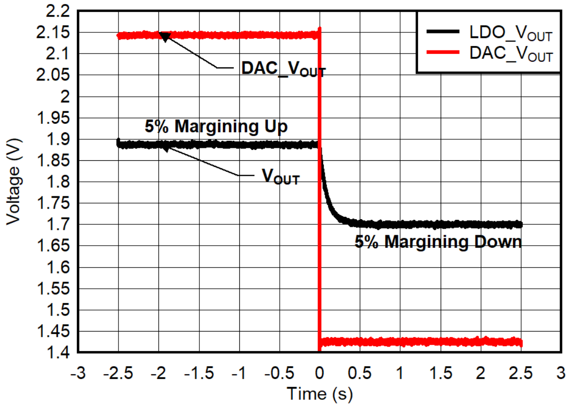


Figure 7-14. Margining From +5% to –5%

When implementing voltage margining with this LDO, there is a time constant associated with the response. This RC time constant originates from the parallel combination of R_{REF} and $C_{NR/SS}$. Section 7.1.13 and Figure 7-14 show this RC effect.

Equation 9 calculates the time constant for this implementation:

$$\tau = R_{REF} \times C_{NR/SS} \quad (9)$$

where:

- R_{REF} is 36kΩ
- $C_{NR/SS}$ is 4.7μF
- τ = 169ms

7.1.14 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 10 calculates P_D:

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \tag{10}$$

Note

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The primary heat conduction path for the package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The power dissipation through the device determines the junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 11. The equation is rearranged for output current in Equation 12.

$$T_J = T_A = (R_{\theta JA} \times P_D) \tag{11}$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \tag{12}$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the RTW package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper. Section 7.1.16 highlights the thermal performance using the TPS7N59EVM-184.

7.1.15 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 13 and are given in the *Electrical Characteristics* table.

$$\begin{aligned} \Psi_{JT}&: T_J = T_T + \Psi_{JT} \times P_D \\ \Psi_{JB}&: T_J = T_B + \Psi_{JB} \times P_D \end{aligned} \tag{13}$$

where:

- P_D is the power dissipated as explained in Equation 10
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

7.1.16 TPS7N58EVM-184 Thermal Analysis

The TPS7N59EVM-184 is used to develop the TPS7N59 thermal model. The RTW package is a 4mm × 4mm, 24-pin WQFN. The PCB is an 8 layer board of 2oz copper. Table 7-5 lists the layer stackup for the EVM.

Table 7-5. TPS7N59EVM-184 PCB Stackup

LAYER	NAME	MATERIAL	THICKNESS (mil)
1	Top overlay	—	—
2	Top solder	Solder resist	0.4
3	Top layer	Copper	1.38
4	Dielectric 1	PP-006	7.17
5	Layer 1	Copper	1.38
6	Dielectric 2	PP-006	7.17
7	Layer 2	Copper	1.38
8	Dielectric 3	PP-006	7.17
9	Layer 3	Copper	1.38
10	Dielectric 4	FR-4 high Tg	7.17
11	Layer 4	Copper	1.37
12	Dielectric 5	PP-006	7.17
13	Layer 5	Copper	1.38
14	Dialectric 6	PP-006	7.17
15	Layer 6	Cooper	1.38
16	Dialectric 7	PP-006	7.17
17	Bottom layer	Cooper	1.38
18	Bottom solder	Solder resist	0.4
19	Bottom overlay	—	—

Table 7-6 shows thermal results for the TPS7N59EVM-184. Figure 7-15 and Figure 7-16 show the thermal gradient on the PCB and device that results when a 1W power dissipation is used through the pass transistor with a 25°C ambient temperature.

Table 7-6. TPS7N59EVM-184 Thermal Results

DUT	$R_{\theta JA}$(°C/W)	Ψ_{JB}(°C/W)	Ψ_{JT}(°C/W)
TPS7N59EVM-184 (Simulation)	15	5.3	0.4
TPS7N59EVM-184 (Bench)	14.3		

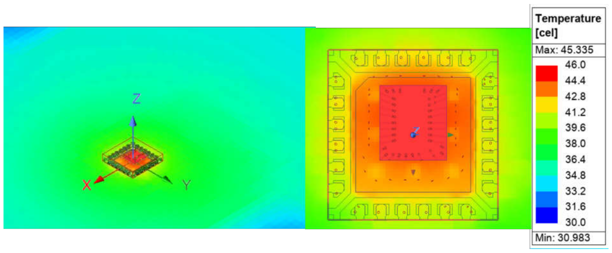


Figure 7-15. TPS7N59EVM-184 Thermal Simulation Gradient

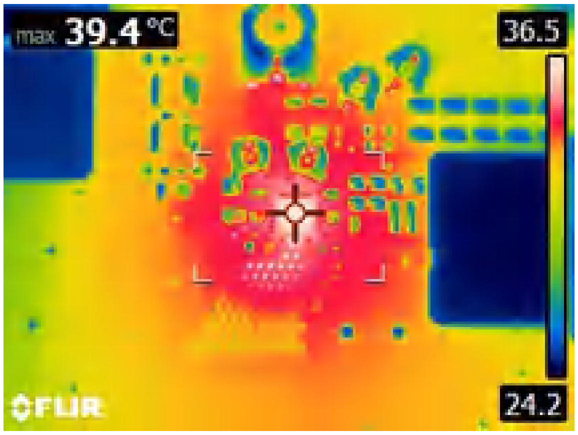


Figure 7-16. TPS7N59EVM-184 Bench Measurement Gradient

7.2 Typical Application

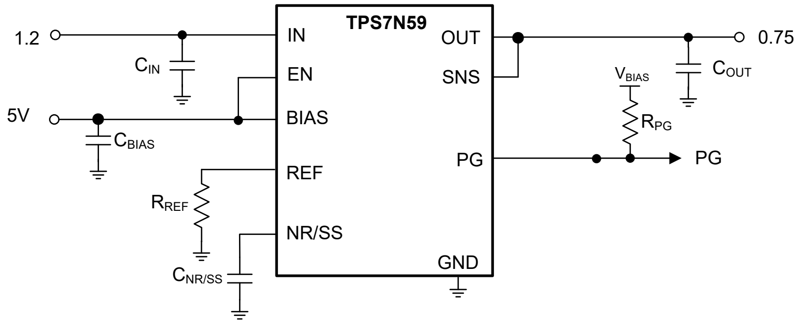


Figure 7-17. Typical Application Schematic

7.2.1 Design Requirements

Table 7-7 lists the required application parameters for this design example.

Table 7-7. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.2V, ±3%, provided by the dc/dc converter
Bias voltage	5V or 12V
Output voltage	0.75V, 1%
Output current	10A (maximum), 8A (minimum)
Noise	Less than 5µV_{RMS}
Maximum load transient	-10mV, 100mA to 10A
Start-up environment	Start-up time < 15ms

7.2.2 Detailed Design Procedure

In this design example, the device is powered by a dc/dc convertor. The load requires a 0.75V clean rail with less than 5µV_{RMS}. The typical 10µF and 22µF input and output capacitors and 4.7µF NR/SS capacitors are used to achieve a good balance between fast start-up time and excellent noise, and PSRR performance and load transient.

The output voltage is set using a 15kΩ, thin-film resistor value calculated as described in the *Output Voltage Setting and Regulation* section. The PG pin is not used and is thus connected to ground to help with thermals. The enable voltage is provided by a external I/O. Figure 7-19 illustrates that the device meets all design noise requirements. Figure 7-20 depicts adequate PSRR performance.

As illustrated in Figure 7-18, the load transient is adequate to the power-supply requirement.

Figure 7-17 depicts the implementation of these components.

7.2.3 Application Curves

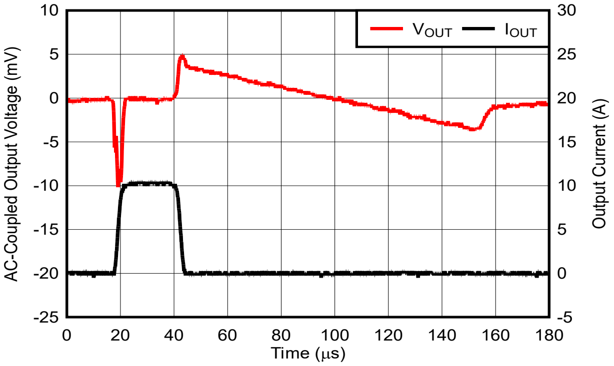


Figure 7-18. Load Transient

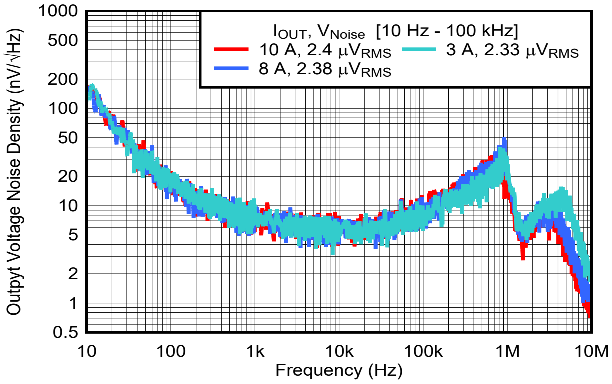


Figure 7-19. Noise vs Frequency

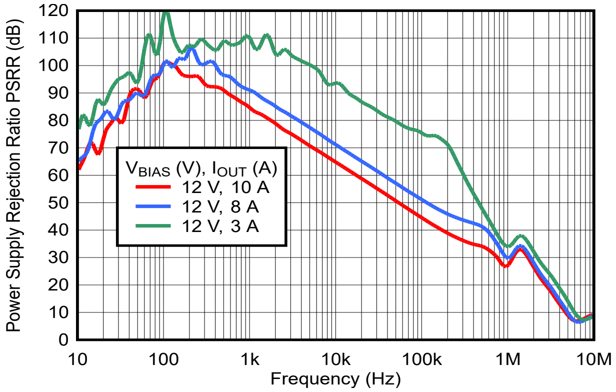


Figure 7-20. PSRR vs Frequency

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply ranging from 0.7V to 6.0V and a BIAS rail up to 12.6V. Verify that the input voltage range provides adequate operational headroom for the device to have a regulated output. This input supply must be well regulated and low impedance. If the input supply is noisy, use additional input capacitors with low ESR and increase the operating headroom to achieve the desired output noise, PSRR, and load transient performance.

There is no sequencing requirement between IN, BIAS, and EN.

7.4 Layout

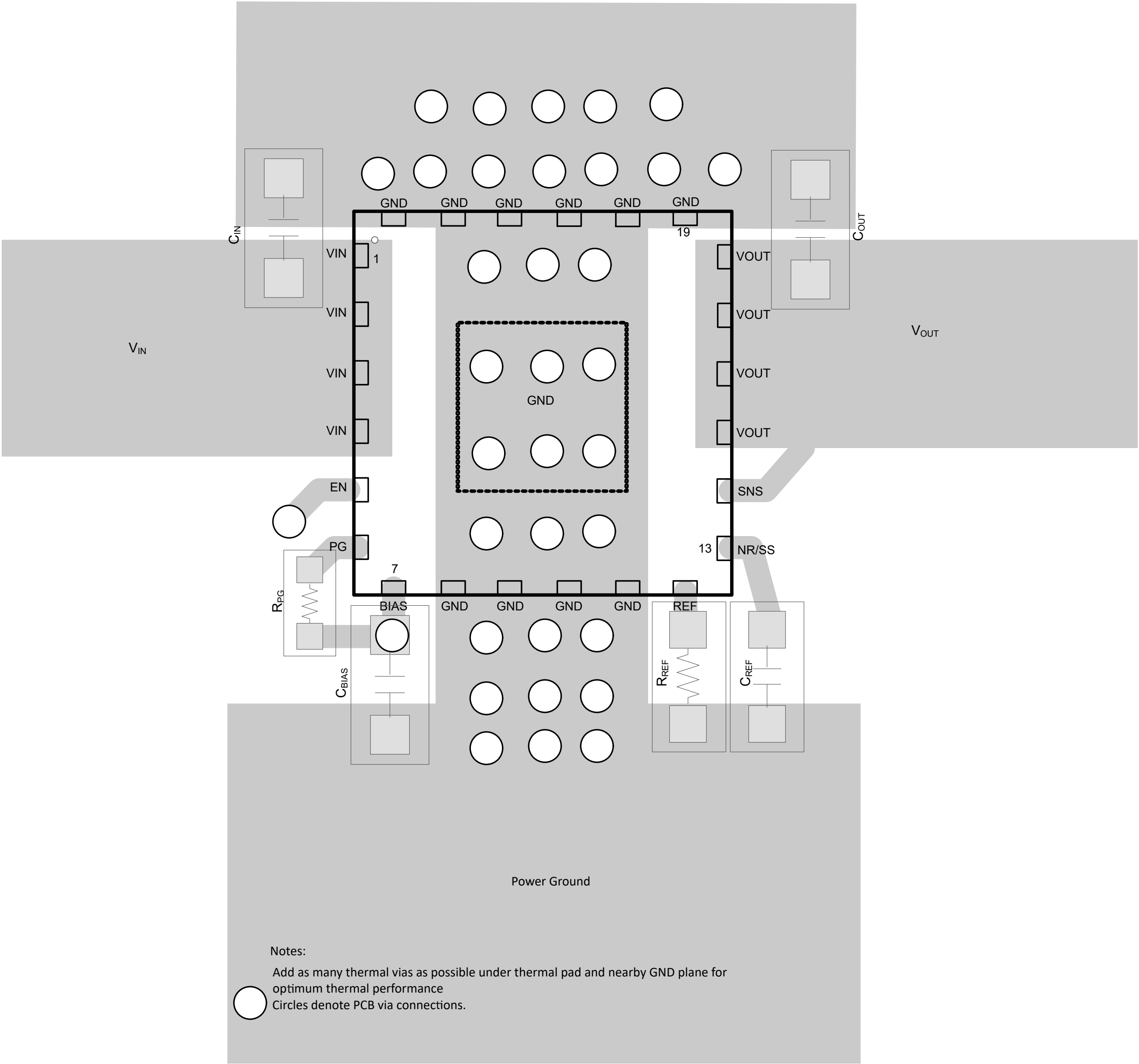
7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. To avoid negative system performance, do not use vias and long traces to the input and output capacitors. The grounding and layout scheme illustrated in Figure 7-21 minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

Because of the wide bandwidth and high output current capability, inductance present on the output negatively impacts load transient response. For best performance, minimize trace inductance between the output and load. A low ESL capacitor combined with low trace inductance limits the total inductance present on the output and optimizes the high-frequency PSRR.

To improve performance, use a ground reference plane, either embedded in the PCB or placed on the bottom side of the PCB opposite the components. This reference plane serves to verify the accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

7.4.2 Layout Example



Notes:
Add as many thermal vias as possible under thermal pad and nearby GND plane for optimum thermal performance
Circles denote PCB via connections.

Figure 7-21. Recommended Layout

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2026) to Revision A (March 2026)	**Page**
• Added features	1
• Updated TBD with 30dB	1
• Deleted NC pin descriptionUpdated pin 13 from NC to NR/SS	3

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

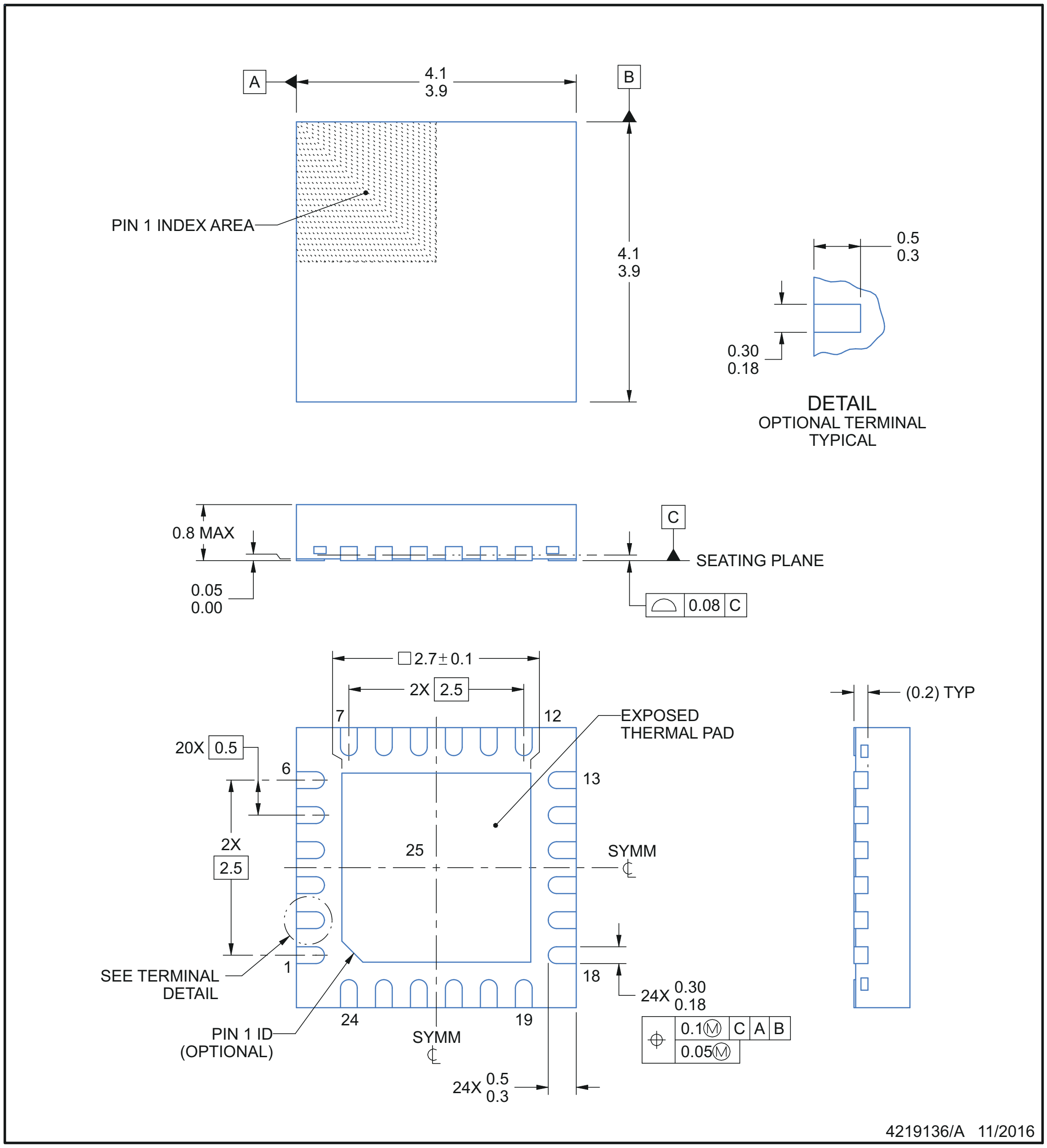
ADVANCE INFORMATION

PACKAGE OUTLINE

RTW0024H

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.

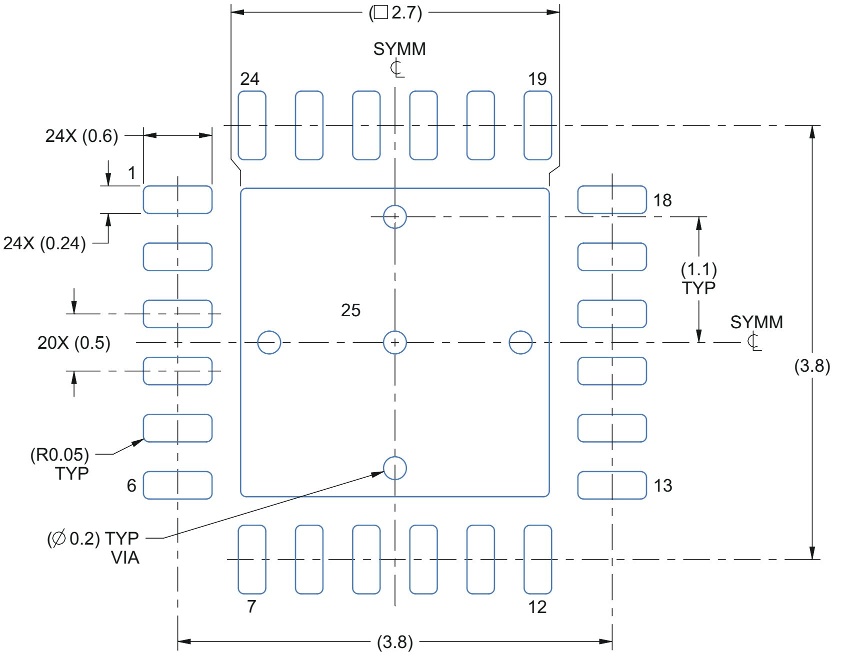
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

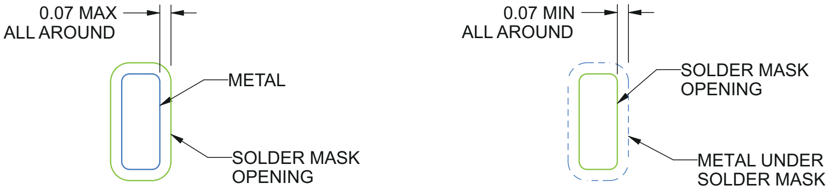
RTW0024H

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219136/A 11/2016

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

Texas Instruments
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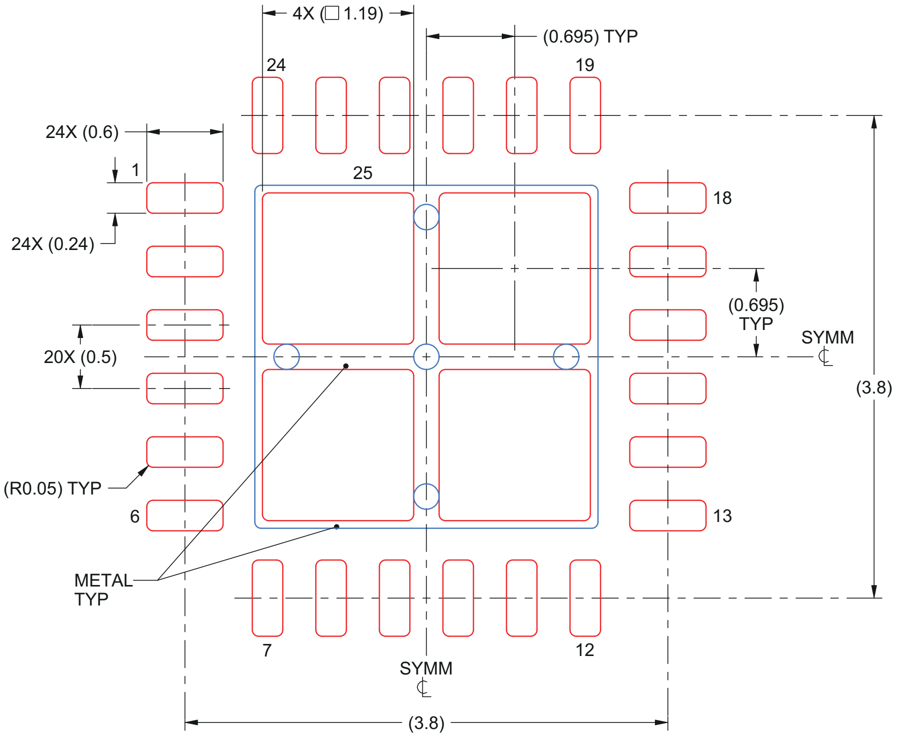
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RTW0024H **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219136/A 11/2016

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS7N5901RTWR	Active	Preproduction	WQFN (RTW) | 24	1 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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