TPSI2260-Q1 600V, 50mA, Automotive Reinforced Solid-State Relay With Avalanche Protection

1 Features

- Qualified for automotive applications
  - AEC-Q100 grade 1: –40 to 125°C T_A
- Low EMI:
  - Meets CISPR25 class 5 performance with no additional components
- Integrated avalanche rated MOSFETs
  - Designed and qualified for reliability for dielectric withstand testing (Hi-Pot)
    - TPSI2260-Q1: I_{AVA} =1mA for 60s pulses
    - TPSI2260C-Q1: I_{AVA} =0.6mA for 60s pulses
    - TPSI2260T-Q1: I_{AVA} = 3mA for 60s pulses
  - 600V standoff voltage
  - R_{ON} = 65Ω (T_J = 25°C)
  - I_{OFF} = 1.22µA at 500V (T_J = 105°C)
- Low primary side supply current
  - 5mA ON state current
  - 3.5µA OFF state current (T_J = 25°C)
- Functional Safety Capable
  - Documentation available to aid in ISO 26262 and IEC 61508 system design
- Robust isolation barrier:
  - > 30 year projected lifetime at 1500V_{RMS} / 2120$_{DC}$ working voltage
  - Reinforced isolation rating, V_{ISO}, up to 5000V_{RMS}
- SOIC 11-pin (DWQ) package with wide pins for improved thermal performance
  - Creepage and clearance ≥ 8mm (primary-secondary)
  - Creepage and clearance ≥ 6mm (across switch terminals)
- Safety-Related Certifications
  - (Planned) DIN EN IEC 60747-17 (VDE 0884-17)
  - (Planned) UL 1577 component recognition program

2 Applications

- Solid state relay
- Hybrid, electric, and power train systems
- Battery management systems (BMS)
- Solar energy
- Onboard charger
- EV charging infrastructure
- See also the TI Reference Designs related to these applications

3 Description

The TPSI2260-Q1 is an isolated solid state relay designed for high voltage automotive and industrial applications. The TPSI2260-Q1 uses TI's high reliability reinforced capacitive isolation technology in combination with internal back-to-back MOSFETs to form a completely integrated solution requiring no secondary side power supply. The TPSI2260-Q1 improves system reliability as TI's capacitive isolation technology does not suffer from mechanical wearout or photo degradation failure modes common in mechanical relay and photo relay components.

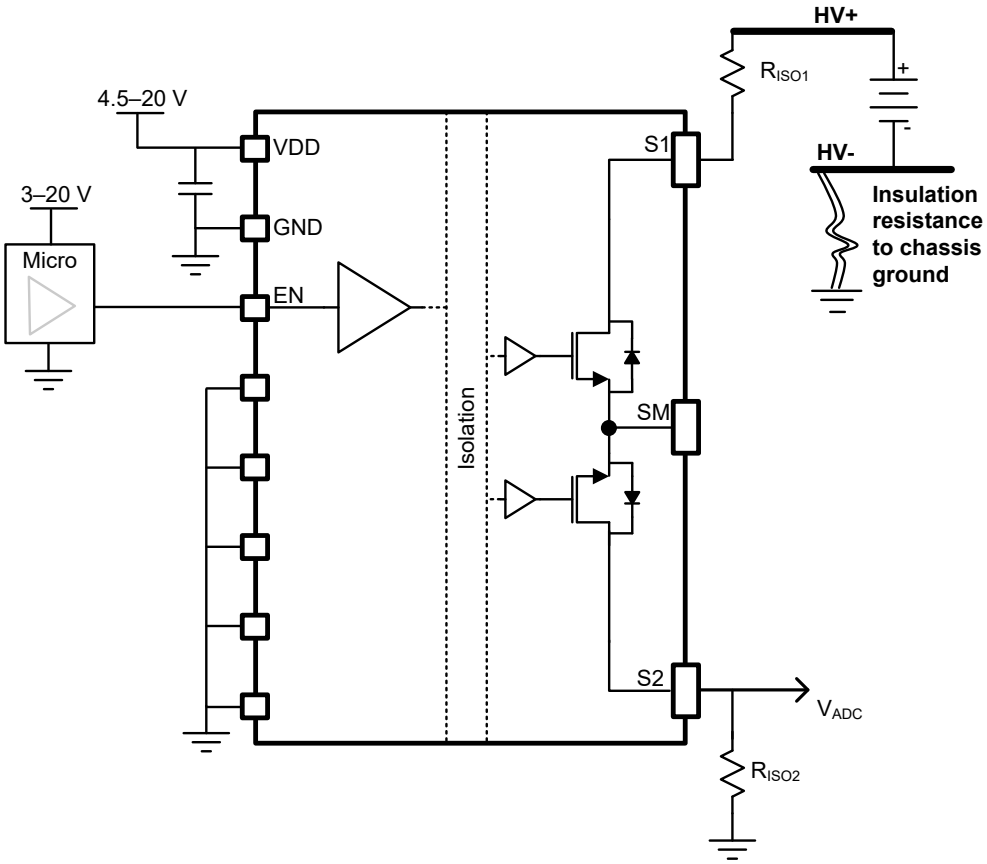
The primary side of the device is powered by only 5mA of input current and incorporates a fail-safe EN pin preventing any possibility of back powering the VDD supply. In most applications, the VDD pin of the device must be connected to a system supply from between 4.5V to 20V and the EN pin of the device must be driven by a GPIO output with Logic high between 2.1V to 20V. In other applications, the VDD and EN pins can be driven together driven together directly from the system supply or from a GPIO output.

The secondary side consists of back-to-back MOSFETs with a standoff voltage of ±600V from S1 to S2. The TPSI2260-Q1 MOSFET avalanche robustness and thermally conscious package design allow it to robustly support system level dielectric withstand testing (HiPot) and DC fast charger surge currents of up to 1mA (0.6mA for TPSI2240C-Q1 and 3mA for TPSI2260T-Q1) without requiring any external components.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPSI2260-Q1	DWQ (SOIC, 11)	10.3mm × 7.5mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPSI2260-Q1 Simplified Application Schematic

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4 Device Comparison Table

DEVICE	AVALANCHE PROTECTION	MAX AVALANCHE CURRENT
TPSI2260-Q1	Standard avalanche protection	1.0mA
TPSI2260C-Q1	Standard avalanche protection	0.6mA
TPSI2260T-Q1	Thermal avalanche protection	3.0mA

5 Pin Configuration and Functions

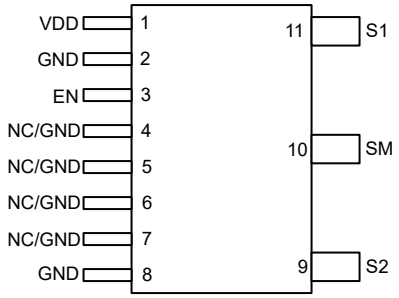


Figure 5-1. TPSI2260-Q1 DWQ Package, 11-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	VDD	P	Power supply for primary side
2	GND	GND	Ground supply for primary side
3	EN	I	Active high switch enable signal
4	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
5	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
6	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
7	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
8	GND	GND	Internally connected to GND, connect externally to ground or leave floating
9	S2	I/O	Switch input
10	SM	NC	For thermal dissipation only, see Layout Guidelines for more information.
11	S1	I/O	Switch input

(1) P = power, I = input, O = output, GND = ground, NC = no connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
V_{VDD}	Primary side supply voltage(2)	–0.3	20.7	V
V_{EN}	Enable Voltage(2)	–0.3	20.7	V
$I_{S1,S2}$	Switch current, S1/S2	–55	55	mA
$I_{AVA,S1,S2}$	Repetitive avalanche rating, TPSI2260-Q1, 60s pulse, S1/S2(3)	–1	1	mA
$I_{AVA,S1,S2}$	Repetitive avalanche rating, TPSI2260C-Q1, 60s pulse, S1/S2(3)	–0.6	0.6	mA
$I_{AVA,S1,S2}$	Repetitive avalanche rating, TPSI2260T-Q1, 60s pulse, S1/S2(3)	–3	3	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Voltage values are with respect to GND.
(3) 5 minutes accumulated over lifetime in increments of no longer than 60 second periods, duty cycle < 10%

6.2 ESD Ratings

				VALUE	UNIT
HBM_{Prim}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	Primary Side Pins No. 1-8	±2000	V
HBM_{Sec}		Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 1C	Secondary Side Pins No. 9-11	±1000	V
CDM	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4	All pins	±750	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{VDD}	Primary side supply voltage(1)	4.5		20	V
V_{EN}	Enable voltage(1)	0		20	V
V_{S2S1}	Switch input voltage	–600		600	V
$I_{S1,S2}$	Switch current	–50		50	mA
T_A	Ambient operating temperature	–40		125	°C
T_J	Junction operating temperature	–40		150	°C

(1) Voltage values are with respect to GND.

6.4 Thermal Information

THERMAL METRIC (1)		DEVICE DWQ (SOIC) 11 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	82	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	16.5	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	38.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation, total	V_{VDD} = 5V, V_{EN} = 5V peak to peak, V_{S1S2} = 600V, R_{S1} = 500kΩ f_{EN} = 1Hz square wave			30.5	mW
P_{D_P}	Maximum power dissipation (primary)				30	mW
P_{D_S}	Maximum power dissipation (secondary)				0.5	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
IEC 60664-1				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External Creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-III	
		Rated mains voltage ≤ 1000V_{RMS}	I-II	
DIN V VDE 0884-11:2017-01(2), IEC 60747-17:2020				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2120	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave)	1500	V_{RMS}
		DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification)	7070	V_{PK}
		V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production)	8484	V_{PK}
V_{IMP}	Maximum Impulse isolation voltage(6)	Tested in air per IEC 62638-1, 1.2/50µs waveform	7690	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Tested in oil per IEC 62638-1, 1.2/50µs waveform, V_{TEST} = 1.3 × V_{IOSM} = 6500V_{PK} (qualification)	10000	V_{PK}

6.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3,V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.2 × V_{IORM} = 1800V_{PK}, t_m = 10s	≤5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.6 × V_{IORM} , t_m = 10s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test), V_{ini} = V_{IOTM}, t_{ini} = 1s; $V_{pd(m)}$ = 1.875 × V_{IORM} = , t_m = 1s	≤5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2πft), f = 1MHz	1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500V, T_A = 25°C	>10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	>10^{11}	
		V_{IO} = 500V at T_S = 150°C	>10^{9}	
	Pollution degree		2	
	Climatic category		40/150/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO}, t = 60s (qualification) V_{TEST} = 1.2 × V_{ISO}, t = 1s (100% production)	5000	V_{RMS}
Misc.				
V_{ISO}	Withstand isolation voltage		7070	V_{DC}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.
(6) Testing is carried out in air to determine the intrinsic surge immunity of the package.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Not Planned, contact TI to request.	Plan to certify according to UL 1577 Component Recognition Program	Not Planned, contact TI to request.	Not Planned, contact TI to request.
Reinforced insulation; Maximum transient isolation voltage, 7070 V_{PK}; Maximum repetitive peak isolation voltage, 2120V_{PK}; Maximum surge isolation voltage, 10000V_{PK}		Single protection, 5000V_{RMS}		
Certificate planned		Certificate planned		

6.8 Safety Limiting Values

PARAMETER(1) (2)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety VDD Current	$R_{\theta JA}$ = 82°C/W, V_{VDD} = 20V, T_J = 150°C, T_A = 25°C			76	mA
	Safety Switch Current (On State)	$R_{\theta JA}$ = 82°C/W, V_{VDD} = 20V, T_J = 150°C, T_A = 25°C			71	
	Safety Switch Current (Off State, 60 second)	$R_{\theta JA, EVM, 60S}$ (3) = 71.2°C/W, V_{VDD} = 0V, T_J = 150°C, T_A = 25°C			2.2	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 82°C/W, T_J = 150°C, T_A = 25°C.			1.52	W
T_S	Maximum safety temperature				150	°C

(1) Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.
(2) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.
(3) Assuming PCB layout similar to EVM in Layout Guideline section

6.9 Electrical Characteristics

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_J = 25°C, V_{VDD} = 5V, V_{EN} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PRIMARY SIDE SUPPLY (VDD)						
V_{UVLO}	VDD undervoltage threshold	VDD rising	4.1	4.3	4.5	V
		VDD falling	4.0	4.2	4.45	V
		Hysteresis	40	100	150	mV
I_{VDD_ON}	VDD current, device powered on	V_{EN} = 5V, T_J = 25°C		5	11	mA
		V_{EN} = 5V, –40°C ≤ T_J ≤ 150°C		5	12	mA
I_{VDD_OFF}	VDD current, 5V, device powered off	V_{VDD} = 5V, V_{EN} = 0V, T_J = 25°C		4	8	µA
		V_{VDD} = 5V, V_{EN} = 0V, T_J = 105°C		6.3	11	µA
		V_{VDD} = 5V, V_{EN} = 0V, T_J = 125°C		7.6	16	µA
		V_{VDD} = 5V, V_{EN} = 0V, –40°C ≤ T_J ≤ 150°C			30	µA
	VDD current, 20V, device powered off	V_{VDD} = 20V, V_{EN} = 0, V T_J = 25°C		9.2	10.5	µA
		V_{VDD} = 20V, V_{EN} = 0V, T_J = 105°C		13	17	
		V_{VDD} = 20V, V_{EN} = 0V, T_J = 125°C		15	25	
		V_{VDD} = 20V, V_{EN} = 0V, –40°C ≤ T_J ≤ 150°C			40	
FET CHARACTERISTICS (S1, S2)						
R_{DSON}	On resistance	I_O = 2mA, T_J = 25°C		65	88	Ω
		I_O = 2mA, T_J = 85°C		88	120	
		I_O = 2mA, T_J = 105°C		96	125	
		I_O = 2mA, T_J = 125°C		105	140	
		I_O = 2mA, –40°C ≤ T_J ≤ 150°C			150	

6.9 Electrical Characteristics (continued)

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_J = 25°C, V_{VDD} = 5V, V_{EN} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OFF}	Off leakage, 600V	V = ±600V, T_J = 25°C		0.058	0.25	µA
		V = ±600V, T_J = 85°C			0.5	
		V = ±600V, T_J = 105°C			1.5	
		V = ±600V, T_J = 125°C			6	
		V = ±600V, –40°C ≤ T_J ≤ 150°C			50	
	Off leakage, 500V	V = ±500V, T_J = 25°C		0.055	0.25	µA
		V = ±500V, T_J = 85°C			0.43	
		V = ±500V, T_J = 105°C			1.22	
		V = ±500V, T_J = 125°C			5.75	
		V = ±500V, –40°C ≤ T_J ≤ 150°C			44	
V_{AVA}	Avalanche voltage	I_O = 10 µA, T_J = 25°C	650	770		V
		I_O = 100 µA, T_J = 150°C	650	770		
C_{OSS}	S1, S2 capacitance	$V_{S1,S2}$ = 0V, SM float, F = 1MHz		188		pF
T_{TAP1}	Thermal Avalanche Protection threshold	Assertion	155			C
T_{TAP_END}	Thermal Avalanche Protection threshold	De-assertion	85		125	C
LOGIC-LEVEL INPUT (EN						
V_{IL}	Input logic low voltage		0.0		0.8	V
V_{IH}	Input logic high voltage		2.1		20.0	V
V_{HYS}	Input logic hysteresis		100	250	300	mV
I_{IL}	Input logic low current	V_{EN} = 0V	–0.1		0.1	µA
		V_{EN} = 0.8V	0.1	0.68	1.8	µA
I_{IH}	Input logic high current	V_{EN} = 10V	6.0	13.5	30	µA
I_{IH}	Input logic high current	V_{EN} = 5V	1.5	4.5	12	µA
		V_{EN} = 20V	15	32	65	µA
I_{VDD_FS}	VDD fail-safe current	V_{EN} = 20V, V_{VDD} = 0V	–0.1	0	0.1	µA
R_{PD}	Pulldown resistance	Two point measurement, V_{EN} = 0.5V and V_{EN} = 0.8V	550	1180	2100	kΩ
NOISE IMMUNITY						
CMTI	Common-mode transient immunity	$\|V_{CM}\|$ = 500V	100			V/ns

6.10 Switching Characteristics

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_A = 25°C, V_{VDD} = 5V, V_{EN} = 5V.

MODE	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switching Characteristics						

6.10 Switching Characteristics (continued)

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_A = 25°C, V_{VDD} = 5V, V_{EN} = 5V.

MODE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN switching	t_{PD_ON}	Input HI to Output voltage falling propagation delay	V_{IN} = 500V R_L = 1MΩ		170	370	µs
	t_F	Output fall time			47	100	
	t_{ON}	Input HI to Output LO delay			220	440	
	t_{PD_OFF}	Input LO to Output voltage rising propagation delay			178	290	
	t_R	Output rise time			29	70	
	t_{OFF}	Input LO to Output HI delay			200	350	
EN and VDD switching	t_{PD_ON}	Input HI to Output voltage falling propagation delay	V_{IN} = 500V R_L = 1MΩ		260	500	µs
	t_F	Output fall time			50	100	
	t_{ON}	Input HI to Output LO delay			310	590	
	t_{PD_OFF}	Input LO to Output voltage rising propagation delay			170	290	
	t_R	Output rise time			30	70	
	t_{OFF}	Input LO to Output HI delay			200	350	

6.11 Typical Characteristics

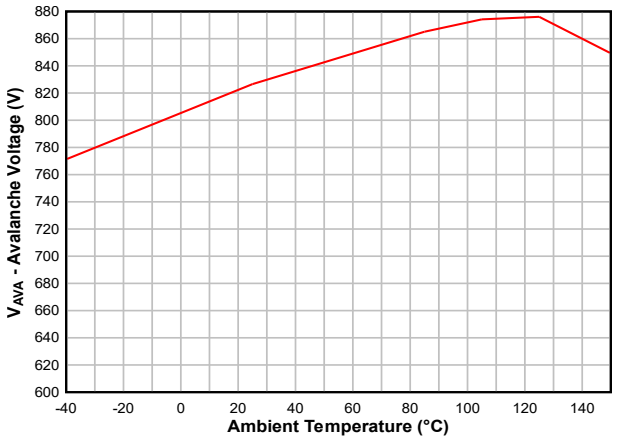


Figure 6-1. Avalanche Voltage vs Ambient Temperature (I_O = 100uA)

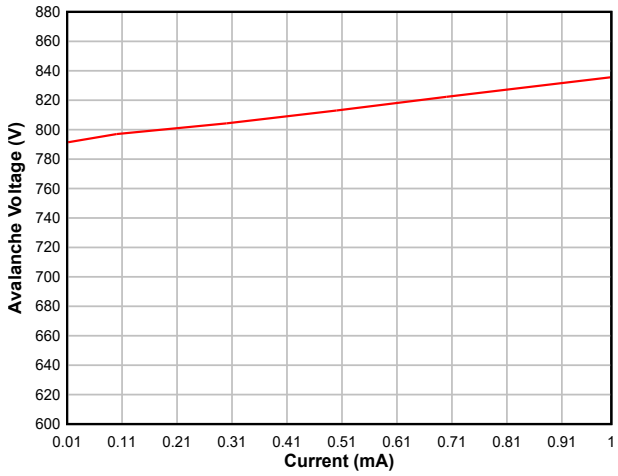


Figure 6-2. Avalanche Voltage vs Avalanche Current

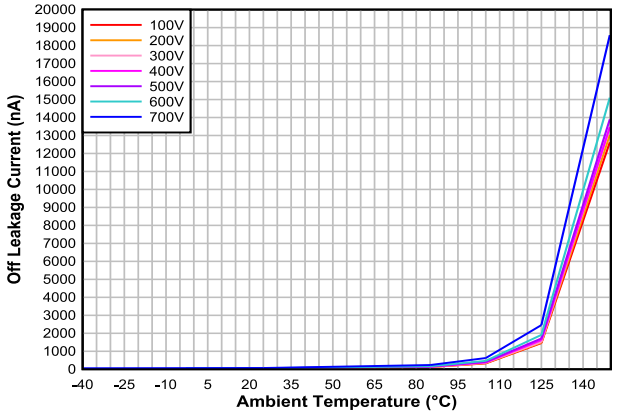


Figure 6-3. Off Leakage Current vs Ambient Temperature

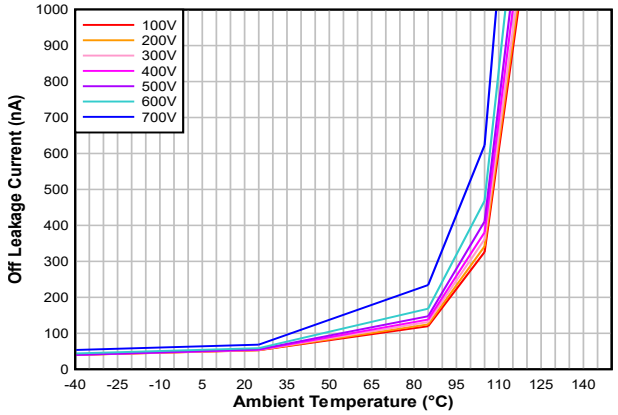


Figure 6-4. Off Leakage Current vs Ambient Temperature (Zoomed)

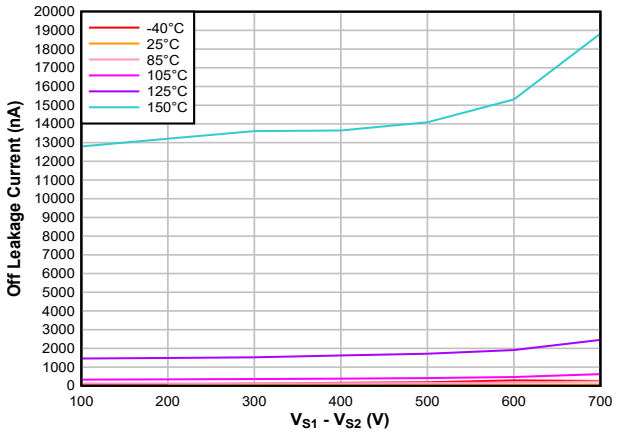


Figure 6-5. Off Leakage Current vs Output Voltage

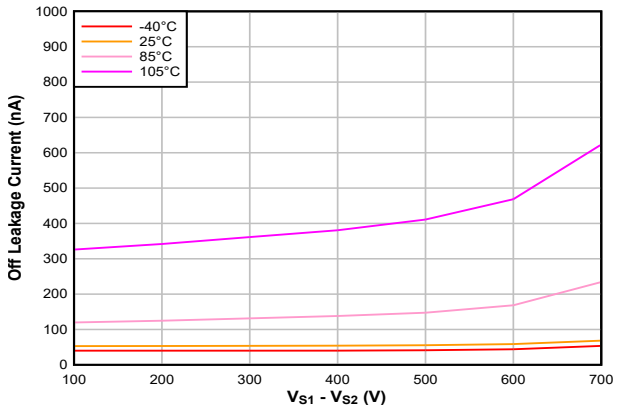


Figure 6-6. Off Leakage Current vs Output Voltage (Zoomed)

6.11 Typical Characteristics (continued)

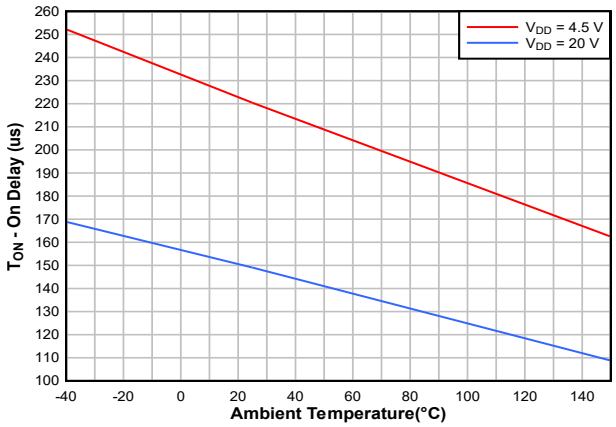


Figure 6-7. Input to Output ON Delay (V_{IN} = 500V)

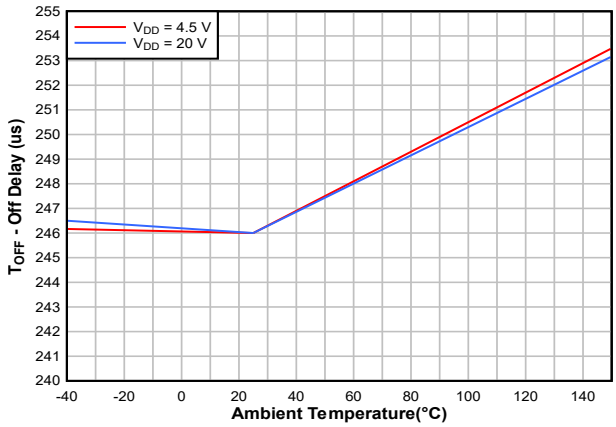


Figure 6-8. Input to Output OFF Delay (V_{IN} = 500V)

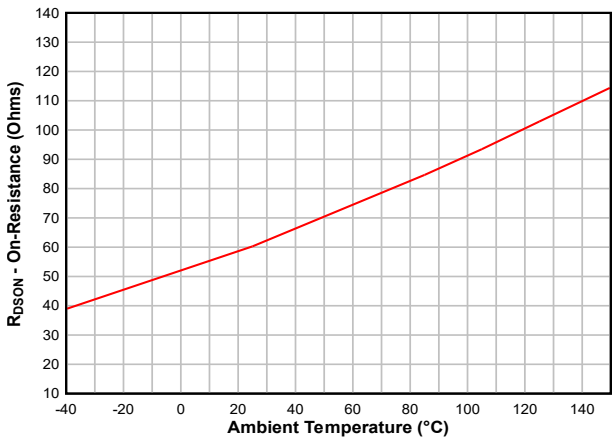


Figure 6-9. Typical On-Resistance vs Ambient Temperature

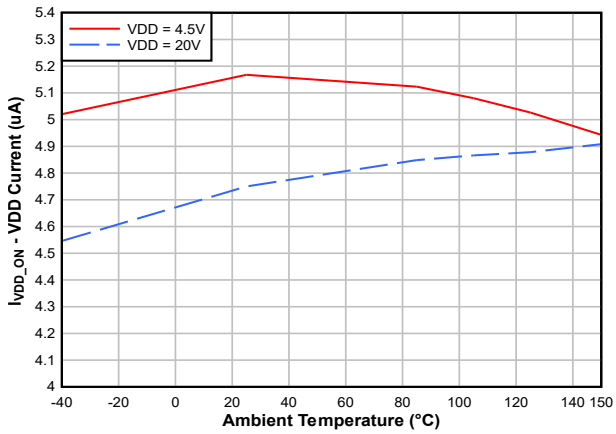


Figure 6-10. VDD Current vs Ambient Temperature

7 Parameter Measurement Information

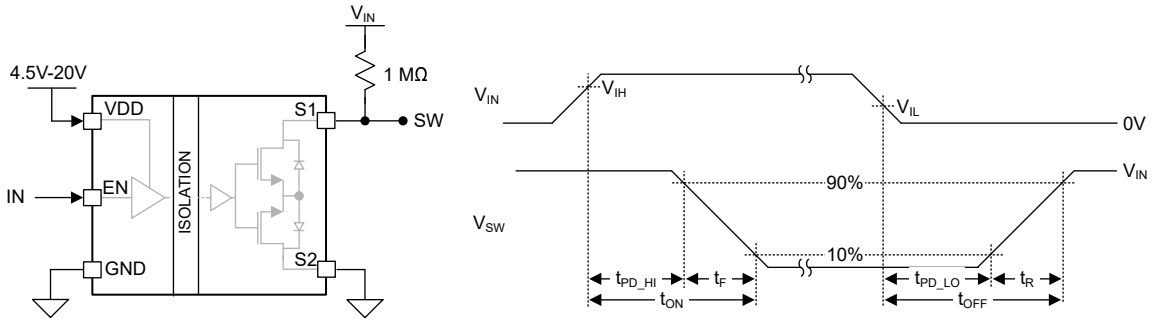


Figure 7-1. Timing Diagram, EN Switching

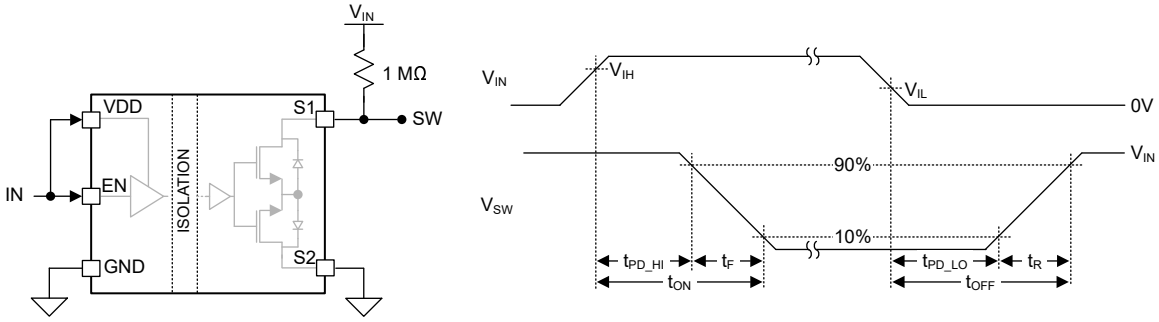


Figure 7-2. Timing Diagram, EN and VDD Switching

8 Detailed Description

8.1 Overview

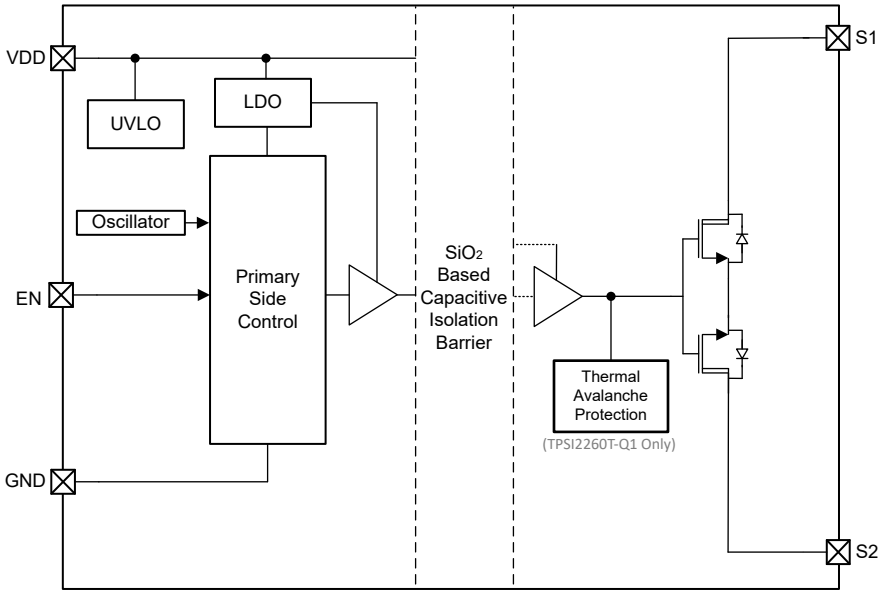
The TPSI2260-Q1 is an isolated solid state relay designed for high voltage automotive and industrial applications. TI's high reliability capacitive isolation technology in combination with back-to-back MOSFETs form a completely integrated solution requiring no secondary side power supply.

As seen in the *Functional Block Diagram*, the primary side consists of a driver which delivers power and enable logic information to each of the internal MOSFETs on the secondary side. The on-board oscillator controls the frequency of the driver's operation and the Spread Spectrum Modulation (SSM) controller varies the driver frequency to improve system EMI performance. When VDD voltage is above the UVLO threshold, and the enable pin is brought HI, the oscillator starts and the driver sends power and a logic HI across the barrier. When the enable pin is brought LO or the VDD voltage falls below the UVLO threshold, the driver is disabled. The lack of activity communicates a logic LO to the secondary side and the MOSFETs are disabled.

The pair of MOSFETs on the secondary side has a dedicated full-bridge rectifier to form its local power supply and a receiver. The receiver determines the logic state delivered from the primary side through the capacitive isolation barrier and uses a slew rate controlled driver to drive the MOSFET's gate. The receiver performs signal conditioning on the signals received across the barrier to filter common mode interference and ensure that the MOSFETs are controlled according to the logic sent by the primary side driver and the system.

The avalanche robust MOSFETs and the thermal benefits of the widened pins on the 11 DWQ package enable the TPSI2260-Q1 to support dielectric withstand testing (HiPot) and DC fast charger surge currents of up to 1mA without requiring any external protection components. The Thermal Avalanche Protection (TAP) feature included in the TPSI2260T-Q1 version of the device further improves the avalanche current capability by monitoring the junction temperature and enabling the MOSFETs to keep the temperature in a safe operating range allowing it to support a higher avalanche current.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Avalanche Robustness

When the voltage between the S1 and S2 pins exceeds +/-600V the secondary side MOSFETs could enter an avalanche mode of operation. The MOSFETs and the 11 DWQ package have been designed and qualified to be robust in this mode of operation to support Dielectric Withstand Testing (HiPot). To help ensure the thermal performance of the the system in this mode of operation, refer to the PCB Layout Guidelines.

8.4 Device Functional Modes

Table 8-1. Device Functional Modes

VDD	EN	S1S2 STATE	COMMENTS
Powered Up(1)	L	OFF	VDD current is in OFF state range.
	H	ON	VDD current is in ON state range.
Powered Down(2)	L	OFF	VDD current is in OFF state range.
	H	OFF	Primary side analog is powered on, VDD current is between OFF state and ON state ranges.

(1) VDD ≥ VDD undervoltage rising threshold.
(2) VDD ≤ VDD undervoltage falling threshold.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPSI2260-Q1 is a 600V, 50mA automotive isolated switch optimized for high voltage switching in measurement applications, especially those that require switching across an isolation barrier or galvanically isolated domain. Common end equipments include energy storage systems (ESS), solar panel arrays, EV chargers, and EV battery management systems. The device enables the system designer to reduce cost and improve reliability by replacing mechanical relays and optically isolated devices.

The TPSI2260-Q1's enable input is fail safe and does not need to be driven from the same domain as the VDD pin supply.

The TPSI2260-Q1 supports an input voltage range of 4.5V to 20V on the VDD primary supply pin and a logic high from 2.1V to 20V on the enable pin. The secondary side supports high voltage switching from –600V to 600V.

9.1.1 TI Reference Designs

The TI reference designs linked below are a helpful introduction to high voltage applications using the TPSI2260-Q1. To maximize the thermal performance of the TPSI2260-Q1 for dielectric withstand testing (HiPot), please follow the Layout Guidelines contained within this datasheet.

- TIDA-010232: High Voltage Insulation Monitoring
- TIDA-01513: Automotive High Voltage and Isolation Leakage Measurements

9.2 Typical Application

9.2.1 Insulation Resistance Monitoring

In high voltage applications such as electric vehicle systems, the high voltage battery pack is intentionally isolated from the chassis domain of the car to protect the driver and prevent damage to electrical components. These systems actively monitor the integrity of this insulation to ensure the safety of the system throughout its lifetime. This active monitoring is referred to as insulation resistance monitoring (also known as isolation check, insulation check, isolation monitoring, insulation monitoring, and residual current monitoring (RCM)) and is performed by measuring the resistances from each of the battery terminals to the chassis ground, illustrated below as R_{ISOP} and R_{ISON}.

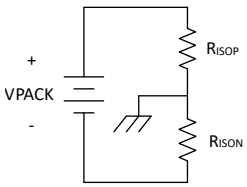


Figure 9-1. Insulation Resistance Model

There are multiple design architectures using the TPSI2260-Q1 to measure these insulation resistances, R_{ISOP} and R_{ISON}. Some architectures employ a microcontroller that performs measurements from the high voltage domain, which is referred to in this document as the Battery V- Reference architecture. Others use

a microcontroller in the low voltage domain, which is referred to in this document as the Chassis Ground Reference architecture. The primary difference between the two architectures is the node that the MCU uses as its GND reference. An example of a Battery V- MCU is the BQ79731-Q1 UIR sensor.

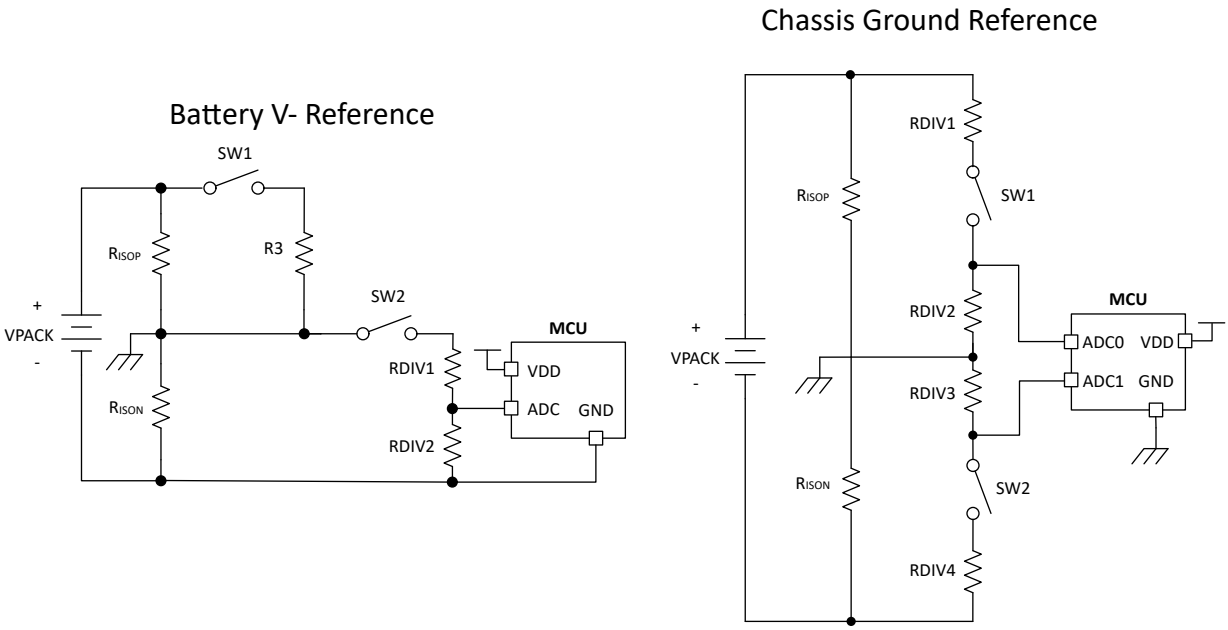


Figure 9-2. Different MCU ADC Reference Examples

The two following sections demonstrate the measurement algorithms and the systems of equations used to calculate the isolation resistances using each architecture.

9.2.2 Battery V- Reference Example

A Battery V- Reference architecture is shown below with the TPSI2260-Q1 illustrated as a switch (SW1 and SW2). SW2 initiates a connection between the chassis and PACK- and enables the measurement path to the ADC. SW1 initiates a connection between the chassis and the PACK+. RDIV1 and RDIV2 form a divider which scales the measured voltages down to the appropriate ADC range.

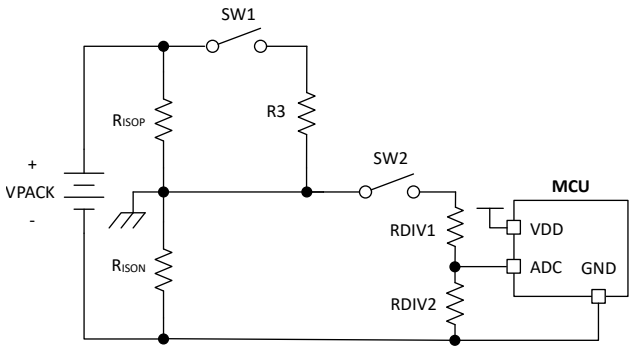


Figure 9-3. Battery V- Reference Architecture

Take two ADC measurements to obtain enough information to calculate the two unknown isolation resistances. The first measurement is taken with SW1 open and SW2 closed. The second measurement is taken with SW1 closed and SW2 closed. With these two measurements, it is possible to solve the system of equations and calculate R_{ISOP} and R_{ISON}.

In the following example the voltage on the chassis ground is arbitrarily referred to as V_{RISONx}.

For the first ADC measurement SW2 is closed as shown below and the following equations relate the ADC voltage to the other parameters in the system in this condition:

- V_{ADC1} measurement 1: SW1 open, SW2 closed

$$V_{RISON1} = V_{PACK} \times \frac{R_{ISON} || (R_{DIV1} + R_{DIV2})}{R_{ISOP} + (R_{ISON} || R_{DIV1} + R_{DIV2})} \quad (1)$$

$$V_{ADC1} = V_{RISON1} \times \frac{R_{DIV2}}{R_{DIV1} + R_{DIV2}} \quad (2)$$

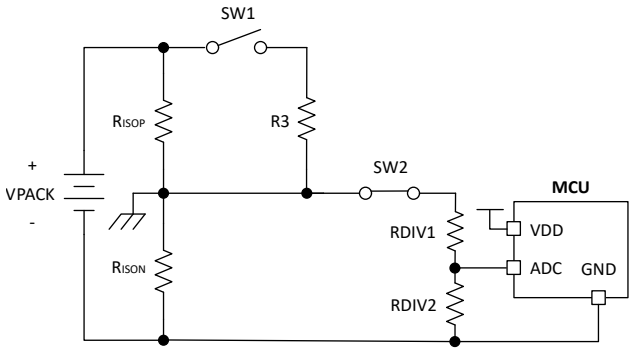


Figure 9-4. Battery V- Reference Switch Positions for ADC1 Measurement

For the second ADC measurement SW1 and SW2 are closed as shown below and the following equations relate the ADC voltage to the other parameters in the system in this condition:

- V_{ADC2} measurement 2: SW1 closed, SW2 closed

$$V_{RISON2} = V_{PACK} \times \frac{R_{ISON} || (R_{DIV1} + R_{DIV2})}{(R_{ISOP} || R_3) + (R_{ISON} || (R_{DIV1} + R_{DIV2})} \quad (3)$$

$$V_{ADC2} = V_{RISON2} \times \frac{R_{DIV2}}{R_{DIV1} + R_{DIV2}} \quad (4)$$

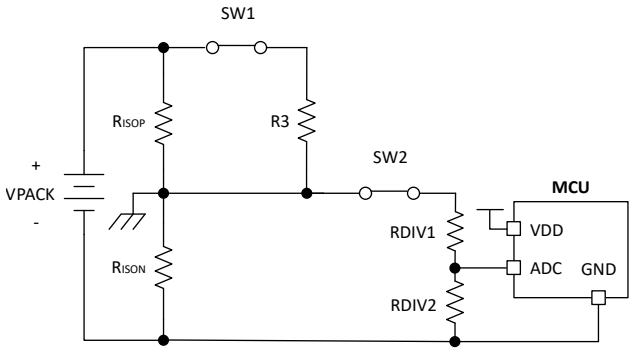


Figure 9-5. Battery V- Reference Switch Positions for ADC2 Measurement

9.2.3 Chassis Ground Reference Example

A Chassis Ground Reference architecture is shown below. SW1 and SW2 initiate connections to the PACK+ and PACK-, and enable the corresponding measurement paths to the ADCs through the corresponding resistor dividers. RDIV1, RDIV2, RDIV3, and RDIV4 scale the measured voltages down to the appropriate ADC ranges.

This first measurement is taken with SW1 closed and SW2 open and the second measurement is taken with SW1 open and SW2 closed.

- VADC1: SW1 closed, SW2 open

$$V_{ADC1} = V_{RDIV2} = V_{PACK}\frac{(R_{ISOP}||(R_{DIV1}+R_{DIV2}))}{(R_{ISOP}||(R_{DIV1}+R_{DIV2})+R_{ISON})} \times \frac{R_{DIV2}}{R_{DIV1}+R_{DIV2}} \quad (5)$$

- VADC2: SW1 open, SW2 closed

$$V_{ADC2} = V_{RDIV3} = -V_{PACK}\frac{(R_{ISON}||(R_{DIV3}+R_{DIV4}))}{(R_{ISON}||(R_{DIV3}+R_{DIV4}))+R_{ISOP})} \times \frac{R_{DIV3}}{R_{DIV3}+R_{DIV4}} \quad (6)$$

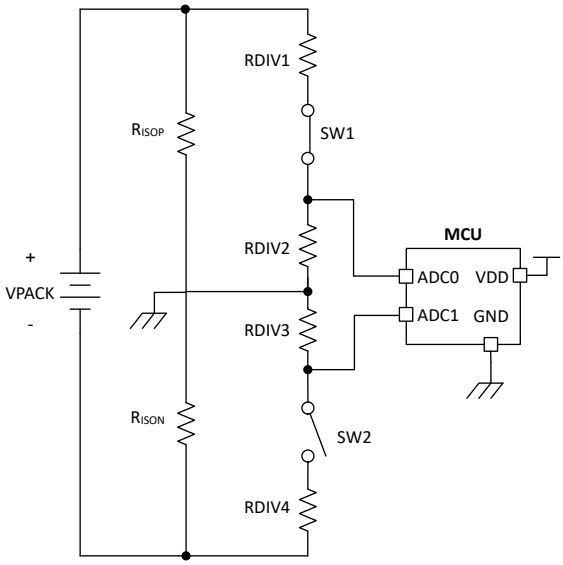


Figure 9-6. Chassis Ground Reference Switch Positions for ADC1 Measurement

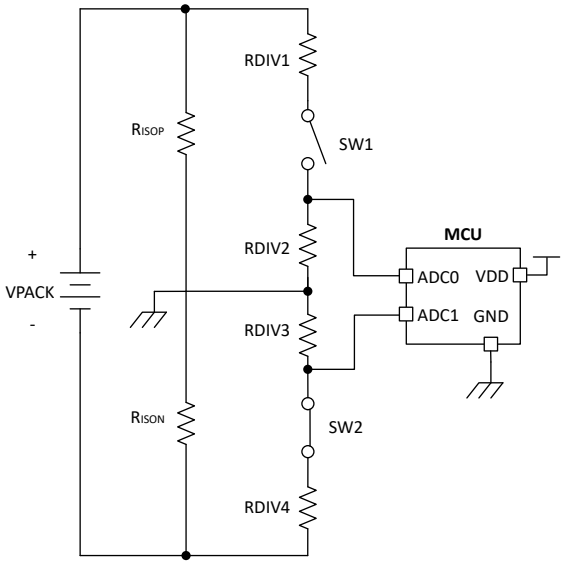


Figure 9-7. Chassis Ground Reference Switch Positions for ADC2 Measurement

9.2.4 Dielectric Withstand Testing (HiPot)

The TPSI2260-Q1 is specifically designed to support dielectric withstand testing. In a high voltage system, a dielectric withstand test (HiPot) can be administered during the characterization, production or maintenance of the system to validate the reliability of the insulation barriers and galvanically isolated domains it contains. These withstand voltage tests intentionally stress the components spanning these domains and put them in an overvoltage condition. MOSFETs that are placed under these overvoltage conditions enters avalanche mode and begin conducting current at a high voltage, dissipating high power and heating up. TPSI2260T-Q1 integrates Thermal Avalanche Protection (TAP). When the internal temperature of the IC increases beyond

T_{TAP} this mode enables. In this mode, the device enables and disable the main power FET to regulate its internal temperature and be able to sustain higher avalanche currents. The design and qualification of the TPSI2260T-Q1 is completed with this state in mind and supports up to 3mA I_{AVA} for 60 second intervals, while the TPSI2260-Q1 supports up to 1mA I_{AVA} for 60 second intervals (0.6mA for the TPSI2260C-Q1).

The dielectric withstand test voltage (V_{HiPot}), the TPSI2260-Q1's avalanche voltage (V_{AVA}), and the resistance (R) in series with the TPSI2260-Q1 must be selected to limit the avalanche current (I_{AVA}) to the corresponding current limit depending on the test duration. In addition, the PCB design must follow the recommendations in the Layout Guidelines section to establish adequate thermal performance to keep the junction temperature (T_J) below the absolute maximum rating of the TPSI2260-Q1.

9.2.5 Design Requirements

Table 9-1 lists the Design Requirements for a typical insulation resistance monitoring application using the Chassis Ground Reference architecture and the TPSI2260-Q1 for switching.

Table 9-1. Typical Design Parameters For Insulation Resistance Monitoring Using the TPSI2260-Q1 – Chassis Ground Reference Architecture

PARAMETER	VALUE
V_{PACK} Voltage (maximum)	500V
Primary side supply (V_{VDD})	5V ±10%
Dielectric withstand voltage test	2850V
	60s
Surge voltage (IEC61000-3-5)	2500V

9.2.6 Detailed Design Procedure - Chassis Ground Reference

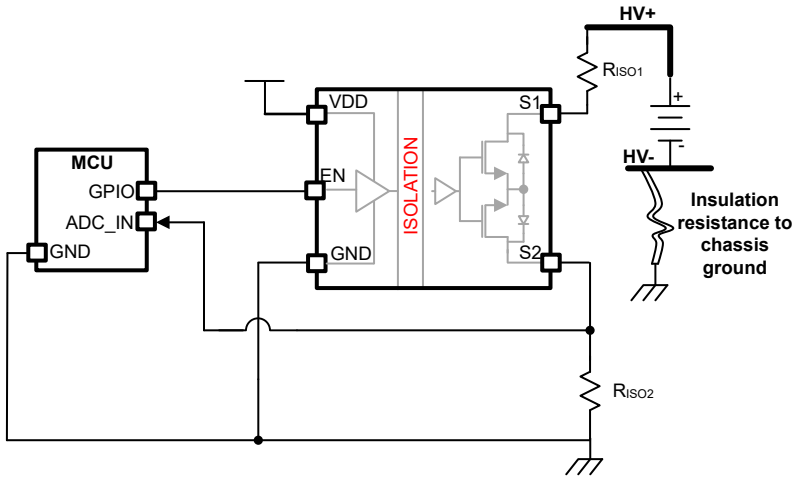


Figure 9-8. Chassis Ground Reference

9.2.6.1 R_{ISO1} Selection

To protect the TPSI2260-Q1, R_{ISO1} must be sized to limit the current in an overvoltage condition. The amount of resistance required to protect the TPSI2260-Q1 depends on the amount of overvoltage applied. For example, during a dielectric withstand voltage test (HiPot) of 2850V for 60 seconds, the S1 to S2 voltage will be clamped to 1300V (V_{AVA} minimum) by the TPSI2260-Q1 and the minimum R_{ISO1} resistance required to keep the current under 1mA would be 2.2MΩ.

$$I_{AVA} = \frac{V_{HIPOT} - V_{AVA}}{R_{ISO1}} = \frac{2850V - 650V}{2.2\ M\Omega} = 1.0mA \quad (7)$$

Similarly, the minimum R_{ISO1} resistance required to keep the current of the TPSI2260T-Q1under 3mA would be 734kΩ.

DC OVERVOLTAGE	R_{ISO1} MINIMUM (60 second intervals)
2000V	1350kΩ
2850V	2200kΩ
3500V	2850kΩ
4300V	3650kΩ

9.2.7 Application Performance Plot

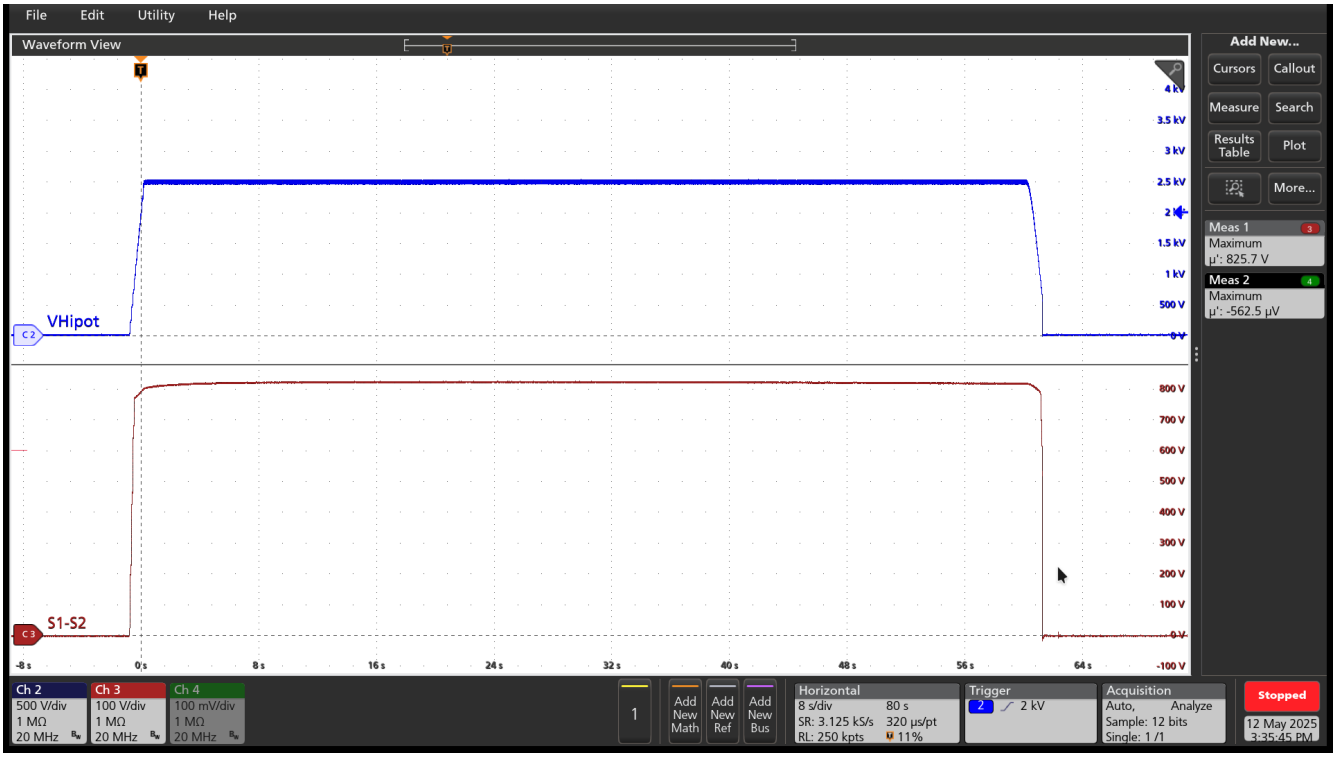


Figure 9-9. Avalanche Voltage (V_{S1S2}) at V_{HIPOT}= 2500V with 900kΩ Limiting Resistor

9.3 Power Supply Recommendations

To ensure a reliable supply voltage, TI recommends that a 100nF ceramic capacitor be placed between the VDD pin and the GND pin of the TPSI2260-Q1. The capacitor should be placed as close to the device's VDD pin as possible < 10mm.

9.4 Layout

9.4.1 Layout Guidelines

9.4.1.1 Component Placement

Decoupling capacitors for the primary side VDD supply must be placed as close as possible to the device pins.

9.4.1.2 EMI Considerations

The TPSI2260-Q1 employs spread spectrum modulation (SSM) with a power transfer frequency of 2MHz to improve its EMI capabilities. In most applications no additional system design considerations are required to meet the CISPR 25 Class 5 standard performance.

If CISPR25 Class 5 is required on the secondary side, a split limiting resistor configuration is recommended for best EMI performance, as shown in TPSI2260-Q1 Layout Example.

9.4.1.3 ESD Considerations

No additional components are required to pass IEC 61000-4-2 up-to 6kV contact.

If contact >6kV strikes is required, a split resistance configuration increases ESD performance to >8kV contact. Alternatively, ESD capacitors between primary and secondary side can be added to improve ESD performance in non-split resistance architectures.

9.4.1.4 High-Voltage Considerations

The creepage from the primary side to the secondary side and the creepage from the S1 pin to S2 pin of the TPSI2260-Q1 must be maintained according to system requirements. It is most likely that the system designer avoids any top layer PCB routing underneath the body of the package or between the S1, SM, and S2 pins.

9.4.2 Layout Example

Varying PCB implementations are possible depending on both the system EMI requirements and the system dielectric withstand testing (HiPot) parameters. The following figures detail a TPSI2260-Q1 layout example optimized for best EMI and ESD performance by implementing split resistance architecture on the secondary side.

An example 2-layer circuit layout using the TPSI2260-Q1 is shown below.

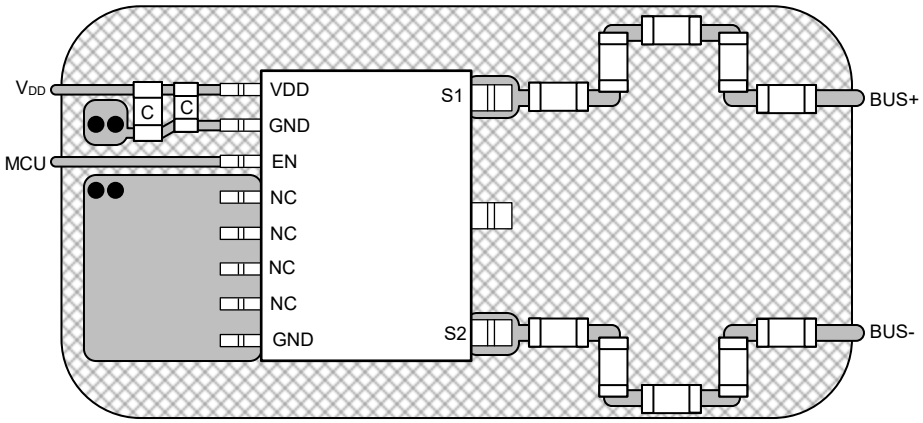


Figure 9-10. TPSI2260-Q1 Example Layout - Top Layer

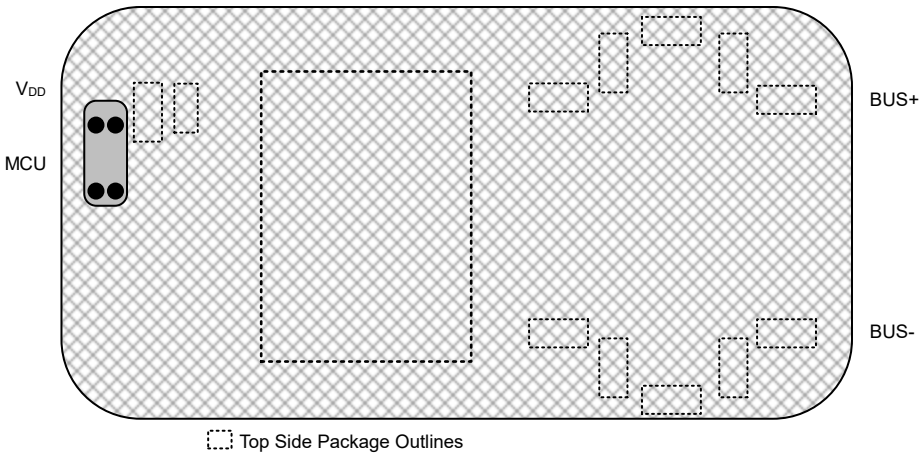


Figure 9-11. TPSI2260-Q1 Example Layout - Bottom Layer

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2025) to Revision B (April 2026)	Page
• Added TPSI2260C-Q1 data throughout document	1
• Moved TI Reference Designs from Application Information to TI Reference Designs	17
• Moved Component Placement from Layout Guidelines to Component Placement	23
• Moved EMI Considerations from Layout Guidelines to EMI Considerations	23
• Moved ESD Considerations from Layout Guidelines to ESD Considerations	24
• Moved High-Voltage Considerations from Layout Guidelines to High-Voltage Considerations	24

Changes from Revision * (June 2025) to Revision A (December 2025)	Page
• Changed status from Advance Information to Production Data	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPSI2260QDWQRQ1	Active	Preproduction	SOIC (DWQ) | 11	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPSI2260CQDWQRQ1	Active	Production	SOIC (DWQ) | 11	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	2260CQ
TPSI2260QDWQRQ1	Active	Production	SOIC (DWQ) | 11	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	2260Q
TPSI2260TQDWQRQ1	Active	Production	SOIC (DWQ) | 11	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	2260TQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

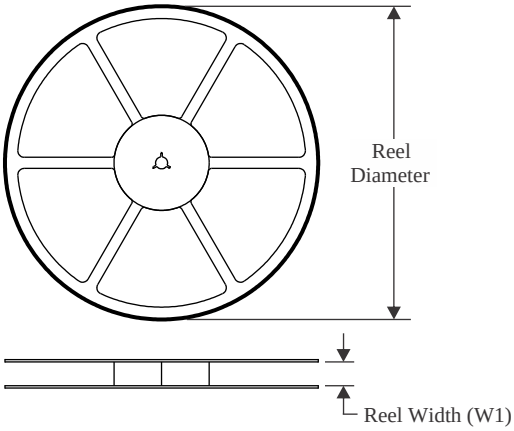
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

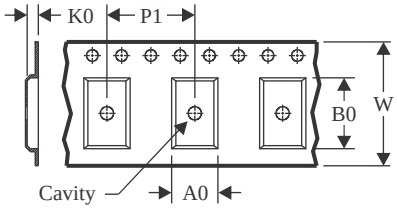
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

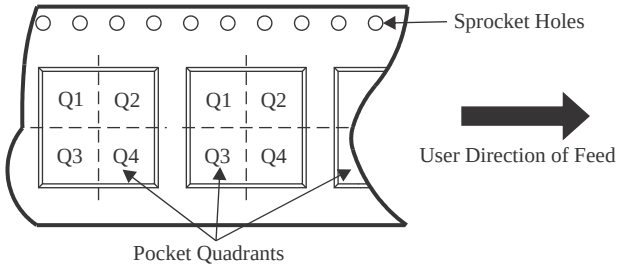


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

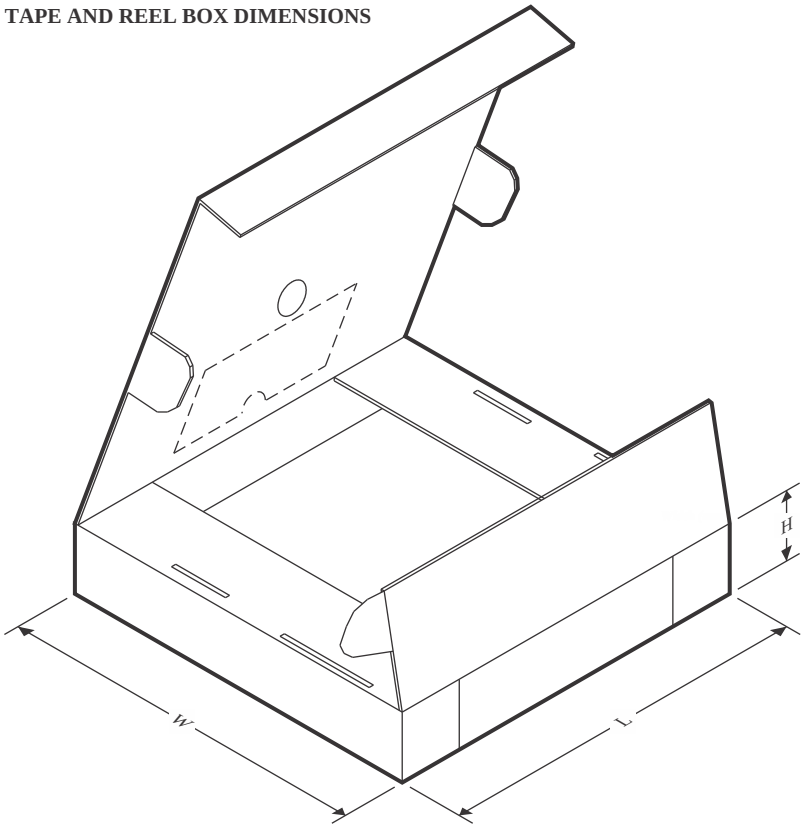
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSI2260QDWQRQ1	SOIC	DWQ	11	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

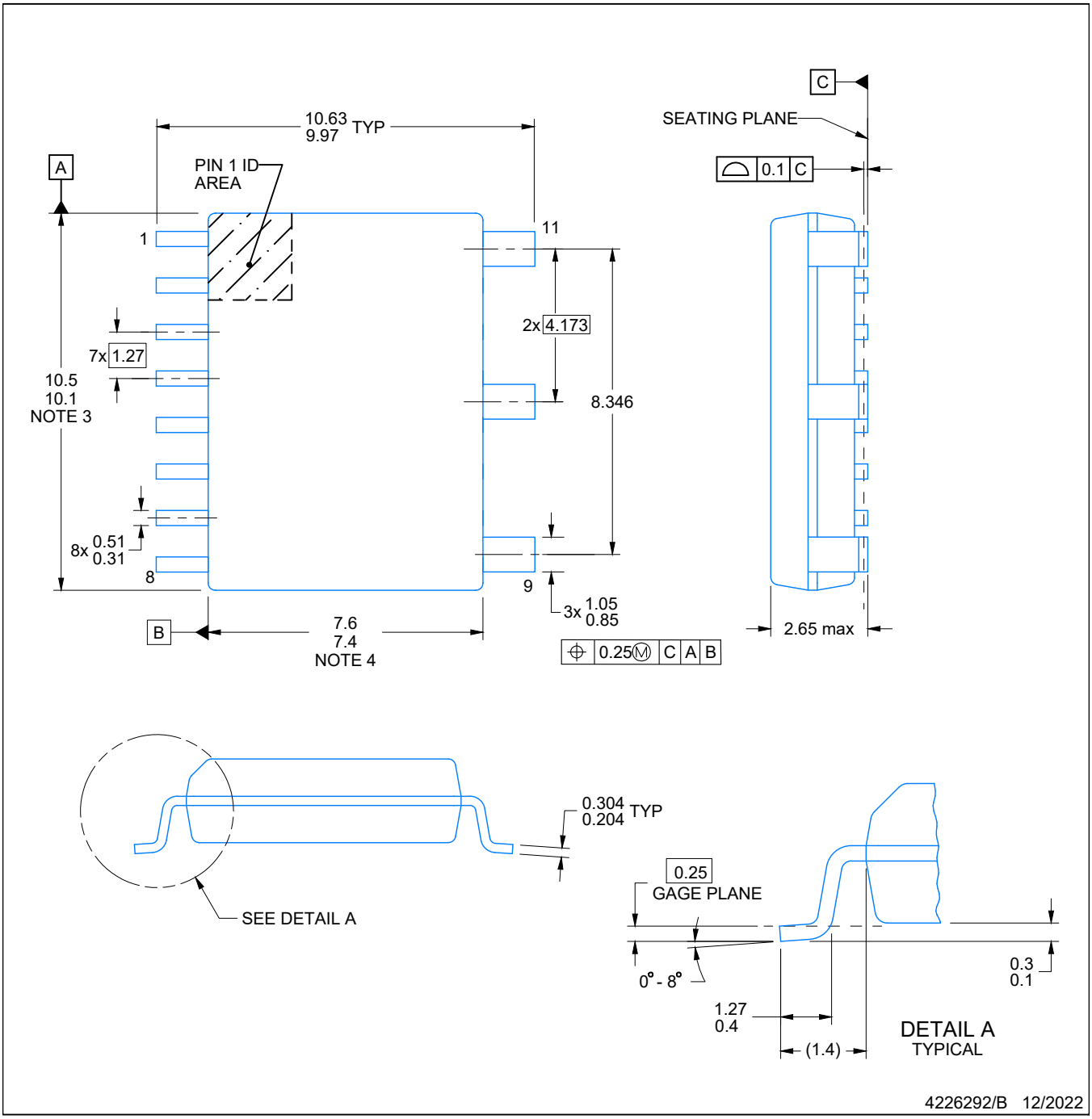
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSI2260QDWQRQ1	SOIC	DWQ	11	2000	350.0	350.0	43.0

PACKAGE OUTLINE

DWQ0011A

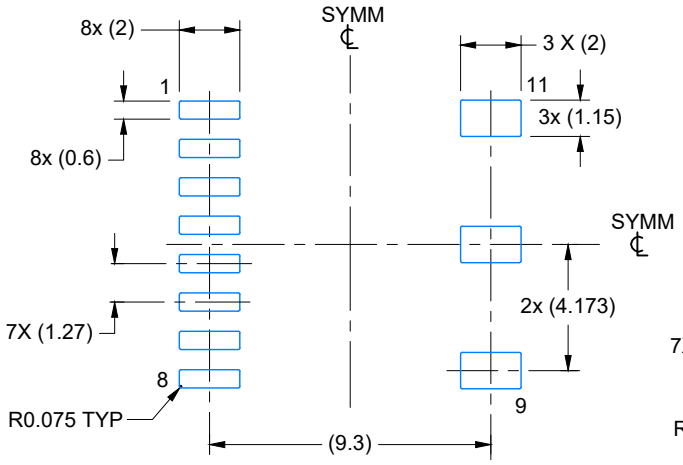
SOIC - 2.65 mm max height

SMALL OUTLINE PACKAGE

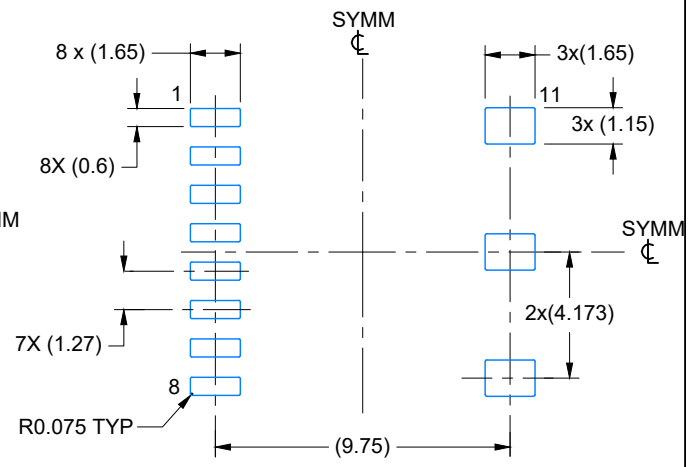


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

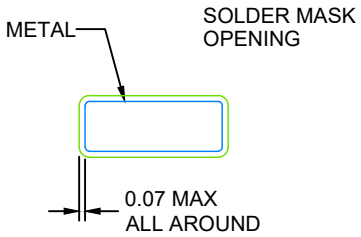


IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

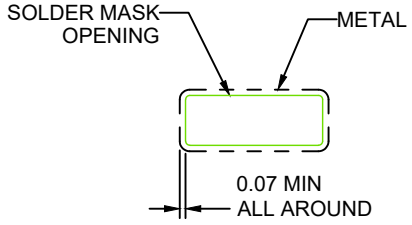


HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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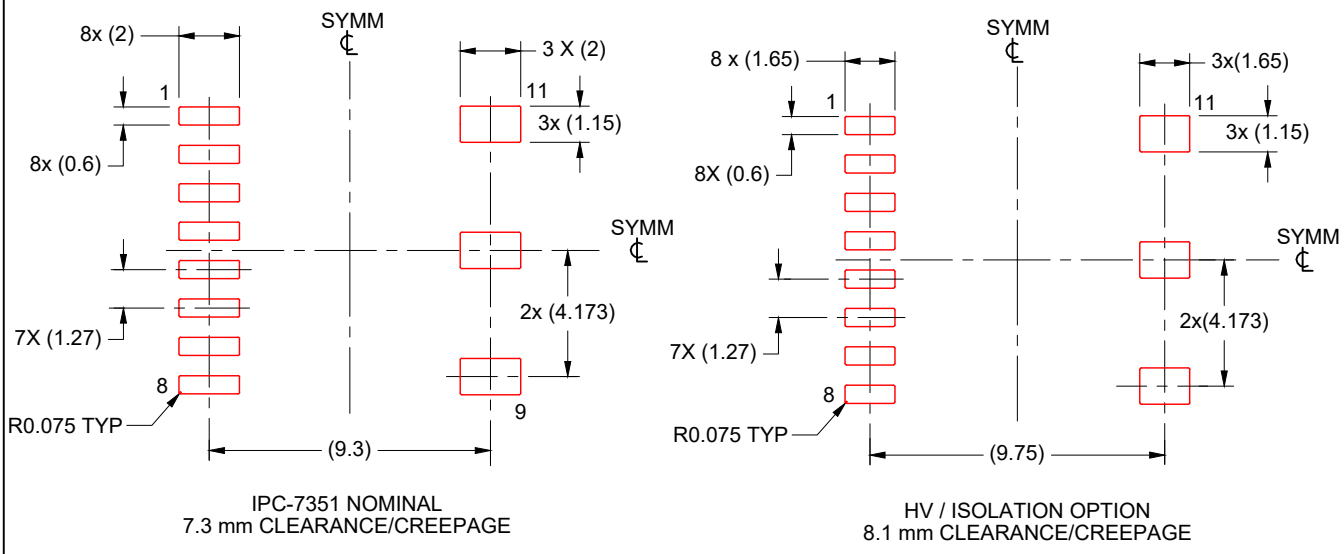
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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