TPSM81299 95nA Quiescent Current, 5.5V Boost Module with Input Current Limit and Fast Transient Performance

1 Features

- Input voltage range: 0.5V to 5.5V
- 0.7V minimum start-up voltage
- Input operating voltage (PVIN) down to 150mV with signal AVIN > 0.7V
- Output voltage range: 1.8V to 5.5V for device with input current limit no more than 1.2A
- Average input current limit: 5mA; 25mA; 50mA; 100mA; 250mA, 500mA, 1.2A, 1.5A (different versions)
- 95nA typical quiescent current into VOUT
- 60nA typical shutdown current into AVIN
- Up to 88% efficiency at PVIN =AVIN=3.6V, VOUT = 5V, and IOUT =10µA
- Up to 94% efficiency at PVIN=AVIN = 3.6V, VOUT = 5V, and I_{OUT} =200mA
- Fast transient performance: setting time ~8µs at PVIN=AVIN = 3.6V, VOUT = 5V, IOUT = 0A -> 200mA
- True disconnection at EN low
- Automatic PFM/PWM mode transition
- Auto pass-through at AVIN > VOUT
- Output SCP and thermal shutdown protections
- QFN package (3mm x 2.7mm x 1.27mm)

2 Applications

- Smart watch, Smart band
- Portable medical equipment
- TWS
- Optical module

3 Description

The TPSM81299 is a synchronous boost module, with inductor and converter both incorporated inside, providing 95nA ultra-low quiescent current and average input current limit. The device provides a power product for portable equipment with alkaline battery and coin cell battery. This device features high efficiency under light-load condition to achieve long operation time and average input current limit avoids battery discharging with high current.

The TPSM81299 has wide input voltage range from 0.5V to 5.5V and output voltage ranges from 1.8V to 5.5V. The device has different versions for average input current limit from 5mA to 1.5A. The TPSM81299 with 1.2A current limit supports up to 600mA output current from 3.6V to 5V conversion and achieve approximately 94% efficiency at 200mA load.

The TPSM81299 has optional fast-load transient performance at output voltage is 4.5V, 5V or 5.5V. In fast-load transient mode, the typical setting time is 8µs when output current transient from 0A to 200mA.

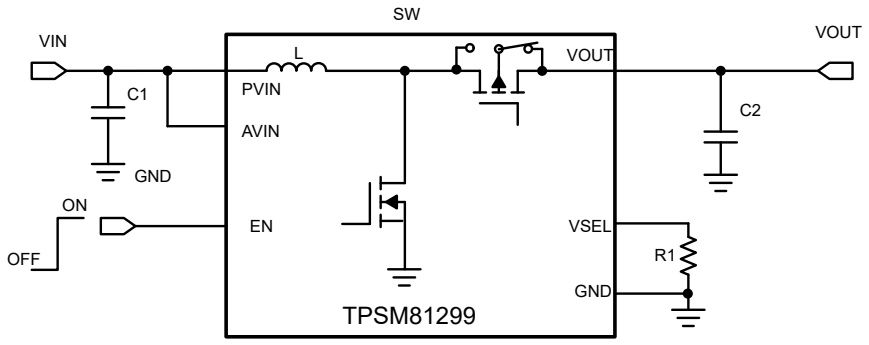
The device supports true shutdown function when it is disabled.

The TPSM81299 offers a very small solution size with 7-pin 3mm x 2.7mm QFN package .

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TPSM81299	QFN-FCMOD	3mm x 2.7mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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4 Device Comparison Table

Part Number	Average input current limit	Output voltage range
TPSM81299	1.2A	1.8V~5.5V
TPSM812991(1)	5mA	1.8V~5.5V
TPSM812992(1)	25mA	1.8V~5.5V
TPSM812993(1)	50mA	1.8V~5.5V
TPSM812994(1)	100mA	1.8V~5.5V
TPSM812995(1)	250mA	1.8V~5.5V
TPSM812996(1)	500mA	1.8V~5.5V
TPSM812997(1)	1.5A	1.8V~5.0V

(1) Product Preview. Contact TI factory for more information.

5 Pin Configuration and Functions

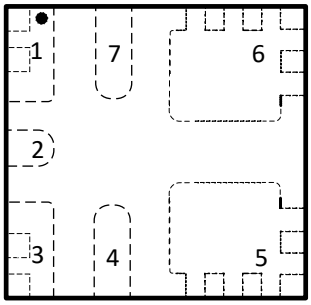


Figure 5-1. TPSM81299QFN Package, 7-Pin (Top View)

Table 5-1. Pin Functions

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VSEL	I	Boost output voltage selection pin. Connect a resistor between this pin and ground to select one of 21 output voltages.
2	VOUT	PWR	Boost converter output
3	GND	PWR	Ground
4	AVIN	I	IC signal supply input
5	PVIN	PWR	IC power supply input
6	SW	PWR	The switch pin of the converter inside, which pin is connected to the drain of the internal low-side power MOSFET , source of the internal high-side power MOSFET, and the inductor inside the module.
7	EN	I	Enable logic input. Logic high voltage enables the device. Logic low voltage disables the device.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	PVIN, AVIN,VOUT, SW, EN, VSEL	-0.3	6.5	V
	SW spike at 10 ns	-0.7	8	V
	SW spike at 1 ns	-0.7	10	V
T_J	Operating Junction Temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
PVIN	Power Input voltage	0.5		5.5	V
AVIN	Signal Input voltage	0.5		5.5	V
V_{OUT}	Boost output voltage, for device with input current limit no more than 1.2A	1.8		5.5	V
V_{OUT}	Boost output voltage, for device with 1.5 A input current limit	1.8		5.0	V
C_{IN}	Effective Input Capacitance at the VIN pin	2.2			µF
C_{OUT}	Effective Output Capacitance at the VOUT pin, with output current lower than 1A		10		µF
C_{OUT}	Effective Output Capacitance at the VOUT pin, for device with 1.5 A input current limit or with output currrent more than 1A		20		µF
T_J	Junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPSM81299 QFN Standard	TPSM81299 QFN EVM	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.2	56.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.4	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.1	14.1	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		TPSM81299 QFN Standard	TPSM81299 QFN EVM	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	24.3	29.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = -40°C to 125°C, PVIN=AVIN = 3.6V and V_{OUT} = 5.0V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		Version	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY							
AVIN	Signal Input voltage range	TPSM81299	PVIN=AVIN	0.5		5.5	V
V_{IN_UVLO}	Undervoltage lockout threshold	TPSM81299	AVIN rising, PVIN open			0.7	V
V_{IN_UVLO}	Undervoltage lockout threshold	TPSM81299	AVIN falling, PVIN open			0.5	V
I_Q	Quiescent current into AVIN pin	TPSM81299	IC enabled, No load, AVIN=3.6V , PVIN=3.6V, No switching, T_J up to 85°C		0.5		nA
I_Q	Quiescent current into VOUT pin	TPSM81299	IC enabled, No load, No switching, T_J up to 85°C		95	300	nA
I_{SD}	Shutdown current into AVIN pin	TPSM81299	EN = LOW, PVIN =3.6V , AVIN=3.6V, VOUT = 0 V		60		nA
I_{LKG_SW}	Leakage current into SW pin (from SW pin to VOUT pin)	TPSM81299	AVIN=3.6V, PVIN=0,VSW = 3.0 V, V_{OUT} = 0 V, TJ = 25°C		1	4	nA
I_{LKG_SW}	Leakage current into SW pin (from SW pin to VOUT pin)	TPSM81299	AVIN=3.6V, PVIN=0,VSW = 3.0 V, V_{OUT} = 0 V, TJ up to 85°C		1	20	nA
I_{LKG_SW}	Leakage current into SW pin (from SW pin to GND pin)	TPSM81299	AVIN=3.6V, PVIN=0,VSW = 3.0 V, V_{OUT} = 0 V, TJ = 25°C		1	15	nA
I_{LKG_SW}	Leakage current into SW pin (from SW pin to GND pin)	TPSM81299	AVIN=3.6V, PVIN=0,VSW = 3.0 V, V_{OUT} = 0 V, TJ up to 85°C		1	200	nA
OUTPUT							
V_{OUT}	Output voltage setting range	All		1.8		5.5	V
V_{OUT_ACY}	Output voltage accuracy	All	PWM, PFM mode	-2		2	%
$V_{OUT\_SNOOZE\_ACY}$	Output voltage accuracy	All	normal mode		V_{OUT_ACY}+ 37.5mV		V
			fast mode		V_{OUT_ACY}+ 15mV		V
POWER SWITCH							
$R_{DS(on)}$	High-side MOSFET on resistance	TPSM81299	V_{OUT} = 5.0 V		150		mΩ
$R_{DS(on)}$	Low-side MOSFET on resistance	TPSM81299	V_{OUT} = 5.0 V		121		mΩ
I_{LIM}	Input current limit	TPSM81299	AVIN=PVIN = 3.6 V, V_{OUT} = 5.0 V	0.96	1.2	1.44	A
I_{LH}	Inductor current ripple	TPSM81299			350		mA
L	Incorporated Power Inductance	TPSM81299			1		µH

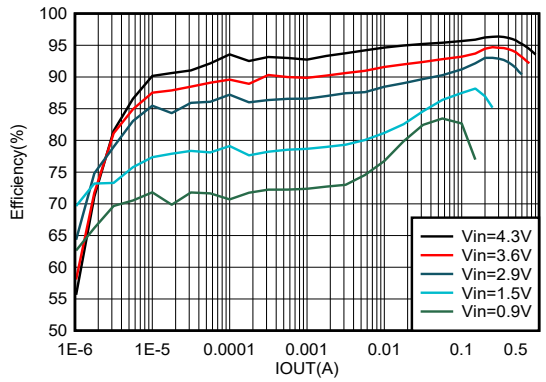
6.5 Electrical Characteristics (continued)

T_J = -40°C to 125°C, PVIN=AVIN = 3.6V and V_{OUT} = 5.0V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		Version	TEST CONDITIONS	MIN	TYP	MAX	UNIT
APPLICATION							
LOGIC INTERFACE							
V_{EN_H}	EN logic high threshold	All	AVIN >= 1.05 V			0.84	V
V_{EN_L}	EN logic low threshold	All	AVIN >= 1.05 V	0.36			V
V_{EN_H}	EN logic high threshold	All	AVIN < 1.05 V			0.8*VIN	V
V_{EN_L}	EN logic low threshold	All	AVIN < 1.05 V	0.2*VIN			V
I_{EN_LKG}	Leakage current into EN pin	All	VEN=5V		1	50	nA
R_{EN}	EN pin pulldown resistor	All	EN=low		800		kΩ
PROTECTION							
T_{SD}	Thermal shutdown threshold		T_J rising		150		°C
T_{SD_HYS}	Thermal shutdown hysteresis		T_J falling below T_{SD}		20		°C

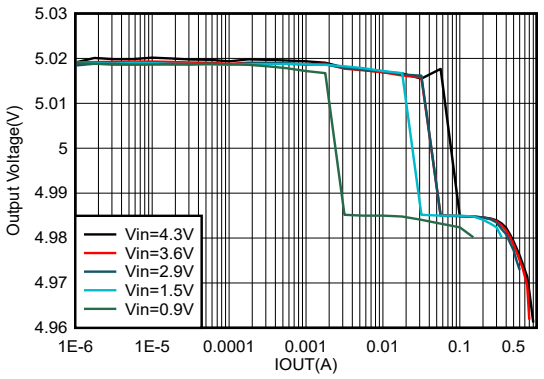
6.6 Typical Characteristics

PVIN and AVIN connected together , denoted as V_{IN} ,V_{IN}= 3.6V, V_{OUT} = 5V, Normal Mode, T_J = 25°C, unless otherwise noted



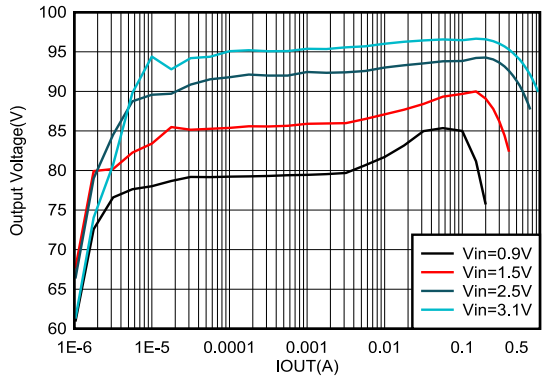
V_{IN} = 0.9V, 1.5V, 2.9V, 3.6V, 4.3V; V_{OUT} = 5.0V

Figure 6-1. 5.0V VOUT Efficiency with Different Inputs Under Normal Mode



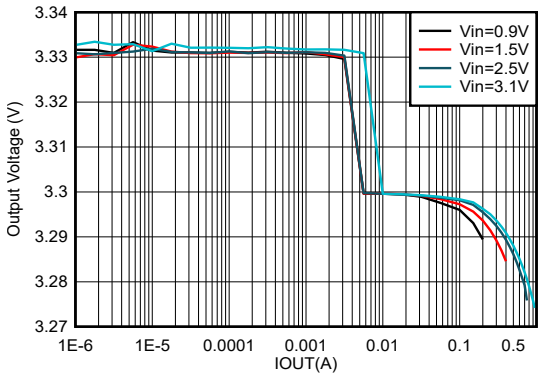
V_{IN} = 0.9V, 1.5V, 2.9V, 3.6V, 4.3V; V_{OUT} = 5.0V

Figure 6-2. 5.0V VOUT Load Regulation with Different Inputs Under Normal Mode



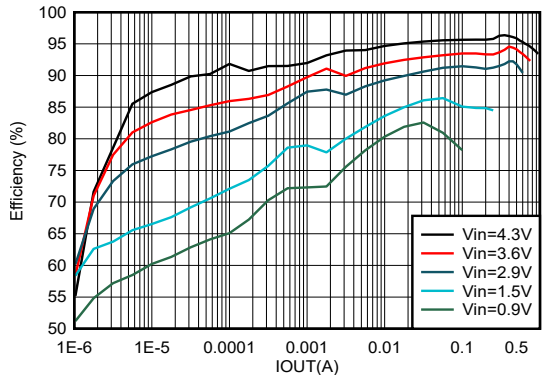
V_{IN} = 0.9V, 1.5V, 2.5V, 3.1V; V_{OUT} = 3.3V

Figure 6-3. 3.3V VOUT Efficiency with Different Inputs Under Normal Mode



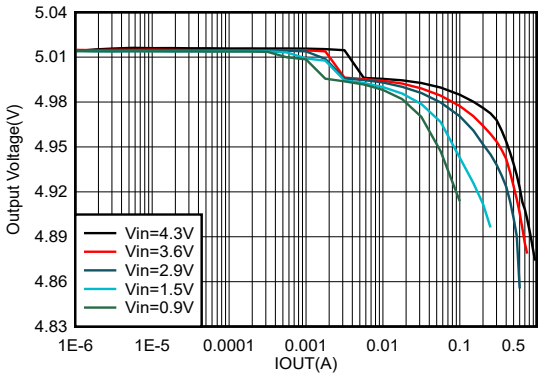
V_{IN} = 0.9V, 1.5V, 2.5V, 3.1V; V_{OUT} = 3.3V

Figure 6-4. 3.3V VOUT Load Regulation with Different Inputs Under Normal Mode



V_{IN} = 0.9V, 1.5V, 2.9V, 3.6V, 4.3V; V_{OUT} = 5.0V

Figure 6-5. 5.0V VOUT Efficiency with Different Inputs Under Fast Mode

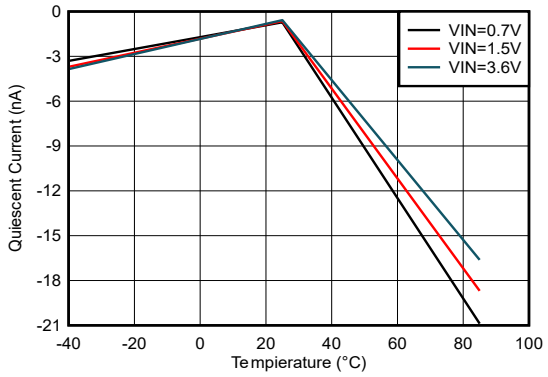


V_{IN} = 0.9V, 1.5V, 2.9V, 3.6V, 4.3V; V_{OUT} = 5.0V

Figure 6-6. 5.0V VOUT Load Regulation with Different Inputs Under Fast Mode

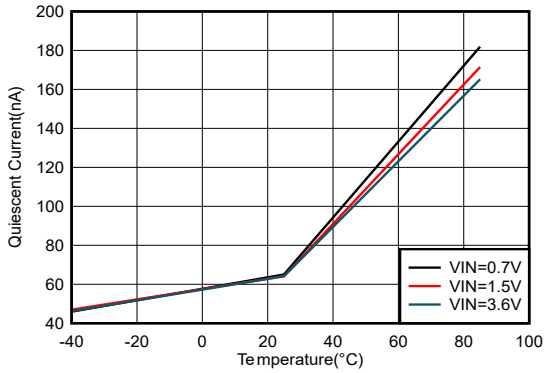
6.6 Typical Characteristics (continued)

PVIN and AVIN connected together , denoted as V_{IN} ,V_{IN}= 3.6V, V_{OUT} = 5V, Normal Mode, T_J = 25°C, unless otherwise noted



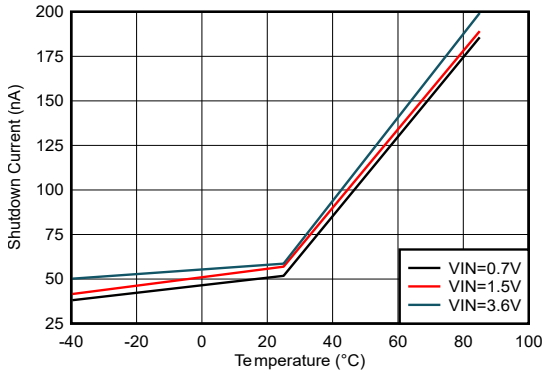
V_{IN} = 0.7V, 1.5V,3.6V; V_{OUT} = 5.0V, no switching

Figure 6-7. Quiescent Current into AVIN vs Temperature



V_{IN} = 0.7V, 1.5V,3.6V; V_{OUT} = 5.0V, no switching

Figure 6-8. Quiescent Current into VOUT vs Temperature



V_{IN} = 0.7V, 1.5V,3.6V; V_{OUT} = 5.0V

Figure 6-9. Shutdown Current into AVIN vs Temperature

7 Detailed Description

7.1 Overview

The TPSM81299x is a synchronous step-up module and operates in a hysteretic current control scheme. The TPSM81299x has a wide input voltage supply range between 0.5V and 5.5V (0.7V rising voltage for start-up). The TPSM81299x only consumes 95nA quiescent current and achieves high efficiency under light load condition.

The TPSM81299 device provide an input current limit of 1.2A. The TPSM81299x family provide an input current limit ranging from 5 mA to 1.5 A. A device with an input current limit of no more than 1.2A is able to have an output voltage set between 1.8V and 5.5V. For 1.5A version device, the Vout is recommended to set from 1.8V to 5.0V.

The TPSM81299x provides a fast transient performance mode and accurate load regulation mode for different system.

7.2 Functional Block Diagram

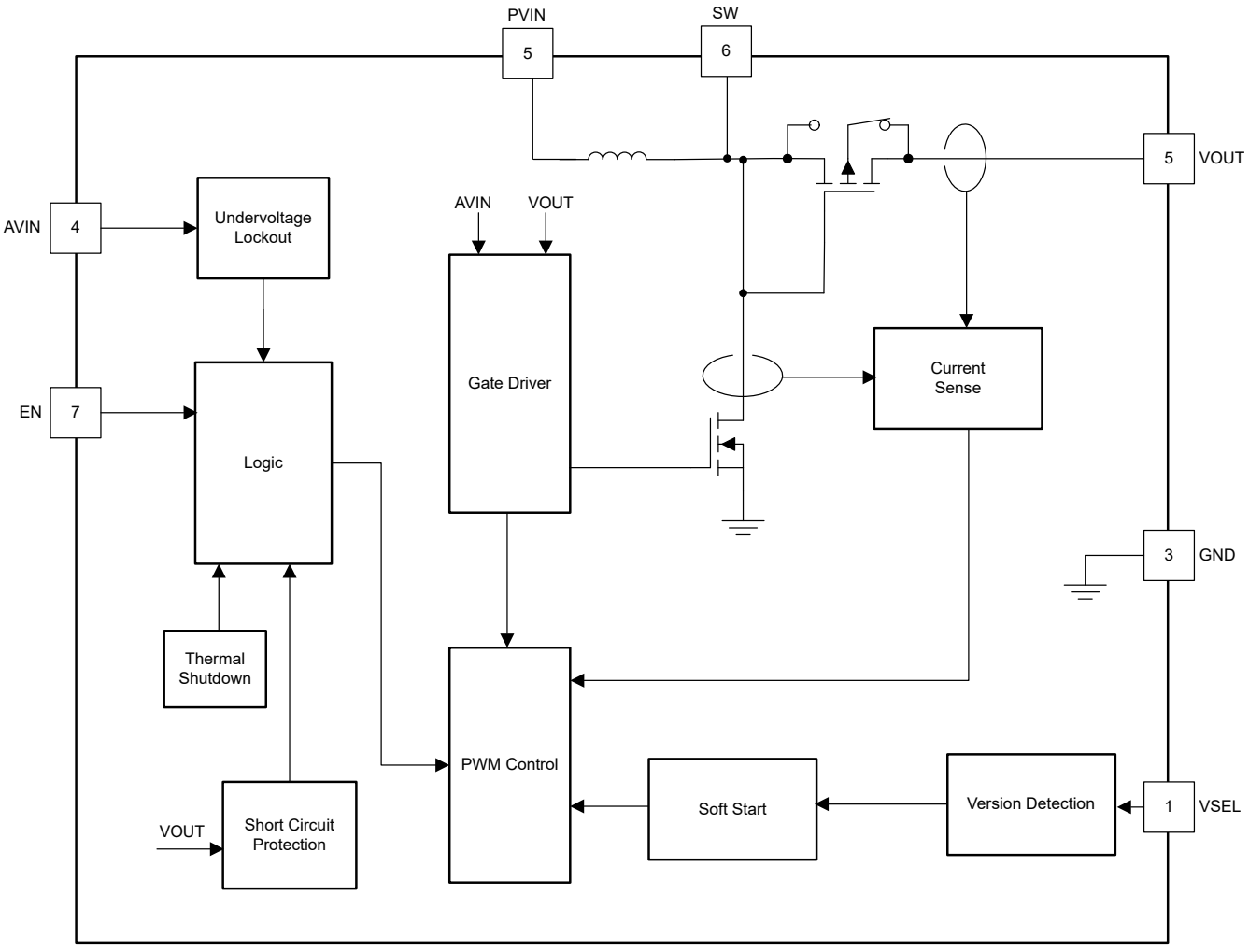


Figure 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Boost Control Operation

The TPSM81299 boost module is controlled by a hysteretic current mode controller. This controller regulates the output voltage by keeping the inductor ripple current constant in the range of 350mA and adjusting the valley current of this inductor depending on the output load. Since the input voltage, output voltage and inductor value all affect the rising and falling slopes of inductor ripple current, the switching frequency is not fixed and is determined by the operation condition. If the required average input current is lower than the average inductor current defined by this constant ripple, the inductor current goes discontinuously to keep the efficiency high under light load condition. If the load current is reduced further, the boost module enters into Burst mode. In Burst mode, the boost module ramps up the output voltage with several switching cycles. Once the output voltage exceeds a setting threshold (Vout_target + 50mV in normal mode and Vout_target + 25mV in fast load transient mode), the device stops switching and goes into a sleep status. In sleep status, the device consumes less quiescent current, 95nA. The boost module resumes switching when the output voltage is below the setting threshold (Vout_target + 25mV in normal mode and Vout_target + 10mV in fast load transient mode). The device exits the Burst mode when the output current is no longer supported in this mode.

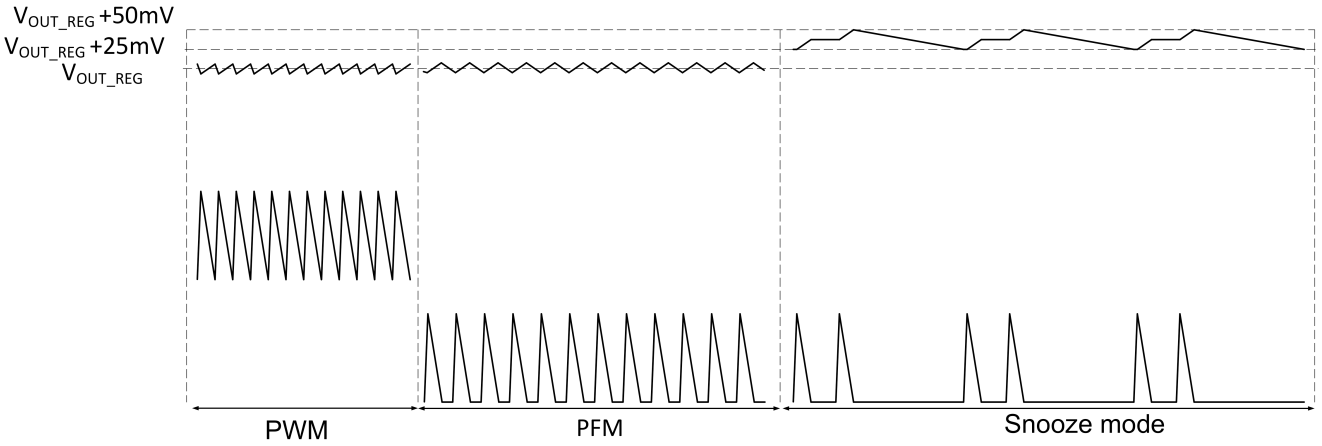


Figure 7-2. Control Modes under Different Load

7.3.2 Version Detection

The TPSM81299 supports 21 internal output voltage setting options by connecting a resistor between the VSEL pin and ground.

During start-up, when output voltage reaches close to 1.8V, the device starts to detect the configuration conditions of the VSEL pin. The TPSM81299 checks the VSEL pin by lowering resistance setting options to higher setting options until the user finds the setting configuration by a 10µs clock. After detecting the configuration, the TPSM81299 latches the setting output regulation voltage.

The TPSM81299 does not detect the VSEL pins during operation, so changing the resistor during operation does not change the VSEL setting. Toggling the EN pin during operation is one way to refresh it.

For proper operation, TI suggests that setting the VSEL resistance accuracy to 1% and the parasitic to less than 10pF.

Table 7-1. VSEL Pin Configuration

Resistance (kΩ)	VOUT_REG (V)	Resistance (kΩ)	VOUT_REG (V)	Resistance (kΩ)	VOUT_REG (V)	Resistance (kΩ)	VOUT_REG (V)
0(GND)	3.3	12.1	4.5	49.9	3.6	191	2.5
3.01	5.5	14.7	4.5(fast)	75	3.5	237	2.2
4.75	5.5(fast)	18.2	4.3	100	3.2	294	2
6.19	5.2	22.6	4	124	3	365	1.8
7.87	5	28.7	3.8	154	2.8	442/ VOUT pin	5(fast)
9.76	4.8						

7.3.3 Undervoltage Lockout

The TPSM81299 has a built-in undervoltage lockout (UVLO) circuit so that the device works properly. When the input voltage is above the UVLO rising threshold of 0.7V , which enables the TPSM81299 to boost the output voltage. After the TPSM81299 starts up and the output voltage is above 1.8V, the TPSM81299 works with the input voltage as low as 0.5V.

7.3.4 Switching Frequency

The TPSM81299 boost module does not have fixed frequency and it maintains a constant inductor ripple current in the range of 350mA, so the frequency is determined by the operation condition. The frequency is approximately 3MHz when the input is 3.6V, output is 5V, inductor is 1µH. Refer to calculate the efficiency. The estimated switching frequency f in continuous current mode is calculated by Equation 1. The switching frequency is not a constant value, but is determined by inductance, input voltage, and output voltage.

$$f = \frac{V_{IN} \times (V_{OUT} - V_{IN} \times \eta)}{L \times I_{LH} \times V_{OUT}} \quad (1)$$

where

- L is the inductor value, 1uH typically in the module
- V_{IN} is the power input voltage
- V_{OUT} is the output voltage
- I_{LH} is the inductor current ripple, typically 350mA
- η is the converting efficiency

7.3.5 Average Input Current Limit

The TPSM81299 employs the input average current protection (OCP) function. If the inductor average current reaches the current limit threshold ILIM, the control loop limits the inductor average current. In this case the output voltage decreases until the power balance between input and output is achieved. If the output drops below the input voltage, the TPSM81299 enters Down Mode. If the output drops below 1.6V, the TPSM81299 enters into startup process again. In Pass-Through operation, input current limit function is not enabled.

7.3.6 Enable and Disable

When the input voltage is above UVLO rising threshold and the EN pin is pulled to high voltage, the TPSM81299 is enabled. When the EN pin is pulled to low voltage, the TPSM81299 goes into true shutdown mode. In true shutdown mode, the device stops switching and the high-side MOSFET fully turns off, providing the completed disconnection between input and output. Less than 60nA input current is consumed in shutdown mode.

7.3.7 Soft-Start Timing

After the EN pin is tied to high voltage, the TPSM81299 begins to start up, referring to Figure 7-3 to see process profile. Use caution when creating the system design, there is a possibility that the input current limit is marginally different than the defined value during the soft start process.

When output voltage is lower than 0.5V, TPSM81299 works in short circuit protection mode, at which time the current limit is roughly 20mA to mitigate the power loss. As output voltage ramps higher than 0.5V, whereas before reaching 1.8V, the device operates at the boundary of Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM). As a result, the inductor peak current is limited to around 350mA during this stage, and the average inductor current is limited to 80mA. After the output voltage rises to 1.8V, the TPSM81299 starts to detect the output voltage configuration of the VSEL pins, then latches the configuration. The version detection time depends on the resistance at VSEL pin, the higher resistance, the longer version detection time. For example, for 5V normal version, the TPSM81299 needs approximately 170µs for version detection. After version detection, TPSM81299 continues switching and output rises further. The internal soft-start time is approximately 1.3ms, and the output soft start time varies with the different output capacitance, load condition, and configuration conditions. The average input current limits after version detection stage are slightly different among TPSM81299 family devices. In terms of the higher input current limit version device, the actual average inductor current limit is even smaller than defined input current limit, when output voltage is lower than 2.5V and higher than 1.8V, in order to reduce the inrush current during start up. For instance, the TPSM81299 and TPSM812997 limits the inductor average current lower than 500mA and TPSM812996 limits the inductor average current lower than 250mA, when output voltage is ranging between 1.8V and 2.5V. After output voltage increases to 2.5V, the input current limit is back to normal defined value, namely TPSM81299 back to 1.2A , TPSM812996 back to 500mA, and TPSM812997 back to 1.5A. For the low input current limit versions TPS612991/2/3/4/5, the input current limit is the same as the defined value once the output voltage is higher than 1.8V. Typically the device works at DCM during start up.

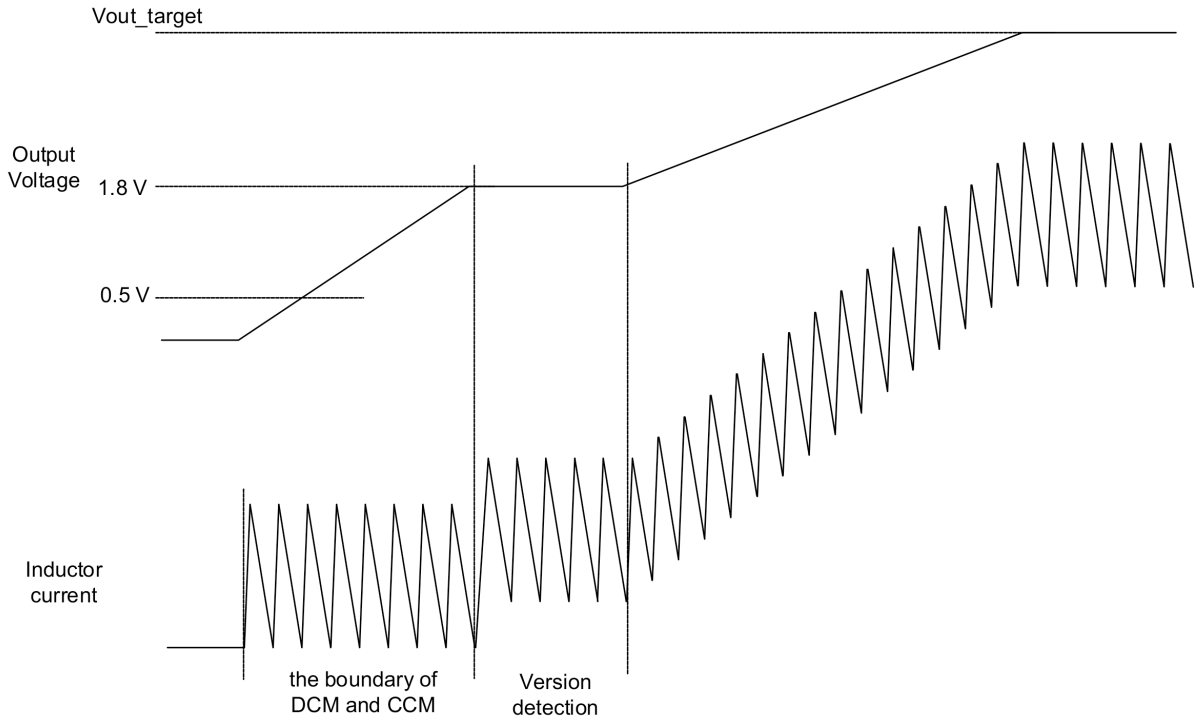


Figure 7-3. Soft-Start Timing

7.3.8 Down Mode

During the start-up, when the input voltage is higher than the output voltage, the TPSM81299 works at the down mode to keep the switching. In the Down Mode, the behavior of the rectifying PMOS by pulling its gate to input voltage instead of to ground. In this way, the voltage drop across the PMOS is increasing as high as to regulate the output voltage. The high side PMOS works under saturation area, thus the efficiency is much lower than boost mode. The power loss also increases in this mode, which needs to be taken into account for thermal consideration. Moreover, the current limit decreases as well under down mode, with TPSM81299 decreasing by 20% and TPSM812994 decreasing by 40%.

7.3.9 Pass-Through Operation

The TPSM81299 features down mode and pass-through operation when input voltage is close to or higher than output voltage.

During down mode operation, the device regulates the output voltage to the target voltage even when the input voltage is higher than the output voltage. The control circuit changes the behavior of the rectifying P-channel MOSFET by pulling its gate to input voltage instead of to ground. In this way, the voltage drop across the P-channel MOSFET is increasing as high as to regulate the output voltage.

In pass through mode, the TPSM81299 stops switching and turns on the high-side P-channel MOSFET. The output voltage is the input voltage minus the voltage drop across the DCR of the inductor and the on-resistance ($R_{DS(on)}$) of the P-channel MOSFET. During pass though operation, the device disables the input current limit function, reverse current protection, and thermal shutdown.

For the input current limit is equal or higher than 250mA version, with input voltage ramping up, the device goes into down mode when AVIN >VOUT-35mV. The device stays in down mode until AVIN >VOUT+100mV and then goes automatically into pass through operation. In the pass through operation, output voltage follows input voltage. The TPSM81299exits pass though operation and goes back to boost mode when the output voltage drops below the setting target voltage minus 75mV.

For the input current limit equal or lower than 100mA version, with input voltage ramping up, the device goes into down mode when AVIN >VOUT-35mV(Vboost_down). It stays in down mode until AVIN >VOUT+38mV(Vdown_pass) and then goes automatically into pass through operation. In the pass through operation, output voltage follows input voltage. The TPSM81299 exits pass though operation and goes back to boost mode when the output voltage drops below the setting target voltage minus 78mV(Vpass_boost)device.

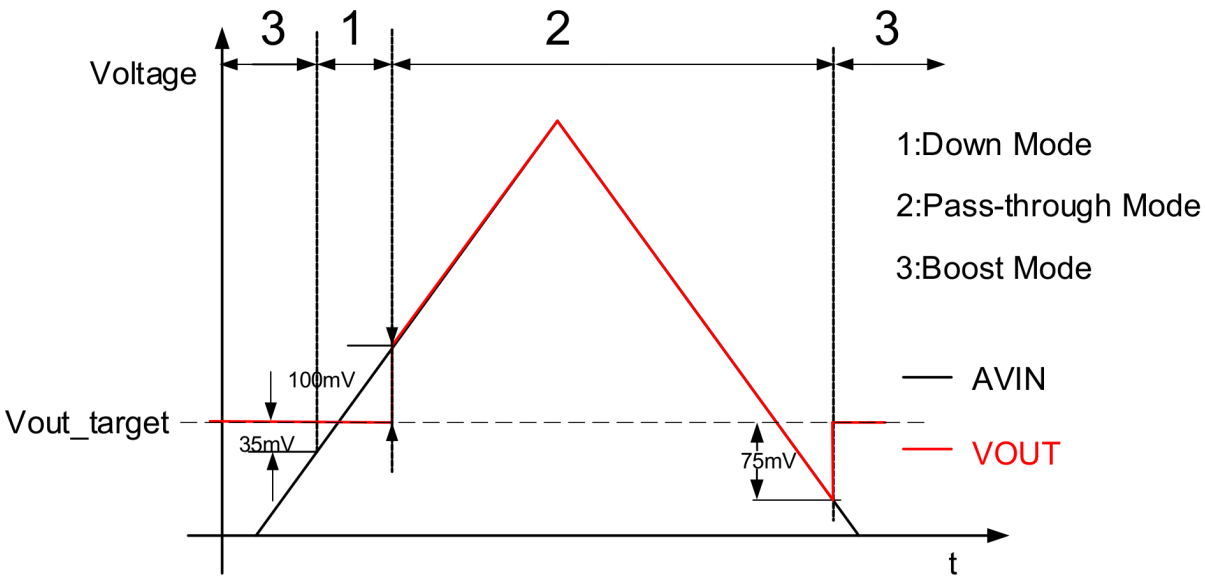


Figure 7-4. Mode Transition for 250mA and Higher Input Current Limit Version

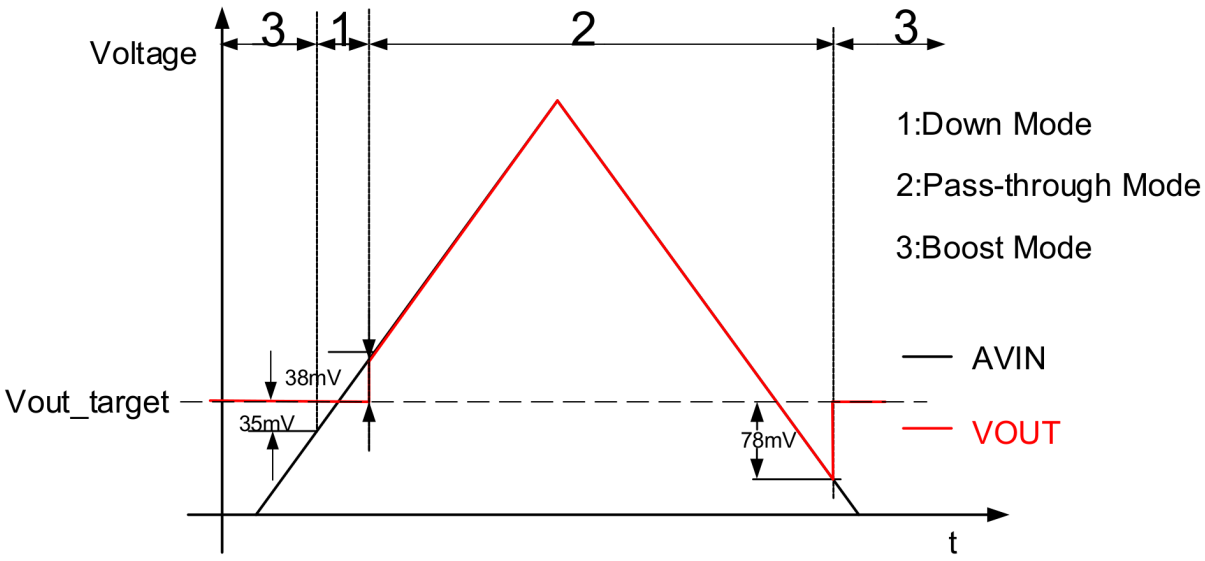


Figure 7-5. Mode Transition for 100mA and Lower Input Current Limit Version

7.3.10 Output Short-to-Ground Protection

When the VOUT pin is short to ground and the output voltage declines to less than 0.5V, the TPSM81299 device begins to limit the inductor current, the same with soft-start operation. The TPSM81299 works at the boundary of discontinuous conduction mode (DCM) and continuous conduction mode (CCM) when the input voltage is lower than 1.8V and works at DCM when input voltage is higher than 1.8V.

After the short circuit is released, the TPSM81299 goes through the soft-start sequence again to the regulated output voltage.

7.3.11 Thermal Shutdown

The TPSM81299 goes into thermal shutdown once the junction temperature exceeds 150°C. When the junction temperature drops below the thermal shutdown temperature threshold less the hysteresis, typically 130°C, the device starts operating again.

7.4 Device Functional Modes

7.4.1 Fast Load Transient Mode and Normal Mode

The TPSM81299 has two modes, fast load transient mode and normal mode, which is selected by VSEL pin.

In the fast load transient mode, the loop response speed is fast. For example, the load transient settling time is 8 µs when output current transient from 0A to 200mA at 3.6V Vin to 5V Vout condition. But the trade-off is the load regulation. Normal mode has the better load regulation.

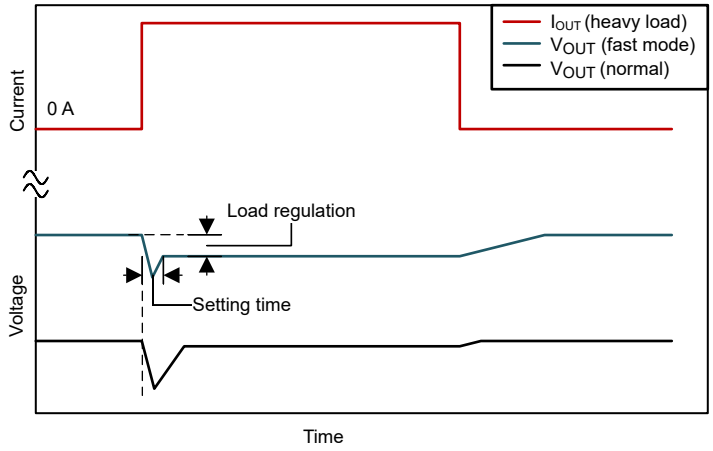


Figure 7-6. Transient Performance Comparison Under Fast Mode and Normal Mode

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPSM81299x is a synchronous step-up module and operates in a hysteretic control scheme. The TPSM81299x has a wide input voltage supply range between 0.5V and 5.5V(0.7V rising of start-up). The device only consumes 95nA quiescent current and achieves high efficiency under light load condition.

The TPSM81299 provides the input current limit of 1.2A and supports true shutdown function at EN is low.

The TPSM81299x provides a fast transient performance mode and accurate load regulation mode for different system.

8.2 Typical Application-Li-ion Battery to 5V Boost Converter Under Normal Mode

The TPSM81299 selects output voltage by setting different VSEL resistors, according to Table 8-1. Set VSEL resistor to 7.87kΩ to regulate the output to 5V with normal mode condition.

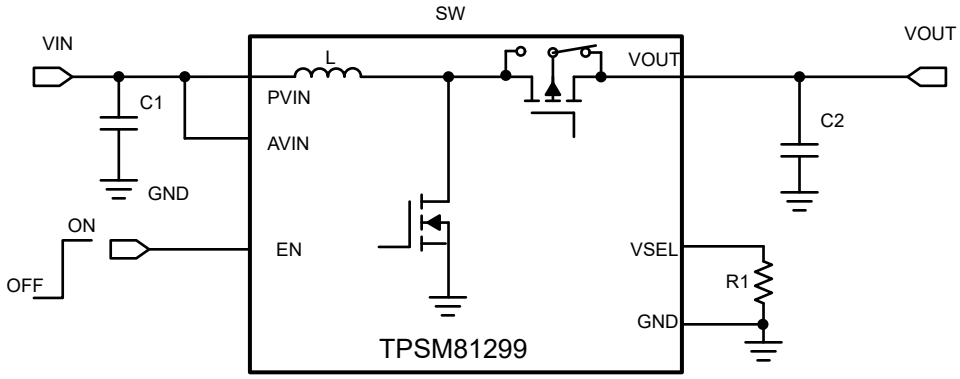


Figure 8-1. 3.6V Input Source to 5V Output Boost Converter Under Normal Mode

8.2.1 Design Requirements

The design parameters are listed in Table 8-1.

Table 8-1. Design Requirements

PARAMETERS	VALUES
Input Voltage	2.7V ~ 4.3V
Output Voltage	5V (normal mode)
Output Current	500mA
Output Voltage Ripple	± 50mV

8.2.2 Detailed Design Procedure

8.2.2.1 Maximum Output Current

The maximum output capability of the TPSM81299 is determined by the input-to-output ratio and the current limit of the boost converter. There is no need to place extra inductor outside, because a typical 1μH inductor has already be embedded. The maximum output current can be estimated by Equation 2.

$$I_{OUT\,(max)} = \frac{V_{IN}\, I_{LIM}}{V_{OUT}} \eta \quad (2)$$

where

- η is the conversion efficiency, use 85% for estimation.
- I_{LIM} is the average switch current limit.

Minimum input voltage, maximum boost output voltage, and minimum current limit I_{LIM} are used as the worst case condition for the estimation.

8.2.2.2 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. The ripple voltage is related to capacitor capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple voltage can be calculated by Equation 3.

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times V_{RIPPLE}} \quad (3)$$

where

- D_{MAX} is the maximum switching duty cycle.
- V_{RIPPLE} is the peak-to-peak output ripple voltage.
- I_{OUT} is the maximum output current.
- f_{SW} is the switching frequency.

Consider the ESR impact on the output ripple if tantalum or aluminum electrolytic capacitors are used. The output peak-to-peak ripple voltage caused by the ESR of the output capacitors can be calculated by Equation 4.

$$V_{RIPPLE(ESR)} = I_{L(P)} \times R_{ESR} \quad (4)$$

Take care when evaluating the derating of a ceramic capacitor under DC bias voltage, aging, and AC signal. For example, the DC bias voltage significantly reduces capacitance. A ceramic capacitor loses more than 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to make sure there is adequate capacitance at the required output voltage. Increasing the output capacitor makes the output ripple voltage smaller in PWM mode.

TI recommends using the X5R or X7R ceramic output capacitor in the range of 4µF to 1000µF effective capacitance. The output capacitor affects the small signal control loop stability of the boost regulator. Effective output capacitance is no less than 20µF as soon as output current is higher than 1A or the TPSM812997, the 1.5A input current limit version device is used. otherwise the boost regulator potentially becomes unstable.

8.2.2.3 Input Capacitor Selection

Multilayer X5R or X7R ceramic capacitors are excellent choices for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Place input capacitors as close as possible to the device. While a 10µF input capacitor is sufficient for most applications, using larger values can be used to reduce input current ripple without limitations. Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, a load step at the output can induce ringing at the PVIN and AVIN pin. When coupled with the output., this ringing is mistaken as loop instability or even damage to the device. In this circumstance, place additional bulk capacitance (tantalum or aluminum electrolytic capacitor) between ceramic input capacitor and the power source to reduce ringing that can occur between the inductance of the power source leads and ceramic input capacitor.

8.2.3 Application Curves

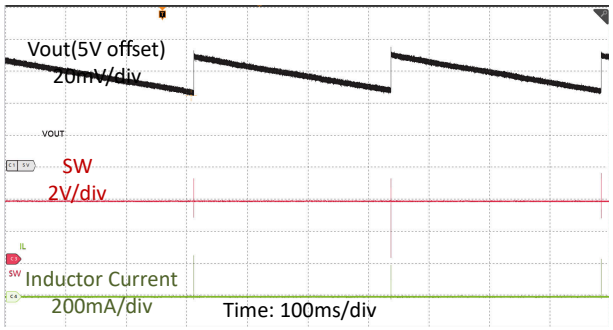


Figure 8-2. Switching Waveform at Open Load

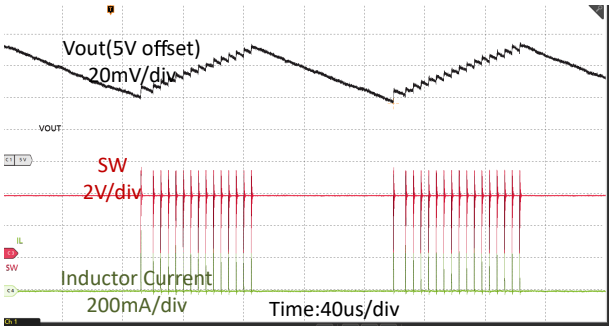


Figure 8-3. Switching Waveform at Light Load

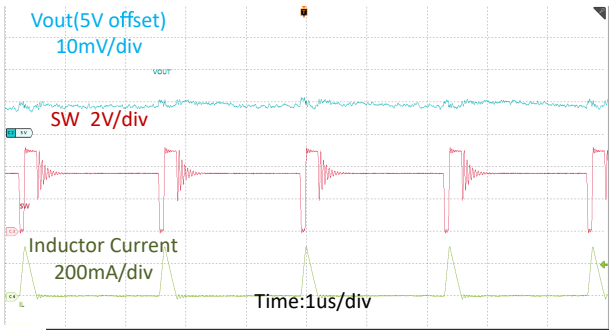


Figure 8-4. Switching Waveform at Medium Load

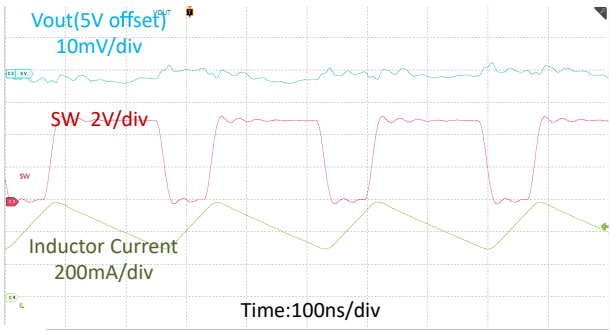


Figure 8-5. Switching Waveform at Heavy Load

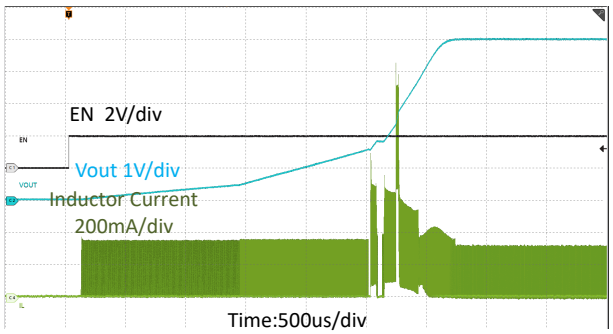


Figure 8-6. Start-Up by EN

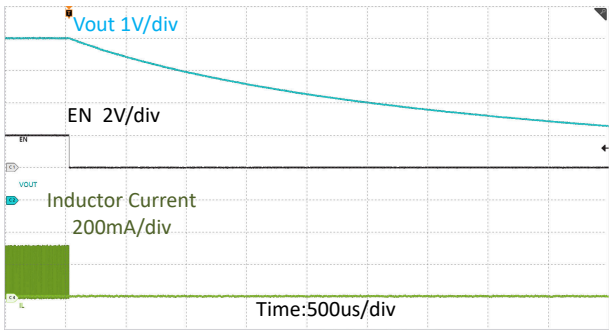
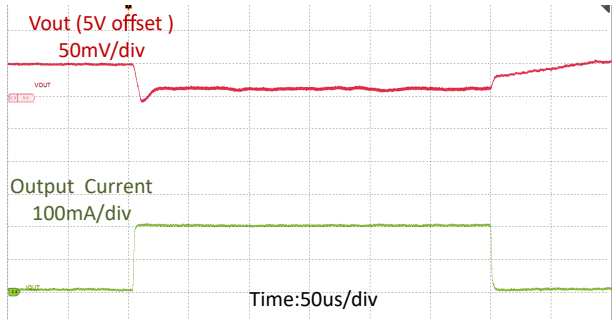
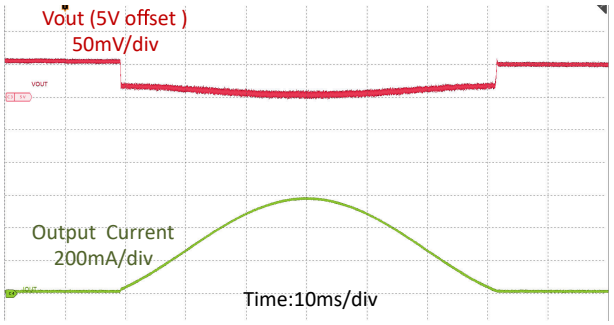


Figure 8-7. Shutdown by EN



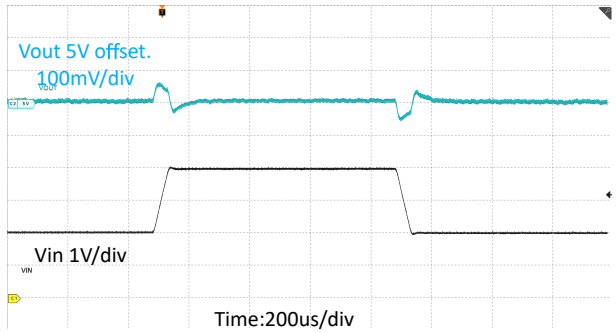
V_{IN} = 3.6V, V_{OUT} = 5V, I_{OUT} = 0 to 200mA with 20-µs slew rate

Figure 8-8. Load Transient



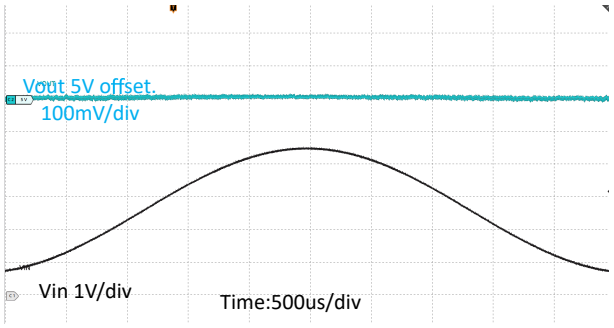
V_{IN} = 3.6V, V_{OUT} = 5V, I_{OUT} = 0 to 400mA sweep

Figure 8-9. Load Sweep



V_{IN} = 2V to 4V with 20-us slew rate, V_{OUT} = 5V, R_{load} = 50Ω

Figure 8-10. Line Transient



V_{IN} = 0.7V to 4.5V Sweep, V_{OUT} = 5V, R_{load} = 50Ω

Figure 8-11. Line Sweep

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 0.5V to 5.5V. Well regulate the input supply. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is a tantalum or aluminum electrolytic capacitor with a value of 100µF. Rate the output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TPSM81299.

8.4 Layout

8.4.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. An inefficient layout leads to stability and EMI issues. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitors are placed as close as possible to the device.

8.4.2 Layout Example

The bottom layer is a large GND plane connected by vias.

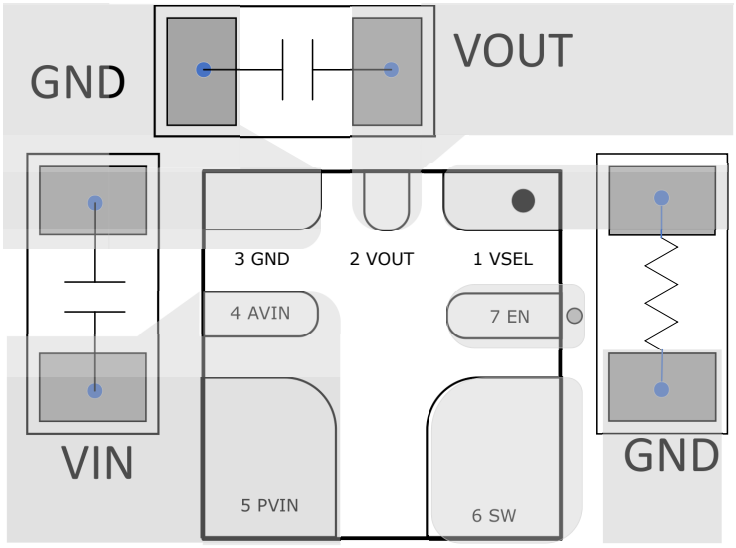


Figure 8-12. Layout Example-QFN

8.5 Thermal Information

The maximum junction temperature is restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and maintain the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 5.

$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}} \tag{5}$$

where

- T_A is the maximum ambient temperature for the application
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

The TPSM81299 comes in a QFN-FCMOD package. The real junction-to-ambient thermal resistance of the package greatly depends on the PCB type and layout. Using thick PCB copper and soldering GND pin to a large ground plate enhances the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Performing Accurate PFM Mode Efficiency Measurements Application Report*
- Texas Instruments, *Accurately Measuring Efficiency of Ultra-low-IQ Devices Technical Brief*
- Texas Instruments, *IQ: What it is, What it isn't, and How to Use it Techanical Brief*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

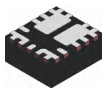
DATE	REVISION	NOTES
July 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

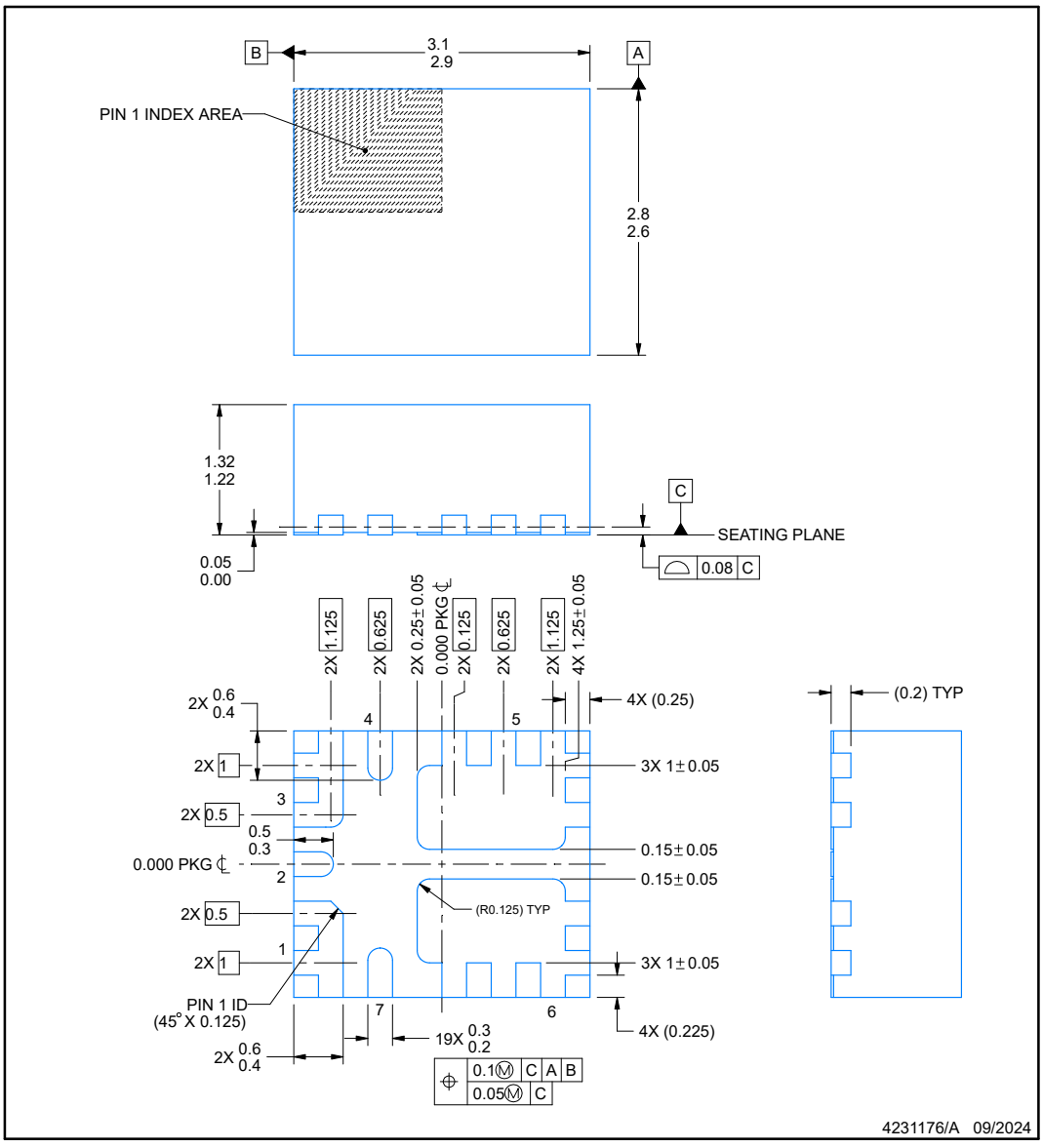
PACKAGE OUTLINE

VCM0007A



QFN-FCMOD - 1.32 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



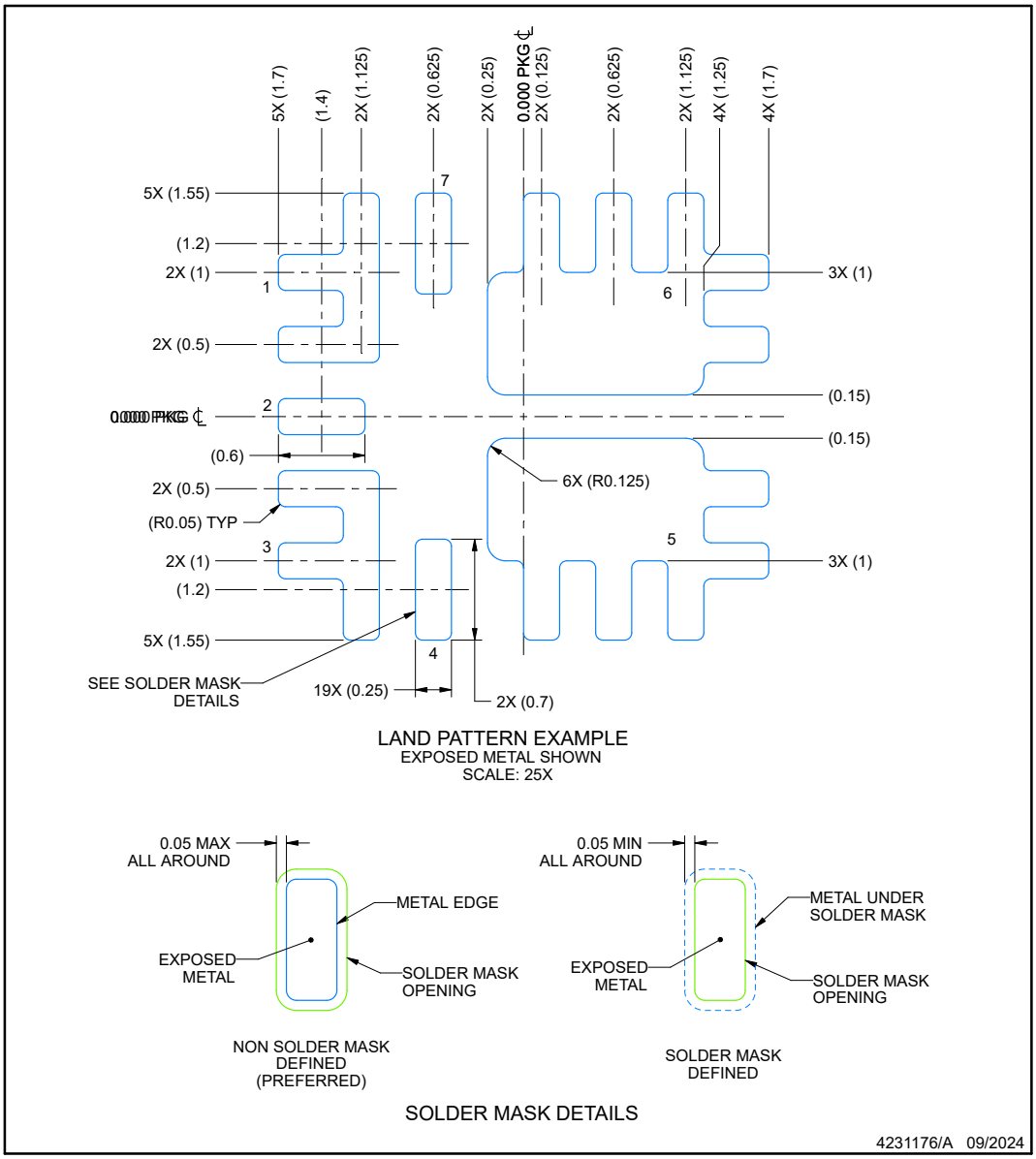
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

VCM0007A — **QFN-FCMOD - 1.32 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



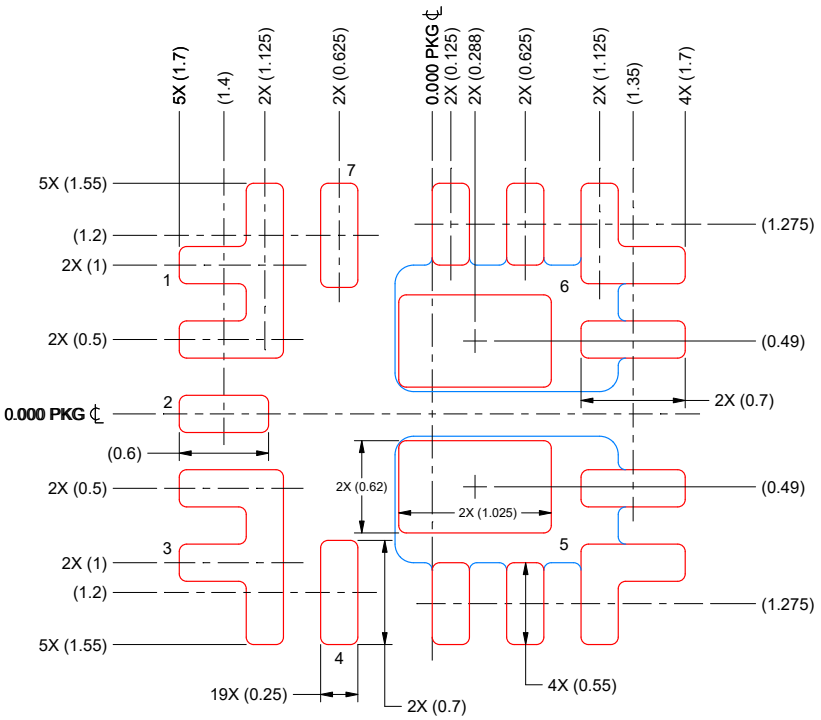
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VCM0007A — **QFN-FCMOD - 1.32 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 5 & 6: 71%

4231176/A 09/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM81299VCMR	Active	Production	QFN-FCMOD (VCM) | 7	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	81299

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

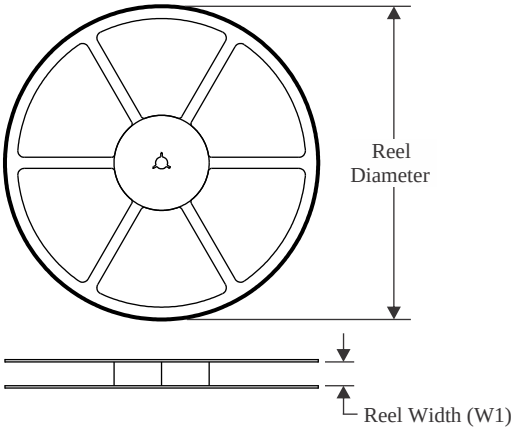
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

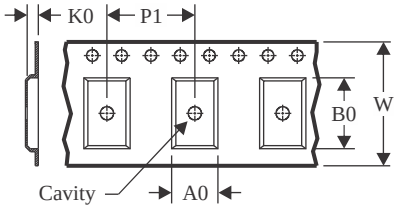
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

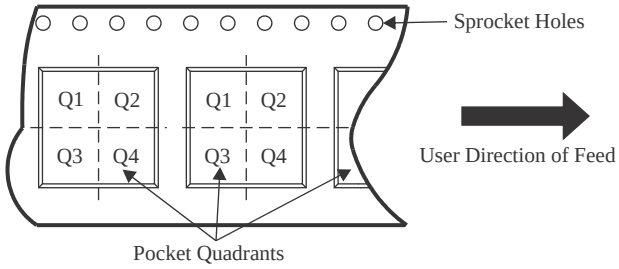


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

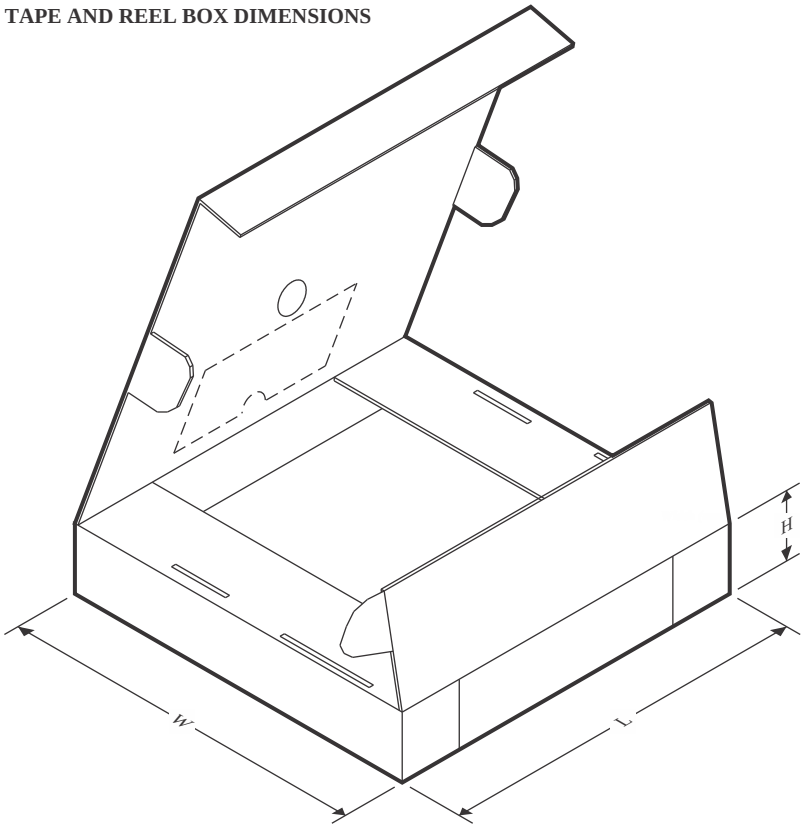
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM81299VCMR	QFN-FCMOD	VCM	7	3000	330.0	12.4	2.95	3.25	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM81299VCMR	QFN-FCMOD	VCM	7	3000	367.0	367.0	38.0

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Last updated 10/2025