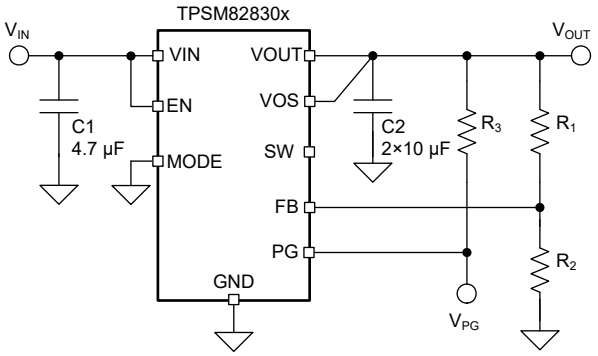
TPSM82830x, Low EMI, 2.25V to 5.5V input, 1A, 2A, and 3A Step-Down Power Modules With Integrated Inductor in QFN and MagPack™ Packages

1 Features

- Optimized EMI performance
  - Facilitates CISPR 11/32 compliance
  - MagPack technology shields inductor and IC
  - Integrated on-chip noise-filtering capacitors
- 0.5V to 4.5V adjustable output voltage
- 1% FB voltage accuracy (–40°C to 125°C T_J)
- 55mΩ dropout resistance
- 2.25V to 5.5V input voltage range
- 2.0MHz switching frequency
- 7µA operating quiescent current
- DCS-Control topology
- Excellent transient response
- MODE pin selectable FPWM or PSM
- Supports 1.2V GPIO
- 100% duty cycle for lowest dropout
- Active output discharge
- Power-good output
- Thermal shutdown protection
- Hiccup or latch-off OCP/OVP
- Package options with no bondwires
  - Standard QFN, 1.95mm height
  - Shielded MagPack package, 1.95mm height
- Create a custom design using the TPSM828303 with the WEBENCH® Power Designer

2 Applications

- Industrial PC
- LPDDR5 0.5V VDDQ Supply
- ASIC, SoC, and MCU supply
- Factory automation and control
- Medical patient monitor
- Generic point of load



Typical Application Schematic

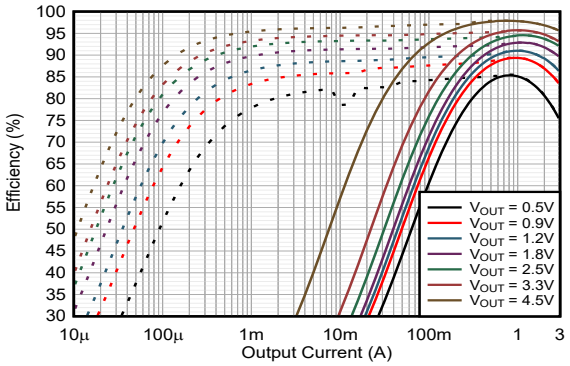
3 Description

The TPSM82830x are a family of 1A, 2A, and 3A, pin-to-pin compatible, easy-to-use, synchronous, step-down, DC/DC modules with integrated inductor and EMI reduction technologies. The devices use DCS-Control topology for fast transient response with small output capacitance. The output voltage can be set down to 0.5V with high feedback voltage accuracy of 1% over the full operating junction temperature range. A mode pin selects between power saving and forced-PWM mode. The power save mode is for longer battery life and the forced PWM mode reduces ripple with continuous conduction in the inductor at a quasi fixed switching frequency. An internal soft-start circuit reduces inrush current and a power-good signal indicates correct output voltage. HICCUP short-circuit protection combined with thermal shutdown protect device and application. The family is available in a 3.0mm × 3.0mm QFN package and in the 2.5mm × 2.6mm MagPack package.

Device Information

PART NUMBER(2)	OUTPUT CURRENT	PACKAGE(3)	PACKAGE SIZE(1)
TPSM828301	1A	RDS (QFN-FCMOD, 9)	3.0mm × 3.0mm
TPSM828302	2A		
TPSM828303	3A		
TPSM828301(4)	1A	VCB (QFN-FCMOD, 10)	2.6mm × 2.5mm
TPSM828302(4)	2A		
TPSM828303	3A		

(1) See the *Device Options* table.
(2) For more information, see Section 11.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.
(4) Preview information (not Production Data).



Efficiency at V_{IN} = 5V, VCB Package

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4 Device Options

PART NUMBER	OUTPUT CURRENT	SOFT START, tSS	OCP MODE	PACKAGE	OUTPUT VOLTAGE
TPSM828301ARDSR	1 A	300µs	Hiccup(2)	QFN RDS	Adjustable(1)
TPSM828302ARDSR	2 A	300µs	Hiccup(2)	QFN RDS	
TPSM828303ARDSR	3 A	300µs	Hiccup(2)	QFN RDS	
TPSM828303KPVCBR(3)	1 A	880µs	Hiccup(2)	QFN VCB	
TPSM828301APVCBR(3)	1 A	300µs	Hiccup(2)	QFN VCB	
TPSM828302APVCBR(3)	2 A	300µs	Hiccup(2)	QFN VCB	
TPSM828303APVCBR	3 A	300µs	Hiccup(2)	QFN VCB	

(1) For fixed output voltage versions, please contact Marketing for availability.
(2) For versions with OCP/OVP Latch-off, please contact Marketing for availability.
(3) Preview information (not Production Data).

5 Pin Configuration and Functions

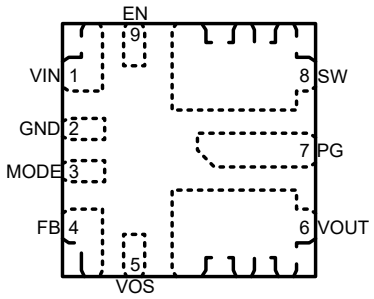


Figure 5-1. RDS Package, 9-Pin QFN-FCMOD Top View

Table 5-1. Pin Functions: RDS Package

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VIN	1	PWR	Input voltage pin. Connect the input capacitor as close as possible between V_{IN} and GND.
GND	2	PWR	Ground pin
MODE	3	I	The device runs in PSM/PWM mode when this pin pulls low and in forced-PWM mode when pulled high. This action can also be done when the device is in-operation. Do not leave this pin floating.
FB	4	I	Feedback pin. Connect the resistive output voltage divider to this pin.
VOS	5	I	Output voltage sense pin. Connect this pin directly after the inductor.
VOUT	6	PWR	Output voltage pin
PG	7	O	Power good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave this pin floating.
SW	8	PWR	Switch pin of the converter, internally connected the inductor. For lowest EMI, leave this pin unconnected or solder this pin to a small pad for thermal improvement.
EN	9	I	Device enable pin. To enable the device, pull this pin high. Pulling this pin low disables the device. Do not leave this pin unconnected.

(1) I = input, O = output, PWR = power

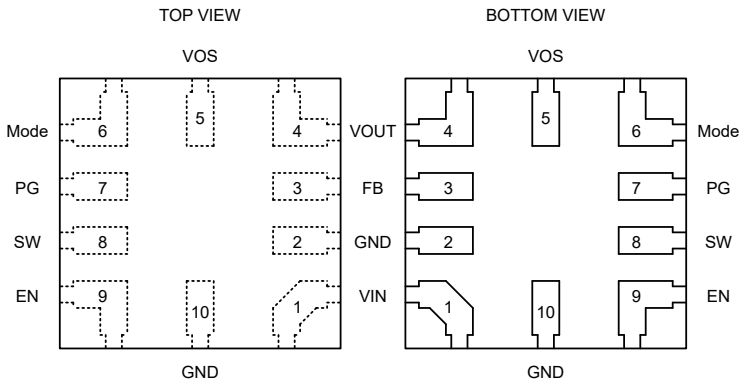


Figure 5-2. VCB Package, 10-Pin QFN-FCMOD

Table 5-2. Pin Functions: VCB Package

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VIN	1	PWR	Input voltage pin. Connect the input capacitor as close as possible between V_{IN} and GND.
GND	2, 10	PWR	Ground pins
FB	3	I	Feedback pin. Connect the resistive output voltage divider to this pin.
VOUT	4	PWR	Output voltage pin
VOS	5	I	Output voltage sense pin. Connect this pin directly after the inductor.
MODE	6	I	The device runs in PSM/PWM mode when this pin pulls low and in forced-PWM mode when pulled high. This action can also be done when the device is in operation. Do not leave this pin floating.
PG	7	O	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave this pin floating.
SW	8	PWR	Switch pin of the converter, internally connected the inductor. For lowest EMI, leave this pin unconnected or solder this pin to a small pad for thermal improvement.
EN	9	I	Device enable pin. To enable the device, pull this pin high. Pulling this pin low disables the device. Do not leave this pin unconnected.

(1) I = input, O = output, PWR = power

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage (2)	VIN, EN, MODE, FB, PG	–0.3	6	V
	SW (DC), VOS, VOUT	–0.3	V_{IN} + 0.3	V
	SW (AC , < 10 ns) (3)	–2.5	10	V
Operating junction temperature	T_J	–40	125	°C
Storage temperature	T_{stg}	–55	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal.
(3) While switching

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	± 2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.25		5.5	V
V_{OUT}	Output voltage range	0.5		4.5	V
C_{IN}	Effective input capacitance (1)	3			µF
C_{OUT}	Effective output capacitance (1)	12		200	µF
I_{OUT}	Output current range; TPSM828301			1	A
I_{OUT}	Output current range; TPSM828302			2	A
I_{OUT}	Output current range; TPSM828303 (2)			3	A
I_{PG}	Power-good input current capability			1	mA
T_J	Operating junction temperature (2)	–40		125	°C

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer´s DC bias curves for the effective capacitance vs DC voltage applied.
(2) In applications where high power dissipation and high ambient temperatures are present, the maximum output current must be derated to operate the module within the operating temperature range.

6.4 Thermal Information RDS Package

THERMAL METRIC (1)		TPSM82830xARDSR		UNIT
		RDS (QFN-FCMOD)		
		9 pins (JEDEC board)	9 pins (EVM board)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	59.4	49.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.5	n/a(2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.8	n/a(2)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.7	23.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics note.
(2) Not applicable to an EVM.

6.5 Thermal Information VCB Package

THERMAL METRIC(1)		TPSM828303PVCBR		UNIT
		VCB (QFN-FCMOD)		
		10 pins (JEDEC board)	10 pins (EVM board)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.1	66.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.1	n/a(2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.4	n/a(2)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	(–1.7)(3)	(–1.6)(3)	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.2	35.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics note.
(2) Not applicable to an EVM.
(3) Case top temperature can be higher than temperature of active circuit because of inductor power dissipation leading to a negative Junction-to-top characterization parameter.

6.6 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 2.25 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating quiescent current	EN = V_{IN}, I_{OUT} = 0 mA, V_{OUT} = 1.8 V, MODE = GND, device not switching		7	17	µA
I_{SD}	V_{IN} shutdown supply current	EN = low, T_J = –40°C to 85°C		100	700	nA
$V_{UVLO(+)}$	Rising UVLO threshold voltage (V_{IN})		2.05	2.15	2.25	V
$V_{UVLO(hys)}$	UVLO hysteresis (V_{IN})		90	120		mV
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	T_J rising		150		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC PINs						
$V_{EN(+)}$	High-level input voltage (EN)		0.8			V
$V_{EN(-)}$	Low-level input voltage (EN)				0.35	V
$V_{MODE(+)}$	High-level input voltage (MODE)		0.8			V
$V_{MODE(-)}$	Low-level input voltage (MODE)				0.35	V
$I_{EN(LKG)}$	EN Input leakage current	V_{EN} = HIGH		10	100	nA
$I_{MODE(LKG)}$	MODE Input leakage current	V_{MODE} = HIGH		10	100	nA
STARTUP						
t_{SS}	Internal fixed soft-start time	From V_{OUT} = 0 to V_{OUT} = 95%	180	300	440	µs
t_{SS}	Internal fixed soft-start time	From V_{OUT}= 0 to V_{OUT}= 95%; only TPSM82830x***K*** versions	530	880	1300	µs
$t_{d(EN)}$	Enable delay time	From EN HIGH to device starts switching		120	220	µs

6.6 Electrical Characteristics (continued)

T_J = –40°C to +125°C, V_{IN} = 2.25 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE VOLTAGE						
V_{FB}	Feedback voltage accuracy	PWM mode(1)	495	500	505	mV
V_{FB}	Feedback voltage accuracy	PWM mode(1)	–1		+1	%
V_{FB}	Feedback voltage accuracy	PFM mode, $C_{OUT,eff}$ ≥ 15 µF	–1		+2	%
$I_{FB(LKG)}$	FB input leakage current, adjustable version	V_{FB} = 0.5 V		10	70	nA
$I_{VOS(LKG)}$	VOS input leakage current	V_{EN} = low		100	500	nA
POWER GOOD						
$V_{PG,UV(+)}$	Rising power-good threshold voltage (output undervoltage)	PG pin low, V_{FB} rising	94	96	98	%
$V_{PG,UV(-)}$	Falling power-good threshold voltage (output undervoltage)	PG pin high, V_{FB} falling	90	92	94	%
$V_{PG,OV(+)}$	Rising power-good threshold voltage (output overvoltage)	PG pin high, V_{FB} rising	108	110	112	%
$V_{PG,OV(-)}$	Falling power-good threshold voltage (output overvoltage)	PG pin low, V_{FB} falling	102.5	105	107	%
$t_{d(PG)}$	Power-good delay at start-up	Low-to-high transition on the PG pin at start up		128		µs
$t_{d(PGO)}$	Power-good deglitch delay during operation	High-to-low or low-to-high transition on the PG pin	30	45	60	µs
$I_{PG(LKG)}$	PG pin Leakage current when open drain output is high	V_{PG} = 5.0 V		10	100	nA
$V_{PG,OL}$	PG pin low-level output voltage	I_{PG} = 1 mA			0.4	V
POWER STAGE						
R_{DP}	Dropout resistance	TPSM82830x, V_{IN} ≥ 5 V, 100% mode, T_J = 25°C, VCB package		55		mΩ
R_{DP}	Dropout resistance	TPSM82830x, V_{IN} ≥ 5 V, 100% mode, T_J = 25°C, RDS package		61		mΩ
R_{DP}	Dropout resistance	TPSM82830x, V_{IN} = 2.7 V, 100% mode, T_J = 25°C		78	105	mΩ
f_{SW}	Switching frequency, PWM mode	I_{OUT} = 1 A, V_{OUT} = 1.8 V		2.0		MHz
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	TPSM828301	1.8	2.1	2.6	A
$I_{HS(OC)}$	High-side peak current limit	TPSM828302	2.7	3.3	3.9	A
$I_{HS(OC)}$	High-side peak current limit	TPSM828303	4.0	4.6	5.4	A
$I_{LS(NOC)}$	Low-side negative current limit	Sinking current limit on LS FET		–1.8		A
OUTPUT DISCHARGE						
I_{DIS}	Output discharge current on SW pin	V_{IN} > 2 V, V_{SW} = 0.4 V, EN = LOW	75	400		mA

(1) Output voltage accuracy is specified as a static parameter. For dynamic behavior refer to the corresponding sections in the datasheet.

6.7 Typical Characteristics

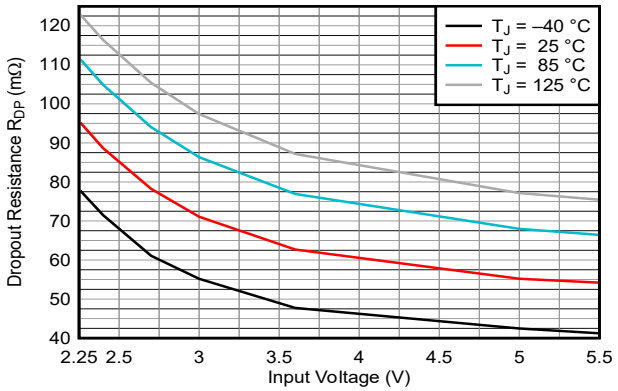


Figure 6-1. TPSM82830x Dropout Resistance RDS Package

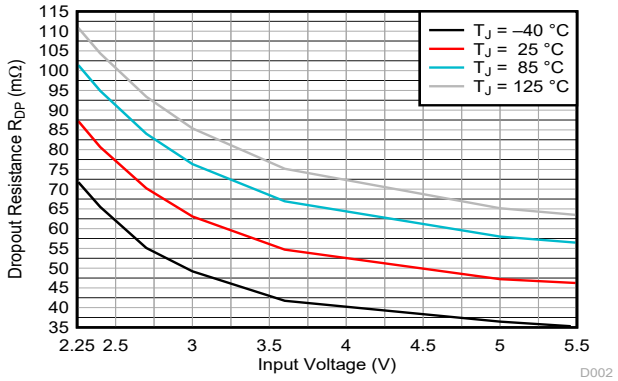


Figure 6-2. TPSM82830x Dropout Resistance VCB Package

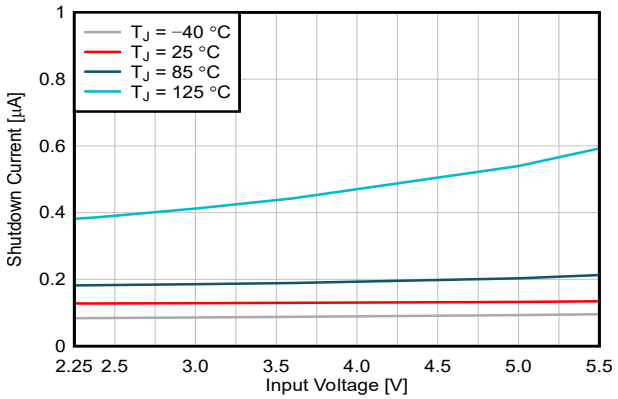


Figure 6-3. Shutdown Current

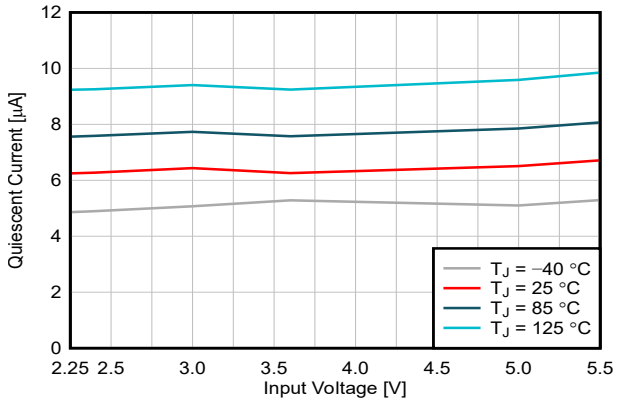


Figure 6-4. Quiescent Current

7 Detailed Description

7.1 Overview

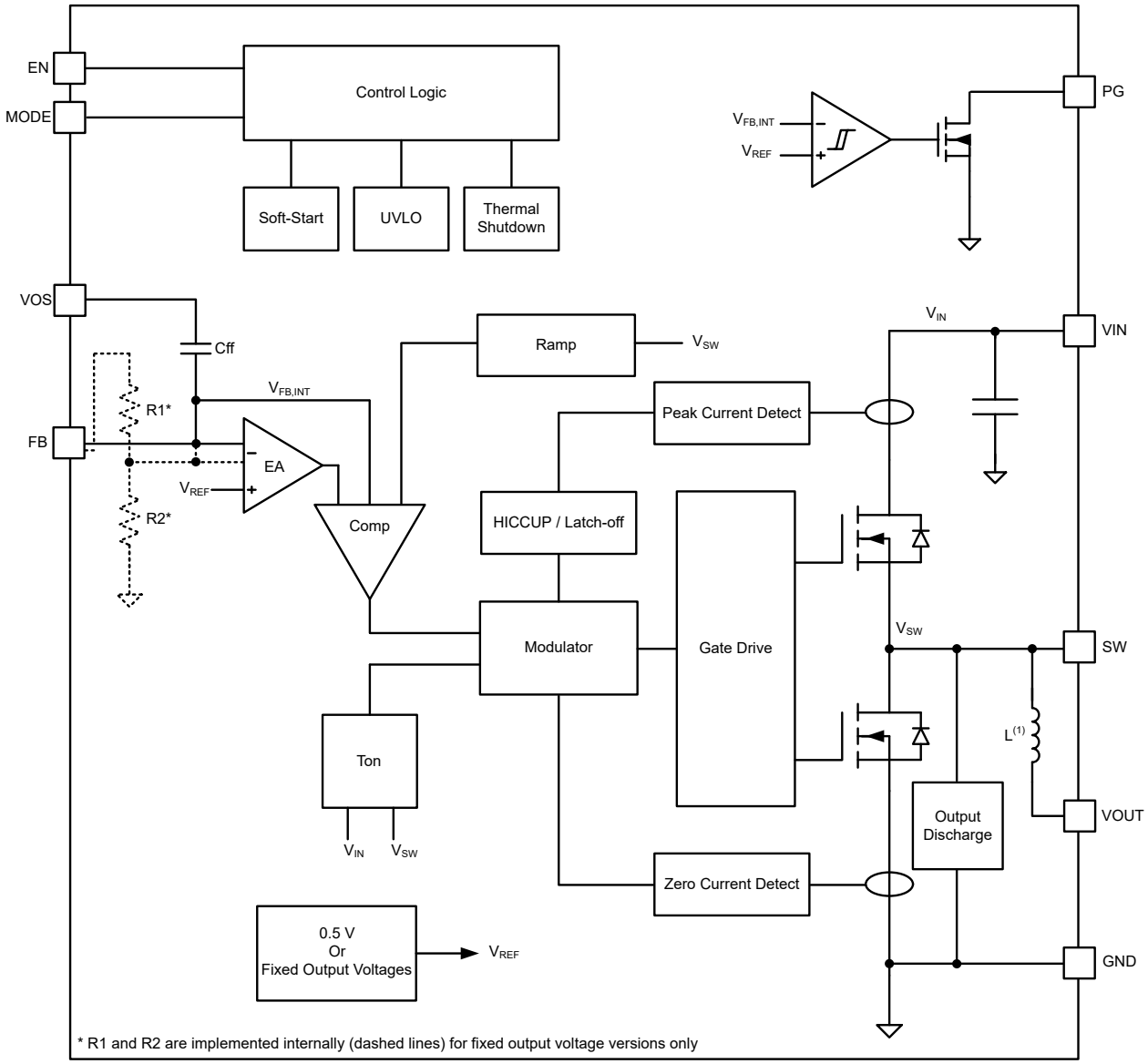
The TPSM82830x is a family of low-voltage step-down modules available in 1A, 2A and 3A versions. These devices use a DCS-Control scheme which transitions seamlessly from pulse-width modulation (PWM) at medium and high output currents to pulsed-frequency modulation (PFM) at low output currents. During PWM operation, the devices switch at 2MHz; during PFM operation, the switching frequency varies with the load current and reduces as the load current decreases. For applications that require the lowest possible output voltage ripple or a constant switching frequency, a high logic level on the MODE pin forces the devices to use PWM under all load conditions (at the expense of lower efficiency at low output currents). An external resistor-divider sets the output voltage anywhere from 0.5V to 4.5V and the nominal switching frequency is 2MHz with a controlled variation over the input voltage range.

Device variants are available that support both hiccup and latch-off protection behavior.

The TPSM82830x devices offer two significant advantages compared to previous devices in this series: Transient performance has improved significantly by usage of a fast comparator in both PFM and PWM modes, and EMI is reduced by an optimized gate driver and on-chip decoupling capacitors.

The VCB package version uses MagPack technology to deliver the highest-performance power module design. Leveraging the Texas Instruments proprietary integrated-magnetics MagPack packaging technology, these power modules deliver industry-leading power density, high efficiency and good thermal performance, ease of use, and reduced EMI emissions.

7.2 Functional Block Diagram



A. Inductance value is 470nH in RDS packageand 400nH in VCB package.

7.3 Feature Description

7.3.1 Pulse Width Modulation (PWM) Operation

If the MODE pin is LOW and at load currents larger than half the inductor ripple current, the device operates in pulse width modulation in continuous conduction mode (CCM) as shown in Figure 7-1. The PWM operation is based on an adaptive constant on-time control with stabilized switching frequency. To achieve a stable switching frequency in a steady state condition, the on-time is calculated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times 500ns \quad (1)$$

If the MODE pin is HIGH, the converter maintains a forced-PWM operation for all load currents.

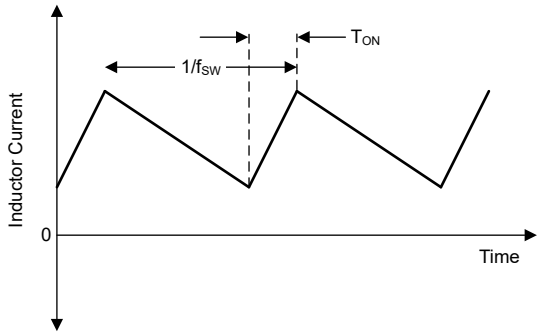


Figure 7-1. Continuous Conduction Mode (PWM-CCM) Current Waveform

7.3.2 Power Save Mode (PSM) Operation

To maintain high efficiency at light loads, the device enters power save mode (PSM) at the boundary to discontinuous conduction mode (DCM). This event happens when the output current becomes smaller than half of the ripple current of the inductor. The device operates with a fixed on-time, and the switching frequency decreases proportional to the load current as shown in Figure 7-2. Calculate as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{T_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \left[\frac{V_{IN} - V_{OUT}}{L} \right]} \quad (2)$$

Use L=470nH for the RDS package and L=400nH for the VCB package.

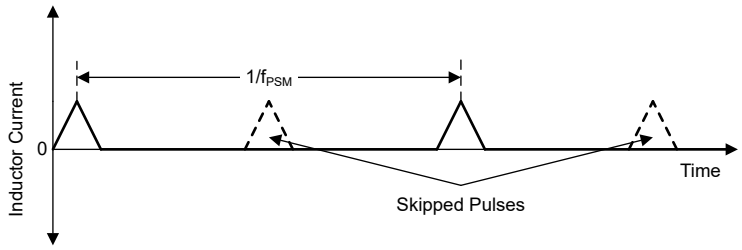


Figure 7-2. Discontinuous Conduction Mode (PSM-DCM) Current Waveform

In PSM, the output voltage rises slightly above the nominal target, which can be minimized using larger output capacitance. At duty cycles larger than 90%, the device does not enter PSM and maintains output regulation in PWM mode.

7.3.3 Start-Up and Soft Start

When the EN voltage goes High, the device starts loading the default values into the device registers. This action is done within $t_{d(EN)}$. After that, the internal soft-start circuitry controls the output voltage during start-up. This control avoids excessive inrush current and makes sure of a controlled output voltage ramp. This control also prevents unwanted voltage drops from high-impedance power sources or batteries. Finally, the PG signal has a delay $t_{d(PG)}$ at start-up. Figure 7-3 shows a start-up sequence, where the EN pin is pulled up to VIN.

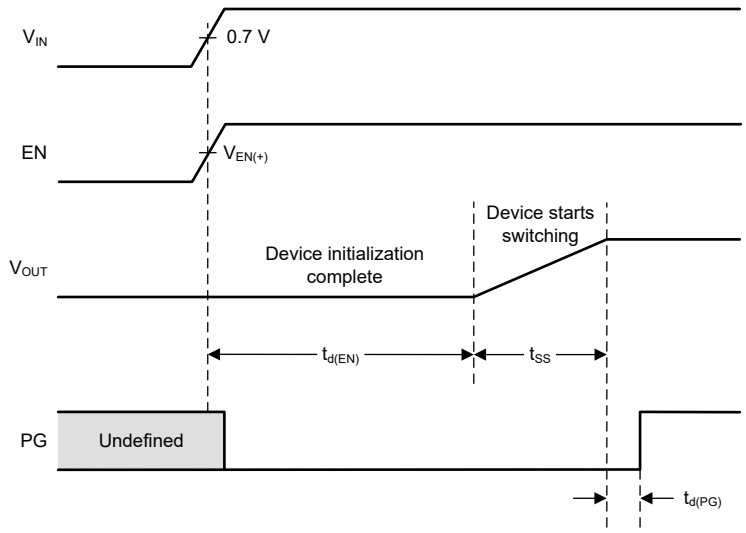


Figure 7-3. Start-Up Timing When EN is Pulled Up to VIN

Figure 7-4 shows a start-up sequence, where an external signal is connected to the EN pin. The soft start function has a second purpose. During start-up the output capacitor needs to charge. Larger output voltage combined with large output capacitance can trigger an over current event and prevent the device from starting up correctly. The circuit designer needs to select the maximum output capacitance in accordance to the target output voltage and start-up time. The TPSM82830xK version can mitigate the peak output current with a longer start-up time.

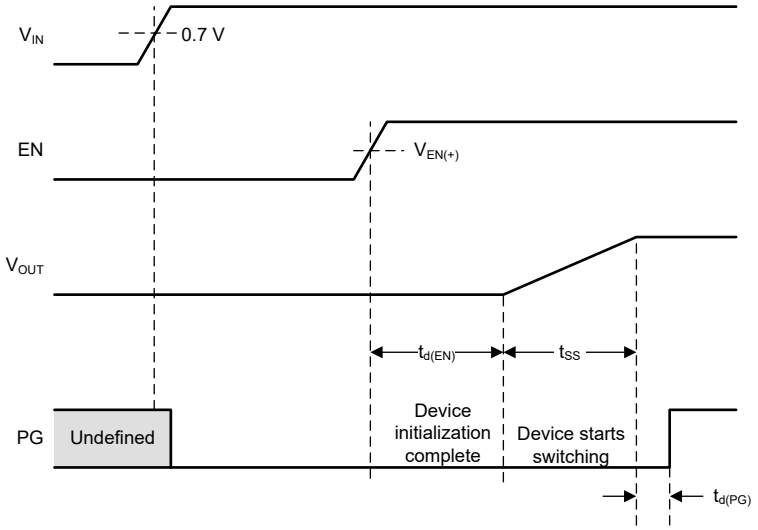


Figure 7-4. Start-Up Timing When an External Signal is Connected to the EN Pin

The TPSM82830x can start into a prebiased output if enabled for the first time. For a new prebiased operation, a power cycle is needed to disable the active output discharge. Figure 7-5 shows a start-up into a prebiased output voltage.

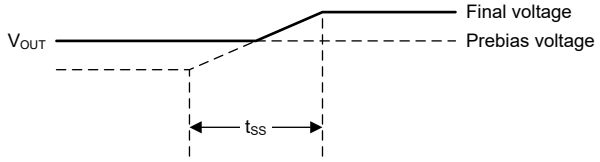


Figure 7-5. Start-Up into a Prebiased Output

7.3.4 Switch Cycle-by-Cycle Current Limit

All the devices in the family have a cycle-by-cycle current limit function. When the device detects that the current in the high-side FET exceeds the high-side current limit, either due to a heavy load or a short-circuit condition, the device immediately turns off the high-side FET and turns on the low-side FET. The high-side FET turns on again at the start of the next switching cycle. Note that because of the propagation delay in the current limit comparator (typically 60ns), the current flowing in the high-side FET when the device detects a current limit condition can be slightly higher than the current limit specified in the device Electrical Characteristics.

7.3.5 Undervoltage Lockout

The undervoltage lockout (UVLO) function prevents misoperation of the device if the input voltage drops below the UVLO threshold.

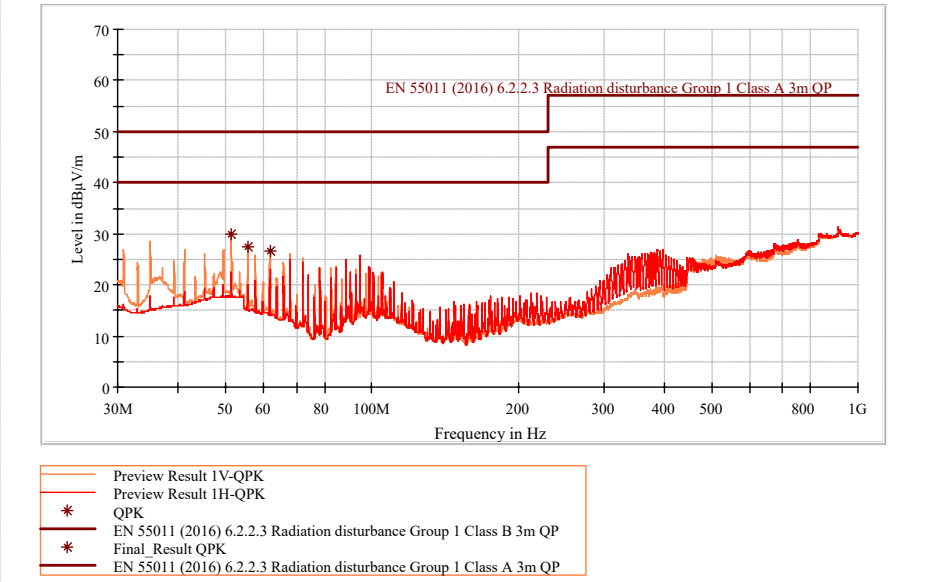
7.3.6 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 150°C (typical), the device goes in thermal shutdown with a hysteresis of typically 20°C. After T_J has decreased enough, the device resumes normal operation.

7.3.7 Optimized EMI Performance

TPSM82830x devices incorporate advanced techniques to minimize Electromagnetic Interference (EMI) and makes complying with stringent EMI standards simple. By integrating capacitors directly onto the silicon, parasitic elements are reduced and loop area is minimized, effectively reducing high-frequency noise emissions primarily above 450 MHz. The on-chip capacitors make sure of low-inductance paths for high-frequency AC switching current and damping voltage ringing.

Additionally to the on-chip capacitors, the gate driver has been improved with advanced slew rate control mechanisms and by smoothing the supply voltage. The switch node voltage is controlled in a way to reduce sharp edges and minimize voltage overshoot, consequently diminishing EMI.



The above plot is measured on the EVM with the TPSM828303ARDSR and standard BOM.

I_{OUT} = 3A V_{IN} = 5.5V V_{OUT} = 1.8V

Figure 7-6. Radiated EMI Performance (CISPR 11 Radiated Emission Test with Class A and Class B Limits)

7.3.8 VOUT Accuracy

The output voltage accuracy of TPSM82830x depends on various contributors listed in Table 7-1. Mitigation possibilities and responsibility are listed to help selecting correct design measures for the application.

Table 7-1. Output Voltage Accuracy

CONTRIBUTOR	MITIGATION	RESPONSIBILITY
Feedback divider	Higher resistor accuracy of feedback divider	Circuit designer
Error amplifier	Device calibration	Device manufacturer
Reference voltage	Device calibration	Device manufacturer
Input voltage and input voltage transients	Low impedance power source, input capacitor adapted to load step	Circuit designer
Load current and load current transients	Output capacitor adapted to load step	Circuit designer
Noise	Input filter, on die filter, pinout, layout	Circuit designer and device manufacturer
Board layout	Separate noisy signals from noise sensitive signals, control slew rate on digital signals located close to sensitive signals	Circuit designer and device manufacturer

Output transients can have significant impact on VOUT accuracy. Slow changes can be compensated by the regulation loop and do not require attendance. Fast transient like those in system on chips or microprocessors can exceed the speed of the regulation loop and require output capacitance as temporary energy reservoir. The DCS topology allows reducing the output capacitance for changes occurring over multiple switching cycles. When the load step is instant, which means the complete load step happens within one clock cycles, then sufficient output capacitance is needed. This need is supported by the TPSM82830x with large output capacitance tolerance.

The PG pin of TPSM82830x is located near the sensitive VOS pin on the die. Therefore, some impact of PG toggling on the output voltage can be seen (see PG to VOUT Influence). The effect can be minimized by keeping VOS and FB in the layout as far apart from PG as possible. If the layout is very dense then the effect can also be minimized by adding a capacitor of up to 33nF to the PG pin. As a mitigation measure, the circuit designer can add the footprint for an optional capacitor connected to PG in the layout.

7.4 Device Functional Modes

7.4.1 Enable, Disable, and Output Discharge

The device starts operation when Enable (EN) is set High. The input threshold levels are typically 0.8V for rising and 0.35V for falling signals. Do not leave EN floating. Shutdown is forced if EN is pulled Low with a shutdown current of typically 100nA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off and the output voltage is actively discharged through the SW pin by a current sink. Therefore VIN must remain present for the discharge to function.

7.4.2 Minimum Duty Cycle and 100% Mode Operation

There is no limitation for small duty cycles because, even at very low duty cycles, the switching frequency is reduced as needed to always make sure of a proper regulation.

If the output voltage (V_{OUT}) comes close to the input voltage (V_{IN}), the device enters 100% mode. While the high-side switch is constantly turned on, the low-side switch is switched off. This action is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The difference between V_{IN} and V_{OUT} is determined by the voltage drop across the high-side FET and the DC resistance of the inductor. The minimum V_{IN} that is needed to maintain a specific V_{OUT} value is estimated as:

$$V_{IN,min} = V_{OUT} + I_{OUT,MAX} \times R_{DP} \quad (3)$$

where

- $V_{IN,min}$ = Minimum input voltage to maintain an output voltage

- $I_{OUT,MAX}$ = Maximum output current
- R_{DP} = Resistance from VIN to VOUT, which includes the high-side MOSFET on-resistance and DC resistance of the inductor

7.4.3 Power Good

The TPSM82830x has a built-in power-good (PG) function. The PG pin goes high impedance when the output voltage has reached the nominal value. Otherwise, including when disabled, in UVLO or in thermal shutdown, PG is Low (see Table 7-2). The PG function is formed with a window comparator, which has an upper and lower voltage threshold. The PG pin is an open-drain output and is specified to sink up to 1mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 5.5V.

Table 7-2. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, V_{FB} ≥ 0.48V	√	
	EN = High, V_{FB} ≤ 0.56V		√
	EN = High, V_{FB} ≤ 0.525V	√	
	EN = High, V_{FB} ≥ 0.55V		√
Shutdown	EN = Low		√
Thermal shutdown	$T_J > T_{JSD}$		√
UVLO	$0.7V < V_{IN} < V_{UVLO}$		√
Power supply removal	V_{IN} < 0.7V	√	

The PG signal can be used for sequencing of multiple rails by connecting the PG signal to the EN pin of other converters. Leave the PG pin unconnected when not used. The PG rising edge and falling edge has a blanking time of $t_{d(PGO)}$, as shown in Figure 7-7. At start-up, the delay of PG signal is $t_{d(PG)}$ after soft start is finished.

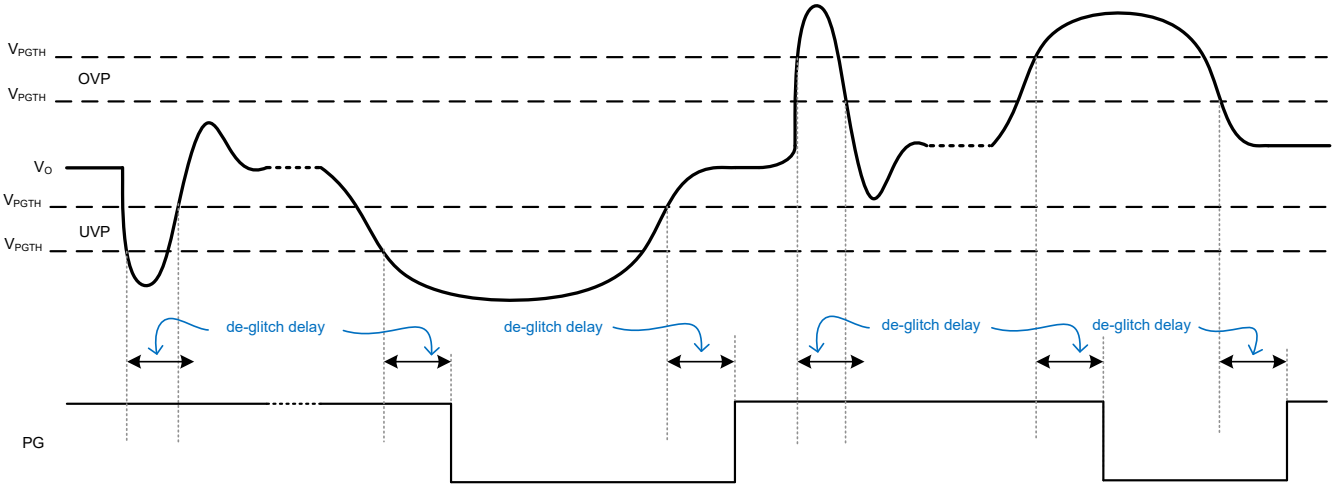


Figure 7-7. Power-Good Behavior

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

The TPSM82830x is a synchronous step-down converter power module, where the required power inductor is integrated inside the package. The inductance value is 470nH with a ±20% tolerance for the RDS package and 400nH with a ±20% tolerance for the VCB package. The family members within a package category are pin-to-pin and BOM-to-BOM compatible with each other.

8.2 Typical Application

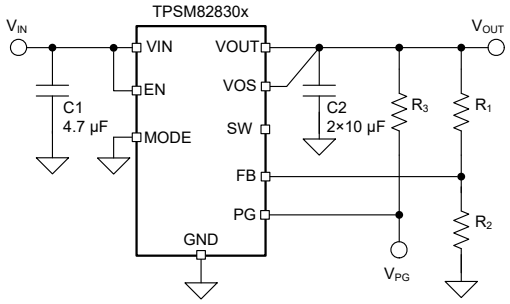


Figure 8-1. Typical Application of TPSM82830x

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.25V to 5.5V
Output voltage	1.8V
Output ripple voltage	< 15mV

Table 8-2 lists the components used for the example.

Table 8-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	4.7µF, Ceramic capacitor, 6.3V, X7R, size 0603, JMK107BB7475KA-T	Taiyo Yuden
C2	2 × 10µF, Ceramic capacitor, 10V, X7R, size 0603, GRM188Z71A106KA73D	Murata
R1	Depending on the output voltage, 523kΩ 1/16W, 1%, size 0402 for 1.8V	Std
R2	200kΩ, Chip resistor, 1/16W, 1%, size 0402	Std
R3	100kΩ, Chip resistor, 1/16W, 1%, size 0402	Std

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM82830x device with the WEBENCH® Power Designer.

1. In the part number field, start entering the part number if there is a preference and wait until a part list appears. If there is no preference, leave this field blank.
2. In the next section (auto-filled if you started with a part number) enter the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
3. In the "Design Considerations" section select your design priorities.
4. View your design proposal and compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools here: Design and simulation tools.

8.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to Equation 4:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.5V} - 1\right) \quad (4)$$

R2 can be any value between 200kΩ and 600kΩ to achieve high efficiency at light load while providing acceptable noise immunity.

8.2.2.3 Input Capacitor Selection

The input capacitor is the low-impedance energy source for the converter, which helps provide stable operation. Because the buck converter has a pulsating input current, a low ESR ceramic input capacitor is required for best input voltage filtering to minimize input voltage spikes. Place the capacitor between VIN and GND pins and as close as possible to those pins.

For most applications, a minimum effective input capacitance of 3µF is sufficient, though a larger value reduces input current ripple and is recommended. When operating from a high impedance source, TI recommends a larger input buffer capacitor ≥10µF to avoid voltage drops during start-up and load transients. Additionally, small de-coupling capacitors can also be used in case of noise at the input if the device. The input capacitor can be increased without any limit for better input voltage filtering.

Table 8-3 shows a list of recommended capacitors.

Table 8-3. List of Recommended Capacitors

NOMINAL CAPACITANCE [µF]	VOLTAGE RATING [V]	DIMENSIONS [mm]	MFR PART NUMBER(1)
4.7	6.3	1.6 × 0.8 × 0.8	MSASJ168BB7475MTNA01, Taiyo Yuden
4.7	10	2.0 × 1.25 × 1.25	C2012X7R1A475K125AC, TDK
10	10	1.6 × 0.8 × 0.8	GRM188Z71A106KA73#, MuRata

(1) See the *Third-party Products Disclaimer*

8.2.2.4 Output Capacitor Selection

The DCS-Control scheme of the TPSM82830x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. To keep low resistance

up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage ripple. Considering the DC-bias derating the capacitance, the recommended minimum effective output capacitance is 12µF. The recommended typical output capacitor value is 2 × 10µF or 1 × 22µF with an X5R or X7R dielectric. Table 8-4

Table 8-4. List of Recommended Capacitors

NOMINAL CAPACITANCE [µF]	VOLTAGE RATING [V]	DIMENSIONS [mm]	MFR PART NUMBER(1)
10	6.3	2.0 × 1.5 × 1.25	MSASJ21GAB7106MTNA01, Taiyo Yuden
10	10	2.0 × 1.25 × 1.25	C2012X7R1A106K125AC, TDK
10	10	1.6 × 0.8 × 0.8	GRM188Z71A106KA73#, MuRata
10	10	1.6 × 0.8 × 0.8	C1608X5R1A106K080AC, TDK
22	10	2.0 × 1.25 × 1.25	GRM21BZ71A226ME15#, MuRata
22	10	1.6 × 0.8 × 0.8	C1608X5R1A226M080AC, TDK

8.2.3 Application Curves

T_A = 25°C, V_{IN} = 5 V, V_{OUT} = 1.8 V, BOM = Table 8-2 unless otherwise noted.

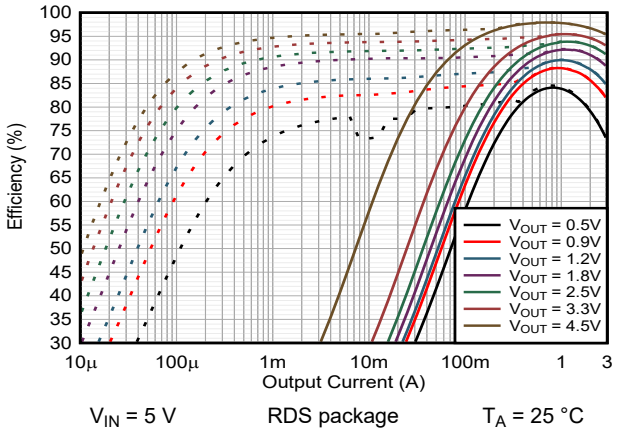


Figure 8-2. Efficiency versus Output Current

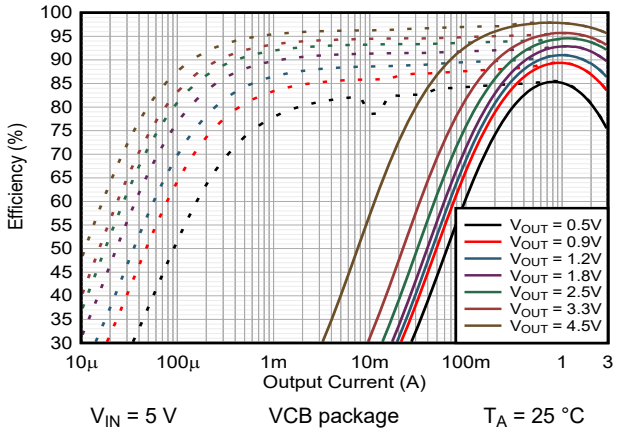


Figure 8-3. Efficiency versus Output Current

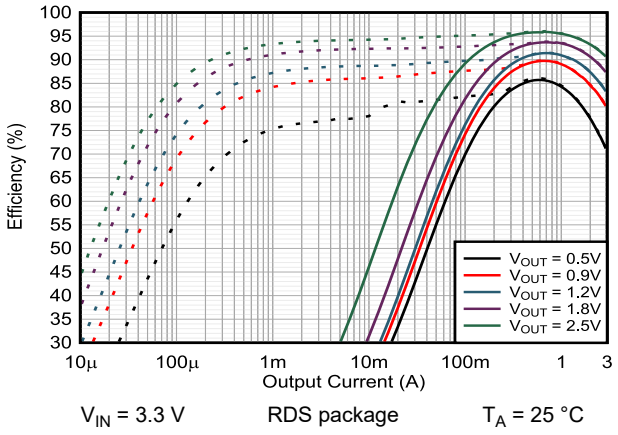


Figure 8-4. Efficiency versus Output Current

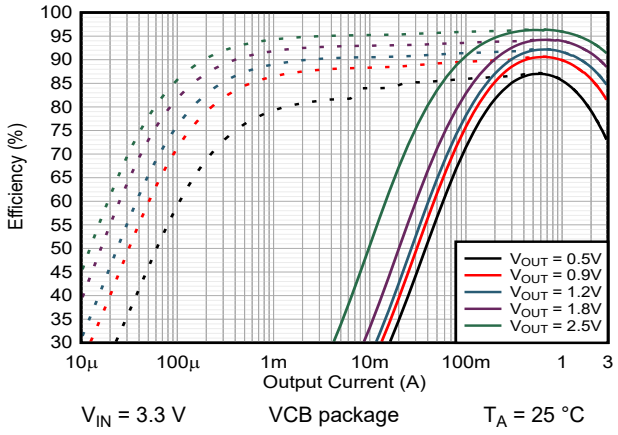


Figure 8-5. Efficiency versus Output Current

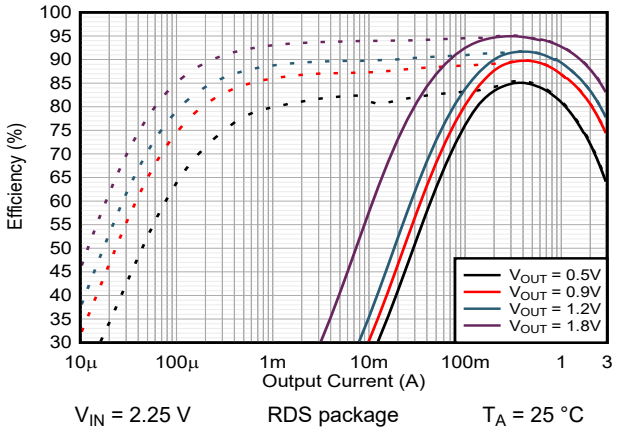


Figure 8-6. Efficiency versus Output Current

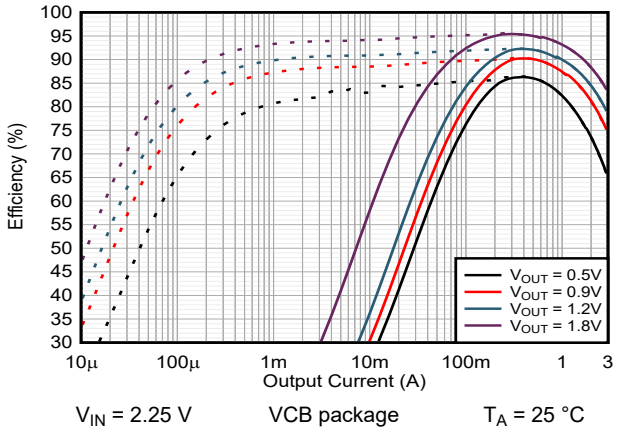


Figure 8-7. Efficiency versus Output Current

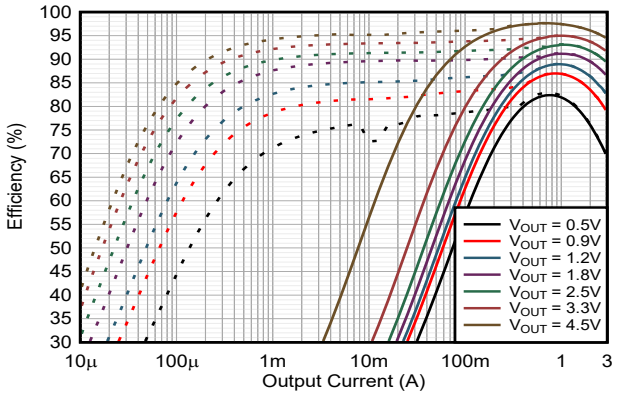


Figure 8-8. Efficiency versus Output Current

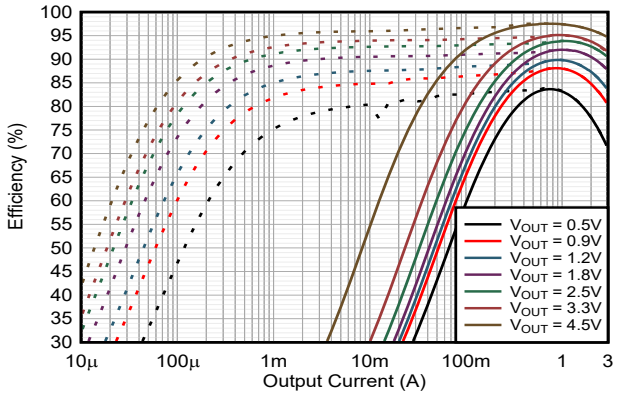


Figure 8-9. Efficiency versus Output Current

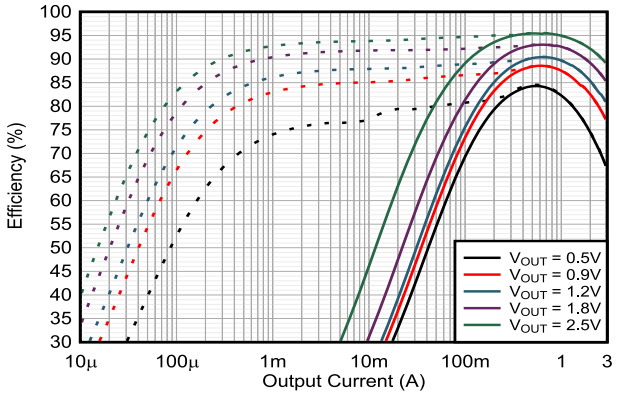


Figure 8-10. Efficiency versus Output Current

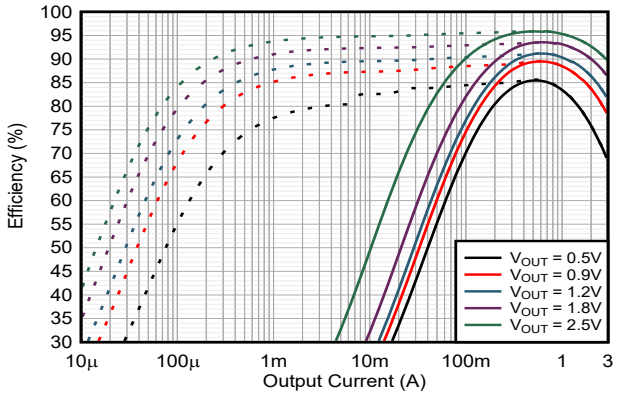


Figure 8-11. Efficiency versus Output Current

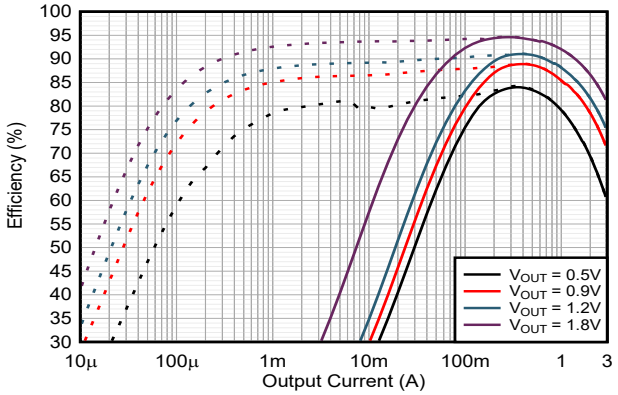


Figure 8-12. Efficiency versus Output Current

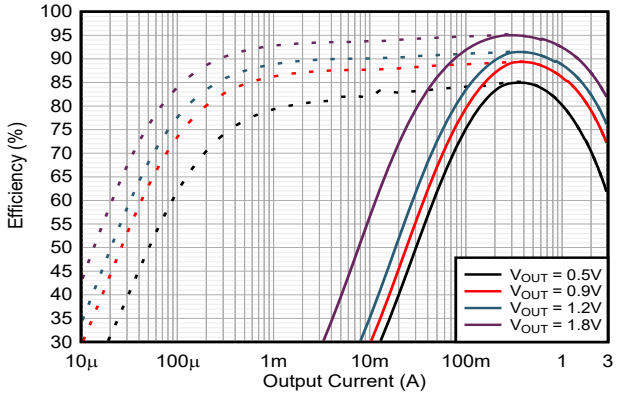
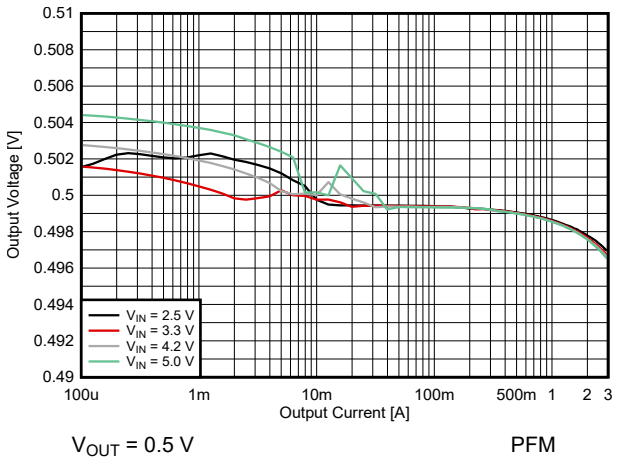
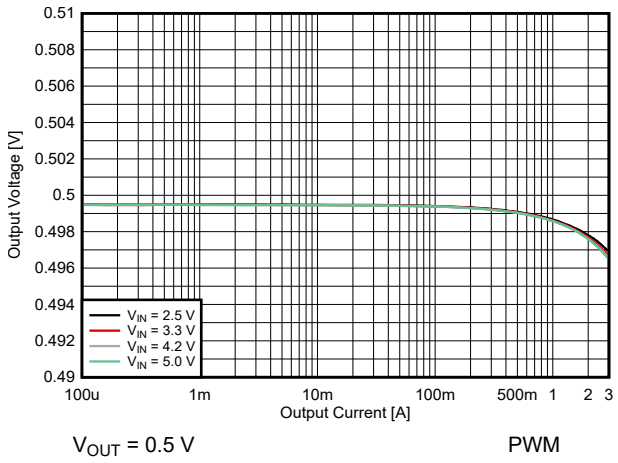


Figure 8-13. Efficiency versus Output Current



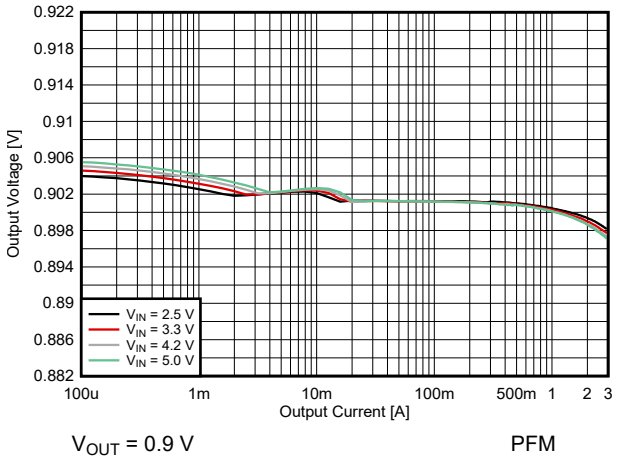
V_{OUT} = 0.5 V PFM

Figure 8-14. Output Voltage versus Output Current



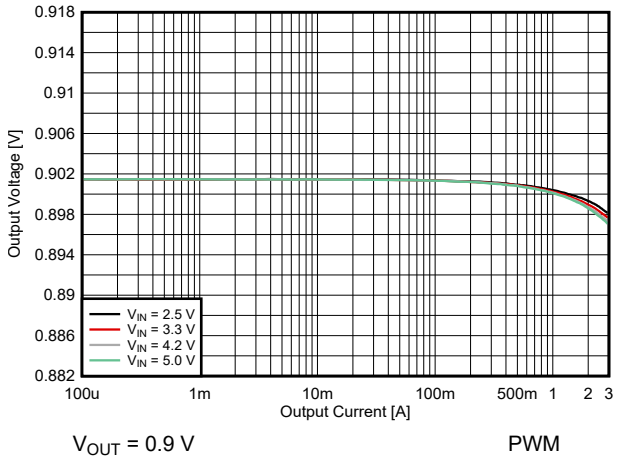
V_{OUT} = 0.5 V PWM

Figure 8-15. Output Voltage versus Output Current



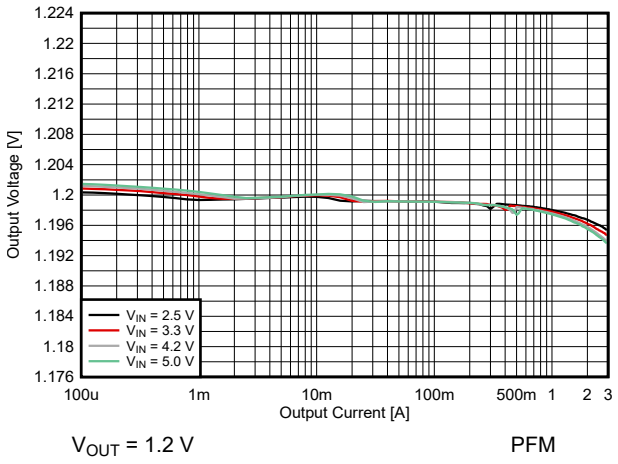
V_{OUT} = 0.9 V PFM

Figure 8-16. Output Voltage versus Output Current



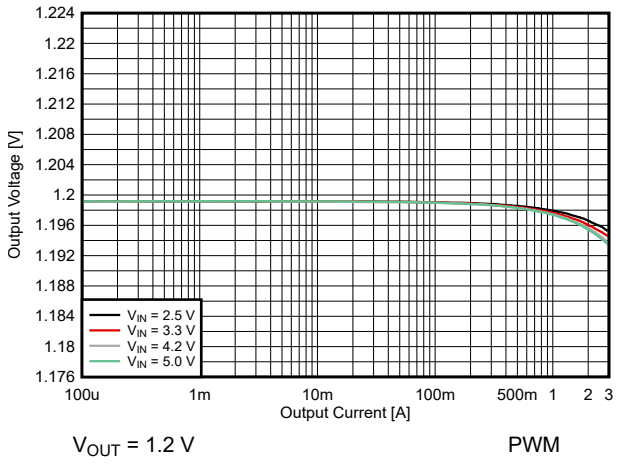
V_{OUT} = 0.9 V PWM

Figure 8-17. Output Voltage versus Output Current



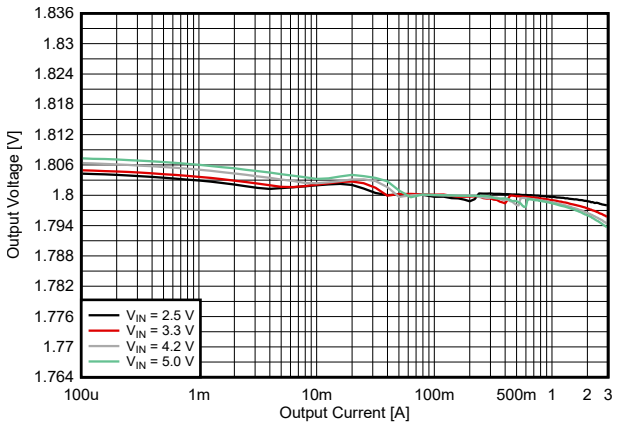
V_{OUT} = 1.2 V PFM

Figure 8-18. Output Voltage versus Output Current



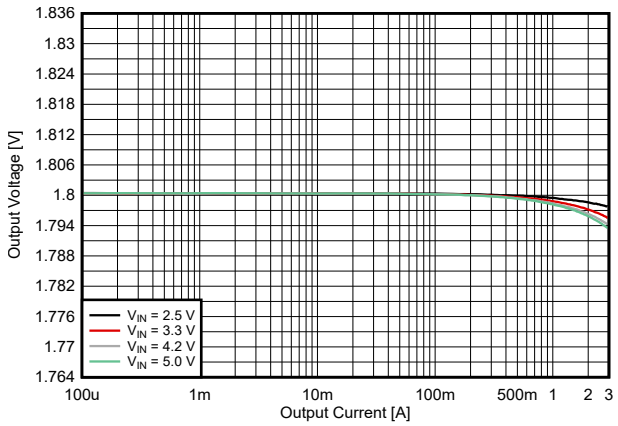
V_{OUT} = 1.2 V PWM

Figure 8-19. Output Voltage versus Output Current



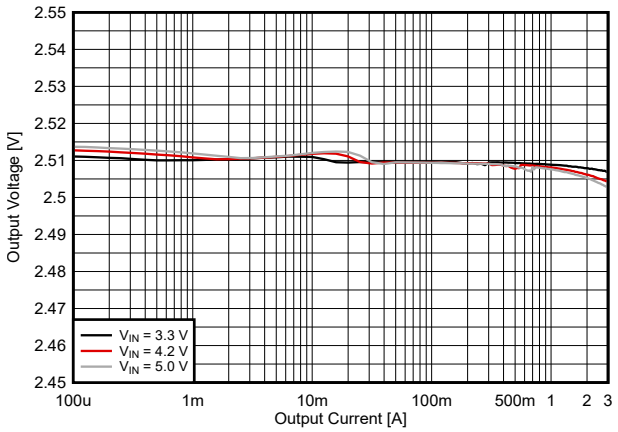
V_{OUT} = 1.8 V PFM

Figure 8-20. Output Voltage versus Output Current



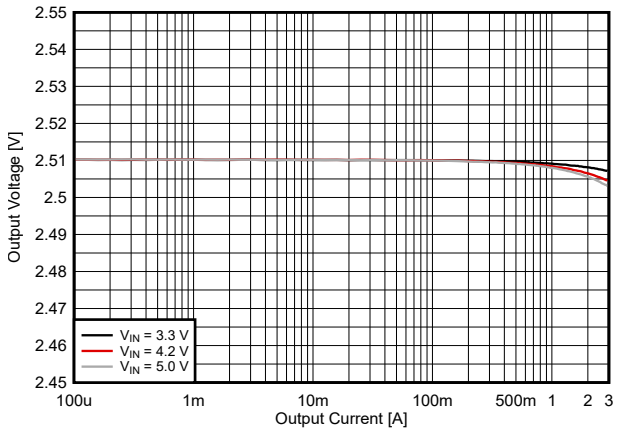
V_{OUT} = 1.8 V PWM

Figure 8-21. Output Voltage versus Output Current



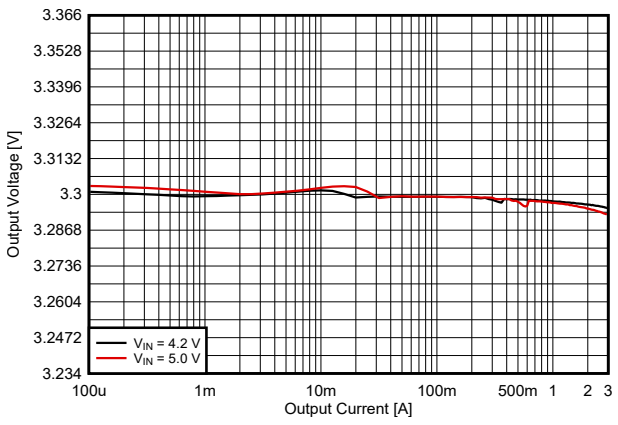
V_{OUT} = 2.5 V PFM

Figure 8-22. Output Voltage versus Output Current



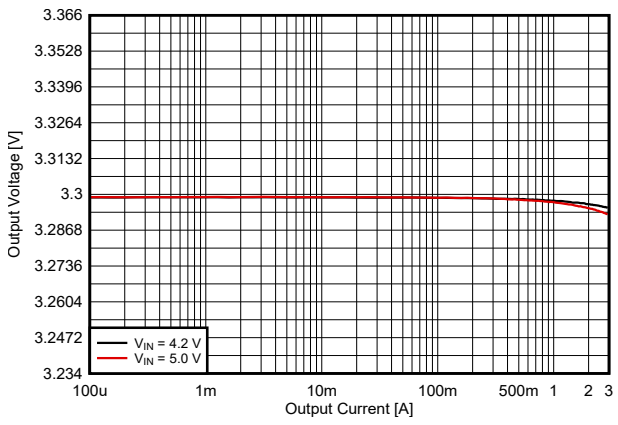
V_{OUT} = 2.5 V PWM

Figure 8-23. Output Voltage versus Output Current



V_{OUT} = 3.3 V PFM

Figure 8-24. Output Voltage versus Output Current



V_{OUT} = 3.3 V PWM

Figure 8-25. Output Voltage versus Output Current

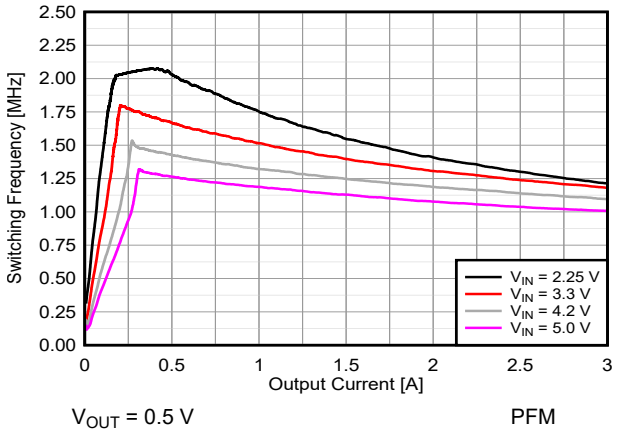


Figure 8-26. Switching Frequency versus Output Current

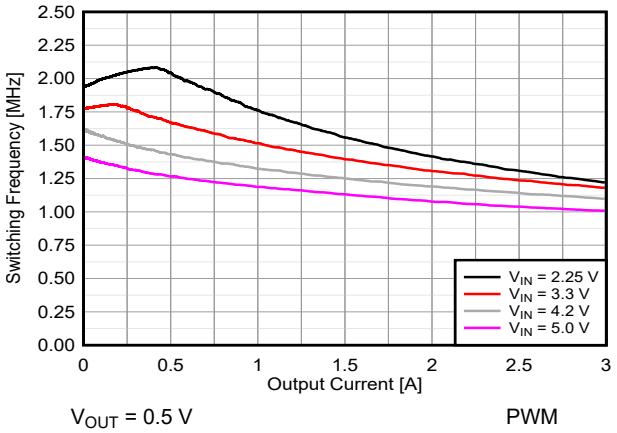


Figure 8-27. Switching Frequency versus Output Current

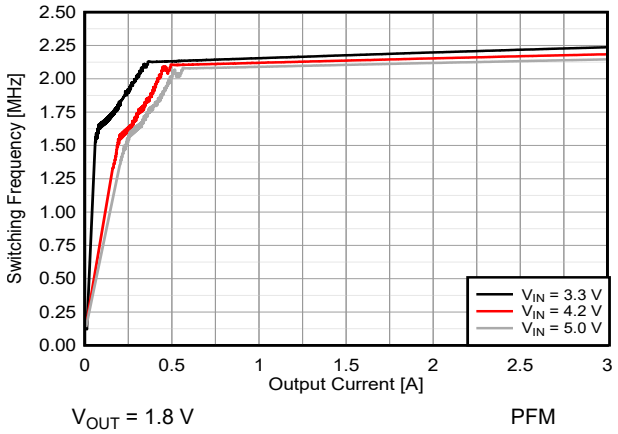


Figure 8-28. Switching Frequency versus Output Current

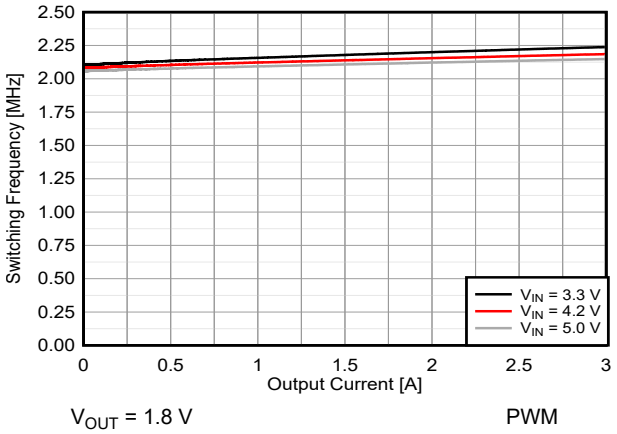


Figure 8-29. Switching Frequency versus Output Current

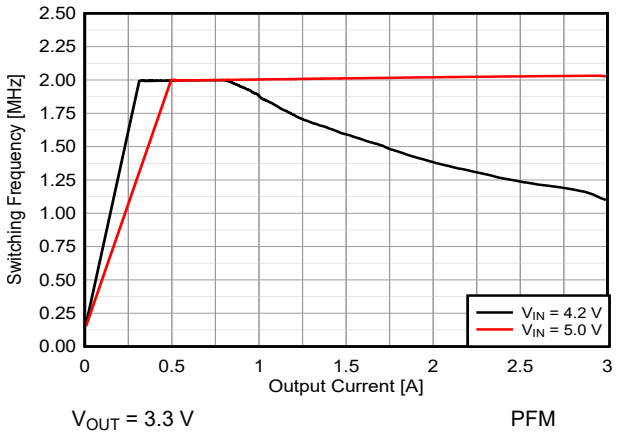


Figure 8-30. Switching Frequency versus Output Current

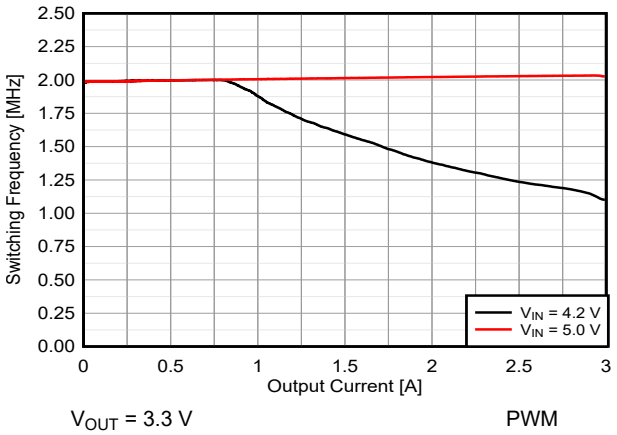
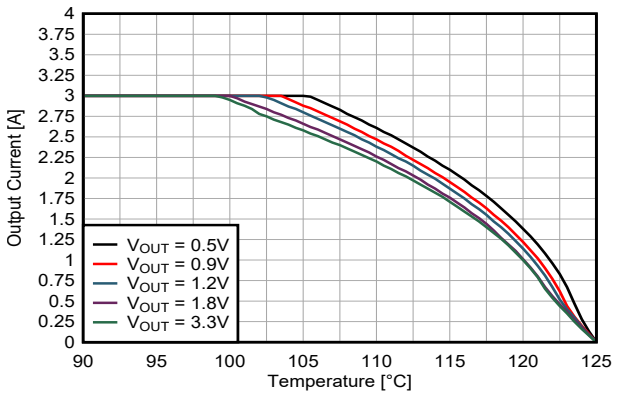
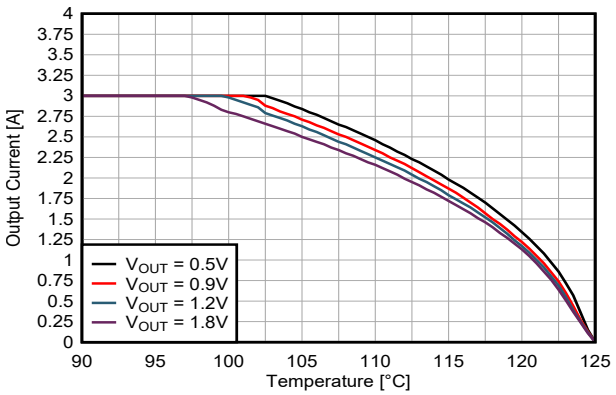


Figure 8-31. Switching Frequency versus Output Current



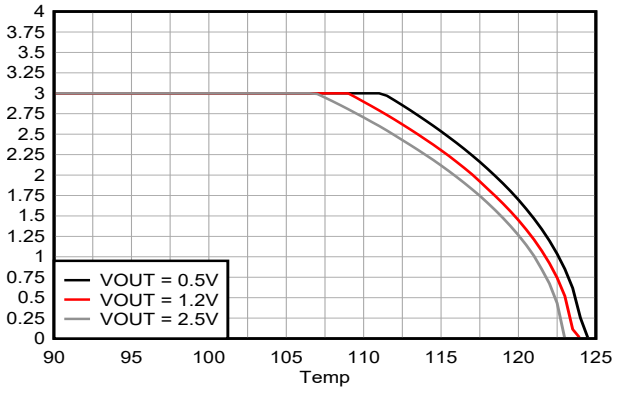
V_{IN} = 5.0 V T_{Jmax} = 125°C θ_{JA}= 49.8°C/W

Figure 8-32. Thermal Derating (Safe Operating Area) RDS Package



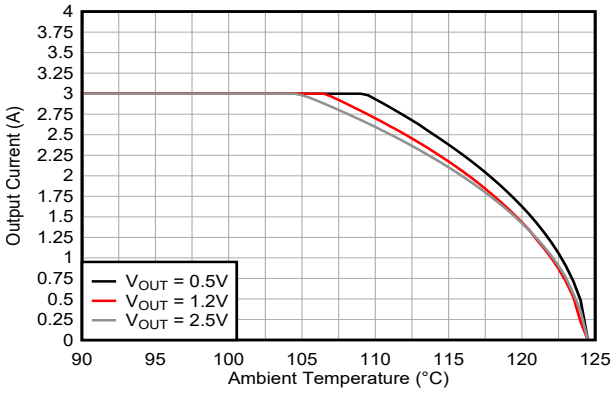
V_{IN} = 3.3 V T_{Jmax} = 125°C θ_{JA} = 49.8°C/W

Figure 8-33. Thermal Derating (Safe Operating Area) RDS Package



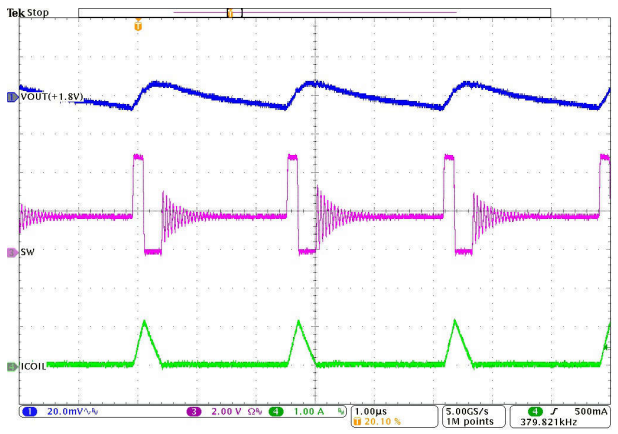
V_{IN} = 5.0 V T_{Jmax} = 125°C θ_{JA}= 66.5°C/W

Figure 8-34. Thermal Derating (Safe Operating Area) VCB Package



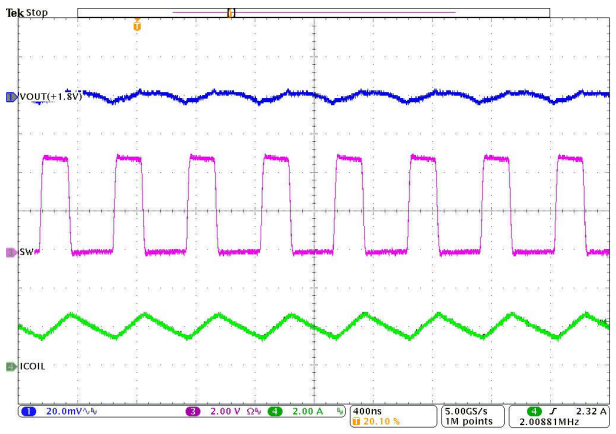
V_{IN} = 3.3 V T_{Jmax} = 125°C θ_{JA} = 66.5°C/W

Figure 8-35. Thermal Derating (Safe Operating Area) VCB Package



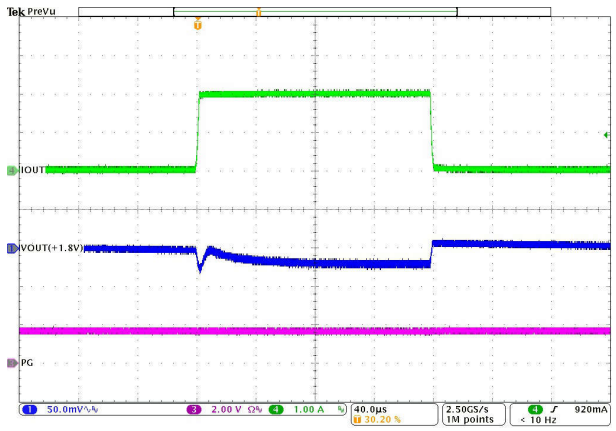
I_{OUT} = 100 mA PFM

Figure 8-36. Output Voltage Ripple



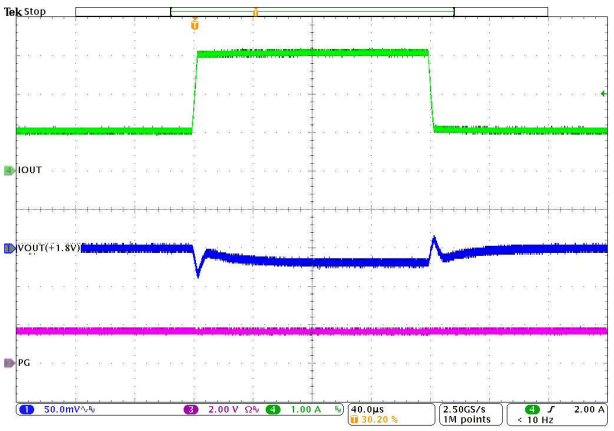
I_{OUT} = 2 A PWM

Figure 8-37. Output Voltage Ripple



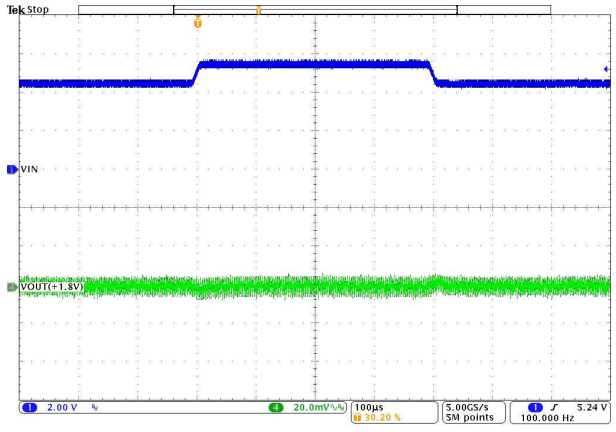
I_{OUT} = 1 mA to 2 A PFM Slew rate = 1 A/µs

Figure 8-38. Load Transient



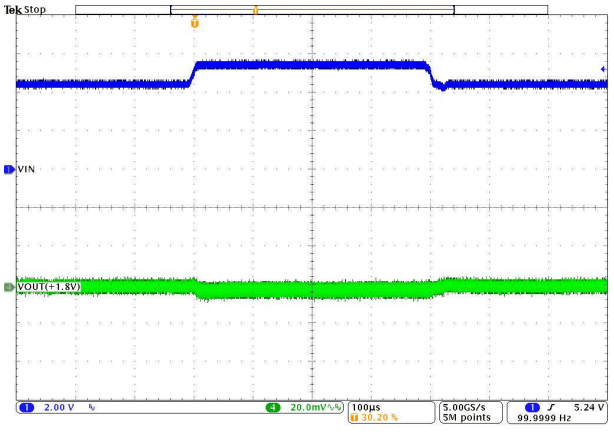
I_{OUT} = 0 mA to 1 A PWM Slew rate = 1 A/µs

Figure 8-39. Load Transient



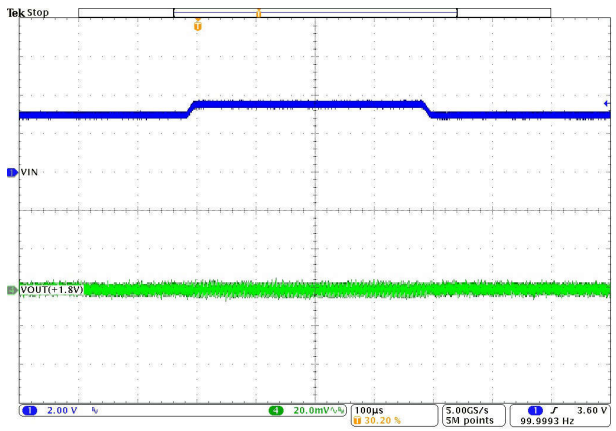
V_{IN} = 4.5 V to 5.5 V PFM I_{OUT} = 100 mA

Figure 8-40. Line Transient



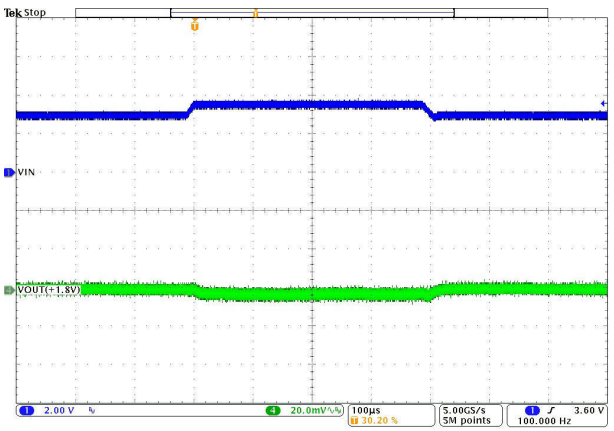
V_{IN} = 4.5 V to 5.5 V PFM or PWM I_{OUT} = 2 A

Figure 8-41. Line Transient



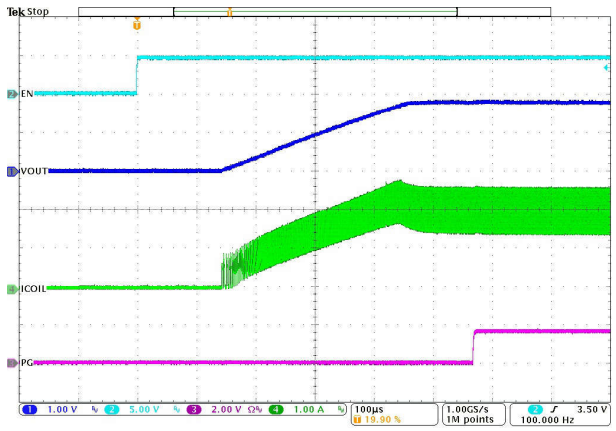
V_{IN} = 3.0 V to 3.6 V PFM I_{OUT} = 100 mA
V_{OUT} = 1.8 V

Figure 8-42. Line Transient



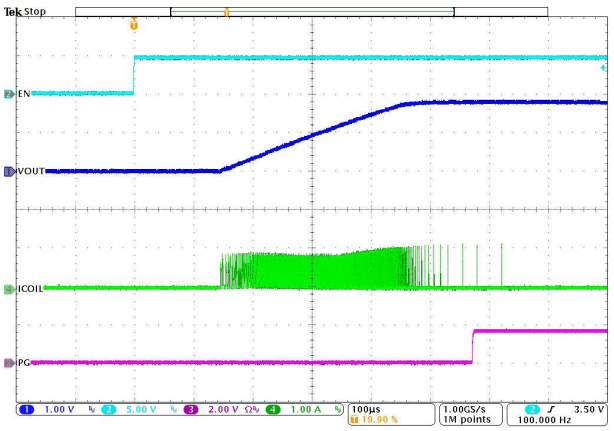
V_{IN} = 3.0 V to 3.6 V PFM or PWM I_{OUT} = 2 A
V_{OUT} = 1.8 V

Figure 8-43. Line Transient



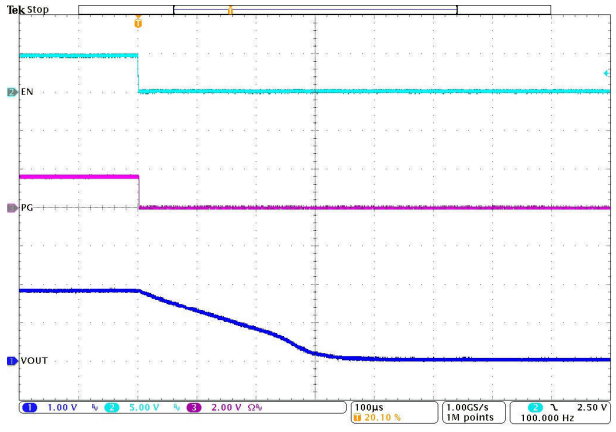
I_{OUT} = 2 A PFM or PWM

Figure 8-44. Start-Up With Load



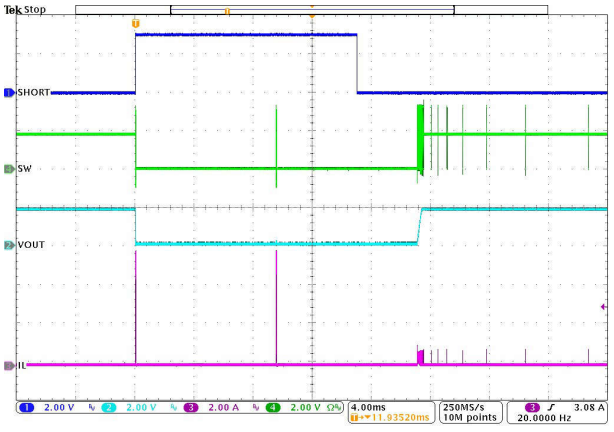
I_{OUT} = 0 mA PFM

Figure 8-45. Start-Up With No Load



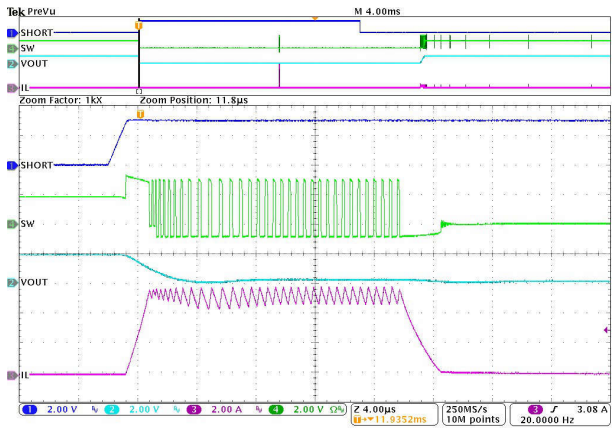
I_{OUT} = 0 mA PFM

Figure 8-46. Disable, Active Output Discharge at No Load



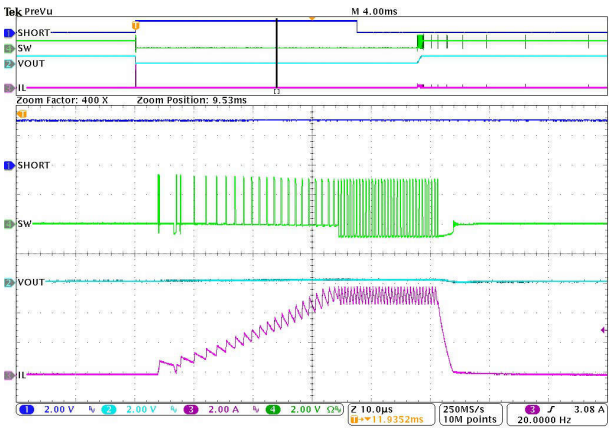
I_{OUT} = 1 A PFM or PWM

Figure 8-47. HICCUP Short-Circuit Protection



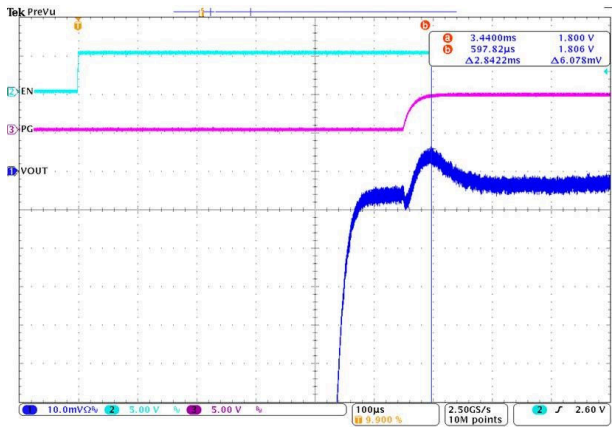
I_{OUT} = 1.0 A PFM or PWM

Figure 8-48. HICCUP Short-Circuit Protection (Zoom In)



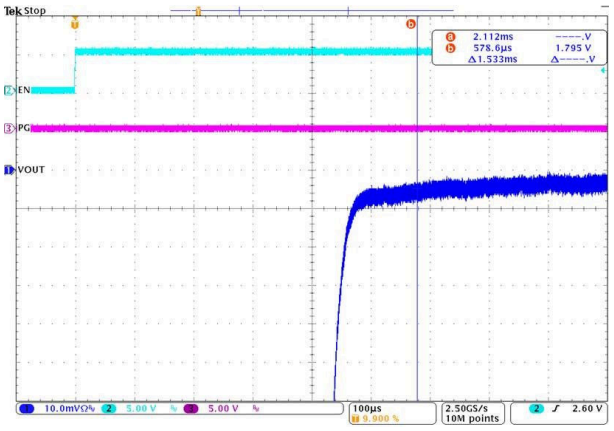
I_{OUT} = 1.0 A PFM or PWM

Figure 8-49. HICCUP Short-Circuit Protection (Zoom In - Second Hiccup)



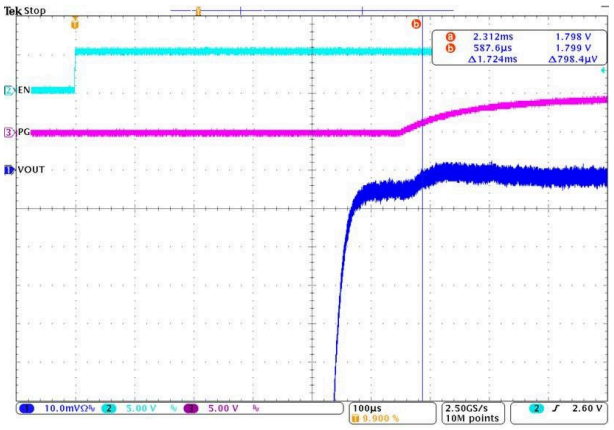
I_{OUT} = 0 A PG pin no capacitor PFM or PWM

Figure 8-50. PG to VOUT Influence



I_{OUT} = 0 A PG pin connected to GND PFM or PWM

Figure 8-51. PG to VOUT Influence



I_{OUT} = 0 A PG pin 1nF, pull-up 100kΩ PFM or PWM

Figure 8-52. PG to VOUT Influence

8.3 Power Supply Recommendations

The TPSM82830x family does not have special requirements for the input power supply and is designed to operate from an input voltage supply range from 2.25 V to 5.5 V. The output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the device.

8.4 Layout

8.4.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the device. See *Layout Example* for the recommended low EMI PCB layout.

- Place the input and output capacitors as close as possible to the IC. This action keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- Connect the low side of the input and output capacitors properly to the GND pin to avoid a ground potential shift.
- Take special care to avoid noise being induced. The sense traces connected to FB is a signal trace. Keep these traces away from SW nodes. The connection of the output voltage trace for the FB resistors must be made at the output capacitor.
- Refer to *Layout Example* for an example of component placement, routing, and thermal design with good EMI performance.

8.4.2 Layout Example

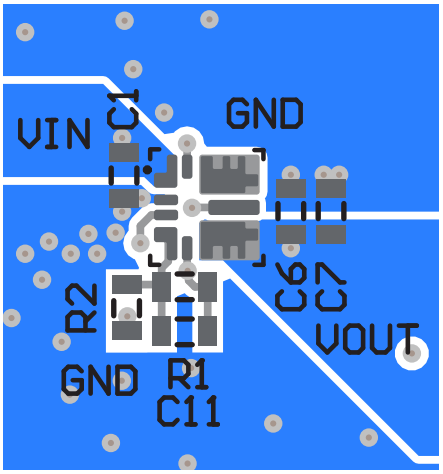


Figure 8-53. PCB Layout Recommendation (RDS Package)

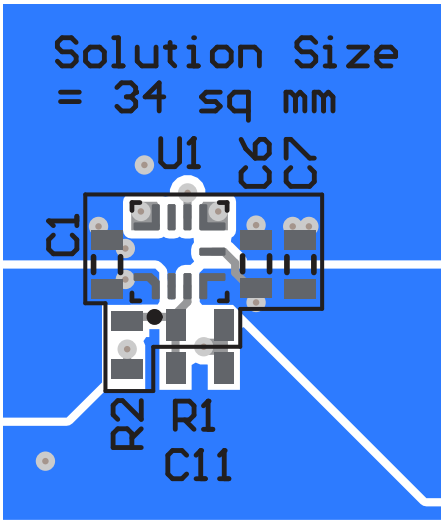


Figure 8-54. PCB Layout Recommendation (VCB Package)

8.4.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

The Thermal Data section in *Thermal Information Module* provides the thermal metric of the device on the EVM after considering the PCB design of real applications. The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see the Thermal Characteristics application notes, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics*.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM82830x device with the WEBENCH® Power Designer.

1. In the part number field, start entering the part number if there is a preference and wait until a part list appears. If there is no preference, leave this field blank.
2. In the next section (auto-filled if you started with a part number) enter the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
3. In the "Design Considerations" section select your design priorities.
4. View your design proposal and compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools here: Design and simulation tools.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

MagPack™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2024) to Revision C (April 2025) **Page**

- Added bullet "MagPack technology shields inductor and IC" 1
- Deleted bullet "Measurements according to CISPR available" 1
- Deleted "PSpice and SIMPLIS models available" bullet 1
- Updated bullet with package options to include package height and "with no bondwires" 1
- Deleted TPSM828303PVCBR (Advance information) from the *Device Information* table. 1
- Deleted package height from the *Device Information* table 1
- Added TPSM828301 (VCB) and TPSM828302 (VCB) (Preview information) to *Device Information* table 1
- Added "a family of 1A, 2A, and 3A, pin-to-pin compatible" in the *Description* 1
- Changed from "Based on the DCS-Control topology, the devices have a fast transient response yet with small output capacitance" to "The devices use DCS-Control topology for fast transient response with small output capacitance" in the *Description* 1
- Changed from "The power save mode prolongs battery life at low output currents and the forced PWM mode maintains continuous conduction in the inductor to reduce ripple at constant switching frequency" to "The power save mode is for longer battery life and the forced PWM mode reduces ripple with continuous conduction in the inductor at a quasi fixed switching frequency" in the *Description* 1
- Changed from "An internal soft-start circuit ramps the voltage up tightly controlled and a power-good signal indicates correct output voltage" to "An internal soft-start circuit reduces inrush current and a power-good signal indicates correct output voltage" in the *Description* 1
- Deleted "The devices support 100% mode" from the *Description* 1
- Changed from "3.0mm × 3.0mm × 1.95mm QFN package and 2.5mm × 2.6mm × 1.95mm" to "3.0mm × 3.0mm QFN package and in the 2.5mm × 2.6mm" in the *Description* 1
- Deleted "Advance information (not Production Data)" table note from TPSM828303PVCBR in the *Device Options* table 3
- Added TPSM828303KPVCBR, TPSM828301APVCBR, and TPSM828302APVCBR with "Preview information (not Production Data)" table note in the *Device Options* table. 3
- Changed TPSM828303PVCBR advance information to TPSM828303APVCBR for release to production in the *Device Options* table 3
- Added column with soft-start time information in the *Device Options* table 3
- Change the description of pin 8 in both *Pin Functions* tables from "which is connected to the internal power MOSFET and the inductor. Avoid connecting this pin to larger traces as this can increase EMI. this pin can stay unconnected or be soldered " to "internally connected the inductor. For lowest EMI, leave this pin unconnected or solder this pin " 3
- Deleted VOUT from line 1 in *Absolute Maximum Ratings* 5
- Added two additional lines for voltage in *Absolute Maximum Ratings*, one for pins SW (DC), VOS, and VOUT and one for SW (AC, < 10ns) with table note "While switching" 5
- Added parameter tSS in *Electrical Characteristics* table in section STARTUP for device version TPSM828303xK 5
- Changed parameter name td(PG) to td(PGO) in section POWER GOOD for deglitch delay during operation 5
- Added table note to parameter VFB in section REFERENCE VOLTAGE indicating the parameter is a DC parameter 5
- Changed paragraph "The VCB package version uses MagPack technology for even further EMI reduction. MagPack, a Texas Instruments proprietary integrated-magnetics packaging technology, delivers the highest-performance power module design. Besides EMI reduction, MagPack enhances efficiency and thermal properties of power modules. This feature enables an industry-leading power density" to "The VCB package version uses MagPack technology to deliver the highest-performance power module design. Leveraging the

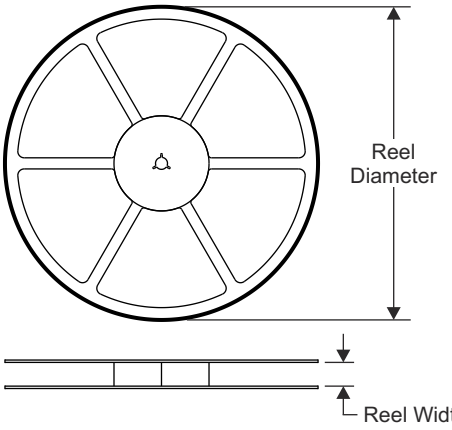
Changes from Revision A (December 2023) to Revision B (June 2024)	Page
• Added TPSM828303PVCBR (Advance Information)	1

11 Mechanical, Packaging, and Orderable Information

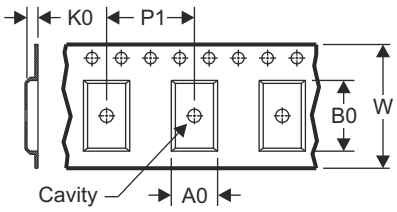
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

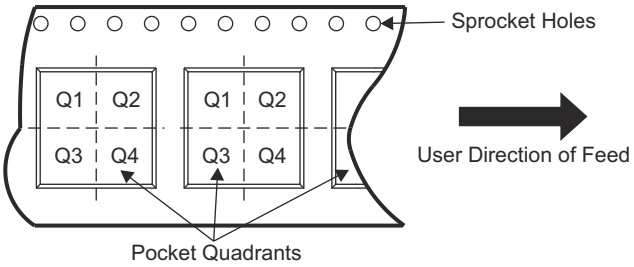


TAPE DIMENSIONS



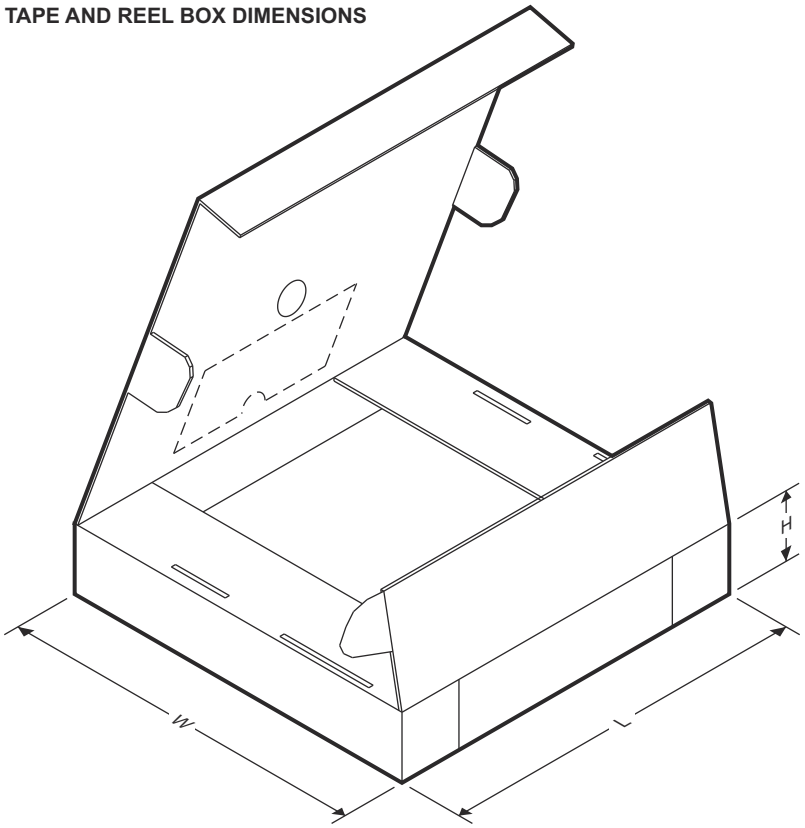
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM828303PVCBR	QFN-FCMOD	RDS	9	3000	180	8.4	0.77	1.65	0.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



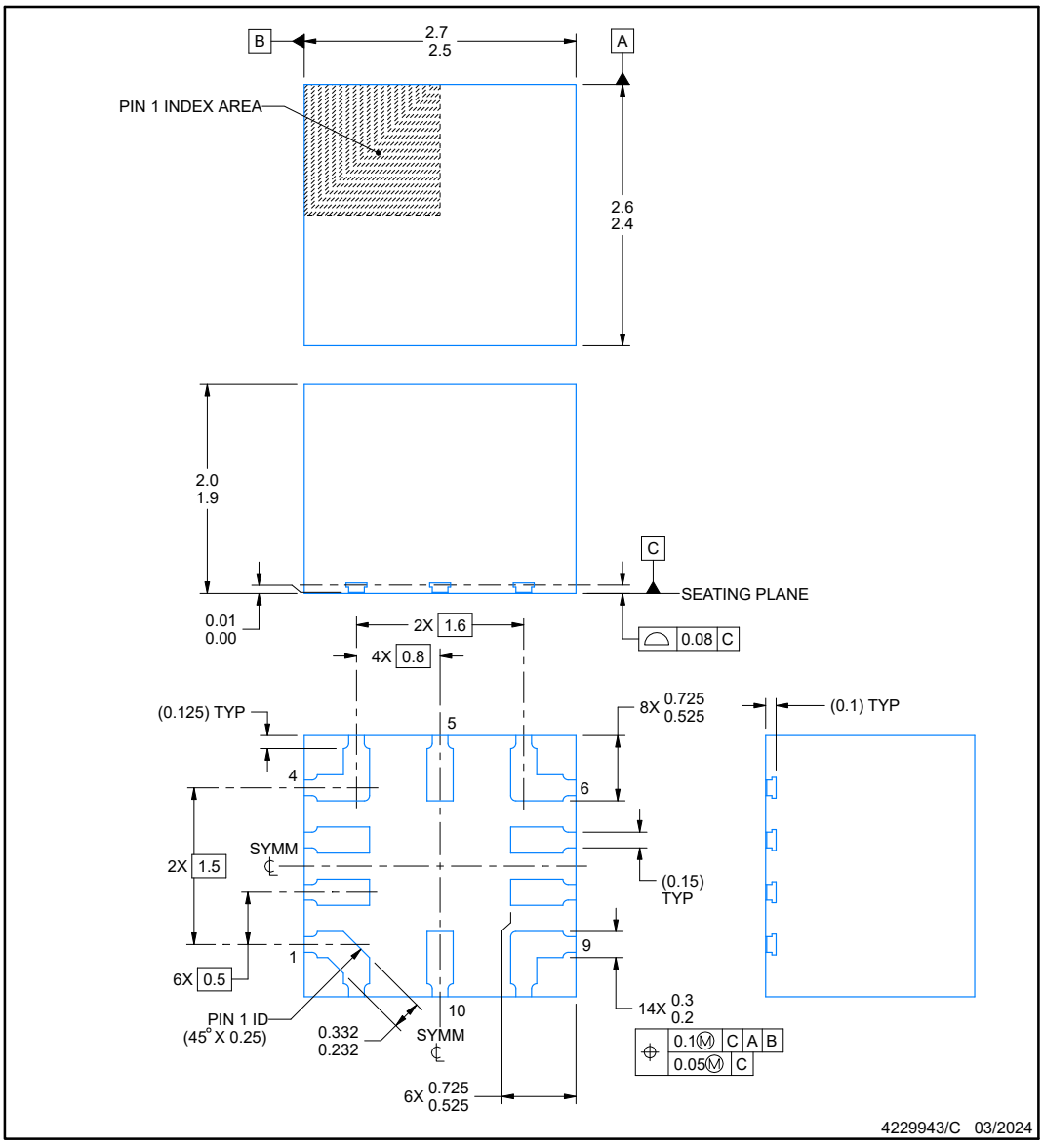
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM828303PVCBR	QFN-FCMOD	RDS	9	3000	182	182	20

PACKAGE OUTLINE

VCB0010A

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

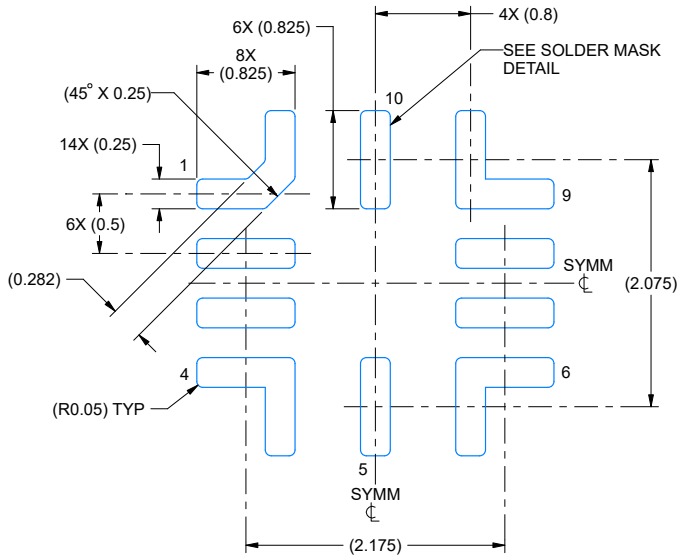
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

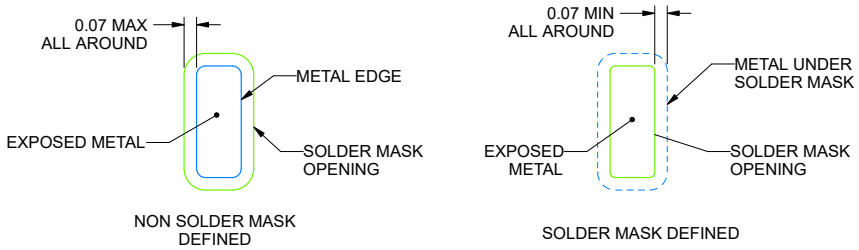
VCB0010A

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4229943/C 03/2024

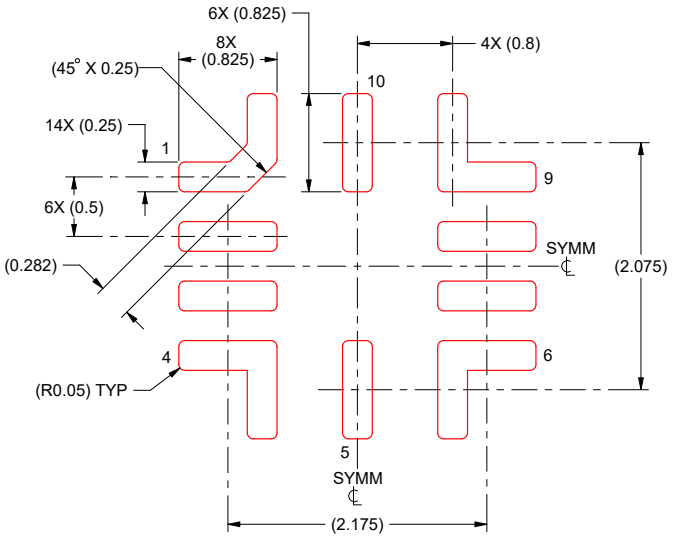
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VCB0010A — **QFN-FCMOD - 2 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4229943/C 03/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM828301ARDSR	Active	Production	QFN-FCMOD (RDS) | 9	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TM8301
TPSM828301ARDSR.A	Active	Production	QFN-FCMOD (RDS) | 9	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TM8301
TPSM828302ARDSR	Active	Production	QFN-FCMOD (RDS) | 9	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TM8302
TPSM828302ARDSR.A	Active	Production	QFN-FCMOD (RDS) | 9	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TM8302
TPSM828302ARDSR.B	Active	Production	QFN-FCMOD (RDS) | 9	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPSM828303APVCBR	Active	Production	QFN-FCMOD (VCB) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	3QPI
TPSM828303APVCBR.A	Active	Production	QFN-FCMOD (VCB) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	3QPI
TPSM828303ARDSR	Active	Production	QFN-FCMOD (RDS) | 9	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TM8303
TPSM828303ARDSR.A	Active	Production	QFN-FCMOD (RDS) | 9	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TM8303
TPSM828303ARDSR.B	Active	Production	QFN-FCMOD (RDS) | 9	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

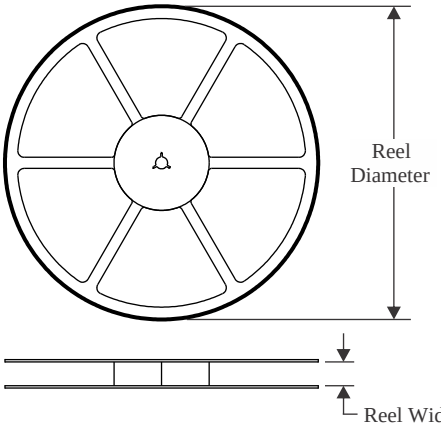
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

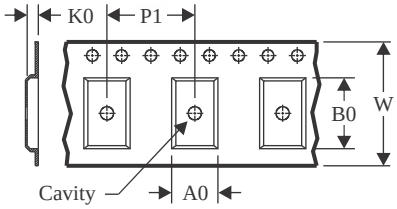
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

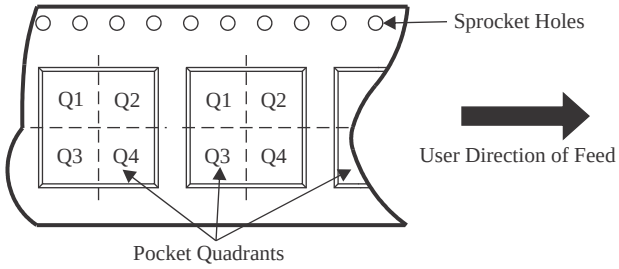


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

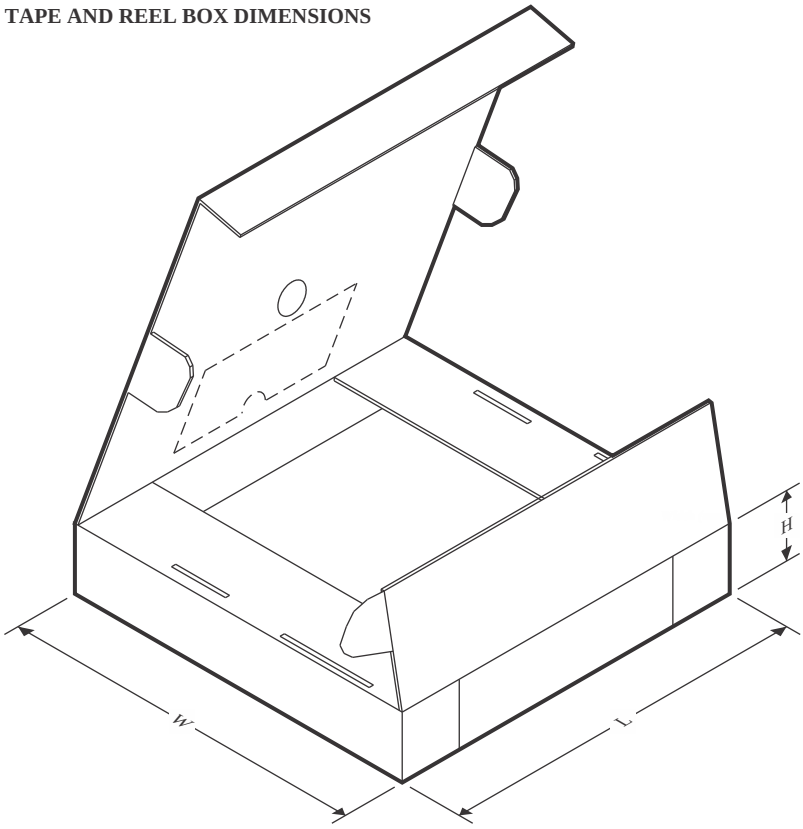
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM828301ARDSR	QFN-FCMOD	RDS	9	3000	330.0	17.6	3.3	3.3	2.25	8.0	12.0	Q2
TPSM828302ARDSR	QFN-FCMOD	RDS	9	3000	330.0	17.6	3.3	3.3	2.25	8.0	12.0	Q2
TPSM828303APVCBR	QFN-FCMOD	VCB	10	2500	330.0	12.4	2.9	2.8	2.2	8.0	12.0	Q2
TPSM828303ARDSR	QFN-FCMOD	RDS	9	3000	330.0	17.6	3.3	3.3	2.25	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

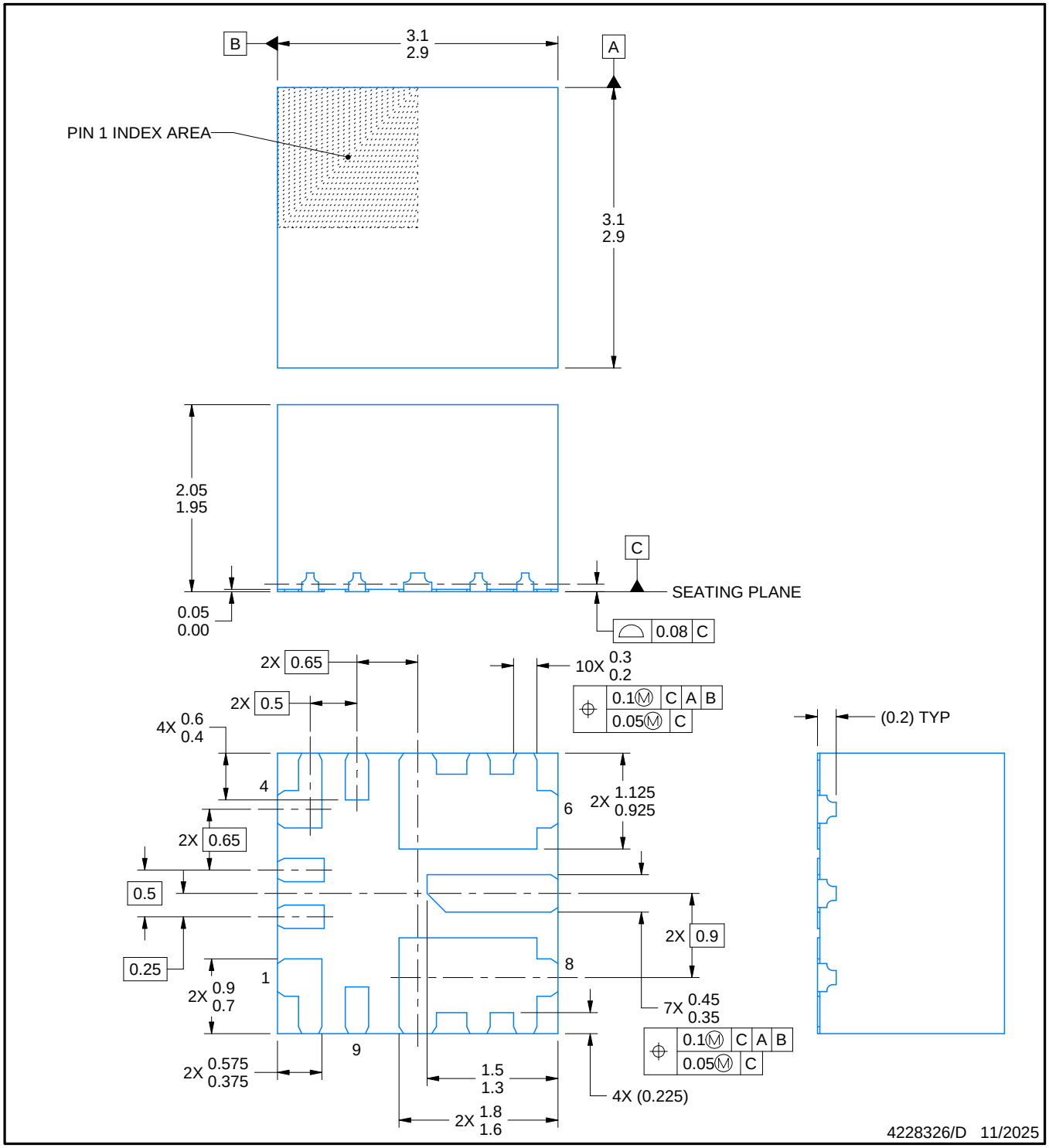
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM828301ARDSR	QFN-FCMOD	RDS	9	3000	336.0	336.0	48.0
TPSM828302ARDSR	QFN-FCMOD	RDS	9	3000	336.0	336.0	48.0
TPSM828303APVCBR	QFN-FCMOD	VCB	10	2500	367.0	367.0	35.0
TPSM828303ARDSR	QFN-FCMOD	RDS	9	3000	336.0	336.0	48.0

PACKAGE OUTLINE

RDS0009A

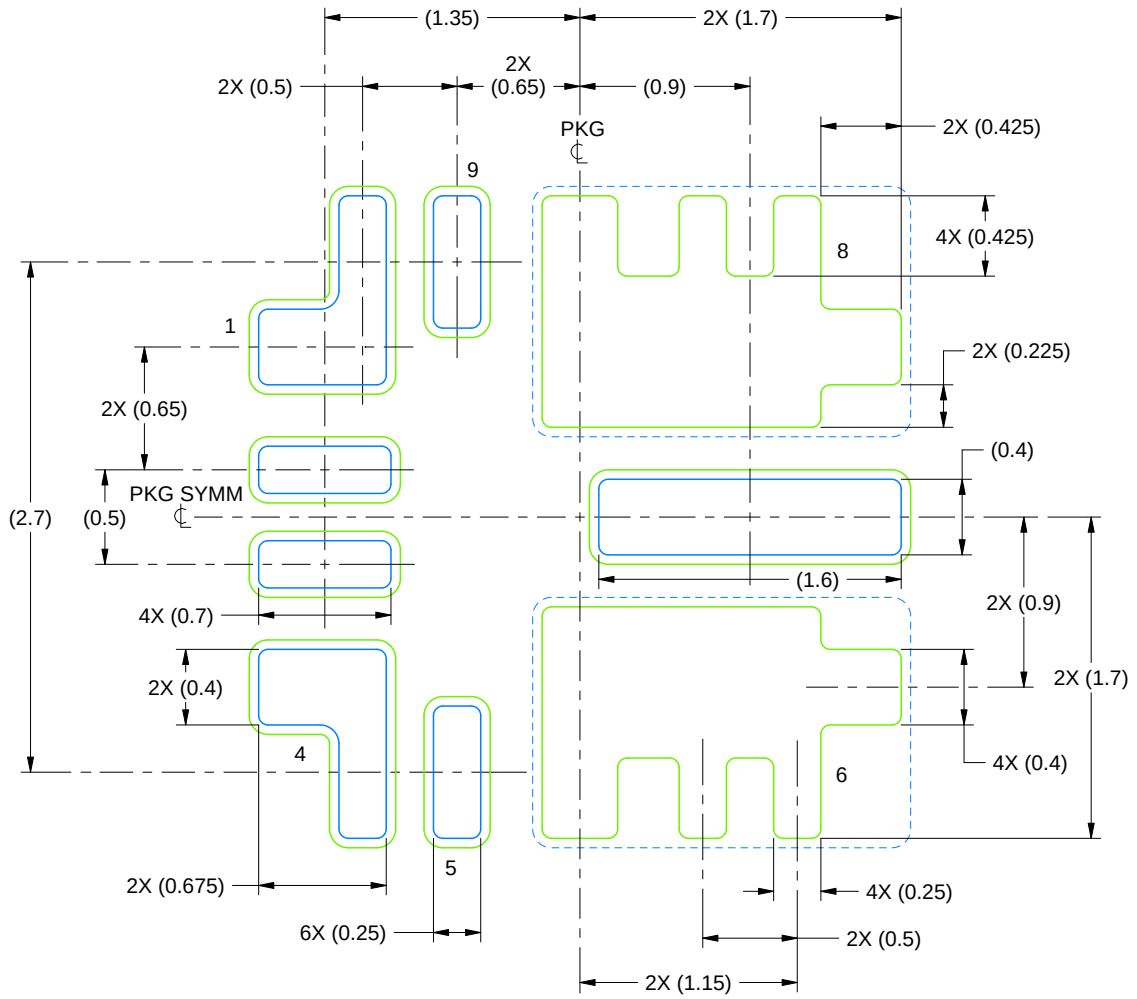
QFN-FCMOD - 2.05 mm max height

QUAD FLATPACK - NO LEAD

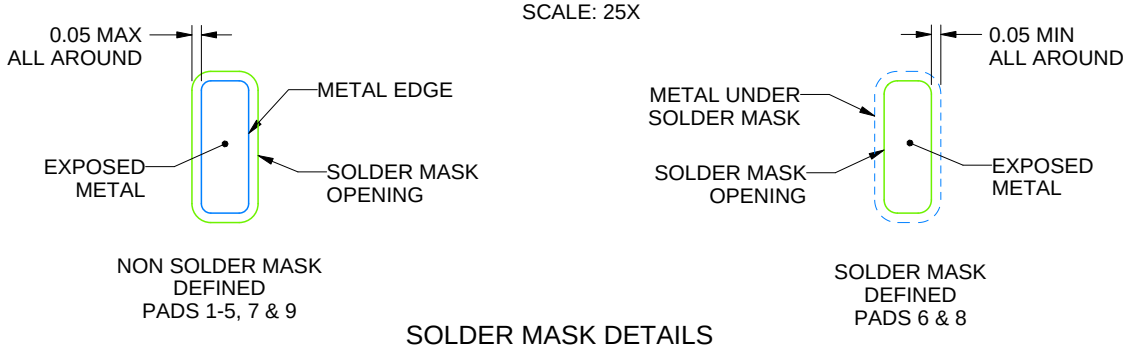


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 25X

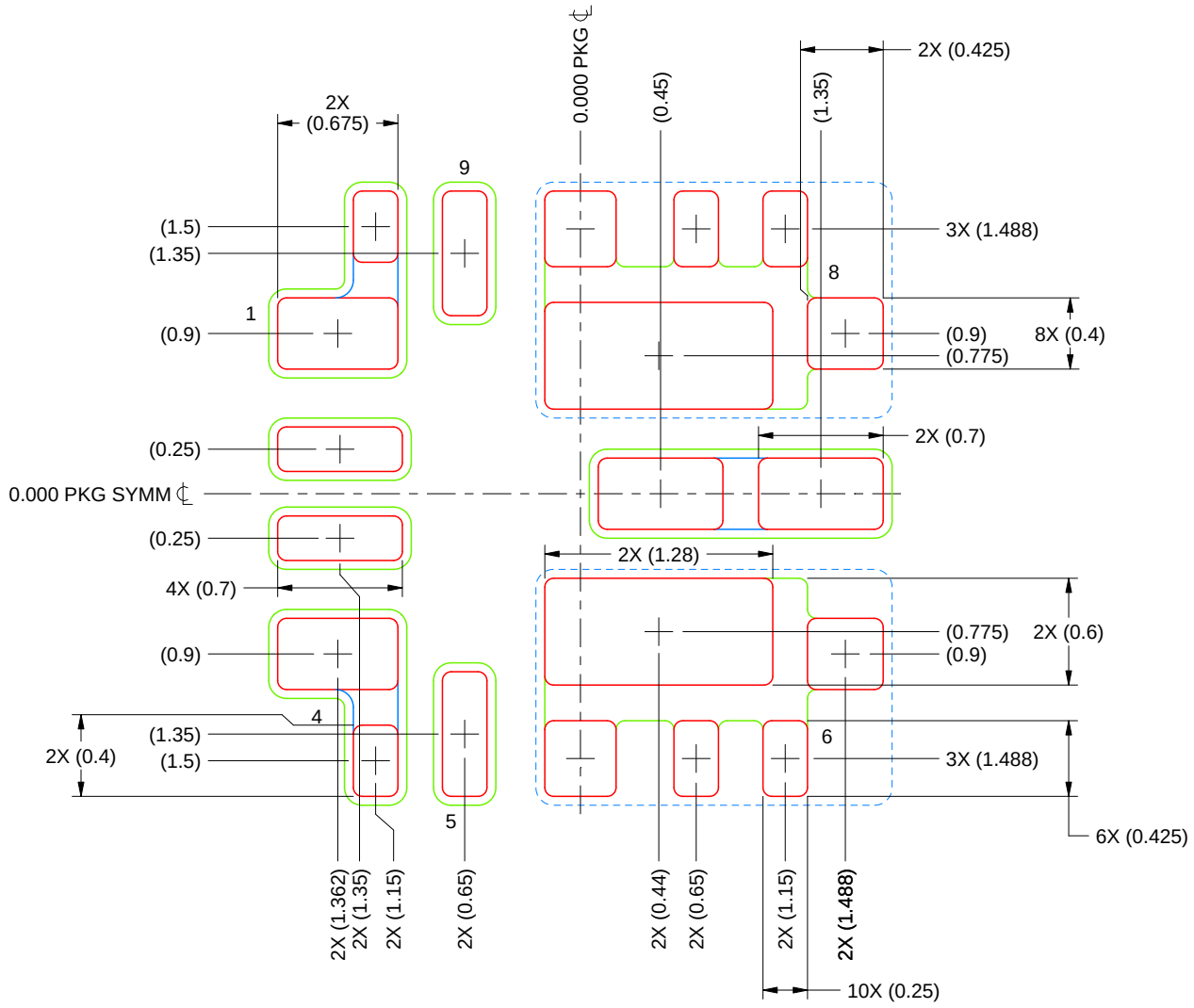


SOLDER MASK DETAILS

4228326/D 11/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 4 & 7: 88%
PADS 6 & 8: 76%

4228326/D 11/2025

NOTES: (continued)

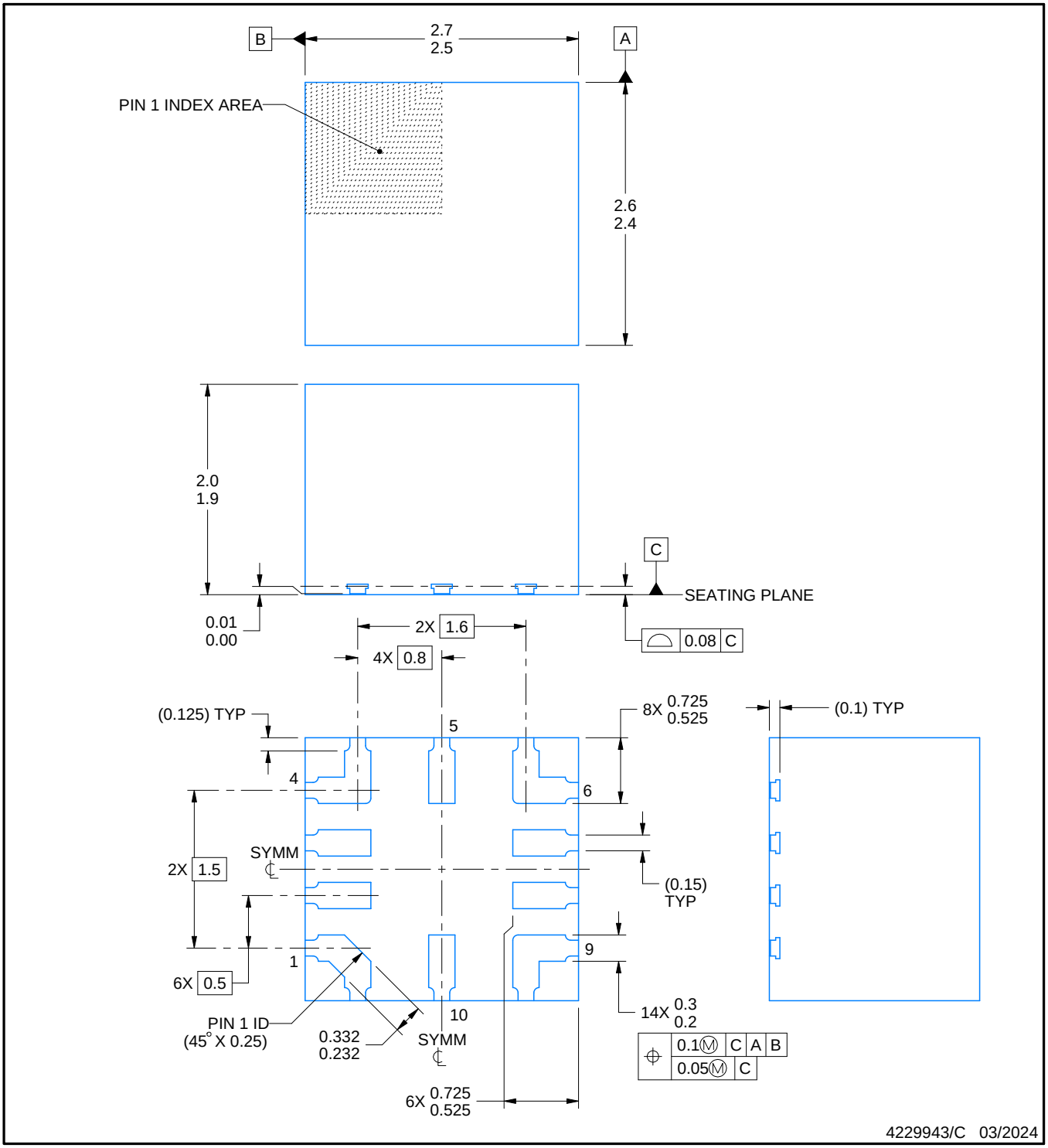
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

VCB0010A

PACKAGE OUTLINE

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

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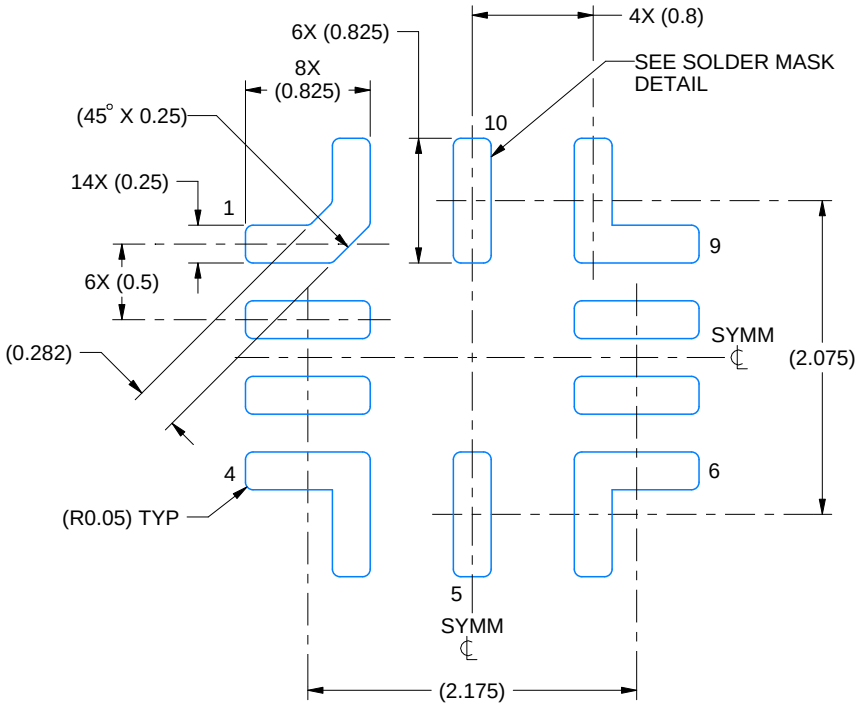
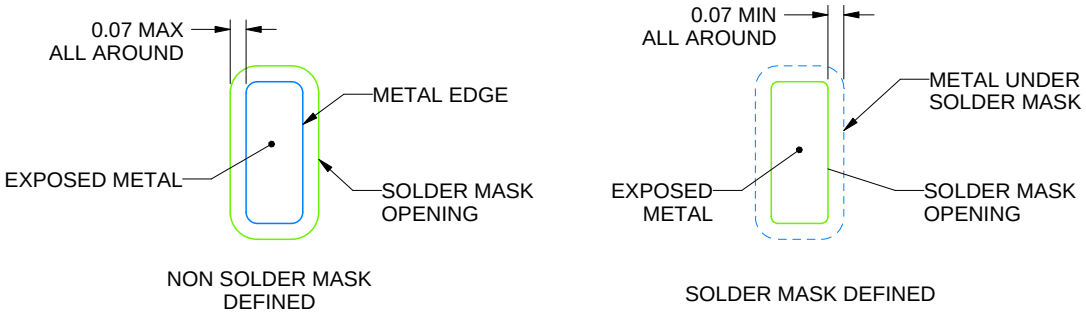
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

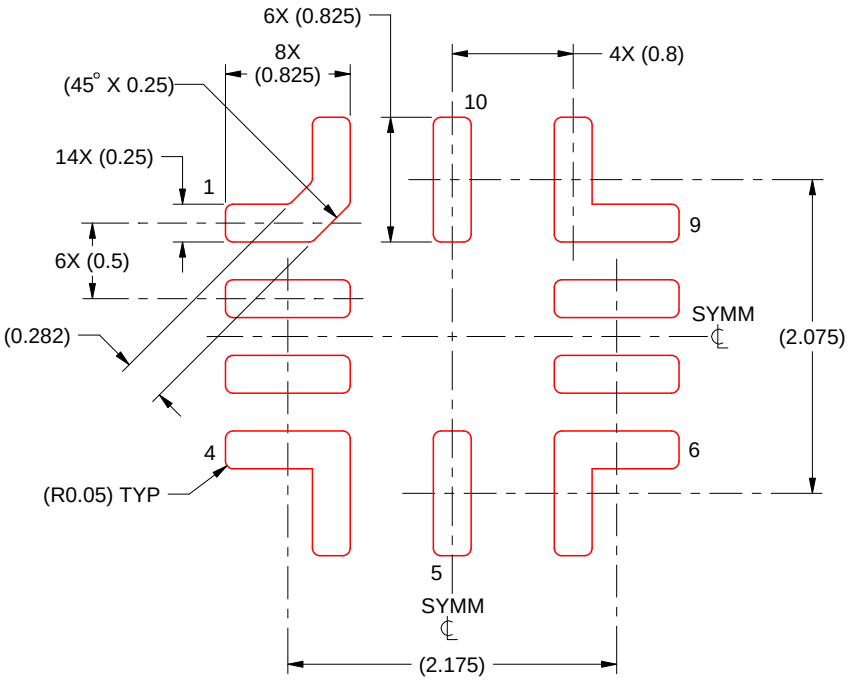


SOLDER MASK DETAILS

4229943/C 03/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4229943/C 03/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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