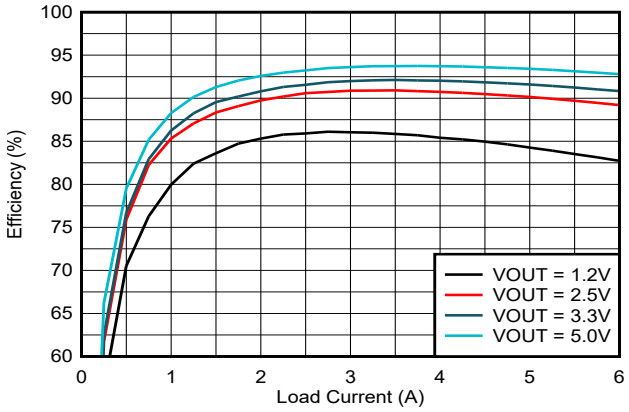
TPSM8F7x20 4V to 17V, 4/6A, Quad Step-Down Power Module

1 Features

- Fixed-frequency, peak current mode (PCM) control
- Small form factor 12.0mm x 7.0mm x 2.4mm, overmolded BGA power module
- Four independent synchronous buck outputs
- Supports 2, 3, and 4-phase stackability for higher output current
- High-efficiency, integrated MOSFETs, inductor, and basic passives.
- 4V to 17V input voltage range
- 0.6V to 11V output voltage range
- Selectable internal or external compensation
- Continuously adjustable switching frequency from 400kHz to 2.2MHz
- Synchronizable to an external clock
- 0.6V, ±0.75% voltage reference accuracy over the full temperature range
- Sequencing features
  - Enable with adjustable input UVLO
  - Power-good output monitor
  - Output discharge
  - Monotonic start-up into prebiased outputs
  - Adjustable soft-start time with external SS pin
- Output overvoltage (OV), undervoltage (UV), overcurrent (OC), and thermal shutdown protection
- Analog temperature output on the MSEL1/2 pins
- –40°C to 125°C module temperature range
- Create a custom design using TPSM8F7x20 with the WEBENCH® Power Designer

2 Applications

- Test and measurement, aerospace
- Medical and healthcare
- FPGA, ASIC, and DSP I/O voltage



Typical Efficiency, 12V Input, 1MHz Fsw

3 Description

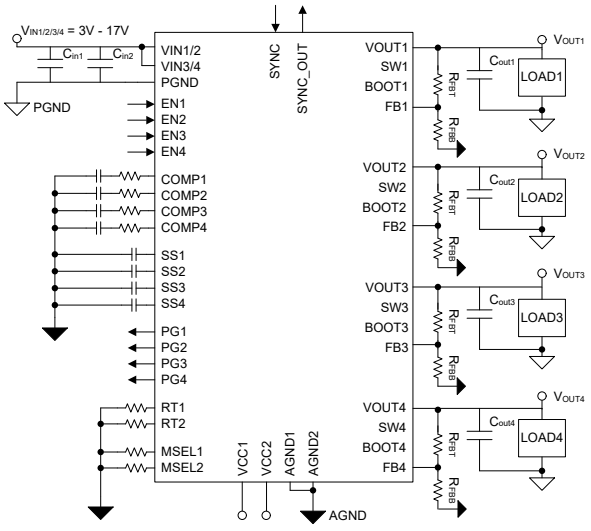
The TPSM8F7x20 is a power-dense quad-channel buck power module designed to provide efficient and reliable power conversion for a wide output voltage range from 0.6V to 11V. The module integrates MOSFETs, inductor, and select capacitors to reduce board space and layout complexity. The module can be configured into both multiphase and multi-output rails by supporting 2, 3, and 4-phase stackability with interleaved phases. Under steady-state conditions the module operates in FCCM with a fixed-frequency that is resistor adjustable from 400kHz to 2.2MHz and synchronizable to an external clock.

TPSM8F7x20 module employs current mode control with internal and external compensation. Sequencing requirements are easily met with the external soft-start, active output discharge, adjustable EN, and power-good features. A full suite of protection features (output OV and UV, input UVLO, TSD, OC) are also included for robustness.

Device Information

PART NUMBER(3)	PACKAGE(1)	PACKAGE SIZE(2)
TPSM8F7420	APG (FCCSP, 112)	12.0mm × 7.0mm
TPSM8F7620		

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) See the *Device Comparison Table*.



Typical Schematic

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4 Device Comparison Table

DEVICE	ORDERABLE PART NUMBER	RATED CHANNEL CURRENT	PACKAGE	JUNCTION TEMPERATURE RANGE
TPSM8F7620	TPSM8F7620APGR	6A	FCCSP (112)	–40°C to 125°C
TPSM8F7420	TPSM8F7420APGR	4A	FCCSP (112)	–40°C to 125°C

5 Pin Configuration and Functions

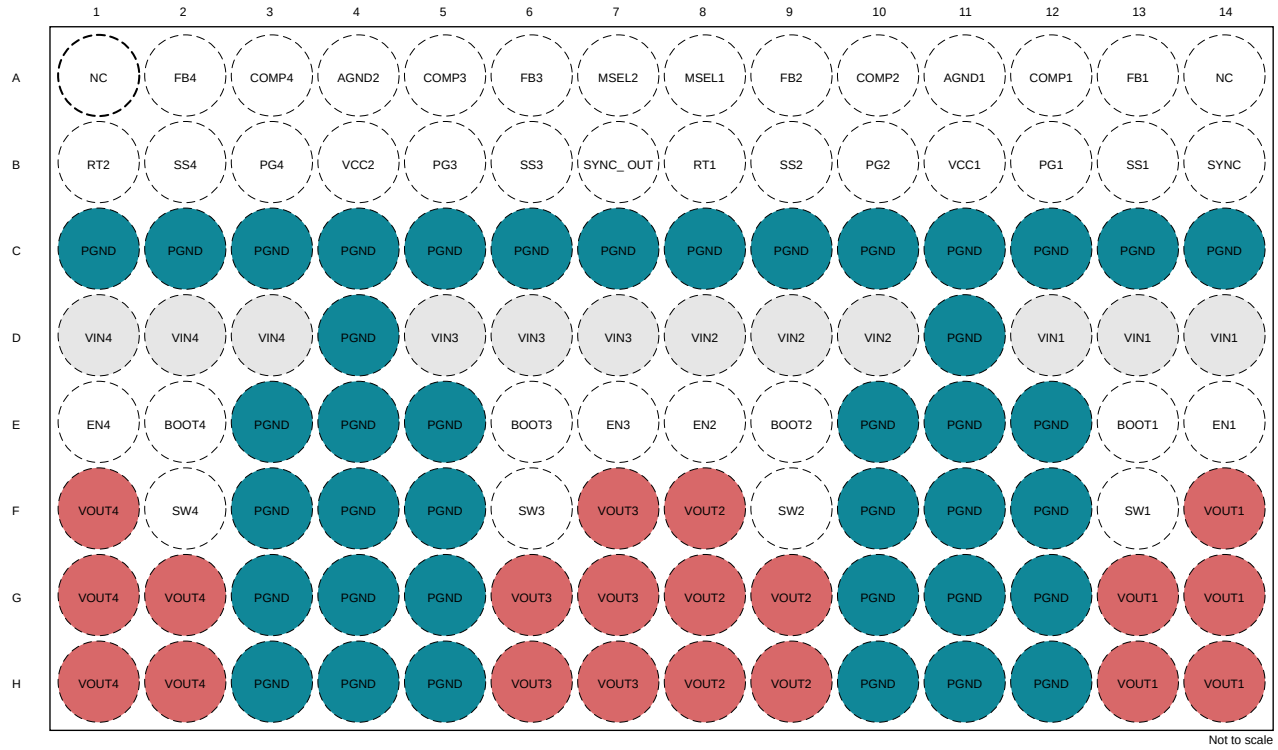


Figure 5-1. 112-Pin FCCSP, APG Package (Top View)

Legend	
VIN*x*	PGND
VOUT*x*	All other pins

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
D12, D13, D14	VIN1	I	Input supply to the regulator. Place the decoupling input capacitors from the VIN pins to PGND pins as close as possible. There is an internal 100nF high-frequency decoupling from VIN to PGND on each channel of the module.
D8, D9, D10	VIN2		
D5, D6, D7	VIN3		
D1, D2, D3	VIN4		
F14, G13, G14, H13, H14	VOUT1	O	VOUT power connection. Connect the output capacitors from VOUT to PGND close to the module output pins.
F8, G8, G9, H8, H9	VOUT2		
F7, G6, G7, H6, H7	VOUT3		
F1, G1, G2, H1, H2	VOUT4		

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, D4, D11, E3, E4, E5, E10, E11, E12, F3, F4, F5, F10, F11, F12, G3, G4, G5, G10, G11, G12, H3, H4, H5, H10, H11, H12	PGND	G	Ground return for the power stage. This pin is internally connected to the source of the low-side MOSFET.
E13	BOOT1	I/O	Supply for the internal high-side MOSFET gate driver. Connected to an internal 100nF capacitor between SW and BOOT. Monitoring connection only, use as NC in design.
E9	BOOT2		
E6	BOOT3		
E2	BOOT4		
F13	SW1	O	Switch node of the module. Monitoring connection only, use as NC in design.
F9	SW2		
F6	SW3		
F2	SW4		
B14	SYNC	I	An external clock can be applied to this pin to synchronize the switching frequency.
B7	SYNC_ OUT	O	Synchronization signal between top and bottom channel pairs. Monitoring connection only, use as NC in design or as SYNC for another regulator.
A8	MSEL1	I/O	Multi-function select pin. A resistor from the MSEL pin to AGND selects between internal and external compensation and sets the channel configuration and phase. A ±1% tolerance resistor is required. After startup, this pin becomes an analog temperature output.
A7	MSEL2		
E14	EN1	I	Enable pin. An active high input to EN enables VOUT. EN must never be left floating.
E8	EN2		
E7	EN3		
E1	EN4		
B11	VCC1	P	Internal LDO regulator output. An internal 2.2µF capacitor is connected between VCC1, VCC2 and AGND1, AGND2 respectively. VCC can be used as a pullup for PG. Otherwise leave VCC floating.
B4	VCC2		
A13	FB1	I	Feedback pin for output voltage regulation. Connect this pin to the midpoint of the resistor divider to set the output voltage. A ±1% tolerance resistor or better is recommended.
A9	FB2		
A6	FB3		
A2	FB4		
A11	AGND1	G	Analog ground connection. Ground return for the internal voltage reference and analog circuits. Tie AGND1 and AGND2 together with a low-impedance connection.
A4	AGND2		
B8	RT1	I	Frequency programming pin. A resistor from RT to AGND sets the oscillator frequency between 400kHz and 2.2MHz. A ±1% tolerance resistor is recommended.
B1	RT2		
B13	SS1	I	Connect a capacitor from the SS pin to AGND to set the soft-start time.
B9	SS2		
B6	SS3		
B2	SS4		

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
A12	COMP1	I/O	Output of the GM error amplifier in external compensation mode. Current sharing signal in multiphase mode. Can be left floating for internal compensation mode.
A10	COMP2		
A5	COMP3		
A3	COMP4		
B12	PG1	O	Open-drain power-good status signal. Connect an external pullup resistor to VCC or external voltage source. When the FB voltage moves outside the specified limits, PG goes low after the specified delay.
B10	PG2		
B5	PG3		
B3	PG4		
A1, A14	NC	N/A	No connection. This pin can be left floating.

(1) I = input, O = output, P = power, G = ground, N/A = not applicable

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN	–0.3	18	V
Pin voltage(2)	VOUT	–0.3	15	V
Pin voltage(2)	SW	–0.3	18	V
Pin voltage(2)	BOOT - SW	–0.3	6	V
Pin voltage(2)	EN	–0.3	18	V
Pin voltage(2)	PG, MSEL, RT, FB	–0.3	6	V
Pin voltage(2)	COMP	–0.3	6	V
Pin voltage(2)	SS	-0.3	6	V
Pin voltage(2)	SYNC, SYNC_OUT	–0.3	5.5	V
Pin voltage(2)	VCC to AGND	–0.3	5.5	V
Pin voltage(2)	PGND to AGND voltage differential	–1	2	V
Sink current	PG		10	mA
Mechanical Vibration	20 – 2000 Hz (X, Y, Z)		20	G
Mechanical Shock	Module mechanical shock rating (+/- X, Y, Z)		1500	G
T_{module}	Operating module temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal (unless otherwise noted).

6.2 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{OUT}	Output voltage		0.6		11	V
V_{IN}	Input voltage		4		17	V
F_{SW}	Switching frequency		400		2200	kHz
I_{OUT}	Output current range	TPSM8F7420	0		4	A
I_{OUT}	Output current range	TPSM8F7620	0		6	A
T_J	Operating module temperature		–40		125	°C

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.4 Thermal Information

THERMAL METRIC[1]		TPSM8F7x20 APG (FCCSP) 112 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	13.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.94	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.56	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note

6.5 Electrical Characteristics

Over recommended input voltage range, T_J = –40°C to +125°C. Typical values are at T_J = 25°C and V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current in VIN1 + VIN2, VIN3 + VIN4, multiphase mode	Non-switching, V_{EN} = 2V, MSEL=41.2kΩ, RT=6.8kΩ, SS=0V		2	4.9	mA
I_Q	Quiescent current in VIN1 + VIN2, VIN3 + VIN4, multi-output mode	Non-switching, V_{EN} = 2V, MSEL=29.4kΩ, RT=6.8kΩ, SS=0V		4.3	8.2	mA
I_{SD}	Shutdown supply current in VIN1 + VIN2, VIN3 + VIN4	V_{EN} = 0V		2	10.1	µA
UVLO						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising		3.5	3.8	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling		2.5	3	V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis			1.2		V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.125	1.25	1.375	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	0.75	0.84	1.0	V
$V_{EN(H)}$	EN voltage hysteresis		0.25	0.4	0.55	V
$V_{EN(W)}$	EN voltage wake-up threshold		0.4			V
I_{EN}	EN pin sourcing current post EN rising threshold	V_{EN} = V_{IN} = 12V			400	nA
INTERNAL LDO						
V_{VCC}	Internal LDO output voltage	V_{IN} ≥ 5V, I_{VCC} ≤ 100mA	4	4.4	5	V
I_{VCC}	Internal LDO short-circuit current limit	V_{IN} = 12V	130	220		mA
REFERENCE VOLTAGE						
V_{FB_INT}	FB reference voltage	Internal compensation selected, no load current.	595.5	600	604.5	mV
V_{FB_EXT}	FB reference voltage	External compensation selected, V_{COMP} = 0.6V	595.5	600	604.5	mV
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = 0.6V		10	250	nA
ERROR AMPLIFIER						
g_{m-ext}	EA transconductance - External Comp	V_{FB} = V_{COMP}	840	1000	1150	µS
$I_{COMP(src)}$	EA source current - External Comp	V_{COMP} = 1V, V_{FB} = 0.4V	100	155	400	µA
$I_{COMP(sink)}$	EA sink current - External Comp	V_{COMP} = 1V, V_{FB} = 0.8V	50	155	500	µA
SWITCHING FREQUENCY						
$f_{SW-max(FCCM)}$	Switching frequency, FCCM operation	R_{RT} = 6.81kΩ to AGND	1.95	2.2	2.4	MHz
$f_{SW\ (FCCM)}$	Adjustable switching frequency range	R_{RT} resistor from 6.81kΩ to 39.2kΩ to AGND	0.4		2.2	MHz
SYNCHRONIZATION						
$V_{IH(sync)}$	SYNC High-Level Threshold			1.25	1.5	V
$V_{IL(sync)}$	SYNC Low-Level Threshold		0.65	1.0		V
$V_{OH(sync)}$	Sync output high voltage min	No loading on SYNC_OUT pin		4.4		V

6.5 Electrical Characteristics (continued)

Over recommended input voltage range, T_J = –40°C to +125°C. Typical values are at T_J = 25°C and V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OL(sync)}$	Sync output low voltage max	No loading on SYNC_OUT pin		0.6		V
$f_{SYNC-2p2}$	Frequency sync range around 2.2MHz	R_{RT} = 6.81kΩ to AGND	1.76	2.2	2.64	MHz
$f_{SYNC-0p4}$	Frequency sync range around 400kHz	R_{RT} = 39.2kΩ to AGND	320	400	480	kHz
$t_{SYNC(IH)}$	Minimum pulse width of external synchronization signal above $V_{IH(sync)}$			50		ns
$t_{SYNC(IL)}$	Minimum pulse width of external synchronization signal below $V_{IL(sync)}$			50		ns
$t_{SYNC-SW(delay)}$	Delay from SYNC rising edge to SW rising edge			40		ns
STARTUP						
$I_{SS(R)}$	Soft-start charge current	V_{SS} = 0 V		21		µA
t_{EN}	EN HIGH to start of switching delay	V_{IN} > $VIN_{UVLO(R)}$			1300	µs
$R_{SS(F)}$	Soft-start discharge resistance			22	45	Ω
POWER STAGE						
$t_{ON(min)}$	Minimum ON pulse width (1)	V_{IN} = 12V		45	60	ns
$t_{OFF(min)}$	Minimum OFF pulse width (1)	V_{IN} = 4V		60	105	ns
OVERCURRENT PROTECTION						
$I_{HS(OC1)}$	High-side peak current limit TPSM8F7620	Peak current limit on HS FET	8.2	9	9.6	A
$I_{HS(OC2)}$	High-side peak current limit TPSM8F7420	Peak current limit on HS FET	6.3	7.2	8.2	A
$I_{LS(OC1)}$	Low-side valley current limit TPSM8F7620	Valley current limit on LS FET	5.9	6.8	7.2	A
$I_{LS(OC2)}$	Low-side valley current limit TPSM8F7420	Valley current limit on LS FET	4.4	5.4	6.4	A
$I_{LS1(NOC)}$	Low-side negative current limit TPSM8F7620	Sinking current limit on LS FET		–4	–3	A
$I_{LS3(NOC)}$	Low-side negative current limit TPSM8F7420	Sinking current limit on LS FET		–3.5	–2.5	A
$V_{Hiccup-FB}$	Hiccup threshold on FB pin	HS FET On-time > 165 ns	0.18	0.23	0.3	V
$t_{Hiccup-1}$	Wait time before entering Hiccup		126	128	130	Curent Limit cycles
$t_{Hiccup-2}$	Hiccup time before re-start		50	70		ms
OUTPUT DISCHARGE						
$R_{Discharge}$	Output discharge resistance	V_{IN} = 12V, V_{OUT} = 2.5V, power conversion disabled		19.5		Ω
POWER GOOD						
V_{PGTH-1}	Power-Good threshold (PG)	PGOOD low, V_{FB} rising	93	96	99	% V_{REF}
V_{PGTH-2}	Power-Good threshold (PG)	PGOOD high, V_{FB} falling	91	93	95	% V_{REF}
V_{PGTH-3}	Power-Good threshold (PG)	PGOOD high, V_{FB} rising	109	113	117	% V_{REF}
V_{PGTH-4}	Power-Good threshold (PG)	PGOOD low, V_{FB} falling	107	110	113	% V_{REF}
$t_{PGOOD(R)}$	PG delay from V_{FB} valid to PGOOD high	V_{VOUT} = 3.3V	300		700	µs
$t_{PGOOD(F)}$	PG delay from V_{FB} invalid to PGOOD low	V_{VOUT} = 3.3V		47		µs
$I_{PG(LKG)}$	PG pin Leakage current when open drain output is high	V_{PG} = 3.3 V			0.075	µA
$V_{PG-D(LOW)}$	PG pin output low-level voltage for both channels	I_{PG} = 1 mA, V_{EN} = 0 V, V_{IN} > $V_{IN(PG\_VALID)}$.			400	mV
R_{PG}	Pull Down MOSFET Resistance	I_{PG} = 1 mA, V_{EN} = 3.3 V.		35	90	Ω
$V_{IN(PG\_VALID)}$	Minimum VIN for valid PG output	Pull up resistance on PG - R_{PG} = 10 kΩ, Voltage Pull up on PG - V_{PULLUP_PG}=3V, $V_{PG-D\ (LOW)}$=0.4V			1.2	V
THERMAL SHUTDOWN						

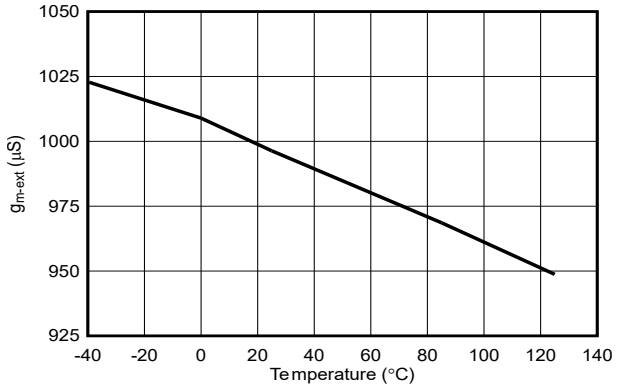
6.5 Electrical Characteristics (continued)

Over recommended input voltage range, T_J = –40°C to +125°C. Typical values are at T_J = 25°C and V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{J(SD)}$	Thermal shutdown threshold (1)	Temperature rising	153	167	186	°C
$T_{J(HYS)}$	Thermal shutdown hysteresis (1)			9		°C
T_{sense}	TEMP sensing accuracy (1)	After calibration at T_A=25°C	–10		+10	°C

(1) Verified by design.

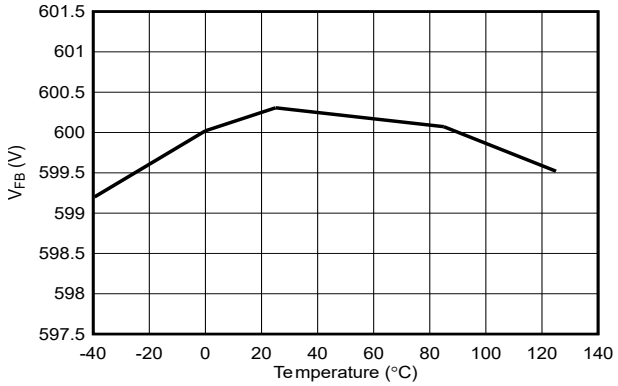
6.6 Typical Characteristics



V_{IN}= 12V External Compensation

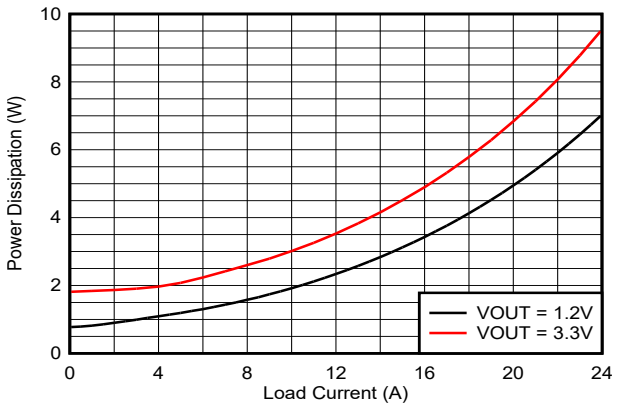
TPSM8F7620

Figure 6-1. Error Amplifier GM vs Temperature



V_{FB}=V_{COMP}

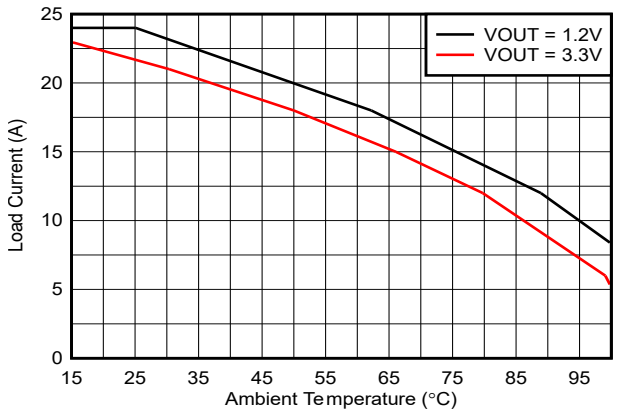
Figure 6-2. V_{FB} vs Temperature



V_{IN}= 12V 4-PH Output 22°C Ambient

f_{SW}= 1MHz TPSM8F7620 No Heat Sink

Figure 6-3. Power Dissipation 12V Input



V_{IN}= 12V 4-PH Output 0 LFM

f_{SW}= 1MHz TPSM8F7620 No Heat Sink

Figure 6-4. Maximum Output Current vs Ambient Temperature

7 Detailed Description

7.1 Overview

The TPSM8F7x20 is an easy-to-use, synchronous buck DC/DC power module designed for a wide variety of applications where small solution size, flexible multiphase/multi-output, and compensation configurability are important. With four channels of integrated power MOSFETs, inductors, capacitors, and PWM controllers, the TPSM8F7x20 operates over an input voltage range of 4V to 17V. The module delivers up to 4/6A per channel with the TPSM8F7420/TPSM8F7620 respectively. Selectable internal or external control loop compensation gives the designer maximum flexibility to reduce the amount of output capacitors while maintaining stability.

With an adjustable switching frequency from 400kHz to 2.2MHz using the RT pin, the TPSM8F7x20 has a wide output voltage range up to 11V.

Several EMI reduction features are included in the module.

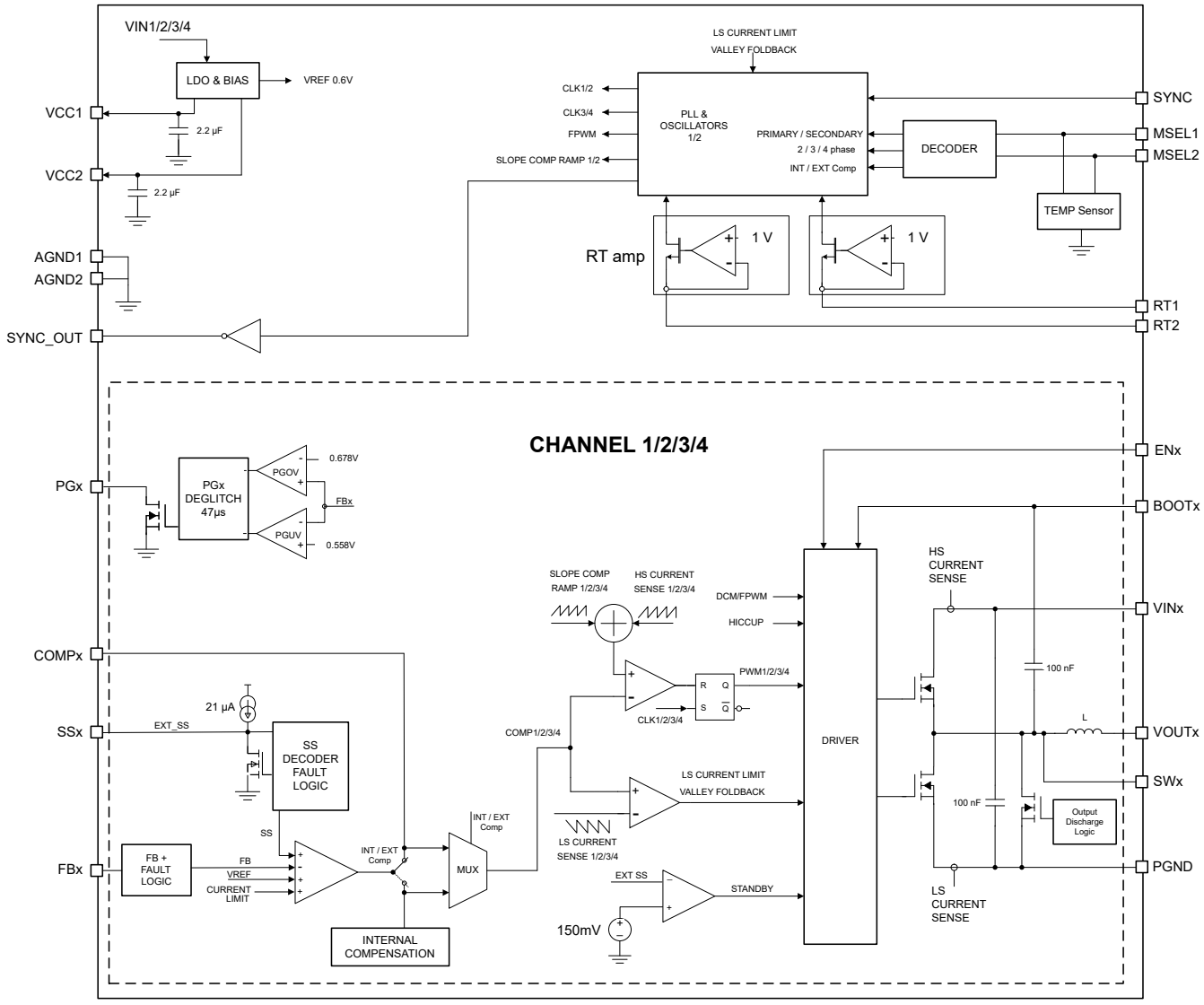
- Integrated high-frequency capacitor layouts minimize parasitic inductance, switch-voltage ringing, and radiated field coupling
- Clock synchronization and FPWM mode enable constant switching frequency across the load current range
- Integrated power MOSFETs with enhanced gate drive control enable low-noise PWM switching

The TPSM8F7x20 module also includes inherent protection features for robust system requirements:

- An open-drain power good (PG) indicator for power-rail sequencing and fault reporting
- An active output voltage discharge and external soft-start pin enable predictable sequencing
- Precision enable input with hysteresis, providing
  - Programmable line undervoltage lockout (UVLO)
  - Remote ON and OFF capability
- Hiccup-mode overcurrent protection with cycle-by-cycle peak and valley current limits
- Thermal shutdown with automatic recovery

Leveraging a pin arrangement designed for simple layout that requires only a few external components, the TPSM8F7x20 is specified to maximum internal operating temperatures of 125°C. See Section 6.6 to estimate suitability in a given ambient environment.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage Range (VIN)

The VIN pin voltage supplies the internal control circuits of the device and provides the input voltage to the power stage. The input voltage for VIN can range from 4V to 17V. The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 1V. A voltage divider connected to the EN pin can adjust the input voltage UVLO as appropriate.

The minimum input voltage required for start-up is 3.5V. Take extra care to make sure that the voltage at the VIN pins of the module (VIN1/2/3/4) does not exceed the absolute maximum voltage rating of 18V during line or load transient events. Voltage ringing at the VIN pins that exceeds the Absolute Maximum Ratings can damage the IC.

Note that VIN1/2 and VIN3/4 can be powered from a separate supply, but powering up both VIN supplies at the same time is recommended.

7.3.2 Bias Supply Regulator (VCC)

VCC is the output of the internal LDO regulator used to supply the control circuits of the TPSM8F7x20. The nominal VCC voltage is 4.4V. This module integrates the VCC bypass capacitor so no additional components are needed, saving board space and layout time.

To prevent unsafe operation, VCC has UVLO protection that prevents switching if the internal voltage is too low.

VCC must not be used to power external circuitry. Do not load VCC or short VCC to ground. VCC can be used as a pull up to the PG pin.

7.3.3 Device Configuration Pin (MSEL)

The MSEL pin is used to set up the device configuration and compensation. There are five different output rail configurations listed in Table 7-1. The configurations specify which and how many channels are paralleled together to provide the module outputs. For example, the configuration "2+2" means there are two total output voltage rails. The first rail is formed fromVOUT1 and VOUT2 and the second rail is formed from VOUT3 and VOUT4. The "1+3" configuration means there are still two output rails, VOUT1 is a single-phase output and VOUT2/3/4 are tied together to form a three-phase output. By using the MSEL pin to configure the device, phase interleaving is set according to the phase angles discussed in Section 7.3.4.

When configured for external compensation the COMP pin becomes the output of the GM error amplifier and Type-II compensation can be used in the control loop. When configured for internal compensation, no additional components on COMP are needed. Note that multiphase configurations can only use external compensation because the COMP signal is shared across each phase in the stack. See Section 7.3.9 for more information.

The MSEL pin also serves as a junction temperature monitor. After pinstrap detection is completed, an analog voltage proportional to the junction temperature is driven on the MSEL pin referenced to AGND. See Section 7.3.15 for more information.

Table 7-1. R_{SEL} Resistor Selection

CONFIG	COMP1	COMP2	R_{MSEL1} (kΩ)	COMP3	COMP4	R_{MSEL2} (kΩ)
1+1+1+1	Internal 1		9.53	Internal 1		9.53
	Internal 2		19.1	Internal 2		19.1
	External		29.4	External		29.4
1+1+2	Internal 1		9.53	External		41.2
	Internal 2		19.1			
	External		29.4			
2+2	External		41.2	External		41.2
1+3(1)	Internal 1	External	56.2	External		121
	Internal 2		73.2			
	External		93.1			

Table 7-1. R_{SEL} Resistor Selection (continued)

CONFIG	COMP1	COMP2	R_{MSEL1} (kΩ)	COMP3	COMP4	R_{MSEL2} (kΩ)
4+0[2]	External		121	External		121

(1) This configuration always uses CH1 as the standalone primary and CH2 as the multiphase primary
(2) This configuration always uses CH1 as the multiphase primary

7.3.4 Multiphase Output Configuration

The multiphase buck converter topology is created by putting multiple buck converters in parallel and involves interleaving the phases 360/N degrees apart from one another. Where N is the number of phases. Some advantages to the multiphase buck converter are:

- Increased output current by N times
- Reduced output voltage ripple
- Reduced input current ripple
- Improved thermal spreading

To configure the device in a multiphase output, the SS, EN, and COMP pins of the respective channels must be tied together as specified in Table 7-3. Review Table 7-1 to see what multiphase configurations are supported by this device.

When selecting multiphase or multi-output configurations with this module, the phases are interleaved according to Table 7-2.

Table 7-2. Phase Interleaving per Configuration

CONFIG	SW1	SW2	SW3	SW4
1+1+1+1	0°	180°	90°	270°
1+1+2				
2+2				
4+0				
1+3	0°	180°	300°	60°

The individual channels in the TPSM8F7x20 can be configured as a standalone output, multiphase primary, or multiphase secondary. The primary device in a multiphase stack is always the first channel within the stack. For example, in the "1+3" configuration CH2 corresponds to the 3-PH primary channel and CH3/4 are the multphase secondaries. The details of the recommended pin connections for each Primary and Secondary are given in Table 7-3.

Table 7-3. Multiphase Pin Connections

PIN	PRIMARY	SECONDARY
FB	VOUT Resistor Divider	NC/Float
EN	VIN Resistor Divider or Enable/Control	Connect to Primary's EN
SS	Connect C_{SS} from this pin to AGND	Connect to Primary's SS
COMP	Connect compensation network from this pin to AGND	Connect to Primary's COMP
PG	Connect R_{PG} from this pin to VCC	NC/Float

7.3.5 Enable and Adjustable UVLO

Apply a voltage less than 0.4V to the EN1, EN2 and EN3, EN4 pins to put the TPSM8F7x20 into shutdown mode. In shutdown mode, the quiescent current drops to 2µA (typical). Above this voltage but below the lower EN threshold, VCC is active but switching on SW1 and SW2 remains inactive. After EN1 is above $V_{EN(R)}$, SW1 becomes active. EN2 controls switching on the second output SW2. In multi-output configuration ENx can

be used to independently turn off the VOUTx output voltage. In single-output multiphase configuration EN on primaries and secondaries must be tied together.

The EN pins can not be left floating. The simplest method to enable the operation is to connect the EN pins to VIN. This action allows the self-start-up of the device when VIN drives the internal VCC above the UVLO level. However, many applications benefit from employing an enable divider string, which establishes a precision input undervoltage lockout (UVLO). The precision UVLO can be used for the following:

- Sequencing based on VIN voltage
- Preventing the device from retriggering when used with long input cables

Note that EN thresholds are accurate. The rising enable threshold has a 10% tolerance. Hysteresis is enough to prevent retriggering upon shutdown of the load. The external logic output of another IC can also be used to drive the EN terminals, allowing system power sequencing.

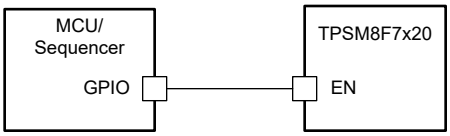


Figure 7-1. Enable using an External Sequencer

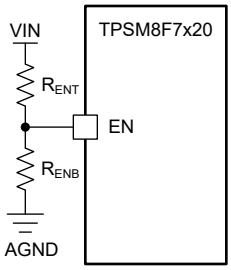


Figure 7-2. VIN UVLO Using the EN Pin

Resistor values can be calculated using the following equations.

$$R_{ENB} = R_{ENT} \times \left(\frac{V_{EN(R)}}{V_{IN(on)} - V_{EN(R)}} \right) \quad (1)$$

$$V_{OFF} = V_{IN(on)} \times \left(1 - V_{EN(H)} \right) \quad (2)$$

where

- $V_{IN(on)}$ = V_{IN} turn-on voltage
- V_{OFF} = V_{IN} turn-off voltage

7.3.6 Adjustable Switching Frequency

The adjustable switching frequency is set using a resistor from the RT1 and RT2 pins to AGND. See Table 7-4 below for example resistor values. A resistor value that falls outside of the recommended range can cause the device to stop switching. Do not apply a pulsed signal to this pin to force synchronization. If synchronization is needed, use the SYNC pin.

The TPSM8F7x20 has four total switching channels. The first two channels are set by RT1 and the second two by RT2. All of the channels on this module are required to share the same switching frequency in steady-state to verify that each channel has the correct phase. This means that the RT1 and RT2 resistors must use the same 1% resistance value.

$$R_T[k\Omega] = \left(\frac{15.92}{F_{SW}[MHz]} - 0.526\right) \quad (3)$$

For example, for f_{SW} = 400kHz, R_T = (15.92 / 0.4) - 0.526 = 39.27, so a 39.2kΩ resistor is selected as the closest choice.

Table 7-4. Typical R_T values

R_T (kΩ)	CALCULATED FREQUENCY (kHz)
6.81	2170
10.0	1512
15.4	1000
19.6	791
23.7	657
31.6	496
39.2	402

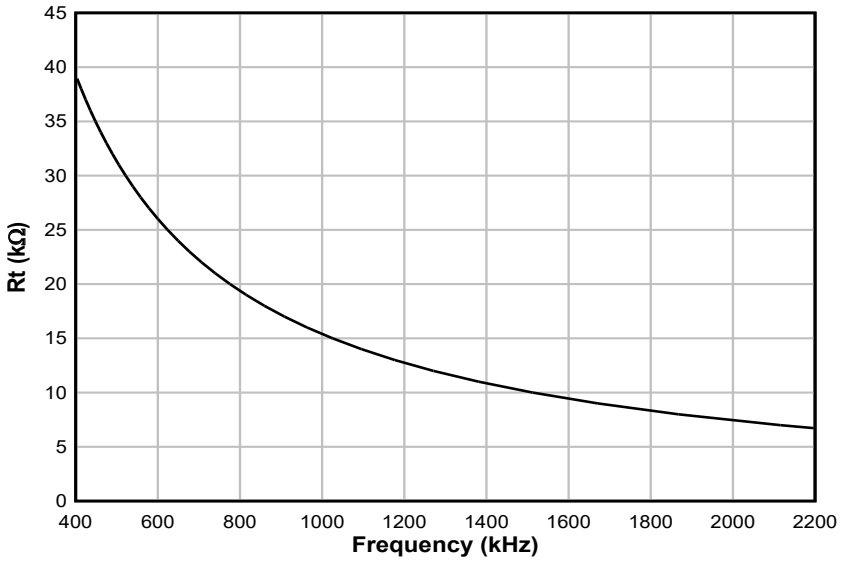
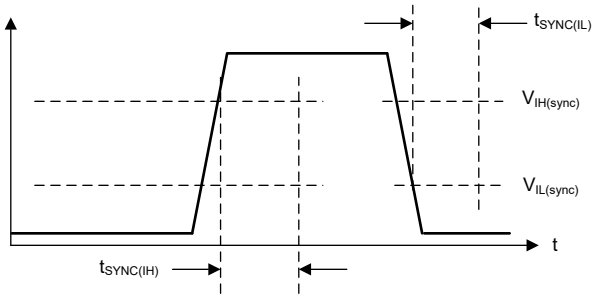


Figure 7-3. Setting Clock Frequency

7.3.7 Device Synchronization (SYNC)

The SYNC pin is used to synchronize the internal oscillator to an external clock. When synchronized to an external clock, the TPSM8F7x20 operates in FPWM. The internal oscillator can be synchronized to a positive edge into the SYNC pin. The rising edge voltage at the SYNC pin must exceed the SYNC amplitude threshold of $V_{IH(sync)}$ to trip the internal synchronization pulse detector. The minimum SYNC rising pulse and falling pulse durations must be longer than $t_{SYNC(IH)}$ and $t_{SYNC(IL)}$ respectively. The TPSM8F7x20 switching action can

be synchronized to an external clock from 320kHz to 2.6MHz. When synchronizing to an external clock, the frequency input must be within approximately ±20% of the internal clock frequency programmed by the RT pin. This action prevents large frequency changes in the event of loss of synchronization. This action is also used to set the slope compensation for secondary devices.



This image shows the conditions needed for detection of a synchronization signal.

Figure 7-4. Typical SYNC Waveform

7.3.7.1 Clock Locking

The TPSM8F7x20 uses the SYNC pin input differently depending on the configuration selected by the MSEL pin. When CH1 is configured to be the multiphase primary channel, which occurs in the "4+0" and "2+2" configurations, then CH1 uses a PLL circuit to lock the CH1 oscillator frequency to the SYNC input. In all other configurations where CH1 is a standalone output, the SYNC input directly connects the CH1 oscillator. Then the PLL circuit is used for phase interleaving between CH1 and CH2.

After a valid synchronization signal is detected on the SYNC pin, a clock locking procedure is initiated. If CH1 is a standalone single-phase output, then SYNC directly connects the CH1 oscillator and changes the switching frequency immediately. In all other configurations, after approximately 32 pulses, the clock frequency abruptly changes to the frequency of the synchronization signal. While the frequency adjusts suddenly, phase is maintained so the clock cycle lying between operation at the default and synchronization frequencies is of intermediate length. There are no very long or very short pulses. After frequency is adjusted, phase is adjusted over a few tens of cycles so that rising synchronization edges correspond to rising the SW node pulses.

7.3.8 Adjustable Output Voltage (FB)

The TPSM8F7x20 has an adjustable output voltage range from 0.6V up to a maximum of 11V. Setting the output voltage requires two feedback resistors, designated as R_{FBT} and R_{FBB}. The reference voltage at the feedback (FB) pin is set at 0.6V with a feedback system accuracy over the full junction temperature range of ±0.75% with respect to AGND.

Calculate the value for R_{FBB} using Equation 4 below based on a recommended range for R_{FBT} of 10kΩ to 100kΩ.

$$R_{FBB}(k\Omega) = \frac{R_{FBT}(k\Omega)}{\frac{V_{OUT}}{0.6} - 1} \quad (4)$$

Note that higher feedback resistances consume less DC current. However, an upper R_{FBT} resistor value higher than 1MΩ renders the feedback path more susceptible to noise. Higher feedback resistances generally require more careful layout of the feedback path. Make sure to locate the feedback resistors close to the FB and AGND pins, keeping the feedback trace as short as possible (and away from noisy areas of the PCB). See *Layout Example* guidelines for more detail.

7.3.9 Control Loop Compensation (COMP)

The TPSM8F7x20 employs peak current mode control which makes the control loop simple to compensate. The COMP pin is the output of the GM error amplifier, and Type-II compensation can be implemented with a series R_{COMP}-C_{COMP} connected between COMP and AGND.

Increasing the R_{COMP} resistance results in higher loop gain and tends to require proportionately larger output capacitors. Decreasing C_{COMP} increases the DC loop response of the device, resulting in faster transient settling times but can lower phase margin at the cross-over frequency and can require adjustments to the output capacitance.

7.3.10 Slope Compensation

The TPSM8F7x20 uses a slope compensation ramp to maintain stability across a wide range of duty cycles. The ramp is proportional to the programmed switching frequency through the RT pin resistor. The ramp follows the equation:

$$M_a = \frac{59.54}{RT(k\Omega)}\left(\frac{A}{\mu s}\right) \quad (5)$$

for the TPSM8F7620 and

$$M_a = \frac{92.84}{RT(k\Omega)}\left(\frac{A}{\mu s}\right) \quad (6)$$

for the TPSM8F7420

7.3.11 Power-Good Output Voltage Monitoring

The PG pin of the TPSM8F7x20 resembles a standard open-drain power-good function. There are three major differences between the PG function and the normal power-good function seen in most regulators:

- A delay has been added for release of reset. See Table 7-5.
- PG output signals a fault (pulls the output to ground) while the part is disabled.
- PG continues to operate with input voltage as low as 1.2V. Below this input voltage, PG output can be high impedance.

A 10kΩ or greater pullup resistor from PG to VCC or external voltage source is required for proper PG signaling.

There are a total of four power-good pins on the TPSM8F7x20. If the device is configured to have four outputs, indicating the 1+1+1+1 configuration, then each VOUTx have a corresponding PGx. However, for configurations with less than four outputs, only the primary channel's PG pin is used. For example, in a 4+0 configuration, PG1 is the only power-good pin that is used and the rest can be left floating.

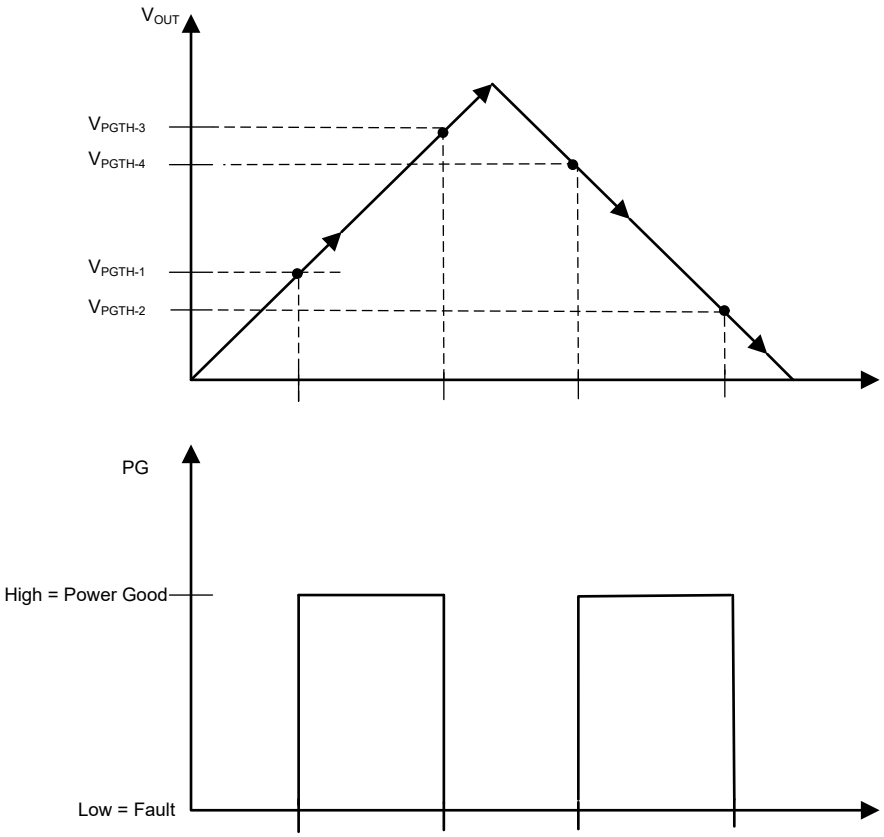


Figure 7-5. PG Static Voltage Thresholds

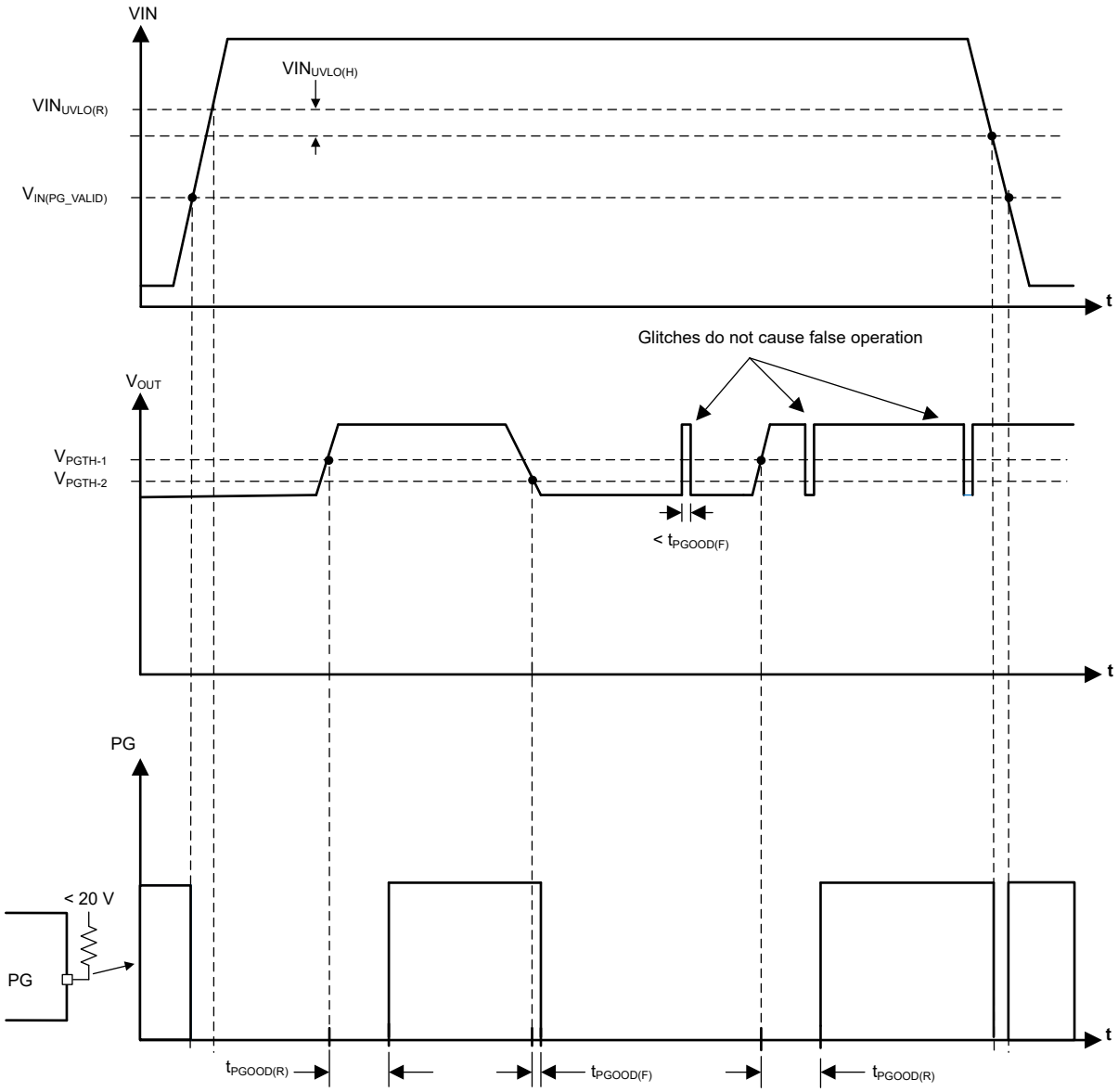


Figure 7-6. PG Timing Diagram (Excludes OV Events)

Table 7-5. Conditions that Cause PG to Signal a Fault (Pull Low)

PG FALLING CONDITIONS	PG RISING CONDITIONS
FB below V_{PGTH-2} for longer than $t_{PGOOD(F)}$	FB above V_{PGTH-1}
FB above V_{PGTH-3} for longer than $t_{PGOOD(F)}$	FB below V_{PGTH-4}
Thermal Shutdown	Junction temperature falls below $T_{J(SD)}$- $T_{J(HYS)}$
EN low	t_{EN} passes after EN becomes high
VIN below $VIN_{UVLO(F)}$, but above $V_{IN(PG\_VALID)}$	VIN above $VIN_{UVLO(R)}$

In addition to signaling a fault upon overvoltage detection (FB above V_{PGTH-3} for longer than $t_{PGOOD(F)}$), the switch node is shut down and a small, approximately 1mA pulldown is applied to the SW node. Once the output overvoltage fault is removed (FB below V_{PGTH-4}) then switching resumes on the SW node.

The PG signal can be used for start-up sequencing of downstream regulators, or for fault protection and output monitoring.

7.3.12 Output Discharge

Output discharge is always enabled to provide power-down sequencing and protect the load when the part isn't in regulation. With output discharge the output voltage is pulled low by a discharge resistor $R_{Discharge}$ of typically 19.5Ω when V_{OUT} is 2.5V. The output discharge function is enabled during thermal shutdown, UVLO, or when EN is pulled low.

7.3.13 Soft-Start (SS)

To prevent inrush current when VOUT is enabled, the TPSM8F7x20 uses an adjustable soft-start pin to slowly ramp the reference voltage. The soft-start feature limits in-rush current on start-up and facilitates a smooth ramp up of VOUT. Soft start is triggered by any of the following conditions:

- EN is used to turn on the device.
- Recovery from a hiccup waiting period
- Recovery from shutdown due to overtemperature protection.
- Power is applied to the VIN of the IC or the VCC UVLO is released.

After soft start is triggered, the IC takes the following actions:

- The reference used by the IC to regulate output voltage is slowly ramped from zero. The net result is that output voltage, if previously 0V, takes t_{SS} to reach 90% of the target value.
- Operating mode is set to diode emulation. This allows start-up without pulling output low if there is a voltage already present on the output.
- Hiccup is disabled for the duration of soft start

This operation allows the use of output capacitors and loading conditions that cause current to border on current limit during start-up without triggering hiccup. In addition, if output voltage is prebiased, the output is not pulled down.

The following equation can be used to calculate the soft-start capacitor value C_{SS} based on the desired soft-start time t_{SS}.

$$C_{SS} = t_{SS} \times \frac{I_{SS(R)}}{V_{FB}} \quad (7)$$

The soft-start charge current $I_{SS(R)}$ and the nominal reference voltage V_{FB} can be found in the Electrical Characteristics.

7.3.14 Overcurrent Protection (OCP)

The TPSM8F7x20 is protected from overcurrent conditions using cycle-by-cycle current limiting of the peak inductor current. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

The TPSM8F7x20 employs hiccup overcurrent protection if there is an extreme overload. In hiccup mode, the module is shut down and kept off for 70ms (typical) before a restart is attempted. If an overcurrent or short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, thus preventing overheating and potential damage to the device. After the fault is removed, the module automatically recovers and returns to normal operation.

7.3.15 Temperature Output

The TPSM8F7x20 has the ability to measure the internal junction temperature of the IC. Internal device temperature can be measured through the voltage on the MSEL1 and MSEL2 pins after the part is enabled and starts switching.

The following equation is used to convert the measured voltage to a temperature signal.

$$T_j = \frac{\left(V_{MSEL\_cal} - V_{MSEL}\right)}{2.10208\frac{mV}{°C}} + T_{cal} \quad (8)$$

Where V_{MSEL_cal} is the MSEL voltage measured at T_{cal} and V_{MSEL} is the measured MSEL voltage to calculate junction temperature T_j. T_{cal} needs to be measured with a thermocouple or IR camera at the module package. Do not add more than 200pF of capacitative loading is placed on this pin. The MSEL pin voltage is expected to be in the range of 0.35V to 0.8V for temperatures ranging from -40°C to 125°C.

7.3.16 Thermal Shutdown

Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 167°C (typical) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the TPSM8F7x20 attempts to restart when the junction temperature falls below 158°C (typical).

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides ON and OFF control for the TPSM8F7x20. When V_{EN} is below approximately 0.25V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 2 µA (typical). The TPSM8F7x20 also employs internal undervoltage protection. If the input voltage is below the UV threshold, the regulator remains off.

7.4.2 Standby Mode

The internal LDO for the VCC bias supply has a lower enable threshold than the regulator. When V_{EN} is above $V_{EN(W)}$ and below the precision enable threshold of $V_{EN(R)}$, the internal LDO is on and regulating. The precision enable circuitry is turned on after the internal V_{CC} is above the UVLO threshold. The switching action and voltage regulation are not enabled until V_{EN} rises above the precision enable threshold.

7.4.3 Active Mode

The TPSM8F7x20 is in active mode when V_{VCC} and V_{EN} are above the relevant thresholds and no fault conditions are present. The simplest method to enable operation is to connect V_{EN} to V_{IN}, which allows self start-up when the applied input voltage exceeds the minimum start-up voltage.

7.4.3.1 Peak Current Mode Operation

The following operating description of the TPSM8F7x20 refers to *Functional Block Diagram* and the waveforms in Figure 7-7. Both supply a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) NMOS switches with varying duty cycle (D). During the HS switch on-time, the SW terminal voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off-time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, forcing V_{SW} to swing below ground by the voltage drop across the LS switch. The regulator loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on-time of the HS switch over the switching period: $D = T_{ON} / (T_{ON} + T_{OFF})$.

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D = V_{OUT} / V_{IN}$.

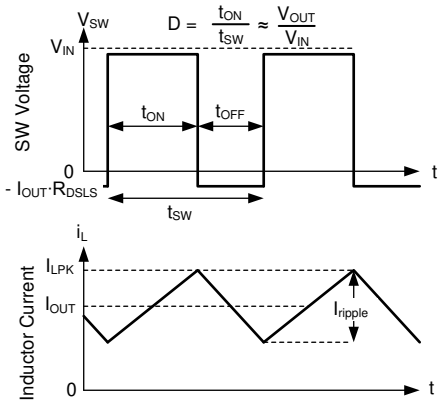
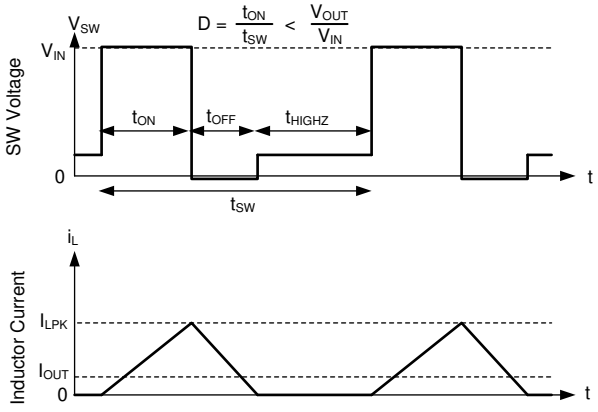


Figure 7-7. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

To get accurate DC load regulation, a voltage feedback loop is used. Peak and valley inductor currents are sensed for peak current mode control and current protection. The regulator operates with continuous conduction mode with constant switching frequency when load level is above one half of the minimum peak inductor current. The externally and internally-compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

7.4.3.2 Diode Emulation

Diode emulation prevents reverse current though the inductor, which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. Frequency is reduced when peak inductor current goes below $I_{PEAK-MIN}$. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



In discontinuous mode (DCM), the low-side device is turned off after inductor current is near zero. As a result, after output current is less than half of inductor ripple in CCM, the part operates in DCM. This is equivalent to saying that diode emulation is active.

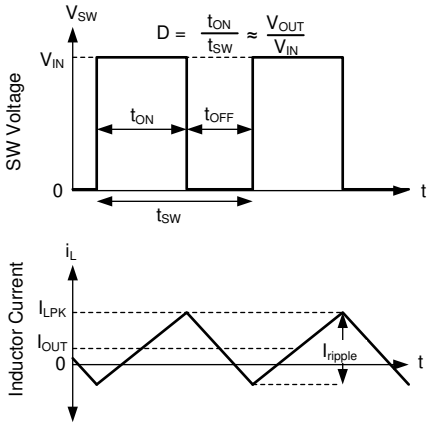
Figure 7-8. PFM Operation

The TPSM8F7x20 has a minimum peak inductor current setting in that is used during startup. That being said, when current is reduced to a low value with fixed input voltage, on-time is constant. Regulation is then achieved by adjusting frequency. DCM is enabled during soft-start to ramp up VOUT and prevent a prebiased output from being discharged. Otherwise, the part operates in Forced CCM mode even at light load.

7.4.3.3 FPWM Mode Operation

In steady-state operation, the part always operates in FPWM mode. Exceptions include faults, current limits, and startup.

In FPWM Mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by the negative current limit circuitry. See the *Electrical Characteristics* for negative current limit values.



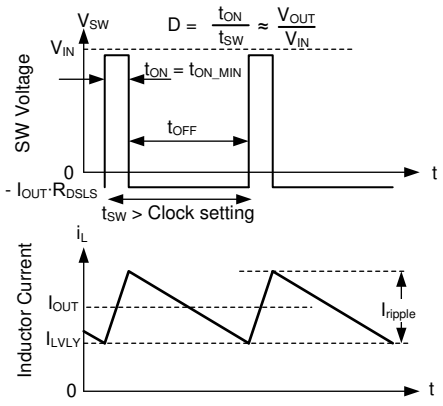
FPWM mode Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of Iripple.

Figure 7-9. FPWM Mode Operation

In FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on-time, even while lightly loaded. This allows good behavior during faults which involves the output being pulled up.

7.4.3.4 Minimum On-time (High Input Voltage) Operation

The TPSM8F7x20 continues to regulate output voltage if the input-to-output voltage ratio requires an on-time less than the minimum on-time of the chip with a given clock setting. This is accomplished using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If, for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If the device is not operating within the current limit, the maximum valley current is set above the peak inductor current. This prevents valley control from being used unless there is a failure to regulate using peak current only. If the input-voltage to output-voltage ratio is too high, even though current exceeds the peak value dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. See t_{ON_MIN} in the *Electrical Characteristics*. As a result, the compensation circuit reduces both peak and valley current. After a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Because on-time is fixed at the minimum value, this type of operation resembles that of a device using a COT control scheme. See Valley Current Mode Operation.

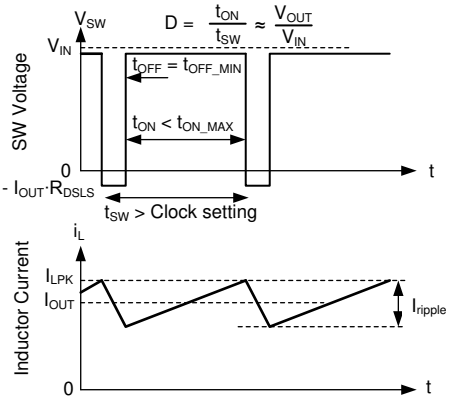


In valley control mode, the minimum inductor current is regulated, not peak inductor current.

Figure 7-10. Valley Current Mode Operation

7.4.3.5 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the needed duty factor. At a given clock frequency, duty factor is limited by minimum off-time. After this limit is reached, if clock frequency is maintained, output voltage falls. Instead of allowing the output voltage to drop, the TPSM8F7x20 extends on-time past the end of the clock cycle until the required peak inductor current is achieved. The clock can start a new cycle after peak inductor current is achieved or after a pre-determined maximum on-time, $t_{ON\text{-}MAX}$, of approximately 9µs passes. As a result, after the needed duty factor cannot be achieved at the selected clock frequency due to the existence of a minimum off-time, frequency drops to maintain regulation. If input voltage is low enough that the output voltage cannot be regulated even with an on-time of t_{ON_MAX}, output voltage drops to slightly below input voltage.



This image shows the switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by t_{ON_MAX}.

Figure 7-11. Dropout Waveforms

7.4.3.6 Recovery from Dropout

In some applications, input voltage can drop below the desired output voltage then recover to a higher value suddenly. With most regulators, the sudden increase in input voltage results in output voltage rising at a rate limited only by current limit until regulation is achieved. As input voltage reaches the desired output voltage,

there is overshoot due to wind up in the control loop. This overshoot can be large in applications that have small output capacitors and light loads. Also, large inrush currents can cause large fluctuations on the input line after the regulator starts regulating the output voltage. This typically requires less current than during this initial inrush.

The TPSM8F7x20 greatly reduces inrush current and overshoot. This is done by engaging the soft-start circuit whenever the input voltage suddenly rises, after dipping low enough to cause the output voltage to droop. To prevent this feature from accidentally engaging, output voltage must fall more than 1% to engage this feature. Also, this feature engages only if operating in dropout or current limit, preventing interference with normal transient response but allowing several percent overshoot while engaging. If output voltage is very close to the desired level, overshoot is reduced by inductor current not having time to rise to a high level before regulation starts.

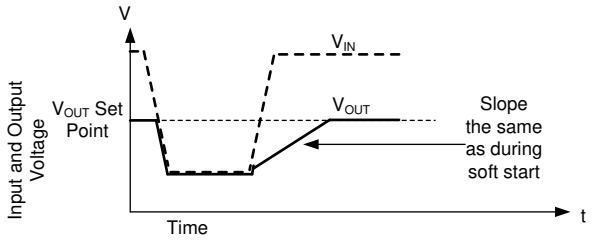


Figure 7-12. VOUT Overshoot Prevention when Recovering from Dropout

8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPSM8F7x20 synchronous buck module requires only a few external components to convert from a wide range of input and output voltages at an output current up to 4/6A per single phase output and up to 8/12A for two-phase outputs.

8.2 Typical Applications

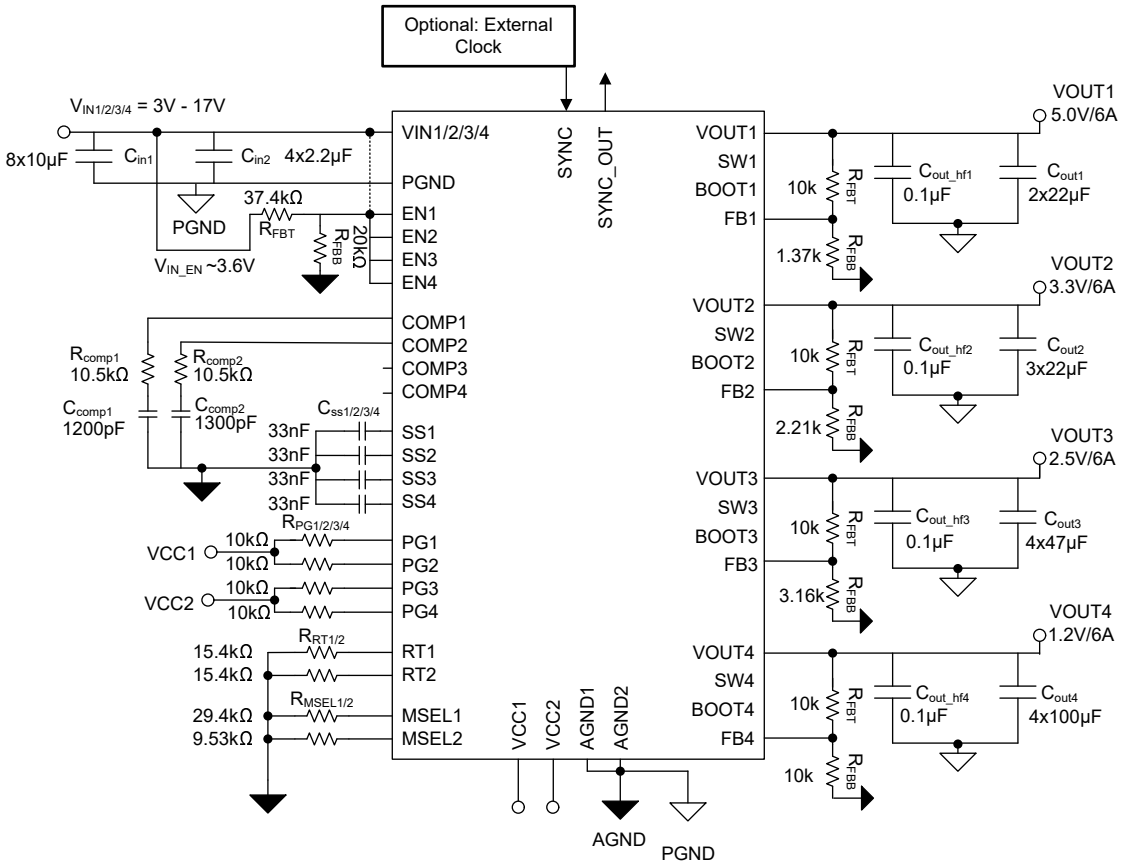


Figure 8-1. Four Output Application Schematic

8.2.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER		VALUE
Input Voltage	VIN	12V
Output Voltage	VOUT1	5V
	VOUT2	3.3V
	VOUT3	2.5V
	VOUT4	1.2V
Maximum Output Current	IOUT1/2/3/4	6A
Switching Frequency	f_{SW}	1MHz
Load Transient Regulation	VOUT3/4 Load profile: 1A to 4A, 1A/µs.	±4% of VOUT
Soft-start time	All channels	1ms

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM8F7x20 module with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Module Operating Area

The TPSM8F7x20 offers a wide range of operating conditions and flexibility to the user. There are a few constraints to the operating area that must be considered:

- Minimum on-time ($t_{ON(min)}$): refers to the minimum controllable pulse width when SW is pulled high

$$t_{ON(min)} < \frac{V_{OUT}}{V_{IN} \times f_{SW}} \tag{9}$$

- Minimum off-time ($t_{OFF(min)}$): refers to the minimum low-side FET on time when SW is pulled low

$$t_{OFF(min)} < \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f_{SW}} \tag{10}$$

- Current limit and inductor current ripple: refer to Section 8.2.2.5

These constraints drive the switching frequency selection based on the desired output voltages selected on the module especially if a wide range of output voltages is desired or there is a restriction on the switching frequency.

8.2.2.3 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Lower switching frequency implies reduced switching losses, typically resulting in less power dissipated in the IC. Lower power dissipated in the IC results in higher system efficiency and a lower IC temperature. However, higher switching frequency allows the use of smaller output capacitors, hence, a more compact design.

In this design a 1MHz switching frequency is used, so RT is chosen to be 15.4kΩ. Note that on the quad module, both RT1 and RT2 are needed. If another switching frequency is desired, please refer to Section 7.3.6.

8.2.2.4 Setting the Output Voltage

The output regulation target can be programmed using an adjustable resistor divider network. The divider network is comprised of the top and bottom feedback resistors, R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage at the internal error amplifier input equal to the internal reference voltage, V_{FB} = 0.6V. The total resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Lower resistance values reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R_{FBT} is around 25kΩ with a maximum value of 1MΩ. Refer to Equation 4 to calculate exact values of the feedback divider. Use divider resistors with 1% tolerance or better.

For this design the following feedback dividers are used to generate four different output voltages.

Table 8-2. Resistor Divider Selection for VOUT

OUTPUT	TARGET V_{OUT}(V)	R_{FBT}(kΩ)	R_{FBB}(kΩ)
VOUT1	5.0	10.0	1.37
VOUT2	3.3	10.0	2.21
VOUT3	2.5	10.0	3.16

Table 8-2. Resistor Divider Selection for VOUT (continued)

OUTPUT	TARGET V_{OUT}(V)	R_{FBT}(kΩ)	R_{FBB}(kΩ)
VOUT4	1.2	10.0	10.0

8.2.2.5 Integrated Inductor Considerations

The TPSM8F7x20 module has an integrated inductor with a fixed inductance of 0.68µH for the TPSM8F7620 and 1µH for the TPSM8F7420. Inductor current ripple in a buck converter is given by Equation 11 and ripple current must be accounted for in the design process. The inductor ripple current must be sufficiently small so that the high-side peak current limit and the low-side negative current limits are not tripped. Half of the inductor current ripple needs to be greater than the low-side negative current limit and less than the high-side peak current limit minus DC load current. The RT pin can be used to set the switching frequency of the buck module so that the inductor ripple current is sufficiently small for the desired VIN and VOUT.

$$\frac{\Delta i_L}{\Delta t} = \frac{V_{IN} \times D}{L \times f_{SW}} \tag{11}$$

8.2.2.6 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 10µF ceramic capacitance is required at each VINx/ground pin pair of the TPSM8F7x20. Use 2x 10µF ceramic capacitance or more for better EMI performance. This must be rated for at least the maximum input voltage that the application requires. Having twice the maximum input voltage is preferred for reducing DC bias derating. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients.

Often, using an electrolytic capacitor on the input in parallel with the ceramics is desirable. This action is especially true if long leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help dampen ringing on the input supply caused by the inductance of the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 13. The maximum input ripple occurs when operating nearest to 50% duty cycle. Using the nominal design example values of $I_{OUT(MAX)}$ = 6A, C_{IN} = 10µF, and f_{SW} = 1000kHz, the input voltage ripple with the 12V is targeted to be kept under 150mV. Be sure to include DC bias derating on the input capacitors. For the selected input capacitors the capacitance is down 70% from the nominal value at a 12V input.

Due to the power path routing of the quad module where VIN2 and VIN3 are not accessible from the outer edge of the package, TI recommends placing additional decoupling capacitors directly underneath the module on the bottom layer. In this design, 4x2.2µF capacitors are used to provide an additional decoupling to the input noise and ripple.

The input capacitors must also have a ripple current rating greater than the maximum RMS input current. The RMS input current can be calculated using Equation 12.

Table 8-3. C_{IN} Calculation Table

OUTPUT	$C_{IN(MIN)}$(µF)	C_{IN} Selected
VOUT1	5.8	2x10µF
VOUT2	4.8	2x10µF
VOUT3	4.0	2x10µF
VOUT4	2.2	2x10µF

$$I_{CINRMS} = I_{OUT} \times \sqrt{\frac{(V_{INMIN} - V_{OUT})}{V_{INMIN}} \times \frac{V_{OUT}}{V_{INMIN}}} \tag{12}$$

$$\Delta V_{IN} = \frac{I_{OUTMAX} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}}}{C_{IN} \times fsw} \quad (13)$$

8.2.2.7 Soft-Start Capacitor

The soft-start capacitor can be calculated from a target soft-start time.

$$C_{SS} = t_{SS} \times \frac{I_{SS(R)}}{V_{FB}} \quad (14)$$

$$C_{SS} = 1ms \times \frac{21\mu A}{0.6V} = 35nF \quad (15)$$

So, a 0.033µF capacitor is chosen for this design. Note that 1ms soft-start time is considered a relatively fast startup and a longer soft-start time can be selected to further limit inrush current if that is of concern.

8.2.2.8 VCC and BOOT Capacitors

The TPSM8F7x20 has integrated VCC and BOOT capacitors. This is designed to save the user time, board space, and reduce layout mistakes. No additional capacitors are needed on the VCC and BOOT pins.

8.2.2.9 Output Capacitor Selection

The output capacitors are selected to meet the output voltage ripple and load transient performance. The output capacitor for this design is selected as the worst case capacitance needed to meet both transients requirements and output voltage ripple. C_{OUT} can be calculated such that the output impedance is sufficiently low to meet load transient requirements. The impedance of C_{OUT} at the crossover frequency (f_{co}) is a good estimate of the maximum output impedance. The output impedance shows how much voltage deviation occurs for a given load step.

$$|Z_{OUT}| = \frac{\Delta V_{OUT}}{\Delta I_{step}} \quad (16)$$

Where

- ΔV_{OUT} is the undershoot or overshoot from the load step. Typically a percentage of V_{OUT}.
- ΔI_{step} is the change in load current during the transient.

Then C_{OUT} can be calculated from the following formula.

$$C_{OUT} = \frac{1}{2 \times \pi \times f_{co} \times |Z_{OUT}|} \quad (17)$$

Next, the output voltage ripple requirement is used to calculate the output capacitance. In this case, all ceramic output capacitors are used so the ESR ripple can be neglected.

$$C_{OUT} = \frac{\Delta i_{L\_ripple}}{8 \times f_{SW} \times \Delta V_{OUT\_ripple}} \quad (18)$$

The maximum of the two C_{OUT} values calculated in this section are used to meet both ripple and load transient performance targets.

8.2.2.10 Compensation Selection

There are two options for compensating the control loop when designing with TPSM8F7x20. External compensation on the COMP pin provides the most configurability, however there are also two internal compensation options to save board space and reduce BOM count. Internal compensation 1 is a higher gain setting and is targeted for better transient performance. Internal compensation 2 has a lower gain setting and is targeted for minimal output capacitance while maintaining stability.

The compensation components R_{COMP} and C_{COMP} that form the Type-II compensator can be calculated by analysis of the voltage loop gain and simplified into equations below. The three equations below assume base units for all variables in the equation.

$$F_M = \frac{1}{T_S \times \left(M_a + \frac{\frac{V_{IN}}{2} - V_{OUT}}{L} \right)} \tag{19}$$

$$R_{COMP} = \frac{\frac{R_f}{N} \times 2 \times \pi \times f_{co}}{\left(\frac{R_{FB\_B}}{R_{FB\_B} + R_{FB\_T}} \right) \times GM_{MAX} \times \left(\frac{V_{IN} \times F_M}{\frac{L \times I_{OUT}}{V_{OUT}} + C \times V_{IN} \times F_M} \right)} \tag{20}$$

$$C_{COMP} = \frac{\tan\left(65° + \tan^{-1}\left(\frac{f_{co}}{\left(\frac{I_{OUT}}{2 \times \pi \times V_{OUT} \times C} \right) \times \left(1 + \frac{V_{OUT} \times C \times F_m \times V_{IN}}{I_{OUT} \times L} \right)} \right) \right)}{2 \times \pi \times R_{COMP} \times f_{co}} \tag{21}$$

Table 8-4. Control Loop Variables

Device	R_f
TPSM8F7620	0.1095
TPSM8F7420	0.1405

Where

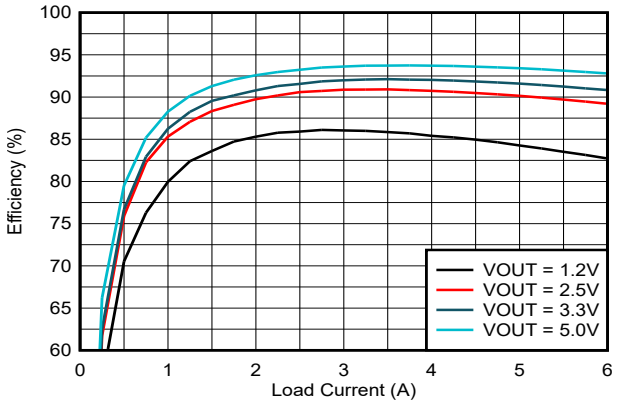
- f_{co} is the desired crossover frequency which is recommended to be kept less than 100kHz.
- M_a is the slope compensation ramp defined in Section 7.3.10
- R_f is the current sense to COMP voltage scaling factor
- N is the number of phases in parallel

When internal compensation is selected, R_{COMP} is internally set so the R_{COMP} equation can be resolved to calculate C_{OUT} based on desired crossover frequency.

Table 8-5. Internal and External Compensation Parameters

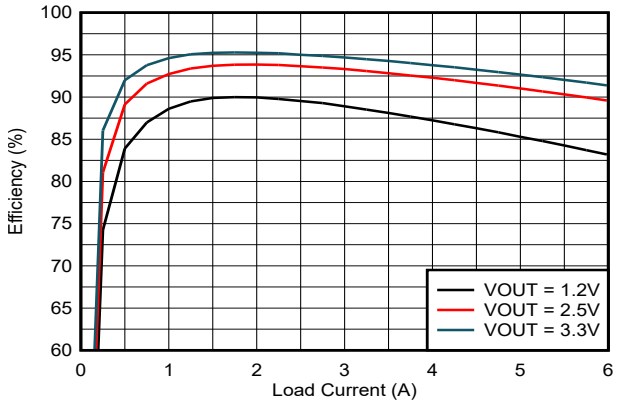
MSEL COMPx SETTING	TYPICAL GM (µS)	R_{COMP}(MΩ)	C_{COMP}(pF)
External	1000	External	External
Internal 1	12	1.4	20
Internal 2	12	0.4	20

8.2.3 Application Curves



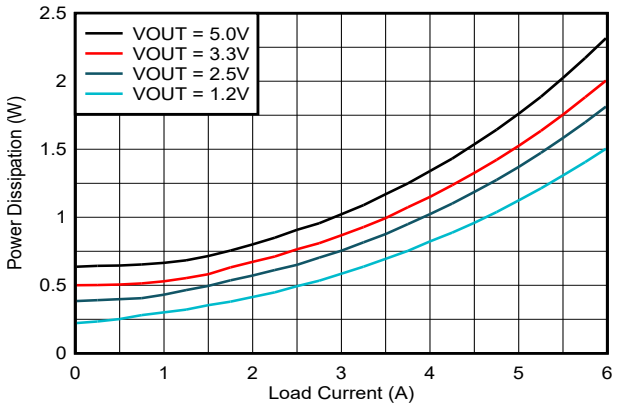
f_{SW} = 1MHz V_{IN}= 12V
TPSM8F7620

Figure 8-2. Efficiency vs Output Current



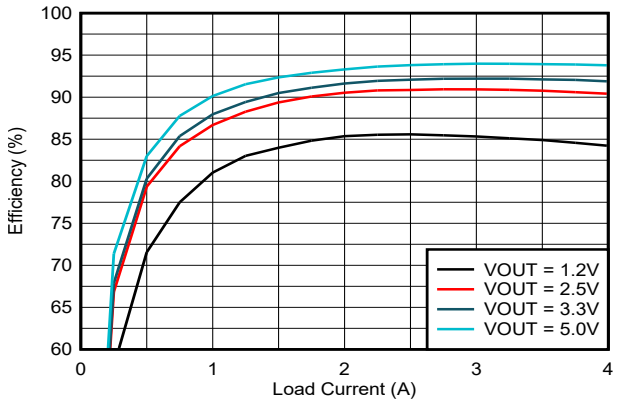
f_{SW} = 1MHz V_{IN}= 5V
TPSM8F7620

Figure 8-3. Efficiency vs Output Current



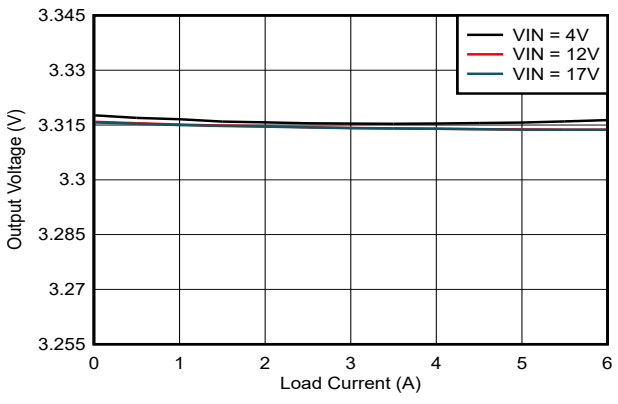
f_{SW} = 1MHz V_{IN}= 12V
TPSM8F7620

Figure 8-4. Power Dissipation



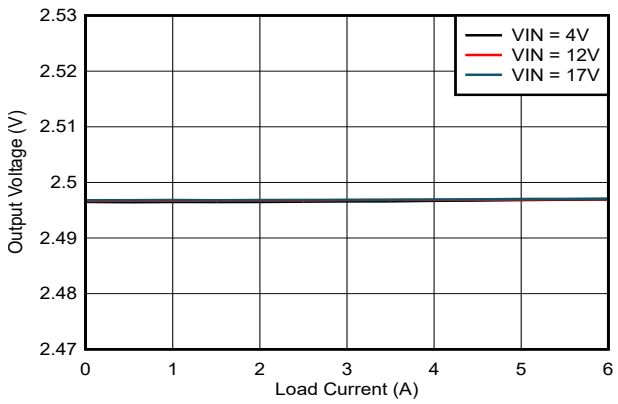
f_{SW} = 1MHz V_{IN}= 12V
TPSM8F7420

Figure 8-5. Efficiency vs Output Current



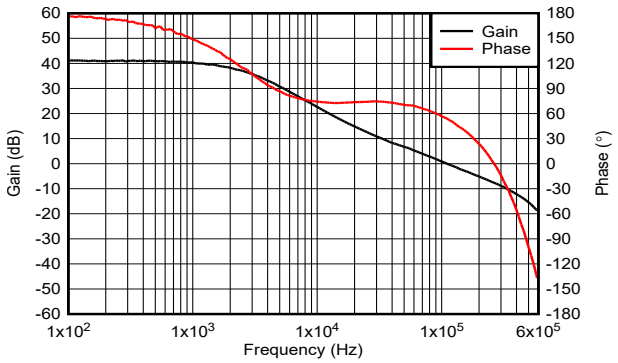
f_{SW} = 1MHz External Compensation
TPSM8F7620
V_{OUT}= 3.3V Referenced to AGND

Figure 8-6. Load Regulation



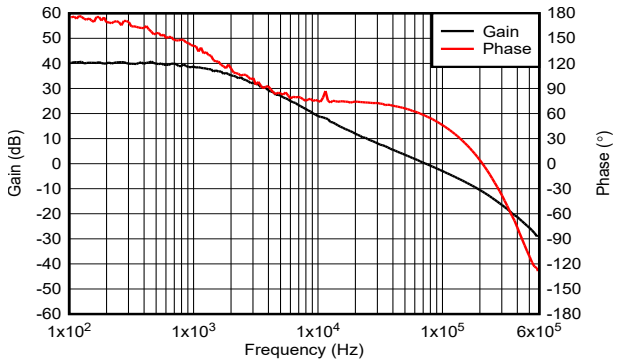
f_{SW} = 1MHz Internal Compensation
TPSM8F7620
V_{OUT}= 2.5V Referenced to AGND

Figure 8-7. Load Regulation



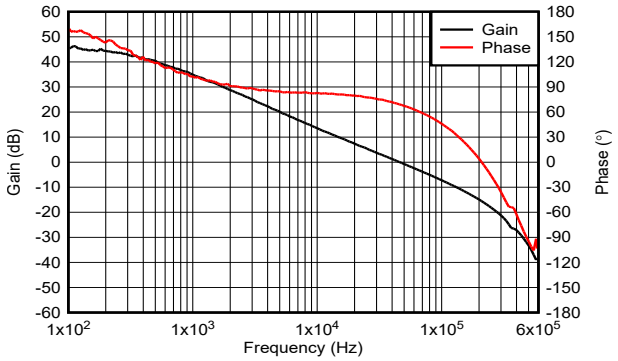
V_{IN}= 12V V_{OUT}= 5V I_{OUT}= 3A
f_{SW} = 1MHz TPSM8F7620

Figure 8-8. Voltage Loop Bode Plot VOUT1



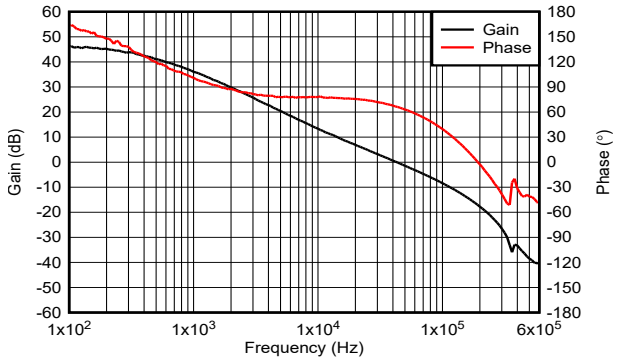
V_{IN}= 12V V_{OUT}= 3.3V I_{OUT}= 3A
f_{SW} = 1MHz TPSM8F7620

Figure 8-9. Voltage Loop Bode Plot VOUT2



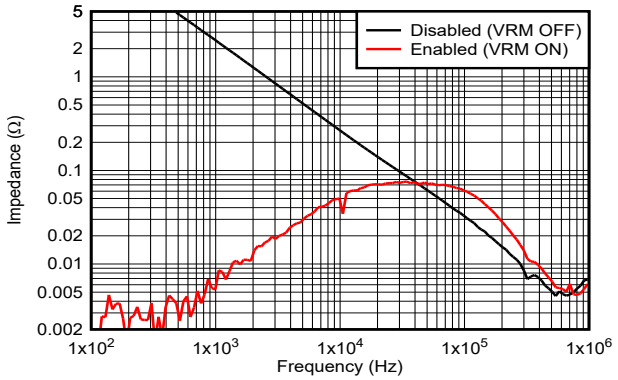
V_{IN}= 12V V_{OUT}= 2.5V I_{OUT}= 6A
f_{SW} = 1MHz TPSM8F7620

Figure 8-10. Voltage Loop Bode Plot VOUT3



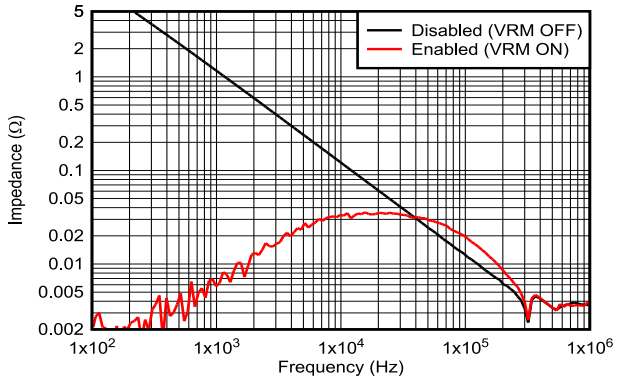
V_{IN}= 12V V_{OUT}= 1.2V I_{OUT}= 6A
f_{SW} = 1MHz TPSM8F7620

Figure 8-11. Voltage Loop Bode Plot VOUT4



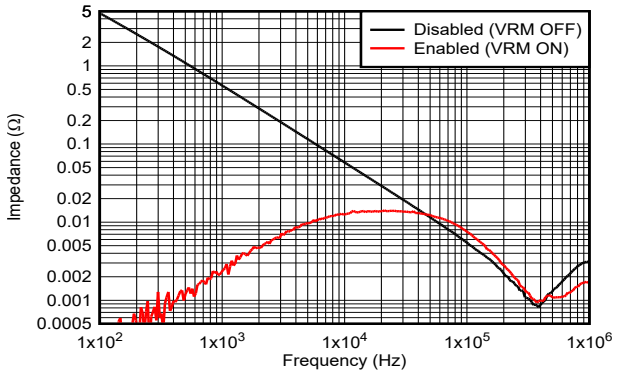
V_{IN}= 12V V_{OUT}= 3.3V I_{OUT} = 6A
f_{SW} = 1MHz TPSM8F7620

Figure 8-12. VOUT2 Output Impedance



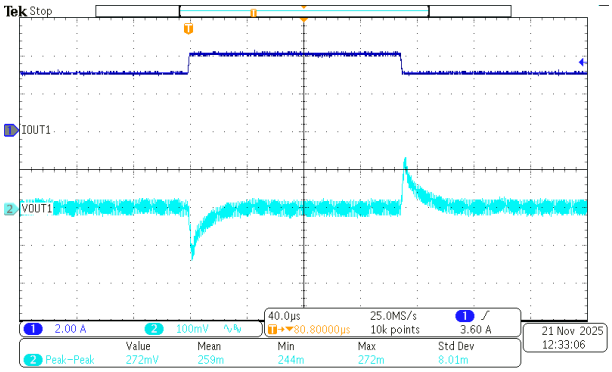
V_{IN}= 12V V_{OUT}= 2.5V I_{OUT} = 6A
f_{SW} = 1MHz TPSM8F7620

Figure 8-13. VOUT3 Output Impedance



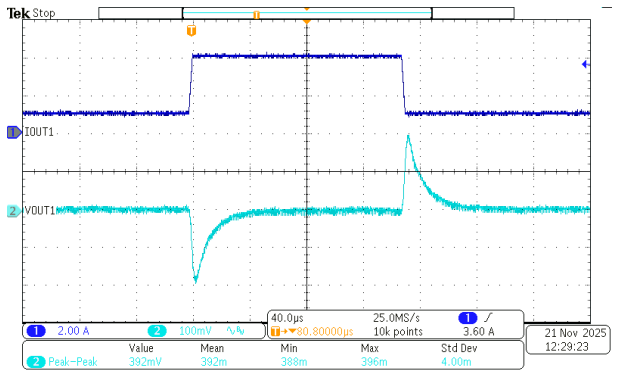
V_{IN}= 12V V_{OUT}= 1.2V I_{OUT} = 6A
f_{SW} = 1MHz TPSM8F7620

Figure 8-14. VOUT4 Output Impedance



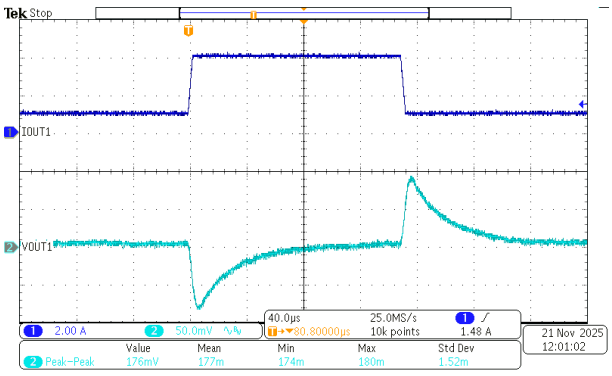
V_{IN}= 12V V_{OUT}= 5.0V I_{OUT} = 3A to 4A, 1A/µs
f_{SW} = 1MHz TPSM8F7620

Figure 8-15. VOUT1 Load Transient Response



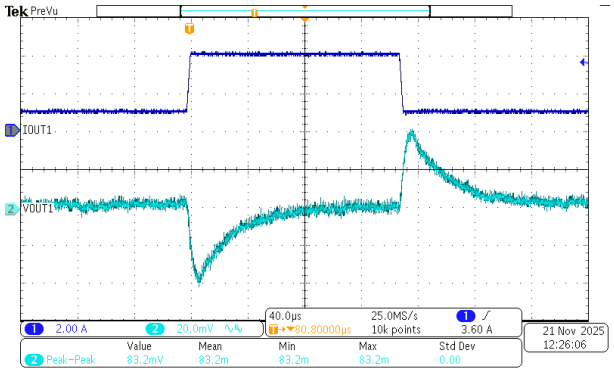
V_{IN}= 12V V_{OUT}= 3.3V I_{OUT} = 1A to 4A, 1A/µs
f_{SW} = 1MHz TPSM8F7620

Figure 8-16. VOUT2 Load Transient Response



V_{IN}= 12V V_{OUT}= 2.5V I_{OUT} = 1A to 4A, 1A/µs
f_{SW} = 1MHz TPSM8F7620

Figure 8-17. VOUT3 Load Transient Response



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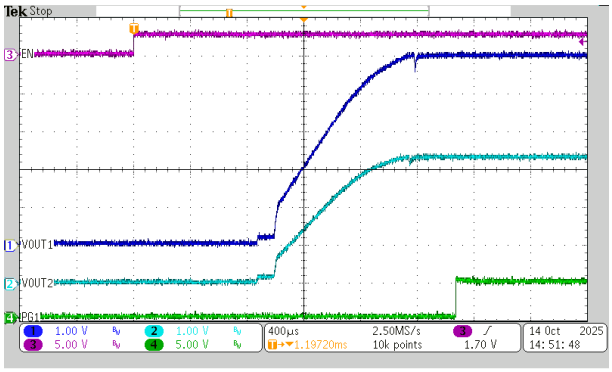
V_{IN}= 12V V_{OUT}= 1.2V I_{OUT} = 1A to 4A, 1A/µs
f_{SW} = 1MHz TPSM8F7620

Figure 8-18. VOUT4 Load Transient Response



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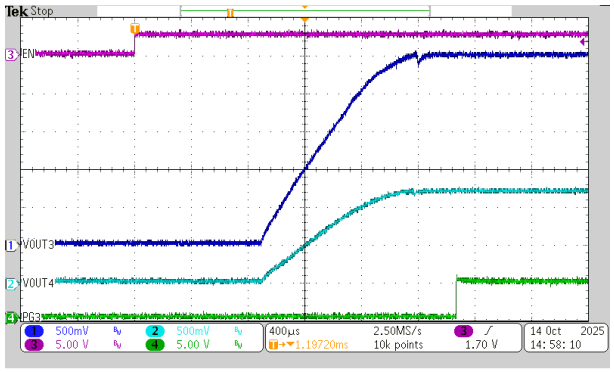
V_{IN} = 12V V_{OUT} = 5V & 3.3V I_{OUT} = 0A
f_{SW}=1MHz External Compensation

Figure 8-19. VOUT1 and VOUT2 Startup From EN



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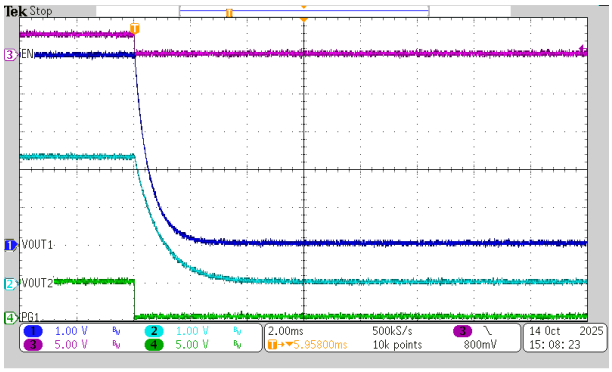
V_{IN} = 12V V_{OUT} = 2.5V & 1.2V I_{OUT} = 0A
f_{SW}=1MHz Internal Compensation

Figure 8-20. VOUT3 and VOUT4 Startup From EN



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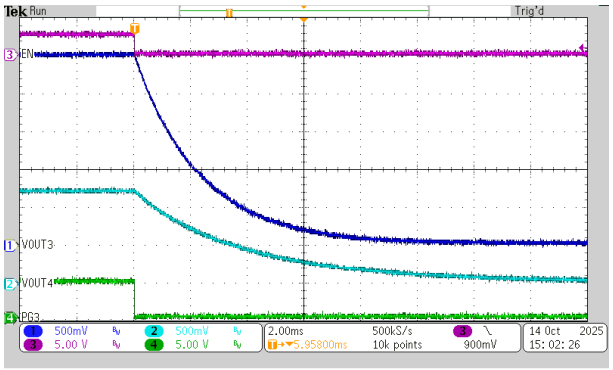
V_{IN} = 12V V_{OUT} = 5V & 3.3V I_{OUT} = 0A
f_{SW}=1MHz External Compensation

Figure 8-21. VOUT1 and VOUT2 Shutdown From EN



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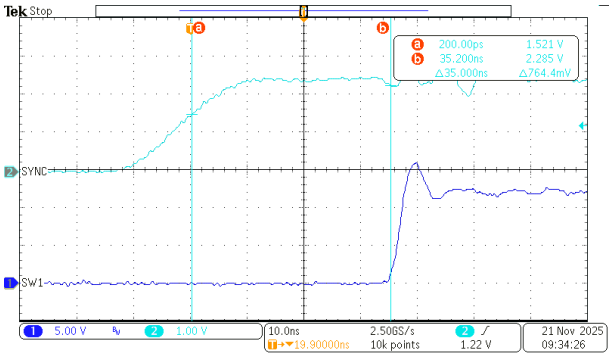
V_{IN} = 12V V_{OUT} = 2.5V & 1.2V I_{OUT} = 0A
f_{SW}=1MHz Internal Compensation

Figure 8-22. VOUT3 and VOUT4 Shutdown From EN



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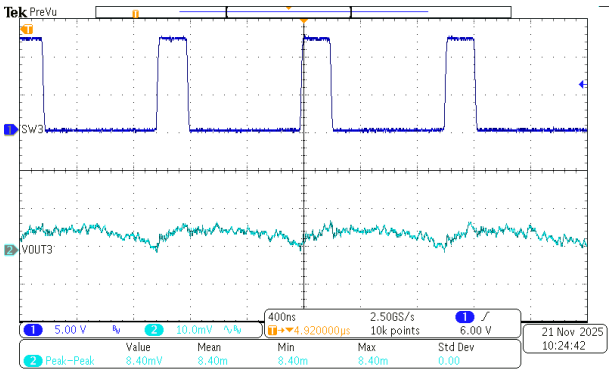
V_{IN} = 12V f_{SW}=1MHz

Figure 8-23. SYNC to SW1 Delay



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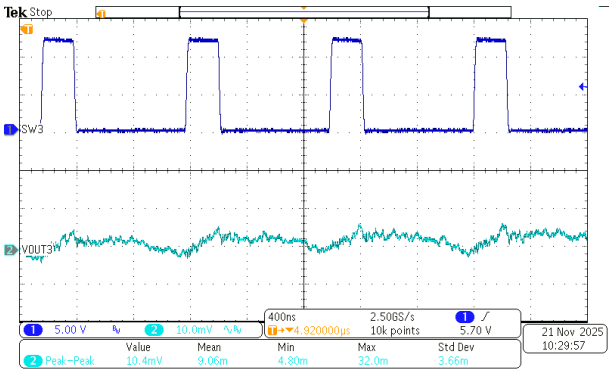
V_{IN} = 12V VOUT AC Coupled, 20MHz BW I_{OUT} = 0A
f_{SW}=1MHz TPSM8F7620

Figure 8-24. VOUT3 Steady-State Ripple



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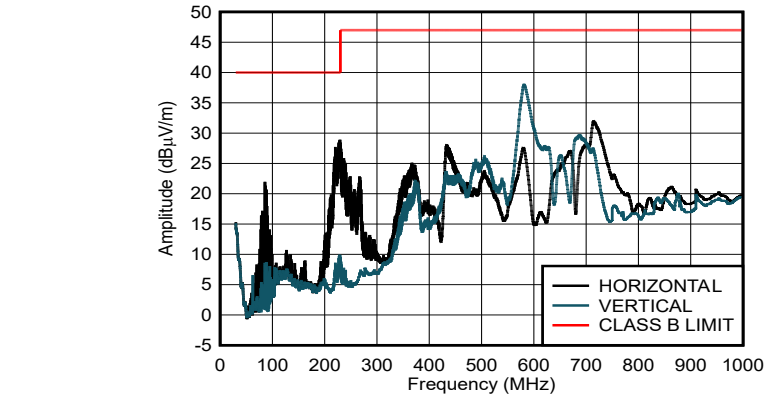
V_{IN} = 12V VOUT AC Coupled, 20MHz BW I_{OUT} = 6A
f_{SW}=1MHz TPSM8F7620

Figure 8-25. VOUT3 Steady-State Ripple



V_{IN} = 12V All channels enabled I_{OUT4} = 2.8A

Figure 8-26. Radiated Emissions Test CISPR32 Class B Limits

8.3 2-PH Application

Use the following design procedure to design multiphase outputs.

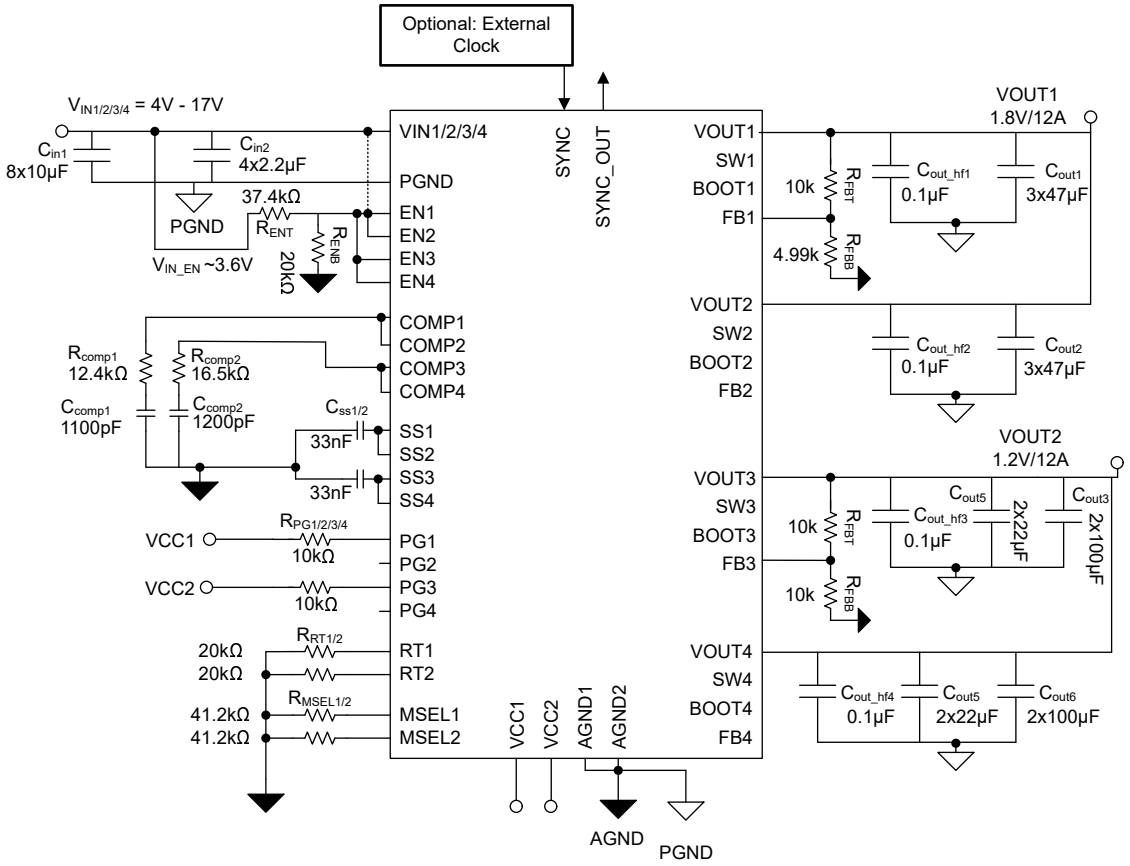


Figure 8-27. 2-PH + 2-PH Application Schematic

8.3.1 Design Requirements

Table 8-6. 2-PH Design Parameters

PARAMETER		VALUE
Input Voltage	VIN	12V
Output Voltage	VOUT1	1.8V
	VOUT2	1.2V
Maximum Output Current	IOUT1/2	12A
Switching Frequency	f_{SW}	750kHz
Load Transient Regulation	VOUT1/2 Load profile: 1A to 7A, 1A/µs.	±4% of VOUT
Soft-start time	All channels	1ms

8.3.2 Detailed Design Procedure

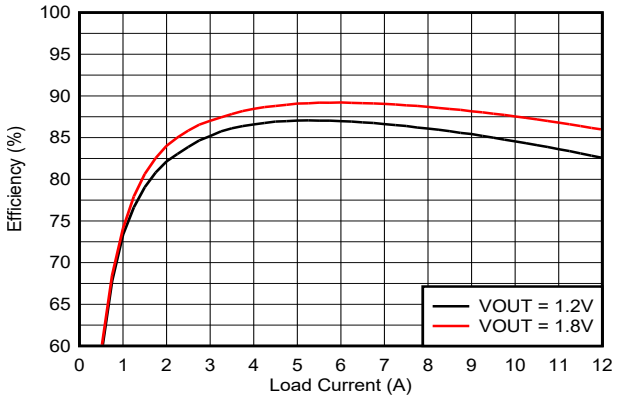
The design procedure for a 2-PH design using the TPSM8F7x20 is very similar to the 1-PH design procedure. The goal of this section is to describe the differences in the design procedure versus a single phase design as presented in Section 8.2

Following the guidelines in Section 7.3.4, the VOUT2, EN2, SS2, and COMP2 pins were tied to VOUT1, EN1, SS1, and COMP1 respectively. Because CH2 is a secondary channel, the user can leave PG and FB floating. The same connections were made between CH3 and CH4 because CH3 and CH4 form the second 2-PH output on the quad module. The soft-start capacitor is set the same way as a single phase design.

The switching frequency is selected the same way as a single phase design using the RT pin.

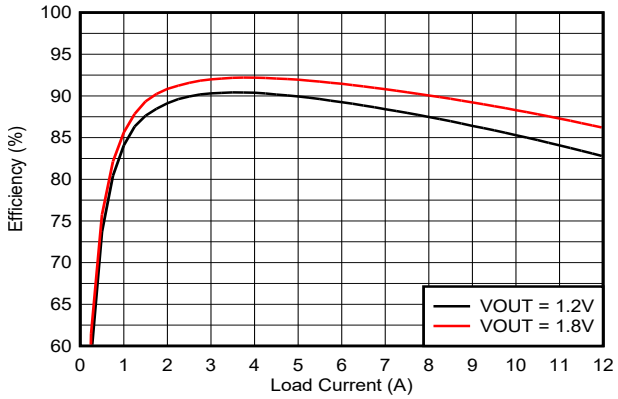
To compensate the multiphase control loop, use the same equations in Section 8.2.2.10 to find RCOMP and CCOMP. Note that there is a variable called N which represents the total number of phases in the stack and is set to 2 in the case of 2-PH output. For the variable "C" in the RCOMP and CCOMP equations, use the total output capacitance on the 2-PH output.

8.3.3 Application Curves 2-PH



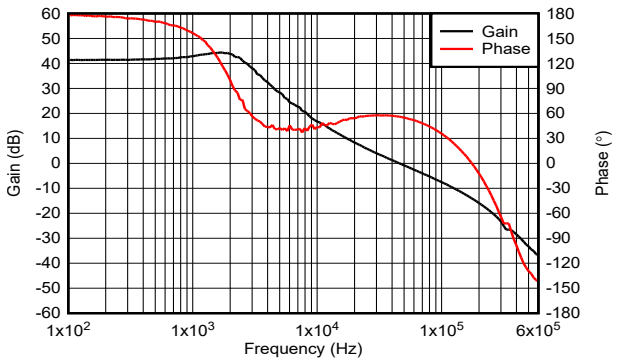
f_{SW} = 750kHz V_{IN}= 12V
TPSM8F7620

Figure 8-28. Efficiency vs Output Current



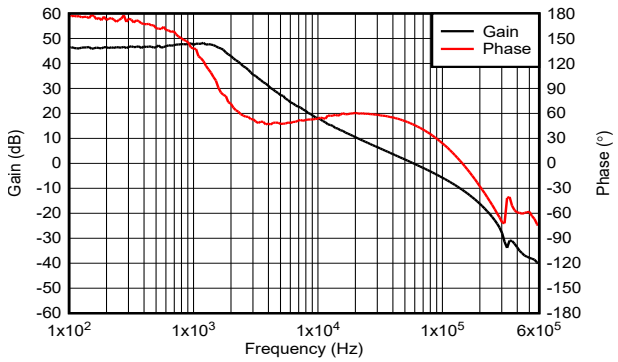
f_{SW} = 750kHz V_{IN}= 5V
TPSM8F7620

Figure 8-29. Efficiency vs Output Current



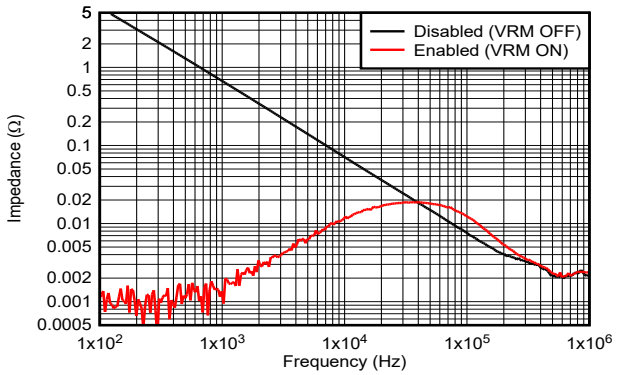
V_{IN}= 12V V_{OUT}= 1.8V I_{OUT}= 6A
f_{SW} = 750kHz TPSM8F7620

Figure 8-30. Voltage Loop Bode Plot VOUT1



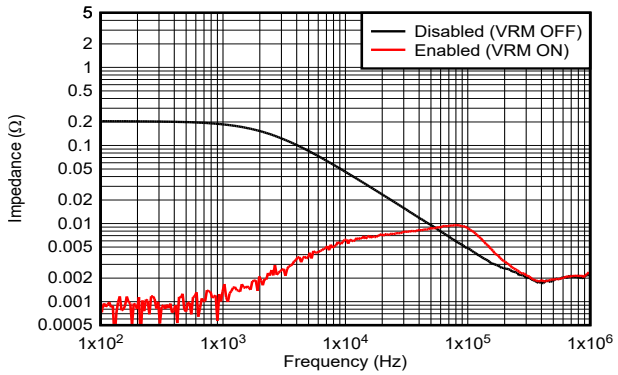
V_{IN}= 12V V_{OUT}= 1.2V I_{OUT}= 6A
f_{SW} = 750kHz TPSM8F7620

Figure 8-31. Voltage Loop Bode Plot VOUT2



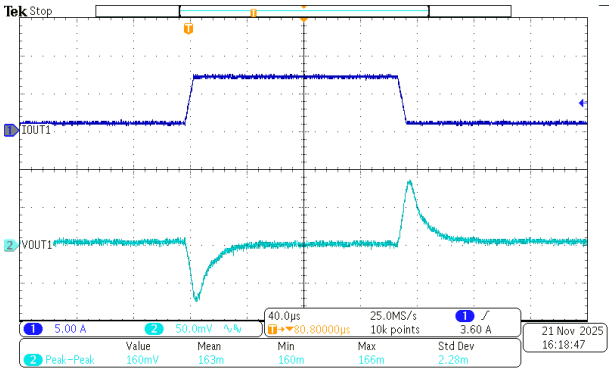
V_{IN} = 12V V_{OUT} = 1.8V I_{OUT} = 12A
f_{SW} = 750kHz TPSM8F7620

Figure 8-32. VOUT1 Output Impedance



V_{IN} = 12V V_{OUT} = 1.2V I_{OUT} = 6A
f_{SW} = 750kHz f_{SW}= 0.2Ω Load

Figure 8-33. VOUT2 Output Impedance



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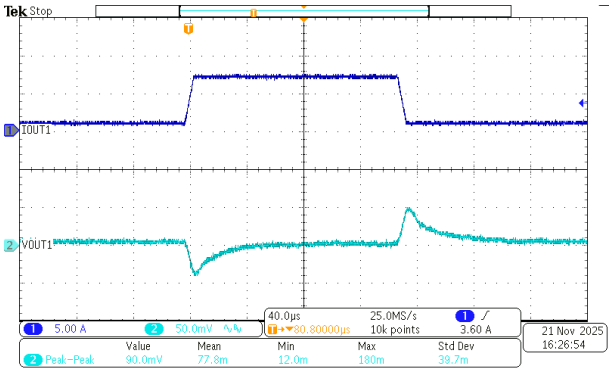
V_{IN} = 12V V_{OUT} = 1.8V I_{OUT} = 1A to 7A, 1A/µs

Figure 8-34. VOUT1 Load Transient



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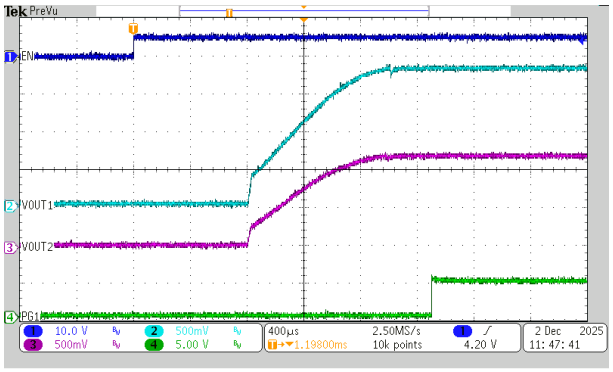
V_{IN} = 12V V_{OUT} = 1.2V I_{OUT} = 1A to 7A, 1A/µs

Figure 8-35. VOUT2 Load Transient



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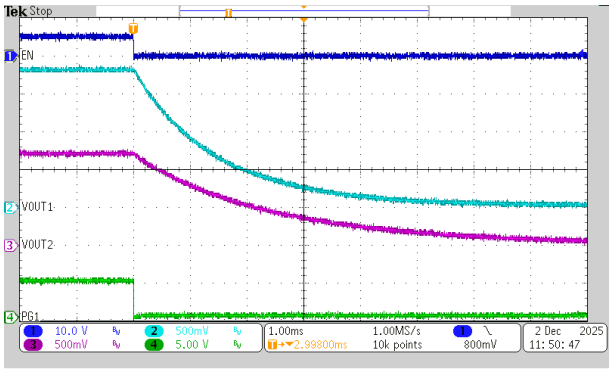
V_{IN} = 12V V_{OUT} = 1.8V & 1.2V I_{OUT} = 0A
f_{SW} = 750kHz External Compensation

Figure 8-36. Startup From EN



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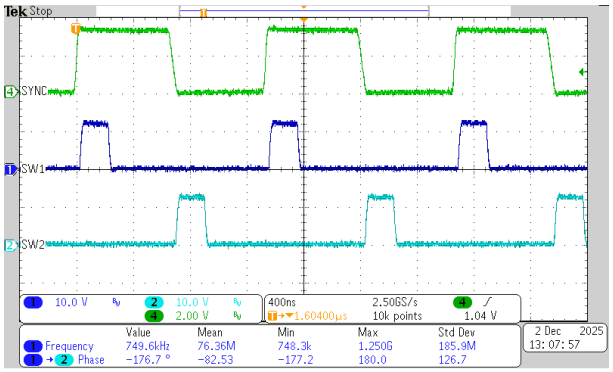
V_{IN} = 12V V_{OUT} = 1.8V & 1.2V I_{OUT} = 0A
f_{SW} = 750kHz External Compensation

Figure 8-37. Shutdown From EN



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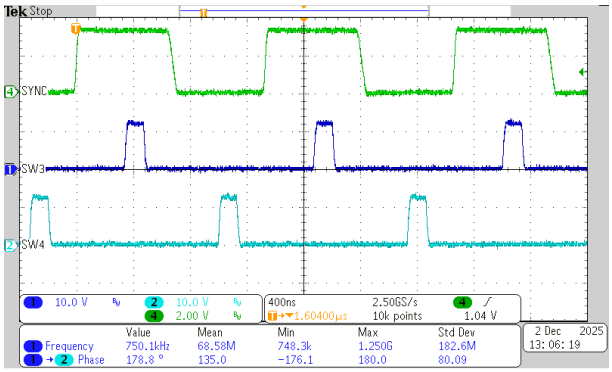
V_{IN} = 12V V_{OUT} = 1.8V I_{OUT} = 0A
f_{SYNC} = 750kHz

Figure 8-38. Phase Interleaving on CH1 and CH2



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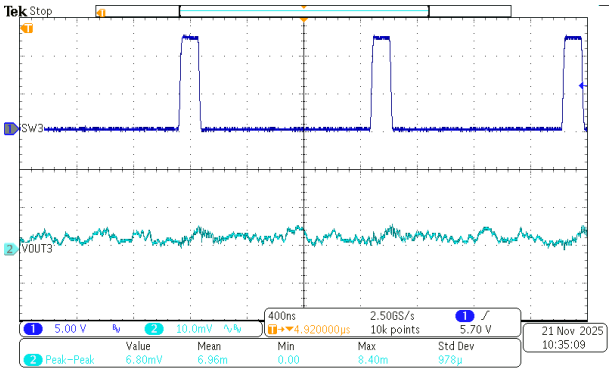
V_{IN} = 12V V_{OUT} = 1.2V I_{OUT} = 0A
f_{SYNC} = 750kHz

Figure 8-39. Phase Interleaving on CH3 and CH4



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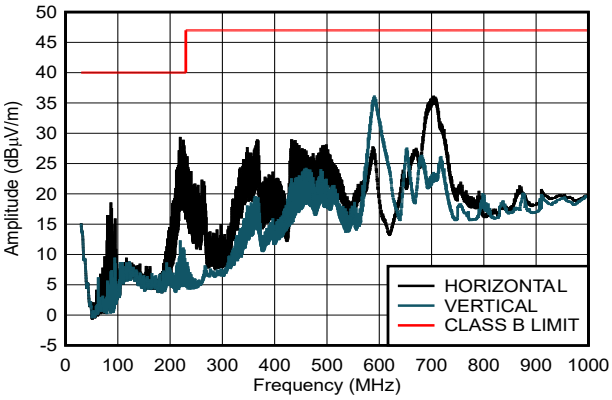
V_{IN} = 12V V_{OUT} = 1.2V I_{OUT} = 0A

Figure 8-40. VOUT2 Steady-State Ripple



V_{IN} = 12V All channels enabled I_{OUT2} = 6A

Figure 8-41. Radiated Emissions Test CISPR32 Class B Limits

8.4 Power Supply Recommendations

The TPSM8F7x20 buck module is designed to operate over a wide input voltage range of 4V to 17V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator circuit. Estimate the average input current with Equation 22.

$$I_{IN} = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \right) \quad (22)$$

where

- η is the efficiency.

If the module is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on module operation. More specifically, the parasitic inductance in combination with the low-ESR ceramic input capacitors form an under-damped resonant circuit, possibly resulting in instability or voltage transients each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the module is operating close to the minimum input voltage, this dip can cause false UVLO triggering and a system reset.

The best method to solve such issues is to reduce the distance from the input supply to the module and use an electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A capacitance in the range of 47µF to 100µF is typically sufficient to provide input parallel damping and helps hold the input voltage steady during large load transients. A typical ESR of 0.1Ω to 0.4Ω provides enough damping for most input circuit configurations.

8.5 Layout

Proper PCB design and layout is important in high-current, fast-switching module circuits (with high internal voltage and current slew rates) to achieve reliable device operation and design robustness this primarily affects the performance of EMI and thermal dissipation of the device on the board.

8.5.1 Layout Guidelines

The following list summarizes the essential guidelines for PCB layout and component placement to optimize DC/DC module performance, including thermals and EMI signature. *Layout Example* shows a recommended PCB layout for the TPSM8F7x20 with optimized placement and routing of the power-stage and small-signal components.

- *Place input capacitors as close as possible to the VIN pins.* The high-frequency currents are decoupled by 0.1µF capacitors integrated on the module.
  - Use low-ESR ceramic capacitors with X7R or X7S dielectric.
  - Ground return paths for the input capacitors must consist of localized top-side planes that connect to the PGND pads under the module.
  - The VIN2 and VIN3 pins are in the middle of the package and is required to route VIN on an inner layer and optional to add 2.2µF VIN capacitors on the bottom or opposite side of the PCB.
- *Place output capacitors as close as possible to the VOUT pins.* A similar dual and symmetrical arrangement of the output capacitors enables lower ripple.
  - Ground return paths for the output capacitors must consist of localized top-side planes that connect to the PGND pads under the module.
  - Even though the VOUT pins are connected internally, use a wide polygon plane on a lower PCB layer to connect these pins together and to the load, thus reducing conduction loss and thermal stress.
- *Keep the FB trace as short as possible by placing the feedback resistors close to the FB pin.* Reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. FB is the input to the voltage-loop error amplifier and represents a high-impedance node

sensitive to noise. Route a trace from the upper feedback resistor to the required point of output voltage regulation.
- *Use a solid ground plane on the PCB layer directly below the top layer with the module.* This plane acts as a noise shield by minimizing the magnetic fields associated with the currents in the switching loops. Connect AGND to PGND in one location as shown in the example layout.
- *Provide enough PCB area for proper heat sinking.* Use sufficient copper area to achieve a low thermal impedance commensurate with the maximum load current and ambient temperature conditions. Provide adequate heat sinking for the TPSM8F7x20 to keep the junction temperature below 125°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of vias under the PGND, VIN, and VOUT pads of the module for effective heat sinking and electrical conduction.
- *Use SMD landing pads for VIN, PGND, and VOUT or any other pins that connect to a copper pour.* All other I/O and signal pins must use NSMD as specified in the Example Board Layout drawing.
- *Dogbone or Via-In-Pad escape routing can be used.*
- *Connect the AGND plane to PGND in one location to prevent ground loops.* Also, connect AGND1 to AGND2 with a low impedance connection on the same AGND copper pour.

8.5.1.1 Thermal Design and Layout

For a DC/DC module to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The TPSM8F7x20 module is available in a small 7mm × 12mm 112-pin BGA 6.4mm × 7mm 56-pin FCBGA package to cover a range of application requirements. The *Thermal Information* table summarizes the thermal metrics of this package with related detail provided by the *Semiconductor and IC Package Thermal Metrics* application note.

The 112-pin BGA package offers a means of removing heat through the BGA balls. This design allows a significant improvement in heat sinking. Designing the PCB with thermal lands, thermal vias, and one or more grounded planes is imperative to complete the heat removal subsystem. The exposed pads of the TPSM8F7x20 are soldered to the ground-connected copper lands on the PCB directly underneath the device package, reducing the thermal resistance to a very low value.

The TPSM8F7x20 uses an overmolded package construction which can be interfaced to a heat sink or cold plate for better thermal dissipation. This is an effective method of increasing the thermal SOA of the device and allow for less derating of the output current due to thermal limitations.

Preferably, use a six-layer board with at least 1oz copper thickness for all layers to provide low impedance, proper shielding and lower thermal resistance. Numerous vias connected from the thermal lands to the internal and solder-side ground planes are vital to promote heat transfer. In a multilayer PCB stack-up, a solid ground plane is typically placed on the PCB layer below the power-stage components. Not only does this design provide a plane for the power-stage currents to flow, but the design also represents a thermally conductive path away from the heat-generating device.

8.5.2 Layout Example

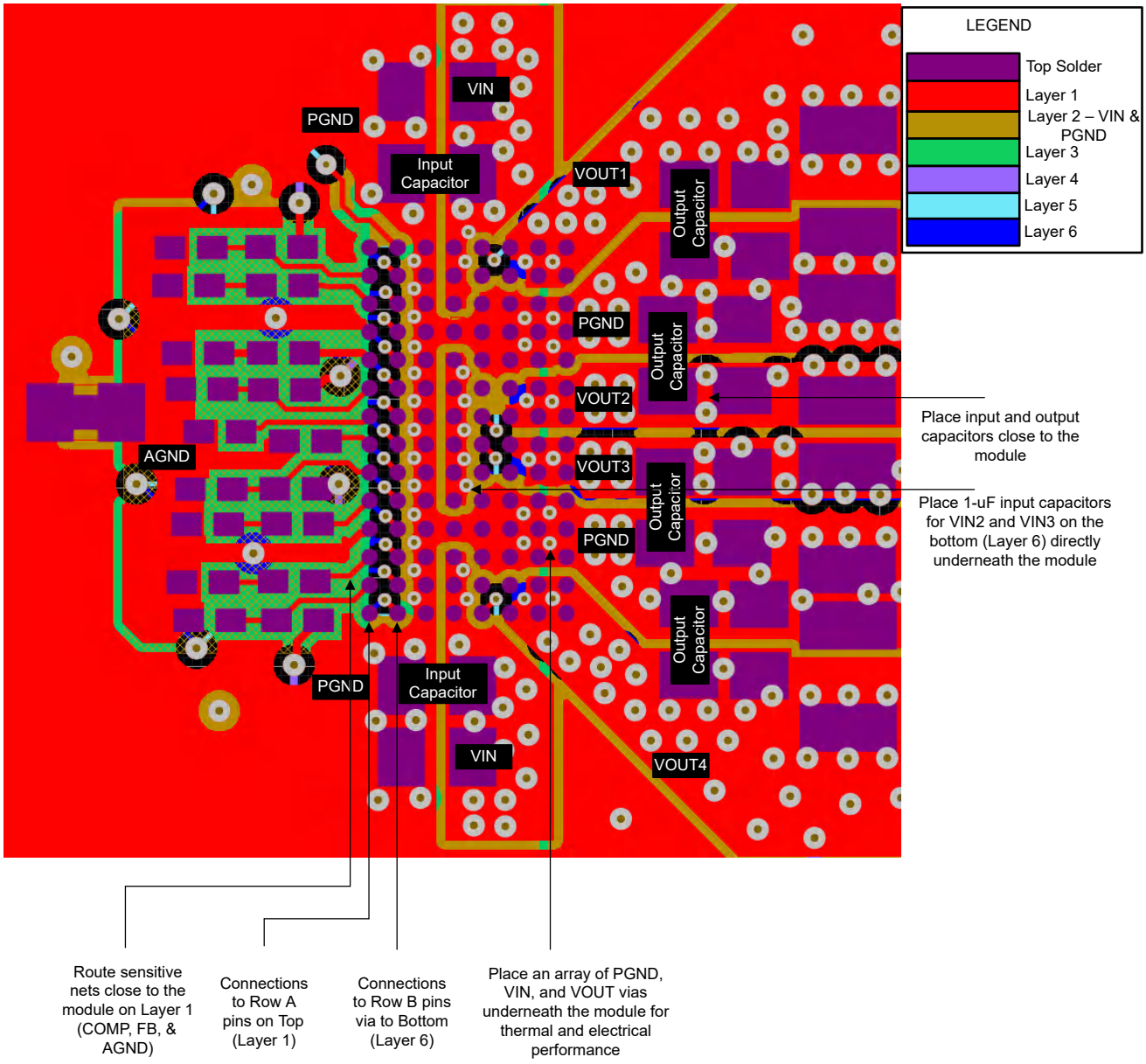


Figure 8-42. Typical Top Layer PCB Design

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.1.2 Development Support

For development support see the following:

- For TI's reference design library, visit the *TI Reference Design library*.
- For TI's WEBENCH Design Environment, visit the *WEBENCH® Design Center*.
- To design a low-EMI power supply, review TI's comprehensive *EMI Training Series*.
- To design an inverting buck-boost (IBB) regulator, visit *DC/DC inverting buck-boost modules*.
- TI Reference Designs:
  - *Multiple Output Power Solution For Kintex 7 Application*
  - *Space-optimized DC/DC Inverting Power Module Reference Design With Minimal BOM Count*
  - *3- To 11.5V_{IN}, –5V_{OUT}, 1.5A Inverting Power Module Reference Design For Small, Low-noise Systems*
- Technical Articles:
  - *Powering Medical Imaging Applications With DC/DC Buck Converters*
  - *How To Create A Programmable Output Inverting Buck-boost Regulator*

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM8F7x20 module with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Quick Reference Guide to TI Buck Switching DC/DC Application Notes* application note
- Texas Instruments, *Innovative DC/DC Power Modules* selection guide
- Texas Instruments, *Enabling Small, Cool and Quiet Power Modules with Enhanced HotRod™ QFN Package Technology* white paper
- Texas Instruments, *Benefits and Trade-offs of Various Power-Module Package Options* white paper
- Texas Instruments, *Simplify Low EMI Design with Power Modules* white paper
- Texas Instruments, *Power Modules for Lab Instrumentation* white paper
- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *Soldering Considerations for Power Modules* application note
- Texas Instruments, *Practical Thermal Design With DC/DC Power Modules* application note

- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application note
- Texas Instruments, *Using the TPSM53602/3/4 for Negative Output Inverting Buck-Boost Applications* application note
- Texas Instruments, *Method of Graphing Safe Operating Area (SOA) Curves in DC-DC Converter* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2025) to Revision A (December 2025)	Page
• Added WEBENCH links throughout the document	1
• Updated CDM specification to ANSI/ESDA/JEDEC JS-002	6

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM8F7420APG	Active	Production	FCCSP (APG) | 112	208 | JEDEC TRAY (5+1)	In-Work	NIAU	Level-3-260C-168 HR	-40 to 125	TM8F42
TPSM8F7620APG	Active	Production	FCCSP (APG) | 112	208 | JEDEC TRAY (5+1)	In-Work	NIAU	Level-3-260C-168 HR	-40 to 125	TM8F62

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

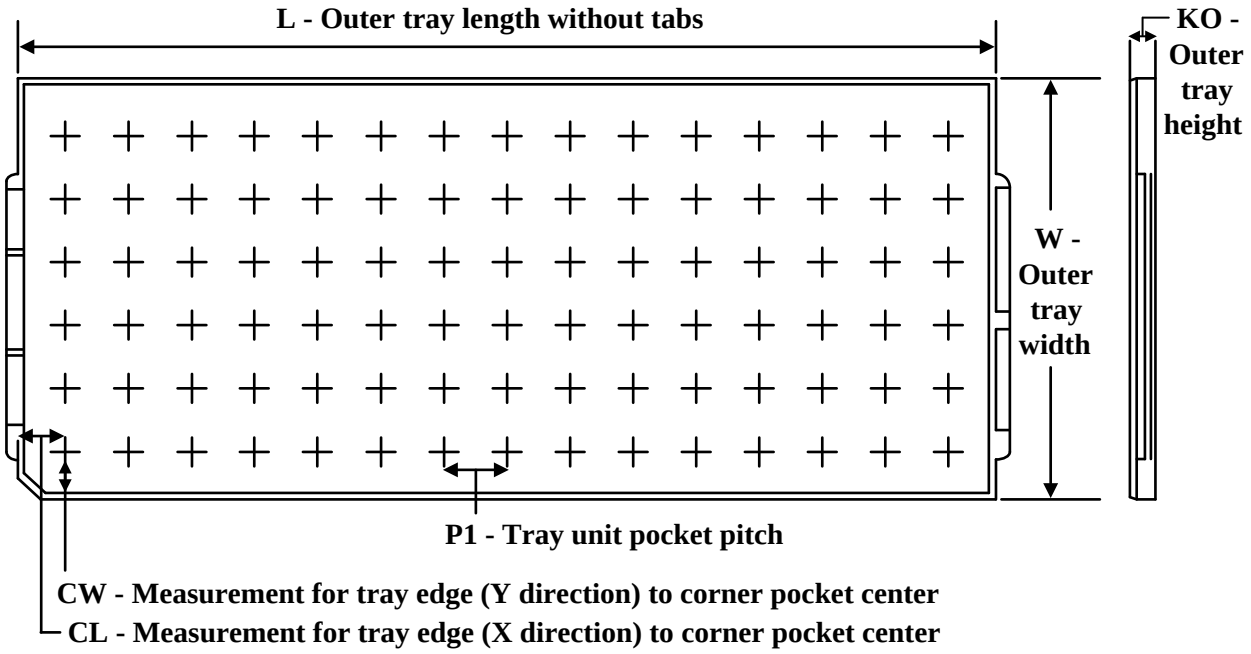
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY

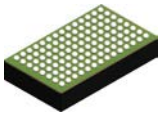


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TPSM8F7420APG	APG	FCCSP	112	208	8x26	150	315	135.9	7.62	16	10	11.95
TPSM8F7620APG	APG	FCCSP	112	208	8x26	150	315	135.9	7.62	16	10	11.95

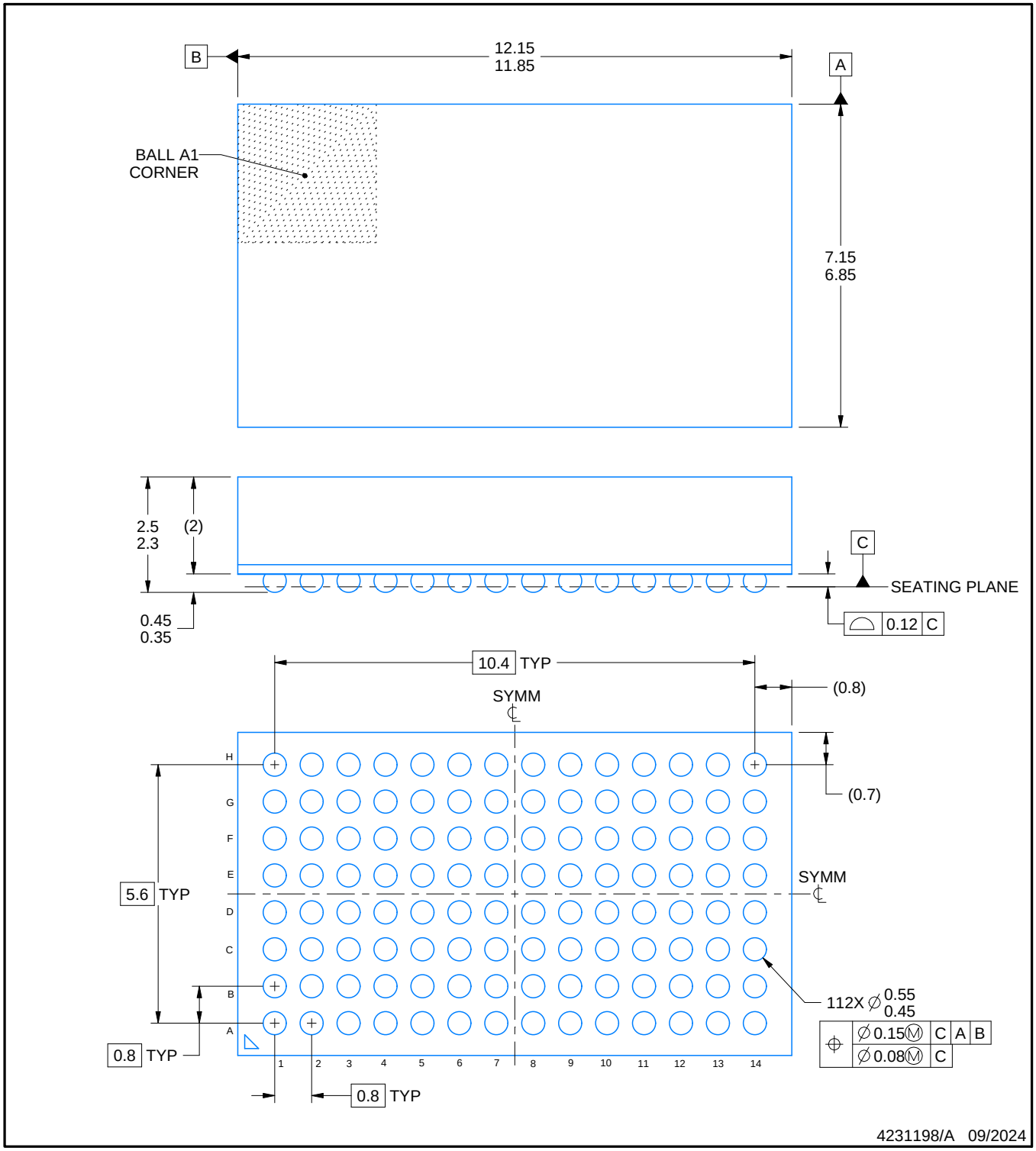
APG0112A



PACKAGE OUTLINE

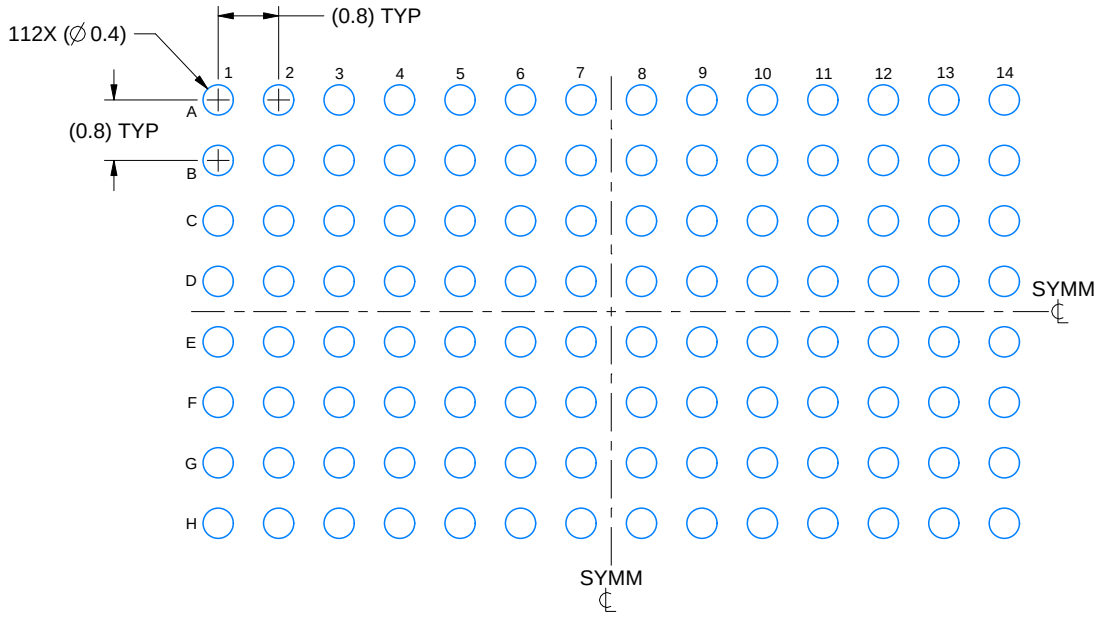
FCCSP - 2.5 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS
NOT TO SCALE

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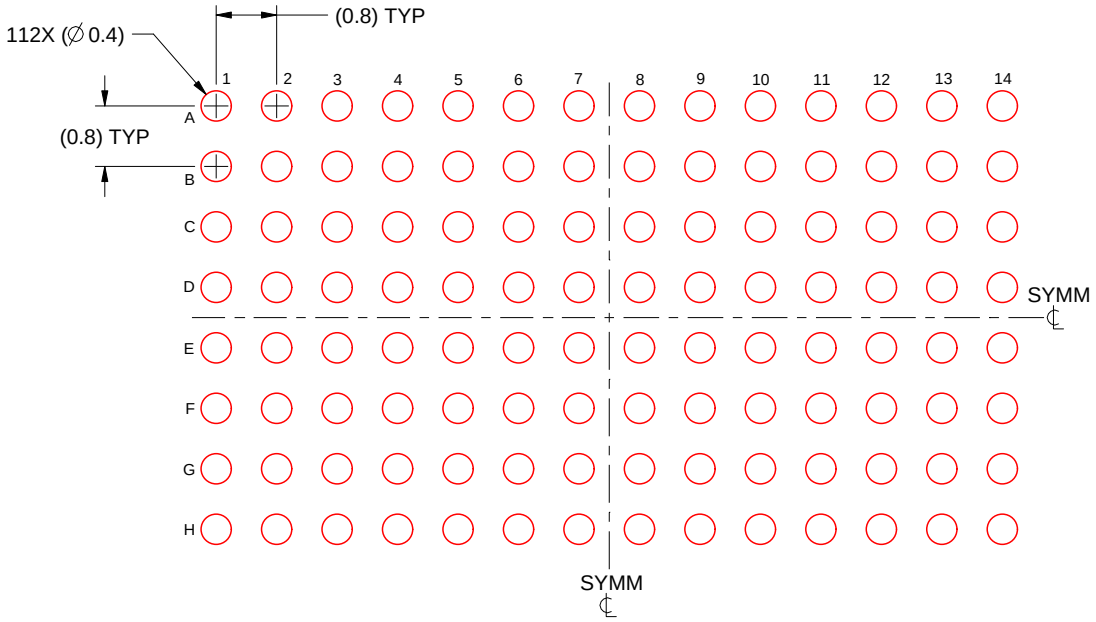
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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