TPUL1G513-Q1 Automotive Single Pin-Selectable Digitally Timed Retriggerable Monostable Multivibrator

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- 1% typical, 10% maximum pulse width variation
- Input glitch filter ignores spurious inputs
- Pre-configured digital timing - no external timing components required
- Three selectable pulse width options per orderable
- Default state (S0 = S1 = LOW) set by internal pull-down resistors (1MΩ)
- Wide operating range from 1.65V to 5.5V
- I/O clamp diodes protect from over- and under-voltage transients
- Schmitt-trigger architecture on all inputs

2 Applications

- Demodulate a digital Amplitude Shift Keying (ASK) signal
- Reset a system for a fixed period of time
- Generate a positive fixed-width digital pulse
- Detect a digital signal rising edge
- Detect a digital signal falling edge
- Debounce a switch

3 Description

The TPUL1G513-Q1 devices are fixed-width pulse generators. The output pulse width can be selected by setting pins S0 and S1. The TPUL1G513-Q1 devices feature rising edge (T) and falling edge ($\overline{T}$) triggers, as well as an asynchronous clear ($\overline{CLR}$) input. Applying a trigger while the output is active (retriggering) causes the output to remain active for one additional pulse width.

Package Information

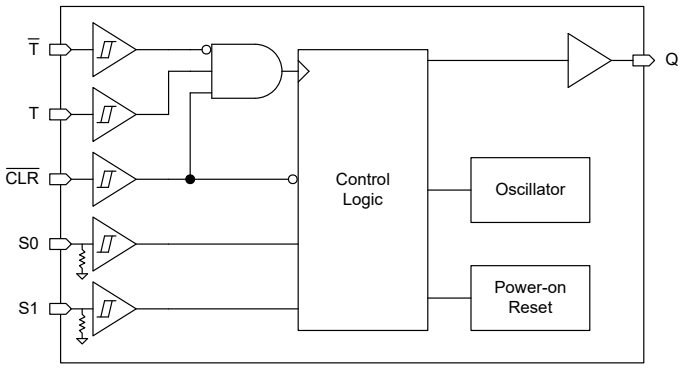
PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)	BODY SIZE(3)
TPUL1G513-Q1	DRL (SOT-5X3, 8)	2.1 × 1.6mm	2.1 × 1.6mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.

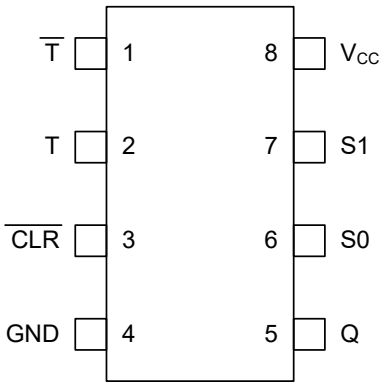
Table 3-1. Device Information

PART NUMBER	SELECTABLE PULSE WIDTH(1)		
	T1	T2(2)	T3
TPUL1G513**00**	1s	3s	6.8s
TPUL1G513**01**	10ms	30ms	68ms
TPUL1G513**02**	10µs	30µs	68µs

(1) Approximate values shown; see *Typical Characteristics* section for details
(2) Default value if S0, S1 are left disconnected



Functional block diagram



Pinout diagram

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....4
5.4 Thermal Information....5
5.5 Electrical Characteristics....5
5.6 Timing Characteristics....6
5.7 Switching Characteristics....8
5.8 Typical Characteristics....9
6 Parameter Measurement Information....11
7 Detailed Description....13
7.1 Overview....13
7.2 Functional Block Diagram....13
7.3 Feature Description....13
7.4 Device Functional Modes....16
8 Application and Implementation....17
8.1 Application Information....17
8.2 Typical Application - Edge Detector....17
8.3 Power Supply Recommendations....19
8.4 Layout....19
9 Device and Documentation Support....21
9.1 Documentation Support....21
9.2 Receiving Notification of Documentation Updates....21
9.3 Support Resources....21
9.4 Trademarks....21
9.5 Electrostatic Discharge Caution....21
9.6 Glossary....21
10 Revision History....21
11 Mechanical, Packaging, and Orderable Information....21

4 Pin Configuration and Functions

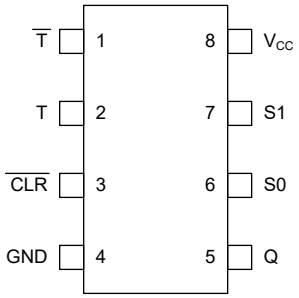


Figure 4-1. TPUL1G513-Q1 DRL Package (Top View)

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DRL NO.		
$\overline{T}$	1	I	Falling edge trigger input; T and $\overline{CLR}$ must be held HIGH
T	2	I	Rising edge trigger input; $\overline{T}$ must be held LOW and $\overline{CLR}$ must be held HIGH
$\overline{CLR}$	3	I	Asynchronous clear, active low; can also be used as a rising edge trigger input with T held HIGH and $\overline{T}$ held LOW
GND	4	G	Ground
Q	5	O	Output, active high
S0	6	I	Configuration input 0; includes internal 1MΩ pull-down resistor
S1	7	I	Configuration input 1; includes internal 1MΩ pull-down resistor
V_{CC}	8	P	Positive supply

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Digital input voltage range(2)		–0.5	V_{CC} + 0.5	V
V_O	Digital output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp diode current, continuous	V_I < -0.5V or V_I > V_{CC} + 0.5		±20	mA
	Input clamp diode current, pulsed 1µs	V_I < -0.5V or V_I > V_{CC} + 0.5		±200	mA
I_{OK}	Output clamp diode current, continuous	V_I < -0.5V or V_I > V_{CC} + 0.5		±20	mA
	Output clamp diode current, pulsed 1µs	V_I < -0.5V or V_I > V_{CC} + 0.5		±200	mA
I_O	Digital output current, continuous	V_O = 0 to V_{CC}		±20	mA
	Digital output current, pulsed 1µs	V_O = 0 to V_{CC}		±100	mA
	Continuous current through V_{CC} or GND			±60	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The voltage ratings may be exceeded if the associated clamp current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordrance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_I	Input Voltage(1)		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH} (2)	High-level output current	V_{CC} = 1.65V to 2.2V		–6	mA
		V_{CC} = 2.3V to 5.5V		–20	mA
I_{OL} (2)	Low-level output current	V_{CC} = 1.65V to 5.5V		20	mA
C_L	Digital output load capacitance	V_{CC} = 1.65V to 5.5V		50	pF
V_{POR}	Power-on reset ramp voltage	$\Delta t/\Delta V_{CC}$ ≥ 20µs/V	0.3	1.5	V
$\Delta t/\Delta V_{CC}$	Power-on ramp rate	V_{CC} = 0.3V to 1.5V	20		µs/V
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.65V to 5.5V		100	ms/V

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
(2) Recommended maximum output current for continuous operation; see *Electrical Characteristics* for test current values to maintain V_{OH} and V_{OL} specifications. Operating with average output current greater than 12mA may impact device reliability and shorten the device lifetime.

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DRL (SOT-5X3)	8	118.4	77.1	26.5	3.9	25.9	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

Over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold		1.65V	0.84	1.02	1.21	V
			1.8V	0.91	1.11	1.31	
			2.5V	1.24	1.48	1.72	
			3.3V	1.59	1.85	2.13	
			5V	2.29	2.65	3.03	
			5.5V	2.5	2.88	3.3	
V_{T-}	Negative switching threshold		1.65V	0.51	0.67	0.85	V
			1.8V	0.58	0.74	0.93	
			2.5V	0.88	1.07	1.29	
			3.3V	1.19	1.42	1.68	
			5V	1.8	2.11	2.47	
			5.5V	1.99	2.32	2.71	
ΔV_T	Hysteresis (V_{T+} - V_{T-})		1.65V	0.23	0.36	0.49	V
			1.8V	0.24	0.37	0.5	
			2.5V	0.29	0.40	0.54	
			3.3V	0.34	0.44	0.55	
			5V	0.43	0.53	0.63	
			5.5V	0.44	0.57	0.66	
V_{OH}	High-level output voltage	I_{OH} = -50µA	1.65V - 5.5V	V_{CC} – 0.1	V_{CC} – 0.01		V
		I_{OH} = -1mA	1.65V	1.5	1.6		
		I_{OH} = -2mA	2.3V	2.1	2.2		
		I_{OH} = -8mA	3V	2.3	2.6		
		I_{OH} = -12mA	4.5V	3.6	4		
		I_{OH} = -12mA	5.5V	4.7	5		

5.5 Electrical Characteristics (continued)

Over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = 50µA	1.65V - 5.5V		0.01	0.1	V
		I_{OL} = 1mA	1.65V		0.01	0.1	
		I_{OL} = 2mA	2.3V		0.02	0.1	
		I_{OL} = 8mA	3V		0.05	0.3	
		I_{OL} = 12mA	4.5V		0.06	0.3	
		I_{OL} = 12mA	5.5V		0.06	0.3	
R_p	Internal pull-up or pull-down resistance		1.65V - 5.5V		1		MΩ
I_I (1)	Input leakage current	V_I = 5.5V or GND	5.5V			±200	nA
I_{CC}	Supply current	Standby state, V_I (2) = V_{CC} or GND, I_O = 0	5.5V		1	5	µA
I_{CC}	Supply current	Active state using low speed oscillator(3), V_I = V_{CC} or GND, I_O = 0	1.65V		6	8	µA
			2.3V		7	9	
			3V		8	11	
			4.5V		12	19	
			5.5V		16	26	
I_{CC}	Supply current	Active state using high speed oscillator(3), V_I = V_{CC} or GND, I_O = 0	1.65V		57	59	µA
			2.3V		61	62	
			3V		65	66	
			4.5V		79	97	
			5.5V		93	123	
ΔI_{CC}	Supply-current change	One input, 0 < V_i < V_{CC}, all other inputs at V_{CC} or GND, I_O = 0	1.65V - 5.5V			1.6	mA
C_I		V_I = 5.5V or GND	5.5V		3		pF

(1) Input leakage current does not include current from internal pull-up or pull-down resistors.
(2) Inputs with internal pull-up or pull-down resistors are externally disconnected during supply current test.
(3) See *Typical Characteristics* for a table of which devices use each oscillator.

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	MIN	MAX	UNIT
t_{wi} (1)	Input pulse duration	Any trigger input	1.65V	473		ns
			1.8V ± 0.15V	473		
			2.5V ± 0.2V	470		
			3.3V ± 0.3V	468		
			5V ± 0.5V	463		
t_{wg} (1)	Glitch pulse duration	Any trigger input	1.65V		90	ns
			1.8V ± 0.15V		90	
			2.5V ± 0.2V		90	
			3.3V ± 0.3V		90	
			5V ± 0.5V		90	

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	MIN	MAX	UNIT
t_{su}	Setup time between trigger inputs	$\overline{T}$ low before T↑ or $\overline{CLR}$↑	1.65V	0		ns
			1.8V ± 0.15V	0		
			2.5V ± 0.2V	0		
			3.3V ± 0.3V	0		
			5V ± 0.5V	0		
		T high before $\overline{T}$↓ or $\overline{CLR}$↑	1.65V	0		ns
			1.8V ± 0.15V	0		
			2.5V ± 0.2V	0		
			3.3V ± 0.3V	0		
			5V ± 0.5V	0		
		$\overline{CLR}$ high before $\overline{T}$↓ or T↑	1.65V	0		ns
			1.8V ± 0.15V	0		
			2.5V ± 0.2V	0		
			3.3V ± 0.3V	0		
			5V ± 0.5V	0		
t_h	Hold time	Any trigger input	1.65V	473		ns
			1.8V ± 0.15V	473		
			2.5V ± 0.2V	470		
			3.3V ± 0.3V	468		
			5V ± 0.5V	463		
$t_{startup}$ (2)	Startup time		1.65V - 5.5V		265	µs

(1) Input pulse duration (t_{wi}) indicates the input signal pulse width required to trigger the device. Glitch pulse duration (t_{wg}) indicates the input signal pulse width that is ignored by the glitch filter. Inputs between $t_{wi(min)}$ and $t_{wg(max)}$ may be ignored or may cause the device to trigger.
(2) Triggers received during device startup may be ignored.

5.7 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Any pulse trigger event on $\overline{T}$, T, or $\overline{CLR}$	Q	C_L = 15pF	1.65V		223	312	ns
				2.3V		212	294	
				3V		207	289	
				4.5V		203	283	
				5.5V		201	281	
			C_L = 50pF	1.65V		231	319	
				2.3V		217	299	
				3V		211	291	
				4.5V		206	285	
				5.5V		204	283	
	$\overline{CLR}$ low	Q	C_L = 15pF	1.65V			82	
				2.3V			68	
				3V			63	
				4.5V			59	
				5.5V			57	
			C_L = 50pF	1.65V			76	
				2.3V			65	
				3V			60	
				4.5V			55	
				5.5V			55	
t_t		Q	C_L = 15pF	1.65V		14	18	ns
				2.3V		10	14	
				3V		8	11	
				4.5V		6	9	
				5.5V		5	8	
			C_L = 50pF	1.65V		23	34	
				2.3V		17	25	
				3V		14	20	
				4.5V		11	16	
				5.5V		10	14	
Δt_{wo} (1)		Q	C_L = 50pF	1.65V to 5.5V		±1	±10	%
C_{pd} (2)		Q	T = V_{CC}, $\overline{T}$ = GND, f_I = 1MHz, C_L = 50pF	1.65V		49		pF
				2.3V		37		
				3V		29		
				4.5V		20		
				5.5V		18		

(1) Variation in output pulse width from nominal.
(2) Power dissipation capacitance is calculated in accordance with CMOS Power Consumption and Cpd Calculation.

5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

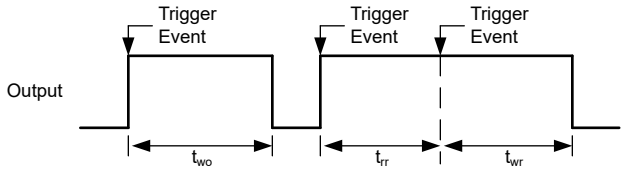


Figure 5-1. Retrigger timing definitions

Table 5-1. Pulse width for each device and configuration

Device	Oscillator	Parameter	Timing Value		
			T1 S1 = H, S0 = L	**T2(1) S1 = L, S0 = L**	**T3 S1 = H, S0 = H**
TPUL1G513**00**	Low speed	t_{wo}	1s	3s	6.8s
		t_{rr}	510ms	510ms	510ms
		t_{wr} (2)	1s	3s	6.8s
		t_{osc}	164ms	164ms	164ms
TPUL1G513**01**	Low speed	t_{wo}	10ms	30ms	68ms
		t_{rr}	0.2ms	0.5ms	1.5ms
		t_{wr} (2)	10ms	30ms	68ms
		t_{osc}	40µs	160µs	480µs
TPUL1G513**02**	High speed(3)	t_{wo}	10µs	32µs	68µs
		t_{rr}	8µs	8µs	8µs
		t_{wr} (2)	2µs	24µs	60µs
		t_{osc}	0.5µs	0.5µs	0.5µs

(1) Default value when S0 and S1 are left disconnected.
(2) The retrigger pulse width (t_{wr}) can additionally vary by up to –t_{osc}.
(3) The high speed clock takes approximately 8µs to start, causing a difference in t_{wo} and t_{wr}.

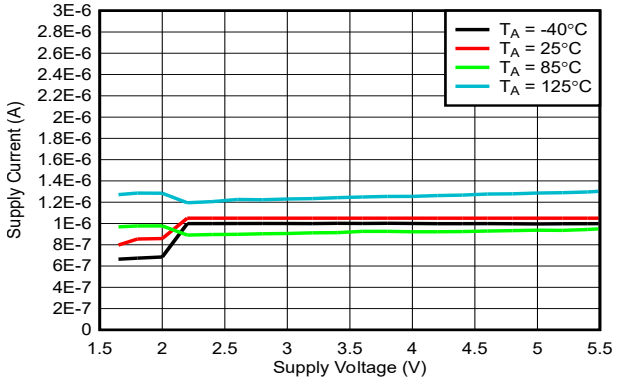


Figure 5-2. Supply Current vs Supply Voltage

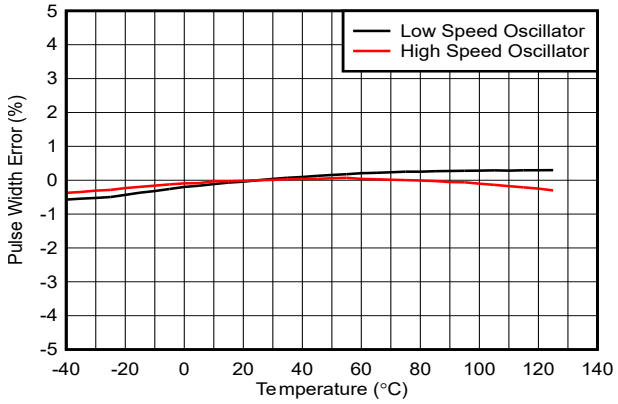


Figure 5-3. Pulse Width Error vs Temperature

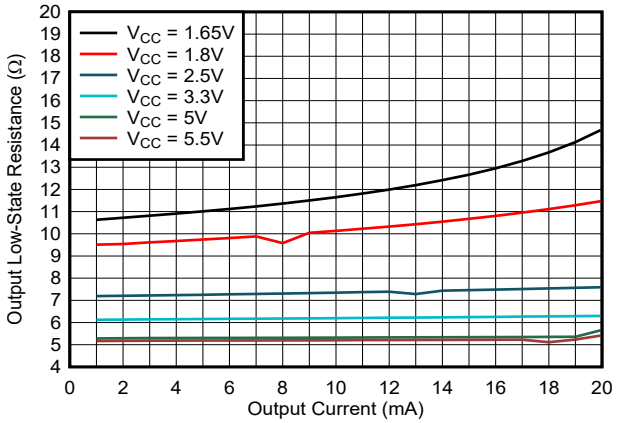


Figure 5-4. Output Low-State Resistance vs Output Current

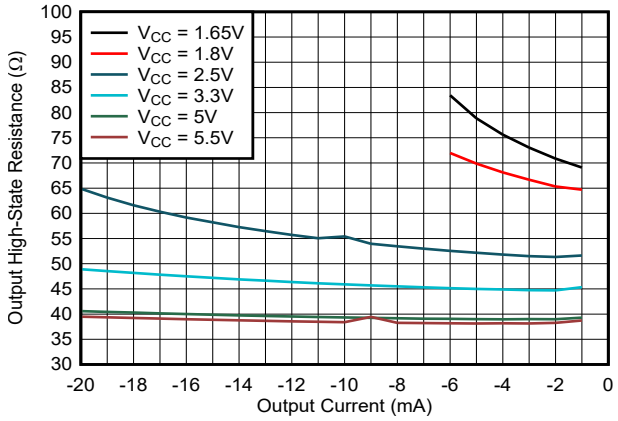
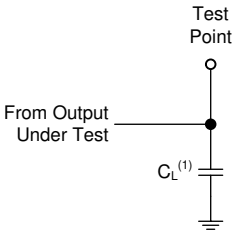


Figure 5-5. Output High-State Resistance vs Output Current

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

The outputs are measured individually with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

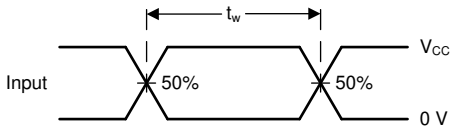


Figure 6-2. Voltage Waveforms, Pulse Duration

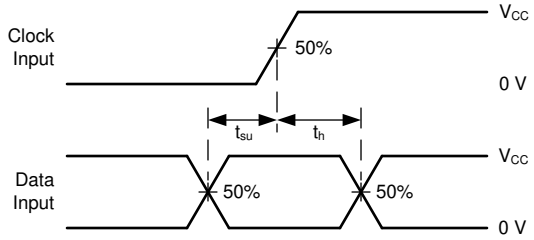
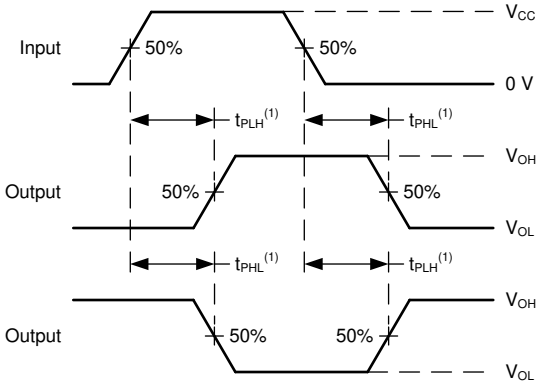
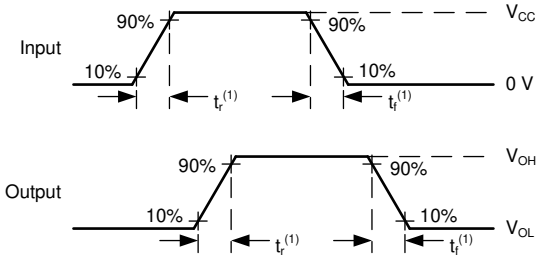


Figure 6-3. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-4. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-5. Voltage Waveforms, Input and Output Transition Times

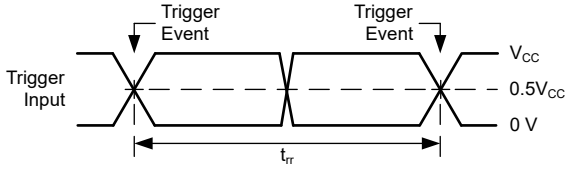


Figure 6-6. Voltage Waveforms, Retrigger Time

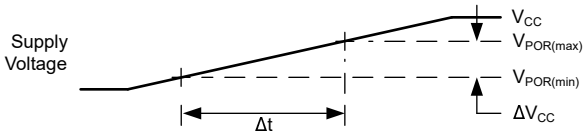


Figure 6-7. Voltage Waveforms, Supply Ramp

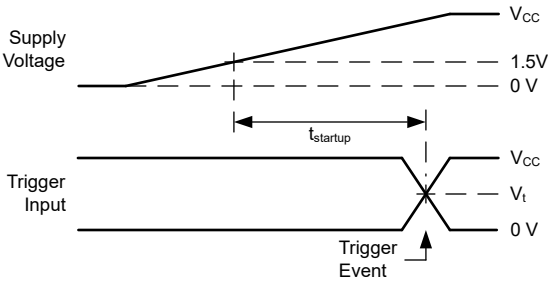


Figure 6-8. Voltage Waveforms, Startup Time

7 Detailed Description

7.1 Overview

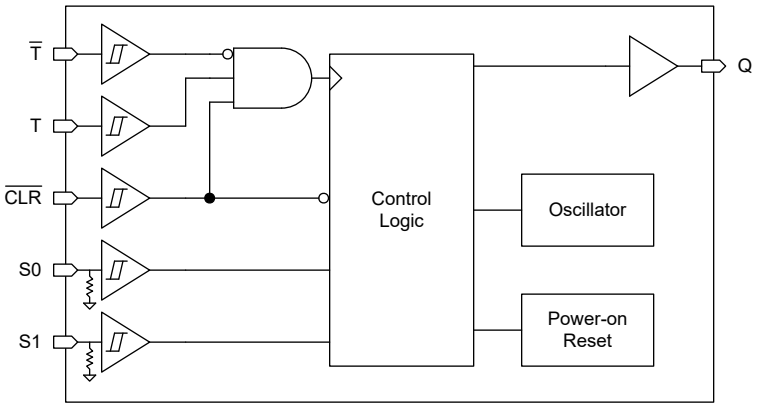
The TPUL1G513-Q1 device contains one digitally timed retriggerable monostable multivibrator circuit. A monostable multivibrator, also commonly known as a "one-shot," produces a single digital pulse when triggered and otherwise maintains a constant output state.

The TPUL1G513-Q1 device features three gated trigger inputs for each channel. For a rising edge trigger, the T or $\overline{CLR}$ input is used. For a falling edge trigger the $\overline{T}$ input is used.

The TPUL1G513-Q1 device includes an asynchronous clear input ($\overline{CLR}$) that can be used to terminate an ongoing output pulse.

When triggered, the TPUL1G513-Q1 outputs a positive digital pulse with pulse width that is pre-defined for each device. The configuration inputs (S0, S1) are used to select one of three possible pulse widths. See the *Typical Characteristics* section for details on the timing options.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Naming Convention

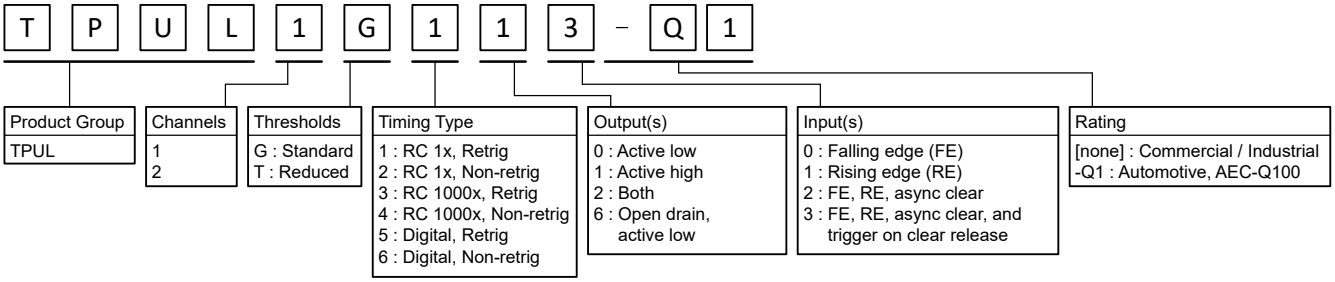


Figure 7-1. Device name meaning

7.3.2 Retriggerable One-Shot

This device includes a retriggerable monostable multivibrator (one-shot) circuit that produces a fixed-width output pulse. The output pulse width for a retriggerable one-shot is extended by additional input triggers while the output is active. The output pulse will expire after the configured time period if no other triggers have been received.

During the retrigger time (t_{rr}), input triggers are ignored. With some timing configurations, the retrigger time can be a significant percentage of the total pulse width. See the *Typical Characteristics* section for more details.

7.3.3 Timing Mechanism and Accuracy

The output pulse width (t_{wo}) is generated by a factory-trimmed internal oscillator and binary counter. Each device offers three configurable pulse widths: T1, T2, and T3. When triggered, the output is immediately activated. The oscillator then activates and drives the counter until the pre-configured count is reached, at which point the oscillator and output deactivate.

Trigger events include oscillator startup time in the total pulse width. Retrigger events complete faster because the oscillator is already running and startup time is eliminated. Refer to the timing table in the *Typical Characteristics* section for expected pulse widths under both initial trigger and retrigger conditions.

The maximum pulse width error is provided as Δt_{wo} in the *Switching Characteristics* section and includes variations due to voltage, design, manufacturing, and temperature. This variation is given as a percentage of the typical pulse width provided in the *Typical Characteristics* section.

7.3.4 CMOS Push-Pull Outputs

This device includes CMOS push-pull outputs. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.5 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device with the maximum value per input defined as ΔI_{CC} in the *Electrical Characteristics* table. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at a valid high or low voltage level. If a system is not actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and will typically meet all requirements.

Inputs that include internal pull-up or pull-down resistors are internally terminated to an appropriate logic level and can be left disconnected.

7.3.6 Latching Logic with Known Power-Up State

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory. In typical logic devices, the output state of each latching circuit is unknown after power is initially applied; however, this device includes an added Power On Reset (POR) circuit which sets the states of all included latching circuits during the power-up ramp prior to the device starting normal functionality.

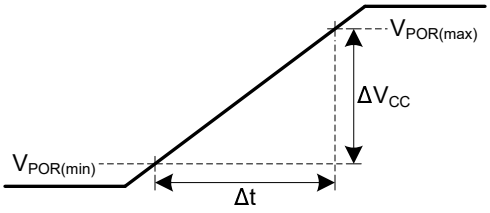


Figure 7-2. Supply (V_{CC}) Ramp Characteristics for Known Power-Up State

Figure 7-2 shows a correct supply voltage turn-on ramp and defines values used in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

Prior to starting the power-on ramp, the supply must be completely off ($V_{CC} \leq V_{POR(min)}$).

The supply voltage must ramp at a rate within the range provided in the *Recommended Operating Conditions* table.

The output state of each latching logic circuit only remains stable as long as power is applied to the device ($V_{CC} \geq V_{POR(max)}$).

Variation from these recommendations will result in the device having an unknown power-up state.

7.3.7 Clamp Diode Structure

As shown in Figure 7-3, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

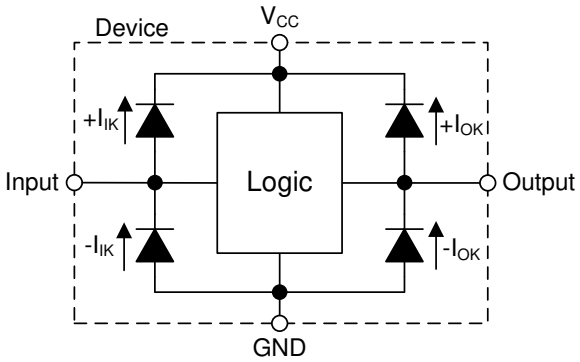


Figure 7-3. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

7.4.1 Startup Operation

The TPUL1G513-Q1 includes an internal power-on reset (POR) circuit that prevents erroneous triggers from occurring during startup. There are details on the supply ramp requirements provided in *Latching Logic with Known Power-Up State*. Normal operation can be started after the startup time ($t_{startup}$) has expired per the *Timing Requirements* table. While active, the POR circuit holds all outputs of the TPUL1G513-Q1 in the high-impedance state.

7.4.2 On-State Operation

The tables below list the on-state functional modes for the TPUL1G513-Q1.

Table 7-1. Timing Configuration Table

INPUTS		CONFIGURED TIMING
S1	S0	
L	L	T2
L	H	—
H	L	T1
H	H	T3

Table 7-2. Function Table

INPUTS(1)			OUTPUTS(2)	
$\overline{CLR}$	$\overline{T}$	T	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L(3)	H(3)
H	X	L	L(3)	H(3)
H	L	↑	⎍ (4)	⎍ (4)
H	↓	H	⎍ (4)	⎍ (4)
↑	L	H	⎍	⎍

(1) H = high voltage level, L = low voltage level, X = don't care

(2) L = driving low, H = driving high, ⎍ = driving high for the defined pulse width time, ⎍ = driving low for the defined pulse width time

(3) These outputs are based on the assumption that the indicated steady-state conditions at the inputs have been set up long enough to complete any output pulse.

(4) If an output pulse is triggered while a previous output pulse is still active and after the retrigger time (t_{rr}) has expired, the output continues to drive high for one retrigger pulse width (t_{wr}).

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPUL1G513-Q1 is used to generate a fixed-width pulse from an input trigger event.

8.2 Typical Application - Edge Detector

In this application, the TPUL1G513-Q1 is used to detect rising or falling edges on an input signal, producing fixed-width pulses at the output for each edge detected. The circuit configuration for a rising edge detector is shown in Figure 8-1. For a falling edge detector, connect the input signal to the $\overline{T}$ input instead of the T input, and connect the T input to V_{CC}. The default timing option (T2) with S0 = S1 = LOW is shown. To select T1, connect S1 to V_{CC}. To select T2, connect S1 and S0 to V_{CC}. Otherwise, the components and configuration are identical.

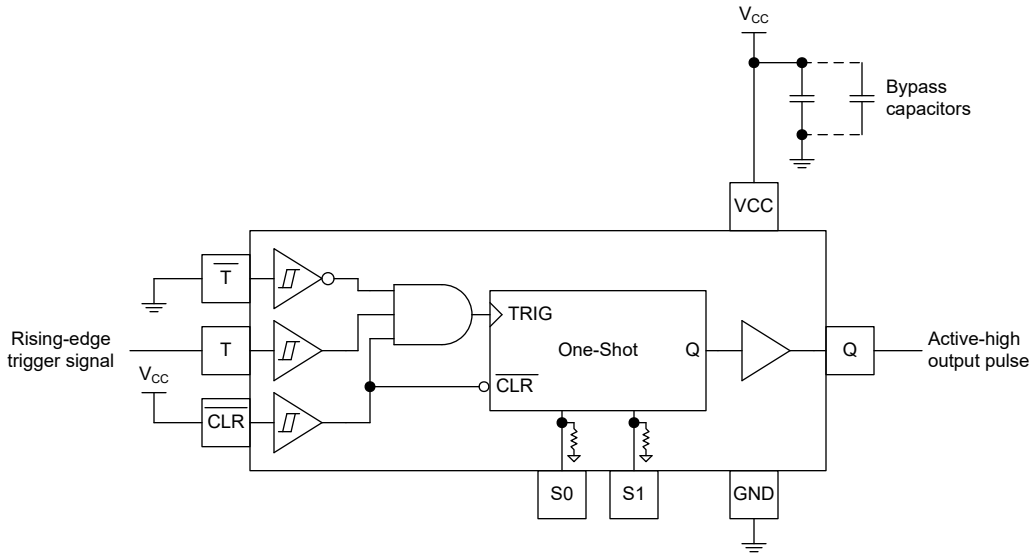


Figure 8-1. Pulse Generator Schematic Using the TPUL1G513-Q1

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the TPUL1G513-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Verify that the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the TPUL1G513-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground

connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The TPUL1G513-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied; however, do not exceed 50pF.

The TPUL1G513-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

The TPUL1G513-Q1 includes inputs with internal pulldown resistors. The pulldown resistors are connected to GND internally and increases the total ground current based on the input voltage (V_i) and pulldown resistance (R_{pd}) per the equation: $I_{pd} = V_i/R_{pd}$

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the TPUL1G513-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The TPUL1G513-Q1 includes inputs with pull-down resistors. These inputs can be left disconnected and will be internally set to GND.

The TPUL1G513-Q1 supports very slow input signal transition rates because it has Schmitt-Trigger inputs. See *Recommended Operating Conditions*.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics* table. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics* section.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the TPUL1G513-Q1 to the receiving device.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

8.2.3 Application Curves

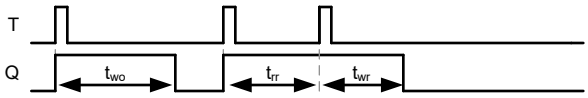


Figure 8-2. Output Pulse Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

During startup, the power supply should ramp within the provided power-up ramp rate range in the *Recommended Operating Conditions* table.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For normal operation of the TPUL1G513-Q1, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output

- Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

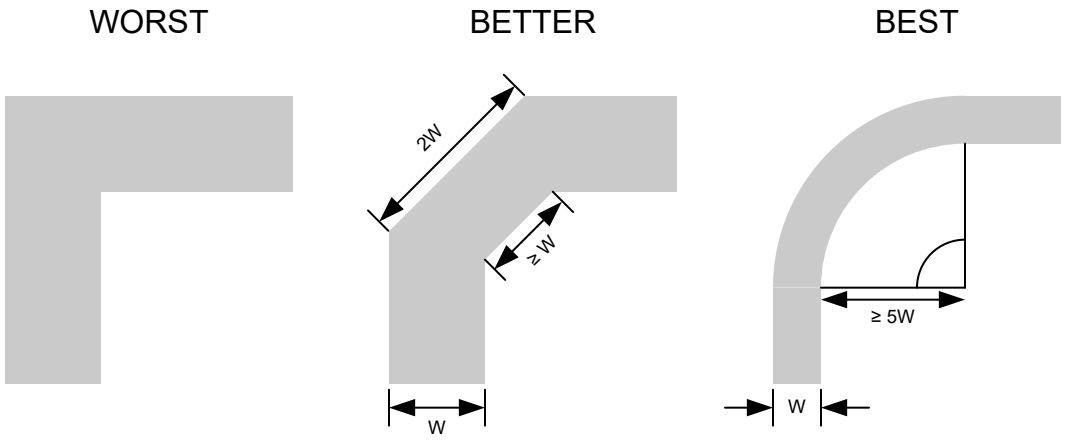


Figure 8-3. Example Trace Corners for Improved Signal Integrity

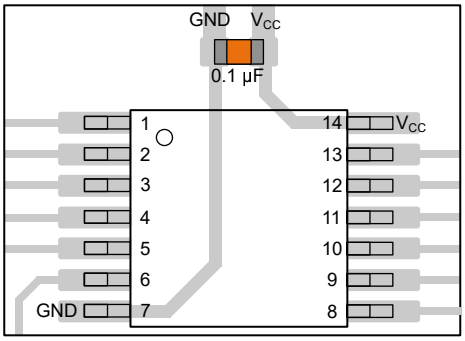


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

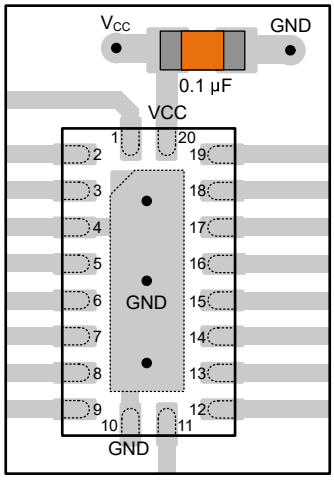


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

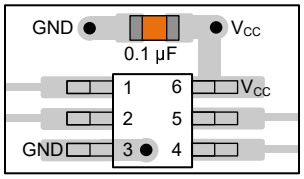


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

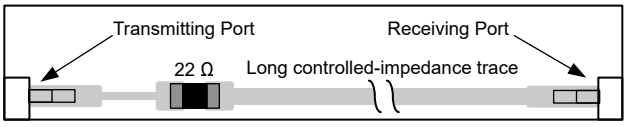


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPUL1G51300DRLRQ1	Active	Production	SOT-5X3 (DRL) | 8	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	QPA00
TPUL1G51301DRLRQ1	Active	Production	SOT-5X3 (DRL) | 8	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	QPA01
TPUL1G51302DRLRQ1	Active	Production	SOT-5X3 (DRL) | 8	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	QPA02

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPUL1G513-Q1 :

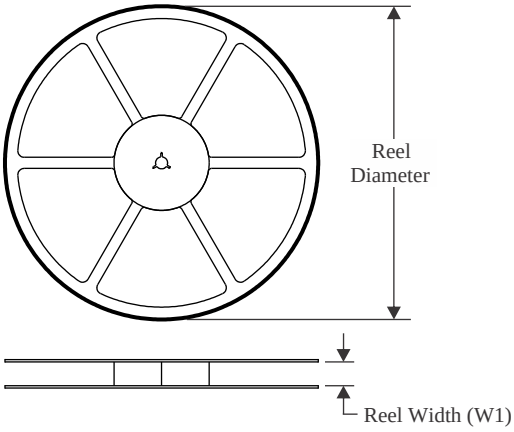
- Catalog : TPUL1G513

NOTE: Qualified Version Definitions:

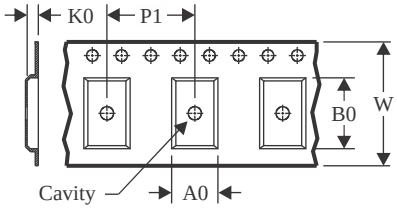
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

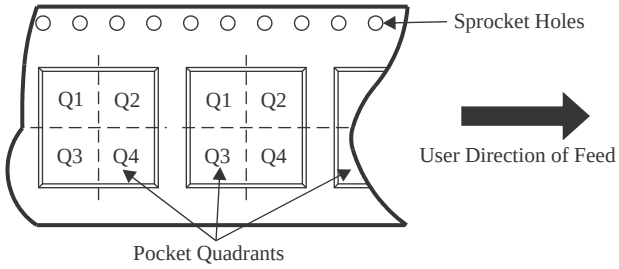


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

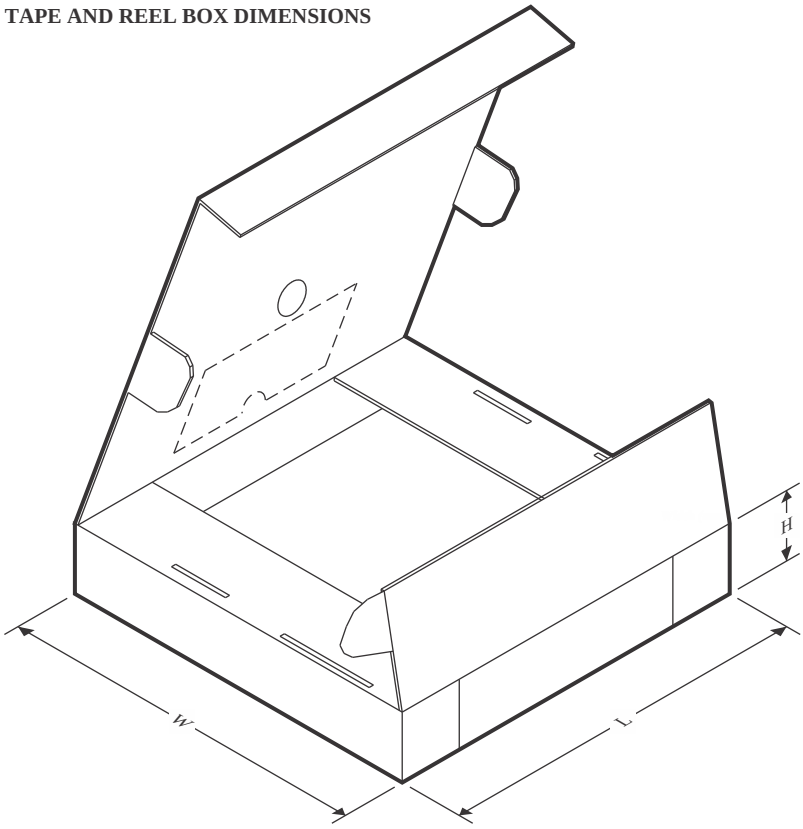
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPUL1G51300DRLRQ1	SOT-5X3	DRL	8	3000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPUL1G51301DRLRQ1	SOT-5X3	DRL	8	3000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPUL1G51302DRLRQ1	SOT-5X3	DRL	8	3000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

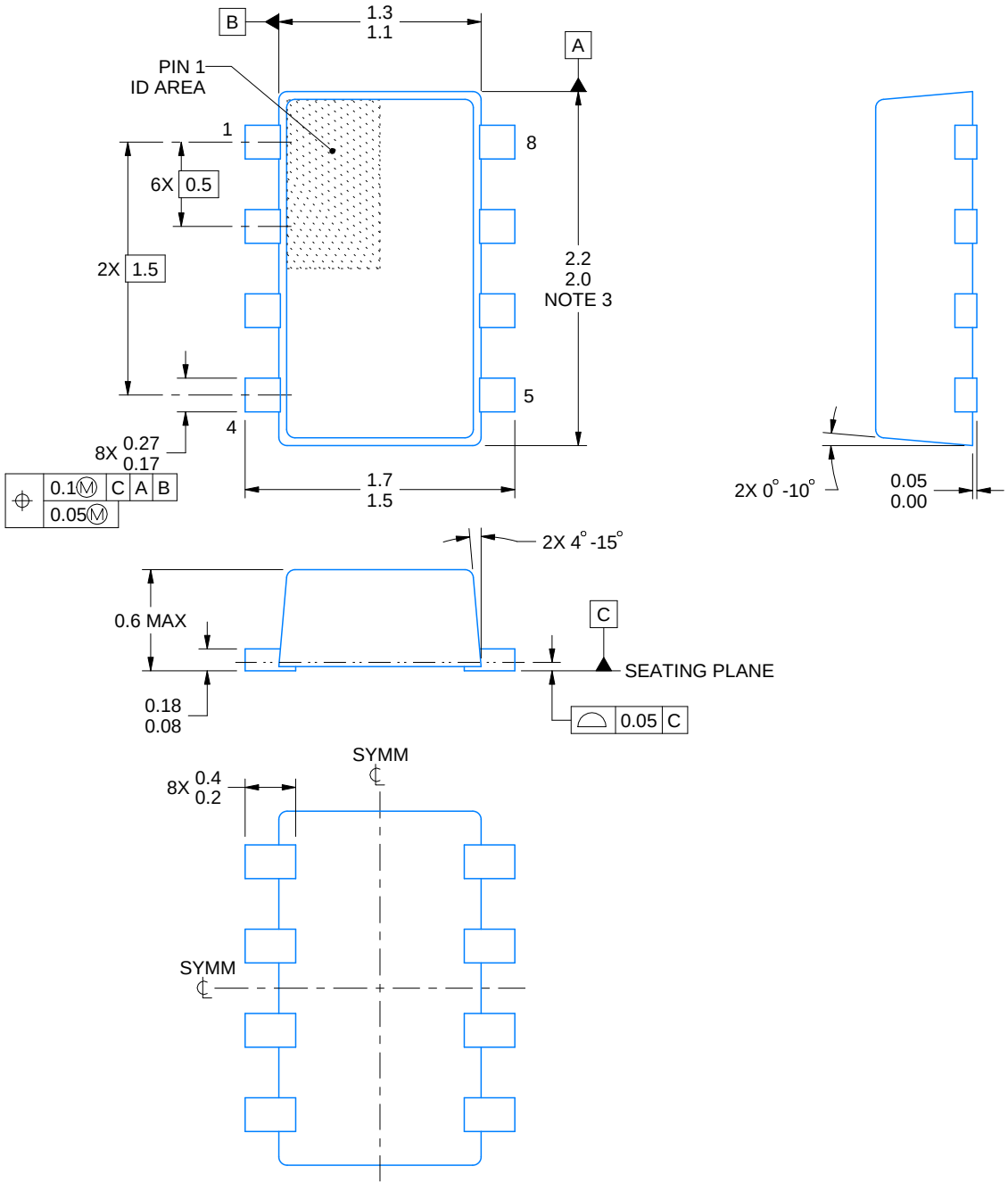
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPUL1G51300DRLRQ1	SOT-5X3	DRL	8	3000	210.0	185.0	35.0
TPUL1G51301DRLRQ1	SOT-5X3	DRL	8	3000	210.0	185.0	35.0
TPUL1G51302DRLRQ1	SOT-5X3	DRL	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



4224486/G 11/2024

NOTES:

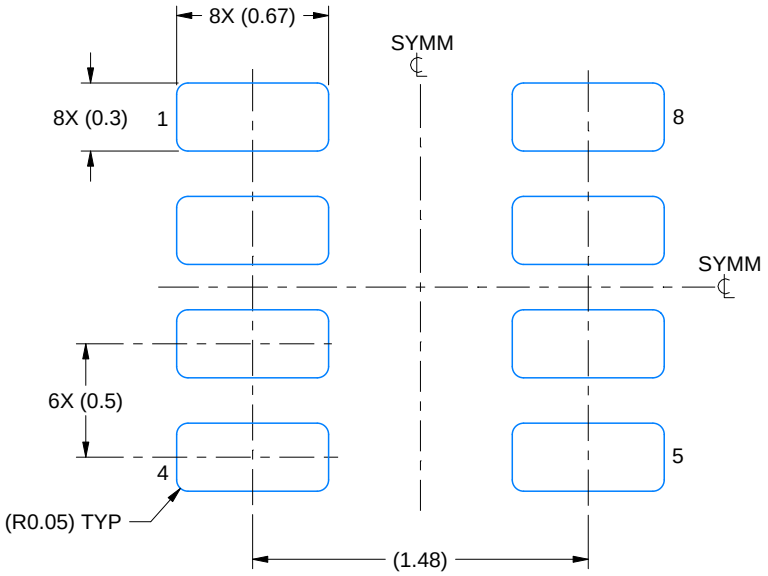
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

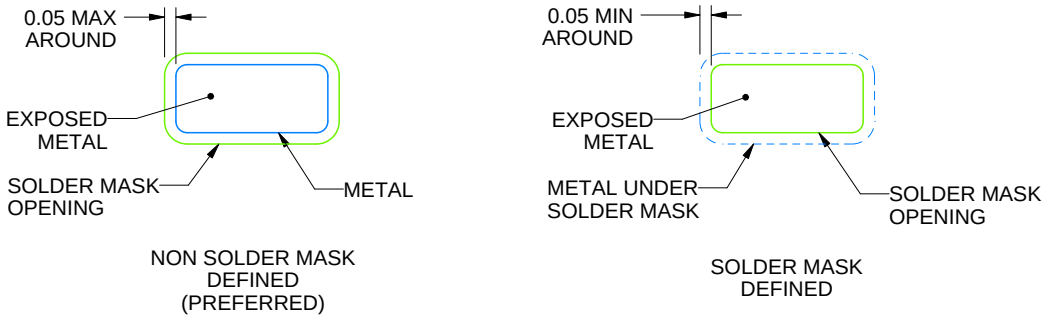
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

4224486/G 11/2024

NOTES: (continued)

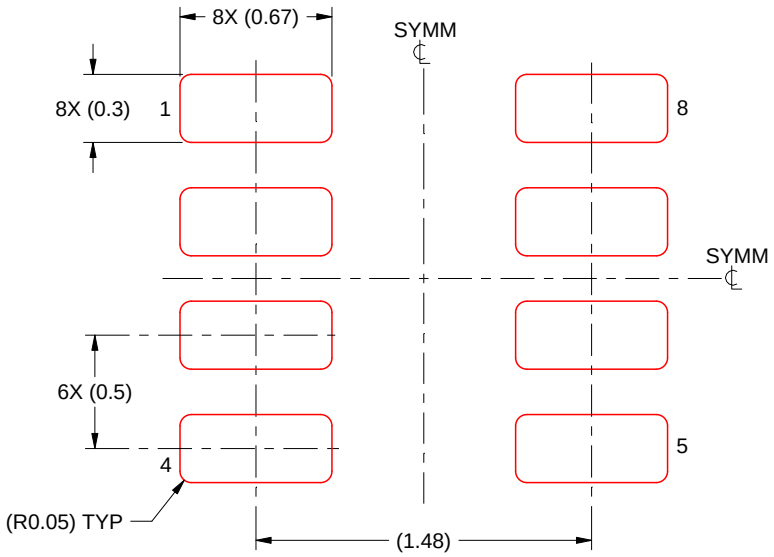
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224486/G 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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