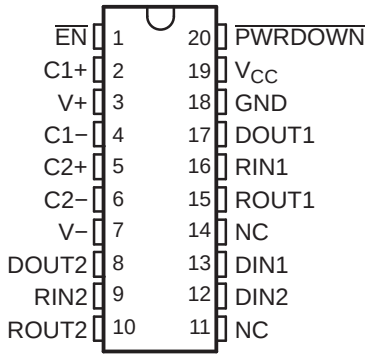
TRS3222
3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD PROTECTION

SLLS815 – JULY 2007

FEATURES

- **RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates With 3-V to 5.5-V V_{CC} Supply**
- **Operates up to 250 kbit/s**
- **Two Drivers and Two Receivers**
- **Low Standby Current . . . 1 µA Typical**
- **External Capacitors . . . 4 × 0.1 µF**
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **Alternative High-Speed Pin-Compatible Device (1 Mbit/s)**
  - **TRSF3222**

DB, DW, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

APPLICATIONS

- **Battery-Powered Systems**
- **PDAs**
- **Notebooks**
- **Laptops**
- **Palmtop PCs**
- **Hand-Held Equipment**

DESCRIPTION/ORDERING INFORMATION

The TRS3222 consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate.

The TRS3222 can be placed in the power-down mode by setting $\overline{\text{PWRDOWN}}$ low, which draws only 1 µA from the power supply. When the device is powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled; V+ is lowered to V_{CC}, and V– is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting $\overline{\text{EN}}$ high.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – DW	Tube of 25	TRS3222CDW	TRS3222C
		Reel of 2000	TRS3222CDWR	
	SSOP – DB	Tube of 70	TRS3222CDB	RS22C
		Reel of 2000	TRS3222CDBR	
	TSSOP – PW	Tube of 70	TRS3222CPW	RS22C
		Reel of 2000	TRS3222CPWR	
–40°C to 85°C	SOIC – DW	Tube of 25	TRS3222IDW	TRS3222I
		SSOP – DB	TRS3222IDWR	
	SSOP – DB	Tube of 70	TRS3222IDB	RS22I
		Reel of 2000	TRS3222IDBR	
	TSSOP – PW	Tube of 70	TRS3222IPW	RS22I
		Reel of 2000	TRS3222IPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Each Driver(1)

INPUTS		OUTPUT DOUT
DIN	$\overline{\text{PWRDOWN}}$	
X	L	Z
L	H	H
H	H	L

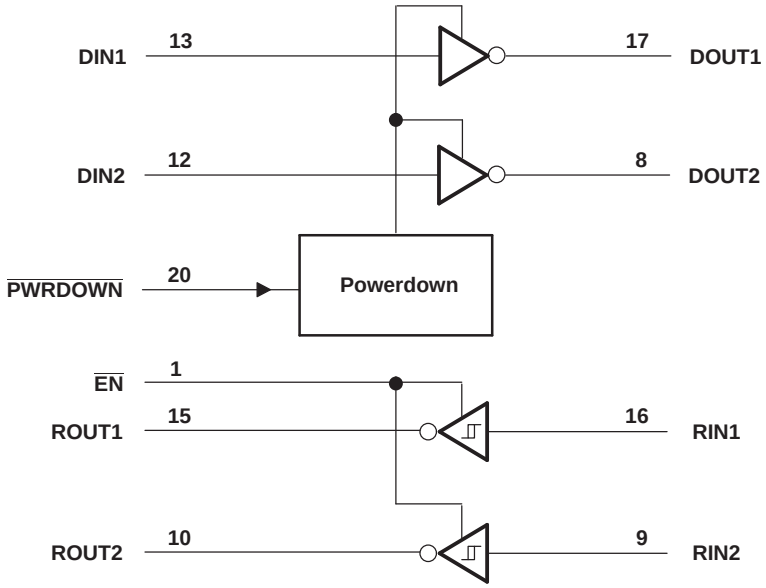
(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver(1)

INPUTS		OUTPUT ROUT
RIN	$\overline{\text{EN}}$	
L	L	H
H	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive output supply voltage range(2)		–0.3	7	V
V–	Negative output supply voltage range(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	Drivers, $\overline{EN}$, $\overline{PWRDOWN}$	–0.3	6	V
		Receivers	–25	25	
V_O	Output voltage range	Drivers	–13.2	13.2	V
		Receivers	–0.3	V_{CC} + 0.3	
θ_{JA}	Package thermal impedance(3)(4)	DB package		70	°C/W
		DW package		58	
		PW package		83	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

See Figure 5

				MIN	NOM	MAX	UNIT
	Supply voltage	V_{CC} = 3.3 V		3	3.3	3.6	V
		V_{CC} = 5 V		4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{EN}$, $\overline{PWRDOWN}$	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{EN}$, $\overline{PWRDOWN}$				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{EN}$, $\overline{PWRDOWN}$		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature	TRS222C		0		70	°C
		TRS222I		–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
I_I	Input leakage current ($\overline{EN}$, $\overline{PWRDOWN}$)			±0.01	±1	µA
I_{CC}	Supply current	No load, $\overline{PWRDOWN}$ at V_{CC}		0.3	1	mA
	Supply current (powered off)	No load, $\overline{PWRDOWN}$ at GND		1	10	µA

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

DRIVER SECTION

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND	5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}	–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}			±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	µA
I_{OS}	Short-circuit output current(3)	V_{CC} = 3.6 V,	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V				
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V	300	10 M		Ω
I_{off}	Output leakage current	$\overline{PWRDOWN}$ = GND, V_{CC} = 3 V to 3.6 V	V_O = ±12 V			±25	µA
		$\overline{PWRDOWN}$ = GND, V_{CC} = 4.5 V to 5.5 V	V_O = ±10 V			±25	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
	Maximum data rate	C_L = 1000 pF, One DOUT switching,	R_L = 3 kΩ, See Figure 1	150	250		kbit/s
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF to 2500 pF, See Figure 2	R_L = 3 kΩ to 7 kΩ,		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	R_L = 3 kΩ to 7 kΩ, V_{CC} = 3.3 V	C_L = 150 pF to 1000 pF	6		30	V/µs
			C_L = 150 pF to 2500 pF	4		30	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

RECEIVER SECTION

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OH} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.5	2.4	V
		V_{CC} = 5 V		1.8	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.2		V
		V_{CC} = 5 V	0.8	1.5		
V_{hys}	Input hysteresis ($V_{IT+} – V_{IT–}$)			0.3		V
I_{off}	Output leakage current	$\overline{EN} = V_{CC}$		±0.05	±10	µA
r_I	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

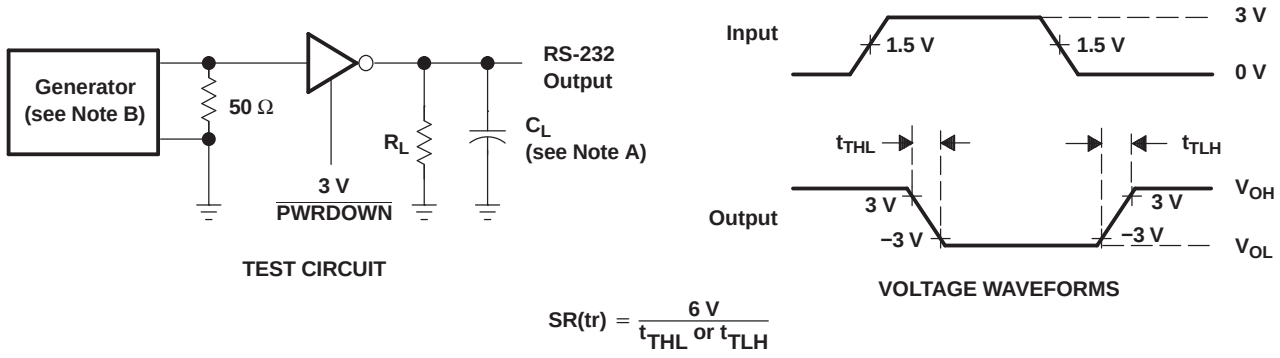
Switching Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See Figure 3		300		ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF, See Figure 3		300		ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 4		200		ns
t_{dis}	Output disable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 4		200		ns
$t_{sk(p)}$	Pulse skew(3)	See Figure 3		300		ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

PARAMETER MEASUREMENT INFORMATION

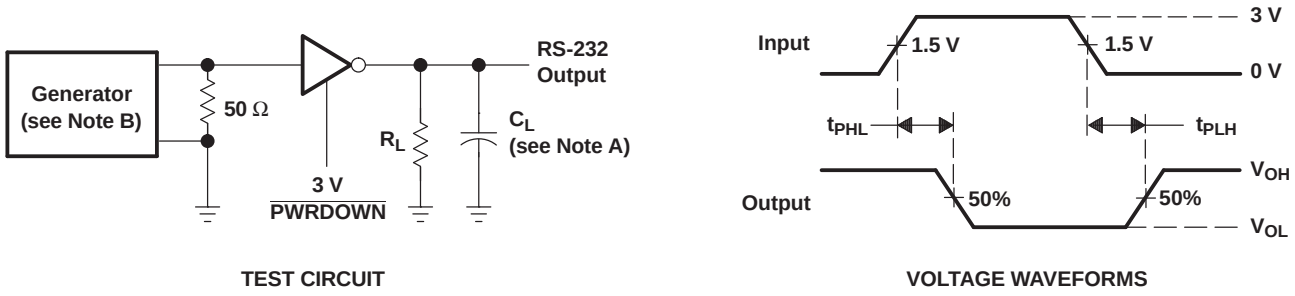


$$SR(tr) = \frac{6\ V}{t_{THL} \text{ or } t_{TLH}}$$

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤10 ns, t_f ≤ 10 ns.

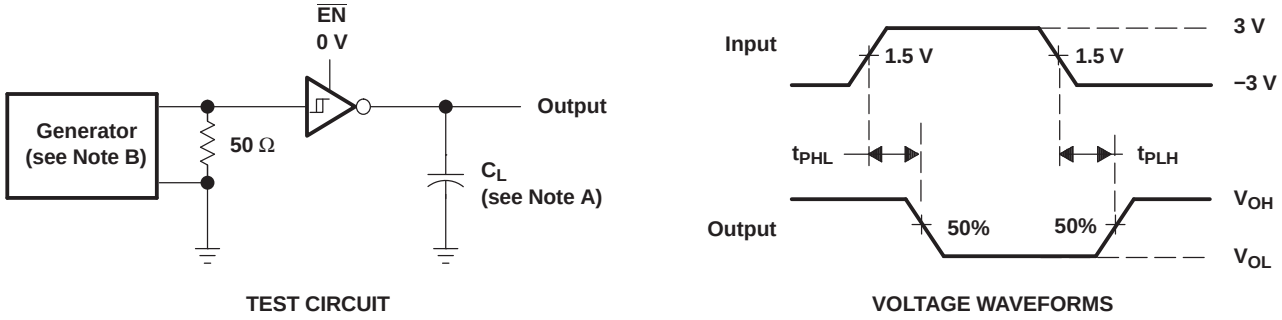
Figure 1. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤10 ns, t_f ≤ 10 ns.

Figure 2. Driver Pulse Skew

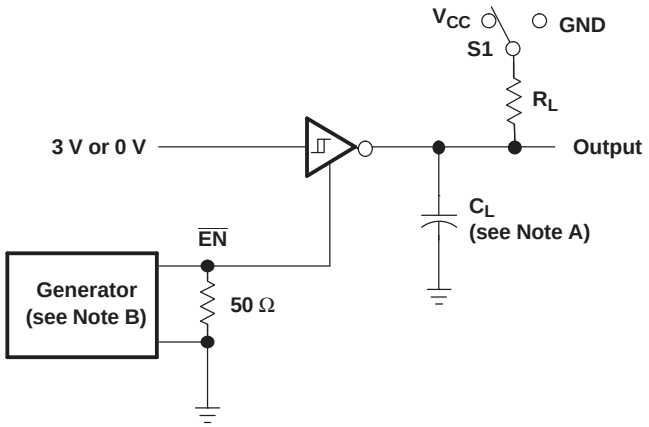


A. C_L includes probe and jig capacitance.

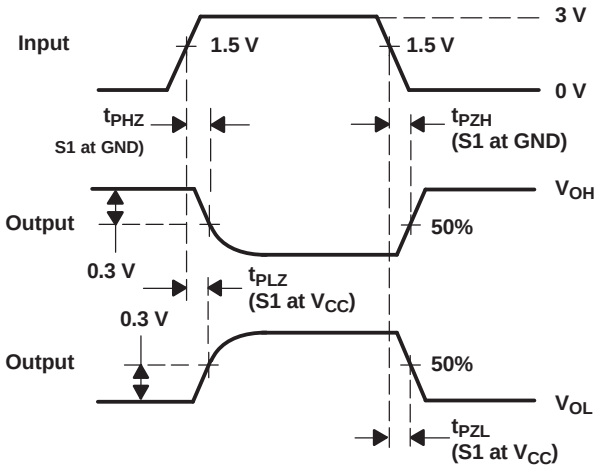
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤10 ns, t_f ≤ 10 ns.

Figure 3. Receiver Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT



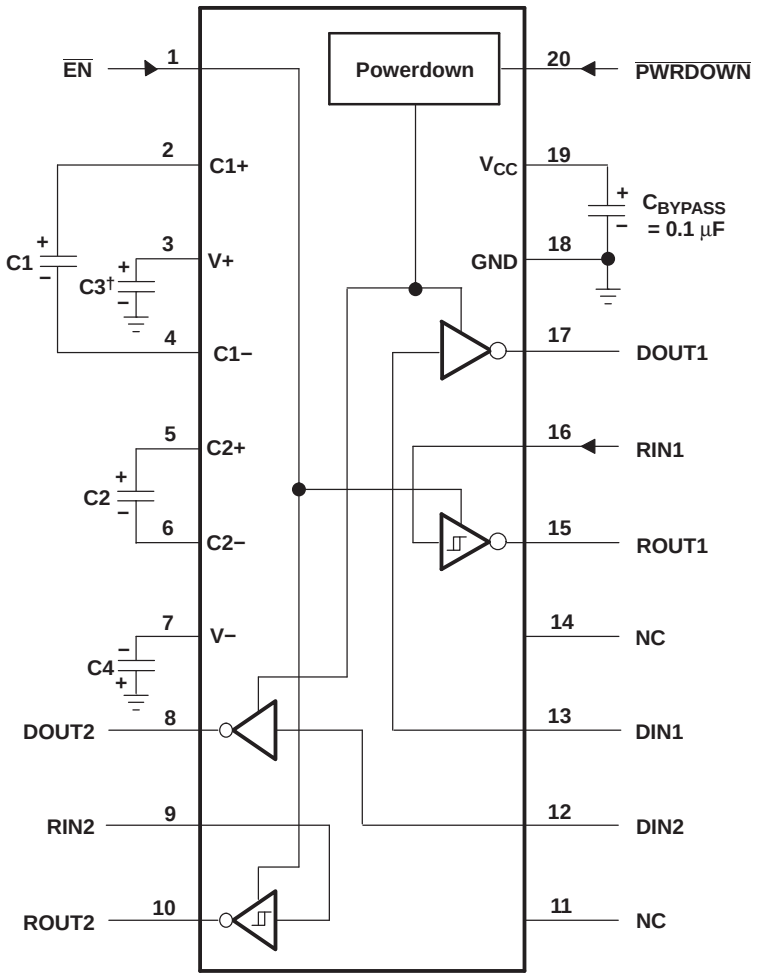
VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤10 ns, t_f ≤ 10 ns.

Figure 4. Receiver Enable and Disable Times

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.
B. NC − No internal connection
C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

Figure 5. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS3222CDBR	Obsolete	Production	SSOP (DB) | 20	-	-	Call TI	Call TI	0 to 70	RS22C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

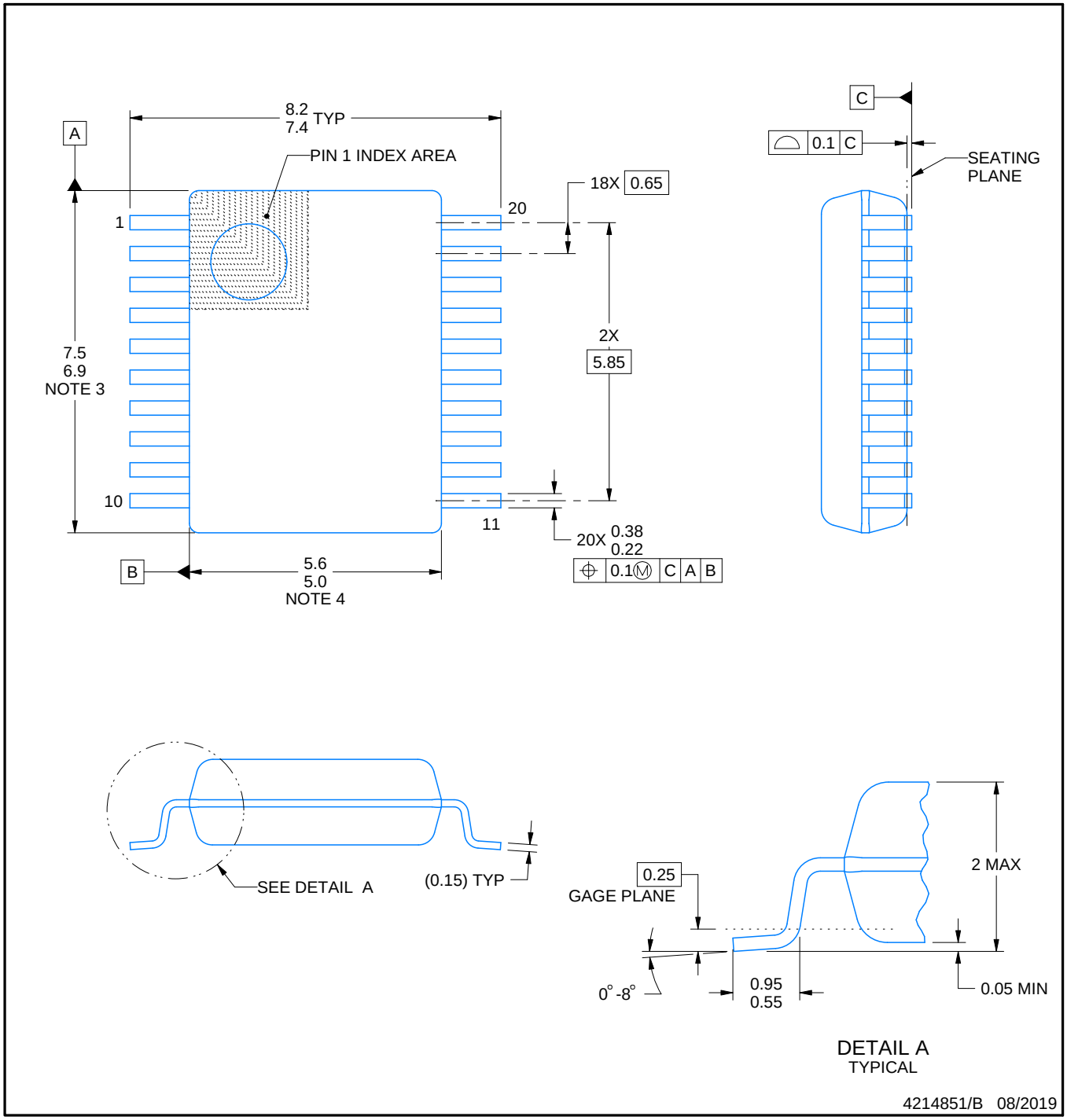
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DB0020A

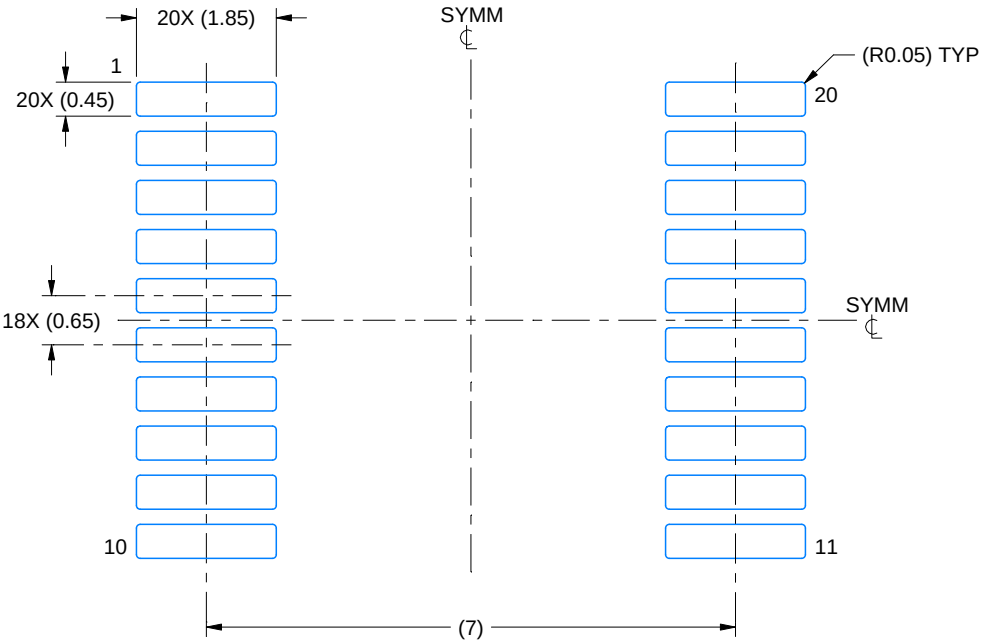
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

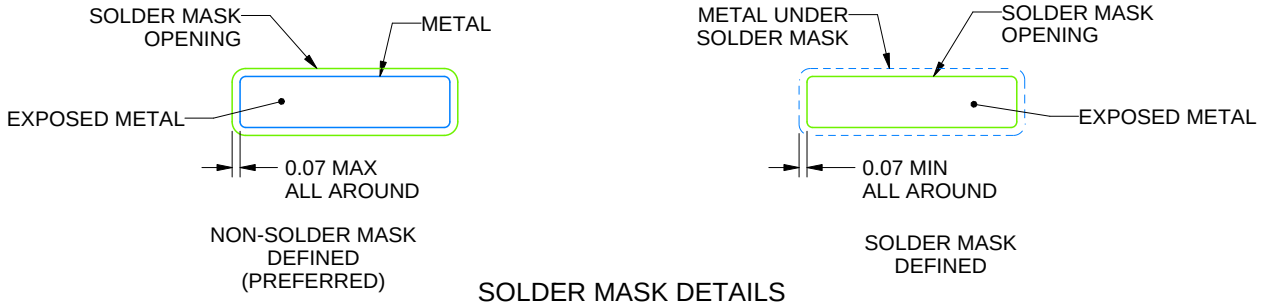


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

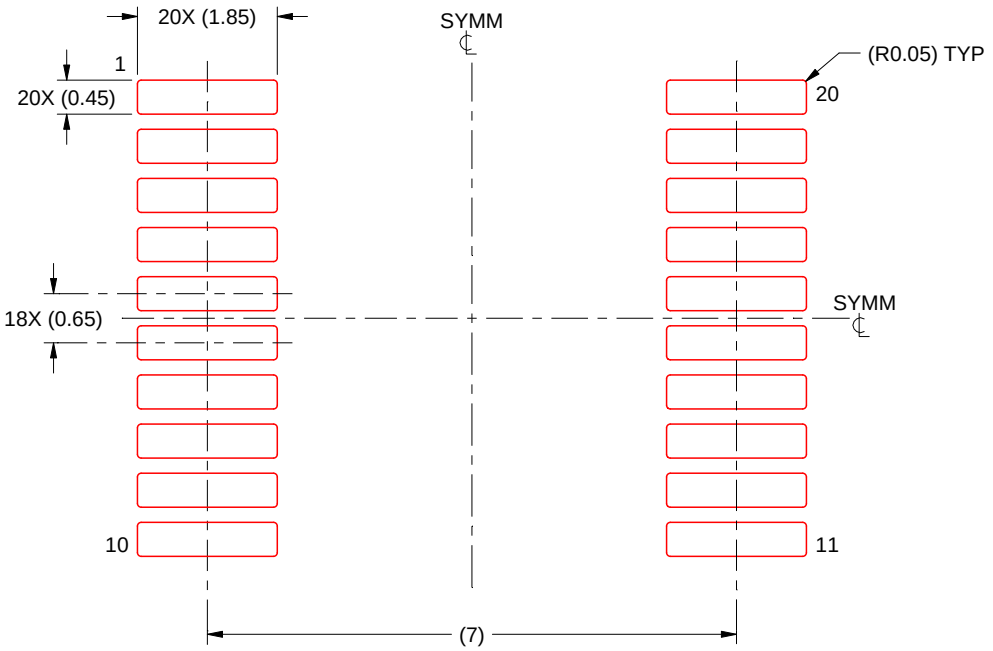
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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