

TSD05 5-V Unidirectional TVS Diode in SOD-323

1 Features

- IEC 61000-4-2 level 4 ESD protection:
 - ± 30 kV contact discharge
 - ± 30 kV air gap discharge
- IEC 61000-4-5 surge protection:
 - 60 A (8/20 μ s)
 - Low clamping voltage: 9 V at 60 A (8/20 μ s)
- IO capacitance:
 - 19 pF (typical)
- DC breakdown voltage: 7 V (typical)
- Ultra low leakage current: 50 nA (maximum)
- Low ESD clamping voltage: 7.5 V at 16 A TLP
- Industrial temperature range: -55°C to $+150^{\circ}\text{C}$
- Industry standard SOD-323 leaded package (2.5 mm \times 1.2 mm \times 0.3 mm)

2 Applications

- 5-V power rails
- [USB VBUS](#)
- GPIO
- Push buttons
- [Grid infrastructure](#)
- EPOS
- [Portable electronics](#)

3 Description

The TSD05 is a unidirectional TVS protection diode designed for clamping harmful transients such as ESD and surge. The TSD05 is rated to dissipate ESD strikes up to ± 30 kV (contact and air gap discharge) and also meets the maximum level specified in the IEC 61000-4-2 international standard (Level 4). For surges, the device can clamp 8/20 μ s surges with peak currents up to 60 A in accordance with the IEC 61000-4-5 standard.

This device also features a 19 pF (typical) IO capacitance enabling it to protect data lines. The low dynamic resistance and low clamping voltage provides system level protection against transient events.

Combining the robust clamping performance and low capacitance of this device, TSD05 is an excellent TVS diode to protect both data and power lines in many different applications.

The TSD05 is offered in the industry standard, leaded SOD-323 package to enable easy solderability.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TSD05	DYF (SOD-323, 2)	2.65 mm \times 1.3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The package size (length \times width) is a nominal value and includes pins, where applicable.



Functional Block Diagram



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4 Revision History

DATE	REVISION	NOTES
July 2023	*	Initial Release

5 Pin Configuration and Functions

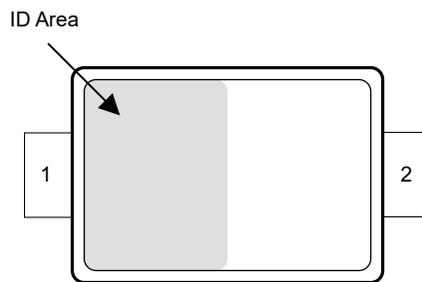


Figure 5-1. DYF Package, 2-Pin SOD-323 (Top View)

Table 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	IO	I/O	Protected Channel
2	GND	GND	Ground. Connect to ground.

(1) I = input, O = output. GND = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Peak Pulse ^{(2) (3)}	IEC 61000-4-5 power ($t_p - 8/20 \mu s$)		530	W
	IEC 61000-4-5 Current ($t_p - 8/20 \mu s$)		60	A
T_A	Ambient Operating Temperature	-55	150	°C
T_{stg}	Storage Temperature	-65	155	°C

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Voltages are with respect to GND unless otherwise noted.
- (3) Measured at 25°C

6.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002 ⁽²⁾	±1000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±30000	V
		IEC 61000-4-2 air-gap discharge	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IO}	Input pin voltage	IO to GND	0		5.5	V
T_A	Operating free-air temperature		-55		150	°C

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TSD05	UNIT
		DYF (SOD-323)	
		2 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	672.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	230.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	541.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	64.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	527.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics

At TA=25°C (unless otherwise noted) ⁽¹⁾

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V _{RWM}	Reverse stand-off voltage	I _{IO} < 50 nA, across operating temperature range			5.5	V
I _{LEAK}	Reverse leakage current	V _{IO} = 5.5 V, IO to GND		5	50	nA
V _{BR}	Break-down voltage	I _{IO} = 1 mA, IO to GND	6	7	8	V
V _{FWD}	Forward voltage	I _{IO} = 1 mA, GND to IO		0.7		V
V _{CLAMP}	Surge clamping voltage, t _p = 8/20 μs ⁽²⁾	I _{PP} = 24 A, IO to GND		8		V
		I _{PP} = 60 A, IO to GND		9		V
		I _{PP} = 60 A, GND to IO		5.5		V
	TLP clamping voltage, t _p = 100 ns	I _{PP} = 16 A, IO to GND		7.5		V
I _{PP} = 16 A, GND to IO			1.1		V	
C _L	Line capacitance	V _{IO} = 0 V; f = 1 MHz, IO to GND		19		pF

(1) Typical parameters are measured at 25°C

(2) Nonrepetitive current pulse 8 to 20 μs exponentially decaying waveform according to IEC 61000-4-5

6.7 Typical Characteristics

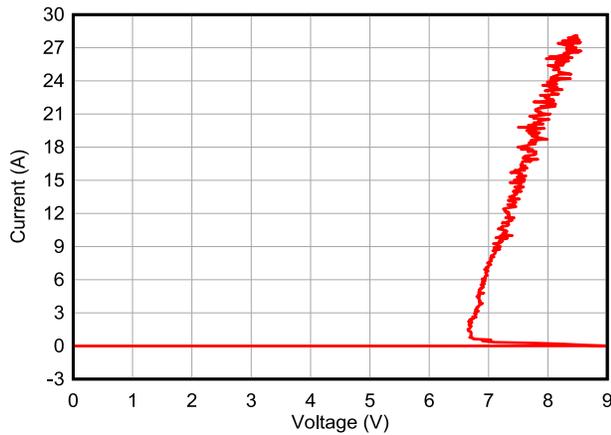


Figure 6-1. Positive TLP Curve

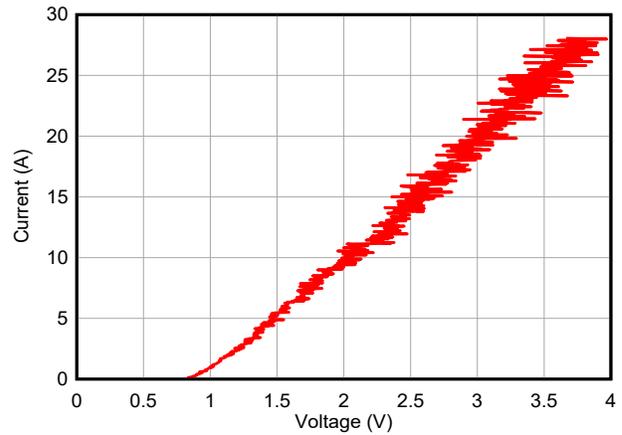


Figure 6-2. Negative TLP Curve

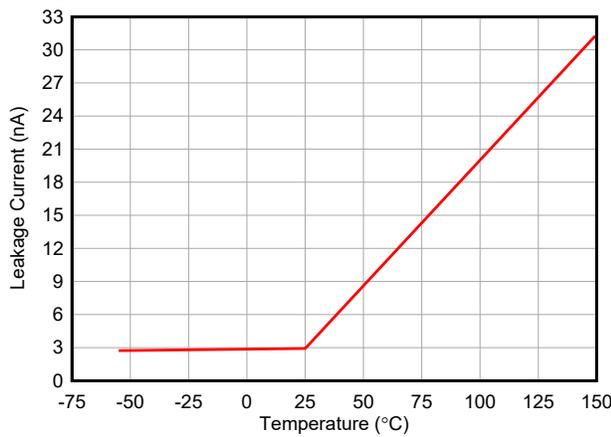


Figure 6-3. Temperature vs Leakage Current

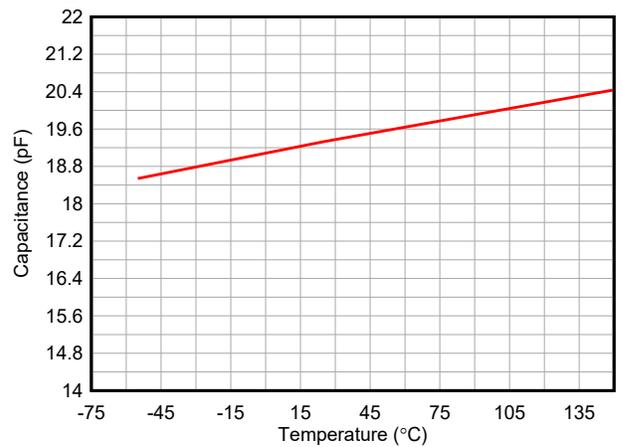


Figure 6-4. Temperature vs Capacitance

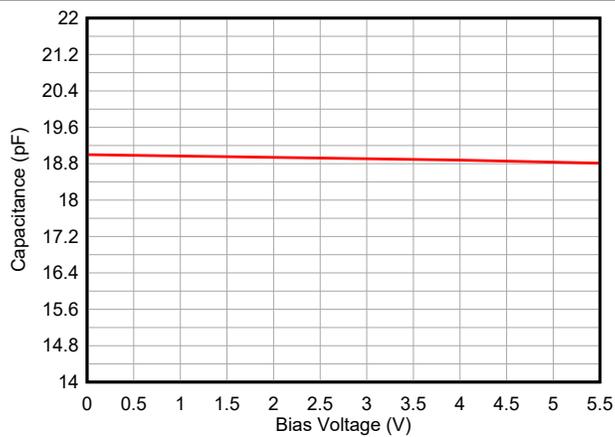


Figure 6-5. Bias Voltage vs Capacitance

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TSD05 is a diode type TVS which provides a path to ground for dissipating transient voltage spikes, such as ESD or surge, on signal lines and power lines. The device should be connected in parallel to the down stream circuitry it is protecting. As the current from the transient passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, refer to the [ESD Packaging and Layout Guide](#).

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Layout Guide application reports](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Picking ESD Diodes for Ultra High-Speed Data Lines application reports](#)
- Texas Instruments, [Reading and Understanding an ESD Protection data sheet](#)

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

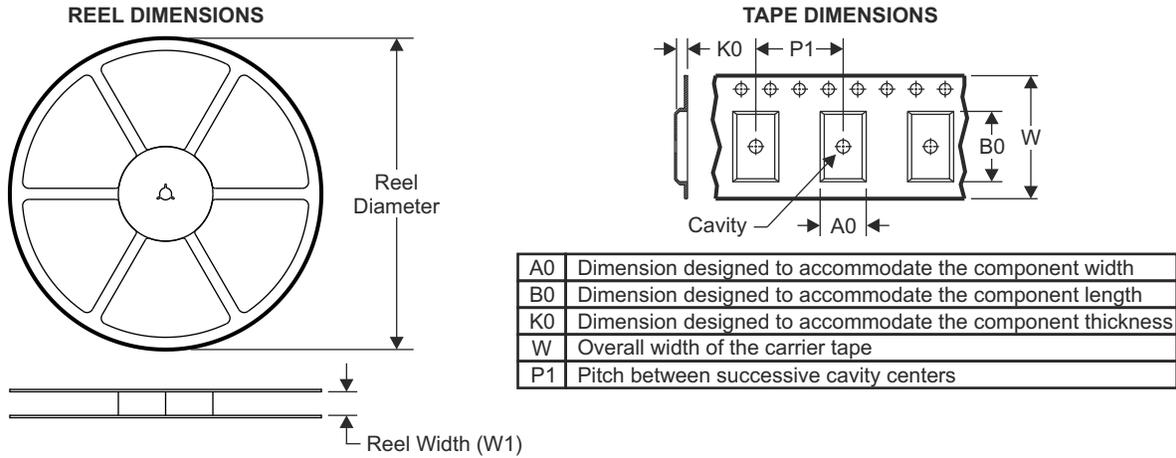
8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

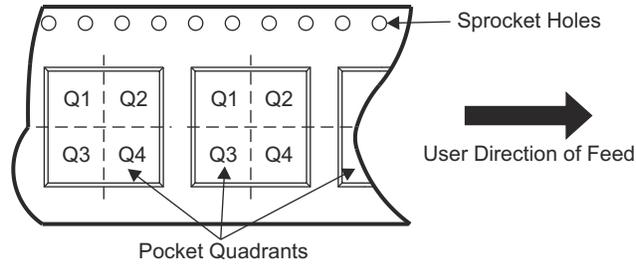
9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Tape and Reel Information

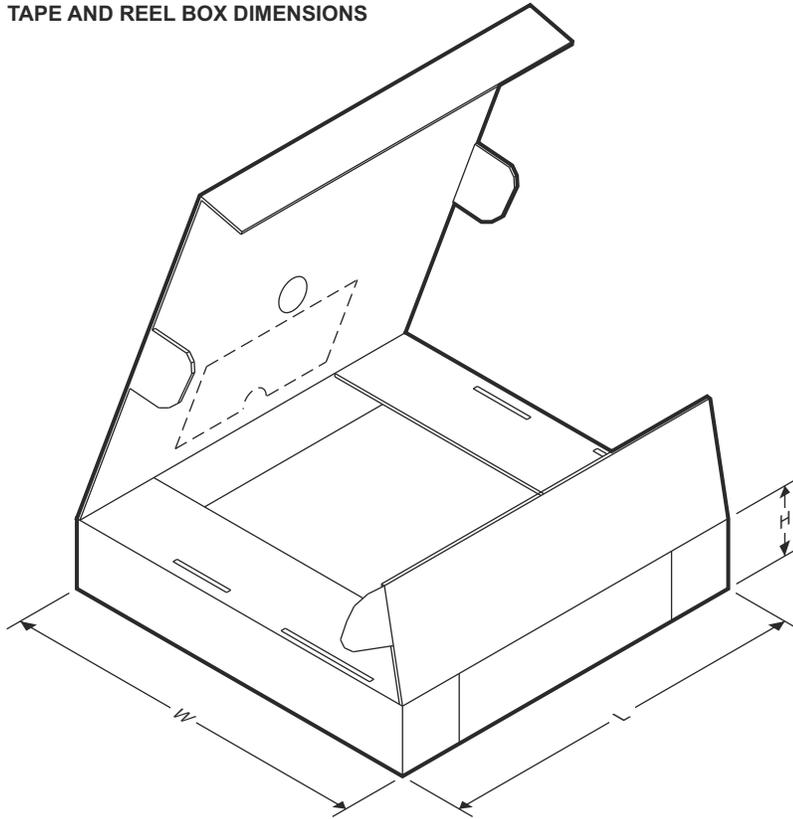


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSD05DYFR	SOD-323	DYF	2	15000	178	8.4	0.36	0.66	0.33	0.2	8	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSD05DYFR	SOD-323	DYF	2	15000	205	200	33

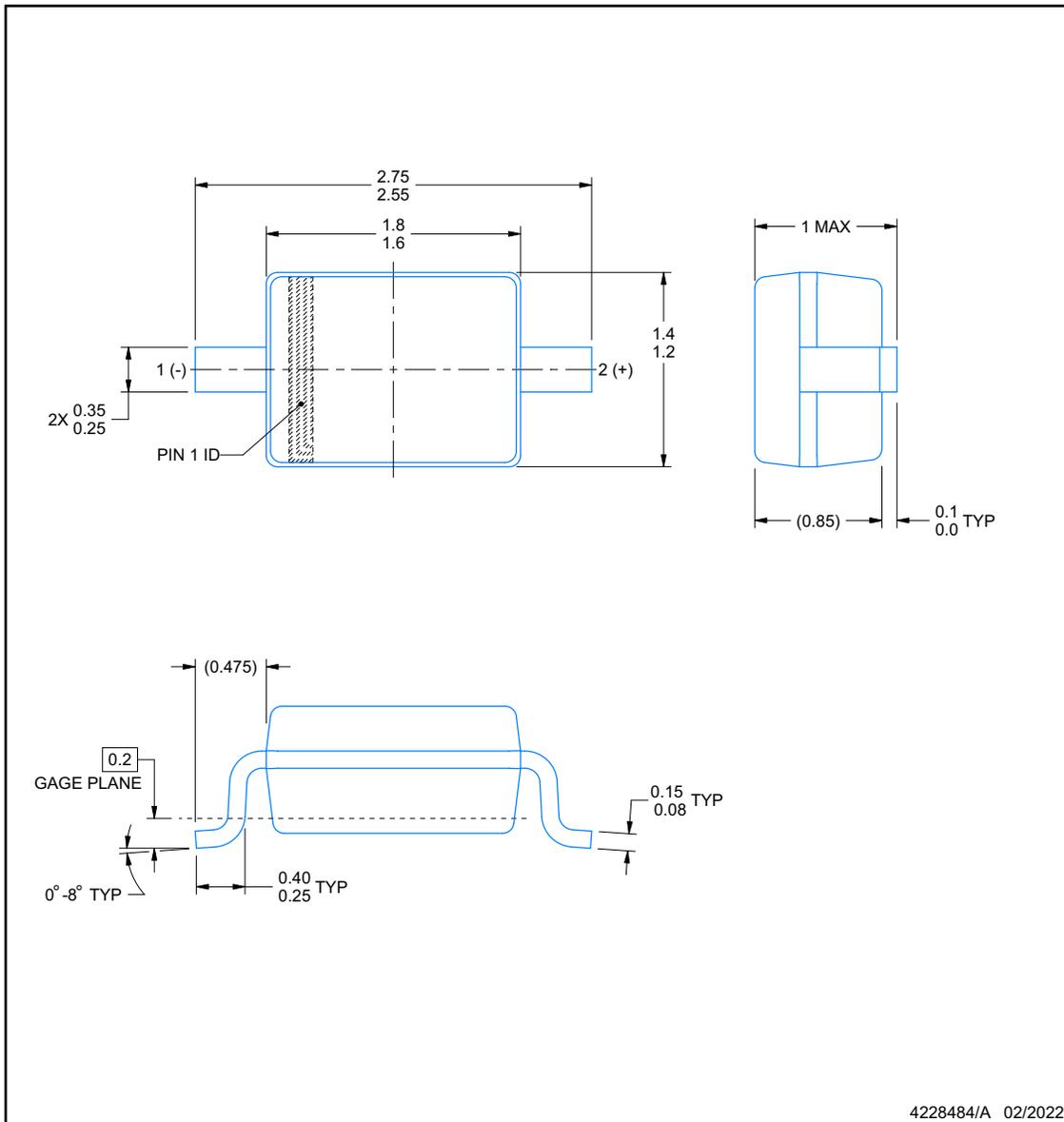
9.2 Mechanical Data



DYF0002A

PACKAGE OUTLINE
SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

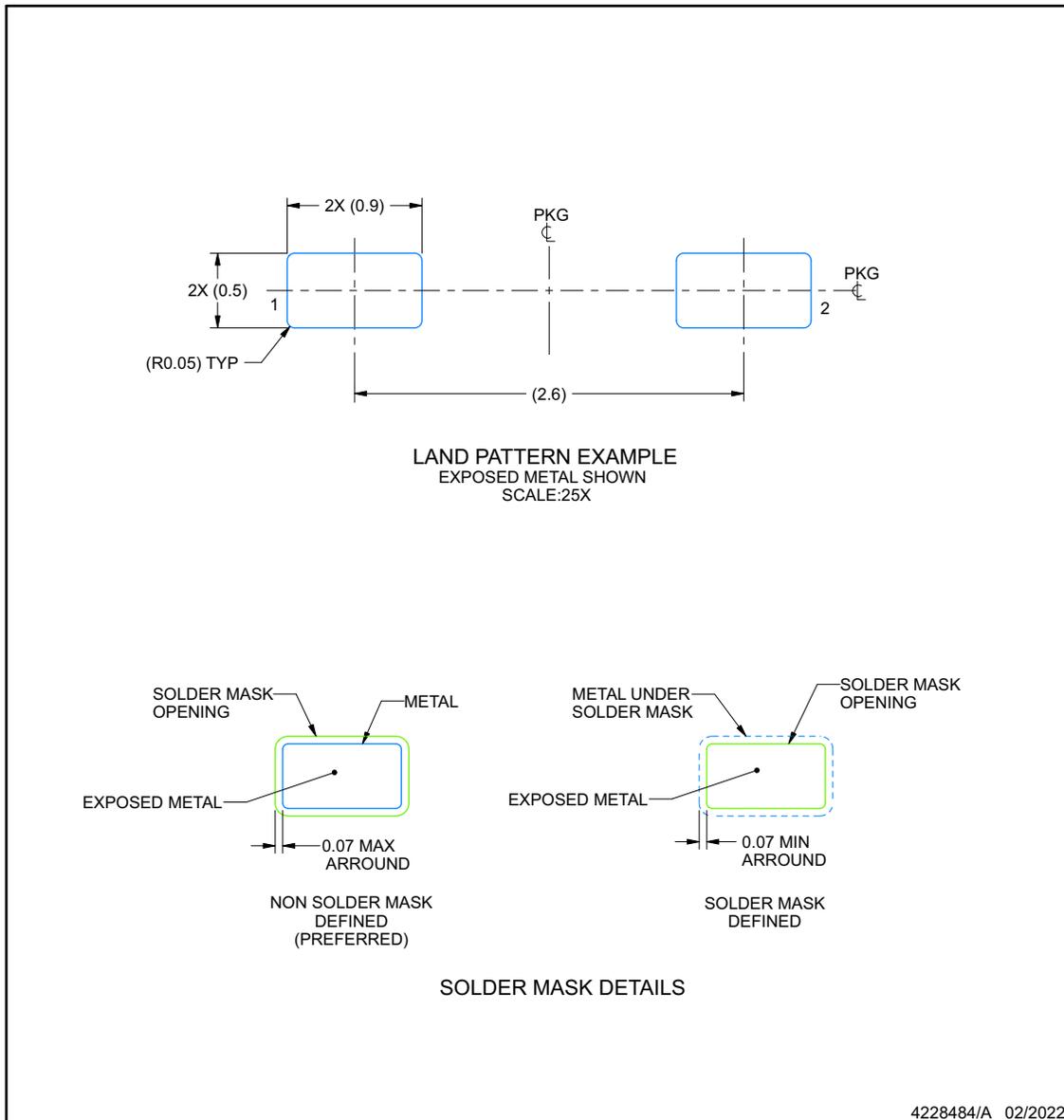
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DYF0002A

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES: (continued)

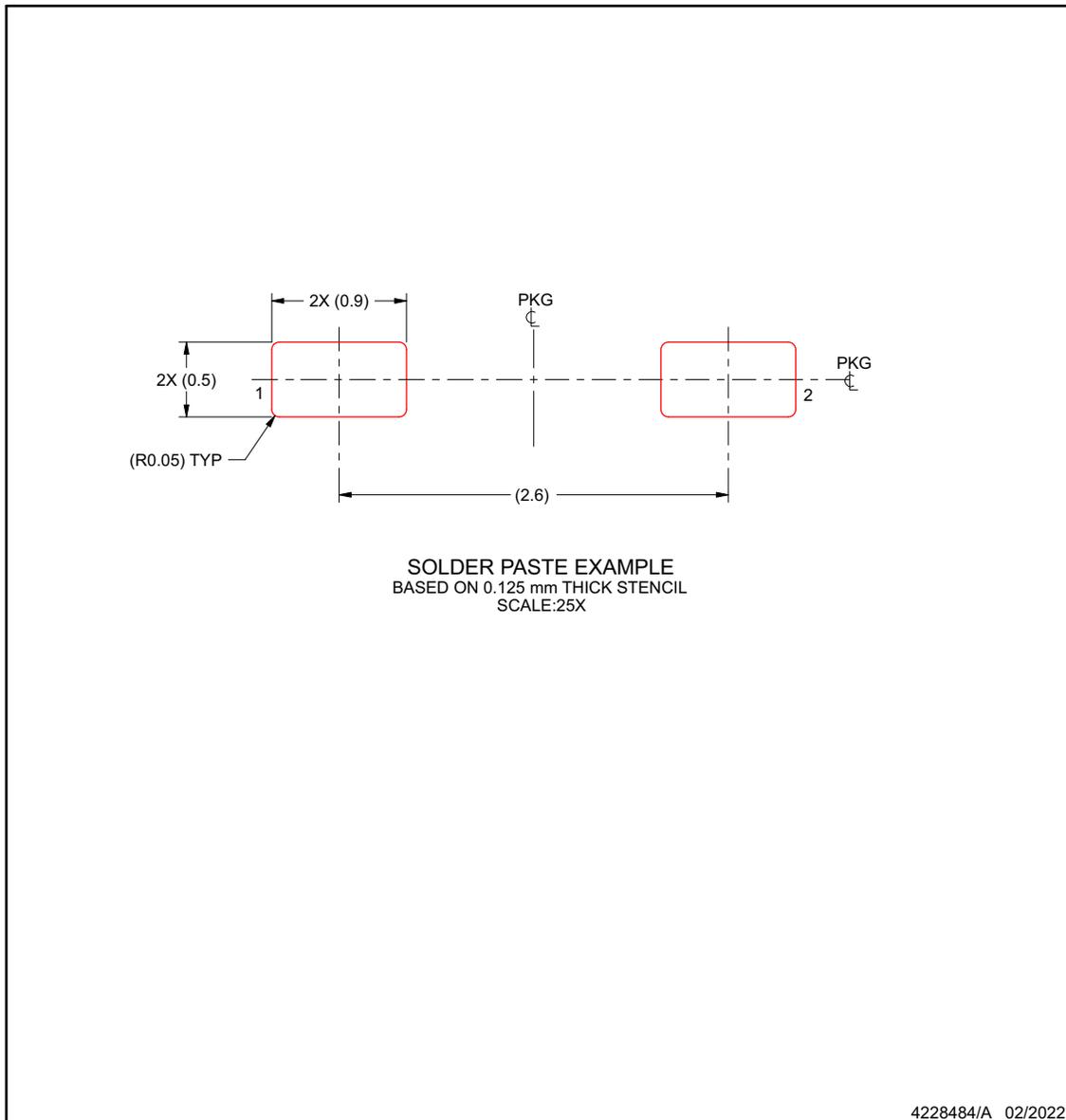
3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYF0002A

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
6. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSD05DYFR	ACTIVE	SOT	DYF	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	33MF	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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