

# TUSB1046A-DCI USB Type-C™ DisplayPort™ ALT Mode 10-Gbps Linear Redriver Crosspoint Switch

## 1 Features

- USB Type-C™ crosspoint switch supporting
  - USB 3.1 SSP + 2 DisplayPort lanes
  - 4 DisplayPort™ lanes
- USB 3.1 Gen 1/Gen 2 up to 10 Gbps
- DisplayPort 1.4 up to 8.1 Gbps (HBR3)
- VESA® DisplayPort alt mode DFP redriving crosspoint switch supporting c, d, e and f configurations
- Ultra-low-power architecture
- Linear redriver with up to 14 dB equalization
- Transparent to DisplayPort link training
- Automatic LFPS de-emphasis control to meet USB 3.1 certification requirements
- Configuration through GPIO or I<sup>2</sup>C
- Intel proprietary DCI capability on USB Type-C for closed chassis debugging
- Hot-plug capable
- Industrial temperature range: –40°C to 85°C (TUSB1046AI-DCI)
- Commercial temperature range: 0°C to 70°C (TUSB1046-DCI)
- 4 mm x 6 mm, 0.4 mm pitch WQFN package

## 2 Applications

- Tablets
- Notebooks
- Desktops
- Docking stations

## 3 Description

The TUSB1046A-DCI is a VESA USB Type-C™ Alt Mode redriving switch supporting USB 3.1 data rates up to 10 Gbps and DisplayPort 1.4 up to 8.1 Gbps for downstream facing port (Host). The device is used for configurations C, D, E, and F from the VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.1. This protocol-agnostic linear redriver is also capable of supporting other USB Type-C Alt Mode interfaces.

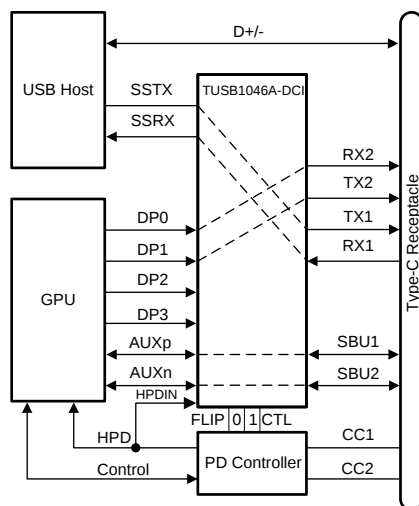
The TUSB1046A-DCI provides several levels of receive linear equalization to compensate for inter-symbol interference (ISI) due to cable and board trace loss. The device operates on a single 3.3-V supply and comes in a commercial temperature range and industrial temperature range.

### Device Information<sup>(1)</sup>

| PART NUMBER    | PACKAGE   | BODY SIZE (NOM)   |
|----------------|-----------|-------------------|
| TUSB1046A-DCI  | WQFN (40) | 4.00 mm x 6.00 mm |
| TUSB1046AI-DCI |           |                   |

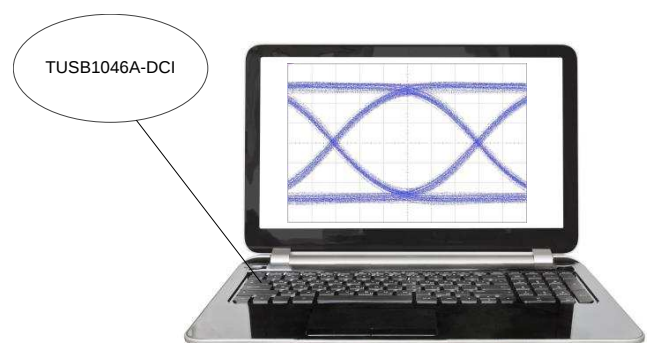
(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Schematics



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### TUSB1046A-DCI Eye Diagram



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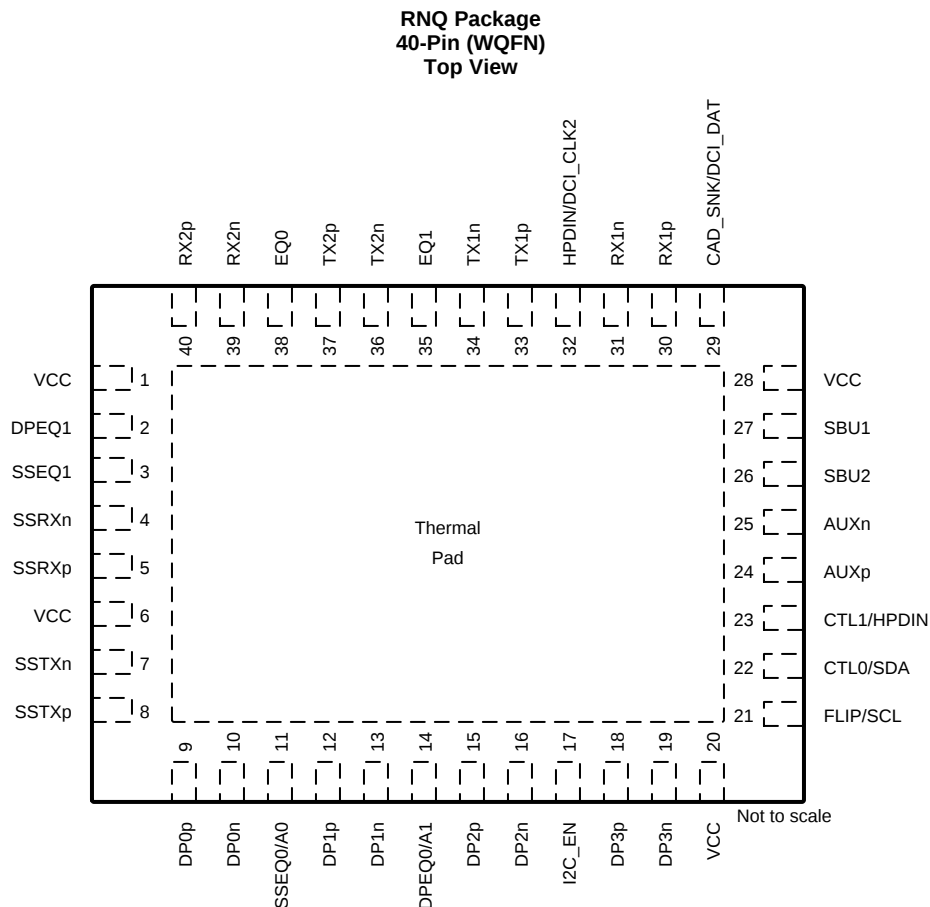
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## 4 Revision History

| Changes from Revision A (April 2018) to Revision B                                                 | Page |
|----------------------------------------------------------------------------------------------------|------|
| • Added following to pin 11 description: If I2C_EN = "F", then this pin must be set to "F" or "0". | 4    |

| Changes from Original (June 2017) to Revision A                                                   | Page |
|---------------------------------------------------------------------------------------------------|------|
| • Changed the appearance of the pinout image in the <i>Pin Configuration and Function</i> section | 3    |
| • Added Note 1 to the <i>Pin Functions</i> table                                                  | 3    |
| • Changed the USB3.1 Control/Status Registers reset value From: 00000000 To: 00000100             | 28   |
| • Changed the Reset value of bit 3:2 From: 00 To: 01 in <a href="#">Table 18</a>                  | 28   |

## 5 Pin Configuration and Functions



### Pin Functions

| PIN  |     | I/O      | DESCRIPTION                                                                                                    |
|------|-----|----------|----------------------------------------------------------------------------------------------------------------|
| NAME | NO. |          |                                                                                                                |
| DP0p | 9   | Diff I   | DP Differential positive input for DisplayPort Lane 0.                                                         |
| DP0n | 10  | Diff I   | DP Differential negative input for DisplayPort Lane 0.                                                         |
| DP1p | 12  | Diff I   | DP Differential positive input for DisplayPort Lane 1.                                                         |
| DP1n | 13  | Diff I   | DP Differential negative input for DisplayPort Lane 1.                                                         |
| DP2p | 15  | Diff I   | DP Differential positive input for DisplayPort Lane 2.                                                         |
| DP2n | 16  | Diff I   | DP Differential negative input for DisplayPort Lane 2.                                                         |
| DP3p | 18  | Diff I   | DP Differential positive input for DisplayPort Lane 3.                                                         |
| DP3n | 19  | Diff I   | DP Differential negative input for DisplayPort Lane 3.                                                         |
| RX1n | 31  | Diff I/O | Differential negative output for DisplayPort or differential negative input for USB3.1 Downstream Facing port. |
| RX1p | 30  | Diff I/O | Differential positive output for DisplayPort or differential positive input for USB3.1 Downstream Facing port. |
| TX1n | 34  | Diff O   | Differential negative output for DisplayPort or USB3.1 downstream facing port.                                 |
| TX1p | 33  | Diff O   | Differential positive output for DisplayPort or USB 3.1 downstream facing port.                                |
| TX2p | 37  | Diff O   | Differential positive output for DisplayPort or USB 3.1 downstream facing port.                                |
| TX2n | 36  | Diff O   | Differential negative output for DisplayPort or USB 3.1 downstream facing port.                                |
| RX2p | 40  | Diff I/O | Differential positive output for DisplayPort or differential positive input for USB3.1 Downstream Facing port. |
| RX2n | 39  | Diff I/O | Differential negative output for DisplayPort or differential negative input for USB3.1 Downstream Facing port. |

**Pin Functions (continued)**

| PIN                            |              | I/O                       | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|--------------------------------|--------------|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                           | NO.          |                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| SSTXp                          | 8            | Diff I                    | Differential positive input for USB3.1 upstream facing port.                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| SSTXn                          | 7            | Diff I                    | Differential negative input for USB3.1 upstream facing port.                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| SSRXp                          | 5            | Diff O                    | Differential positive output for USB3.1 upstream facing port.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| SSRXn                          | 4            | Diff O                    | Differential negative output for USB3.1 upstream facing port.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| EQ1                            | 35           | 4 Level I                 | This pin along with EQ0 sets the USB receiver equalizer gain for downstream facing RX1 and RX2 when USB used.                                                                                                                                                                                                                                                                                                                                                                                                                 |
| EQ0                            | 38           | 4 Level I                 | This pin along with EQ1 sets the USB receiver equalizer gain for downstream facing RX1 and RX2 when USB used.                                                                                                                                                                                                                                                                                                                                                                                                                 |
| CAD_SNK/DCI_DAT <sup>(1)</sup> | 29           | I/O (PD)                  | When I2C_EN ! = 0, this pin functions as DCI data output Leave open if not used. When I2C_EN = 0, this pin is CAD_SNK (L = AUX snoop enabled and H = AUX snoop disabled with all lanes active).                                                                                                                                                                                                                                                                                                                               |
| HPDIN/DCI_CLK <sup>(1)</sup>   | 32           | I/O (PD)                  | When I2C_EN ! = 0, this pin functions as DCI clock output Leave open if not used. When I2C_EN = 0, this pin is an input for Hot Plug Detect received from DisplayPort sink. When HPDIN is Low for greater than 2ms, all DisplayPort lanes are disabled while the AUX to SBU switch will remain closed.                                                                                                                                                                                                                        |
| I2C_EN                         | 17           | 4 Level I                 | I <sup>2</sup> C Programming Mode or GPIO Programming Select. I2C is only disabled when this pin is '0'.<br>0 = GPIO mode (I <sup>2</sup> C disabled)<br>R = TI Test Mode (I <sup>2</sup> C enabled at 3.3 V)<br>F = I <sup>2</sup> C enabled at 1.8 V<br>1 = I <sup>2</sup> C enabled at 3.3 V.                                                                                                                                                                                                                              |
| SBU1                           | 27           | I/O, CMOS                 | SBU1. This pin should be DC coupled to the SBU1 pin on the Type-C receptacle. A 2-M ohm resistor to GND is also recommended.                                                                                                                                                                                                                                                                                                                                                                                                  |
| SBU2                           | 26           | I/O, CMOS                 | SBU2. This pin should be DC coupled to the SBU2 pin on the Type-C receptacle. A 2-M ohm resistor to GND is also recommended.                                                                                                                                                                                                                                                                                                                                                                                                  |
| AUXp                           | 24           | I/O, CMOS                 | AUXp. DisplayPort AUX positive I/O connected to the DisplayPort source through a AC coupling capacitor. In addition to AC coupling capacitor, this pin also requires a 100K resistor to GND. This pin along with AUXN is used by the TUSB1046A-DCI for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C.                                                                                                                                                                                           |
| AUXn                           | 25           | I/O, CMOS                 | AUXn. DisplayPort AUX negative I/O connected to the DisplayPort source through a AC coupling capacitor. In addition to AC coupling capacitor, this pin also requires a 100K resistor to DP_PWR (3.3V). This pin along with AUXP is used by the TUSB1046A-DCI for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C.                                                                                                                                                                                 |
| DPEQ1                          | 2            | 4 Level I                 | DisplayPort Receiver EQ. This along with DPEQ0 will select the DisplayPort receiver equalization gain.                                                                                                                                                                                                                                                                                                                                                                                                                        |
| DPEQ0/A1                       | 14           | 4 Level I                 | DisplayPort Receiver EQ. This along with DPEQ1 will select the DisplayPort receiver equalization gain. When I2C_EN is not '0', this pin will also set the TUSB1046A-DCI I <sup>2</sup> C address.                                                                                                                                                                                                                                                                                                                             |
| SSEQ1                          | 3            | 4 Level I                 | Along with SSEQ0, sets the USB receiver equalizer gain for upstream facing SSTXP/N.                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| SSEQ0/A0                       | 11           | 4 Level I                 | Along with SSEQ1, sets the USB receiver equalizer gain for upstream facing SSTXP/N. When I2C_EN is not '0', this pin will also set the TUSB1046A-DCI I <sup>2</sup> C address. If I2C_EN = "F", then this pin must be set to "F" or "0".                                                                                                                                                                                                                                                                                      |
| FLIP/SCL                       | 21           | 2 Level I                 | When I2C_EN='0' this is Flip control pin, otherwise this pin is I <sup>2</sup> C clock. . When used for I <sup>2</sup> C clock pullup to I <sup>2</sup> C master's VCC I2C supply.                                                                                                                                                                                                                                                                                                                                            |
| CTL0/SDA                       | 22           | 2 Level I                 | When I2C_EN='0' this is a USB3.1 Switch control pin, otherwise this pin is I <sup>2</sup> C data. When used for I <sup>2</sup> C data pullup to I <sup>2</sup> C master's VCC I2C supply.                                                                                                                                                                                                                                                                                                                                     |
| CTL1/HPDIN                     | 23           | 2 Level I (Failsafe) (PD) | DP Alt mode Switch Control Pin. When I2C_EN = '0', this pin will enable or disable DisplayPort functionality. Otherwise, when I2C_EN is not "0", DisplayPort functionality is enabled and disabled through I <sup>2</sup> C registers.<br>L = DisplayPort Disabled.<br>H = DisplayPort Enabled.<br>When I2C_EN is not "0" this pin is an input for Hot Plug Detect received from DisplayPort sink. When this HPDIN is Low for greater than 2 ms, all DisplayPort lanes are disabled and AUX to SBU switch will remain closed. |
| VCC                            | 1, 6, 20, 28 | P                         | 3.3-V Power Supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Thermal Pad                    |              | G                         | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

(1) Not a fail-safe I/O. Actively driving pin high while VCC is removed results in leakage voltage on VCC pins.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                |                                                           | MIN  | MAX            | UNIT |
|------------------------------------------------|-----------------------------------------------------------|------|----------------|------|
| Supply Voltage Range <sup>(2)</sup> , $V_{CC}$ |                                                           | –0.3 | 4              | V    |
| Voltage Range at any input or output pin       | Differential voltage between positive and negative inputs |      | ±2.5           | V    |
|                                                | Voltage at differential inputs                            | –0.5 | $V_{CC} + 0.5$ | V    |
|                                                | CMOS Inputs                                               | –0.5 | $V_{CC} + 0.5$ | V    |
| Maximum junction temperature, $T_J$            |                                                           |      | 125            | °C   |
| Storage temperature, $T_{stg}$                 |                                                           | –65  | 150            | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND terminals.

### 6.2 ESD Ratings

|                                     |                                                                                | VALUE | UNIT |
|-------------------------------------|--------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±5000 | V    |
|                                     | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1500 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|             |                                                                | MIN            | NOM | MAX | UNIT |
|-------------|----------------------------------------------------------------|----------------|-----|-----|------|
| $V_{CC}$    | Main power supply                                              | 3              | 3.3 | 3.6 | V    |
|             | Supply Ramp Requirement                                        |                |     | 100 | ms   |
| $V_{(12C)}$ | Supply that external resistors are pulled up to on SDA and SCL | 1.7            |     | 3.6 | V    |
| $V_{(PSN)}$ | Supply Noise on $V_{CC}$ pins                                  |                |     | 100 | mV   |
| $T_A$       | Operating free-air temperature                                 | TUSB1046A-DCI  |     | 0   | °C   |
|             |                                                                | TUSB1046AI-DCI |     | –40 | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TUSB1046A-DCI | UNIT |
|-------------------------------|----------------------------------------------|---------------|------|
|                               |                                              | RNQ (WQFN)    |      |
|                               |                                              | 40 PINS       |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 37.6          | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 20.7          | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 9.5           | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 0.2           | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 9.4           | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | 2.3           | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Power Supply Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                |                                      | TEST CONDITIONS                                                                                                                               | MIN | TYP  | MAX | UNIT |
|--------------------------|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|------|
| $P_{CC(Active-USB)}$     | Average active power USB Only        | Link in U0 with GEN2 data transmission. EN, EQ cntrl pins = NC, k28.5 pattern at 10 Gbps, $V_{ID} = 1000\text{ mV}_{PP}$ ; CTL1 = L; CTL0 = H |     | 335  |     | mW   |
| $P_{CC(Active-USB-DP1)}$ | Average active power USB + 2 Lane DP | Link in U0 with GEN2 data transmission. EN, EQ cntrl pins = NC, k28.5 pattern at 10 Gbps, $V_{ID} = 1000\text{ mV}_{PP}$ ; CTL1 = H; CTL0 = H |     | 634  |     | mW   |
| $P_{CC(Active-DP)}$      | Average active power 4 Lane DP Only  | Four active DP lanes operating at 8.1Gbps; CTL1 = H; CTL0 = L;                                                                                |     | 660  |     | mW   |
| $P_{CC(NC-USB)}$         | Average power with no connection     | No GEN1 device is connected to TXP/TXN; CTL1 = L; CTL0 = H;                                                                                   |     | 2.4  |     | mW   |
| $P_{CC(U2U3)}$           | Average power in U2/U3               | Link in U2 or U3 USB Mode Only; CTL1 = L; CTL0 = H;                                                                                           |     | 3    |     | mW   |
| $P_{CC(Shutdown)}$       | Device Shutdown                      | CTL1 = L; CTL0 = L; I2C_EN = 0;                                                                                                               |     | 0.85 |     | mW   |

## 6.6 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                                                      |                                                                        | TEST CONDITIONS                                              | MIN                    | TYP                    | MAX  | UNIT          |
|------------------------------------------------------------------------------------------------|------------------------------------------------------------------------|--------------------------------------------------------------|------------------------|------------------------|------|---------------|
| <b>4-State CMOS Inputs(EQ[1:0], SSEQ[1:0], DPEQ[1:0], I2C_EN)</b>                              |                                                                        |                                                              |                        |                        |      |               |
| $I_{IH}$                                                                                       | High level input current                                               | $V_{CC} = 3.6\text{ V}$ ; $V_{IN} = 3.6\text{ V}$            | 20                     |                        | 80   | $\mu\text{A}$ |
| $I_{IL}$                                                                                       | Low level input current                                                | $V_{CC} = 3.6\text{ V}$ ; $V_{IN} = 0\text{ V}$              | -160                   |                        | -40  | $\mu\text{A}$ |
| 4-Level $V_{TH}$                                                                               | Threshold 0 / R                                                        | $V_{CC} = 3.3\text{ V}$                                      |                        | 0.55                   |      | V             |
|                                                                                                | Threshold R/ Float                                                     | $V_{CC} = 3.3\text{ V}$                                      |                        | 1.65                   |      | V             |
|                                                                                                | Threshold Float / 1                                                    | $V_{CC} = 3.3\text{ V}$                                      |                        | 2.7                    |      | V             |
| $R_{PU}$                                                                                       | Internal pull-up resistance                                            |                                                              |                        | 35                     |      | k $\Omega$    |
| $R_{PD}$                                                                                       | Internal pull-down resistance                                          |                                                              |                        | 95                     |      | k $\Omega$    |
| <b>2-State CMOS Input (CTL0, CTL1, FLIP, CAD_SNK, HPDIN) CTL1, CTL0 and FLIP are Failsafe.</b> |                                                                        |                                                              |                        |                        |      |               |
| $V_{IH}$                                                                                       | High-level input voltage                                               |                                                              | 2                      |                        | 3.6  | V             |
| $V_{IL}$                                                                                       | Low-level input voltage                                                |                                                              | 0                      |                        | 0.8  | V             |
| $R_{PD}$                                                                                       | Internal pull-down resistance for CTL1                                 |                                                              |                        | 500                    |      | k $\Omega$    |
| $R_{(ENPD)}$                                                                                   | Internal pull-down resistance for CAD_SNK (pin 29), and HPDIN (pin 32) |                                                              |                        | 150                    |      | k $\Omega$    |
| $I_{IH}$                                                                                       | High-level input current                                               | $V_{IN} = 3.6\text{ V}$                                      | -25                    |                        | 25   | $\mu\text{A}$ |
| $I_{IL}$                                                                                       | Low-level input current                                                | $V_{IN} = \text{GND}$ , $V_{CC} = 3.6\text{ V}$              | -25                    |                        | 25   | $\mu\text{A}$ |
| <b>I<sup>2</sup>C Control Pins SCL, SDA</b>                                                    |                                                                        |                                                              |                        |                        |      |               |
| $V_{IH}$                                                                                       | High-level input voltage                                               | I2C_EN = 0                                                   | $0.7 \times V_{(I2C)}$ |                        | 3.6  | V             |
| $V_{IL}$                                                                                       | Low-level input voltage                                                | I2C_EN = 0                                                   | 0                      | $0.3 \times V_{(I2C)}$ |      | V             |
| $V_{OL}$                                                                                       | Low-level output voltage                                               | I2C_EN = 0; $I_{OL} = 3\text{ mA}$                           | 0                      |                        | 0.4  | V             |
| $I_{OL}$                                                                                       | Low-level output current                                               | I2C_EN = 0; $V_{OL} = 0.4\text{ V}$                          | 20                     |                        |      | mA            |
| $I_{I(I2C)}$                                                                                   | Input current on SDA pin                                               | $0.1 \times V_{(I2C)} < \text{Input voltage} < 3.3\text{ V}$ | -10                    |                        | 10   | $\mu\text{A}$ |
| $C_{I(I2C)}$                                                                                   | Input capacitance                                                      |                                                              |                        |                        | 10   | pF            |
| $C_{(I2C\_FM+\_BUS)}$                                                                          | I2C bus capacitance for FM+ (1MHz)                                     |                                                              |                        |                        | 150  | pF            |
| $C_{(I2C\_FM\_BUS)}$                                                                           | I2C bus capacitance for FM (400kHz)                                    |                                                              |                        |                        | 150  | pF            |
| $R_{(EXT\_I2C\_FM+)}$                                                                          | External resistors on both SDA and SCL when operating at FM+ (1MHz)    | $C_{(I2C\_FM+\_BUS)} = 150\text{ pF}$                        | 620                    | 820                    | 910  | $\Omega$      |
| $R_{(EXT\_I2C\_FM)}$                                                                           | External resistors on both SDA and SCL when operating at FM (400kHz)   | $C_{(I2C\_FM\_BUS)} = 150\text{ pF}$                         | 620                    | 1500                   | 2200 | $\Omega$      |

## 6.7 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                           | TEST CONDITIONS                                                                               | MIN                                                      | TYP        | MAX  | UNIT       |
|---------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|----------------------------------------------------------|------------|------|------------|
| <b>USB Gen 2 Differential Receiver (RX1P/N, RX2P/N, SSTXP/N)</b>    |                                                                                               |                                                          |            |      |            |
| $V_{(RX-DIFF-PP)}$                                                  | Input differential peak-peak voltage swing linear dynamic range                               |                                                          | 2000       |      | mVpp       |
| $V_{(RX-DC-CM)}$                                                    | Common-mode voltage bias in the receiver (DC)                                                 |                                                          | 0          |      | V          |
| $R_{(RX-DIFF-DC)}$                                                  | Differential input impedance (DC)                                                             | 72                                                       |            | 120  | $\Omega$   |
| $R_{(RX-CM-DC)}$                                                    | Receiver DC common mode impedance                                                             | 18                                                       |            | 30   | $\Omega$   |
| $Z_{(RX-HIGH-IMP-DC-POS)}$                                          | Common-mode input impedance with termination disabled (DC)                                    | 25                                                       |            |      | k $\Omega$ |
| $V_{(SIGNAL-DET-DIFF-PP)}$                                          | Input differential peak-to-peak signal detect assert level                                    |                                                          | 80         |      | mV         |
| $V_{(RX-IDLE-DET-DIFF-PP)}$                                         | Input differential peak-to-peak signal detect de-assert Level                                 |                                                          | 60         |      | mV         |
| $V_{(RX-LFPS-DET-DIFF-PP)}$                                         | Low frequency periodic signaling (LFPS) detect threshold                                      | 100                                                      |            | 300  | mV         |
| $V_{(RX-CM-AC-P)}$                                                  | Peak RX AC common-mode voltage                                                                |                                                          |            | 150  | mV         |
| $C_{(RX)}$                                                          | RX input capacitance to GND                                                                   |                                                          | 0.5        | 1    | pF         |
| $R_{L(RX-DIFF)}$                                                    | Differential return Loss                                                                      | 50 MHz – 1.25 GHz at 90 $\Omega$<br>5 GHz at 90 $\Omega$ | -19<br>-10 |      | dB         |
| $R_{L(RX-CM)}$                                                      | Common-mode return loss                                                                       | 50 MHz – 5 GHz at 90 $\Omega$                            | -10        |      | dB         |
| $E_{Q(SS\_TX)}$                                                     | Receiver equalization for upstream facing port                                                | SSEQ[1:0] at 5 GHz                                       | 11         |      | dB         |
| $E_{Q(SS\_RX)}$                                                     | Receiver equalization for downstream facing ports                                             | EQ[1:0] at 5 GHz                                         | 9          |      | dB         |
| <b>USB Gen 2 Differential Transmitter (TX1P/N, TX2P/N, SSRXP/N)</b> |                                                                                               |                                                          |            |      |            |
| $V_{TX(DIFF-PP)}$                                                   | Transmitter dynamic differential voltage swing range.                                         |                                                          | 1600       |      | mVpp       |
| $V_{TX(RCV-DETECT)}$                                                | Amount of voltage change allowed during receiver detection                                    |                                                          |            | 600  | mV         |
| $V_{TX(CM-IDLE-DELTA)}$                                             | Transmitter idle common-mode voltage change while in U2/U3 and not actively transmitting LFPS | -600                                                     |            | 600  | mV         |
| $V_{TX(DC-CM)}$                                                     | Common-mode voltage bias in the transmitter (DC)                                              |                                                          | 1.75       |      | V          |
| $V_{TX(CM-AC-PP-ACTIVE)}$                                           | Tx AC common-mode voltage active                                                              |                                                          |            | 100  | mVpp       |
| $V_{TX(IDLE-DIFF-AC-PP)}$                                           | AC electrical idle differential peak-to-peak output voltage                                   | 0                                                        |            | 10   | mV         |
| $V_{TX(IDLE-DIFF-DC)}$                                              | DC electrical idle differential output voltage                                                | 0                                                        |            | 14   | mV         |
| $V_{TX(CM-DC-ACTIVE-IDLE-DELTA)}$                                   | Absolute DC common-mode voltage between U1 and U0                                             |                                                          |            | 200  | mV         |
| $R_{TX(DIFF)}$                                                      | Differential impedance of the driver                                                          | 75                                                       |            | 120  | $\Omega$   |
| $C_{AC(COUPLING)}$                                                  | AC coupling capacitor                                                                         | 75                                                       |            | 265  | nF         |
| $R_{TX(CM)}$                                                        | Common-mode impedance of the driver                                                           | 18                                                       |            | 30   | $\Omega$   |
| $I_{TX(SHORT)}$                                                     | TX short circuit current                                                                      |                                                          |            | 67   | mA         |
| $C_{TX(PARASITIC)}$                                                 | TX input capacitance for return loss                                                          |                                                          |            | 1.25 | pF         |
| $R_{LTX(DIFF)}$                                                     | Differential return loss                                                                      | 50 MHz – 1.25 GHz at 90 $\Omega$<br>5 GHz at 90 $\Omega$ | -15<br>-13 |      | dB         |
| $R_{LTX(CM)}$                                                       | Common-mode return loss                                                                       | 50 MHz – 5 GHz at 90 $\Omega$                            | -13        |      | dB         |
| <b>AC Characteristics</b>                                           |                                                                                               |                                                          |            |      |            |
| Crosstalk                                                           | Differential crosstalk between TX and RX signal pairs                                         | at 5 GHz                                                 |            | -30  | dB         |
| $C_{(P1dB-LF)}$                                                     | Low frequency 1-dB compression point                                                          | at 100 MHz, 200 mVpp < $V_{ID}$<br>< 2000 mVpp           |            | 1300 | mVpp       |

## AC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                                        |                                                                                      | TEST CONDITIONS                                                                                         | MIN | TYP   | MAX | UNIT             |
|----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|-----|-------|-----|------------------|
| C <sub>(P1dB-HF)</sub>                                                           | High frequency 1-dB compression point                                                | at 5 GHz, 200 mV <sub>PP</sub> < V <sub>ID</sub> < 2000 mV <sub>PP</sub>                                |     | 1000  |     | mV <sub>PP</sub> |
| f <sub>LF</sub>                                                                  | Low frequency cutoff                                                                 | 200 mV <sub>PP</sub> < V <sub>ID</sub> < 2000 mV <sub>PP</sub>                                          |     | 20    | 50  | kHz              |
|                                                                                  | TX output deterministic jitter                                                       | 200 mV <sub>PP</sub> < V <sub>ID</sub> < 2000 mV <sub>PP</sub> , PRBS7, 10 Gbps                         |     | 0.11  |     | UIpp             |
|                                                                                  |                                                                                      | 200 mV <sub>PP</sub> < V <sub>ID</sub> < 2000 mV <sub>PP</sub> , PRBS7, 8.1 Gbps                        |     | 0.08  |     | UIpp             |
|                                                                                  | TX output total jitter                                                               | 200 mV <sub>PP</sub> < V <sub>ID</sub> < 2000 mV <sub>PP</sub> , PRBS7, 10 Gbps                         |     | 0.15  |     | UIpp             |
|                                                                                  |                                                                                      | 200 mV <sub>PP</sub> < V <sub>ID</sub> < 2000 mV <sub>PP</sub> , PRBS7, 8.1 Gbps                        |     | 0.135 |     | UIpp             |
| DisplayPort Receiver (DP[3:0]p or DP[3:0]n)                                      |                                                                                      |                                                                                                         |     |       |     |                  |
| V <sub>ID(PP)</sub>                                                              | Peak-to-peak input differential dynamic voltage range                                |                                                                                                         |     | 2000  |     | V                |
| V <sub>IC</sub>                                                                  | Input common mode voltage                                                            |                                                                                                         |     | 0     |     | V                |
| C <sub>(AC)</sub>                                                                | AC coupling capacitance                                                              |                                                                                                         | 75  |       | 200 | nF               |
| E <sub>Q(DP)</sub>                                                               | Receiver equalization                                                                | DPEQ[1:0] at 4.05 GHz                                                                                   |     |       | 14  | dB               |
| d <sub>R</sub>                                                                   | Data rate                                                                            | HBR3                                                                                                    |     |       | 8.1 | Gbps             |
| R <sub>(ti)</sub>                                                                | Input termination resistance                                                         |                                                                                                         | 80  | 100   | 120 | Ω                |
| DisplayPort Transmitter (TX1p or TX1n, TX2p or TX2n, RX1p or RX1n, RX2p or RX2n) |                                                                                      |                                                                                                         |     |       |     |                  |
| I <sub>TX(SHORT)</sub>                                                           | TX short circuit current                                                             | TX± shorted to GND                                                                                      |     |       | 67  | mA               |
| V <sub>TX(DC-CM)</sub>                                                           | Common-mode voltage bias in the transmitter (DC)                                     |                                                                                                         |     | 1.75  |     | V                |
| AUXp or AUXn and SBU1 or SBU2                                                    |                                                                                      |                                                                                                         |     |       |     |                  |
| R <sub>ON</sub>                                                                  | Output ON resistance                                                                 | V <sub>CC</sub> = 3.3V; V <sub>I</sub> = 0 to 0.4 V for AUXp; V <sub>I</sub> = 2.7 V to 3.6 V for AUXn  |     | 5     | 10  | Ω                |
| ΔR <sub>ON</sub>                                                                 | ON resistance mismatch within pair                                                   | V <sub>CC</sub> = 3.3 V; V <sub>I</sub> = 0 to 0.4 V for AUXP; V <sub>I</sub> = 2.7 V to 3.6 V for AUXN |     |       | 2.5 | Ω                |
| R <sub>ON(FLAT)</sub>                                                            | ON resistance flatness (RON max – RON min) measured at identical VCC and temperature | V <sub>CC</sub> = 3.3 V; V <sub>I</sub> = 0 to 0.4 V for AUXp; V <sub>I</sub> = 2.7 V to 3.6 V for AUXn |     |       | 2   | Ω                |
| V <sub>(AUXP_DC_CM)</sub>                                                        | AUX Channel DC common mode voltage for AUXp and SBU1.                                | V <sub>CC</sub> = 3.3 V                                                                                 | 0   |       | 0.4 | V                |
| V <sub>(AUXN_DC_CM)</sub>                                                        | AUX Channel DC common mode voltage for AUXn and SBU2                                 | V <sub>CC</sub> = 3.3 V                                                                                 | 2.7 |       | 3.6 | V                |
| C <sub>(AUX_ON)</sub>                                                            | ON-state capacitance                                                                 | V <sub>CC</sub> = 3.3 V; CTL1 = 1; V <sub>I</sub> = 0 V or 3.3 V                                        |     | 4     | 7   | pF               |
| C <sub>(AUX_OFF)</sub>                                                           | OFF-state capacitance                                                                | V <sub>CC</sub> = 3.3 V; CTL1 = 0; V <sub>I</sub> = 0 V or 3.3 V                                        |     | 3     | 6   | pF               |

## 6.8 DCI Specific Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                 |                                            | TEST CONDITIONS                                                       | MIN  | TYP | MAX  | UNIT |
|-------------------------------------------|--------------------------------------------|-----------------------------------------------------------------------|------|-----|------|------|
| <b>DCI_CLK and DCI_DAT LVCMOS Outputs</b> |                                            |                                                                       |      |     |      |      |
| $V_{OL}$                                  | Low-Level output voltage                   | $V_{CC} = 3\text{ V}$ ; $I_{OL} = 2\text{ mA}$ ; $C_L = 10\text{ pF}$ |      |     | 0.45 | V    |
| $V_{OH}$                                  | High-Level output voltage                  | $V_{CC} = 3\text{ V}$ ; $I_{OL} = -2\text{ mA}$ ;                     | 2.4  |     |      | V    |
| $R_{DCI}$                                 | Output characteristic impedance            |                                                                       | 21   | 25  | 33   | Ω    |
| $t_{PERIOD}$                              | DCI Clock period                           | Measured at 50%                                                       | 6.67 |     |      | ns   |
| $t_{VALID}$                               | Rising edge of DCI clock to DCI data valid |                                                                       |      |     | 1    | ns   |
| $t_{DCI\_RISE}$                           | DCI output rise time                       | Measured at 20% to 80%.                                               | 350  |     |      | ps   |
| $t_{DCI\_FALL}$                           | DCI output fall time                       | Measured at 80% to 20%                                                | 350  |     |      | ps   |

## 6.9 Timing Requirements

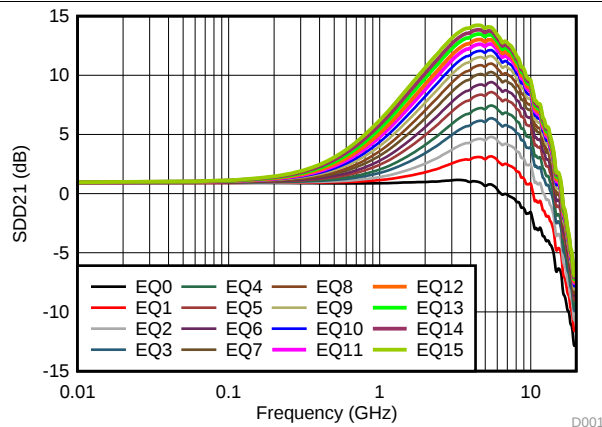
|                      |                                                                     |                                                                       | MIN | NOM | MAX | UNIT |
|----------------------|---------------------------------------------------------------------|-----------------------------------------------------------------------|-----|-----|-----|------|
| <b>USB Gen 1</b>     |                                                                     |                                                                       |     |     |     |      |
| $t_{IDLEEntry}$      | Delay from U0 to electrical idle                                    | See Figure 14                                                         |     | 10  |     | ns   |
| $t_{IDLEExit\_U1}$   | U1 exist time: break in electrical idle to the transmission of LFPS | See Figure 14                                                         |     | 6   |     | ns   |
| $t_{IDLEExit\_U2U3}$ | U2/U3 exit time: break in electrical idle to transmission of LFPS   |                                                                       |     | 10  |     | μs   |
| $t_{RXDET\_INTVL}$   | RX detect interval while in Disconnect                              |                                                                       |     |     | 12  | ms   |
| $t_{IDLEExit\_DISC}$ | Disconnect Exit Time                                                |                                                                       |     | 10  |     | μs   |
| $t_{Exit\_SHTDN}$    | Shutdown Exit Time                                                  |                                                                       |     | 1   |     | ms   |
| $t_{DIFF\_DLY}$      | Differential Propagation Delay                                      | See Figure 13                                                         |     |     | 300 | ps   |
| $t_R, t_F$           | Output Rise/Fall time (see Figure 15)                               | 20%-80% of differential voltage measured 1.7 inch from the output pin |     | 35  |     | ps   |
| $t_{RF\_MM}$         | Output Rise/Fall time mismatch                                      | 20%-80% of differential voltage measured 1.7 inch from the output pin |     |     | 2.6 | ps   |

## 6.10 Switching Characteristics

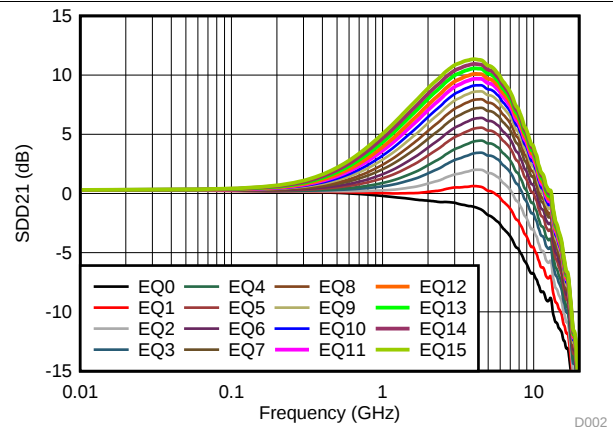
over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                           |                                                                                                                  | TEST CONDITIONS              | MIN  | TYP | MAX | UNIT |
|---------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|------------------------------|------|-----|-----|------|
| <b>AUXp or AUXn and SBU1 or SBU2</b>                                |                                                                                                                  |                              |      |     |     |      |
| $t_{AUX\_PD}$                                                       | Switch propagation delay                                                                                         |                              |      |     | 400 | ps   |
| $t_{AUX\_SW\_OFF}$                                                  | Switching time CTL1 to switch OFF. Not including TCTL1_DEBOUNCE.                                                 |                              |      |     | 500 | ns   |
| $t_{AUX\_SW\_ON}$                                                   | Switching time CTL1 to switch ON                                                                                 |                              |      |     | 500 | ns   |
| $t_{AUX\_INTRA}$                                                    | Intra-pair output skew                                                                                           |                              |      |     | 100 | ps   |
| <b>USB3.1 and DisplayPort mode transition requirement GPIO mode</b> |                                                                                                                  |                              |      |     |     |      |
| $t_{GP\_USB\_4DP}$                                                  | Min overlap of CTL0 and CTL1 when transitioning from USB 3.1 only mode to 4-Lane DisplayPort mode or vice versa. |                              | 4    |     |     | μs   |
| <b>CTL1 and HPDIN</b>                                               |                                                                                                                  |                              |      |     |     |      |
| $t_{CTL1\_DEBOUNCE}$                                                | CTL1 and HPDIN debounce time when transitioning from H to L.                                                     |                              | 2    |     | 10  | ms   |
| <b>I<sup>2</sup>C (Refer to Figure 11)</b>                          |                                                                                                                  |                              |      |     |     |      |
| $f_{SCL}$                                                           | I <sup>2</sup> C clock frequency                                                                                 |                              |      |     | 1   | MHz  |
| $t_{BUF}$                                                           | Bus free time between START and STOP conditions                                                                  |                              | 0.5  |     |     | μs   |
| $t_{HDSTA}$                                                         | Hold time after repeated START condition. After this period, the first clock pulse is generated                  |                              | 0.26 |     |     | μs   |
| $t_{LOW}$                                                           | Low period of the I <sup>2</sup> C clock                                                                         |                              | 0.5  |     |     | μs   |
| $t_{HIGH}$                                                          | High period of the I <sup>2</sup> C clock                                                                        |                              | 0.26 |     |     | μs   |
| $t_{SUSTA}$                                                         | Setup time for a repeated START condition                                                                        |                              | 0.26 |     |     | μs   |
| $t_{HDDAT}$                                                         | Data hold time                                                                                                   |                              | 0    |     |     | μs   |
| $t_{SUDAT}$                                                         | Data setup time                                                                                                  |                              | 50   |     |     | ns   |
| $t_R$                                                               | Rise time of both SDA and SCL signals                                                                            |                              |      |     | 120 | ns   |
| $t_F$                                                               | Fall time of both SDA and SCL signals                                                                            | $20 \times (V_{(I2C)}/5.5V)$ |      |     | 120 | ns   |
| $t_{SUSTO}$                                                         | Setup time for STOP condition                                                                                    |                              | 0.26 |     |     | μs   |
| $C_b$                                                               | Capacitive load for each bus line                                                                                |                              |      |     | 150 | pF   |

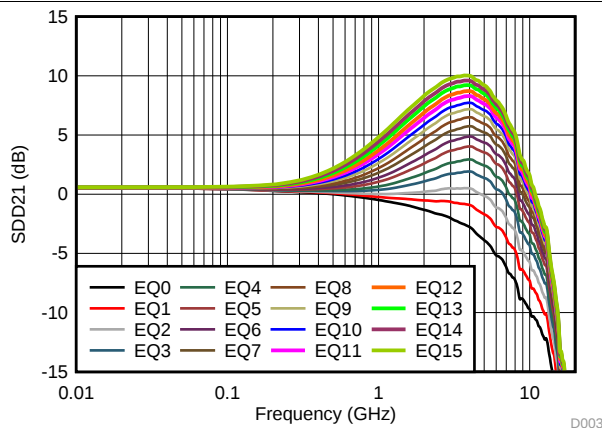
## 6.11 Typical Characteristics



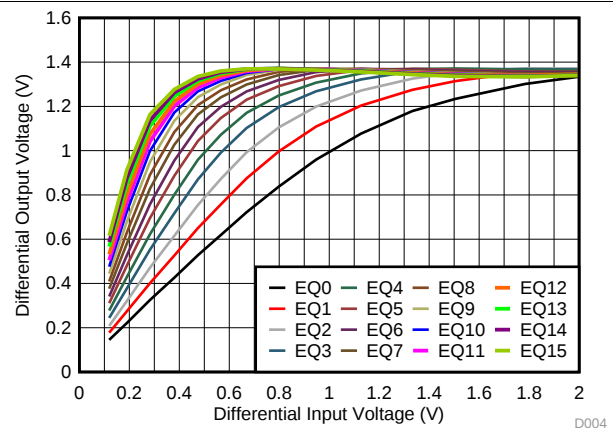
**Figure 1. DisplayPort EQ Settings Curves**



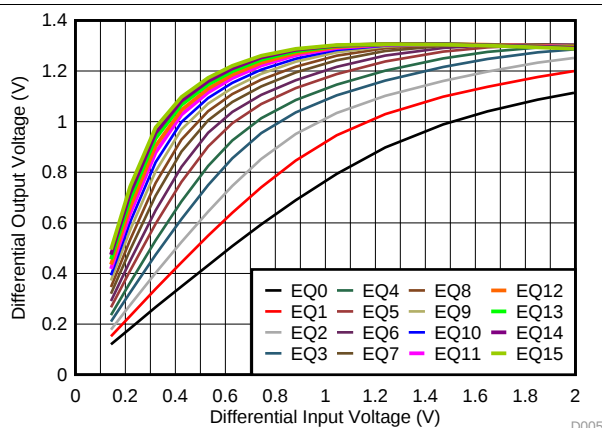
**Figure 2. USB RX EQ Settings Curves**



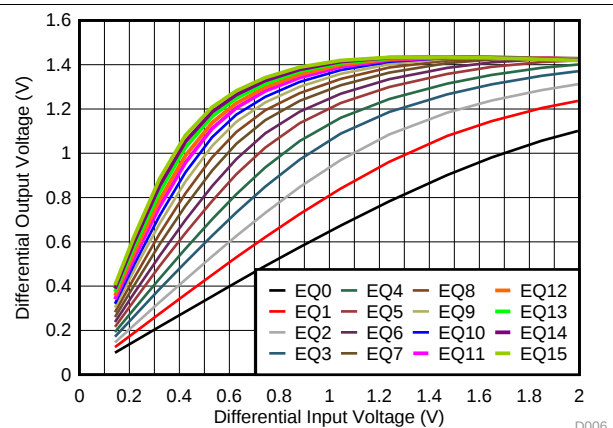
**Figure 3. USB TX EQ Settings Curves**



**Figure 4. DisplayPort Linearity Curves at 4.05 GHz**

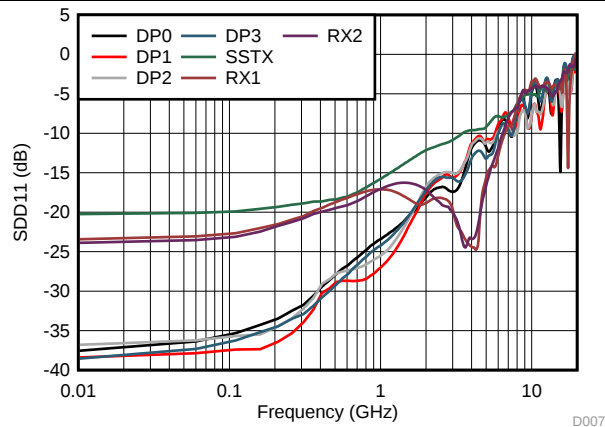


**Figure 5. USB TX Linearity Curves at 5 GHz**

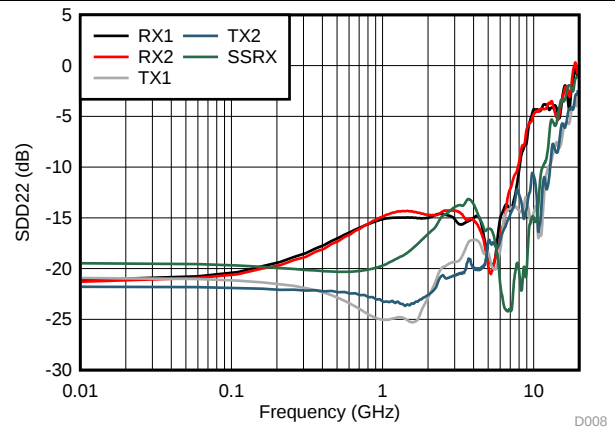


**Figure 6. USB RX Linearity Curves at 5 GHz**

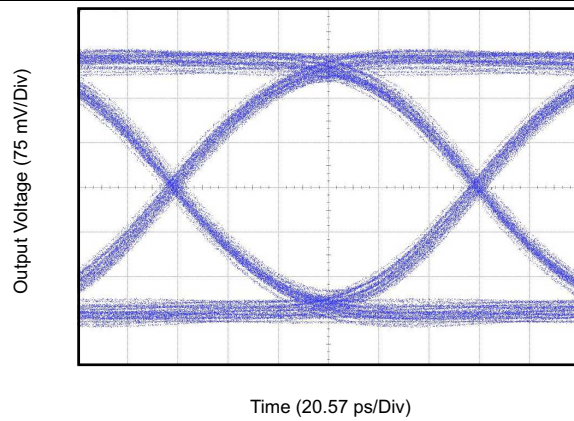
## Typical Characteristics (continued)



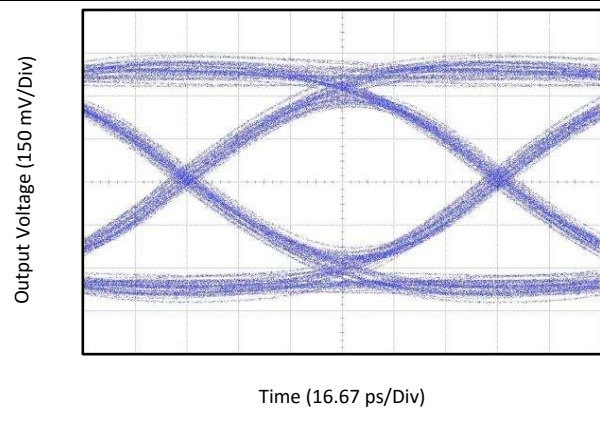
**Figure 7. Input Return Loss Performance**



**Figure 8. Output Return Loss Performance**

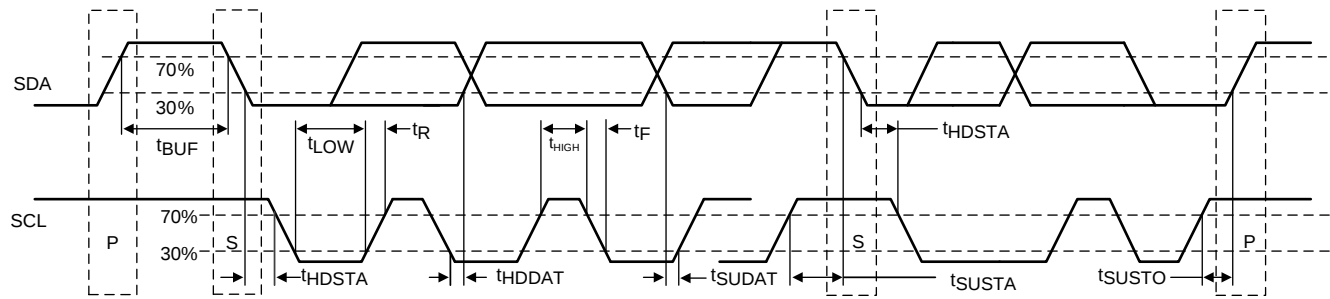


**Figure 9. DisplayPort HBR3 Eye-Pattern Performance with 12-inch Input PCB Trace at 8.1 Gbps**

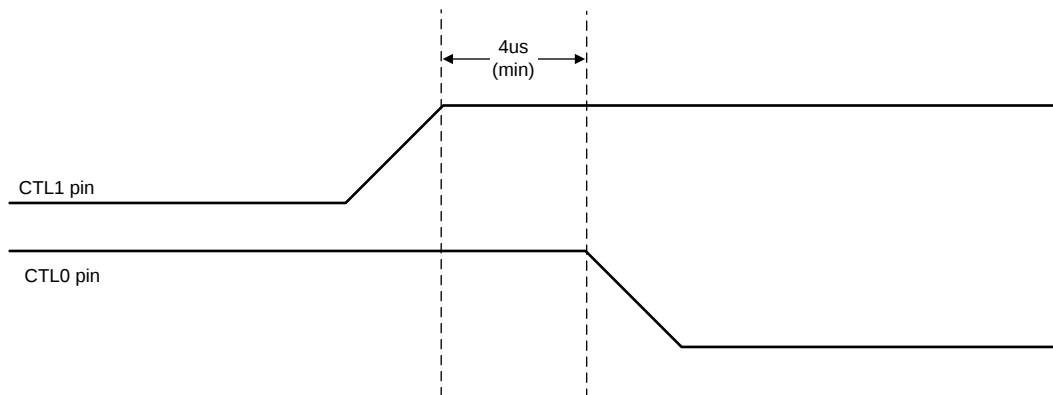


**Figure 10. USB 3.1 Gen2 Eye-Pattern Performance with 12-inch Input PCB Trace at 10 Gbps**

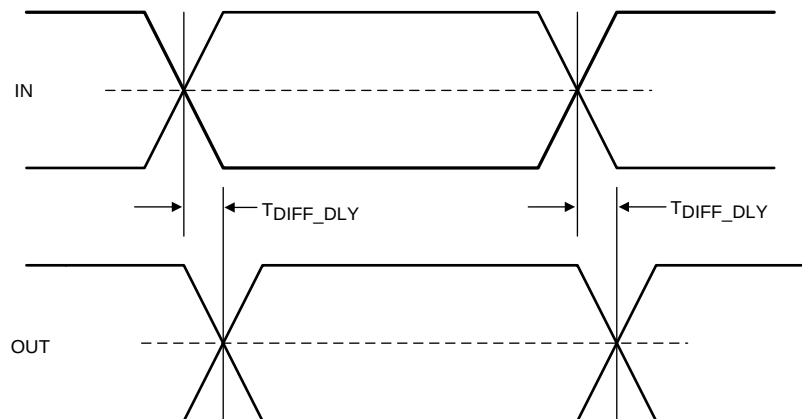
## 7 Parameter Measurement Information



**Figure 11. I²C Timing Diagram Definitions**

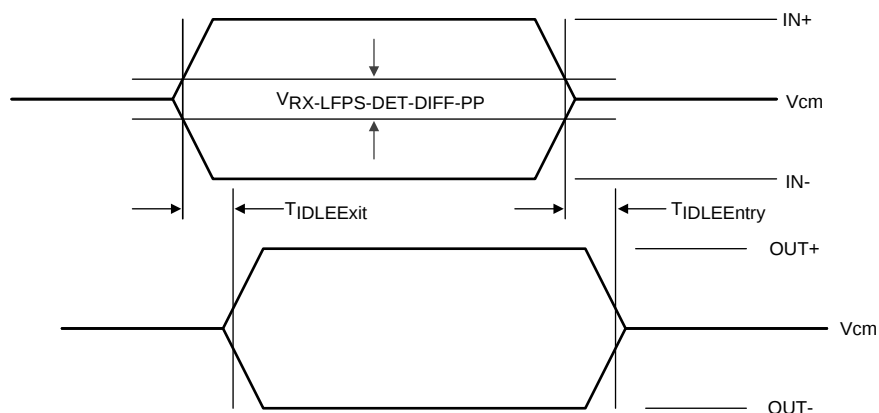


**Figure 12. USB3.1 to 4-Lane DisplayPort in GPIO Mode**

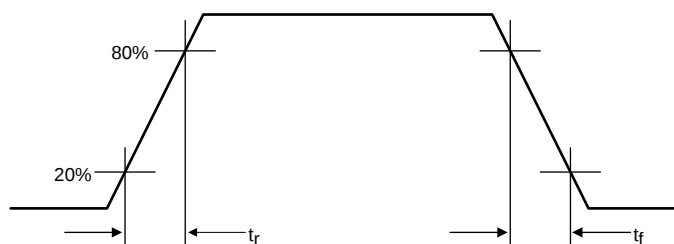


**Figure 13. Propagation Delay**

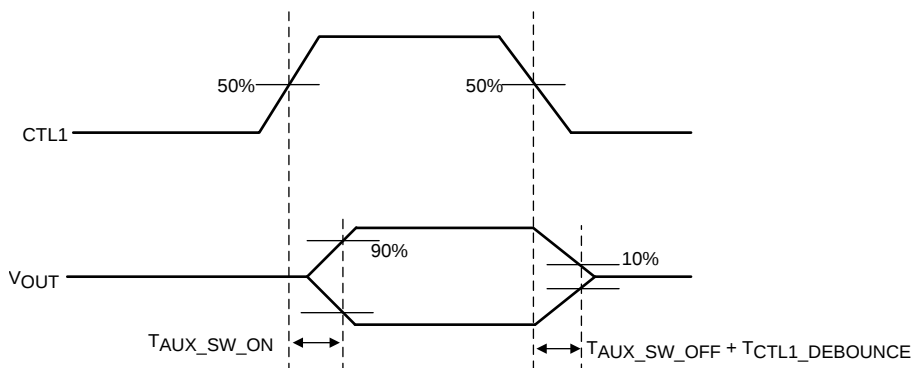
## Parameter Measurement Information (continued)



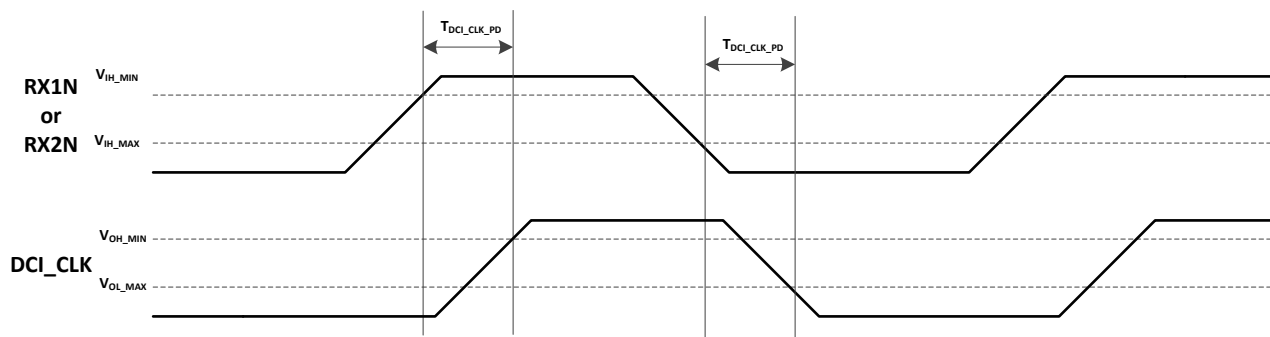
**Figure 14. Electrical Idle Mode Exit and Entry Delay**



**Figure 15. Output Rise and Fall Times**



**Figure 16. AUX and SBU Switch ON and OFF Timing Diagram**



**Figure 17. DCI Clock Propagation Delay**

## 8 Detailed Description

### 8.1 Overview

The TUSB1046A-DCI is a VESA USB Type-C Alt Mode redriving switch supporting data rates up to 8.1 Gbps for downstream facing port. These devices utilize 5<sup>th</sup> generation USB redriver technology. The devices are utilized for DFP configurations C, D, E, and F from the VESA DisplayPort Alt Mode on USB Type-C.

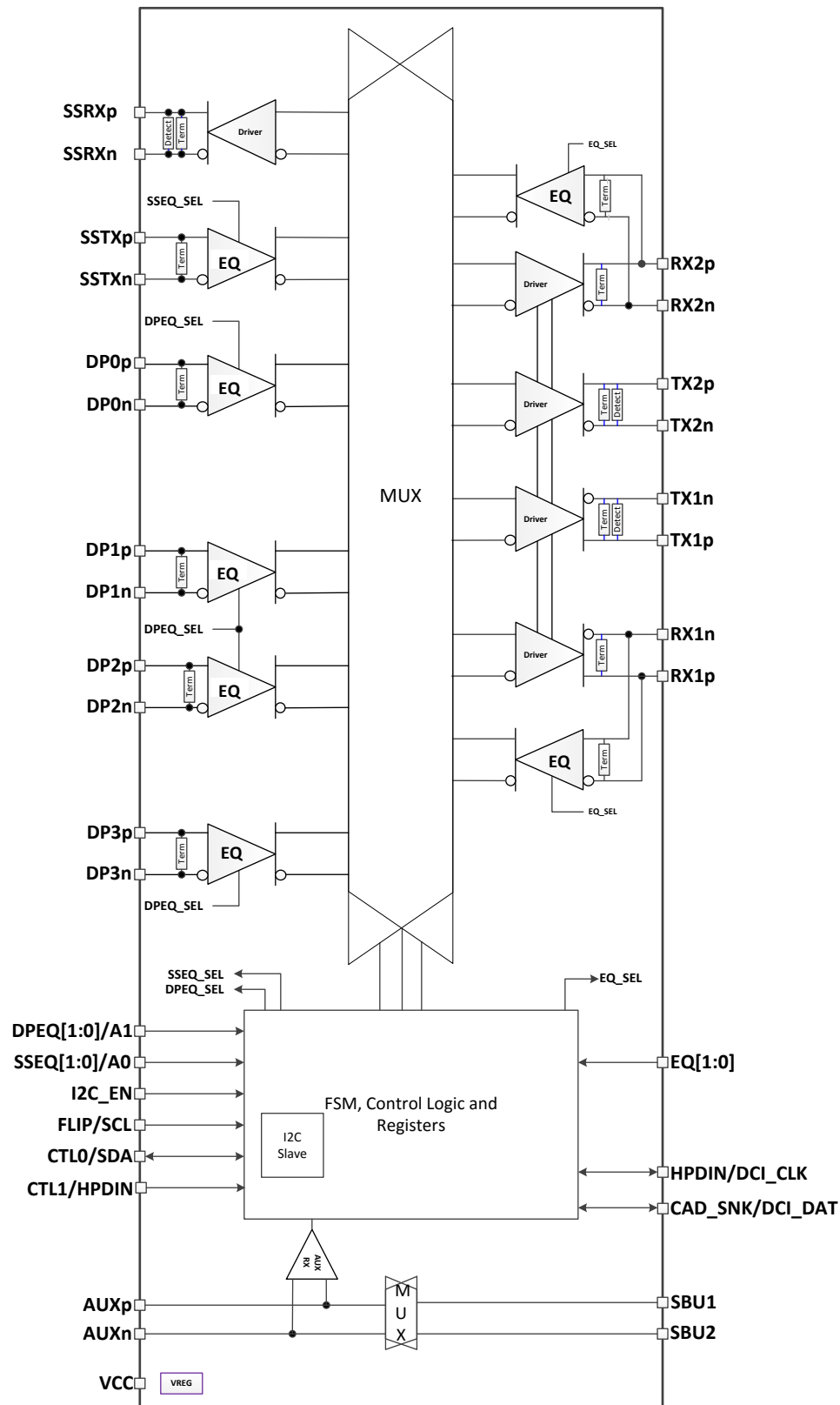
The TUSB1046A-DCI provides several levels of receive equalization to compensate for cable and board trace loss due to inter-symbol interference (ISI) when USB 3.1 Gen1/Gen2 or DisplayPort 1.4 signals travel across a PCB or cable. This device requires a 3.3-V power supply. It comes in a commercial temperature range and industrial temperature range.

For a host application the TUSB1046A-DCI enables the system to pass both transmitter compliance and receiver jitter tolerance tests for USB 3.1 Gen1/Gen2 and DisplayPort version 1.4 HBR3. The re-driver recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. Each channel has a receiver equalizer with selectable gain settings. The equalization should be set based on the amount of insertion loss before the TUSB1046A-DCI receivers. Independent equalization control for each channel can be set using EQ[1:0], SSEQ[1:0], and DPEQ[1:0] pins.

The TUSB1046A-DCI advanced state machine makes it transparent to hosts and devices. After power up, the TUSB1046A-DCI periodically performs receiver detection on the TX pairs. If it detects a USB 3.1 Gen1/Gen2 receiver, the RX termination is enabled, and the TUSB1046A-DCI is ready to re-drive.

The device ultra-low-power architecture operates at a 3.3-V power supply and achieves enhanced performance. The automatic LFPS de-emphasis control further enables the system to be USB3.1 compliant.

## 8.2 Functional Block Diagram



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## 8.3 Feature Description

### 8.3.1 USB 3.1

The TUSB1046A-DCI supports USB 3.1 Gen1/Gen2 datarates up to 10 Gbps. The TUSB1046A-DCI supports all the USB defined power states (U0, U1, U2, and U3). Because the TUSB1046A-DCI is a linear redriver, it can't decode USB3.1 physical layer traffic. The TUSB1046A-DCI monitors the actual physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the USB power state of the USB 3.1 interface.

The TUSB1046A-DCI features an intelligent low frequency periodic signaling (LFPS) detector. The LFPS detector automatically senses the low frequency signals and disables receiver equalization functionality. When not receiving LFPS, the TUSB1046A-DCI will enable receiver equalization based on the EQ[1:0] and SSEQ[1:0] pins or values programmed into EQ1\_SEL, EQ2\_SEL, and SSEQ\_SEL registers.

### 8.3.2 DisplayPort

The TUSB1046A-DCI supports up to 4 DisplayPort lanes at datarates up to 8.1Gbps (HBR3). The TUSB1046A-DCI, when configured in DisplayPort mode, monitors the native AUX traffic as it traverses between DisplayPort source and DisplayPort sink. For the purposes of reducing power, the TUSB1046A-DCI manages the number of active DisplayPort lanes based on the content of the AUX transactions. The TUSB1046A-DCI snoops native AUX writes to DisplayPort sink's DPCD registers 0x00101 (LANE\_COUNT\_SET) and 0x00600 (SET\_POWER\_STATE). TUSB1046A-DCI disables/enables lanes based on value written to LANE\_COUNT\_SET. The TUSB1046A-DCI disables all lanes when SET\_POWER\_STATE is in the D3. Otherwise active lanes will be based on value of LANE\_COUNT\_SET.

DisplayPort AUX snooping is enabled by default but can be disabled by changing the AUX\_SNOOP\_DISABLE register. Once AUX snoop is disabled, management of TUSB1046A-DCI DisplayPort lanes are controlled through various configuration registers. When TUSB1046A-DCI is enabled for GPIO mode (I2C\_EN = "0"), the CAD\_SNK pin can be used to disable AUX snooping. When CAD\_SNK pin is high, the AUX snooping functionality is disabled and all four DisplayPort lanes will be active.

### 8.3.3 4-level Inputs

The TUSB1046A-DCI has (I2C\_EN, EQ[1:0], DPEQ[1:0], and SSEQ[1:0]) 4-level inputs pins that are used to control the equalization gain and place TUSB1046A-DCI into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There is an internal 30 k $\Omega$  pull-up and a 94 k $\Omega$  pull-down. These resistors, together with the external resistor connection combine to achieve the desired voltage level.

**Table 1. 4-Level Control Pin Settings**

| LEVEL | SETTINGS                                                                                         |
|-------|--------------------------------------------------------------------------------------------------|
| 0     | Option 1: Tie 1 K $\Omega$ 5% to GND.<br>Option 2: Tie directly to GND.                          |
| R     | Tie 20 K $\Omega$ 5% to GND.                                                                     |
| F     | Float (leave pin open)                                                                           |
| 1     | Option 1: Tie 1 K $\Omega$ 5%to V <sub>CC</sub> .<br>Option 2: Tie directly to V <sub>CC</sub> . |

### NOTE

All four-level inputs are latched on rising edge of internal reset. After  $t_{\text{cfg\_hd}}$ , the internal pull-up and pull-down resistors will be isolated in order to save power.

## 8.3.4 Receiver Linear Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system before the input of the TUSB1046A-DCI. The receiver overcomes these losses by attenuating the low frequency components of the signals with respect to the high frequency components. The proper gain setting should be selected to match the channel insertion loss before the input of the TUSB1046A-DCI receivers. Two 4-level inputs pins enable up to 16 possible equalization settings. USB3.1 upstream path, USB3.1 downstream path, and DisplayPort each have their own two 4-level inputs. The TUSB1046A-DCI also provides the flexibility of adjusting settings through I<sup>2</sup>C registers.

## 8.4 Device Functional Modes

### 8.4.1 Device Configuration in GPIO Mode

The TUSB1046A-DCI is in GPIO configuration when I2C\_EN = “0”. The TUSB1046A-DCI supports the following configurations: USB 3.1 only, 2 DisplayPort lanes + USB 3.1, or 4 DisplayPort lanes (no USB 3.1). The CTL1 pin controls whether DisplayPort is enabled. The combination of CTL1 and CTL0 selects between USB 3.1 only, 2 lanes of DisplayPort, or 4-lanes of DisplayPort as detailed in [Table 2](#). The AUXp or AUXn to SBU1 or SBU2 mapping is controlled based on [Table 3](#).

After power-up ( $V_{\text{CC}}$  from 0 V to 3.3 V), the TUSB1046A-DCI defaults to USB3.1 mode. The USB PD controller upon detecting no device attached to Type-C port or USB3.1 operation not required by attached device must take TUSB1046A-DCI out of USB3.1 mode by transitioning the CTL0 pin from L to H and back to L.

**Table 2. GPIO Configuration Control**

| CTL1 PIN | CTL0 PIN | FLIP PIN | TUSB1046A-DCI CONFIGURATION             | VESA DisplayPort ALT MODE DFP_D CONFIGURATION |
|----------|----------|----------|-----------------------------------------|-----------------------------------------------|
| L        | L        | L        | Power Down                              | —                                             |
| L        | L        | H        | Power Down                              | —                                             |
| L        | H        | L        | One Port USB 3.1 - No Flip              | —                                             |
| L        | H        | H        | One Port USB 3.1 – With Flip            | —                                             |
| H        | L        | L        | 4 Lane DP - No Flip                     | C and E                                       |
| H        | L        | H        | 4 Lane DP – With Flip                   | C and E                                       |
| H        | H        | L        | One Port USB 3.1 + 2 Lane DP- No Flip   | D and F                                       |
| H        | H        | H        | One Port USB 3.1 + 2 Lane DP– With Flip | D and F                                       |

**Table 3. GPIO AUXp or AUXn to SBU1 or SBU2 Mapping**

| CTL1 PIN | FLIP PIN | MAPPING                    |
|----------|----------|----------------------------|
| H        | L        | AUXp → SBU1<br>AUXn → SBU2 |
| H        | H        | AUXp → SBU2<br>AUXn → SBU1 |
| L > 2 ms | X        | Open                       |

Table 4 Details the TUSB1046A-DCI's mux routing. This table is valid for both I<sup>2</sup>C and GPIO configuration modes.

**Table 4. INPUT to OUTPUT Mapping**

| CTL1 PIN | CTL0 PIN | FLIP PIN | FROM      | TO         |
|----------|----------|----------|-----------|------------|
|          |          |          | INPUT PIN | OUTPUT PIN |
| L        | L        | L        | NA        | NA         |
| L        | L        | H        | NA        | NA         |
| L        | H        | L        | RX1P      | SSRXP      |
|          |          |          | RX1N      | SSRXN      |
|          |          |          | SSTXP     | TX1P       |
|          |          |          | SSTXN     | TX1N       |
| L        | H        | H        | RX2P      | SSRXP      |
|          |          |          | RX2N      | SSRXN      |
|          |          |          | SSTXP     | TX2P       |
|          |          |          | SSTXN     | TX2P       |
| H        | L        | L        | DP0P      | RX2P       |
|          |          |          | DP0N      | RX2N       |
|          |          |          | DP1P      | TX2P       |
|          |          |          | DP1N      | TX2N       |
|          |          |          | DP2P      | TX1P       |
|          |          |          | DP2N      | TX1N       |
|          |          |          | DP3P      | RX1P       |
|          |          |          | DP3N      | RX1N       |
| H        | L        | H        | DP0P      | RX1P       |
|          |          |          | DP0N      | RX1N       |
|          |          |          | DP1P      | TX1P       |
|          |          |          | DP1N      | TX1N       |
|          |          |          | DP2P      | TX2P       |
|          |          |          | DP2N      | TX2N       |
|          |          |          | DP3P      | RX2P       |
|          |          |          | DP3N      | RX2N       |
| H        | H        | L        | RX1P      | SSRXP      |
|          |          |          | RX1N      | SSRXN      |
|          |          |          | SSTXP     | TX1P       |
|          |          |          | SSTXN     | TX1N       |
|          |          |          | DP0P      | RX2P       |
|          |          |          | DP0N      | RX2N       |
|          |          |          | DP1P      | TX2P       |
|          |          |          | DP1N      | TX2N       |
| H        | H        | H        | RX2P      | SSRXP      |
|          |          |          | RX2N      | SSRXN      |
|          |          |          | SSTXP     | TX2P       |
|          |          |          | SSTXN     | TX2N       |
|          |          |          | DP0P      | RX1P       |
|          |          |          | DP0N      | RX1N       |
|          |          |          | DP1P      | TX1P       |
|          |          |          | DP1N      | TX1N       |

### 8.4.2 Device Configuration In I<sup>2</sup>C Mode

The TUSB1046A-DCI is in I<sup>2</sup>C mode when I2C\_EN is not equal to “0”. The same configurations defined in GPIO mode are also available in I<sup>2</sup>C mode. The TUSB1046A-DCI USB3.1 and DisplayPort configuration is controlled based on [Table 5](#). The AUXp or AUXn to SBU1 or SBU2 mapping control is based on [Table 6](#).

**Table 5. I<sup>2</sup>C Configuration Control**

| REGISTERS |         |         | TUSB1046A-DCI CONFIGURATION             | VESA DisplayPort ALT MODE DFP_D CONFIGURATION |
|-----------|---------|---------|-----------------------------------------|-----------------------------------------------|
| CTLSEL1   | CTLSEL0 | FLIPSEL |                                         |                                               |
| 0         | 0       | 0       | Power Down                              | —                                             |
| 0         | 0       | 1       | Power Down                              | —                                             |
| 0         | 1       | 0       | One Port USB 3.1 - No Flip              | —                                             |
| 0         | 1       | 1       | One Port USB 3.1 – With Flip            | —                                             |
| 1         | 0       | 0       | 4 Lane DP - No Flip                     | C and E                                       |
| 1         | 0       | 1       | 4 Lane DP – With Flip                   | C and E                                       |
| 1         | 1       | 0       | One Port USB 3.1 + 2 Lane DP- No Flip   | D and F                                       |
| 1         | 1       | 1       | One Port USB 3.1 + 2 Lane DP– With Flip | D and F                                       |

**Table 6. I<sup>2</sup>C AUXp or AUXn to SBU1 or SBU2 Mapping**

| REGISTERS    |              |         |         | MAPPING                    |
|--------------|--------------|---------|---------|----------------------------|
| AUX_SBU_OVR1 | AUX_SBU_OVR0 | CTLSEL1 | FLIPSEL |                            |
| 0            | 0            | 1       | 0       | AUXp → SBU1<br>AUXn → SBU2 |
| 0            | 0            | 1       | 1       | AUXp → SBU2<br>AUXn → SBU1 |
| 0            | 0            | 0       | X       | Open                       |
| 0            | 1            | X       | X       | AUXp → SBU1<br>AUXn → SBU2 |
| 1            | 0            | X       | X       | AUXp → SBU2<br>AUXn → SBU1 |
| 1            | 1            | X       | X       | Open                       |

### 8.4.3 DisplayPort Mode

The TUSB1046A-DCI supports up to four DisplayPort lanes at data rates up to 8.1 Gbps. TUSB1046A-DCI can be enabled for DisplayPort through GPIO control or through I<sup>2</sup>C register control. When I2C\_EN is ‘0’, DisplayPort is controlled based on [Table 2](#). When not in GPIO mode, enable of DisplayPort functionality is controlled through I<sup>2</sup>C registers.

## 8.4.4 Linear EQ Configuration

Each of the TUSB1046A-DCI receiver lanes has individual controls for receiver equalization. The receiver equalization gain value can be controlled either through I<sup>2</sup>C registers or through GPIOs. [Table 7](#) details the gain value for each available combination when TUSB1046A-DCI is in GPIO mode. These same options are also available in I<sup>2</sup>C mode by updating registers DP0EQ\_SEL, DP1EQ\_SEL, DP2EQ\_SEL, DP3EQ\_SEL, EQ1\_SEL, EQ2\_SEL, and SSEQ\_SEL.

**Table 7. TUSB1046A-DCI Receiver Equalization GPIO Control**

| Equalization Setting # | USB3.1 DOWNSTREAM FACING PORTS |               |                       | USB 3.1 UPSTREAM FACING PORT |                 |                       | ALL DISPLAYPORT LANES |                 |                          |
|------------------------|--------------------------------|---------------|-----------------------|------------------------------|-----------------|-----------------------|-----------------------|-----------------|--------------------------|
|                        | EQ1 PIN LEVEL                  | EQ0 PIN LEVEL | EQ GAIN at 5 GHz (dB) | SSEQ1 PIN LEVEL              | SSEQ0 PIN LEVEL | EQ GAIN at 5 GHz (dB) | DPEQ1 PIN LEVEL       | DPEQ0 PIN LEVEL | EQ GAIN at 4.05 GHz (dB) |
| 0                      | 0                              | 0             | -3.9                  | 0                            | 0               | -1.8                  | 0                     | 0               | 1.0                      |
| 1                      | 0                              | R             | -1.7                  | 0                            | R               | 0.2                   | 0                     | R               | 3.3                      |
| 2                      | 0                              | F             | -0.1                  | 0                            | F               | 1.7                   | 0                     | F               | 4.9                      |
| 3                      | 0                              | 1             | 1.4                   | 0                            | 1               | 3.2                   | 0                     | 1               | 6.5                      |
| 4                      | R                              | 0             | 2.4                   | R                            | 0               | 4.2                   | R                     | 0               | 7.5                      |
| 5                      | R                              | R             | 3.5                   | R                            | R               | 5.3                   | R                     | R               | 8.6                      |
| 6                      | R                              | F             | 4.4                   | R                            | F               | 6.1                   | R                     | F               | 9.5                      |
| 7                      | R                              | 1             | 5.2                   | R                            | 1               | 7.0                   | R                     | 1               | 10.4                     |
| 8                      | F                              | 0             | 5.9                   | F                            | 0               | 7.7                   | F                     | 0               | 11.1                     |
| 9                      | F                              | R             | 6.6                   | F                            | R               | 8.3                   | F                     | R               | 11.7                     |
| 10                     | F                              | F             | 7.1                   | F                            | F               | 8.8                   | F                     | F               | 12.3                     |
| 11                     | F                              | 1             | 7.6                   | F                            | 1               | 9.3                   | F                     | 1               | 12.8                     |
| 12                     | 1                              | 0             | 8.0                   | 1                            | 0               | 9.7                   | 1                     | 0               | 13.2                     |
| 13                     | 1                              | R             | 8.5                   | 1                            | R               | 10.1                  | 1                     | R               | 13.6                     |
| 14                     | 1                              | F             | 8.8                   | 1                            | F               | 10.4                  | 1                     | F               | 14.0                     |
| 15                     | 1                              | 1             | 9.2                   | 1                            | 1               | 10.8                  | 1                     | 1               | 14.4                     |

## 8.4.5 USB3.1 Modes

The TUSB1046A-DCI monitors the physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the state of the USB3.1 interface. Depending on the state of the USB 3.1 interface, the TUSB1046A-DCI can be in one of four primary modes of operation when USB 3.1 is enabled (CTL0 = H or CTLSEL0 = 1b1): Disconnect, U2/U3, U1, and U0.

The Disconnect mode is the state in which TUSB1046A-DCI has not detected far-end termination on both upstream facing port (UFP) or downstream facing port (DFP). The disconnect mode is the lowest power mode of each of the four modes. The TUSB1046A-DCI remains in this mode until far-end receiver termination has been detected on both UFP and DFP. The TUSB1046A-DCI immediately exits this mode and enter U0 once far-end termination is detected.

Once in U0 mode, the TUSB1046A-DCI will redrive all traffic received on UFP and DFP. U0 is the highest power mode of all USB3.1 modes. The TUSB1046A-DCI remains in U0 mode until electrical idle occurs on both UFP and DFP. Upon detecting electrical idle, the TUSB1046A-DCI immediately transitions to U1.

The U1 mode is the intermediate mode between U0 mode and U2/U3 mode. In U1 mode, the TUSB1046A-DCI UFP and DFP receiver termination remains enabled. The UFP and DFP transmitter DC common mode is maintained. The power consumption in U1 is similar to power consumption of U0.

Next to the disconnect mode, the U2/U3 mode is next lowest power state. While in this mode, the TUSB1046A-DCI periodically performs far-end receiver detection. Anytime the far-end receiver termination is not detected on either UFP or DFP, the TUSB1046A-DCI leaves the U2/U3 mode and transitions to the Disconnect mode. It also monitors for a valid LFPS. Upon detection of a valid LFPS, the TUSB1046A-DCI immediately transitions to the U0 mode. In U2/U3 mode, the TUSB1046A-DCI receiver terminations remain enabled but the TX DC common mode voltage is not maintained.

## 8.4.6 Operation Timing – Power Up

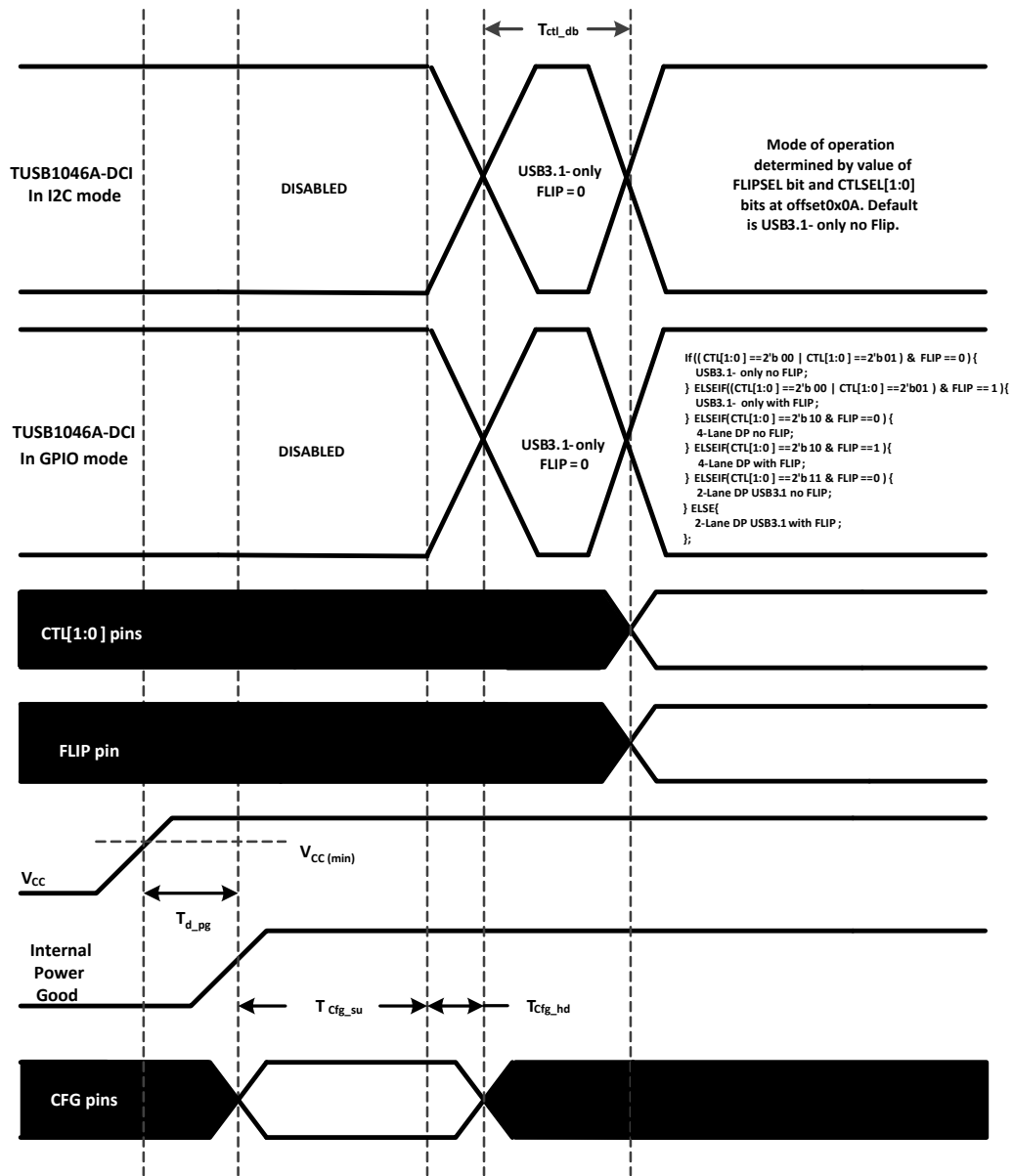


Figure 18. Power-Up Timing

Table 8. Power-Up Timing<sup>(1)(2)</sup>

| PARAMETER       |                                                    | MIN | MAX | UNIT    |
|-----------------|----------------------------------------------------|-----|-----|---------|
| $t_{d\_pg}$     | VCC (minimum) to Internal Power Good asserted high |     | 500 | $\mu$ s |
| $t_{cfg\_su}$   | CFG(1) pins setup <sup>(2)</sup>                   | 250 |     | $\mu$ s |
| $t_{cfg\_hd}$   | CFG(1) pins hold                                   | 10  |     | $\mu$ s |
| $t_{CTL\_DB}$   | CTL[1:0] and FLIP pin debounce                     |     | 16  | ms      |
| $t_{VCC\_RAMP}$ | VCC supply ramp requirement                        |     | 100 | ms      |

(1) Following pins comprise CFG pins: I2C\_EN, EQ[1:0], SSEQ[1:0], and DPEQ[1:0].

(2) Recommend CFG pins are stable when VCC is at min.

## 8.5 Programming

For further programmability, the TUSB1046A-DCI can be controlled using I<sup>2</sup>C. The SCL and SDA pins are used for I<sup>2</sup>C clock and I<sup>2</sup>C data respectively.

**Table 9. TUSB1046A-DCI I<sup>2</sup>C Target Address**

| DPEQ0/A1<br>PIN LEVEL | SSEQ0/A0<br>PIN LEVEL | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (W/R) |
|-----------------------|-----------------------|-------------|-------|-------|-------|-------|-------|-------|-------------|
| 0                     | 0                     | 1           | 0     | 0     | 0     | 1     | 0     | 0     | 0/1         |
| 0                     | R                     | 1           | 0     | 0     | 0     | 1     | 0     | 1     | 0/1         |
| 0                     | F                     | 1           | 0     | 0     | 0     | 1     | 1     | 0     | 0/1         |
| 0                     | 1                     | 1           | 0     | 0     | 0     | 1     | 1     | 1     | 0/1         |
| R                     | 0                     | 0           | 1     | 0     | 0     | 0     | 0     | 0     | 0/1         |
| R                     | R                     | 0           | 1     | 0     | 0     | 0     | 0     | 1     | 0/1         |
| R                     | F                     | 0           | 1     | 0     | 0     | 0     | 1     | 0     | 0/1         |
| R                     | 1                     | 0           | 1     | 0     | 0     | 0     | 1     | 1     | 0/1         |
| F                     | 0                     | 0           | 0     | 1     | 0     | 0     | 0     | 0     | 0/1         |
| F                     | R                     | 0           | 0     | 1     | 0     | 0     | 0     | 1     | 0/1         |
| F                     | F                     | 0           | 0     | 1     | 0     | 0     | 1     | 0     | 0/1         |
| F                     | 1                     | 0           | 0     | 1     | 0     | 0     | 1     | 1     | 0/1         |
| 1                     | 0                     | 0           | 0     | 0     | 1     | 1     | 0     | 0     | 0/1         |
| 1                     | R                     | 0           | 0     | 0     | 1     | 1     | 0     | 1     | 0/1         |
| 1                     | F                     | 0           | 0     | 0     | 1     | 1     | 1     | 0     | 0/1         |
| 1                     | 1                     | 0           | 0     | 0     | 1     | 1     | 1     | 1     | 0/1         |

The following procedure should be followed to write to TUSB1046A-DCI I<sup>2</sup>C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB1046A-DCI 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB1046A-DCI acknowledges the address cycle.
3. The master presents the sub-address (I<sup>2</sup>C register within TUSB1046A-DCI) to be written, consisting of one byte of data, MSB-first.
4. The TUSB1046A-DCI acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I<sup>2</sup>C register.
6. The TUSB1046A-DCI acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB1046A-DCI.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure should be followed to read the TUSB1046A-DCI I<sup>2</sup>C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the TUSB1046A-DCI 7-bit address and a one-value “W/R” bit to indicate a read cycle.
2. The TUSB1046A-DCI acknowledges the address cycle.
3. The TUSB1046A-DCI transmit the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the T I<sup>2</sup>C register occurred prior to the read, then the TUSB1046A-DCI shall start at the sub-address specified in the write.
4. The TUSB1046A-DCI shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I<sup>2</sup>C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the TUSB1046A-DCI transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure should be followed for setting a starting sub-address for I<sup>2</sup>C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB1046A-DCI 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB1046A-DCI acknowledges the address cycle.
3. The master presents the sub-address (I<sup>2</sup>C register within TUSB1046A-DCI) to be written, consisting of one byte of data, MSB-first.

4. The TUSB1046A-DCI acknowledges the sub-address cycle.
5. The master terminates the write operation by generating a stop condition (P).

#### NOTE

If no sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the I<sup>2</sup>C master terminates the read operation. If a I<sup>2</sup>C address write occurred prior to the read, then the reads start at the sub-address specified by the address write.

**Table 10. Register Legend**

| ACCESS TAG | NAME      | MEANING                                                                                |
|------------|-----------|----------------------------------------------------------------------------------------|
| R          | Read      | The field may be read by software                                                      |
| W          | Write     | The field may be written by software                                                   |
| S          | Set       | The field may be set by a write of one. Writes of zeros to the field have no effect.   |
| C          | Clear     | The field may be cleared by a write of one. Write of zero to the field have no effect. |
| U          | Update    | Hardware may autonomously update this field.                                           |
| NA         | No Access | Not accessible or not applicable                                                       |

## 8.6 Register Maps

### 8.6.1 General Register (address = 0x0A) [reset = 00000001]

**Figure 19. General Registers**

| 7        | 6 | 5         | 4               | 3                | 2       | 1            | 0 |
|----------|---|-----------|-----------------|------------------|---------|--------------|---|
| Reserved |   | SWAP_HPDI | EQ_OVERRID<br>E | HPDI_OVRRI<br>DE | FLIPSEL | CTLSEL[1:0]. |   |
| R        |   | R/W       | R/W             | R/W              | R/W     | R/W          |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 11. General Registers**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                           |
|-----|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | Reserved.    | R    | 00    | Reserved.                                                                                                                                                                                                                                                                             |
| 5   | SWAP_HPDI    | R/W  | 0     | 0 – HPDI is in default location (Default)<br>1 – HPDI location is swapped (PIN 23 to PIN 32, or PIN 32 to PIN23).                                                                                                                                                                     |
| 4   | EQ_OVERRIDE  | R/W  | 0     | Setting of this field will allow software to use EQ settings from registers instead of value sample from pins.<br>0 – EQ settings based on sampled state of the EQ pins (SSEQ[1:0], EQ[1:0], and DPEQ[1:0]).<br>1 – EQ settings based on programmed value of each of the EQ registers |
| 3   | HPDI_OVRRI   | R/W  | 0     | 0 – HPDI IN based on state of HPDI_IN pin (Default)<br>1 – HPDI_IN high.                                                                                                                                                                                                              |
| 2   | FLIPSEL      | R/W  | 0     | FLIPSEL. Refer to <a href="#">Table 5</a> and <a href="#">Table 6</a> for this field functionality.                                                                                                                                                                                   |
| 1:0 | CTLSEL[1:0]. | R/W  | 01    | 00 – Disabled. All RX and TX for USB3 and DisplayPort are disabled.<br>01 – USB3.1 only enabled. (Default)<br>10 – Four DisplayPort lanes enabled.<br>11 – Two DisplayPort lanes and one USB3.1                                                                                       |

### 8.6.2 DisplayPort Control/Status Registers (address = 0x10) [reset = 00000000]

**Figure 20. DisplayPort Control/Status Registers (0x10)**

| 7         | 6 | 5 | 4 | 3         | 2 | 1 | 0 |
|-----------|---|---|---|-----------|---|---|---|
| DP1EQ_SEL |   |   |   | DP0EQ_SEL |   |   |   |
| R/W/U     |   |   |   | R/W/U     |   |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 12. DisplayPort Control/Status Registers (0x10)**

| Bit | Field     | Type  | Reset | Description                                                                                                                                                                                                                                            |
|-----|-----------|-------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | DP1EQ_SEL | R/W/U | 0000  | Field selects between 0 to 14dB of EQ for DP lane 1. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 1 based on value written to this field. |
| 3:0 | DP0EQ_SEL | R/W/U | 0000  | Field selects between 0 to 14dB of EQ for DP lane 0. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 0 based on value written to this field. |

### 8.6.3 DisplayPort Control/Status Registers (address = 0x11) [reset = 00000000]

**Figure 21. DisplayPort Control/Status Registers (0x11)**

| 7         | 6 | 5 | 4 | 3         | 2 | 1 | 0 |
|-----------|---|---|---|-----------|---|---|---|
| DP3EQ_SEL |   |   |   | DP2EQ_SEL |   |   |   |
| R/W/U     |   |   |   | R/W/U     |   |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 13. DisplayPort Control/Status Registers (0x11)**

| Bit | Field     | Type  | Reset | Description                                                                                                                                                                                                                                            |
|-----|-----------|-------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | DP3EQ_SEL | R/W/U | 0000  | Field selects between 0 to 14dB of EQ for DP lane 3. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 3 based on value written to this field. |
| 3:0 | DP2EQ_SEL | R/W/U | 0000  | Field selects between 0 to 14dB of EQ for DP lane 2. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 2 based on value written to this field. |

### 8.6.4 DisplayPort Control/Status Registers (address = 0x12) [reset = 00000000]

**Figure 22. DisplayPort Control/Status Registers (0x12)**

| 7        | 6               | 5 | 4              | 3 | 2 | 1 | 0 |
|----------|-----------------|---|----------------|---|---|---|---|
| Reserved | SET_POWER_STATE |   | LANE_COUNT_SET |   |   |   |   |
| R        | RU              |   | RU             |   |   |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 14. DisplayPort Control/Status Registers (0x12)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved        | R    | 0     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 6:5 | SET_POWER_STATE | R/U  | 00    | This field represents the snooped value of the AUX write to DPCD address 0x00600. When AUX_SNOOP_DISABLE = 1'b0, the TUSB1046A-DCI will enable/disable DP lanes based on the snooped value. When AUX_SNOOP_DISABLE = 1'b1, then DP lane enable/disable are determined by state of DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 2'b00 by hardware when CTLSEL1 changes from a 1'b1 to a 1'b0.                                 |
| 4:0 | LANE_COUNT_SET  | R/U  | 00000 | This field represents the snooped value of AUX write to DPCD address 0x00101 register. When AUX_SNOOP_DISABLE = 1'b0, TUSB1046-DCI will enable DP lanes specified by the snoop value. Unused DP lanes will be disabled to save power. When AUX_SNOOP_DISABLE = 1'b1, then DP lanes enable/disable are determined by DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 0x0 by hardware when CTLSEL1 changes from a 1'b1 to a 1'b0. |

## 8.6.5 DisplayPort Control/Status Registers (address = 0x13) [reset = 00000000]

**Figure 23. DisplayPort Control/Status Registers (0x13)**

| 7                 | 6        | 5           | 4           | 3           | 2           | 1           | 0   |
|-------------------|----------|-------------|-------------|-------------|-------------|-------------|-----|
| AUX_SNOOP_DISABLE | Reserved | AUX_SBU_OVR | DP3_DISABLE | DP2_DISABLE | DP1_DISABLE | DP0_DISABLE |     |
| R/W               | R        | R/W         | R/W         | R/W         | R/W         | R/W         | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 15. DisplayPort Control/Status Registers (0x13)**

| Bit | Field             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | AUX_SNOOP_DISABLE | R/W  | 0     | 0 – AUX snoop enabled. (Default)<br>1 – AUX snoop disabled.                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 6   | Reserved          | R    | 0     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 5:4 | AUX_SBU_OVR       | R/W  | 00    | This field overrides the AUXp or AUXn to SBU1 or SBU2 connect and disconnect based on CTL1 and FLIP. Changing this field to 1'b1 will allow traffic to pass through AUX to SBU regardless of the state of CTLSEL1 and FLIPSEL register<br>00 – AUX to SBU connect/disconnect determined by CTLSEL1 and FLIPSEL (Default)<br>01 – AUXp -> SBU1 and AUXn -> SBU2 connection always enabled.<br>10 – AUXp -> SBU2 and AUXn -> SBU1 connection always enabled.<br>11 = AUX to SBU open. |
| 3   | DP3_DISABLE       | R/W  | 0     | When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 3. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 3 functionality.<br>0 – DP Lane 3 Enabled (default)<br>1 – DP Lane 3 Disabled.                                                                                                                                                                                                                               |
| 2   | DP2_DISABLE       | R/W  | 0     | When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 2. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 2 functionality.<br>0 – DP Lane 2 Enabled (default)<br>1 – DP Lane 2 Disabled.                                                                                                                                                                                                                               |
| 1   | DP1_DISABLE       | R/W  | 0     | When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 1. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 1 functionality.<br>0 – DP Lane 1 Enabled (default)<br>1 – DP Lane 1 Disabled.                                                                                                                                                                                                                               |
| 0   | DP0_DISABLE       | R/W  | 0     | DISABLE. When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 0. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 0 functionality.<br>0 – DP Lane 0 Enabled (default)<br>1 – DP Lane 0 Disabled.                                                                                                                                                                                                                      |

### 8.6.6 USB3.1 Control/Status Registers (address = 0x20) [reset = 00000000]

**Figure 24. USB3.1 Control/Status Registers (0x20)**

| 7       | 6 | 5 | 4 | 3       | 2 | 1 | 0 |
|---------|---|---|---|---------|---|---|---|
| EQ2_SEL |   |   |   | EQ1_SEL |   |   |   |
| R/W/U   |   |   |   | R/W/U   |   |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 16. USB3.1 Control/Status Registers (0x20)**

| Bit | Field   | Type  | Reset | Description                                                                                                                                                                                                                                                              |
|-----|---------|-------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | EQ2_SEL | R/W/U | 0000  | Field selects between 0 to 9 dB of EQ for USB3.1 RX2 receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.1 RX2 receiver based on value written to this field. |
| 3:0 | EQ1_SEL | R/W/U | 0000  | Field selects between 0 to 9 dB of EQ for USB3.1 RX1 receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.1 RX1 receiver based on value written to this field. |

### 8.6.7 USB3.1 Control/Status Registers (address = 0x21) [reset = 00000000]

**Figure 25. USB3.1 Control/Status Registers (0x21)**

| 7        | 6 | 5 | 4 | 3        | 2 | 1 | 0 |
|----------|---|---|---|----------|---|---|---|
| Reserved |   |   |   | SSEQ_SEL |   |   |   |
| R        |   |   |   | R/W/U    |   |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 17. USB3.1 Control/Status Registers (0x21)**

| Bit | Field    | Type  | Reset | Description                                                                                                                                                                                                                                                                         |
|-----|----------|-------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | Reserved | R     | 0000  | Reserved                                                                                                                                                                                                                                                                            |
| 3:0 | SSEQ_SEL | R/W/U | 0000  | Field selects between 0 to 11 dB of EQ for USB3.1 SSTXP/N receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of SSEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.1 SSTXP/N receiver based on value written to this field. |

## 8.6.8 USB3.1 Control/Status Registers (address = 0x22) [reset = 00000100]

**Figure 26. USB3.1 Control/Status Registers (0x22)**

| 7         | 6       | 5                  | 4                  | 3                  | 2 | 1                    | 0 |
|-----------|---------|--------------------|--------------------|--------------------|---|----------------------|---|
| CM_ACTIVE | LFPS_EQ | U2U3_LFPS_DEBOUNCE | DISABLE_U2U3_RXDET | DFP_RXDET_INTERVAL |   | USB3_COMPLIANCE_CTRL |   |
| R/U       | R/W     | R/W                | R/W                | R/W                |   | R/W                  |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 18. USB3.1 Control/Status Registers (0x22)**

| Bit | Field                | Type | Reset | Description                                                                                                                                                                                                                      |
|-----|----------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | CM_ACTIVE            | R/U  | 0     | 0 – device not in USB 3.1 compliance mode. (Default)<br>1 – device in USB 3.1 compliance mode                                                                                                                                    |
| 6   | LFPS_EQ              | R/W  | 0     | Controls whether settings of EQ based on EQ1_SEL, EQ2_SEL and SSEQ_SEL applies to received LFPS signal.<br>0 – EQ set to zero when receiving LFPS (default)<br>1 – EQ set to EQ1_SEL, EQ2_SEL, and SSEQ_SEL when receiving LFPS. |
| 5   | U2U3_LFPS_DEBOUNCE   | R/W  | 0     | 0 – No debounce of LFPS before U2/U3 exit. (Default)<br>1 – 200us debounce of LFPS before U2/U3 exit.                                                                                                                            |
| 4   | DISABLE_U2U3_RXDET   | R/W  | 0     | 0 – Rx.Detect in U2/U3 enabled. (Default)<br>1 – Rx.Detect in U2/U3 disabled.                                                                                                                                                    |
| 3:2 | DFP_RXDET_INTERVAL   | R/W  | 01    | This field controls the Rx.Detect interval for the Downstream facing port (TX1P/N and TX2P/N).<br>00 – 8 ms<br>01 – 12 ms (default)<br>10 – 48 ms<br>11 – 96 ms                                                                  |
| 1:0 | USB3_COMPLIANCE_CTRL | R/W  | 00    | 00 – FSM determined compliance mode. (Default)<br>01 – Compliance Mode enabled in DFP direction (SSTX -> TX1/TX2)<br>10 – Compliance Mode enabled in UFP direction (RX1/RX2 -> SSRX)<br>11 – Compliance Mode Disabled.           |

## 9 Application and Implementation

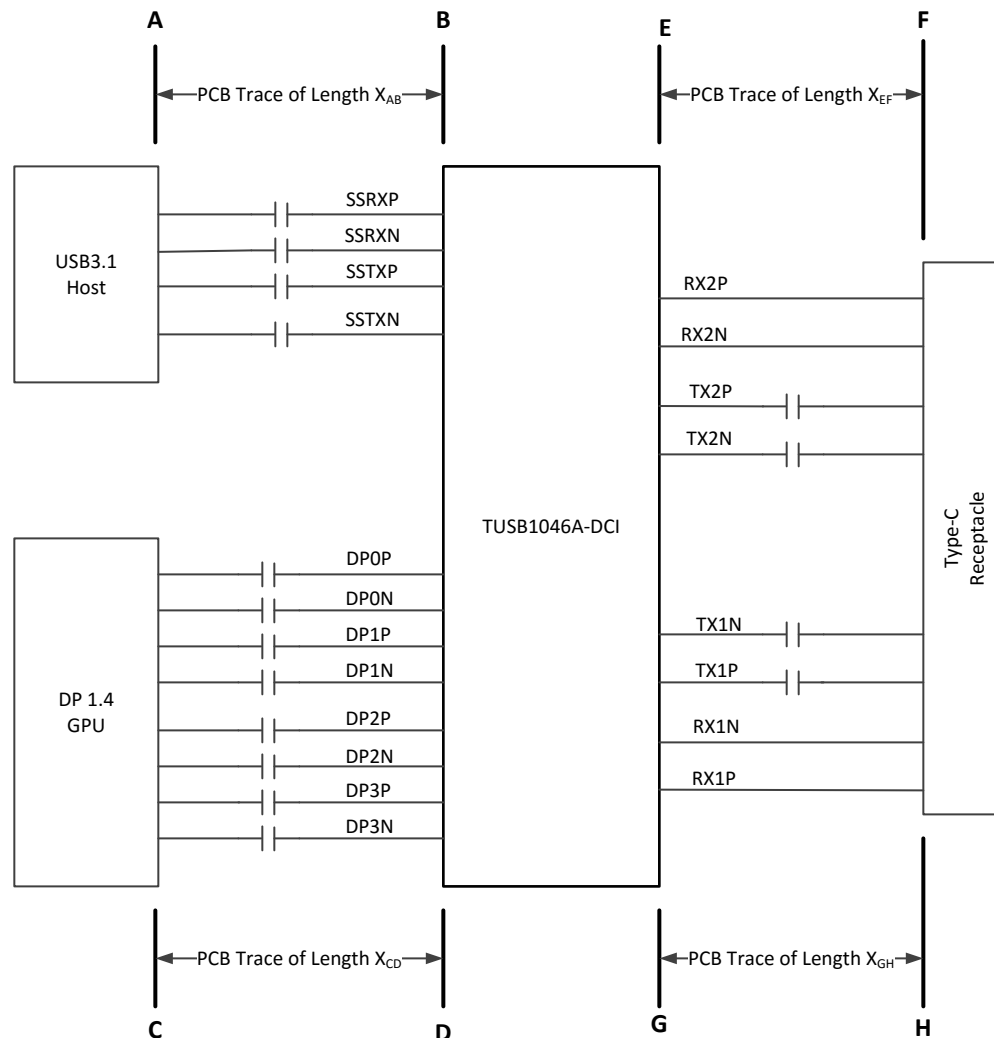
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TUSB1046-DCI is a linear redriver designed specifically to compensation for intersymbol interference (ISI) jitter caused by signal attenuation through a passive medium like PCB traces and cables. Because the TUSB1046-DCI has four independent DisplayPort 1.4 inputs, one upstream facing USB 3.1 Gen1/Gen2 input, and two downstream facing USB 3.1 Gen1/Gen2 inputs, it can be optimized to correct ISI on all those seven inputs through 16 different equalization choices. Placing the TUSB1046-DCI between a USB3.1 Host/DisplayPort 1.4 GPU and a USB3.1 Type-C receptacle can correct signal integrity issues resulting in a more robust system.

### 9.2 Typical Application



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**Figure 27. TUSB1046-DCI in a Host Application**

## Typical Application (continued)

### 9.2.1 Design Requirements

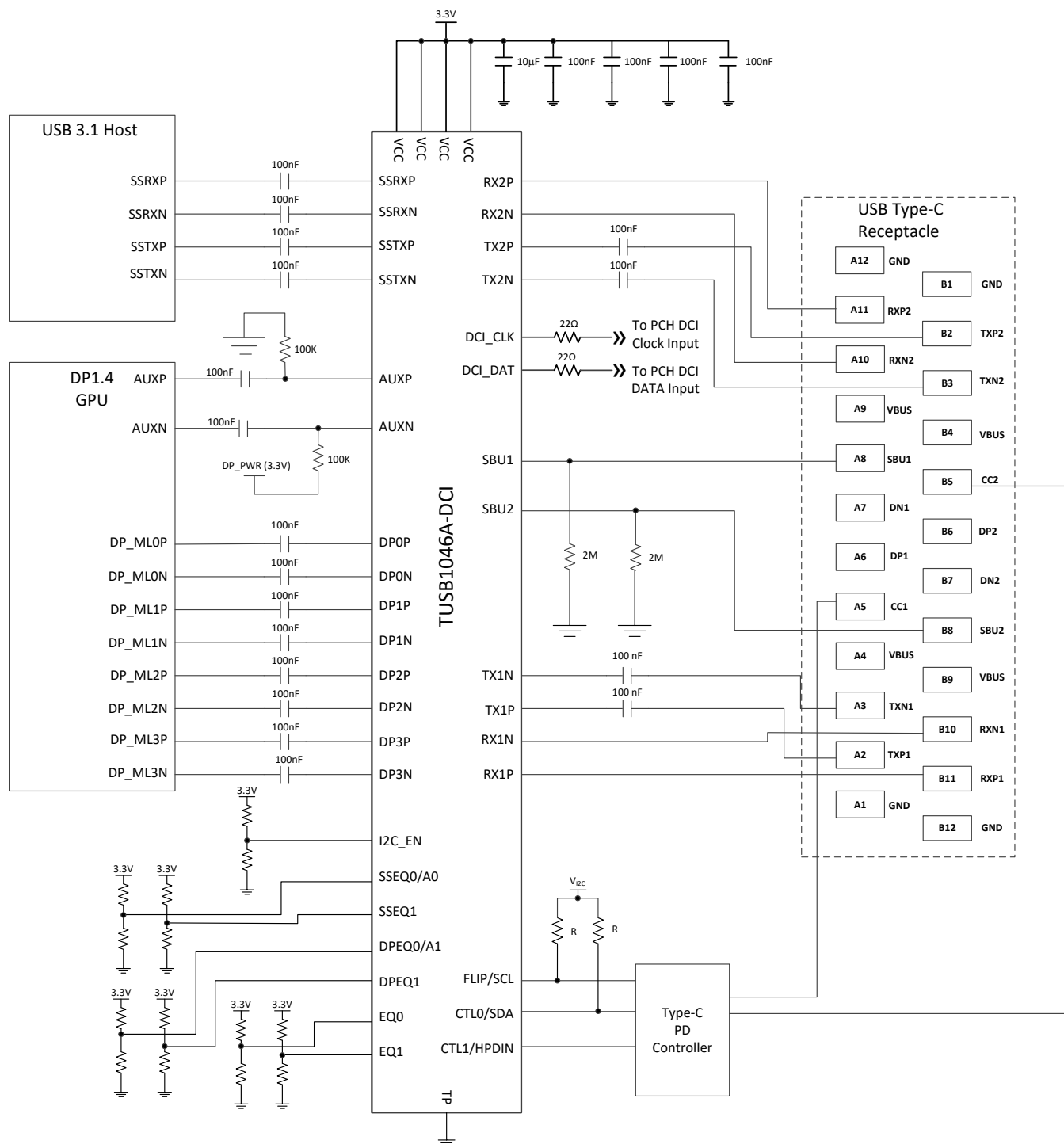
For this design example, use the parameters shown in [Table 19](#).

**Table 19. Design Parameters**

| PARAMETER                               | VALUE                                                            |
|-----------------------------------------|------------------------------------------------------------------|
| A to B PCB trace length, $X_{AB}$       | 12 inches                                                        |
| C to D PCB trace length, $X_{CD}$       | 12 inches                                                        |
| E to F PCB trace length, $X_{EF}$       | 2 inches                                                         |
| G to H PCB trace length, $X_{GH}$       | 2 inches                                                         |
| PCB trace width                         | 4 mils                                                           |
| AC-coupling capacitor (75 nF to 265 nF) | 100 nF                                                           |
| VCC supply (3 V to 3.6 V)               | 3.3 V                                                            |
| I2C Mode or GPIO Mode                   | I2C Mode. (I2C_EN pin != "0")                                    |
| 1.8V or 3.3V I2C Interface              | 3.3V I2C. Pull-up the I2C_EN pin to 3.3V with a 1K ohm resistor. |

### 9.2.2 Detailed Design Procedure

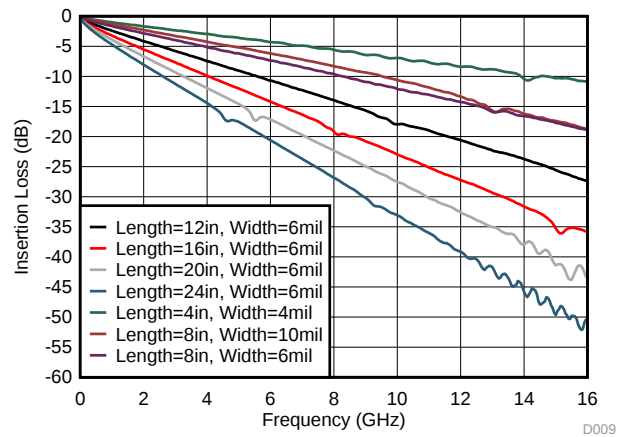
A typical usage of the TUSB1046-DCI device is shown in [Figure 28](#). The device can be controlled either through its GPIO pins or through its I<sup>2</sup>C interface. In the example shown below, a Type-C PD controller is used to configure the device through the I<sup>2</sup>C interface. When configured for I2C mode, pins 29 (RSVD1) and 32 (RSVD2) can be left unconnected. In I2C mode, the equalization settings for each receiver can be independently controlled through I2C registers. For this reason, all of the equalization pins (EQ[1:0], SSEQ[1:0], and DPEQ[1:0]) can be left unconnected. If these pins are left unconnected, the TUSB1046-DCI 7-bit I2C slave address will be 0x12 because both DPEQ/A1 and SSEQ0/A0 will be at pin level "F". If a different I2C slave address is desired, DPEQ/A1 and SSEQ0/A0 pins should be set to a level which produces the desired I2C slave address.



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Figure 28. Application Circuit

### 9.2.3 Application Curve

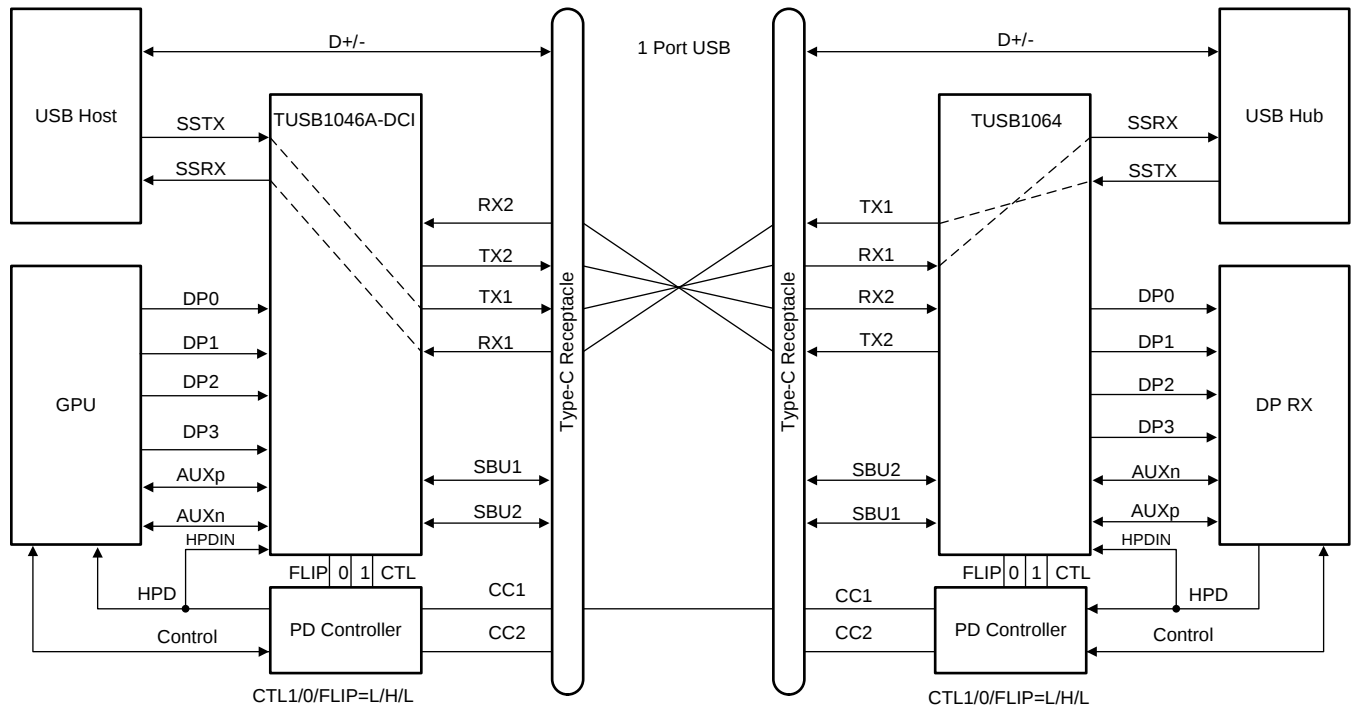


**Figure 29. Insertion Loss of FR4 PCB Traces**

## 9.3 System Examples

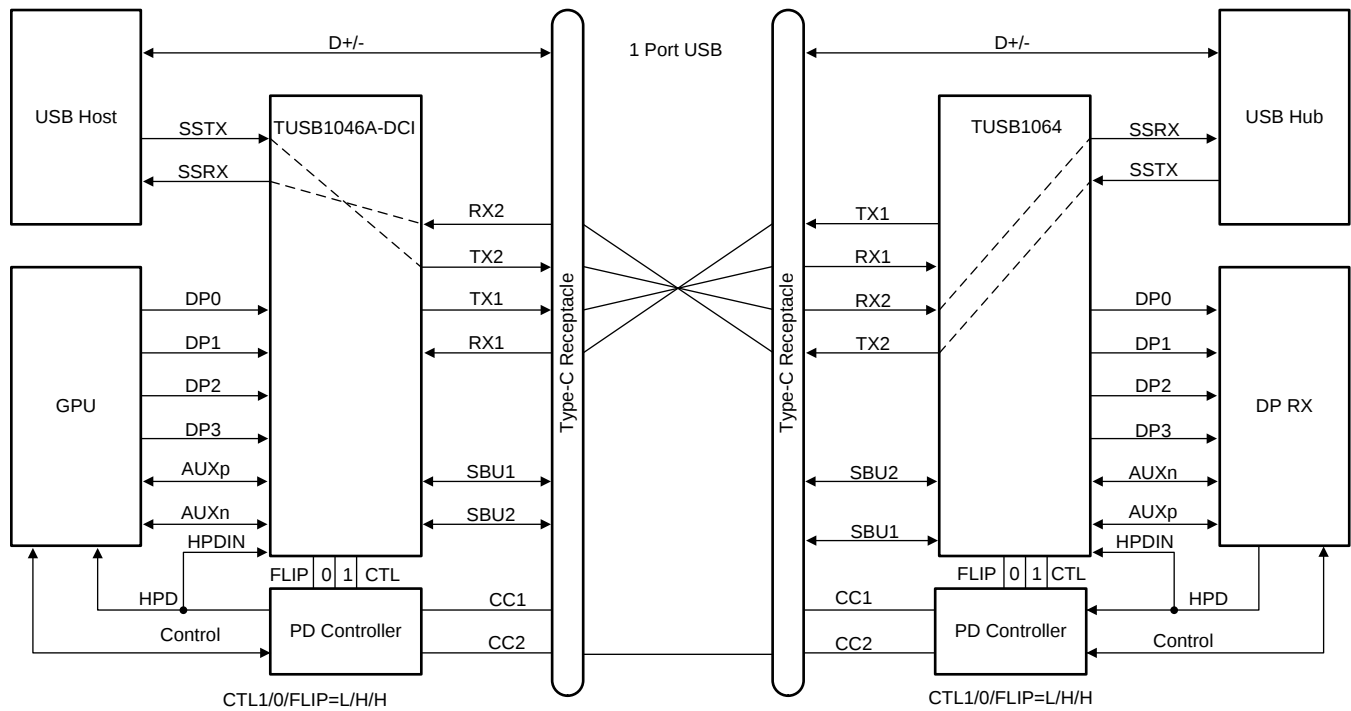
### 9.3.1 USB 3.1 Only

The TUSB1046-DCI is in USB3.1 only when the CTL1 pin is low and CTL0 pin is high.



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**Figure 30. USB3.1 Only – No Flip (CTL1 = L, CTL0 = H, FLIP = L)**

**System Examples (continued)**


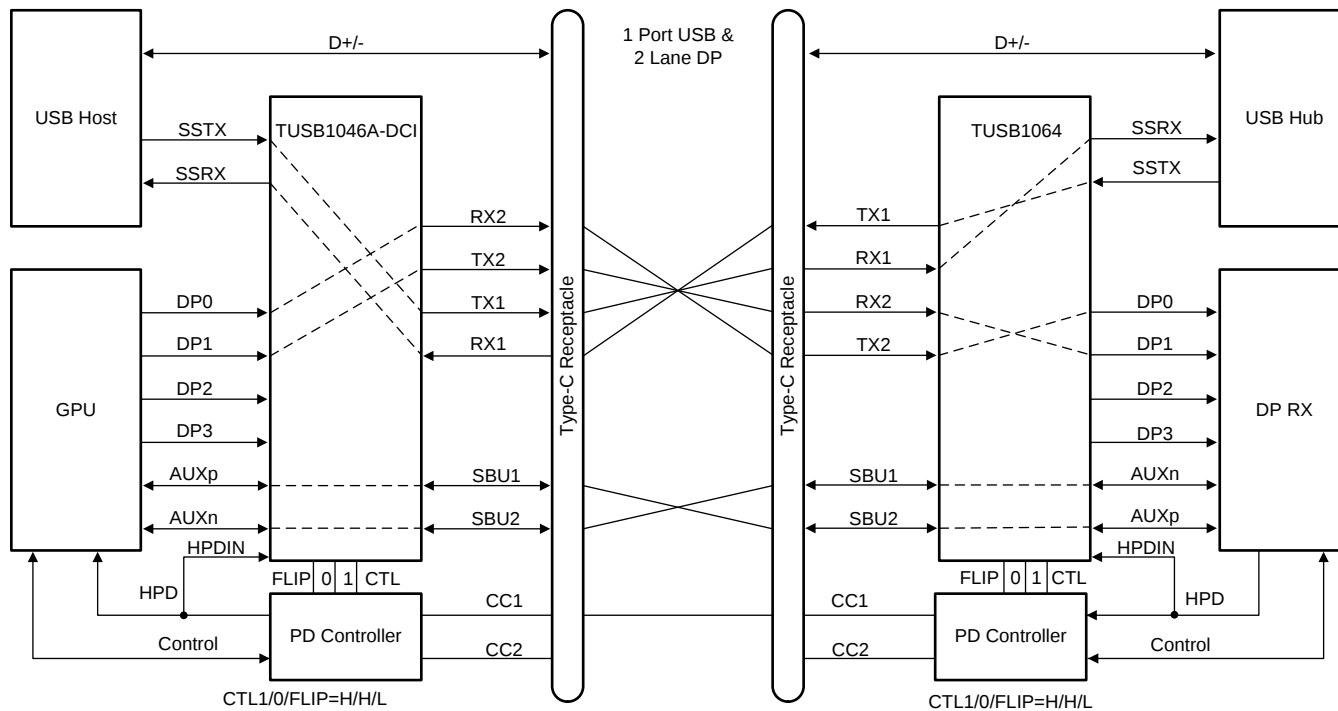
Copyright © 2017, Texas Instruments Incorporated

**Figure 31. USB3.1 Only – With Flip (CTL1 = L, CTL0 = H, FLIP = H)**

## System Examples (continued)

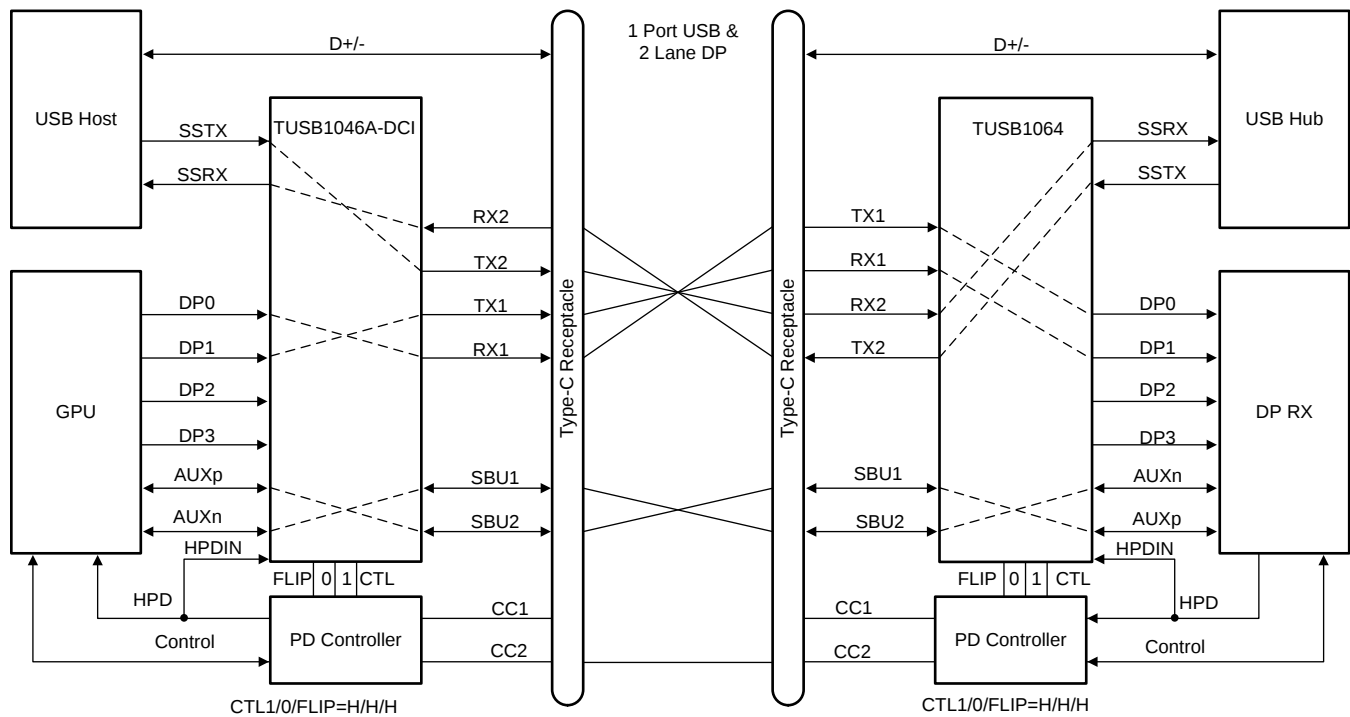
### 9.3.2 USB 3.1 and 2 Lanes of DisplayPort

The TUSB1046-DCI operates in USB3.1 and 2 Lanes of DisplayPort mode when the CTL1 pin is high and CTL0 pin is high.



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**Figure 32. USB3.1 + 2 Lane DP – No Flip (CTL1 = H, CTL0 = H, FLIP = L)**

**System Examples (continued)**


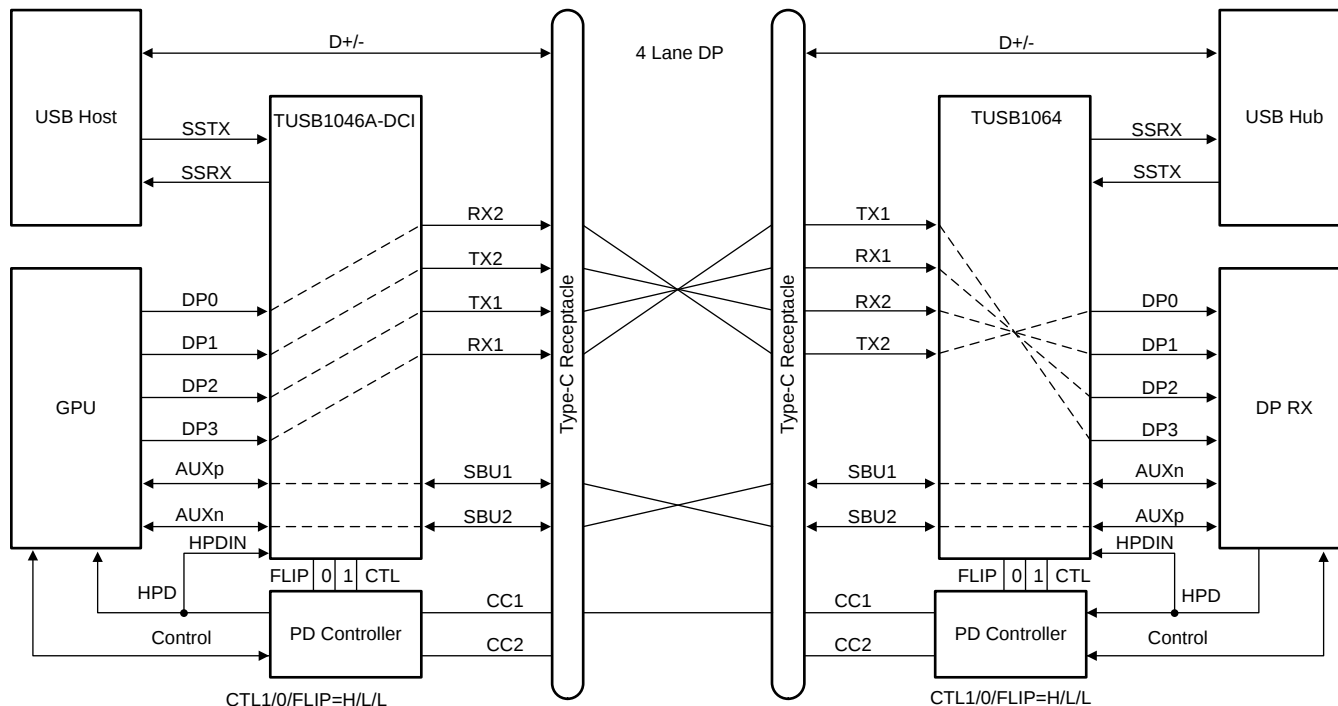
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**Figure 33. USB 3.1 + 2 Lane DP – Flip (CTL1 = H, CTL0 = H, FLIP = H)**

## System Examples (continued)

### 9.3.3 DisplayPort Only

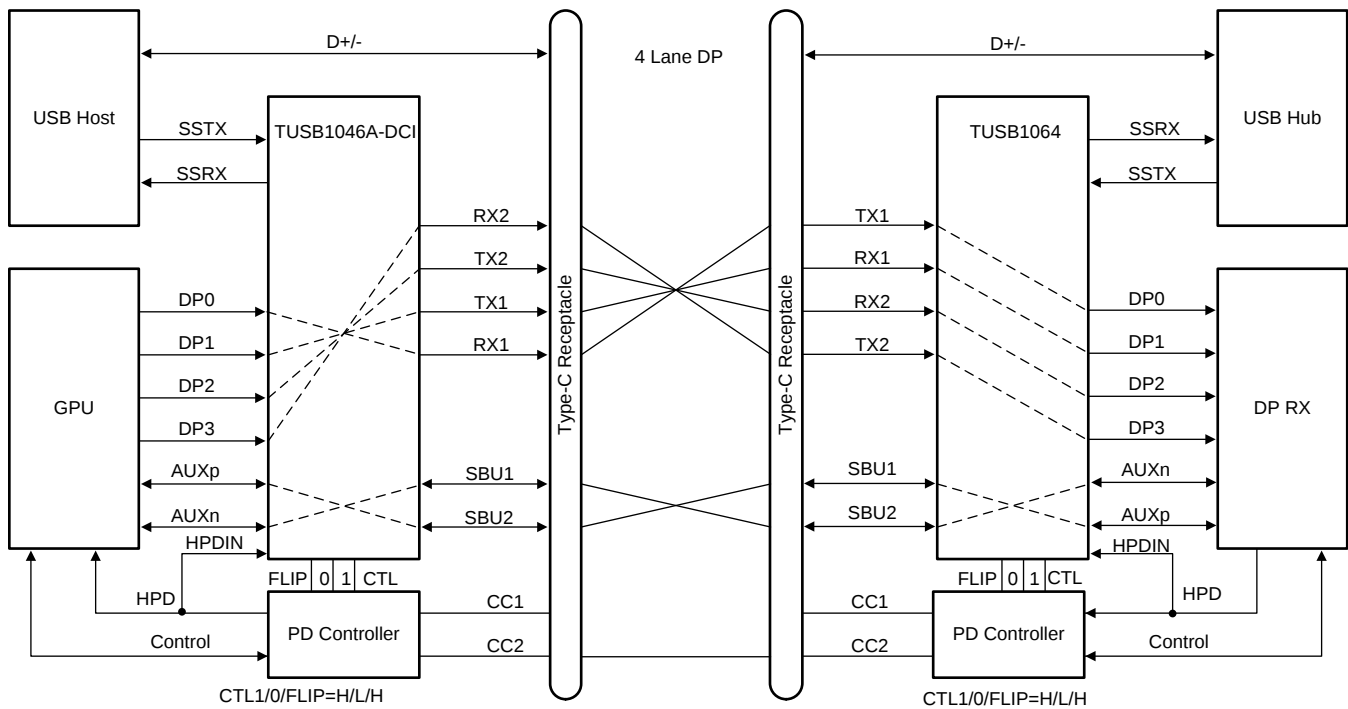
The TUSB1046-DCI operates in 4 Lanes of DisplayPort only mode when the CTL1 pin is high and CTL0 pin is low.



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**Figure 34. Four Lane DP – No Flip (CTL1 = H, CTL0 = L, FLIP = L)**

## System Examples (continued)



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**Figure 35. Four Lane DP – With Flip (CTL1 = H, CTL0 = L, FLIP = H)**

## 10 Power Supply Recommendations

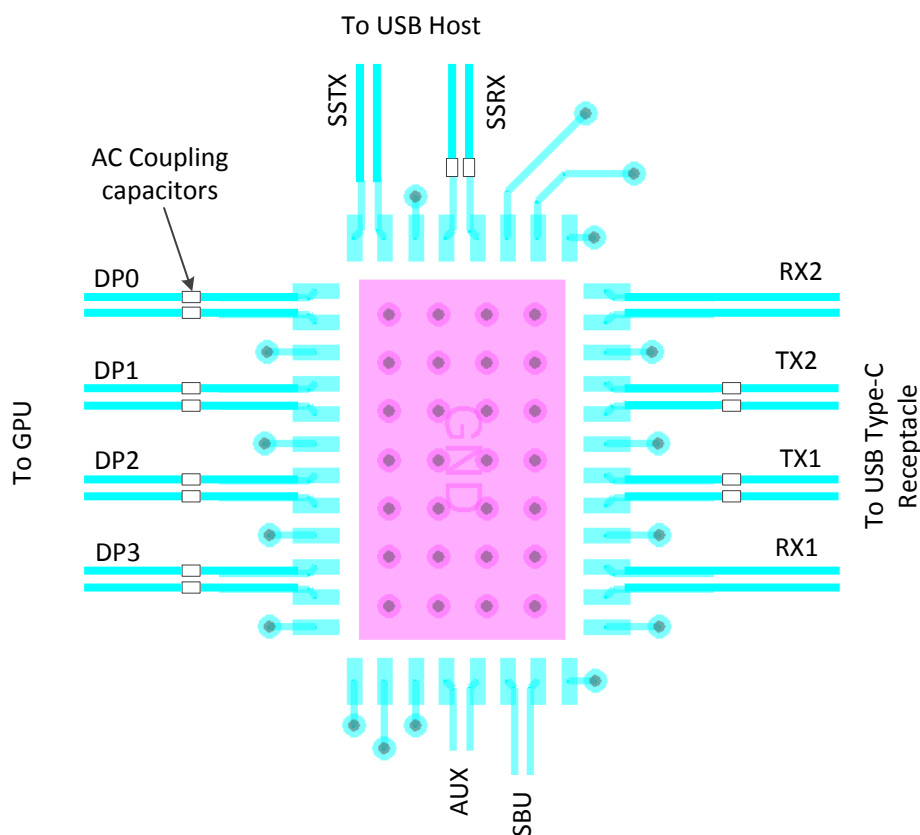
The TUSB1046-DCI is designed to operate with a 3.3-V power supply. Levels above those listed in the [Absolute Maximum Ratings](#) table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3 V. Decoupling capacitors should be used to reduce noise and improve power supply integrity. A 0.1-μF capacitor should be used on each power pin.

## 11 Layout

### 11.1 Layout Guidelines

1. RXP/N and TXP/N pairs should be routed with controlled 90-Ω differential impedance ( $\pm 15\%$ ).
2. Keep away from other high speed signals.
3. Intra-pair routing should be kept to within 2 mils.
4. Length matching should be near the location of mismatch.
5. Each pair should be separated at least by 3 times the signal trace width.
6. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be  $\geq 135$  degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
7. Route all differential pairs on the same of layer.
8. The number of vias should be kept to a minimum. It is recommended to keep the vias count to 2 or less.
9. Keep traces on layers adjacent to ground plane.
10. Do not route differential pairs over any plane split.
11. Adding Test points will cause impedance discontinuity, and therefore, negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

### 11.2 Layout Example



**Figure 36. Layout Example**

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 20. Related Links**

| PARTS          | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|----------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TUSB1046A-DCI  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TUSB1046AI-DCI | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

USB Type-C is a trademark of USB Implementers Forum.

DisplayPort is a trademark of VESA.

VESA is a registered trademark of Video Electronics Standards Association Corporation California.

All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TUSB1046A-DCIRNQR</a>  | Active        | Production           | WQFN (RNQ)   40 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | TUSB46              |
| TUSB1046A-DCIRNQR.B                | Active        | Production           | WQFN (RNQ)   40 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | TUSB46              |
| <a href="#">TUSB1046A-DCIRNQT</a>  | Active        | Production           | WQFN (RNQ)   40 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | TUSB46              |
| TUSB1046A-DCIRNQT.B                | Active        | Production           | WQFN (RNQ)   40 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | TUSB46              |
| TUSB1046ADCIRNQRG4                 | Active        | Production           | WQFN (RNQ)   40 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TUSB46              |
| TUSB1046ADCIRNQRG4.B               | Active        | Production           | WQFN (RNQ)   40 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TUSB46              |
| <a href="#">TUSB1046AI-DCIRNQR</a> | Active        | Production           | WQFN (RNQ)   40 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TUSB46              |
| TUSB1046AI-DCIRNQR.B               | Active        | Production           | WQFN (RNQ)   40 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TUSB46              |
| <a href="#">TUSB1046AI-DCIRNQT</a> | Active        | Production           | WQFN (RNQ)   40 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TUSB46              |
| TUSB1046AI-DCIRNQT.B               | Active        | Production           | WQFN (RNQ)   40 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TUSB46              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TUSB1046A-DCIRNQR  | WQFN         | RNQ             | 40   | 3000 | 330.0              | 12.4               | 4.3     | 6.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TUSB1046A-DCIRNQT  | WQFN         | RNQ             | 40   | 250  | 180.0              | 12.4               | 4.3     | 6.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TUSB1046ADCIRNQRG4 | WQFN         | RNQ             | 40   | 3000 | 330.0              | 12.4               | 4.3     | 6.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TUSB1046AI-DCIRNQR | WQFN         | RNQ             | 40   | 3000 | 330.0              | 12.4               | 4.3     | 6.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TUSB1046AI-DCIRNQT | WQFN         | RNQ             | 40   | 250  | 180.0              | 12.4               | 4.3     | 6.3     | 1.1     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TUSB1046A-DCIRNQR  | WQFN         | RNQ             | 40   | 3000 | 360.0       | 360.0      | 36.0        |
| TUSB1046A-DCIRNQT  | WQFN         | RNQ             | 40   | 250  | 210.0       | 185.0      | 35.0        |
| TUSB1046ADCIRNQRG4 | WQFN         | RNQ             | 40   | 3000 | 367.0       | 367.0      | 35.0        |
| TUSB1046AI-DCIRNQR | WQFN         | RNQ             | 40   | 3000 | 360.0       | 360.0      | 36.0        |
| TUSB1046AI-DCIRNQT | WQFN         | RNQ             | 40   | 250  | 210.0       | 185.0      | 35.0        |



### WQFN - 0.8 mm max height

The drawing consists of three views: a top view, a side view, and a detail view of the pin index area.

- Top View:** Shows the overall footprint of the connector. The total width is 6.1 (5.9). The total height is 4.1 (3.9). The pin index area is defined by a 4.7±0.1 width and a 2.7±0.1 height. The pin index area contains 20 pins, with 10 pins on each side. The pin index area is defined by a 4.7±0.1 width and a 2.7±0.1 height. The pin index area contains 20 pins, with 10 pins on each side. The pin index area is defined by a 4.7±0.1 width and a 2.7±0.1 height. The pin index area contains 20 pins, with 10 pins on each side.
- Side View:** Shows the profile of the connector. The total height is 0.8 MAX. The pin index area is defined by a 0.05 height and a 0.00 offset. The pin index area is defined by a 0.05 height and a 0.00 offset. The pin index area is defined by a 0.05 height and a 0.00 offset. The pin index area is defined by a 0.05 height and a 0.00 offset.
- Detail View:** Shows the pin index area in more detail. The pin index area is defined by a 4.7±0.1 width and a 2.7±0.1 height. The pin index area contains 20 pins, with 10 pins on each side. The pin index area is defined by a 4.7±0.1 width and a 2.7±0.1 height. The pin index area contains 20 pins, with 10 pins on each side.

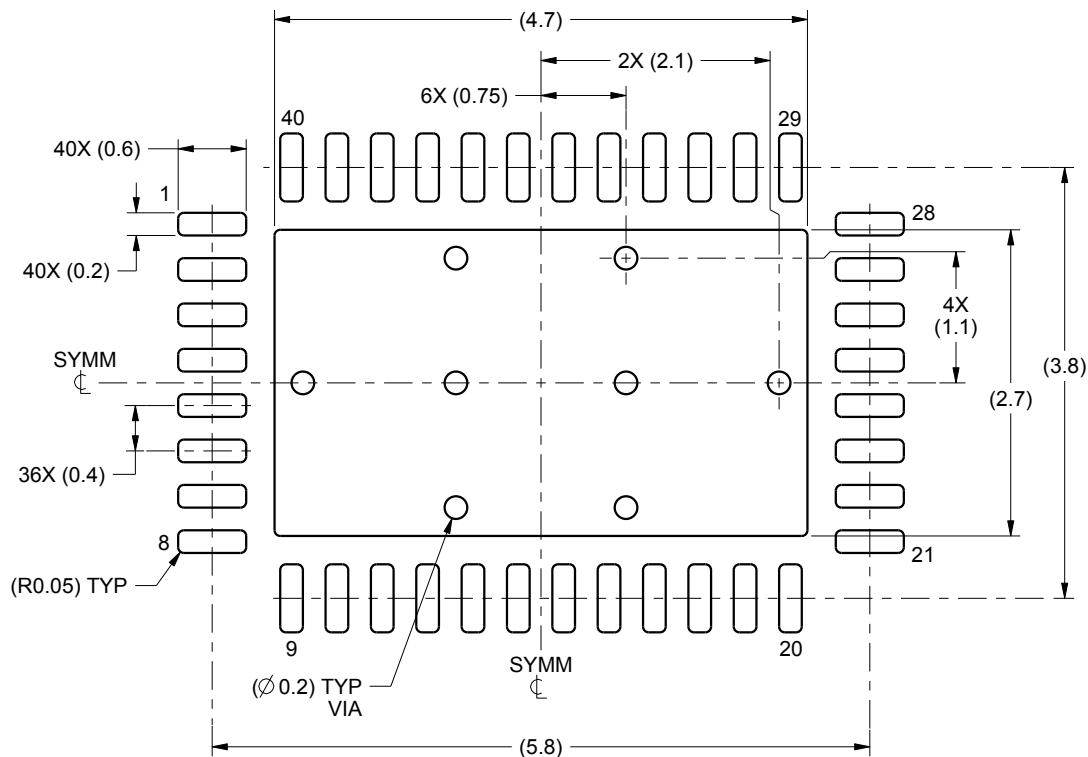
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

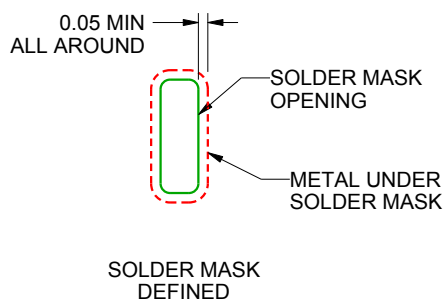
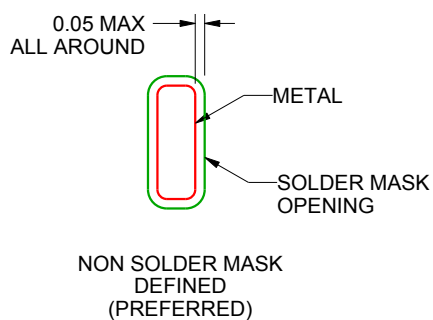
RNQ0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

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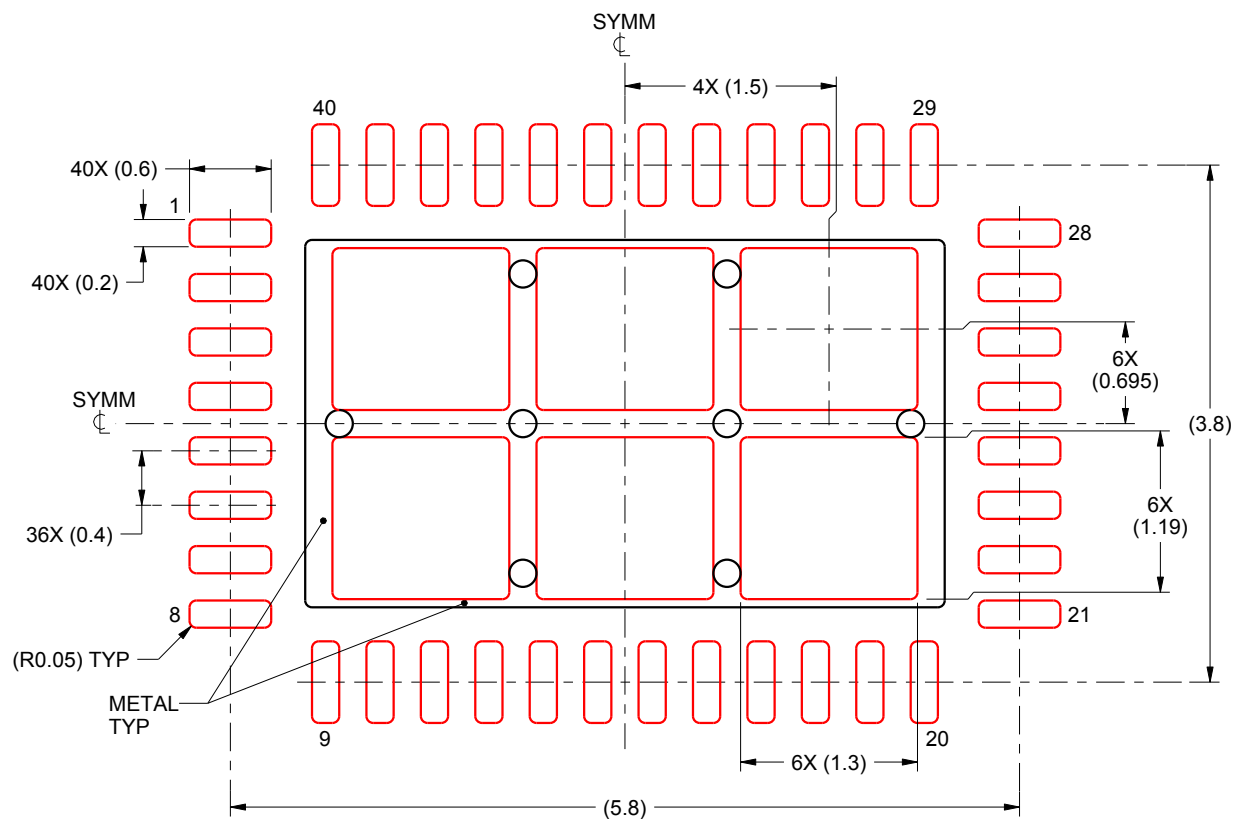
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

**RNQ0040A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
**BASED ON 0.1 mm THICK STENCIL**

**EXPOSED PAD**  
**73% PRINTED SOLDER COVERAGE BY AREA**  
**SCALE:18X**

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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