TUSB542 USB Type-C^{TM} 5Gbps Redriver 2:1 MUX

1 Features

- Provides USB 3.1 Gen-1 5Gbps Super Speed (SS) 2:1 mux for a USB Type-C™ port
- Supports USB Type-C cable and connector specifications
- Ultra low-power architecture:
  - Active 100mA
  - U2/U3 1.3mA
  - No connection 300μA
- Selectable equalization up to 9dB, de-emphasis, and output swing up to 6dB
- Integrated termination
- RX-detect function
- Signal monitoring for power management
- No host or device side requirement – supports USB-C DFP, UFP or DRP port
- Single supply voltage 1.8V ±10%
- Industrial temperature range of –40 – 85°C

2 Applications

- USB 3.1 Gen 1 SS application:
  - Phones
  - Tablets, phablets, and notebooks
  - Docking stations

3 Description

The TUSB542 is a dual channel USB 3.1 Gen1 (5Gbps), also known as USB-C, re-driver supporting systems with USB Type-C connectors. The device offers signal conditioning plus the ability to switch the USB SS signals for the USB Type-C flippable connector. The TUSB542 can be controlled through the SEL pin by an external Configuration Channel Logic Controller to properly mux the signals.

The TUSB542 incorporates receiver equalization and transmitter de-emphasis to maintain signal integrity on both transmit and receive data paths. The receiver equalization offers multiple gain settings to overcome channel degradation from insertion loss and inter-symbol interference. To compensate for downstream transmission line losses, the output driver supports de-emphasis configuration. Additionally, automatic LFPS de-emphasis control allows for full compliance.

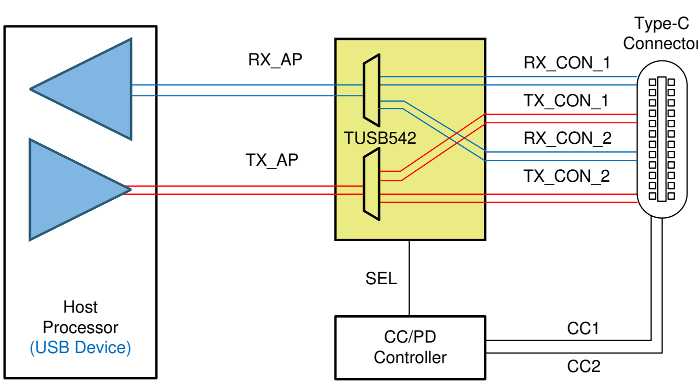
The TUSB542 offers low power consumption on a 1.8V supply with its ultra-low power architecture. The re-driver supports low power modes, which further reduce the idle power consumption.

The USB Type-C redriver is available in a small ultra-thin package, which is an excellent choice for many portable applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TUSB542	RWQ (X2QFN, 18)	2.4mm × 2mm

(1) For more information, see Section 10
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

Sample Application

Table of Contents

4 Pin Configuration and Functions

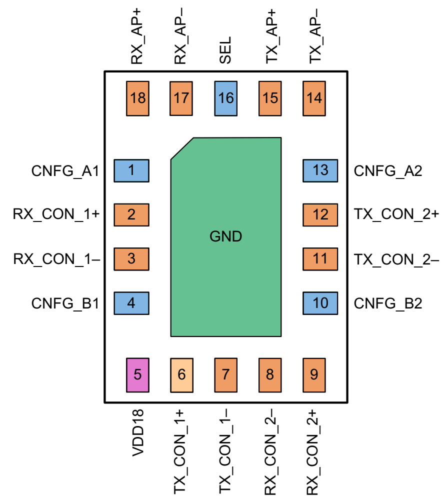


Figure 4-1. RWQ Package, 18-Pin X2QFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VDD18	5	P	1.8V Power Supply
GND	PAD	G	Reference Ground Thermal Pad. Must connect to GND on the board.
SEL	16	Input	2:1 SS MUX control. See Table 1 for signal path settings.210kΩ internal pullup resistor. H: AP SS signals are connected to Type-C position 1 signals. L: AP SS signals are connected to Type-C position 2 signals
CNFG_A1	1	Tri-level Input	Tri-level configuration input pin A1 (for Ch 1): sets channel 1 (AP to redriver) EQ, DE and OS configurations. Pin has integrated pull-up and pull-down resistors of 105kΩ. Refer to Table 6-2 for configuration settings.
CNFG_B1	4	Tri-level Input	Tri-level configuration input pin B1 (for Ch 1): sets channel 1 (AP to redriver) EQ, DE and OS configurations. Pin has integrated pull-up and pull-down resistors of 105kΩ. Refer to Table 6-2 for configuration settings.
CNFG_A2	13	Tri-level Input	Tri-level configuration input pin A2 (for Ch 2): sets channel 2 (redriver to device) EQ, DE and OS configurations. Pin has integrated pull-up and pull-down resistors of 10 5kΩ. Refer to Table 6-2 for configuration settings.
CNFG_B2	10	Tri-level Input	Tri-level configuration input pin B2 (for Ch 2): sets channel 2 (redriver to device) EQ, DE and OS configurations. Pin has integrated pull-up and pull-down resistors of 105kΩ. Refer to Table 6-2 for configuration settings.
RX_AP+	18	Diff output	Differential output to Application Processor (AP), 5 Gbps SS positive signal
RX_AP-	17	Diff output	Differential output to AP, 5Gbps SS negative signal
TX_AP+	15	Diff input	Differential input from AP, 5Gbps SS positive signal
TX_AP-	14	Diff input	Differential input from AP, 5Gbps SS negative signal
Rx_Con_1+	2	Diff input	Differential input from Type-C Connector, Position 1, SS positive signal
Rx_Con_1-	3	Diff input	Differential input from Type-C Connector, Position 1, SS negative signal
Tx_Con_1+	6	Diff output	Differential output to Type-C Connector, Position 1, SS positive signal
Tx_Con_1-	7	Diff output	Differential output to Type-C Connector, Position 1, SS negative signal
Rx_Con_2-	8	Diff input	Differential input from Type-C Connector, Position 2, SS negative signal
Rx_Con_2+	9	Diff input	Differential input from Type-C Connector, Position 2, SS positive signal
Tx_Con_2+	12	Diff output	Differential output to Type-C Connector, Position 2, SS positive signal
Tx_Con_2-	11	Diff output	Differential output to Type-C Connector, Position 2, SS negative signal

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage range, V_{CC}		–0.3	2.3	V
Voltage range at any input or output terminal	Differential I/O	–0.3	1.5	V
	CMOS Inputs	–0.3	2.3	V
Junction temperature, T_J		-40	105	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Main power supply	1.62	1.8	1.98	V
T_A	Operating free-air temperature	–40		85	°C
$C_{(AC)}$	AC coupling capacitor required for TX pins	75		200	nF
$V_{(PSN)}$	AC coupling capacitor required for TX pins			100	mV
$t_{(VCC\_RAMP)}$	V_{CC} supply ramp requirement	0.2		40	ms
$R_{(pullup-down)}$	Pull-up/down resistor to control CNF pins			2.2	kΩ

5.4 Thermal Information

THERMAL METRIC[1]		TUSB542 X2QFN (RWQ) 18 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	49.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics, Power Supply Currents

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
ICC(ACTIVE)	Average active current; link in U0 with SuperSpeed data transmission; OS = 0.9V; DE = 0dB		100	130	mA
ICC(U2/U3)	Average current in U2/U3		1.3		mA
ICC(NC)	Average current with no connection No SuperSpeed device is connected to TXP/TXN		0.3		mA

5.6 Electrical Characteristics, DC

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRI-STATE CMOS INPUTS (CNFG_A1, CNFG_B1, CNFG_A2 and CNFG_B2)						
V_{IH}	High-level input voltage		V_{CC} x 0.75			V
V_{IM}	Mid-level input voltage			V_{CC} / 2		V
V_{IL}	Mid-level input voltage				V_{CC} x 0.25	V
V_F	Floating voltage	V_{IN} = High impedance		V_{CC} / 2		V
$R_{(PU)}$	Internal pull-up resistance			105		kΩ
$R_{(PD)}$	Internal pull-down resistance			105		kΩ
I_{IH}	High-level input current	V_{IN} = 1.98V			26	µA
I_{IL}	Low-level input current	V_{IN} = GND	–26			µA
I_{lkg}	External leakage current (from application board + Application Processor pin high impedance) tolerance	V_{IN} = GND or V_{IN} = 1.98V	–1		1	µA
CMOS INPUT – SEL						
V_{IH}	High-level input voltage		V_{CC} x 0.7			V
V_{IL}	Mid-level input voltage				V_{CC} x 0.3	V
I_{IH}	High-level input current	V_{IN} = 1.98V			5	µA
I_{IL}	Low-level input current	V_{IN} = GND	–16			µA

5.7 Electrical Characteristics, Dynamic

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential Receiver						
$V_{(RX-DC-CM)}$	RX DC common mode voltage		0		2	V
$R_{(RX-CM-DC)}$	Receiver DC common mode impedance	Measured at connector. Present when SuperSpeed USB device detected on TX pins.	18		30	Ω
$R_{(RX-DIFF-DC)}$	Receiver DC differential impedance	Measured at connector. Present when SuperSpeed USB device detected on TX pins.	72		120	Ω
$Z_{(RX-HIGH-IMP-DC-POS)}$	DC input CM input impedance when termination is disabled.	Measured at connector. Present when no SuperSpeed USB device detected on TX pins or while V_{CC} is ramping.	25			kΩ
$V_{(RX-LFPS-DET-DIFF-P-P)}$	LFPS Detect threshold. Below min is noise.	Measured at connector. Below min is squelched.	0.1		0.3	V
$V_{(RX-CM-AC-P)}$	Peak RX AC common mode voltage	Measured at package pin.			150	mV
$C_{(RX-PARASITIC)}$	Rx Input capacitance for return loss	At package pin to AC GND.			1.1	pF
Differential Transmitter						
$V_{(TX-DIFF-PP)}$	Differential peak-to-peak TX voltage swing	OS Low, 0dB DE		0.9		V
		OS High, 0dB DE		1.1		V
$V_{(TX-DIFF- PP-LFPS)}$	LFPS differential voltage swing	OS Low, High	0.8		1.2	V
$V_{(TX-DE- RATIO)}$	Transmitter de-emphasis	Low		0		dB
		Mid		3.5		dB
		High		6		dB
$V_{(TX-RCV-DETECT)}$	The amount of voltage change allowed during Receiver Detection.				0.6	V
$V_{(TX-DC-CM)}$	TX DC common mode voltage	The instantaneous allowed DC common-mode voltage at connector side of AC coupling capacitor.	0		2	V
$V_{(TX-IDLE-DIFF-AC-PP)}$	AC Electrical Idle differential peak-to-peak output voltage	At package pin.	0		10	mV
$V_{(TX-IDLE-DIFF\_DC)}$	DC Electrical Idle differential output voltage	At package pin. After low pass filter to remove AC component.	0		10	nV
$V_{(TX-CM-DC-ACTIVE-IDLE-DELTA)}$	Absolute DC common mode voltage between U1 and U0.	At package pin.			0.2	V
$I_{(TX-SHORT)}$	TX short-circuit current limit				60	mA
$R_{(TX-DC)}$	TX DC common mode impedance	At package pins	18		30	Ω
$R_{(TX-DIFF-DC)}$	TX DC differential impedance		72		120	Ω
$C_{(TX-PARASTIC)}$	TX input capacitance for return loss	At package pins to AC GND			1.25	pF
$T_{(jitter)}$	Total Residual Jitter (peak to peak)			12		ps

5.8 Electrical Characteristics, AC

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Xtalk	Differential Cross talk between TX and RX Signal Pairs	at 2.5 GHz, TX to RX		–45		dB

5.9 Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{IDLEEntry}$	Delay from U0 to electrical idle.	See Figure 5-2		6		ns
$t_{IDLEExit\_U1}$	U1 exit time: break in electrical idle to the transmission of LFPS	See Figure 5-2		6		ns
$t_{IDLEExit\_U2U3}$	U2/U3 exit time: break in electrical idle to transmission of LFPS	From the time when the far end terminations detected for both ports		1		µs
$t_{IDLEExit\_DISC}$	U2/U3 exit time: break in electrical idle to transmission of LFPS	From the time when the far end terminations detected for both ports		2		µs
$t_{DIFF\text{-}DLY}$	Differential propagation delay.	See Figure 5-1		225		ps
$t_{PWRUPACTIVE}$	Time when V_{CC} reach 80% to device active				30	ms

5.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{TX\text{-}RISE\text{-}FALL}$	Transmitter rise/fall time (see Figure 3)	20% to 80% of differential output. At device pins.		80		ps
$t_{RF\text{-}MISMATCH}$	Transmitter rise/fall mismatch	20% to 80% of differential output. At device pins			2.3	ps

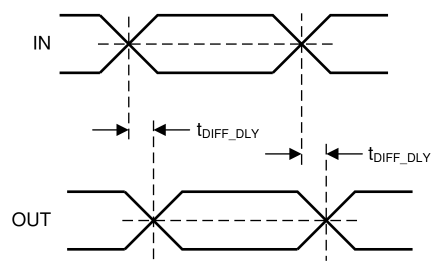


Figure 5-1. Propagation Delay Timing

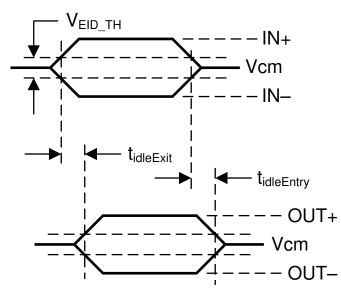


Figure 5-2. Electrical Idle Mode Exit and Entry Delay Timing

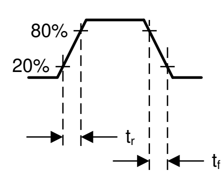
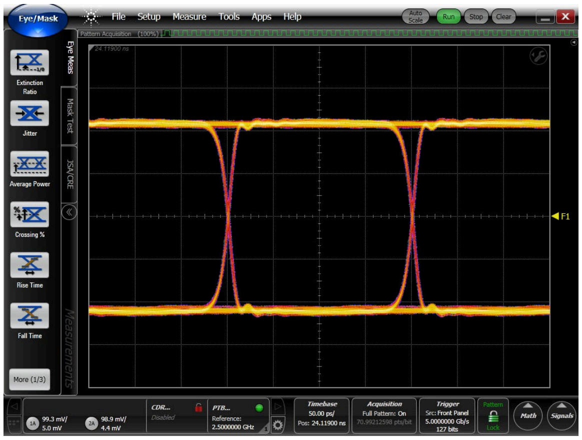


Figure 5-3. Output Rise and Fall Times

5.11 Typical Characteristics

5.11.1 1-Inch Pre Channel



880 mV 5Gbps

Figure 5-4. Input Signal: 1-Inch Input Trace

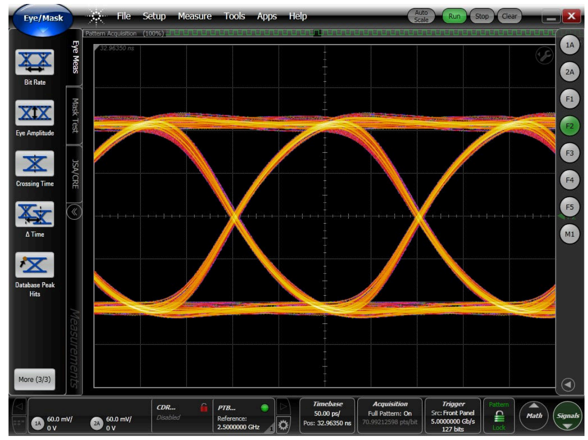


Figure 5-5. Output Signal: 12-Inches Output Trace

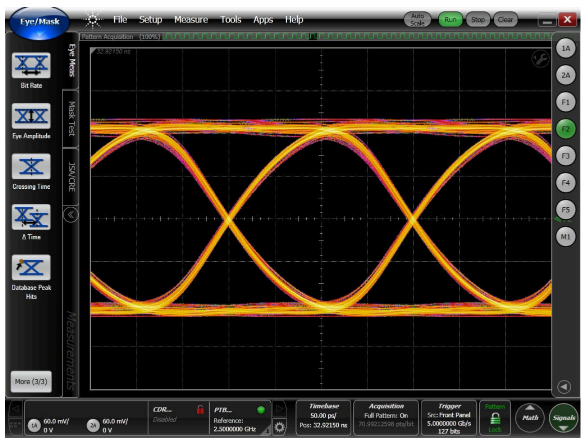


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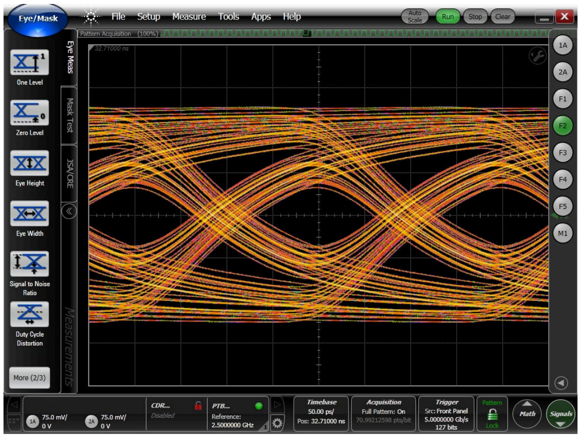
Figure 5-6. Output Signal: 16-Inches Output Trace

5.11.2 24-Inch Pre Channel



880 mV 5Gbps

Figure 5-7. Input Signal: 24-Inch Input Trace

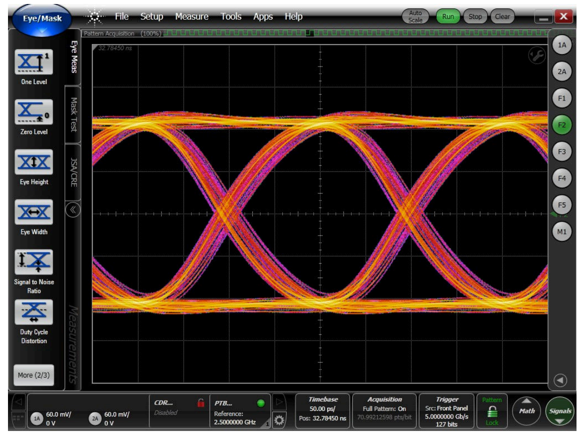


Figure 5-8. Output Signal: 12-Inches Output Trace

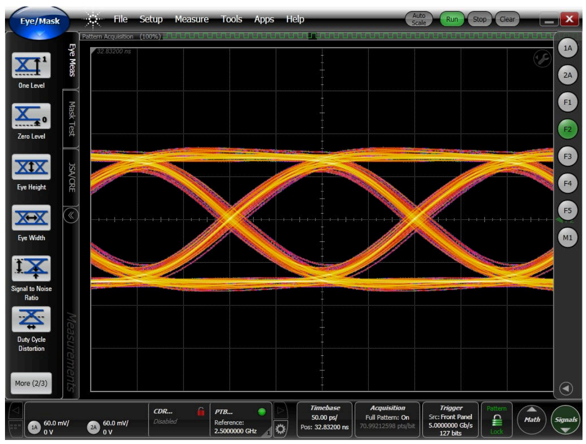
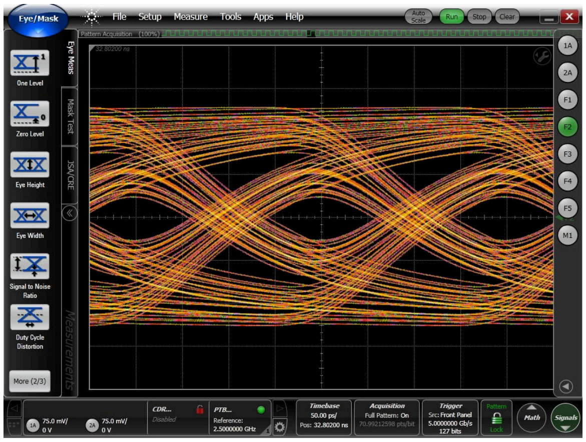


Figure 5-9. Output Signal: 24-Inches Output Trace

5.11.3 32-Inch Pre Channel



880 mV 5Gbps

Figure 5-10. Input Signal: 32-Inch Input Trace

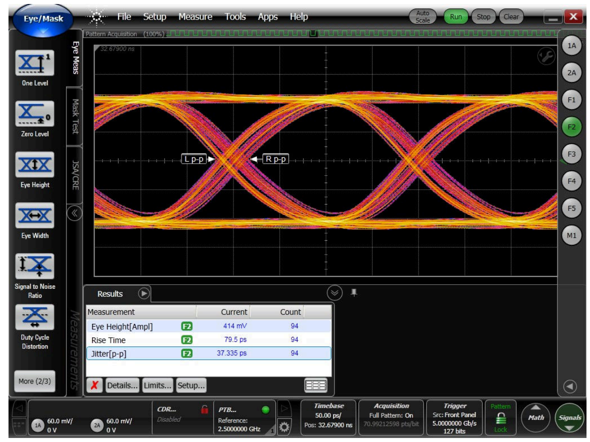


Figure 5-11. Output Signal: 12-Inches Output Trace

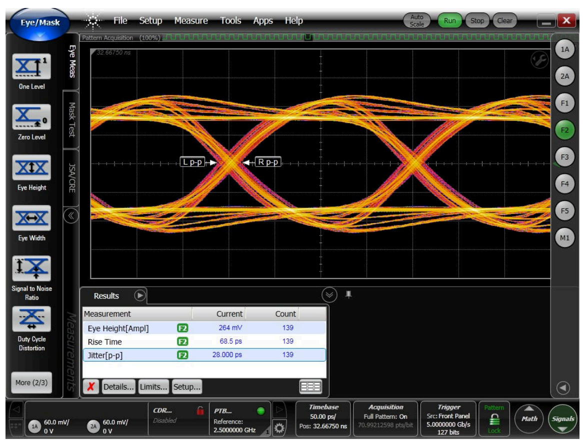


Figure 5-12. Output Signal: 24-Inches Output Trace

6 Detailed Description

6.1 Overview

TUSB542 is an active re-driver for USB 3.1 Gen1 applications; it supports Type-C applications, as well as switching between two Hosts and one device (or vice versa). The device is a dual channel USB 3.1 Gen1 (5Gbps) re-driver supporting systems with USB Type-C connectors. The TUSB542 can be controlled through the SEL, and is best controlled using an external Configuration Channel Logic or Power Delivery Controller to properly mux the signals in Type-C applications.

When 5Gbps Super Speed USB signals travel across a PCB or cable, signal integrity degrades due to loss and inter-symbol interference. The TUSB542 recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. This extends the possible channel length, and enables systems to pass USB 3.1 compliance.

The TUSB542 advanced state machine makes it transparent to hosts and devices. After power up, the TUSB542 periodically performs receiver detection on the TX pair. If it detects a SS USB receiver, the RX termination is enabled, and the TUSB542 is ready to re-drive.

The TUSB542 operates over the industrial temperature range of –40°C to 85°C in the 2 mm x 2.4 mm X2QFN package. The device ultra-low power architecture operates at a 1.8V power supply. The automatic LFPS DeEmphasis control further enables the system to be USB 3.0 compliant. An advanced state machine inside the device monitors the USB SS traffic to perform enhanced power management to operate in no-connect, U2, U3 and active modes.

The USB Type-C connector is designed to allow insertion either upside-up or downside-up. The TUSB542 supports this feature by routing the AP signals to one of two output channels. The SEL input control defines the way that the AP side signals is routed on the re-driver device side. Table 6-1 lists the active MUX configurations based on the SEL input.

Table 6-1. USB SS MUX Control

SEL	Tx_Con_1	Rx_Con_1	Tx_Con_2	Rx_Con_2
H	TX_AP	RX_AP	GND	GND (1)
L	GND	GND (1)	TX_AP	RX_AP

(1) Terminated through 50 K (minimum) resistors

The TUSB542 has flexible configurations to optimize the device using GPIO control pins. Figure 6-1 shows a typical signal chain for mobile applications. Channel 1 is between Application Processor (AP) and TUSB542, Channel 2 is between the TUSB542 redriver and the downstream device. The CNFG_A1 and CNFG_B1 pins provide signal integrity configuration settings for channel 1, while CNFG_A2 and CNFG_B2 pins control the operation of Channel 2 as listed in Table 6-2.

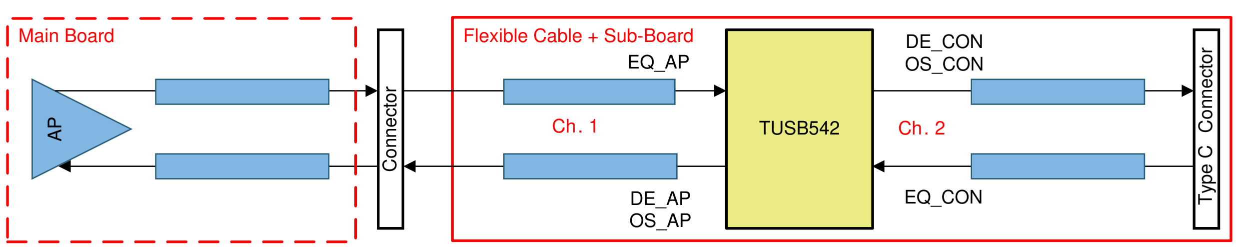


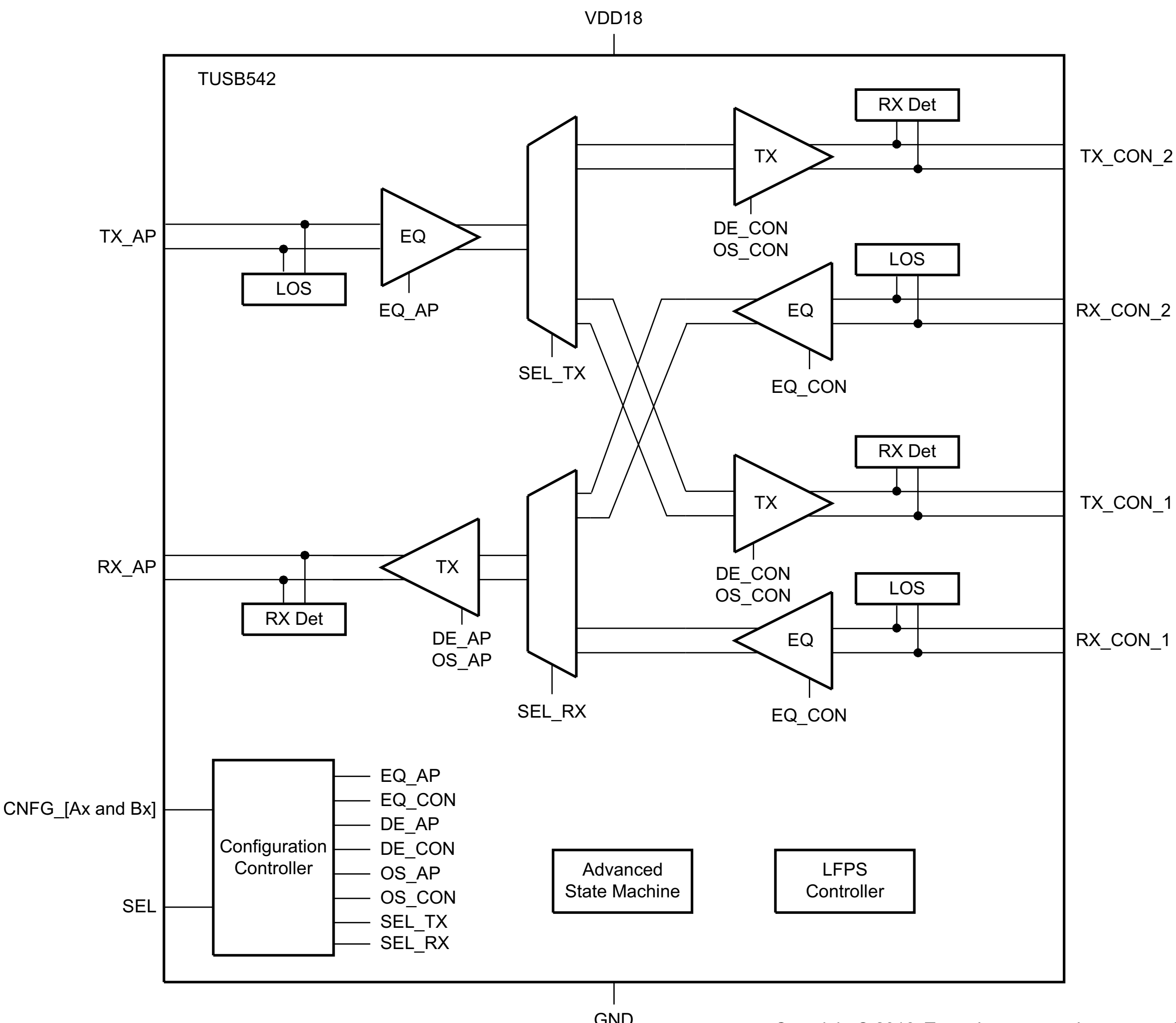
Figure 6-1. Typical Channels

The receiver (RX) of the device provides the flexibility of 0, 3, 6 and 9dB of equalization, while the transmitter (TX) provides the options of 0, 3.5 or 6dB de-emphasis. The transmitter also supports output swing settings of 900 mV and 1.1V.

Table 6-2. Device Signal Conditioning Configuration Settings for TUSB542

Ch1 (AP-Redriver)		DE_AP (dB)	OS_AP (V)	EQ_AP (dB)	Ch2 (Redriver-Conn)		DE_Conn (dB)	OS_Conn (V)	EQ_Conn (dB)
CNFG_A1	CNFG_B1				CNFG_A2	CNFG_B2			
Low	Low	3.5	1.1	3	Low	Low	6	1.1	0
	Float	3.5	0.9	3		Float	3.5	1.1	0
	High	0	1.1	3		High	3.5	0.9	0
Float	Low	0	0.9	3	Float	Low	6	0.9	0
	Float	3.5	1.1	0		Float	3.5	1.1	6
	High	.35	0.9	0		High	3.5	0.9	6
High	Low	0	1.1	0	High	Low	6	1.1	6
	Float	0	0.9	0		Float	6	0.9	6
	High	6	1.1	6		High	6	1.1	9

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Receiver Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system before the input of the TUSB542 receiver. The receiver overcomes these losses by providing gain to the high frequency components of the signals with respect to the low frequency components. The proper gain setting should be selected to match the channel insertion loss before the receiver input of the TUSB542.

6.3.2 De-Emphasis Control and Output Swing

The output differential drivers of the TUSB542 provide selectable de-emphasis and output swing to achieve USB3.1 compliance, these options are configurable by means of 3-state control pins, and its available settings are listed on the Table 6-2. The level of de-emphasis required in the system depends on the channel length after the output of the re-driver. Figure 6-2 shows transmit bits with de-emphasis.

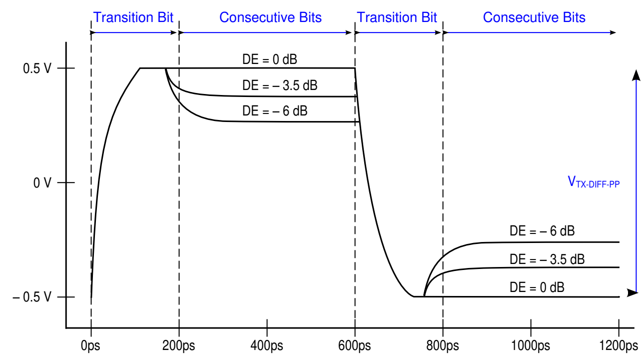


Figure 6-2. Transmitter Differential Voltage in Presence of De-Emphasis

6.3.3 Automatic LFPS Detection

The TUSB542 features an intelligent low frequency periodic signaling (LFPS) controller. The controller senses the low frequency signals and automatically disables the driver de-emphasis, for full USB3.1 compliance.

6.3.4 Automatic Power Management

The TUSB542 deploys RX detect, LFPS signal detection and signal monitoring to implement an automatic power management scheme to provide active, U2/U3 and disconnect modes. The automatic power management is driven by an advanced state machine, which is implemented to manage the device such that the re-driver operates smoothly in the links.

6.4 Device Functional Modes

6.4.1 Disconnect Mode

The Disconnect mode is the lowest power state of the TUSB542. In this state, the TUSB542 periodically checks for far-end receiver termination on both TX. Upon detection of the far-end receiver's termination on both ports, the TUSB542 will transition to U0 mode.

6.4.2 U Modes

6.4.2.1 U0 Mode

The U0 mode is the highest power state of the TUSB542. Anytime super-speed traffic is being received, the TUSB542 remains in this mode.

6.4.2.2 U2/U3 Mode

Next to the disconnect mode, the U2/U3 mode is next lowest power state. While in this mode, the TUSB542 periodically performs far-end receiver detection.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

TUSB542 is a USB 3.1 G1 5Gbps super speed 1:2 or 2:1 redriver de-multiplexer/multiplexer for RX and TX differential pairs. The device is host/device side agnostic and can be used for host or device switching.

7.2 Typical Applications, USB Type-C Port SS MUX

TUSB542 is optimized for USB Type-C port. The device provide multiplexing to select appropriate super speed RX and TX signal pairs resulting from Type-C plug orientation flipping. A companion USB PD or CC controller provides the MUX selection. The device can be used part of UFP, DFP or DRP Type-C port. Figure 7-1 shows typical Type-C applications.

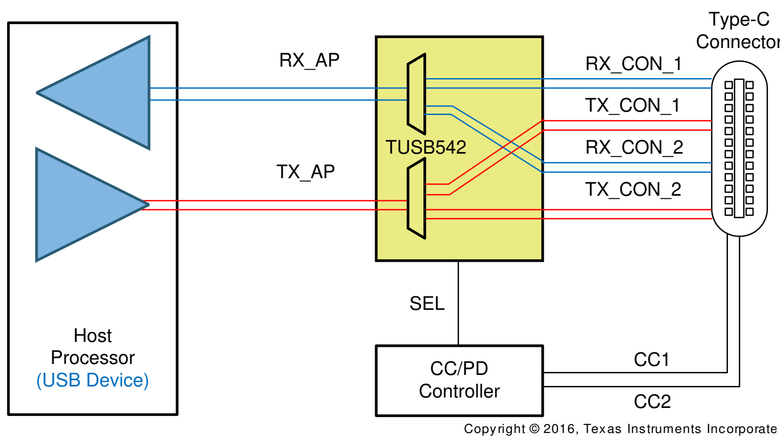


Figure 7-1. USB Type-C Host (Device) Application

7.2.1 Design Requirements

For this design example, use the parameters provided in *Design Parameters*.

The configured value depends on the physical channel (PCB layout) Equalization 0, 3, 6, 9dB (5Gbps) The configured value depends on the physical channel (PCB layout) de-emphasis 0, –3.5, –6dB The configured value depends on the physical channel (PCB layout) Differential impedance 72 - 120 Ω.

Table 7-1. Design Parameters

PARAMETER	VALUE	COMMENT
VDD18	1.8V	
AC Coupling Capacitors for SS signals	100 nF	75-200 nF range allowed. TUSB542 biases both input and output common mode voltage, hence ac-coupling caps as required on both sides. Note: TX pairs need to be biased at the connector.
Pull-up/down resistor to control CNF pins	4.7kΩ	
Input voltage range	100 mV to 1200 mV	
Output voltage range	900 mV to 1100 mV	

7.2.2 Detailed Design Procedure

Figure 7-2 shows an example implementation of an USB Type-C DRP port using TUSB542. Texas Instruments TUSB322 is shown here as channel configuration (CC) controller. Note: connections for CNFG pins of TUSB542 is an example only. The connection of the CNFG pins is application dependent; refer to Table 6-2, where the user can find the available settings.

It is recommended to run an overall system signal integrity analysis, to estimate the channel loss and configure the re-driver. It is also recommended to have pull-up and pull-down option on the configuration pins for debug and testing purposes.

The signal integrity analysis must determine the following:

- Equalization (EQ) setting
- De-emphasis (DE) setting
- Output swing amplitude (OS) setting

The equalization must be set based on the insertion loss in the pre-channel (channel before the TUSB542 device). The input voltage to the device is able to have a large range because of the receiver sensitivity and the available EQ settings.

The de-emphasis setting must be set based on the length and characteristics of the post channel (channel after the TUSB542 device).

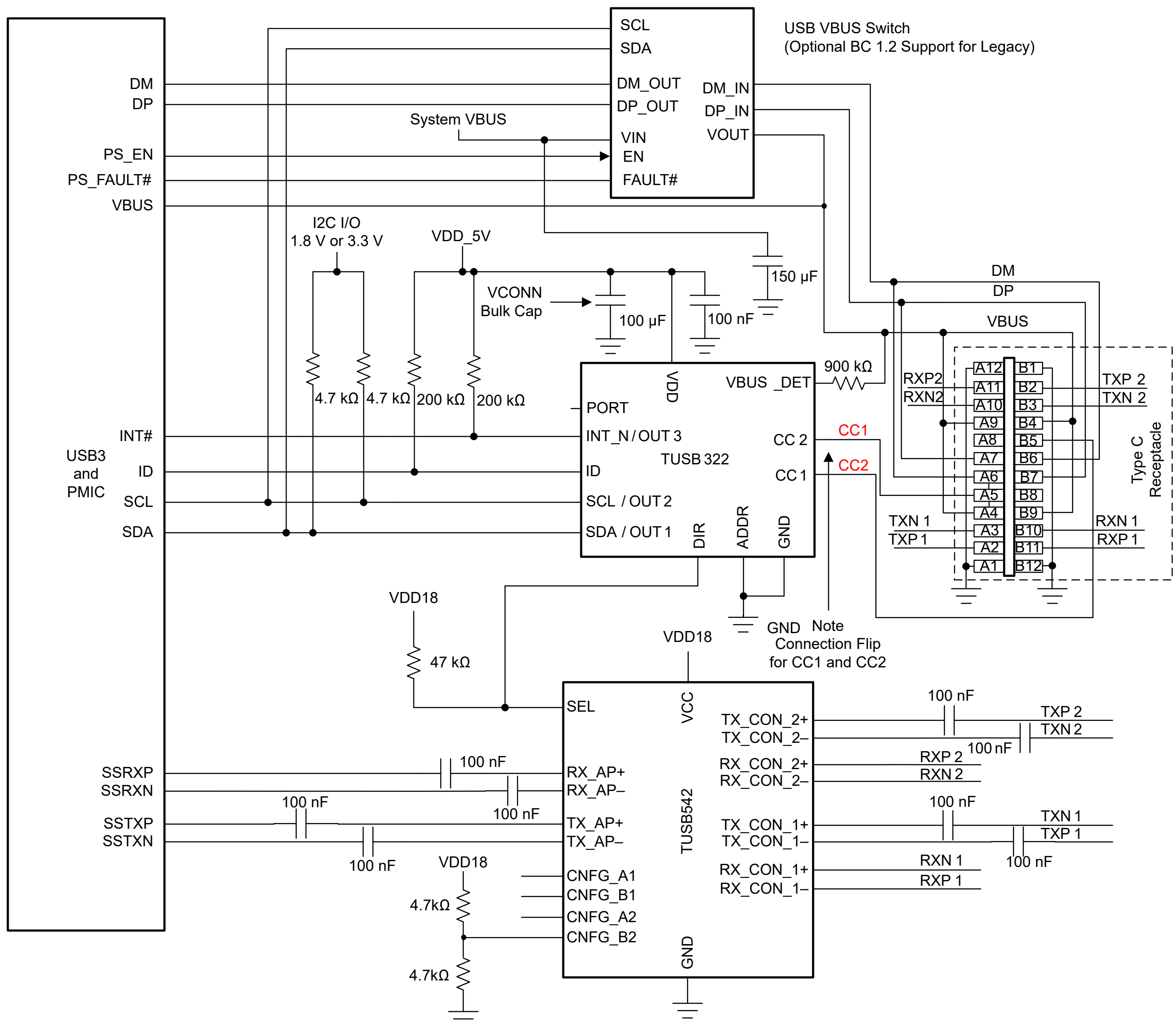


Figure 7-2. USB-C DRP Implementation Using TUSB542 and TUSB322/TUSB321

7.2.3 Application Curves

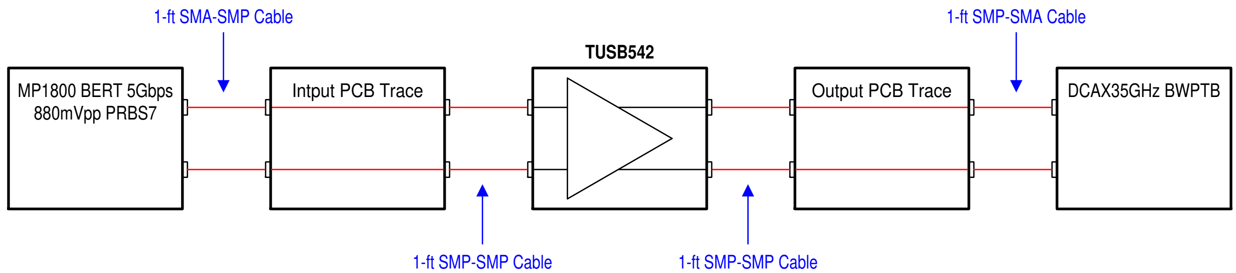


Figure 7-3. Measurement Setup

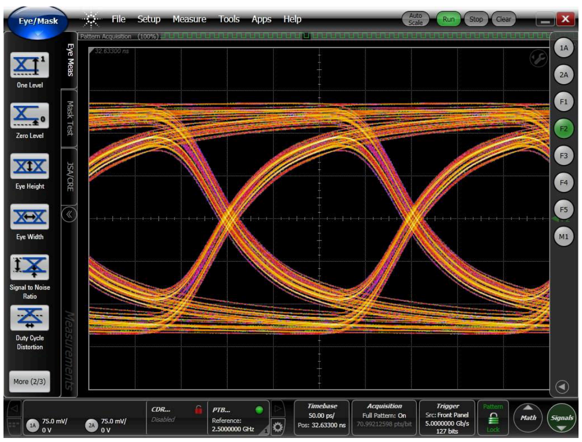


Figure 7-4. Input Signal: 12 Inch Input Trace (Eye Diagram at the Re-driver input)

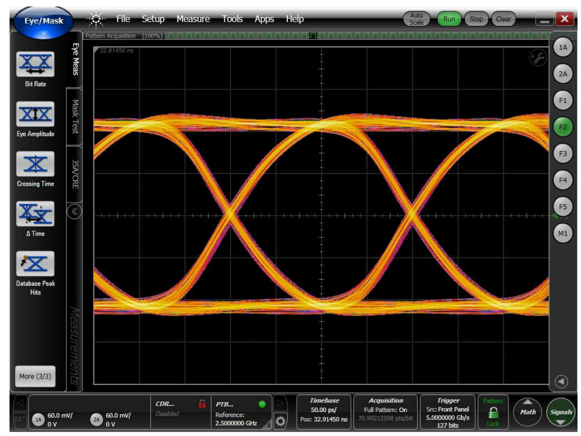


Figure 7-5. Output Signal: 12 Inch Output Trace (Eye Diagram at the DCAX)

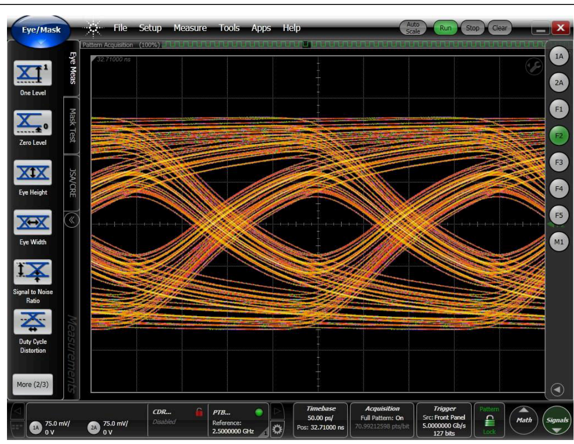


Figure 7-6. Input Signal: 24 Inch Input Trace (Eye Diagram at the Re-driver input)

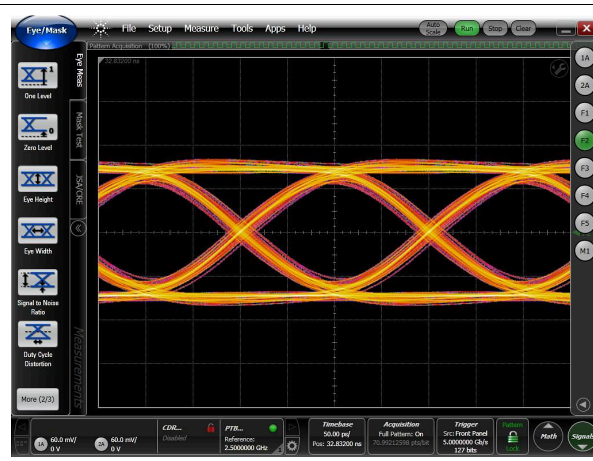


Figure 7-7. Output Signal: 24 Inch Output Trace (Eye Diagram at the DCAX)

7.3 Typical Application: Switching USB SS Host or Device Ports

TUSB542, being USB SS mux/demux, can be used for host or device switching. Figure 7-8 illustrates how the device can be used:

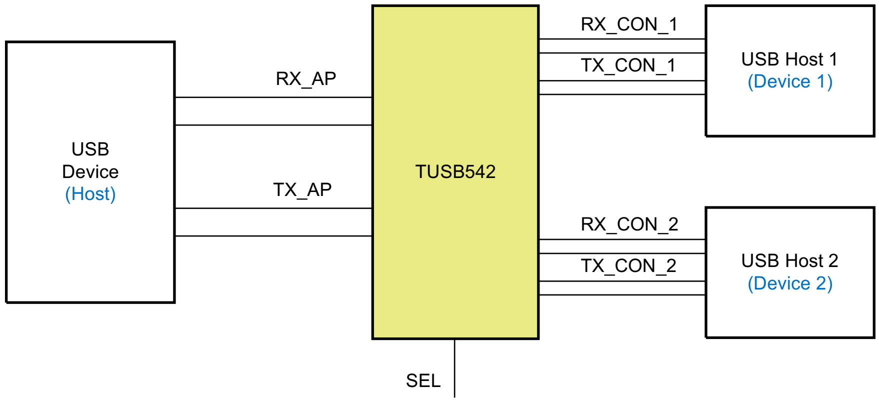


Figure 7-8. Muxing Two Host (Device) Port

7.3.1 Design Requirements

For this design example, use the design parameters shown in *Design Parameters*.

The configured value depends on the physical channel (PCB layout) Equalization 0, 3, 6, 9dB (5Gbps) The configured value depends on the physical channel (PCB layout) de-emphasis 0, –3.5, –6dB The configured value depends on the physical channel (PCB layout) Differential impedance 72 - 120 Ω

Table 7-2. Design Parameters

PARAMETER	VALUE	COMMENT
VDD18	1.8V	
AC Coupling Capacitors for SS signals	100 nF	75-200 nF range allowed. TUSB542 biases both input and output common mode voltage, hence ac-coupling caps as required on both sides. Note: TX pairs need to be biased at the connector.
Pull-up/down resistor to control CNF pins	4.7kΩ	
Input voltage range	100 mV to 1200 mV	
Output voltage range	900 mV to 1100 mV	

7.3.2 Detailed Design Procedure

Figure 7-2 shows an example implementation of an USB Type-C DRP port using TUSB542. Texas Instruments TUSB322 is shown here as channel configuration (CC) controller. Note: connections for CNFG pins of TUSB542 is an example only. The connection of the CNFG pins is application dependent; refer to the Table 6-2, where the user can find the available settings.

It is recommended to run an overall system signal integrity analysis, to estimate the channel loss and configure the re-driver. It is also recommended to have pull-up and pull-down option on the configuration pins for debug and testing purposes.

The signal integrity analysis must determine the following:

- Equalization (EQ) setting
- De-emphasis (DE) setting
- Output swing amplitude (OS) setting

The equalization must be set based on the insertion loss in the pre-channel (channel before the TUSB542 device). The input voltage to the device is able to have a large range because of the receiver sensitivity and the available EQ settings.

The de-emphasis setting must be set based on the length and characteristics of the post channel (channel after the TUSB542 device).

The output swing setting can also be configured based on the amplitude needed to pass the compliance test. This setting is also based on the length of interconnect or cable the TUSB542 is driving.

Refer to the Table 6-2 for a detailed description on how to configure the CONFIG_A1/A2 and CONFIG_B1/A2 terminals, to achieve the desired EQ, OS, and DE settings.

7.3.3 Application Curves

For this design example, use the application curves shown in *Section 7.2.3*.

7.4 Power Supply Recommendations

TUSB542 has internal power on reset circuit to provide clean reset for state machine provided supply ramp and level recommendations are met.

7.5 Layout

7.5.1 Layout Guidelines

- RXP/N and TXP/N pairs should be routed with controlled 90-Ω differential impedance (±15%).
- Keep away from other high speed signals.
- Intra-pair routing should be kept to within 2 mils.
- Length matching should be near the location of mismatch.
- Each pair should be separated at least by 3 times the signal trace width.
- The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
- Route all differential pairs on the same of layer.
- The number of VIAS should be kept to a minimum. It is recommended to keep the VIAS count to 2 or less.
- Keep traces on layers adjacent to ground plane.
- *Do not* route differential pairs over any plane split.
- Adding test points will cause impedance discontinuity, and therefore; negatively impacts signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

7.5.2 Layout Example

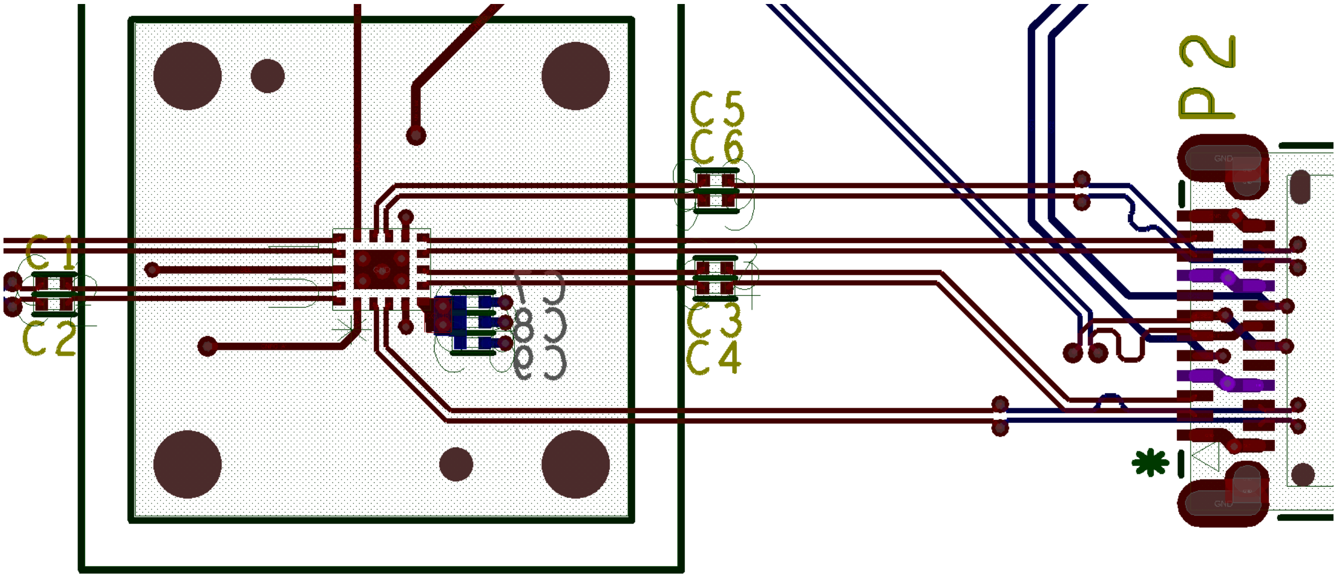


Figure 7-9. Example Layout

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

Type-C™ is a trademark of USB Implementers Forum, Inc..
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2017) to Revision F (December 2023) — **Page**

- Changed Junction temperature MIN value to –40 from -65 in the *Absolute Maximum Ratings* table... 4
- Changed Junction temperature MAX value to 105 from 150 in the *Absolute Maximum Ratings* table... 4
- Changed Storage temperature MAX value to 150 from 105 in the *Absolute Maximum Ratings* table... 4

Changes from Revision D (March 2017) to Revision E (April 2017) — **Page**

- Changed *Feature* From: Selectable Equalization, de-emphasis, and Output Swing To: Selectable Equalization up to 9dB, de-emphasis, and Output Swing up to 6dB ... 1
- Deleted *Feature*: Automatic LFPS de-emphasis Control for USB 3.1 Compliance... 1
- Changed *Feature* From: Can Support USB DFP, UFP or DRP Port To: Supports USB-C DFP, UFP or DRP Port... 1
- Changed Application From: USB Type-C SS Application To: USB 3.1 Gen 1 SS Application... 1
- Changed the *Simplified Schematic* ... 1
- Changed the first five paragraphs of the *Overview* section... 11
- Changed Figure 7-1 ... 14
- Changed the *Design Requirements* and the *Detailed Design Procedure* section of *Typical Applications, USB Type-C Port SS MUX* section... 15
- Changed the *Design Requirements* and the *Detailed Design Procedure* section of *Typical Application: Switching USB SS Host or Device Ports* ... 18

Changes from Revision C (August 2016) to Revision D (March 2017) — **Page**

- Added a MIN value of –65 to the Storage temperature in the *Absolute Maximum Ratings* table... 4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB542RWQR	Active	Production	X2QFN (RWQ) | 18	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54
TUSB542RWQR.A	Active	Production	X2QFN (RWQ) | 18	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54
TUSB542RWQRG4	Active	Production	X2QFN (RWQ) | 18	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54
TUSB542RWQRG4.A	Active	Production	X2QFN (RWQ) | 18	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

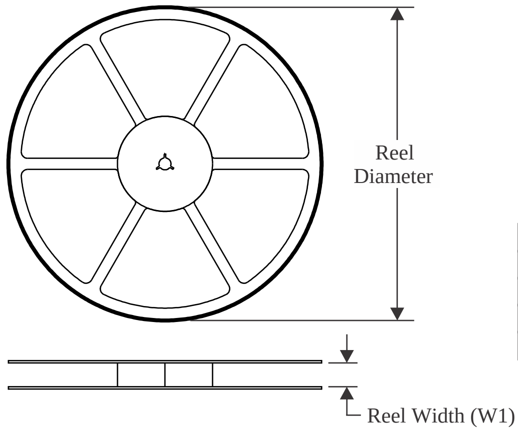
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

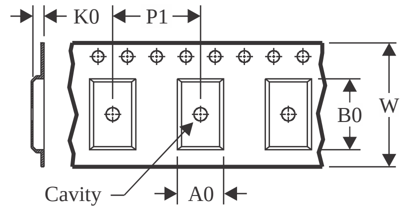
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

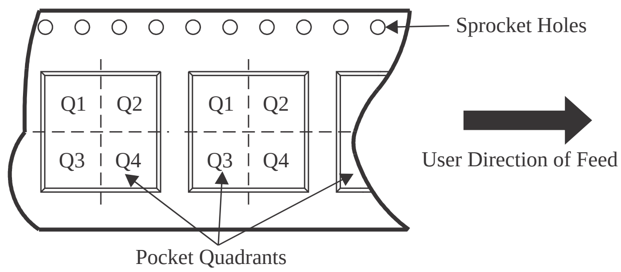


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

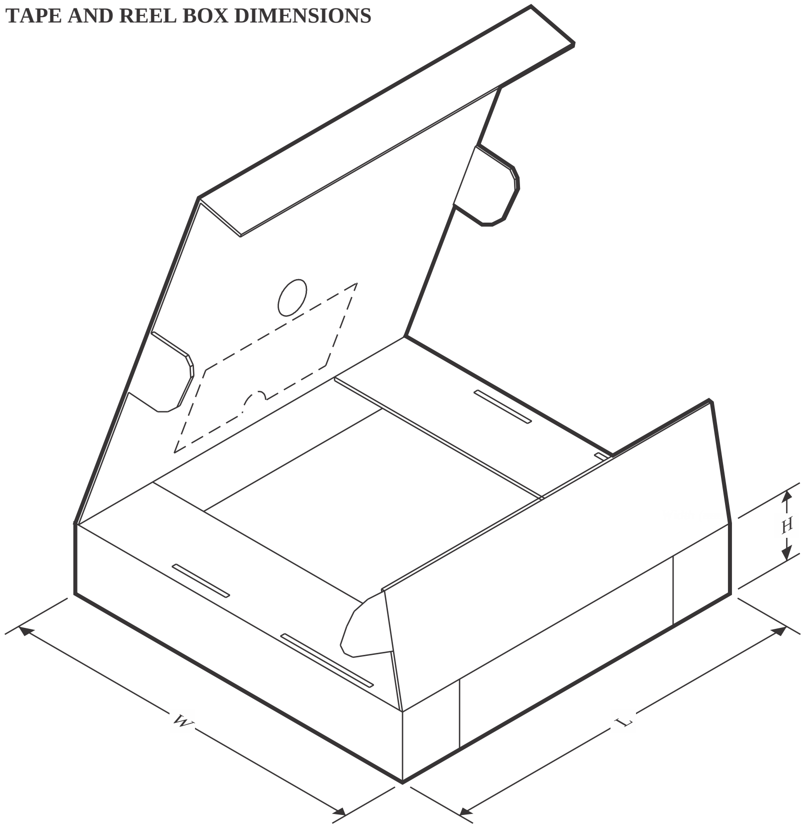
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

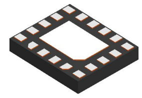
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB542RWQR	X2QFN	RWQ	18	3000	179.0	8.4	2.25	2.65	0.53	4.0	8.0	Q1
TUSB542RWQRG4	X2QFN	RWQ	18	3000	179.0	8.4	2.25	2.65	0.53	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

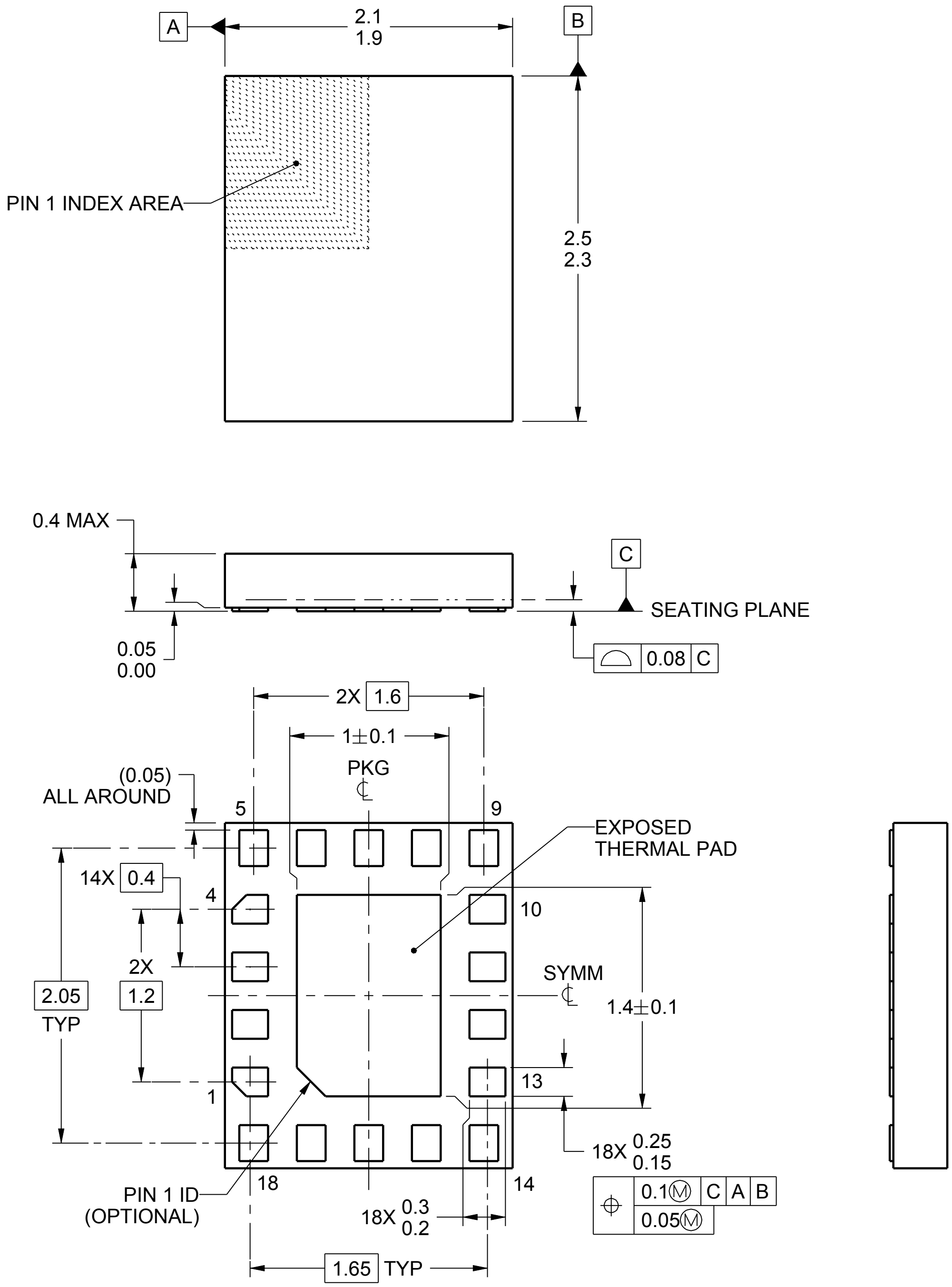
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB542RWQR	X2QFN	RWQ	18	3000	213.0	191.0	35.0
TUSB542RWQRG4	X2QFN	RWQ	18	3000	213.0	191.0	35.0



PACKAGE OUTLINE

X2QFN - 0.4 mm max height

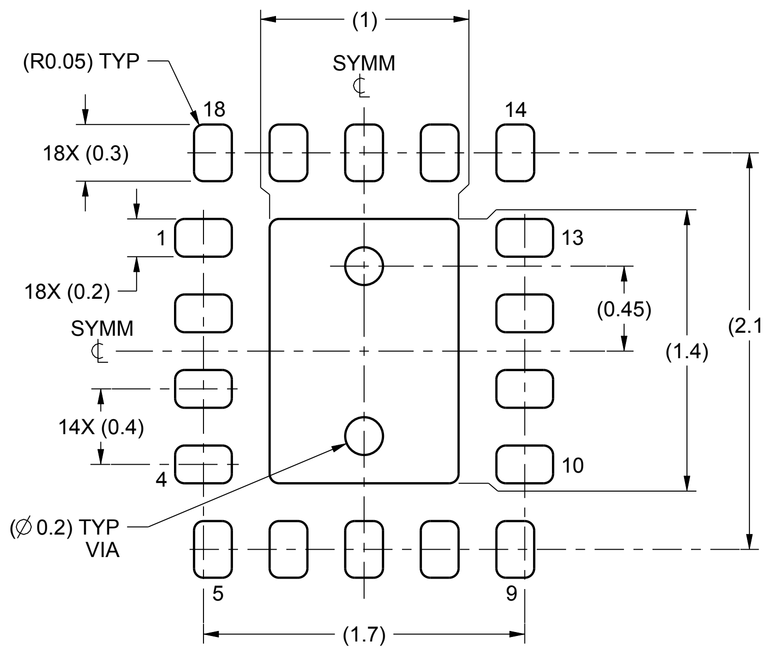
PLASTIC QUAD FLATPACK - NO LEAD



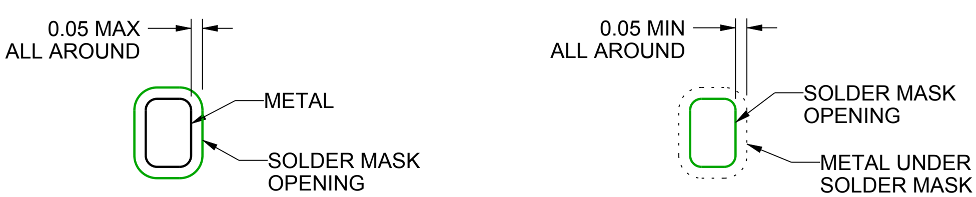
4221962/B 06/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



NON SOLDER MASK DEFINED (PREFERRED)

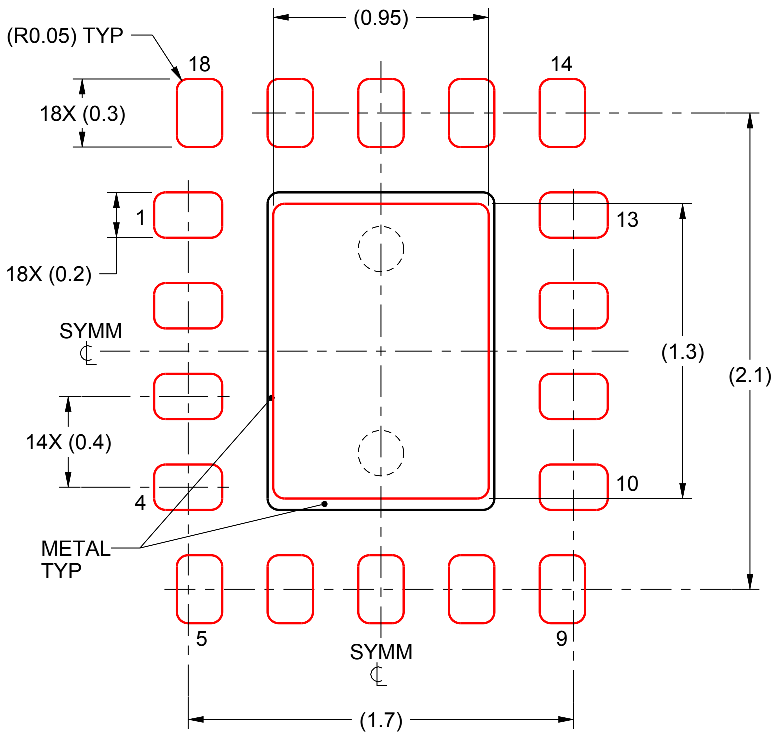
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221962/B 06/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

4221962/B 06/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.