TUSB8020B-Q1 Automotive Two-Port USB 3.0 Hub

1 Features

- Two Port USB 3.0 Compliant Hub
- USB 2.0 Hub Features
  - Multi Transaction Translator (MTT) Hub: Two Transaction Translators
  - Four Asynchronous Endpoint Buffers Per Transaction Translator
- Supports USB Battery Charging Specification Revision 1.2
  - CDP Mode (Upstream Port Connected)
  - DCP Mode (Upstream Port Unconnected)
  - DCP Mode Complies with Chinese Telecommunications Industry Standard YD/T 1591-2009
- Support D+/D- Divider Mode.
- Supports Operation as a USB 3.0 or USB 2.0 Compound Device
- Per Port or Ganged Power Switching and Over-Current Notification Inputs
- OTP ROM, Serial EEPROM or I^2C/SMBus Slave Interface for Custom Configurations:
  - VID and PID
  - Port Customizations
  - Manufacturer and Product Strings (not by OTP ROM)
  - Serial Number (not by OTP ROM)
- Application Feature Selection Using Terminal Selection or EEPROM/ or I^2C/SMBus Slave Interface
- Provides 128-Bit Universally Unique Identifier (UUID)
- Supports On-Board and In-System OTP/EEPROM Programming Via the USB 2.0 Upstream Port
- Single Clock Input, 24-MHz Crystal or Oscillator
- No special driver requirements; works seamlessly on any operating system with USB stack support

2 Applications

- Automotive
- Computer Systems
- Docking Stations
- Monitors
- Set-Top Boxes

3 Description

The TUSB8020B-Q1 is a two-port USB 3.0 compliant hub. It provides simultaneous SuperSpeed USB and high-speed/full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that only supports high-speed or full-speed/low-speed connections, SuperSpeed USB connectivity is disabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed/low-speed connections, SuperSpeed USB and high-speed connectivity are disabled on the downstream ports.

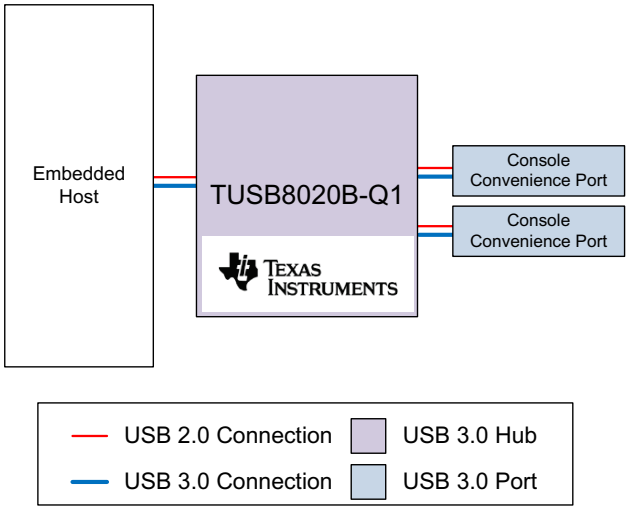
The TUSB8020B-Q1 supports per port or ganged power switching and over-current protection, and supports battery charging applications.

An individually port power controlled hub switches power on or off to each downstream port as requested by the USB host. Also when an individually port power controlled hub senses an over-current event, only power to the affected downstream port will be switched off.

A ganged hub switches on power to all its downstream ports when power is required to be on for any port. The power to the downstream ports is not switched off unless all ports are in a state that allows power to be removed. Also when a ganged hub senses an over-current event, power to all downstream ports will be switched off.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
TUSB8020BIPHPRQ1	HTQFP (48)	7mm × 7mm
TUSB8020BIPHPQ1		



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4 Revision History

Date	Revision	Notes
March 2014	*	Initial release.

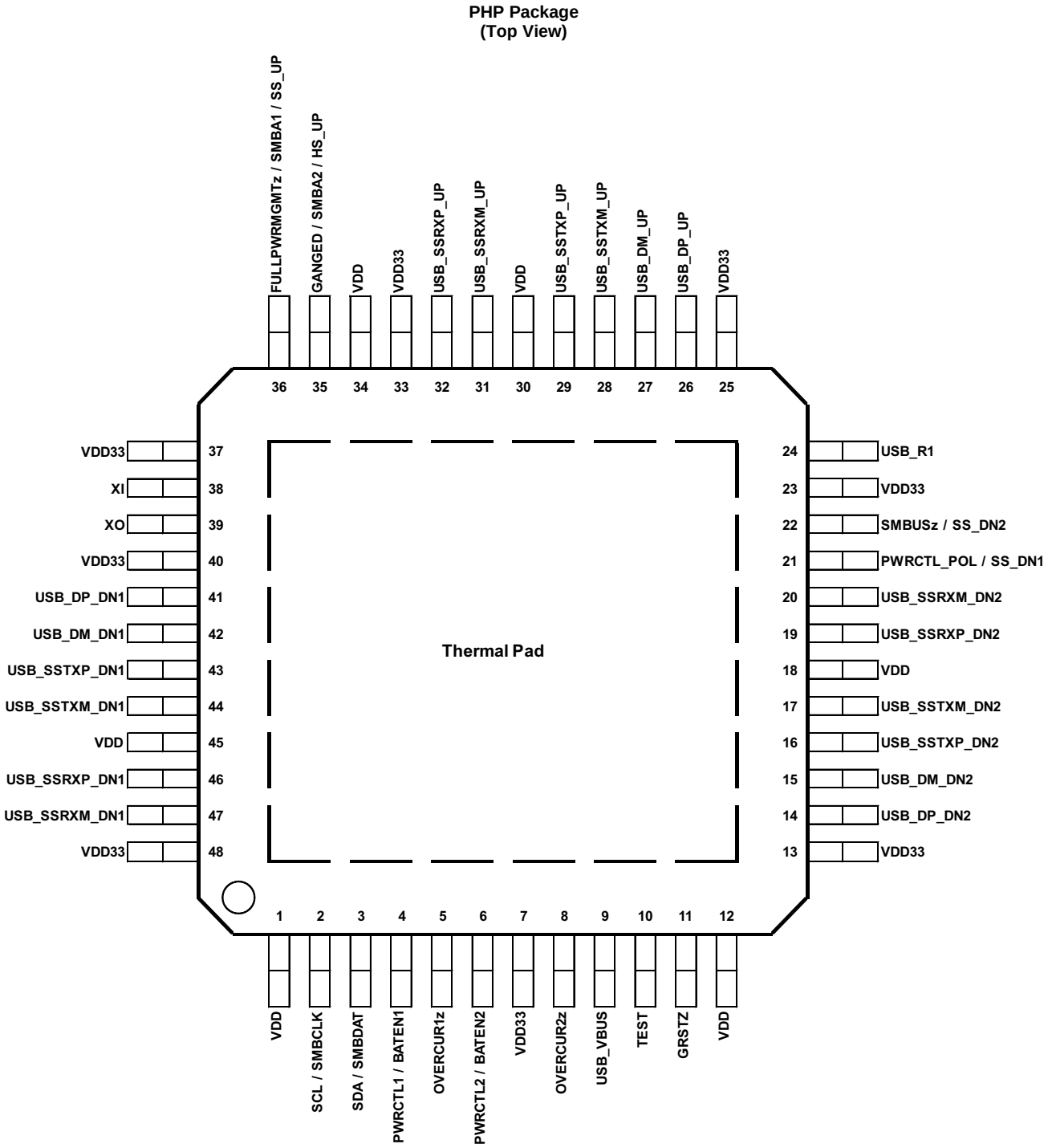
5 Description (Continued)

The TUSB8020B-Q1 downstream ports provide support for battery charging applications by providing USB Battery Charging 1.2 Charging Downstream Port (CDP) handshaking support. It also supports a Dedicated Charging Port (DCP) mode when the upstream port is not connected. The DCP mode supports the USB Battery Charging Specification and the Chinese Telecommunications Industry Standard YD/T 1591-2009. In addition, an automatic mode provides transparent support for BC 1.2 compliant devices and devices supporting Divider Mode charging solutions when the upstream port unconnected.

The TUSB8020B-Q1 provides terminal strap configuration for some features including battery charging support, and also provides customization though OTP ROM, I^2C EEPROM or via an I^2C/SMBus slave interface for PID, VID, and custom port and phy configurations. Custom string support is also available when using an I^2C EEPROM or the I^2C/SMBus slave interface.

The device is available in a 48-terminal HTQFP package and is designed for operation over the industrial temperature range of -40°C to 85°C.

6 Terminal Configuration and Functions



Terminal Functions

TERMINAL		TYPE(1)	DESCRIPTION
NAME	TERMINAL NO.		
Clock and Reset Signals			
GRSTz	11	I PU	Global power reset. This reset brings all of the TUSB8020B-Q1 internal registers to their default states. When GRSTz is asserted, the device is completely nonfunctional.
XI	38	I	Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
XO	39	O	Crystal output. This terminal is the crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
USB Upstream Signals			
USB_SSTXP_UP	29	O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_UP	28	O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_UP	32	I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_UP	31	I	USB SuperSpeed receiver differential pair (negative)
USB_DP_UP	26	I/O	USB High-speed differential transceiver (positive)
USB_DM_UP	27	I/O	USB High-speed differential transceiver (negative)
USB_R1	24	I	Precision resistor reference. A 9.53-kΩ ±1% resistor should be connected between USB_R1 and GND.
USB_VBUS	9	I	USB upstream port power monitor. The VBUS detection requires a voltage divider. The signal USB_VBUS must be connected to VBUS through a 90.9-KΩ ±1% resistor, and to ground through a 10-kΩ ±1% resistor from the signal to ground.
USB Downstream Signals			
USB_SSTXP_DN1	43	O	USB SuperSpeed transmitter differential pair (positive) Downstream Port 1.
USB_SSTXM_DN1	44	O	USB SuperSpeed transmitter differential pair (negative) Downstream Port 1.
USB_SSRXP_DN1	46	I	USB SuperSpeed receiver differential pair (positive) Downstream Port 1.
USB_SSRXM_DN1	47	I	USB SuperSpeed receiver differential pair (negative) Downstream Port 1.
USB_DP_DN1	41	I/O	USB High-speed differential transceiver (positive) Downstream Port 1.
USB_DM_DN1	42	I/O	USB High-speed differential transceiver (negative) Downstream Port 1.
PWRCTL1/BATEN1	4	I/O, PD	USB Port 1 Power On Control for Downstream Power/Battery Charging Enable. The terminal is used for control of the downstream power switch for Port 1. In addition, the value of the terminal is sampled at the de-assertion of reset to determine the value of the battery charging support for Port 1 as indicated in the Battery Charging Support register. 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR1z	5	I, PU	USB DS Port 1 Over-Current Detection input. This terminal is used to connect the over current output of the downstream port power switch for Port 1. 0 = An over current event has occurred 1 = An over current event has not occurred If power management is enabled, the external circuitry needed should be determined by the power switch. In ganged mode either OVERCUR1z or OVERCUR2z can be used. In ganged mode the overcurrent will be reported as a hub event instead of a port event.
USB_SSTXP_DN2	16	O	USB SuperSpeed transmitter differential pair (positive) Downstream Port 2.
USB_SSTXM_DN2	17	O	USB SuperSpeed transmitter differential pair (negative) Downstream Port 2.
USB_SSRXP_DN2	19	I	USB SuperSpeed receiver differential pair (positive) Downstream Port 2.
USB_SSRXM_DN2	20	I	USB SuperSpeed receiver differential pair (negative) Downstream Port 2.
USB_DP_DN2	14	I/O	USB High-speed differential transceiver (positive) Downstream Port 2.
USB_DM_DN2	15	I/O	USB High-speed differential transceiver (negative) Downstream Port 2.
PWRCTL2/BATEN2	6	I/O, PD	Power On Control /Battery Charging Enable for Downstream Port 2. This terminal is used for control of the downstream power switch for Port 2. In addition, the value of the terminal is sampled at the de-assertion of reset to determine the value of the battery charging support for Port 2 as indicated in the Battery Charging Support register. 0 = Battery charging not supported 1 = Battery charging supported

(1) I = input, O = output, I/O = input/output, PU = internal pullup resistor, PD = internal pulldown resistor, and PWR = power signal

Terminal Functions (continued)

TERMINAL		TYPE[1]	DESCRIPTION
NAME	TERMINAL NO.		
OVERCUR2z	8	I, PU	Over-Current Detection for Downstream Port 2. This terminal is used to connect the over current output of the downstream port power switch for Port 2. 0 = An over current event has occurred 1 = An over current event has not occurred If power management is enabled, the external circuitry needed should be determined by the power switch. In ganged mode either OVERCUR1z or OVERCUR2z can be used. In ganged mode the overcurrent will be reported as a hub event instead of a port event.
I²C/SMBUS Signals			
SCL/SMBCLK	2	I/O, PD	I²C clock/SMBus clock. Function of terminal depends on the setting of the SMBUSz input. When SMBUSz = 1, this terminal acts as the serial clock interface for an I²C EEPROM. When SMBUSz = 0, this terminal acts as the serial clock interface for an SMBus host. This pin must be pulled up to use the OTP ROM. Can be left unconnected if external interface not implemented.
SDA/SMBDAT	3	I/O, PD	I²C data/SMBus data. Function of terminal depends on the setting of the SMBUSz input. When SMBUSz = 1, this terminal acts as the serial data interface for an I²C EEPROM. When SMBUSz = 0, this terminal acts as the serial data interface for an SMBus host. This pin must be pulled up to use the OTP ROM. Can be left unconnected if external interface not implemented.
Test and Miscellaneous Signals			
SMBUSz/SS_DN2	22	I, PU	SMBUS mode / SuperSpeed USB Status for Downstream Port 2 The value of the terminal is sampled at the de-assertion of reset to enable I²C or SMBus mode. 0 = SMBus Mode Selected 1 = I²C mode selected After reset, this signal indicates the SuperSpeed USB connection status of downstream port 2. A value of 1 indicates the connection is SuperSpeed USB.
PWRCTL_POL/SS_DN1	21	I/O, PD	Power Control Polarity / SuperSpeed USB Status for Downstream Port 1. The value of the terminal is sampled at the de-assertion of reset to set the polarity of PWRCTL[2:1]. 0 = PWRCTL polarity is active high. 1 = PWRCTL polarity is active loiw. After reset, this signal indicates the SuperSpeed USB connection status of downstream port 1. A value of 1 indicates the connection is SuperSpeed USB.
GANGED/SMBA2/ HS_UP	35	I, PU	Ganged operation enable/SMBus Address bit 2/ High-Speed Status for Upstream Port The value of the terminal is sampled at the de-assertion of reset to set the power switch and over current detection mode as follows: 0 = Individual power control supported when power switching is enabled. 1 = Power control gangs supported when power switching is enabled. When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 2. SMBus slave address bits 2 and 3 are always 1 for the TUSB8020B-Q1. After reset, this signal indicates the High-speed USB connection status of the upstream port. A value of 1 indicates the upstream port is connected to a High-speed USB capable port.
FULLPWRMGMTz/ SMBA1/SS_UP	36	I, PU	Full power management enable/ SMBus Address bit 1/ Super-Speed USB Status for Upstream port The value of the terminal is sampled at the de-assertion of reset to set the power switch control follows: 0 = Power switching supported 1 = Power switching not supported Full power management is the ability to control power to the downstream ports of the TUSB8020B-Q1 using PWRCTL[2:1]/BATEN[2:1]. When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 1. SMBus slave address bit 3 is always 1 for the TUSB8020B-Q1. Can be left unconnected if full power management and SMBus are not implemented. After reset, this signal indicates the SuperSpeed USB connection status of the upstream port. A value of 1 indicates the upstream port is connected to a SuperSpeed USB capable port.
TEST	10	I, PD	TEST mode enable. When this terminal is asserted high at reset enables test mode. This terminal is reserved for factory use. It is recommended to pull-down this terminal to ground.

Terminal Functions (continued)

TERMINAL		TYPE(1)	DESCRIPTION
NAME	TERMINAL NO.		
Power and Ground Signals			
VDD	1, 12, 18, 30, 34, 45	PWR	1.1-V power rail
VDD33	7, 13, 23, 25, 33, 37, 40, 48	PWR	3.3-V power rail
GND	PAD	-	Ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
VDD	Steady-state supply voltage	–0.3 to 1.4	V
VDD33	Steady-state supply voltage	–0.3 to 3.8	V

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–65	150	°C
V_{ESD}	Human-Body Model (HBM) AEC-Q100 Classification Level H2		2000	V
	Charged-Device Model (CDM) AEQ-Q100 Classification Level C4B for corner pins		750	
	Charged-Device Model (CDM) AEQ-Q100 Classification Level C4B for non-corner pins		500	

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD(1)	1.1 supply voltage	0.99	1.1	1.26	V
VDD33	3.3 supply voltage	3	3.3	3.6	V
USB_VBUS	Voltage at USB_VBUS PAD	0		1.155	V
T_A	Operating free-air temperature range	-40	25	85	°C
T_J	Operating junction temperature range	-40	25	105	°C

(1) A 1.05-V, 1.1-V, or 1.2-V supply may be used as long as minimum and maximum supply conditions are met.

7.4 Thermal Information

THERMAL METRIC(1)		TUSB8020B-Q1 PHP 48 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	31.8	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance(3)	16.1	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	13	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	12.9	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance(7)	0.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 3.3-V I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage(1)	VDD33		2	VDD33	V
V_{IL}	Low-level input voltage(1)	VDD33		0	0.8	V
V_I	Input voltage			0	VDD33	V
V_O	Output voltage(2)			0	VDD33	V
t_t	Input transition time (t_{rise} and t_{fall})			0	25	ns
V_{hys}	Input hysteresis(3)				0.13 x VDD33	V
V_{OH}	High-level output voltage	VDD33	I_{OH} = -4 mA	2.4		V
V_{OL}	Low-level output voltage	VDD33	I_{OL} = 4 mA		0.4	V
I_{OZ}	High-impedance, output current(2)	VDD33	V_I = 0 to VDD33		±20	µA
I_{OZP}	High-impedance, output current with internal pullup or pulldown resistor(4)	VDD33	V_I = 0 to VDD33		±225	µA
I_I	Input current(5)	VDD33	V_I = 0 to VDD33		±15	µA

(1) Applies to external inputs and bidirectional buffers.
(2) Applies to external outputs and bidirectional buffers.
(3) Applies to GRSTz.
(4) Applies to pins with internal pullups/pulldowns.
(5) Applies to external input buffers.

7.6 Power-Up Timing Requirements

		MIN	TYP	MAX	UNIT
Td1	V_{DD33} stable before V_{DD} stable. There is no timing relationship between V_{DD33} and V_{DD}	0			ms
Td2	V_{DD} and V_{DD33} stable before de-assertion of GRSTZ.	3			ms
Tsu_io	Setup for MISC inputs sampled at the de-assertion of GRSTZ(1)	0.1			µs
Thd_io	Hold for MISC inputs sampled at the de-assertion of GRSTZ.(1)	0.1			µs
T_{VDD33_RAMP}	V_{DD33} supply ramp requirements	0.2		100	ms
T_{VDD_RAMP}	V_{DD} supply ramp requirements	0.2		100	ms

(1) Misc pins sampled at de-assertion of GRSTZ: FULLPWRMGMTz, GANGED, PWRCTL_POL, SMBUSz, BATEN1, and BATEN2

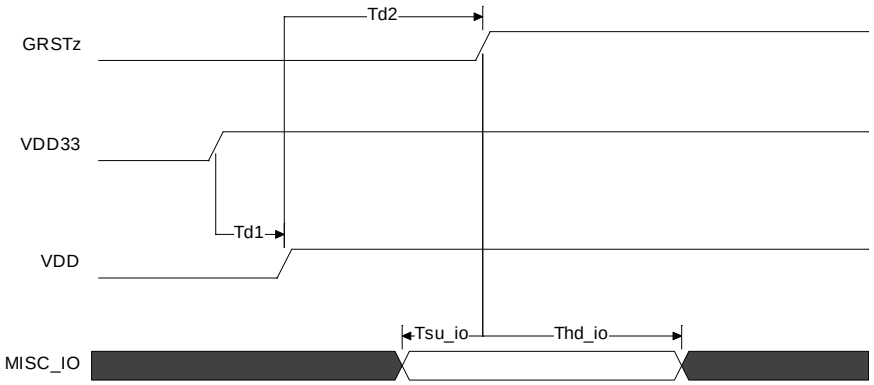


Figure 1. Power-Up Timing Requirements

7.7 Hub Input Supply Current

Typical values measured at T_A = 25°C

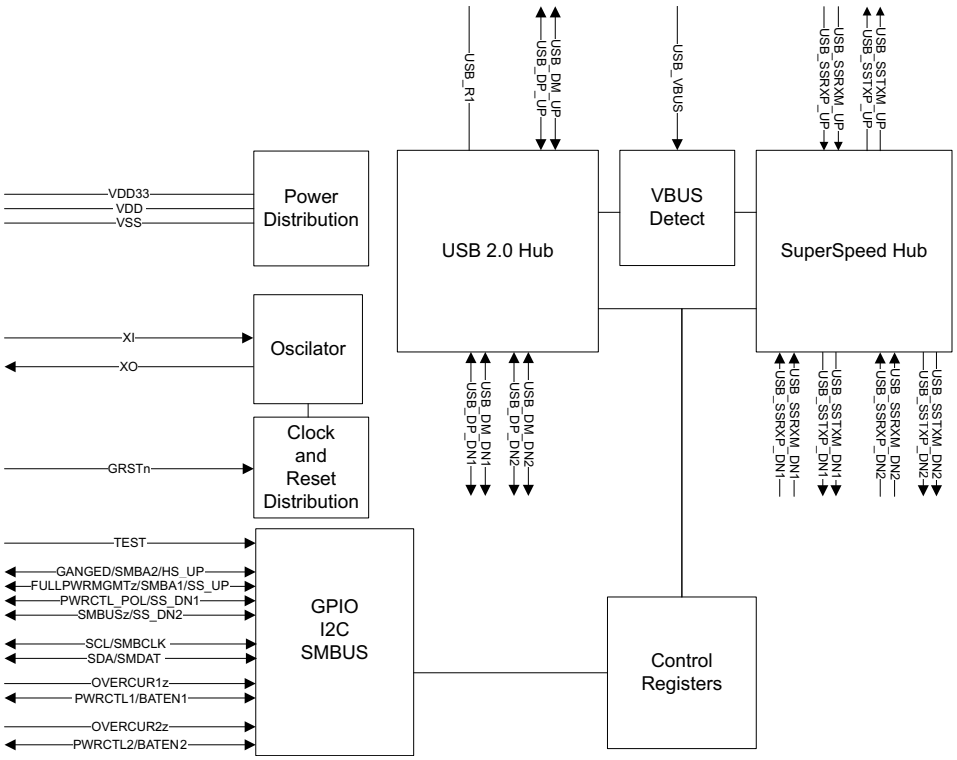
PARAMETER	VDD33	VDD11	UNIT
	3.3 V	1.1 V	
LOW POWER MODES			
Power On (after Reset)	5	39	mA
Disconnect from Host	5	39	mA
Suspend (USB2 Host)	5	39	mA
Suspend (USB3 Host)	6	40	mA
ACTIVE MODES (US state / DS State)			
3.0 host / 1 SS Device and Hub in U1	50	218	mA
3.0 host / 1 SS Device and Hub in U0	50	342	mA
3.0 host / 2 SS Devices and Hub in U1	50	284	mA
3.0 host / 2 SS Devices and Hub in U0	50	456	mA
3.0 host / 1 SS and 1 HS Device in U1	92	242	mA
3.0 host / 1 SS and 1 HS Device in U0	93	364	mA
2.0 host / 1 HS Device active	48	71	mA
2.0 host / 2 HS Devices active	60	80	mA

8 Detailed Description

8.1 Overview

The TUSB8020B-Q1 is a two-port USB 3.0 compliant hub. It provides simultaneous SuperSpeed USB and high-speed/full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that only supports high-speed or full-speed/low-speed connections, SuperSpeed USB connectivity is disabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed/low-speed connections, SuperSpeed USB and high-speed connectivity are disabled on the downstream ports.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Battery Charging Features

The TUSB8020B-Q1 provides support for USB Battery Charging Specification Revision 1.2 (BC 1.2). Battery charging support may be enabled on a per port basis through the REG_6h(batEn[1:0]).

Battery charging support includes both Charging Downstream Port (CDP) and Dedicated Charging Port (DCP) modes. The DCP mode is compliant with the Chinese Telecommunications Industry Standard YD/T 1591-2009.

In addition, to standard BC 1.2 DCP mode, the TUSB8020B-Q1 provides a mode (AUTOMODE) which automatically provides support for BC 1.2 DCP devices and devices that support custom charging indication. AUTOMODE is enabled by default. When in AUTOMODE, the port will automatically switch between a divider mode and the DCP mode depending on the portable device connected. The divided mode places a fixed DC voltage on the ports DP and DM signals which allows some devices to identify the capabilities of the charger. The default divider mode indicates support for up to 5W. The divider mode can be configured to report a high-current setting (up to 10 W) through REG_Ah(HiCurAcpModeEn).

The battery charging mode for each port is dependent on the state of Reg_6h(batEn[n]), the status of the VBUS input, and the state of REG_Ah(autoModeEnz) upstream port as identified in Table 1. Battery charging can also be enabled through the PWRCTL1/BATEN1 and PWRCTL2/BATEN2 pins.

Feature Description (continued)

Table 1. TUSB8020B-Q1 Battery Charging Modes

batEn[n]	VBUS	autoModeEnz	BC Mode Port x (x = n + 1)
0	Don't Care	Don't Care	Don't Care
1	< 4 V	0	Automode(1) (2)
		1	DCP(3) (4)
	> 4 V	Don't Care	CDP(3)

(1) Auto-mode automatically selects divider-mode or DCP mode (BC 1.2 and YD/T 1591-2009).
(2) Divider mode can be configured for high-current mode through register or OTP settings.
(3) USB Battery Charging Specification Revision 1.2 Compliant
(4) Chinese Telecommunications Industry Standard YD/T 1591-2009

8.3.2 USB Power Management

The TUSB8020B-Q1 can be configured for power switched applications using either per-port or ganged power-enable controls and over-current status inputs.

Power switch support is enabled by REG_5h(fullPwrMgmtz) and the per-port or ganged mode is configured by REG_5h(ganged). It can also be enabled through the FULLPWRMGMTz pin. Also ganged or individual control can be controlled by the GANGED pin.

The TUSB8020B-Q1 supports both active high and active low power-enable controls. The PWRCTL[2:1] polarity is configured by REG_Ah(pwrctlPol). The polarity can also be configured by the PWRCTL_POL pin.

8.3.3 One Time Programmable (OTP) Configuration

The TUSB8020B-Q1 allows device configuration through one time programmable non-volatile memory (OTP). The programming of the OTP is supported using vendor-defined USB device requests. For details using the OTP features please contact your TI representative.

Table 2 provides a list features which may be configured using the OTP. The Bit Field section in table shows which features can be controlled by OTP ROM. The bits not listed in the table are not accessible by the OTP ROM.

Table 2. OTP Configurable Features

CONFIGURATION REGISTER OFFSET	BIT FIELD	DESCRIPTION
REG_01h	[7:0]	Vendor ID LSB
REG_02h	[7:0]	Vendor ID MSB
REG_03h	[7:0]	Product ID LSB
REG_04h	[7:0]	Product ID MSB
REG_07h	[0]	Port removable configuration for downstream ports 1. OTP configuration is inverse of rmbl[1:0], i.e. 1 = not removable, 0 = removable.
REG_07h	[1]	Port removable configuration for downstream ports 2. OTP configuration is inverse of rmbl[1:0], i.e. 1 = not removable, 0 = removable.
REG_0Ah	[1]	Automode enable
REG_0Ah	[4]	High-current divider mode enable.
REG_F2h	[3:1]	USB power switch power-on delay.

8.3.4 Clock Generation

The TUSB8020B-Q1 accepts a crystal input to drive an internal oscillator or an external clock source. If a crystal is used, a 1-MΩ shunt resistor is required. It is also important to keep the XI and XO traces as short as possible and away from any switching leads to minimize noise coupling.

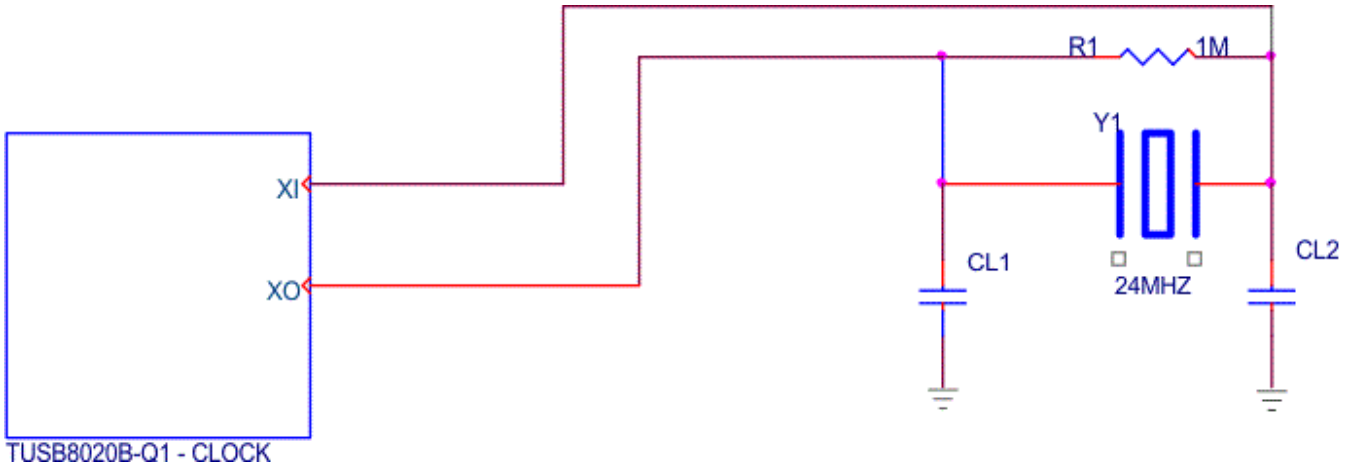


Figure 2. TUSB8020B-Q1 Clock

8.3.4.1 Crystal Requirements

The crystal must be fundamental mode with load capacitance of 12 pF - 24 pF and frequency stability rating of ±100 PPM or better. To ensure proper startup oscillation condition, a maximum crystal equivalent series resistance (ESR) of 50 Ω is recommended. A parallel load capacitor should be used if a crystal source is used. The exact load capacitance value used depends on the crystal vendor. Refer to application note *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* (SLLA122) for details on how to determine the load capacitance value.

8.3.4.2 Input Clock Requirements

When using an external clock source such as an oscillator, the reference clock should have a ±100 PPM or better frequency stability and have less than 50-ps absolute peak to peak jitter or less than 25-ps peak to peak jitter after applying the USB 3.0 jitter transfer function. XI should be tied to the 1.8-V clock source and XO should be left floating.

8.3.5 Power Up and Reset

The TUSB8020B-Q1 does not have specific power sequencing requirements with respect to the VDD or VDD33 power rails. The VDD or VDD33 power rails may be powered up for an indefinite period of time while the other is not powered up if all of these constraints are met:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered up must be limited to 100 hours over the projected life-time of the device.
- Bus contention while VDD33 is powered down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 3 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the de-assertion of GRSTz. This can be generated using programmable-delay supervisory device or using an RC circuit.

8.4 Device Functional Modes

8.4.1 External Configuration Interface

The TUSB8020B-Q1 supports a serial interface for configuration register access. The device may be configured by an attached I^2C EEPROM or accessed as a slave by an SMBus capable host controller. The external interface is enabled when both the SCL/SMBCLK and SDA/SMBDAT terminals are pulled up to 3.3 V at the de-assertion of reset. The mode, I^2C master or SMBus slave, is determined by the state of SMBUSz/SS_DN2 terminal at reset.

8.4.2 I^2C EEPROM Operation

The TUSB8020B-Q1 supports a single-master, standard mode (100 kbit/s) connection to a dedicated I^2C EEPROM when the I^2C interface mode is enabled. In I^2C mode, the TUSB8020B-Q1 reads the contents of the EEPROM at bus address 1010000b using 7-bit addressing starting at address 0.

If the value of the EEPROM contents at byte 00h equals 55h, the TUSB8020B-Q1 loads the configuration registers according to the EEPROM map. If the first byte is not 55h, the TUSB8020B-Q1 exits the I^2C mode and continues execution with the default values in the configuration registers. The hub will not connect on the upstream port until the configuration is completed. If the TUSB8020B-Q1 detected an un-programmed EEPROM (value other than 55h), it will enter Programming Mode and a Programming Endpoint within the hub will be enabled.

Note, the bytes located above offset Ah are optional. The requirement for data in those addresses is dependent on the options configured in the Device Configuration, Phy Custom Configuration, and Device Configuration 2 registers.

For details on I^2C operation refer to the UM10204 I^2C-bus Specification and User Manual.

8.4.3 SMBus Slave Operation

When the SMBus interface mode is enabled, the TUSB8020B-Q1 supports read block and write block protocols as a slave-only SMBus device.

The TUSB8020B-Q1 slave address is 1000 1xyz, where:

- x is the state of GANGED/SMBA2/HS_UP terminal at reset,
- y is the state of FULLPWRMGMTz/SMBA1/SS_UP terminal at reset, and
- z is the read/write bit; 1 = read access, 0 = write access.

If the TUSB8020B-Q1 is addressed by a host using an unsupported protocol it will not respond. The TUSB8020B-Q1 will wait indefinitely for configuration by the SMBus host and will not connect on the upstream port until the SMBus host indicates configuration is complete by clearing the CFG_ACTIVE bit.

For details on SMBus requirements refer to the System Management Bus Specification.

8.5 Register Maps

8.5.1 Configuration Registers

The internal configuration registers are accessed on byte boundaries. The configuration register values are loaded with defaults but can be over-written when the TUSB8020B-Q1 is in I^2C or SMBus mode.

Table 3. TUSB8020B-Q1 Register Map

BYTE ADDRESS	CONTENTS	EEPROM CONFIGURABLE
00h	ROM Signature Register	No
01h	Vendor ID LSB	Yes
02h	Vendor ID MSB	Yes
03h	Product ID LSB	Yes
04h	Product ID MSB	Yes
05h	Device Configuration Register	Yes
06h	Battery Charging Support Register	Yes
07h	Device Removable Configuration Register	Yes
08h	Port Used Configuration Register	Yes
09h	Reserved	Yes, program to 00h
0Ah	Device Configuration Register 2	Yes
0Bh-0Fh	Reserved	
10h-1Fh	UUID Byte [15:0]	No
20h-21h	LangID Byte [1:0]	Yes, if customStrings is set
22h	Serial Number String Length	Yes, if customSerNum is set
23h	Manufacturer String Length	Yes, if customStrings is set
24h	Product String Length	Yes, if customStrings is set
25h-2Fh	Reserved	Yes
30h-4Fh	Serial Number String Byte [31:0]	Yes, if customSerNum is set
50h-8Fh	Manufacturer String Byte [63:0]	Yes, if customStrings is set
90h-CFh	Product String Byte [63:0]	Yes, if customStrings is set
D0-DFh	Reserved	No
F0h	Additional Feature Configuration Register	Yes
F1h	Reserved	No
F2h	Charging Port Control Register	Yes
F3-F7h	Reserved	No
F8h	Device Status and Command Register	No
F9-FFh	Reserved	No

8.5.1.1 ROM Signature Register

Table 4. Register Offset 0h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 5. Bit Descriptions – ROM Signature Register

Bit	Field Name	Access	Description
7:0	romSignature	RW	ROM Signature Register. This register is used by the TUSB8020B-Q1 in I^2C mode to validate the attached EEPROM has been programmed. The first byte of the EEPROM is compared to the mask 55h and if not a match, the TUSB8020B-Q1 aborts the EEPROM load and executes with the register defaults.

8.5.1.2 Vendor ID LSB Register

Table 6. Register Offset 1h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	1	0	1	0	0	0	1

Table 7. Bit Descriptions – Vendor ID LSB Register

Bit	Field Name	Access	Description
7:0	vendorIdLsb	RO/RW	Vendor ID LSB. Least significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 51h representing the LSB of the TI Vendor ID 0451h. The value may be over-written to indicate a customer Vendor ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero the value when reading this register shall reflect the OTP ROM value.

8.5.1.3 Vendor ID MSB Register

Table 8. Register Offset 2h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	0	0

Table 9. Bit Descriptions – Vendor ID MSB Register

Bit	Field Name	Access	Description
7:0	vendorIdMsb	RO/RW	Vendor ID MSB. Most significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 04h representing the MSB of the TI Vendor ID 0451h. The value may be over-written to indicate a customer Vendor ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero the value when reading this register shall reflect the OTP ROM value.

8.5.1.4 Product ID LSB Register

Table 10. Register Offset 3h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	1	0	0	1	0	1

Table 11. Bit Descriptions – Product ID LSB Register

Bit	Field Name	Access	Description
7:0	productIdLsb	RO/RW	Product ID LSB. Least significant byte of the product ID assigned by Texas Instruments and reported in the SuperSpeed Device descriptor. The default value of this register is 25h representing the LSB of the SuperSpeed product ID assigned by Texas Instruments. The value reported in the USB 2.0 Device descriptor is the value of this register bit wise XORed with 00000010b. The value may be over-written to indicate a customer product ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero the value when reading this register shall reflect the OTP ROM value.

8.5.1.5 Product ID MSB Register

Table 12. Register Offset 4h

Bit No.	7	6	5	4	3	2	1	0
Reset State	1	0	0	0	0	0	0	0

Table 13. Bit Descriptions – Product ID MSB Register

Bit	Field Name	Access	Description
7:0	productIdMsb	RO/RW	Product ID MSB. Most significant byte of the product ID assigned by Texas Instruments; the default value of this register is 80h representing the MSB of the product ID assigned by Texas Instruments. The value may be over-written to indicate a customer product ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register will reflect the OTP ROM value.

8.5.1.6 Device Configuration Register

Table 14. Register Offset 5h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	X	X	0	0

Table 15. Bit Descriptions – Device Configuration Register

Bit	Field Name	Access	Description
7	customStrings	RW	Custom strings enable. This bit controls the ability to write to the Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers 0 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers are read only 1 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers may be loaded by EEPROM or written by SMBus The default value of this bit is 0.
6	customSernum	RW	Custom serial number enable. This bit controls the ability to write to the serial number registers. 0 = The Serial Number String Length and Serial Number String registers are read only 1 = The Serial Number String Length and Serial Number String registers may be loaded by EEPROM or written by SMBus The default value of this bit is 0.
5	u1u2Disable	RW	U1 U2 Disable. This bit controls the U1/U2 support. 0 = U1/U2 support is enabled 1 = U1/U2 support is disabled, the TUSB8020B-Q1 will not initiate or accept any U1 or U2 requests on any port, upstream or downstream, unless it receives or sends a Force_LinkPM_Accept LMP. After receiving or sending an FLPMA LMP, it will continue to enable U1 and U2 according to USB 3.0 protocol until it gets a power-on reset or is disconnected on its upstream port. When the TUSB8020B-Q1 is in I^2C mode, the TUSB8020B-Q1 loads this bit from the contents of the EEPROM. When the TUSB8020B-Q1 is in SMBUS mode, the value may be over-written by an SMBus host.
4	RSVD	RO	Reserved. This bit is reserved and returns 1 when read.
3	ganged	RW	Ganged. This bit is loaded at the de-assertion of reset with the value of the GANGED/SMBA2/HS_UP terminal. 0 = When fullPwrMgmtz = 0, each port is individually power switched and enabled by the PWRCTL[2:1]/BATEN[2:1] terminals 1 = When fullPwrMgmtz = 0, the power switch control for all ports is ganged and enabled by the PWRCTL1/BATEN1 terminal When the TUSB8020B-Q1 is in I^2C mode, the TUSB8020B-Q1 loads this bit from the contents of the EEPROM. When the TUSB8020B-Q1 is in SMBUS mode, the value may be over-written by an SMBus host.
2	fullPwrMgmtz	RW	Full Power Management. This bit is loaded at the de-assertion of reset with the value of the FULLPWRMGMTz/SMBA1/SS_UP terminal. 0 = Port power switching and over-current status reporting is enabled 1 = Port power switching and over-current status reporting is disabled When the TUSB8020B-Q1 is in I^2C mode, the TUSB8020B-Q1 loads this bit from the contents of the EEPROM. When the TUSB8020B-Q1 is in SMBUS mode, the value may be over-written by an SMBus host.

Table 15. Bit Descriptions – Device Configuration Register (continued)

Bit	Field Name	Access	Description
1	RSVD	RW	Reserved. This bit is reserved and should not be altered from the default.
0	RSVD	RO	Reserved. This field is reserved and returns 0 when read.

8.5.1.7 Battery Charging Support Register

Table 16. Register Offset 6h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	X	X

Table 17. Bit Descriptions – Battery Charging Support Register

Bit	Field Name	Access	Description
7:2	RSVD	RO	Reserved. Read only, returns 0 when read.
1:0	batEn[1:0]	RW	Battery Charger Support. The bits in this field indicate whether the downstream port implements the charging port features. 0 = The port is not enabled for battery charging support features 1 = The port is enabled for battery charging support features Each bit corresponds directly to a downstream port, i.e. batEn0 corresponds to downstream port 1, and batEN1 corresponds to downstream port 2. The default value for these bits are loaded at the de-assertion of reset with the value of PWRCTL/BATEN[1:0]. When in I2C/SMBus mode the bits in this field may be over-written by EEPROM contents or by an SMBus host.

8.5.1.8 Device Removable Configuration Register

Table 18. Register Offset 7h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	X	X

Table 19. Bit Descriptions – Device Removable Configuration Register

Bit	Field Name	Access	Description
7	customRmbl	RW	Custom removable status. When this field is a 1, the TUSB8020B-Q1 uses rmbl bits in this register to identify removable status for the ports.
6:2	RSVD	RO	Reserved. Read only, returns 0 when read. Bits 3:2 are RW. They are reserved and return zero when read.
1:0	rmbl[1:0]	RW	Removable. The bits in this field indicate whether a device attached to downstream ports 2 through 1 are removable or permanently attached. 0 = The device attached to the port is not removable 1 = The device attached to the port is removable Each bit corresponds directly to a downstream port n + 1, i.e. rmbl0 corresponds to downstream port 1, rmbl1 corresponds to downstream port 2, etc. This field is read only unless the customRmbl bit is set to 1. Otherwise the value of this filed reflects the inverted values of the OTP ROM non_rmb[1:0] field.

8.5.1.9 Port Used Configuration Register

Table 20. Register Offset 8h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	1	1

Table 21. Bit Descriptions – Port Used Configuration Register

Bit	Field Name	Access	Description
7:0	RSVD	RO	Reserved. Read only.

8.5.1.10 PHY Custom Configuration Register

Table 22. Register Offset 9h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 23. Bit Descriptions – PHY Custom Configuration Register

Bit	Field Name	Access	Description
7:6	RSVD	RO	Reserved. Read only, returns 0 when read.
5	RSVD	RW	Reserved. This bit is reserved and should not be altered from the default.
4:2	RSVD	RO	Reserved. Read only, returns 0 when read.
1:0	RSVD	RW	Reserved. This field is reserved and should not be altered from the default.

8.5.1.11 Device Configuration Register 2

Table 24. Register Offset Ah

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	X	0	0	0	0	0

Table 25. Bit Descriptions – Device Configuration Register 2

Bit	Field Name	Access	Description
7	RSVD	RO	Reserved. Read only, returns 0 when read.
6	customBCfeatures	RW	Custom Battery Charging Feature Enable. This bit controls the ability to write to the battery charging feature configuration controls. 0 = The HiCurAcpModeEn and AutoModeEnz bits are read only and the values are loaded from the OTP ROM. 1 = The HiCurAcpModeEn and AutoModeEnz bits are read/write and can be loaded by EEPROM or written by SMBus. from this register. This bit may be written simultaneously with HiCurAcpModeEn and AutoModeEnz.
5	pwrctlPol	RW	Power enable polarity. This bit is loaded at the de-assertion of reset with the inverse value of the PWRCTL_POL terminal. 0 = PWRCTL polarity is active low 1 = PWRCTL polarity is active high When the TUSB8020B-Q1 is in I^2C mode, the TUSB8020B-Q1 loads this bit from the contents of the EEPROM. When the TUSB8020B-Q1 is in SMBUS mode, the value may be over-written by an SMBus host.
4	HiCurAcpModeEn	RO/RW	High-current ACP mode enable. This bit enables the high-current tablet charging mode when the automatic battery charging mode is enabled for downstream ports. 0 = High current divider mode disabled 1 = High current divider mode enabled This bit is read only unless the customBCfeatures bit is set to 1. Otherwise the value of this bit reflects the value of the OTP ROM HiCurAcpModeEn bit.
3	RSVD	RW	Reserved
2	dsportEcrEn	RW	DSPort ECR enable. This bit enables full implementation of the DSPORT ECR (April 2013). 0 = DSPort ECR (April 2013) is enabled with the exception of changes related to the CCS bit is set upon entering U0, and changes related to avoiding or reporting compliance mode entry. 1 = The full DSport ECR (April 2013) is enabled.
1	autoModeEnz	RO/RW	Automatic Mode Enable. This bit is loaded from the OTP ROM. The automatic mode only applies to downstream ports with battery charging enabled when the upstream port is not connected. Under these conditions: 0 = Automatic mode battery charging features are enabled. 1 = Automatic mode is disabled; only Battery Charging 1.2 DCP mode is supported. NOTE: When the upstream port is connected, Battery Charging 1.2 CDP mode will be supported on all ports that enabled for battery charging support regardless of the value of this bit. The Automode is enabled if this field is zero and the pwrctlPol field is zero. This bit is read only unless the customBCfeatures bit is set to 1. Otherwise the value of this bit reflects the value of the OTP ROM AutoModeEnz bit.
0	RSVD	RO	Reserved. Read only, returns 0 when read.

8.5.1.12 UUID Registers

Table 26. Register Offset 10h-1Fh

Bit No.	7	6	5	4	3	2	1	0
Reset State	X	X	X	X	X	X	X	X

Table 27. Bit Descriptions – UUID Byte N Register

Bit	Field Name	Access	Description
7:0	uuidByte[n]	RO	UUID byte N. The UUID returned in the Container ID descriptor. The value of this register is provided by the device and is meets the UUID requirements of Internet Engineering Task Force (IETF) RFC 4122 A UUID URN Namespace.

8.5.1.13 Language ID LSB Register

Table 28. Register Offset 20h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	1	0	0	1

Table 29. Bit Descriptions – Language ID LSB Register

Bit	Field Name	Access	Description
7:0	langIdLsb	RW	Language ID least significant byte. This register contains the value returned in the LSB of the LANGID code in string index 0. The TUSB8020B-Q1 only supports one language ID. The default value of this register is 09h representing the LSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host.

8.5.1.14 Language ID MSB Register

Table 30. Register Offset 21h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	0	0

Table 31. Bit Descriptions – Language ID MSB Register

Bit	Field Name	Access	Description
7:0	langIdMsb	RO/RW	Language ID most significant byte. This register contains the value returned in the MSB of the LANGID code in string index 0. The TUSB8020B-Q1 only supports one language ID. The default value of this register is 04h representing the MSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host.

8.5.1.15 Serial Number String Length Register

Table 32. Register Offset 22h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	1	0	0	0

Table 33. Bit Descriptions – Serial Number String Length Register

Bit	Field Name	Access	Description
7:6	RSVD	RO	Reserved. Read only, returns 0 when read.
5:0	serNumStringLen	RO/RW	Serial number string length. The string length in bytes for the serial number string. The default value is 18h indicating that a 24 byte serial number string is supported. The maximum string length is 32 bytes. When customSernum is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a serial number string of serNumbStringLen bytes is returned at string index 1 from the data contained in the Serial Number String registers.

8.5.1.16 Manufacturer String Length Register

Table 34. Register Offset 23h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 35. Bit Descriptions – Manufacturer String Length Register

Bit	Field Name	Access	Description
7	RSVD	RO	Reserved. Read only, returns 0 when read.
6:0	mfgStringLen	RO/RW	Manufacturer string length. The string length in bytes for the manufacturer string. The default value is 0, indicating that a manufacturer string is not provided. The maximum string length is 64 bytes. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a manufacturer string of mfgStringLen bytes is returned at string index 3 from the data contained in the Manufacturer String registers.

8.5.1.17 Product String Length Register

Table 36. Register Offset 24h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 37. Bit Descriptions – Product String Length Register

Bit	Field Name	Access	Description
7	RSVD	RO	Reserved. Read only, returns 0 when read.
6:0	prodStringLen	RO/RW	Product string length. The string length in bytes for the product string. The default value is 0, indicating that a product string is not provided. The maximum string length is 64 bytes. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a product string of prodStringLen bytes is returned at string index 2 from the data contained in the Product String registers.

8.5.1.18 Serial Number Registers

Table 38. Register Offset 30h-4Fh

Bit No.	7	6	5	4	3	2	1	0
Reset State	X	X	x	x	x	x	x	x

Table 39. Bit Descriptions – Serial Number Registers

Bit	Field Name	Access	Description
7:0	serialNumber[n]	RO/RW	Serial Number byte N. The serial number returned in the Serial Number string descriptor at string index 1. The default value of these registers is set by TI. When customSernum is 1, these registers may be over-written by EEPROM contents or by an SMBus host.

8.5.1.19 Manufacturer String Registers

Table 40. Register Offset 50h-8Fh

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 41. Bit Descriptions – Manufacturer String Registers

Bit	Field Name	Access	Description
7:0	mfgStringByte[n]	RO/RW	Manufacturer string byte N. These registers provide the string values returned for string index 3 when mfgStringLen is greater than 0. The number of bytes returned in the string is equal to mfgStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

8.5.1.20 Product String Registers

Table 42. Register Offset 90h-CFh

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 43. Bit Descriptions – Product String Byte N Register

Bit	Field Name	Access	Description
7:0	prodStringByte[n]	RW	Product string byte N. These registers provide the string values returned for string index 2 when prodStringLen is greater than 0. The number of bytes returned in the string is equal to prodStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

8.5.1.21 Additional Feature Configuration Register

Table 44. Register Offset F0h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 45. Bit Descriptions – Additional Feature Configuration Register

Bit	Field Name	Access	Description
7:1	RSVD	RO	Reserved. Read only, returns 0 when read.
0	usb3spreadDis	RW	USB3 Spread Spectrum Disable. This bit allows firmware to disable the spread spectrum function of the USB3 phy PLL. 0 = Spread spectrum function is enabled 1= Spread spectrum function is disabled This bit is loaded at the de-assertion of reset with the value of the SCL/SMBCLK terminal.

8.5.1.22 Charging Port Control Register

Table 46. Register Offset F2h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 47. Bit Descriptions – Charging Port Control Register

Bit	Field Name	Access	Description
7:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:1	pwronTime	RW	Power On Delay Time. When dsportEcrEn is set, this field sets the delay time from the removal disable of PWRCTL to the enable of PWRCTL when transitioning battery charging modes. For example, when disabling the power on a transition from custom charging mode to Dedicated Charging Port Mode. The nominal timing is defined as follows: TPWRON_EN = (pwronTime + 1) x 200 ms (1) These registers may be over-written by EEPROM contents or by an SMBus host.
0	RSVD	RW	Reserved. This bit is reserved and should not be altered from the default.

8.5.1.23 Device Status and Command Register

Table 48. Register Offset F8h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 49. Bit Descriptions – Device Status and Command Register

Bit	Field Name	Access	Description
7:2	RSVD	RO	Reserved. Read only, returns 0 when read.
1	smbusRst	RSU	SMBus interface reset. This bit loads the registers back to their GRSTz values. This bit is set by writing a 1 and is cleared by hardware on completion of the reset. A write of 0 has no effect.
0	cfgActive	RCU	Configuration active. This bit indicates that configuration of the TUSB8020B-Q1 is currently active. The bit is set by hardware when the device enters the I^2C or SMBus mode. The TUSB8020B-Q1 shall not connect on the upstream port while this bit is 1. When in the SMBus mode, this bit must be cleared by the SMBus host in order to exit the configuration mode and allow the upstream port to connect. The bit is cleared by a writing 1. A write of 0 has no effect.

9 Applications and Implementation

9.1 Application Information

The TUSB8020B-Q1 is a two-port USB 3.0 compliant hub. It provides simultaneous SuperSpeed USB and high-speed/full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, full-speed, or low speed connections on the downstream port. The TUSB8020B-Q1 can be used in any application that needs additional USB compliant ports. For example, a specific notebook may only have two downstream USB ports. By using the TUSB8020B-Q1, the notebook can increase the downstream port count to three.

9.2 Typical Applications

A common application for the TUSB8020B-Q1 is as a self powered standalone USB hub product. The product is powered by an external 5V DC Power adapter. In this application, using a USB cable TUSB8020B-Q1's upstream port is plugged into a USB Host controller. The downstream ports of the TUSB8020B-Q1 are exposed to users for connecting USB hard drives, camera, flash drive, and so forth.

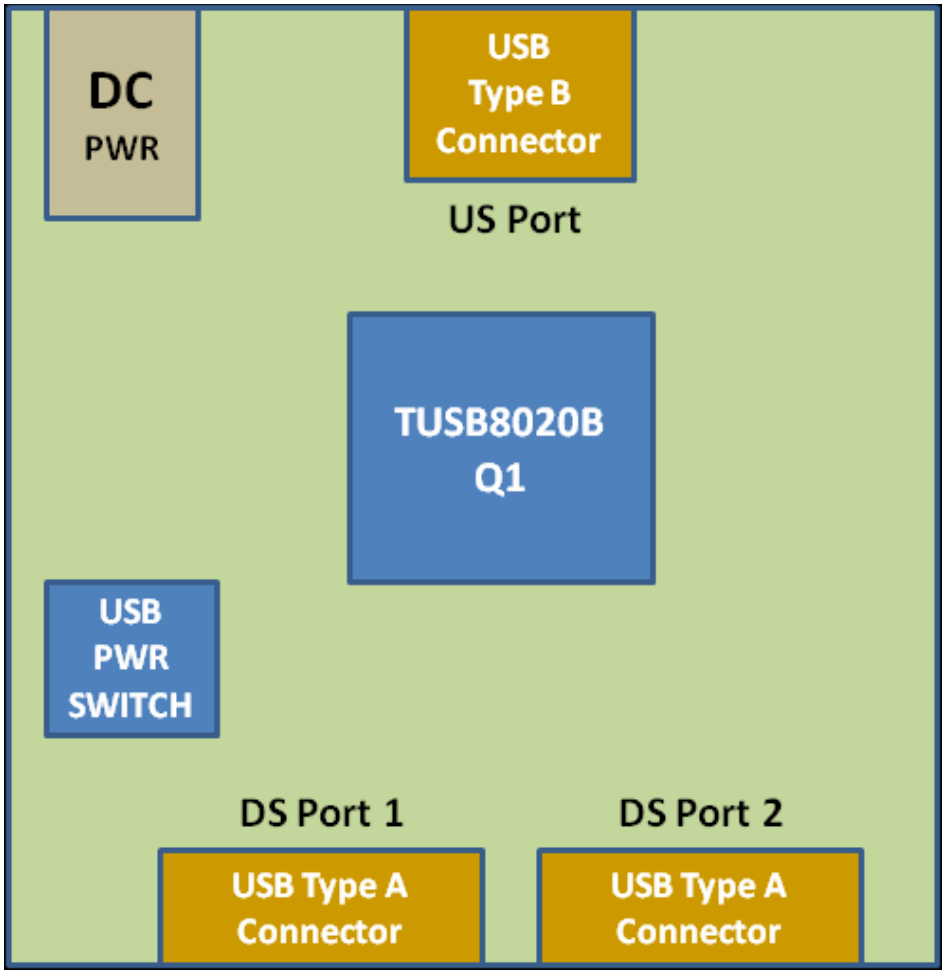


Figure 3. Discrete USB Hub Product

Typical Applications (continued)

9.2.1 Design Requirements

Table 50. Input Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD Supply	1.1V
VDD33 Supply	3.3V
Upstream Port USB Support (SS, HS, FS)	SS, HS, FS
Downstream Port 1 USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
Downstream Port 2 USB Support (SS, HS, FS, LS)	SS, HS, FS, LS
# of Removable Downstream Ports	2
# of Non-Removable Downstream Ports	0
Full Power Management of Downstream Ports	Yes. (FULLPWRMGMTZ = 0)
Individual Control of Downstream Port Power Switch	Yes. (GANGED = 0)
Power Switch Enable Polarity	Active High. (PWRCTL_POL = 0)
Battery Charge Support for Downstream Port 1	Yes
Battery Charge Support for Downstream Port 2	Yes
I2C EEPROM Support	No.
24MHz Clock Source	Crystal

9.2.2 Detailed Design Procedure

9.2.2.1 Upstream Port Implementation

The upstream of the TUSB8020B-Q1 is connected to a USB3 Type B connector. This particular example has GANGED terminal and FULLPWRMGMTZ terminal pulled low which results in individual power support each downstream port. The VBUS signal from the USB3 Type B connector is feed through a voltage divider. The purpose of the voltage divider is to make sure the level meets USB_VBUS input requirements.

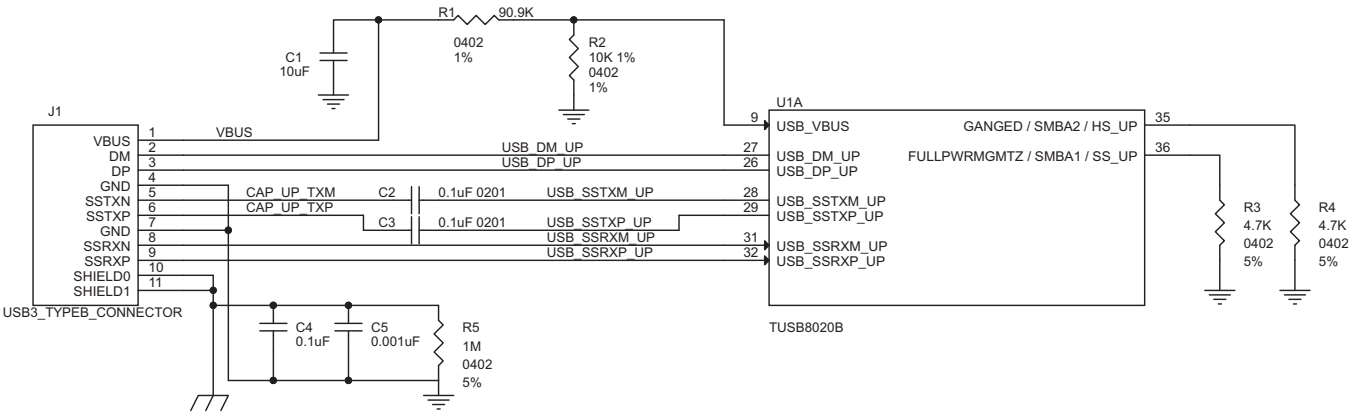


Figure 4. Upstream Port Implementation

9.2.2.2 Downstream Port 1 Implementation

The downstream port 1 of the TUSB8020B-Q1 is connected to a USB3 Type A connector. With BATEN1 terminal pulled up, Battery Charge support is enabled for Port 1. If Battery Charge support is not needed, then pull-up resistor on BATEN1 should be uninstalled. The PWRCTL_POL is pulled down which will result in active high power enable (PWRCTL1 and PWRCTL2) for a USB VBUS power switch.

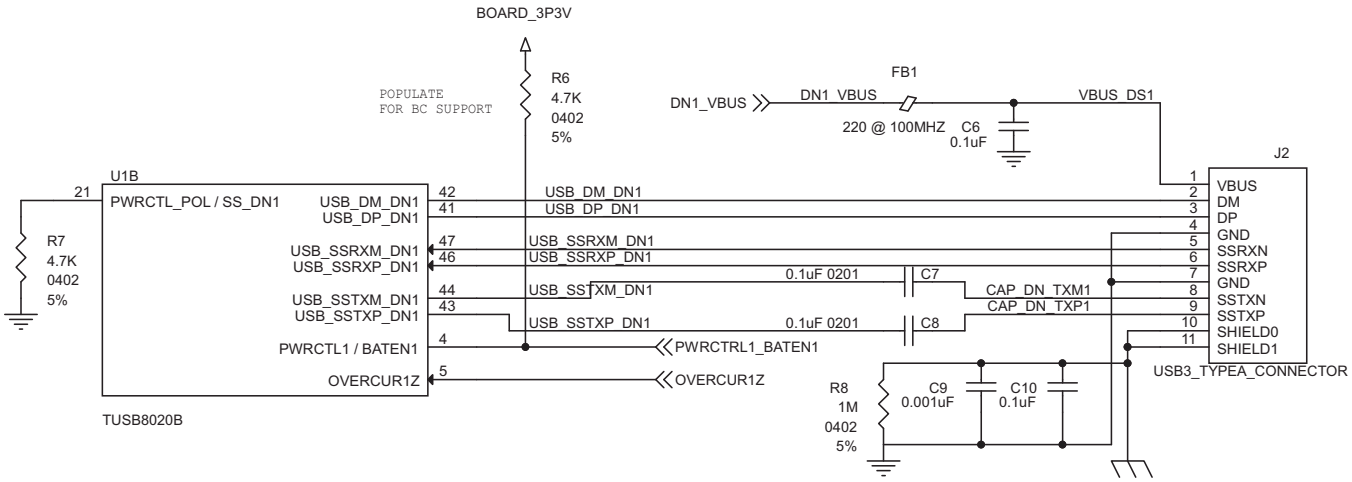


Figure 5. Downstream Port 1 Implementation

9.2.2.3 Downstream Port 2 Implementation

The downstream port 2 of the TUSB8020B-Q1 is connected to a USB3 Type A connector. With BATEN2 terminal pulled up, Battery Charge support is enabled for Port 2. If Battery Charge support is not needed, then pull-up resistor on BATEN2 should be uninstalled.

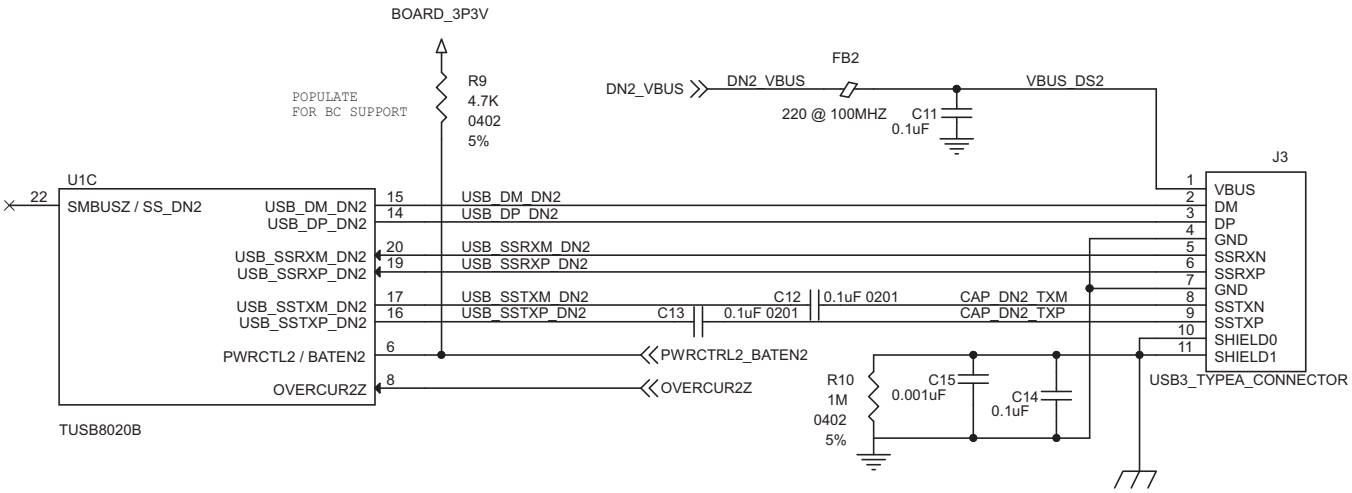


Figure 6. Downstream Port 2 Implementation

9.2.2.4 VBUS Power Switch Implementation

This particular example uses the Texas Instruments TPS2561 dual channel precision adjustable current-limited power switch. For details on this power switch or other power switches available from Texas Instruments, please refer to the Texas Instruments website.

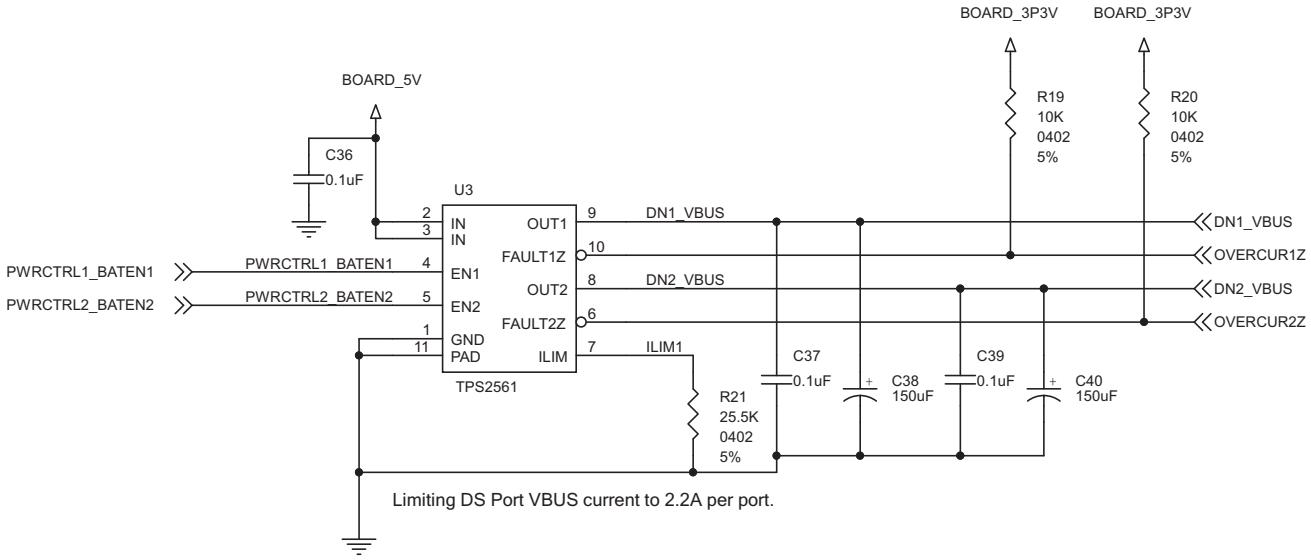


Figure 7. Power Switch Implementation

9.2.2.5 Clock, Reset, and Misc

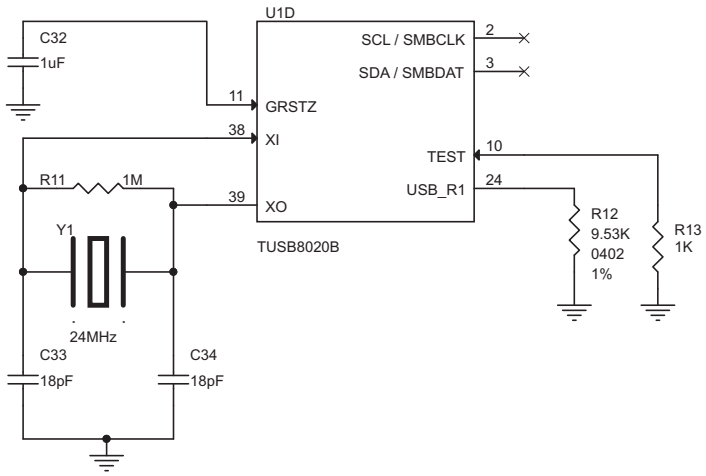


Figure 8. Clock, Reset, and Misc

9.2.2.6 Power Implementation

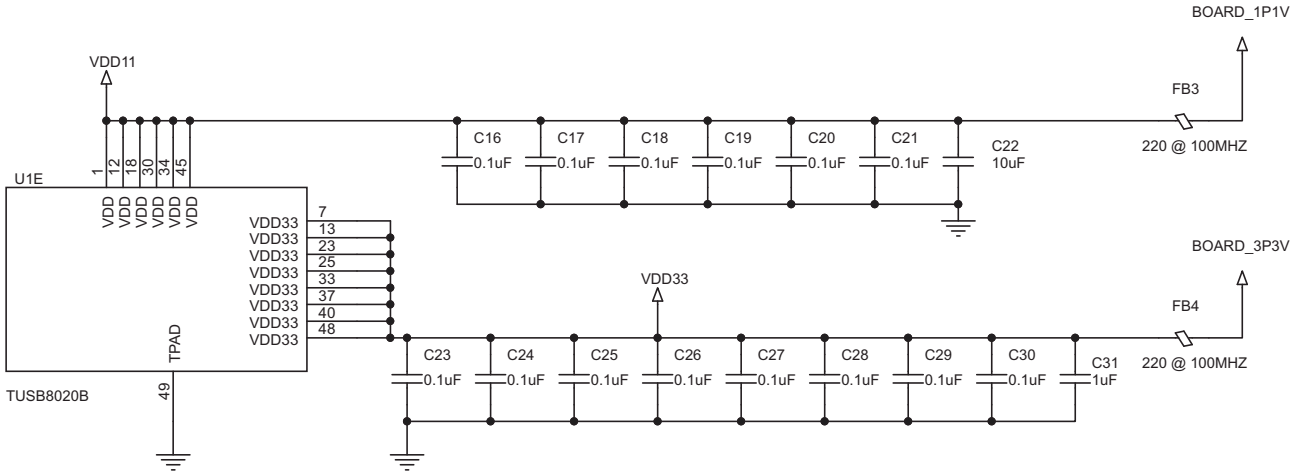


Figure 9. Power Implementation

9.2.3 Application Curves

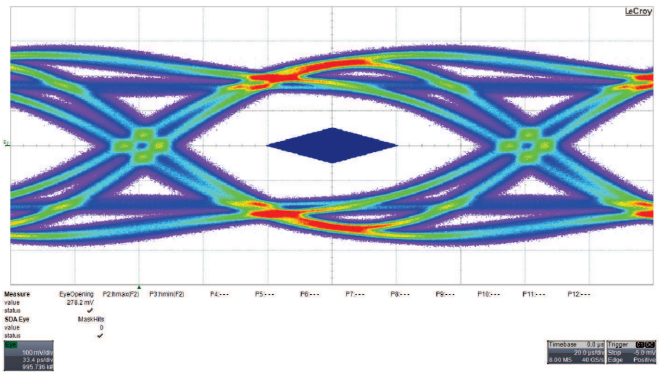


Figure 10. SuperSpeed TX Eye for Downstream Port 1

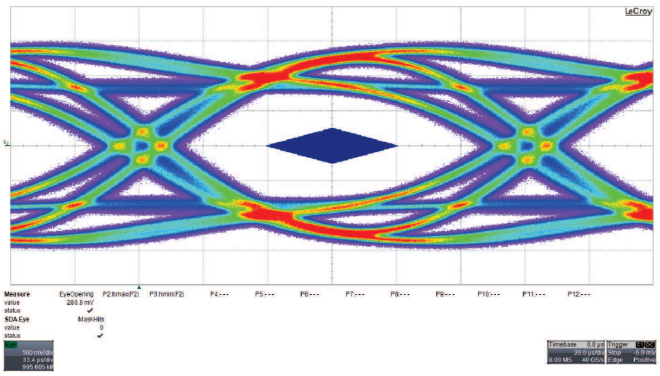


Figure 11. : SuperSpeed TX Eye for Downstream Port 2

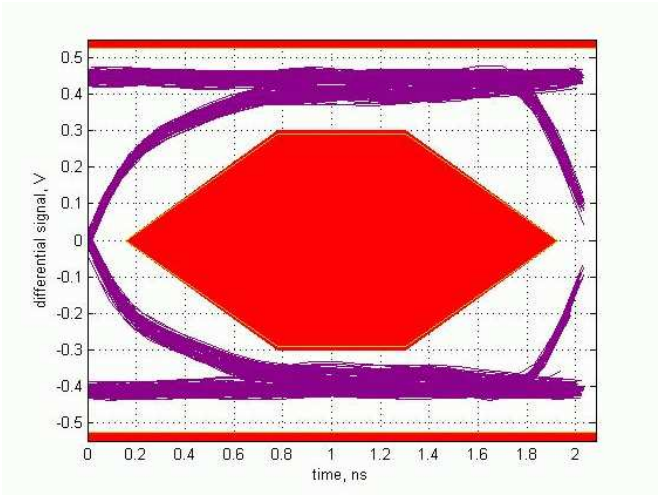


Figure 12. : HighSpeed TX Eye for Downstream Port 1

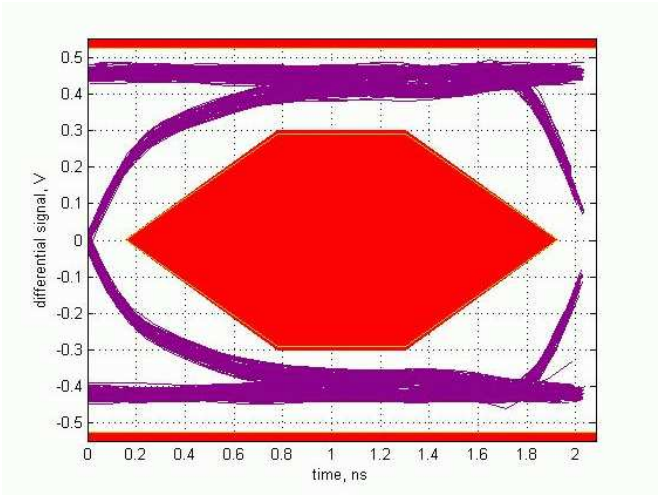


Figure 13. HighSpeed TX Eye for Downstream Port 2

10 Power Supply Recommendations

10.1 Power Supply

V_{DD} should be implemented as a single power plane, as should V_{DD33}.

- The V_{DD} terminals of the TUSB8020B-Q1 supply 1.1 V (nominal) power to the core of the TUSB8020B-Q1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The DC resistance of the ferrite bead on the core power rail can affect the voltage provided to the device due to the high current draw on the power rail. The output of the core voltage regulator may need to be adjusted to account for this or a ferrite bead with low DC resistance (less than 0.05 Ω) can be selected.
- The V_{DD33} terminals of the TUSB8020B-Q1 supply 3.3-V power rail to the I/O of the TUSB8020B-Q1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- All power rails require a 10-µF capacitor or 1-µF capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. The smaller decoupling capacitors should be placed as close to the TUSB8020B-Q1 power pins as possible with an optimal grouping of two of differing values per pin.

10.2 Downstream Port Power

- The downstream port power, VBUS, must be supplied by a source capable of supplying 5 V and at least 900 mA per port. Downstream port power switches can be controlled by the TUSB8020BPHP signals. It is also possible to leave the downstream port power always enabled.
- A large bulk low-ESR capacitor of 22 µF or larger is required on each downstream port's VBUS to limit in-rush current.
- The ferrite beads on the VBUS pins of the downstream USB port connections are recommended for both ESD and EMI reasons. A 0.1-µF capacitor on the USB connector side of the ferrite provides a low impedance path to ground for fast rise time ESD current that might have coupled onto the VBUS trace from the cable.

10.3 Ground

It is recommended that only one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the TUSB8020B-Q1 and any of the voltage regulators should be connected to this plane with vias. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

11 Layout

11.1 Layout Guidelines

11.1.1 Placement

1. 9.53K ±1% resistor connected to terminal USB_R1 should be placed as close as possible to the TUSB8020B-Q1.
2. A 0.1-µF capacitor should be placed as close as possible on each V_{DD} and V_{DD33} power pin.
3. The 100-nF capacitors on the SSTXP and SSTXM nets should be placed close to the USB connector (Type A, Type B, and so forth).
4. The ESD and EMI protection devices (if used) should also be placed as possible to the USB connector.
5. If a crystal is used, it must be placed as close as possible to the TUSB8020B-Q1's XI and XO terminals.
6. Place voltage regulators as far away as possible from the TUSB8020B-Q1, the crystal, and the differential pairs.
7. In general, the large bulk capacitors associated with each power rail should be placed as close as possible to the voltage regulators.

11.1.2 Package Specific

1. The TUSB8020B-Q1 package as a 0.5-mm pin pitch.
2. The TUSB8020B-Q1 package has a 3.6-mm x 3.6-mm thermal pad. This thermal pad must be connected to ground through a system of vias.
3. All vias under device, except for those connected to thermal pad, should be solder masked to avoid any potential issues with thermal pad layouts.

11.1.3 Differential Pairs

This section describes the layout recommendations for all the TUSB8020B-Q1 differential pairs: USB_DP_XX, USB_DM_XX, USB_SSTXP_XX, USB_SSTXM_XX, USB_SSRXP_XX, and USB_SSRXM_XX.

1. Must be designed with a differential impedance of 90 Ω ±10%.
2. In order to minimize cross talk, it is recommended to keep high speed signals away from each other. Each pair should be separated by at least 5 times the signal trace width. Separating with ground as depicted in the layout example will also help minimize cross talk.
3. Route all differential pairs on the same layer adjacent to a solid ground plane.
4. Do not route differential pairs over any plane split.
5. Adding test points will cause impedance discontinuity and will therefore negative impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
6. Avoid 90° turns in trace. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135°. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
7. Minimize the trace lengths of the differential pair traces. The maximum recommended trace length for SS differential pair signals and USB 2.0 differential pair signals is eight inches. Longer trace lengths require very careful routing to assure proper signal integrity.
8. Match the etch lengths of the differential pair traces (i.e. DP and DM or SSRXP and SSRXM or SSTXP and SSTXM). There should be less than 5 mils difference between a SS differential pair signal and its complement. The USB 2.0 differential pairs should not exceed 50 mils relative trace length difference.
9. The etch lengths of the differential pair groups do not need to match (i.e. the length of the SSRX pair to that of the SSTX pair), but all trace lengths should be minimized.
10. Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close as possible to the TUSB8020B-Q1 device.
11. To ease routing, the polarity of the SS differential pairs can be swapped. This means that SSTXP can be routed to SSTXM or SSRXM can be routed to SSRXP.

Layout Guidelines (continued)

12. Do not place power fuses across the differential pair traces.

11.2 Layout Example

11.2.1 Upstream Port

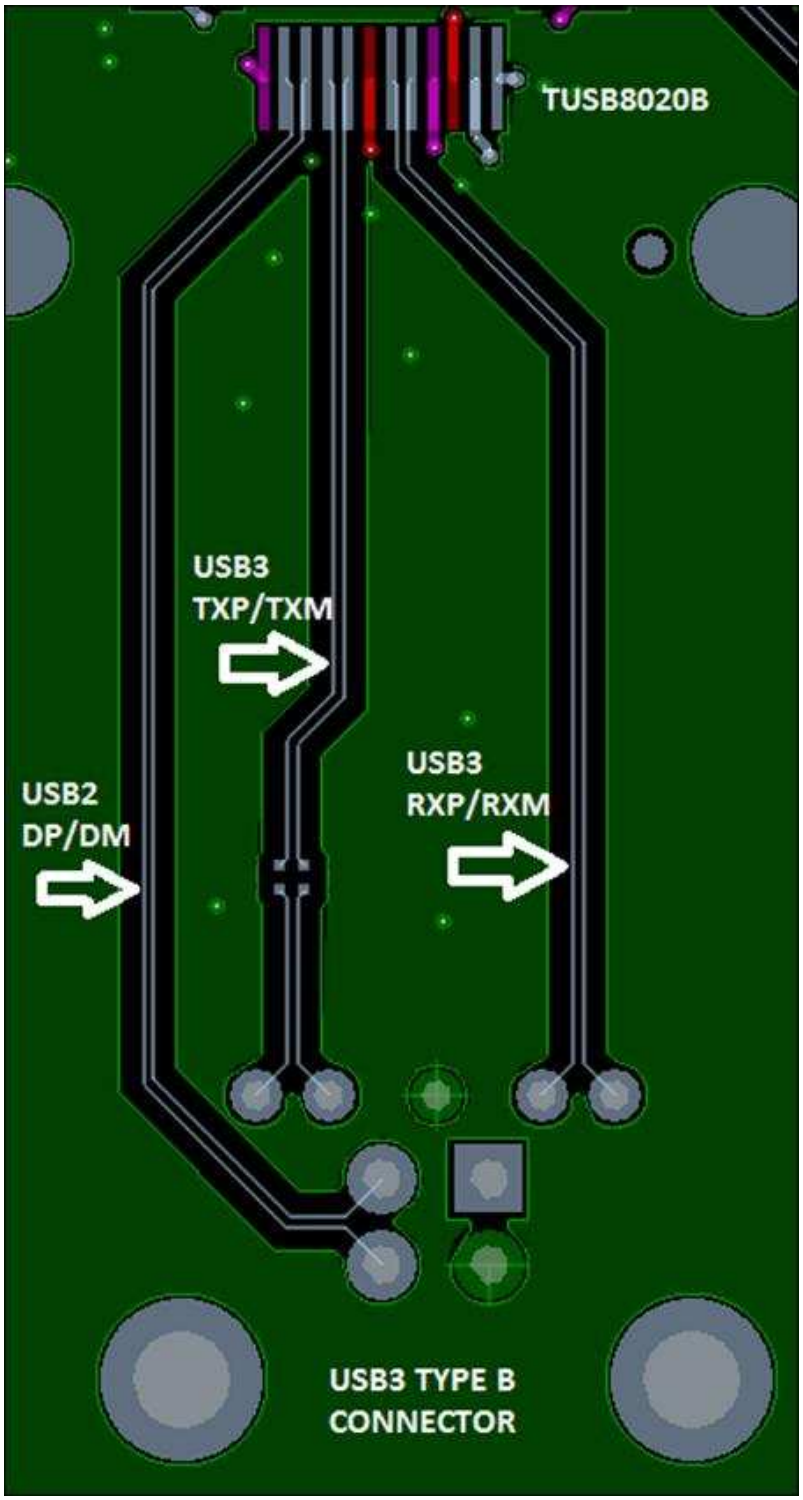


Figure 14. Example Routing of Upstream Port

Layout Example (continued)

11.2.2 Downstream Port

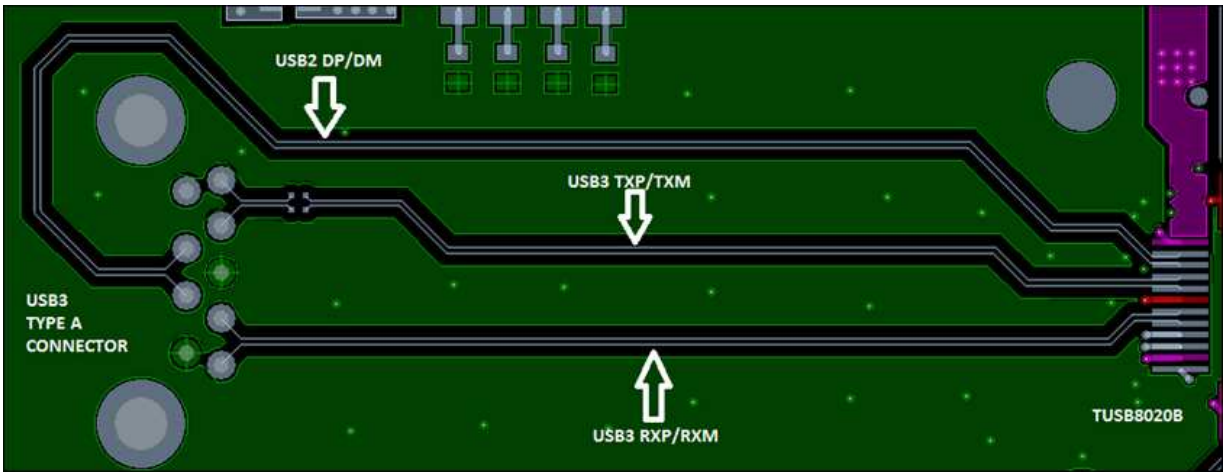


Figure 15. Example Routing of Downstream Port

11.2.3 Thermal Pad

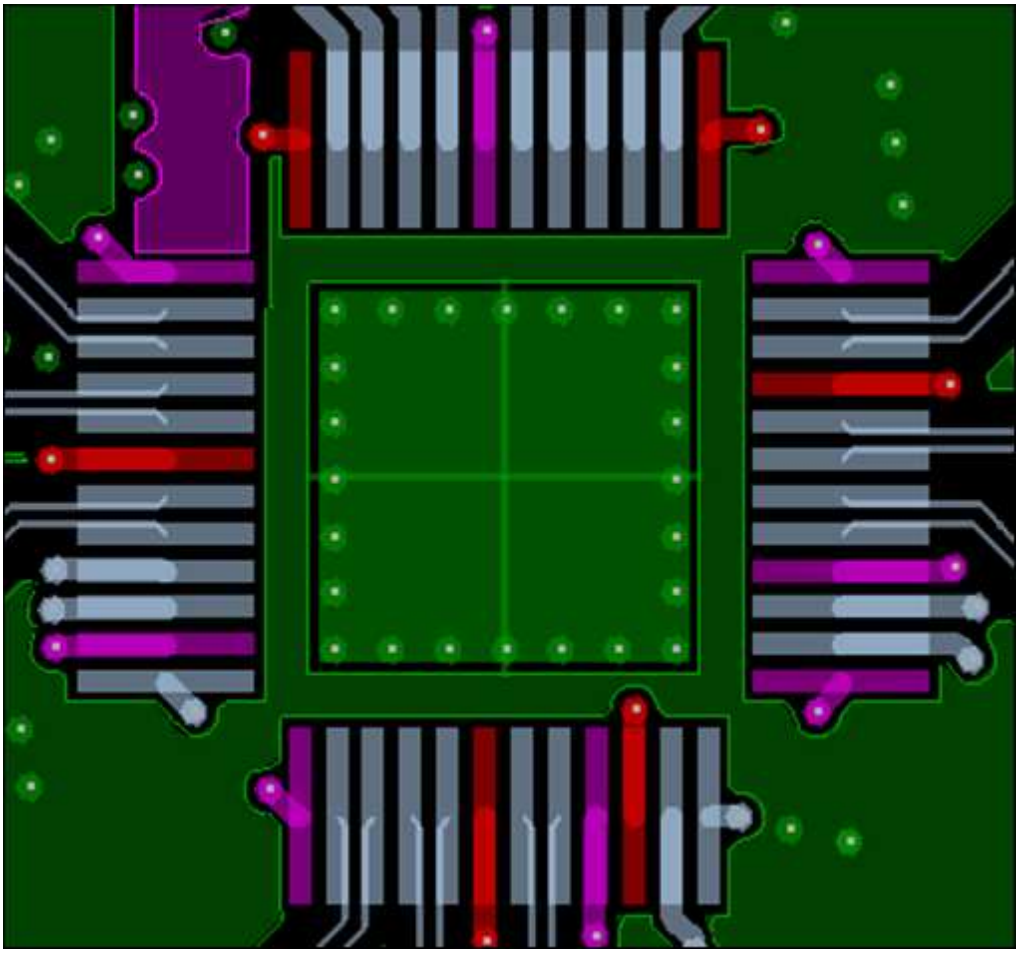


Figure 16. Example Thermal Pad Layout

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB8020BIPHPQ1	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T8020BIQ1
TUSB8020BIPHPQ1.A	Active	Production	HTQFP (PHP) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T8020BIQ1
TUSB8020BIPHPRQ1	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T8020BIQ1
TUSB8020BIPHPRQ1.A	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T8020BIQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TUSB8020B-Q1 :

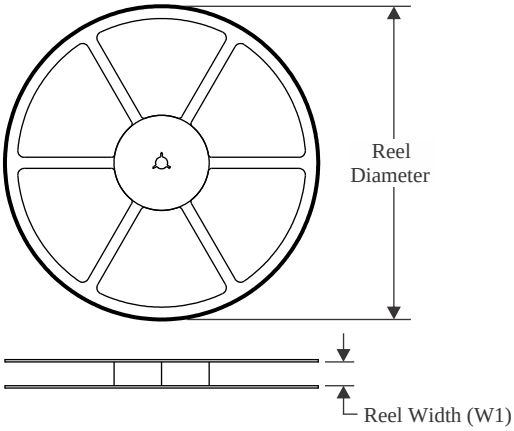
- Catalog : TUSB8020B

NOTE: Qualified Version Definitions:

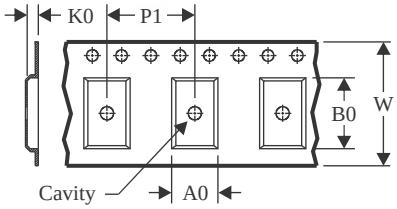
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

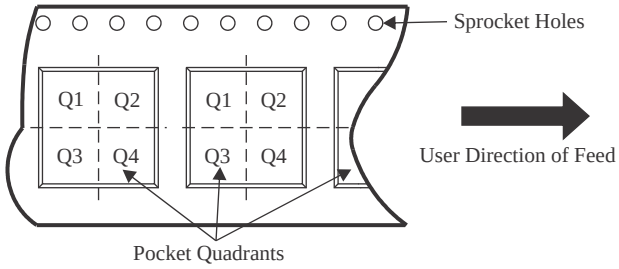


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

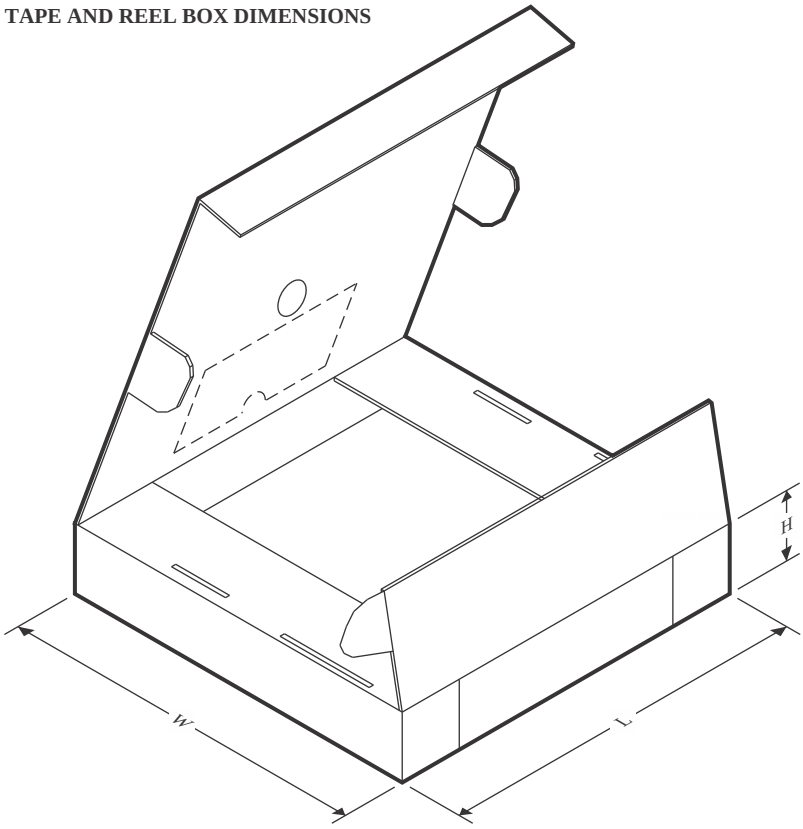
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB8020BIPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

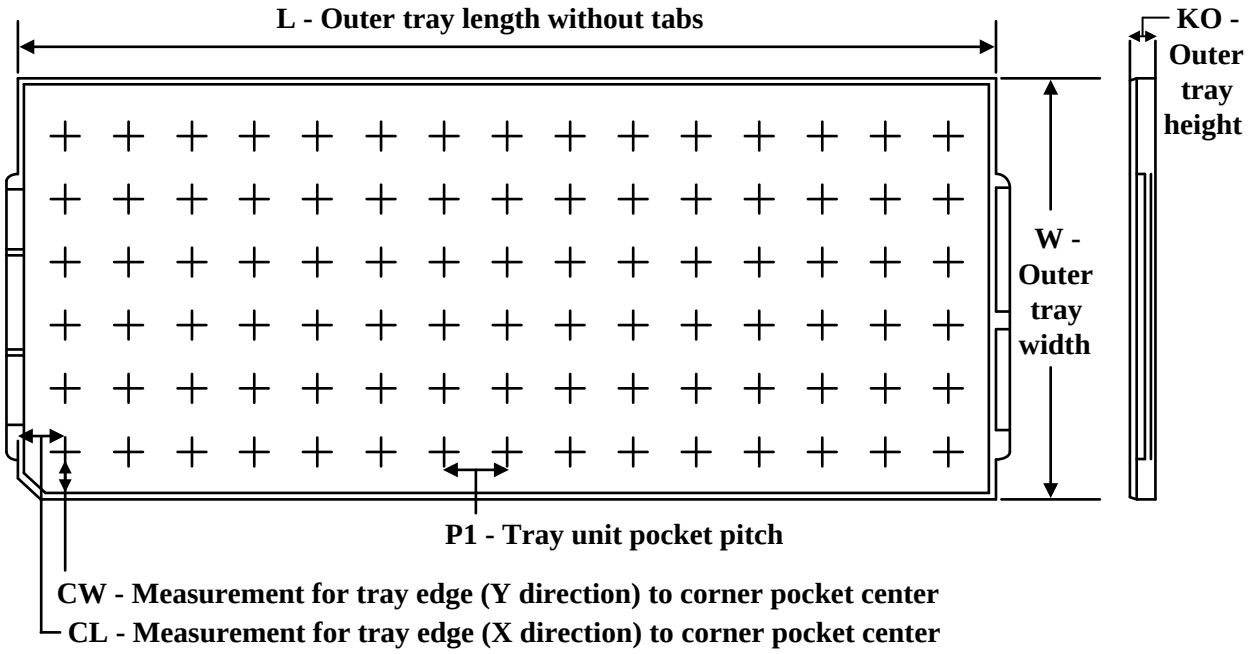
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB8020BIPHPRQ1	HTQFP	PHP	48	1000	336.6	336.6	31.8

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TUSB8020BIPHPQ1	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TUSB8020BIPHPQ1.A	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

GENERIC PACKAGE VIEW

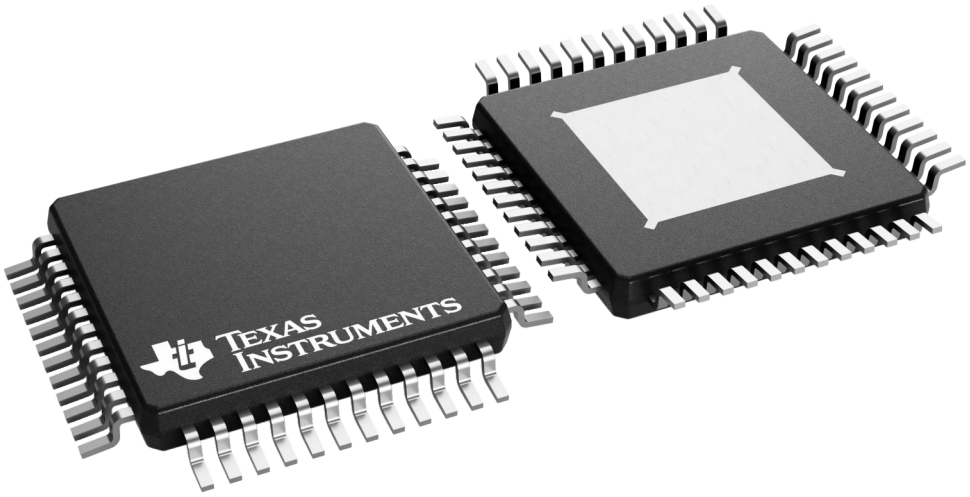
PHP 48

TQFP - 1.2 mm max height

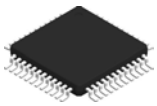
7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



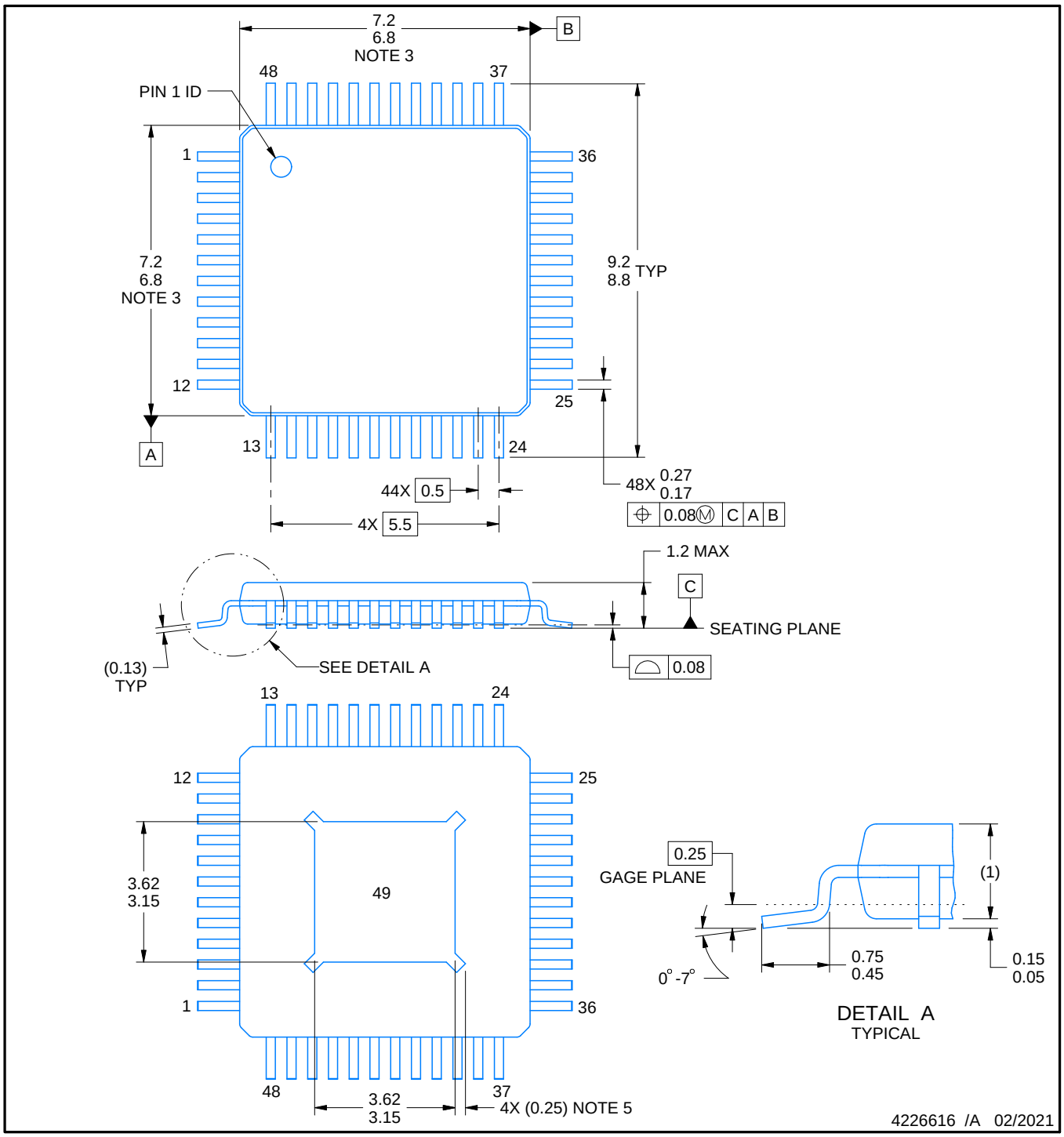
4226443/A



PACKAGE OUTLINE

PHP0048E

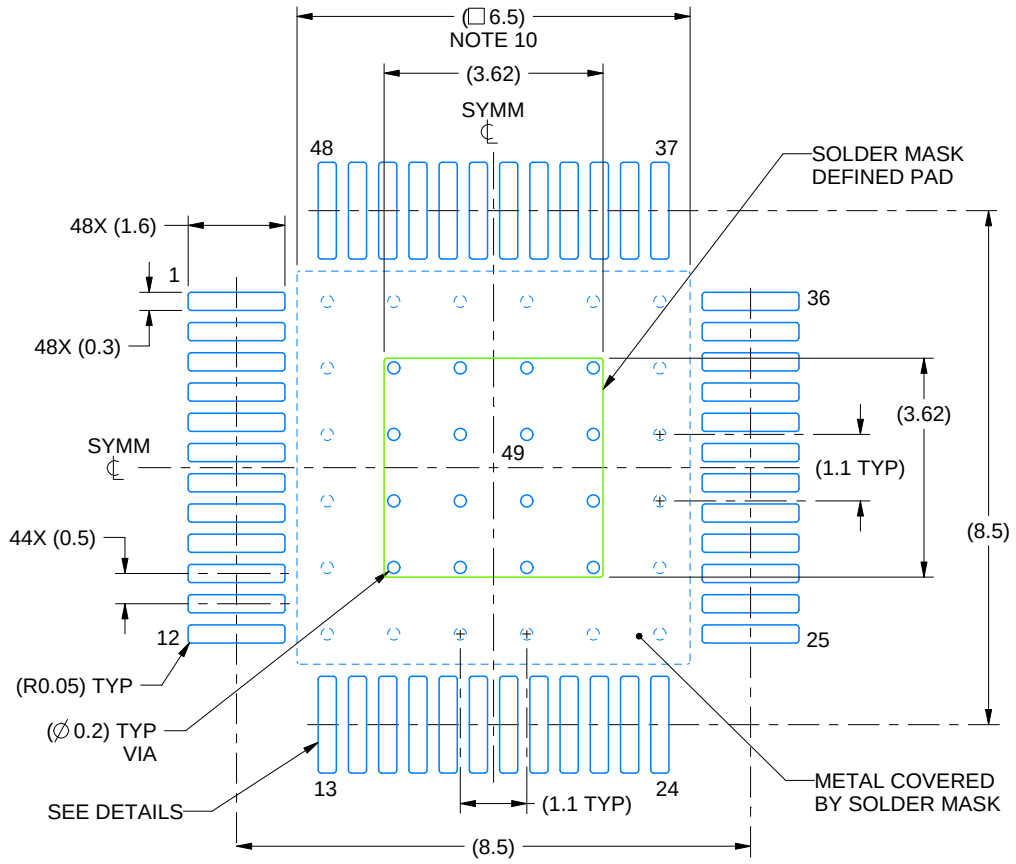
PowerPAD™ HTQFP - 1.2 mm max height



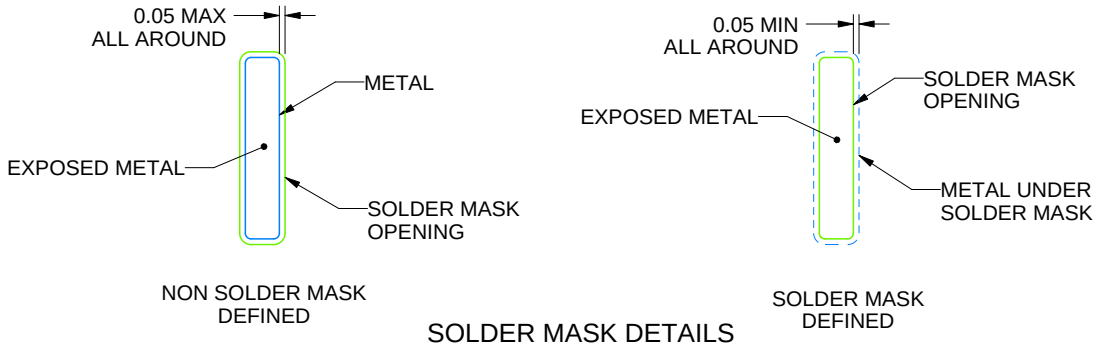
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

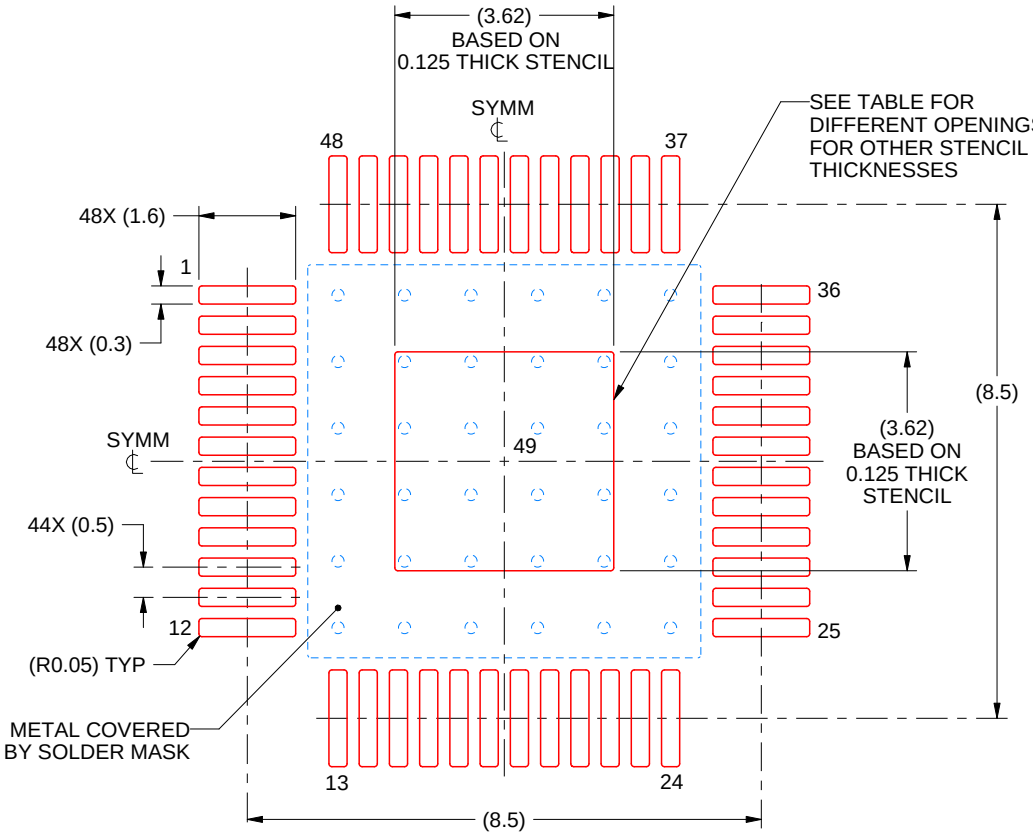


SOLDER MASK DETAILS

4226616 /A 02/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.05 X 4.05
0.125	3.62 x 3.62 (SHOWN)
0.150	3.30 x 3.30
0.175	3.06 x 3.06

4226616 /A 02/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025