TVS5200 52V Flat-Clamp Surge Protection Device

1 Features

- IEC 61000-4-5 Surge Protection:
  - 30A (8/20µs)
  - Clamping voltage: 58.9V typical at 20A (8/20µs)
- Low leakage current:
  - 25nA typical at 27°C
  - 100nA typical at 85°C
- Low capacitance: 154pF
- Integrated IEC 61000-4-2 ESD protection

2 Applications

- 48V USB Type-C EPR
- Power lines

3 Description

The TVS5200 robustly shunts up to 30A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes. The TVS5200 uses a unique feedback mechanism to provide precise flat clamping during a fault, reinforcing system exposure below 60V. The tight voltage regulation allows designers to confidently select system components with a lower voltage tolerance, lowering system costs and complexity without sacrificing robustness.

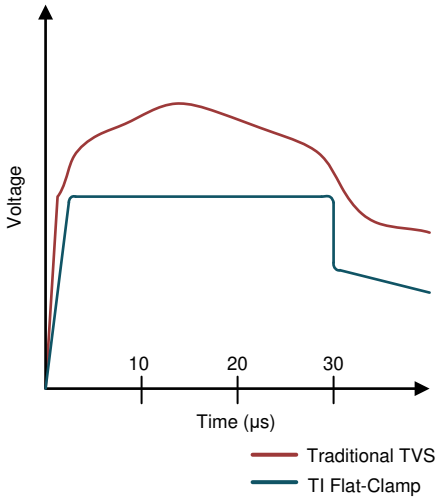
In addition, the TVS5200 is available in a 1.6mm × 1.6mm footprint, which is designed for space constrained applications. The extremely low device leakage and capacitance allows a minimal effect on the protected line.

The TVS5200 is part of TI's Flat-Clamp family of surge devices. For more information on the other devices in the family, see the *Related Products* section.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE (2)
TVS5200	VEB (DFN1616, 6)	1.6mm × 1.6mm

(1) For more information, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Voltage Clamp Response to 8/20µs Surge Event

Table of Contents

4 Related Products

Device	V_{RWM} (V)	V_{CLAMP} at I_{pp} (V)	I_{PP} (8/20 µs) (A)	Leakage Current (nA)	Polarity	Package
TVS0500	5	9.2	43	0.07	Unidirectional	DRV (SON-6)
TVS0701	7	11	30	0.25	Bidirectional	DRB (SON-8)
TVS1400	14	18.4	43	2.2	Unidirectional	DRV (SON-6)
TVS1401	14	20.5	30	1.1	Bidirectional	DRB (SON-8)
TVS1800	18	22.7	40	1.2	Unidirectional	DRV (SON-6)
TVS1801	18	27.4	30	0.4	Bidirectional	DRB (SON-8)
TVS2200	22	27.6	40	3.5	Unidirectional	DRV (SON-6)
TVS2201	22	29.6	30	2	Bidirectional	DRB (SON-8)
TVS2210	22	27.6	25	6	Unidirectional	YMZ (0402)
TVS2700	27	32.5	40	1.8	Unidirectional	DRV (SON-6)
TVS2701	27	34	27	0.8	Bidirectional	DRB (SON-8)
TVS3300	33	38	35	19	Unidirectional	DRV (SON-6), YZF (WCSP)
TVS3301	33	40	27	2.5	Bidirectional	DRB (SON-8)
TVS4000	40	50.4	24	4.45	Unidirectional	VEB (DFN1616)
TVS5200	52	60.5	30	20	Unidirectional	VEB (DFN1616)
TVS5800	58	70.9	25	6	Unidirectional	VEB (DFN1616)

5 Pin Configuration and Functions

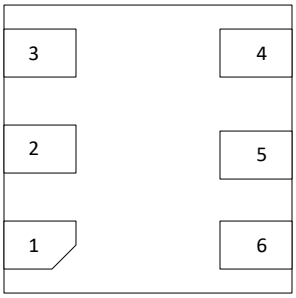


Figure 5-1. VEB Package, 6-Pin DFN1616

Table 5-1. Pin Functions

PIN		TYPE [1]	DESCRIPTION
NAME	NO.		
IN	4, 5, 6	I	ESD and surge protected channel
GND	1, 2, 3	GND	Ground

(1) I = input, GND = ground

6 Specifications

6.1 Absolute Maximum Ratings

T_A = 27°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum Surge	IEC 61000-4-5 Current (8/20µs)		30	A
	IEC 61000-4-5 Power (8/20µs)		1875	W
T_A	Ambient Operating Temperature	-40	125	°C
T_{stg}	Storage Temperature	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime

6.2 ESD Ratings - JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±15	kV
		IEC 61000-4-2 air-gap discharge	±15	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{RWM}	Reverse Stand-off Voltage			52	V

6.5 Thermal Information

THERMAL METRIC(1)		TVS5200 VEB (DFN1616) 6 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	132.1	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	61.5	°C/W
R_{qJB}	Junction-to-board thermal resistance	34.5	°C/W
Y_{JT}	Junction-to-top characterization parameter	1.04	°C/W
Y_{JB}	Junction-to-board characterization parameter	34.4	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse Stand-off Voltage		-0.5		52	V
I_{LEAK}	Leakage Current	Measured at $V_{IN} = V_{RWM}$ T_A = 27°C		25	800	nA
		Measured at $V_{IN} = V_{RWM}$ T_A = 85°C		100	1300	nA
		Measured at $V_{IN} = V_{RWM}$ T_A = 105°C		220	1500	nA
V_F	Forward Voltage	I_{IN} = 1mA from GND to IO	0.25	0.5	0.65	V
V_{BR}	Break-down Voltage	I_{IN} = 1mA from IO to GND	54			V
V_{CLAMP}	Clamp Voltage	10A IEC 61000-4-5 Surge (8/20µs) from IO to GND, V_{IN} = 0V before surge, 27°C		58.6	60	V
		20A IEC 61000-4-5 Surge (8/20µs) from IO to GND, V_{IN} = 0V before surge, 27°C		58.9	60	V
R_{DYN}	8/20µs surge dynamic resistance	Calculated from V_{CLAMP} at .5*I_{pp} and I_{pp} surge current levels, 27°C		26		mΩ
C_{IN}	Input pin capacitance	$V_{IN} = V_{RWM}$, f = 1MHz, 30mV_{pp}, IO to GND		154		pF

6.7 Typical Characteristics

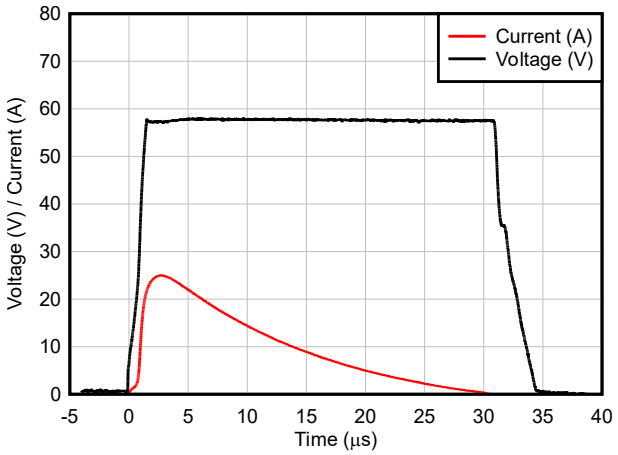


Figure 6-1. 8/20µs Surge Response at 25A

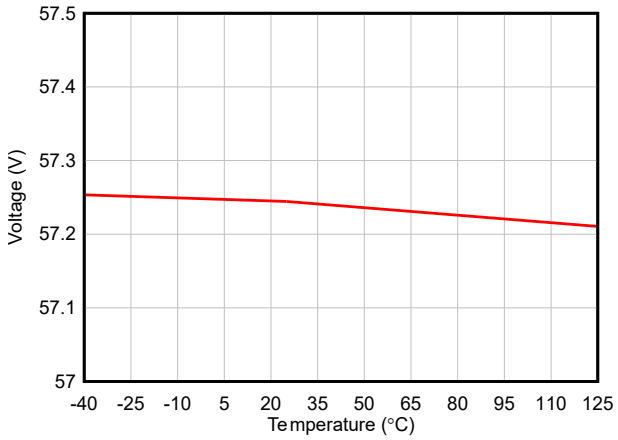


Figure 6-2. Breakdown Voltage (1mA) vs Temperature

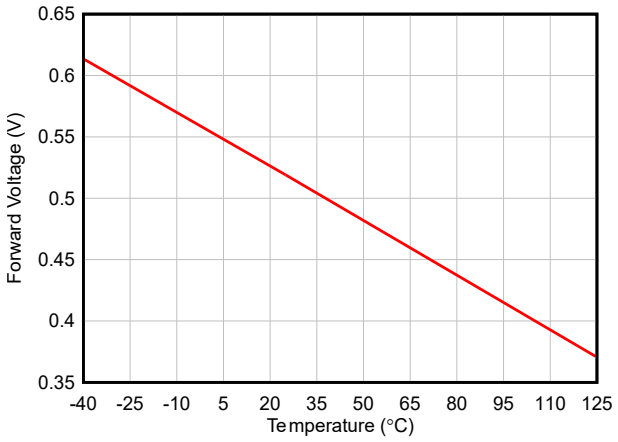


Figure 6-3. Forward Voltage vs Temperature

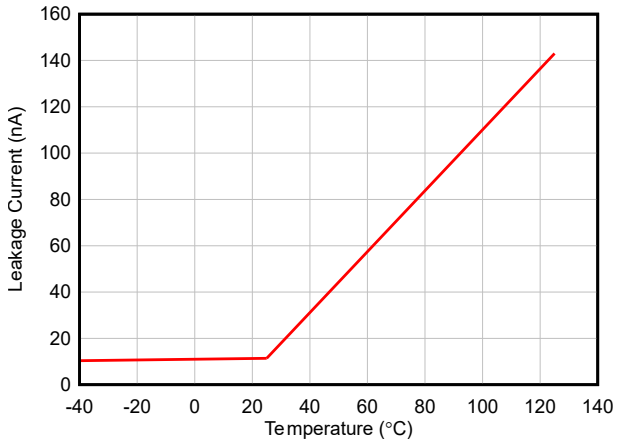


Figure 6-4. Leakage Current vs Temperature at 52V

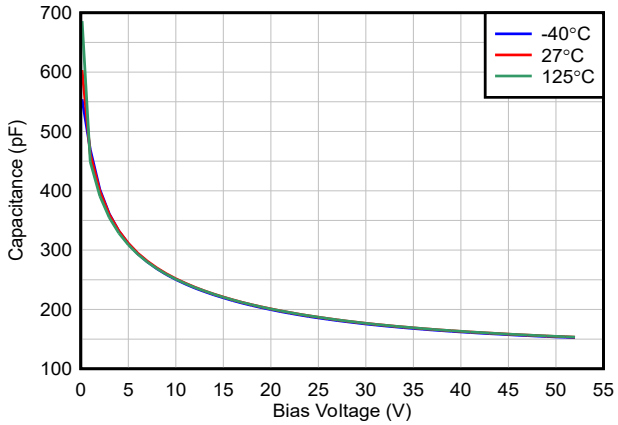


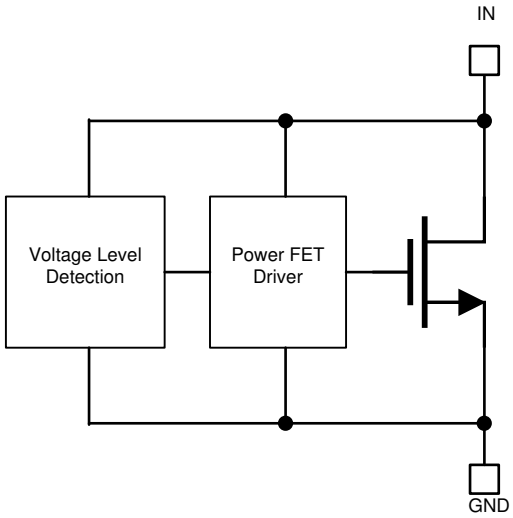
Figure 6-5. Capacitance vs Bias Voltage Across Temperature

7 Detailed Description

7.1 Overview

The TVS5200 is a precision clamp with a low, flat clamping voltage during transient overvoltage events like surge and protecting the system with zero voltage overshoot. For a detailed overview of the Flat-Clamp family of devices, please reference TI's Flat-Clamp surge protection technology for efficient system protection white paper. This document explains in detail the functional operation of the devices and how the TVS5800 impacts and improves system design.

7.2 Functional Block Diagram



7.3 Feature Description

The TVS5200 is a precision clamp that handles 30A of IEC 61000-4-5 8/20µs surge pulse. The flat clamping feature helps keep the clamping voltage very low to keep the downstream circuits from being stressed. The flat clamping feature can also help end-equipment designers save cost by opening up the possibility to use lower-cost, lower voltage tolerant downstream ICs. The TVS5200 has minimal leakage under the standoff voltage of 52V, making TVS5200an good candidate for applications where low leakage and power dissipation is a necessity. IEC 61000-4-2 ratings make TVS5200 a robust protection design for ESD events. Wide ambient temperature range of -40°C to +125°C, a good candidate for most applications. Compact packages enables the TVS5200 to be used in small devices and save board area.

7.4 Device Functional Modes

7.4.1 Protection Specifications

The TVS5200 is specified according to both the IEC 61000-4-5 standard. The IEC 61000-4-5 standard requires protection against a pulse with a rise time of 8µs and a half length of 20µs.

The TVS5200 has been tested according to IEC 61000-4-5 to pass a ±1kV surge test through a 42Ω coupling resistor and a 0.5µF capacitor. This test is a common test requirement for industrial signal I/O lines and the TVS5200 is designed as a protection option for applications with that requirement.

The TVS5200 also integrates IEC 61000-4-2 level 4 ESD Protection. These combine to maintain that the device can protect against most transient conditions regardless of length or type.

For more information on TI's test methods for Surge, ESD, and EFT testing, reference TI's IEC 61000-4x Testing Application Note

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TVS5200 can be used to protect any power, analog, or digital signal from transient fault conditions caused by the environment or other electrical components.

8.2 Typical Application

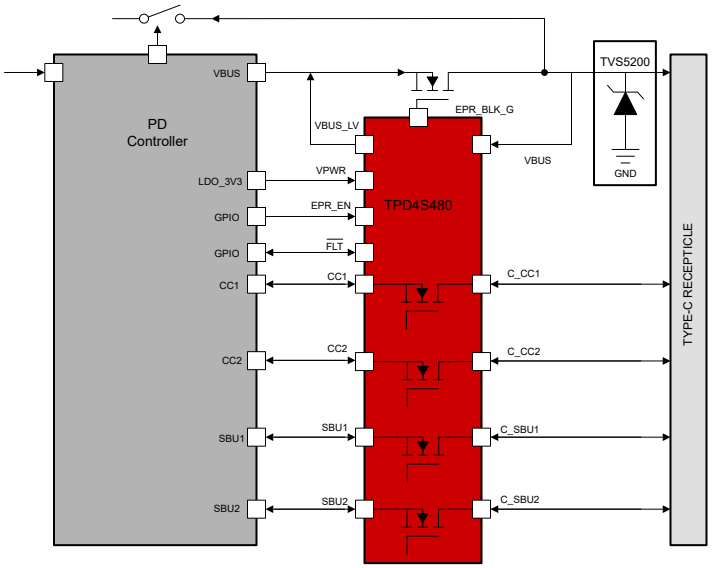


Figure 8-1. TVS5200 Application Schematic

8.2.1 Design Requirements

An application for the TVS5200 is protecting a USB Extended Power Range (EPR) Port Protector. In this example, the TVS5200 is protecting the VBUS pin of a USB Type-C® 48V EPR Port Protector such as TPD4S480, that has a nominal voltage of 48V and a clamping voltage requirement of 63V. The TVS5200 has a max clamping voltage of 60V which makes the device a great option for protection. Also, the maximum expected VBUS voltage can reach 50.9V, amounting to a 5% tolerance which means the working voltage of the TVS needs to be at or above 50.9V. For more information on the EPR Port Protector, see the TPD4S480 datasheet.

Most industrial interfaces such as this require protection against ±1kV surge test through a 42Ω coupling resistor and a 0.5µF capacitor, equaling roughly 24A of surge current. Without any input protection, if a surge event is caused by lightning, coupling, ringing, or any other fault condition this input voltage can rise to hundreds of volts for multiple microseconds, violating the absolute maximum input voltage and harming the device. An optimal surge protection diode maximizes the useable voltage range while still clamping at a safe level for the system, TI's Flat-Clamp technology provides the best protection option.

8.2.2 Detailed Design Procedure

If the TVS5200 is in place to protect the device, during a surge event the voltage rises to the breakdown of the diode at V, and then the TVS5200 turns on, shunting the surge current to ground. With the low dynamic resistance of the TVS5200, large amounts of surge current has minimal impact on the clamping voltage. The

dynamic resistance of the TVS5200 is around 26mΩ, which means 30A of surge current causes a voltage raise of 30A × 26mΩ = 0.78V. Because the device turns on at 57.8V, this means the TPD4S480 input is exposed to a maximum of 57.8V + 0.78V = 58.6V during surge pulses. This maintains robust protection of your circuit.

The small size of the device also improves fault protection by lowering the effect of fault current coupling onto neighboring traces. The small form factor of the TVS5200 allows the device to be placed extremely close to the input connector, lowering the length of the path fault current takes through the system compared to larger protection options.

8.3 Power Supply Recommendations

The TVS5200 is a clamping device so there is no need to power the device. To verify that the device functions properly do not violate the recommended V_{IN} voltage range (0V to 52V) .

8.4 Layout

8.4.1 Layout Guidelines

The optimum placement is close to the connector. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.

Route the protected traces straight. Eliminate any sharp corners on the protected traces between the TVS5200 and the connector by using rounded corners with the largest radii possible. Electric fields tend to build up on corners, increasing EMI coupling.

8.4.2 Layout Example

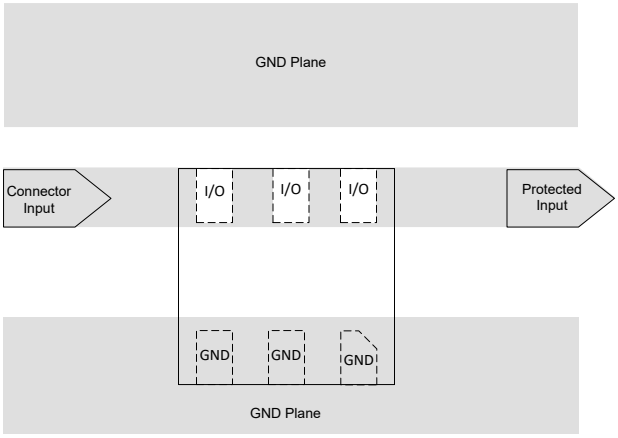


Figure 8-2. TVS5200 DFN1616 Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Flat-Clamp TVS Evaluation Kit*
- Texas Instruments, *How to select a Surge Diode*
- Texas Instruments, *Flat-Clamp surge protection technology for efficient system protection*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

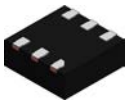
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

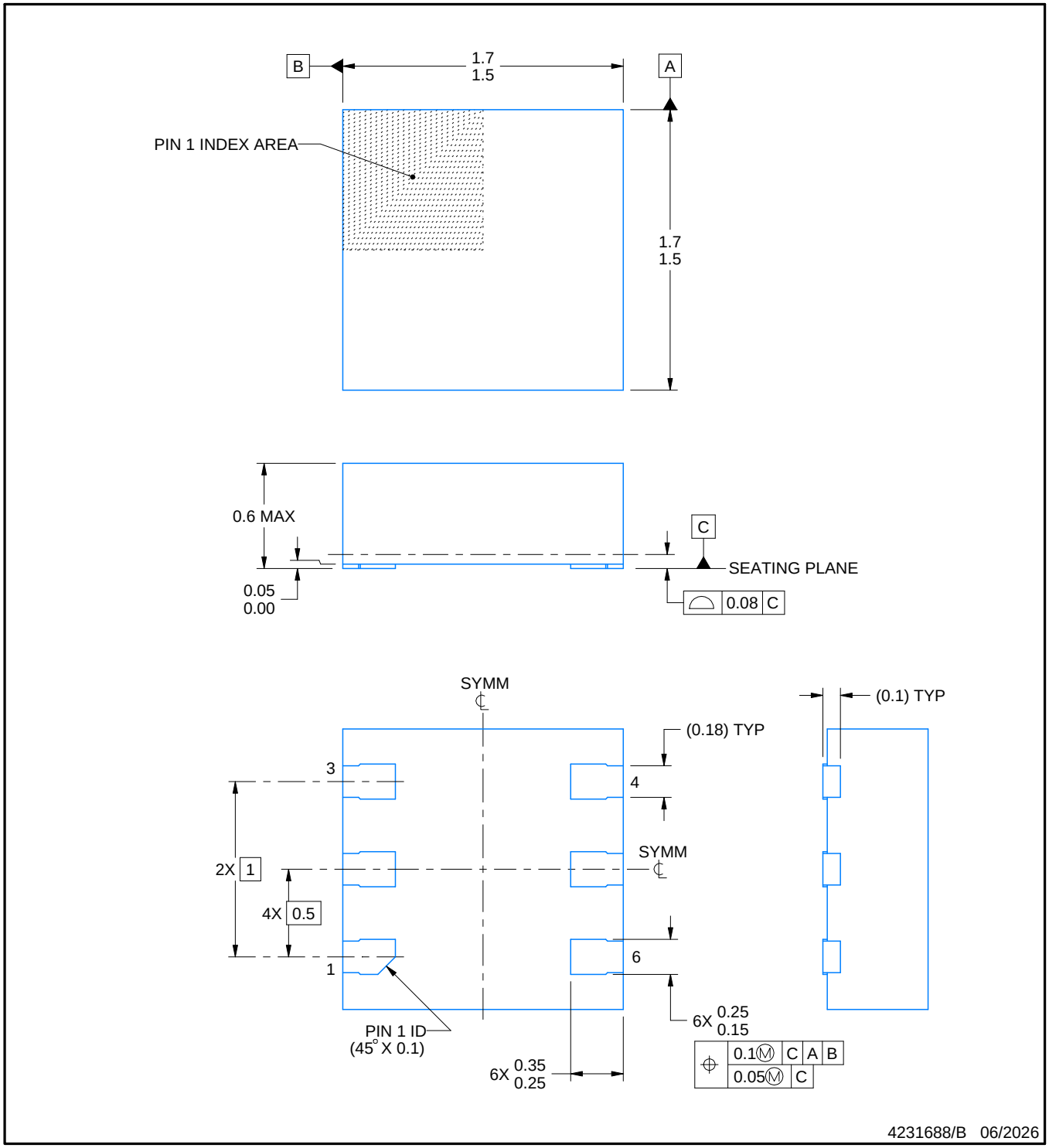
VEB0006A



PACKAGE OUTLINE

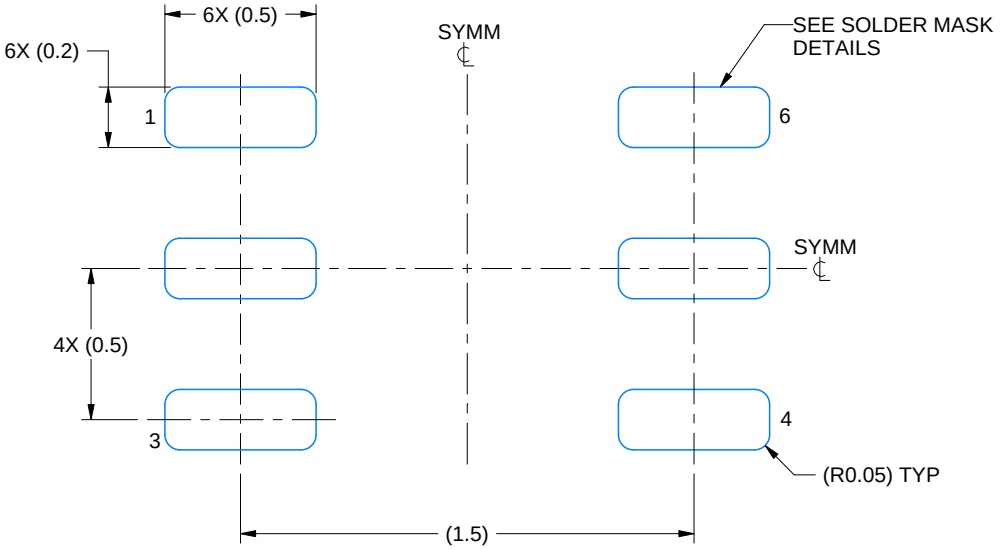
UQFN-HR - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

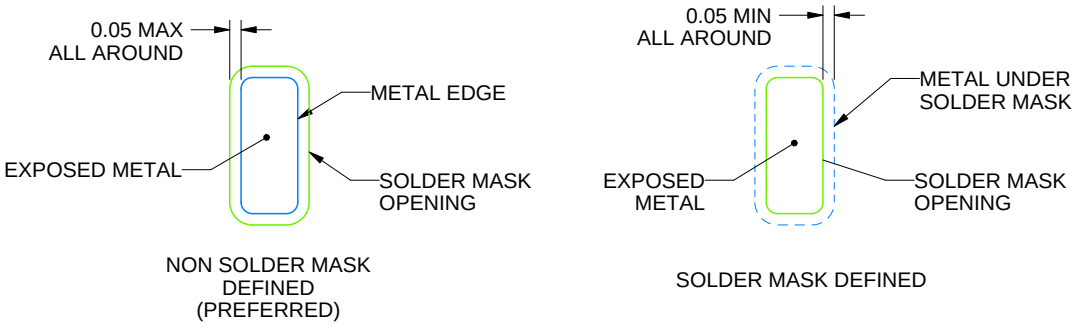


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS

4231688/B 06/2026

NOTES: (continued)

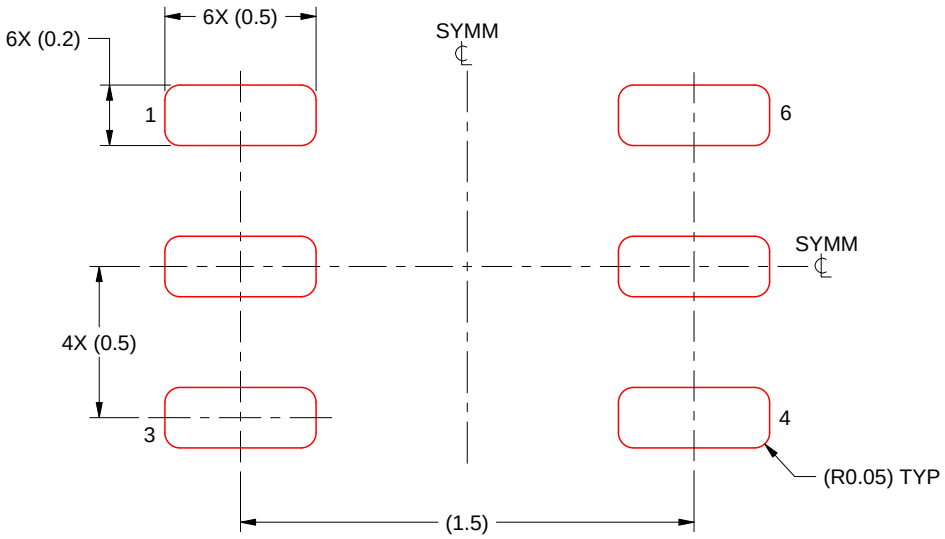
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VEB0006A

UQFN-HR - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 40X

4231688/B 06/2026

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025